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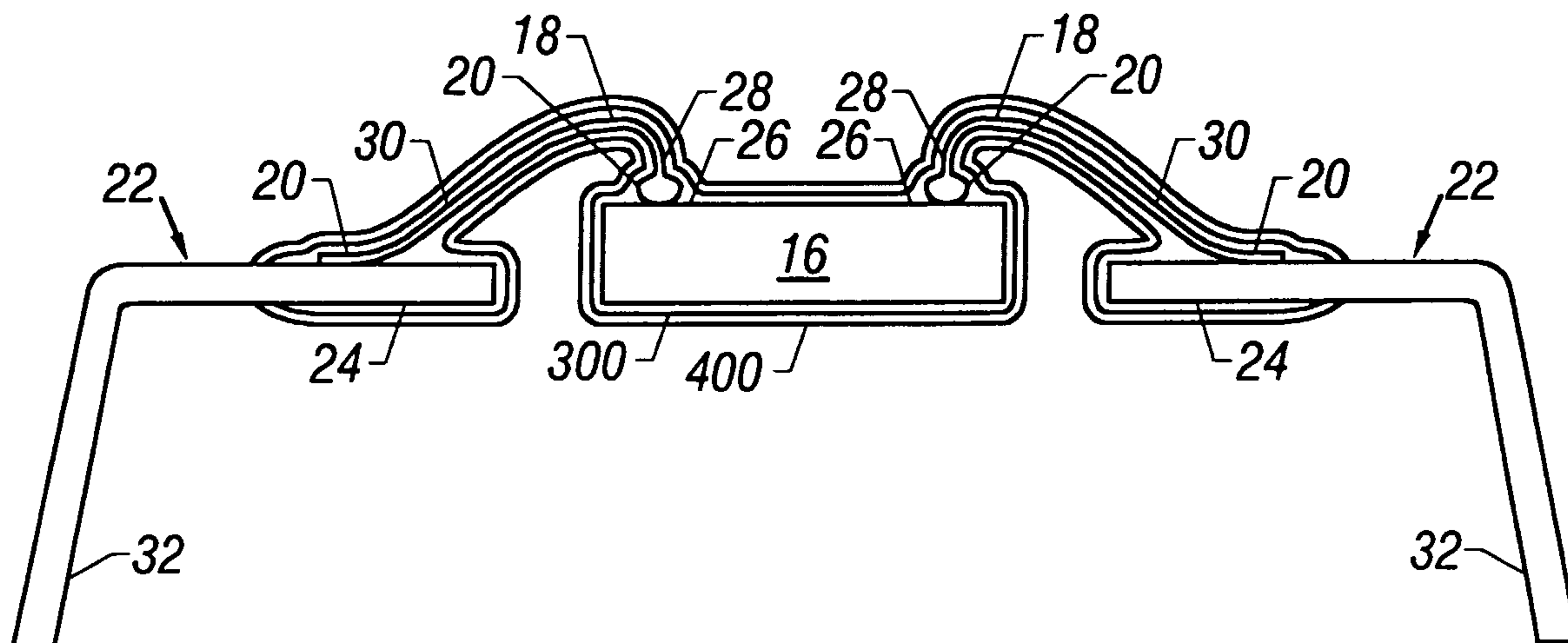

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A hermetically coated device (10) includes an integrated semiconductor circuit die (16), a first layer comprising an inorganic material, the first layer (300) enveloping the integrated circuit die (16), a second layer (400), the second layer (400) enveloping the integrated semiconductor circuit die (16). Formation of such device includes steps of providing an integrated semiconductor circuit die (16), applying a first layer (300) comprising an inorganic material, the first layer (300) enveloping integrated semiconductor circuit die (16), and applying a second layer (400), the second layer (400) enveloping the integrated semiconductor circuit die (16).

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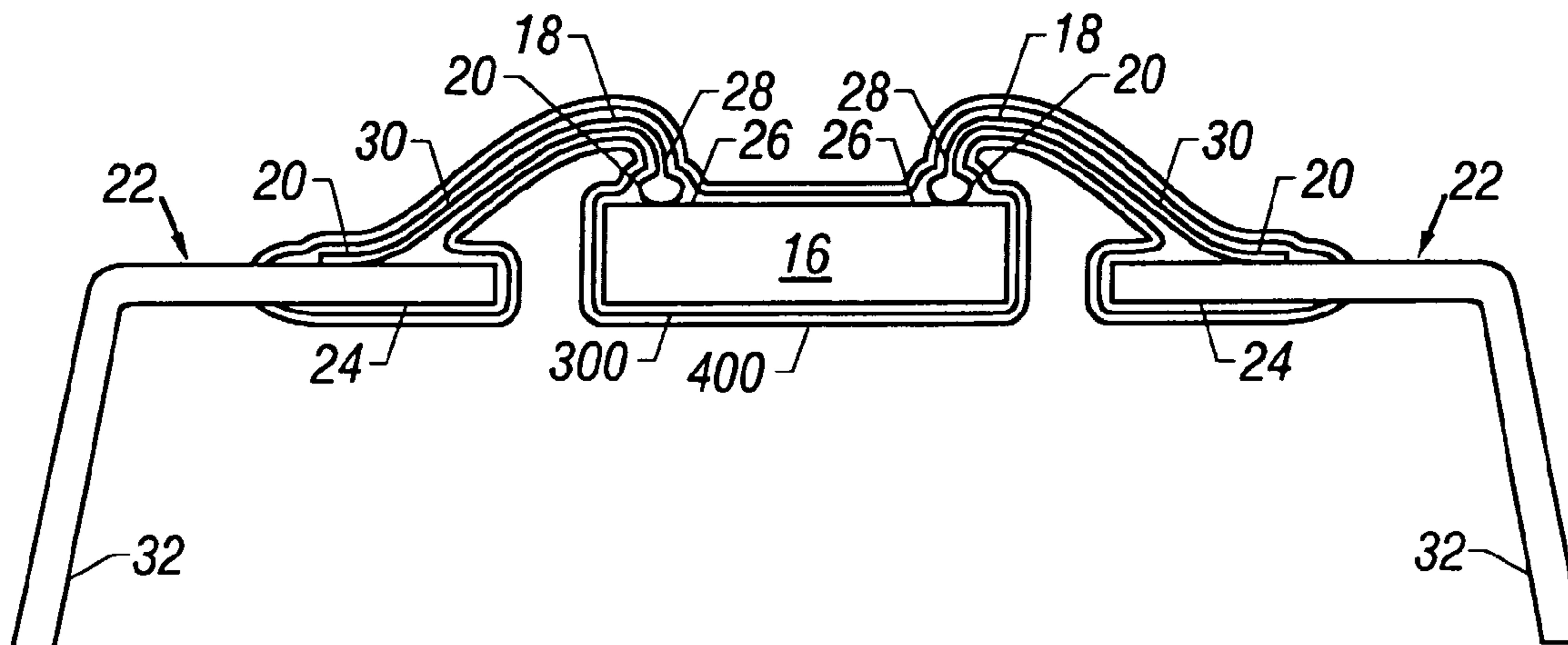

(57) Abstract: A hermetically coated device (10) includes an integrated semiconductor circuit die (16), a first layer comprising an inorganic material, the first layer (300) enveloping the integrated circuit die (16), a second layer (400), the second layer (400) enveloping the integrated semiconductor circuit die (16). Formation of such device includes steps of providing an integrated semiconductor circuit die (16), applying a first layer (300) comprising an inorganic material, the first layer (300) enveloping integrated semiconductor circuit die (16), and applying a second layer (400), the second layer (400) enveloping the integrated semiconductor circuit die (16).

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ELECTRONIC DEVICE PACKAGING

5 **BACKGROUND OF THE INVENTION**

The present invention relates to electronic device packaging, and more particularly to hermetic packaging at electronic devices. Even more particularly, the present invention relates to multilayer hermetic
10 coating in electronic device packaging.

Integrated semiconductor circuits are critical devices in most electronic systems today. These integrated semiconductor circuits have been broadly used in a variety of fields. Historically, two versions of
15 many integrated semiconductor circuits were designed by manufacturers, one packaged in a non-hermetic plastic package (plastic packaged microelectronics (PEM) device), such as molded epoxy, silicone or phenolic; and another packaged in a hermetic ceramic package. The hermetic
20 ceramic packages were typically used in very sensitive, harsh environment and/or high reliability applications, such as military applications, including weapon systems; space applications, such as for use on Earth space orbit satellites; aerospace applications; ruggedized commercial
25 and medical applications; and transportation applications, such as automotive and avionics applications.

One problem heretofore addressed by hermetic ceramic packages was to prevent the invasion of moisture,
30 ions and other impurities, including oxygen, into critical portions of the package, for example, wire bond sites, and into an integrated semiconductor circuit die. This invasion of impurities can cause oxidation and other erosion of the integrity of the affected structures
35 thereby causing failure of the device. This invasion takes place readily in plastic package devices through cracks or gaps occurring in the molding and in some cases through diffusion through the plastic itself, both of

which form paths from an outside environment to the packages contents.

Problematically, in recent years, device manufacturers, for economic reasons, have ceased production of ceramic package devices, thus leaving entities in need of high reliability devices for sensitive applications without a suitable device for their application. Microelectronics are highly susceptible to gases, chemicals and particulates that invade plastic package devices. Pitfalls associated with this sensitivity can include: moisture causing corrosion; chemicals destroying wire bonds, internal circuitry and other pertinent aspects of the device. Further, before a package is added to a device, particulates present in injection molded or otherwise manufactured packages are capable of scratching the surface of the integrated semiconductor circuit die, potentially breaking wire bonds and causing shorts/opens inside the device, and are capable of reacting with or corroding the wire bonds, wires, leads or integrated semiconductor circuit die.

Thus, hermetically sealed packages are required for many applications where contaminants can jeopardize the functional integrity of the device, or where long-term reliability and/or operation in extreme environments are required.

As mentioned above heretofore, the current solution to these issues has been to use ceramic package devices. Ceramic packaging technology provides the hermetic sealing and long-term reliability required by many entities. However, the downfall of these packages has been that they are more expensive than similar plastic packages, tend to weigh more, and require specialized manufacturing equipment to produce. Although, the ceramic package device does effectively address the issue of hermeticity, the ceramic package device frequently provides a level of reliability and ruggedness that exceeds the levels actually required for most applications.

In contrast, the main advantage of plastic package devices is their ability to be mass-produced more cheaply and more easily than other currently available technologies. However, unlike with ceramic package devices, the largest percentages of failures in plastic package devices can be directly or indirectly related to their inherent lack of hermeticity and to the manufacturing techniques employed. Current users of plastic package devices in high-reliability applications are either incurring higher costs for maintenance of inferior products or suffering from a lack of long-term reliability.

A further advantage of plastic package devices is their abilities to operate at higher frequencies due to the lower dielectric constant of plastic, as compared to ceramic. Also, smaller sizes achievable in plastic package devices enables components to be placed closer together, thereby reducing propagation delays. Further, copper leads in plastic package devices have better electrical and thermal conductivity than KOVAR alloy that is used in the leads of ceramic package devices.

Ceramic package devices perform more consistently at high frequency than plastic package devices because moisture in the plastic can vary, changing the dielectric constant of the package and altering the operating speed of the integrated semiconductor circuit die.

Flexibility in low stress plastic formulations is gained at the expense of increased permeability due to the addition of plasticizers.

An alternative to ceramic package devices employs "wafer-level" coating of the integrated semiconductor circuit die itself, which adds yet more complexity to the manufacturing process, and brings with it engineering challenges as well. The die level application of the coating increases the hermetically of the integrated semiconductor circuit die as well as the structural reliability of the device at a lower cost and

in a manner that can be integrated into current production facilities. Unfortunately, this process must be performed as a fabrication step, before the integrated semiconductor circuit die is cut form the wafer, and thus requires altering "fab" processes. Problematically, once the integrated semiconductor circuit die is cut from the water, edges of the integrated semiconductor circuit die remain exposed and susceptible to contaminants. Furthermore, bonding pads on the surface of the integrated semiconductor circuit die must be exposed (for wire bonding for example) and thus create a further point of susceptibility to contamination. And, disadvantageously, this approach does nothing to protect the wires or wire bonds, a common point of contamination-caused failure. U.S. Patent No. 5,780,163, issued to Camilletti et al., provides an example of "water-level" coating.

Hermetic coatings have also been applied to the integrated semiconductor circuit die and wire bonds after the die is attached to a die attach substrate and the wires are wire bonded to the integrated semi-conductor circuit die and leads. These hermetic coatings use plasma chemical vapor deposition of silicon nitride to prevent moisture from contaminating the device. This process can also be done to deposit diamond like carbon, silicon oxide and other insulating materials. One example of this type of hermetic coating is shown in U.S. Patent No. 5,096,851, issued to Yamazaki et al.

Single layer PARYLENE coatings (pary-xylylene) have been applied to the integrated semiconductor circuit die and wire bonds prior to packaging for the purpose of allowing for distortion of the wire bonds without short circuiting and reducing the requirements for high tolerances associated with relatively short length wires. U.S. Patent No. 5,824,568, issued to Zechmans describes single layer PARYLENE coatings.

Bi-layer and tri-layer coating technologies have also been developed to provide moisture and oxygen

barriers using including parylene/BCB/SiO2, parylene/A1203, and parylene/SiO2. In these approaches, a PARYLENE layer is first applied, and then one or more subsequent ceramic layers are applied.

5

SUMMARY OF THE INVENTION

The present invention advantageously provides an approach for hermetic packaging of integrated semiconductor circuits.

10 The present invention can be characterized in one embodiment as a hermetically coated device comprising an integrated semiconductor circuit die; a first layer comprising an inorganic material, the first layer enveloping the integrated semiconductor circuit die; and 15 a second layer, the second layer enveloping the integrated semiconductor circuit die.

In a further embodiment, the present invention can be characterized as a method of making a hermetically coated device. The method comprises providing an 20 integrated semiconductor circuit die; applying a first layer comprising an inorganic material, the first layer enveloping the integrated semiconductor circuit die; and applying a second layer, the second layer enveloping the integrated semiconductor circuit die.

25

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects, features and advantages of the present invention will be more apparent from the following more particular description thereof, 30 presented in conjunction with the following drawings wherein:

FIG. 1A is a cross-sectional view illustrative of a typical plastic package device, including a plastic package, a die attach substrate, an integrated 35 semiconductor circuit die, wires, wire bonds and leads;

FIG. 1B is a partial cross sectional view of a plastic package device, such as in FIG. 1, showing

failure modes that affect such plastic package device due to a lack of hermeticity;

FIG. 2 is a cross-sectional view illustrative of a die/wire/lead structure such as may be assembled
5 prior to application of duplex coatings in accordance with a first embodiment of the present invention;

FIG. 3 is a cross-sectional view showing the die/wire/lead structure with an inorganic coating applied thereover;

10 FIG. 4 is a cross-sectional view showing the die/wire/lead structure with the inorganic coating applied over the die/wire/lead structure applied over the inorganic coating;

FIG. 5 is a cross-sectional view showing the
15 die/wire/lead structure with duplex coatings, i.e., the inorganic coating with the organic coating thereover, having been enclosed in a plastic package;

FIG. 6 is a flowchart illustrating the method applied in FIGS. 2 through 5;

20 FIG. 7 is a cross-sectional view showing a plastic packaged device, the die attach substrate, including the plastic package, integrated semiconductor circuit die, the wires and the leads within the plastic package, having been encapsulated by an inorganic
25 coating;

FIG. 8 is a cross-sectional view showing the die/substrate/wire/lead/package structure with the inorganic coating encapsulating the die/substrate/wire/lead/package structure and an organic
30 coating applied over the inorganic coating;

FIG. 9 shows a flowchart outlining the steps applied in FIGS. 7 through 9; and

FIG. 10 is a perspective assembly view of one variation of a plastic case that benefits from the
35 embodiments of FIGS. 2 through 8;

FIG. 11 is a perspective assembly view of another variation of the plastic case of FIG. 10;

FIG. 12 is a perspective view, partially in cross section, of a variation of a plastic package device showing a die/wire/lead structure with an inorganic coating encapsulating the die/wire/lead structure, with
5 an organic coating applied thereover, such as in FIG. 4, and further showing the due/wire/lead structure packaged within a plastic package, such as in FIG. 5, forming a die/substrate/wire/lead/package structure, the die/substrate/wire/lead/package structure being shown
10 with another inorganic coating encapsulating the die/substrate/wire/lead/package structure and another organic coating applied over the other inorganic coating, such as in FIG. 8.

Corresponding reference characters indicate
15 corresponding components throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following description of the presently
20 contemplated best mode of practicing the invention is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention. The scope of the invention should be determined with reference to the claims.

25 Referring first to FIG. 1A, a cross-sectional view is shown of a plastic package structure (or plastic encapsulated microelectronic (PEM) device), including the plastic package, a die attach substrate, an integrated semiconductor circuit die, wires, wire bonds and leads.
30 In practice, as is well known in the art, the leads form part of a lead frame prior to assembly of the plastic package structure. The lead frame holds and aligns the leads until the leads are encapsulated at respective interior ends of the leads by the plastic package.

35 Prior to encapsulation, the die and die attach substrate are positioned near a center of the lead frame, near the interior ends of the leads, and wire bonds are formed in a conventional manner, such as by ultrasonic

bonding, between bond pads on the integrated semiconductor circuit die, and the interior ends of the leads. These wire bonds are formed by bonding a first end of each of the wires to a respective bond pad on the
5 dye, and by bonding a second end of each of the wires to s respective one of the interior ends of the leads.

Once all of the wires are bonded to the respective bond pads and interior ends of the leads, the resulting structure (such as is shown in FIG. 2) is
10 encapsulated in the plastic package, such as by injection molding. This encapsulation of the resulting structure includes leaving exterior ends of the leads exposed and protruding from the plastic package, so that the are available for connection to an electrical system, such as
15 by soldering the exterior ends of the leads to a printed circuit board. During this injection molding process some movement of the free portions of the wires, i.e., middle portions, is typical.

As will be appreciated by the skilled artisan,
20 the above description of the assembly process for a plastic package system, or plastic package integrated circuit device, represents just one plastic package device known in the art, a dual inline pin device. Many other examples, such as flip-chip devices, ball grid
25 array devices, pin grid array devices, bottom chip carrier devices, leaded chip carrier devices, leadless chip carrier devices, quad-flat pack devices, thin quad-flat pack devices, chip carrier J-bend devices, single inline pin devices, DIL-bent-SIL devices, very small
30 peripheral array devices, chip scale packaging devices, and numerous similar devices, all benefit from the advantageous techniques described herein below. Thus, the plastic packed integrated semiconductor circuit of FIG., and the examples described below, should be appreciated
35 as just that, examples.

Problematically, the above-described plastic packaged integrated semiconductor circuit is susceptible to the infusion and moisture and other contaminants, such

as oxygen, which can cause the corrosio
the wires, the wire bonds, and the integrated semiconductor circuit die. These contaminants enter the plastic package through cracks, such as may for between the plastic package and the exterior ends of the leads where the exterior ends of the leads exit the plastic package; and in some cases may enter by diffusing through the plastic package itself.

Referring to FIG. 1B, a partial cross section view is shown illustrating various failure modes addressed by the embodiments described herein. These include infiltration of moisture and ions through the plastic package, package delamination, chemical contamination from agents in the plastic package, ball bond fracture, package cracks, and the like.

One of the major paths for moisture ingress in all plastic package devices is where the leads exit the plastic package. The adhesion between the metal and plastic is not good, partly because of release agents added to the resin to ease in the removal of the cured parts from the transfer mold. The narrow gap caused by this metal/plastic separation results in high capillary forces that can draw moisture into the package, along the bond wires and finally to the die. Sealing this gap effectively has proven difficult since flexing the lead, or heating the lead during soldering can break this tenuous seal.

FIGS. 2 through 6 below represent one approach in accordance with the teachings herein to hermetically sealing the integrated semiconductor circuit die, wires, and wire bonds so as to prevent the infusion of contaminants, and thus contamination and ultimately failure of the plastic packaged system.

Referring next to FIG. 2 (and step ___ in FIG. 6), shown is an assembly made up of the die, the wires, the wire bonds and the leads (which, as mentioned above are, at this point, part of a lead frame. This assembly,

such as may be used in the plastic package system of FIG. 1 is also one possible starting point for the present embodiments.

As can be seen, the wires are connected electrically between respective bonding pads on an upper surface of the integrated semiconductor circuit die and respective leads of the lead frame.

The bonding of the wires to the bonding pads and to the leads may be achieved in a conventional manner using, for example, ultrasonic bonding techniques, as are well known in the art.

Referring next to FIG. 3 (and step ___ in FIG. 6), shown is an assembly made up of the integrated semiconductor circuit die, the wires, the wire bonds and the leads. Also shown is a first layer of a duplex coating. The first layer of the duplex coating is a layer of an inorganic ceramic-like material applied so as to encapsulate the integrated semiconductor circuit die, the wire bonds, the wires, and the interior ends of the leads.

Encapsulation of the integrated semiconductor circuit die, the wires, the wire bonds and the leads with the first layer of the duplex coating, i.e., the inorganic ceramic like material, is preferably effected by non-line-of-sight processes such as CVD, PECVD, metalorganic chemical vapor deposition and sputtering at temperatures below approximately 300C. Sol-gel technology may be used but is inferior in that the material application may damage some of the components. The preferred techniques use a low pressure chamber with the chemicals introduced in a vapor phase, although other approaches are contemplated, such as atmospheric pressure processes.

One process that can be used to encapsulate the integrated semiconductor circuit die (or the plastic package device, or both, as described further hereinbelow) is atomic layer deposition (ALD). This technique achieves an impermeable ceramic coating at low

temperatures without the use of plasma, which may damage or destroy the integrated semiconductor circuit die. Corrosion is addressed by using phosphorus and halogen-free precursors. Pinholes, a problem with some other chemical vapor deposition methods, cannot be propagated by this technique. The atomic layer deposition has processing temperatures in the range of 150 - 250°C and intrinsic precise layer thickness control at the atomic scale.

Atomic layer deposition (ALD) and atomic layer epitaxial (ALE), and their companion technique metalorganic chemical vapor deposition (MOCVD), are well suited to producing layered structures, either epitaxial or non-epitaxial. Metalorganic chemical vapor deposition can also deposit thicker monolithic layers. A large number of materials can be deposited by these techniques. Dielectrics which may be deposited by atomic layer epitaxial (ALE) in polycrystalline or amorphous form are aluminum nitride, silicon nitride, silicon carbide, alumina, titania, zirconia, hafnia, silica, magnesia, yttria, ceria, niobium oxide, tantalum oxide, lanthanum oxide, strontium titanate and barium titanate.

Thin-film technology makes it possible to deposit a very thin (down to a few atoms in thickness) layer of material on a substrate or surface. With proper system design, both metalorganic chemical vapor deposition and atomic layer epitaxial modes can be carried out in the same deposition system. The thin films grown by the metalorganic chemical vapor deposition technique are either textured polycrystalline or epitaxial single crystal depending on the substrates used.

Atomic layer epitaxy (ALE) is a special modification of the chemical vapor deposition technique for depositing thin films and related surface structures. The unique feature of atomic layer epitaxial is the self-limiting film growth mechanism which gives it a number of attractive properties, like accurate and simple film

thickness control, sharp interfaces, uniformity over large areas, excellent conformality, good reproducibility, multilayer processing capability, and high film qualities at relatively low temperatures.
5 Other than being able to deposit the particular preferred materials for the barrier layer, other aspects of the process justify its selection. Specifically, this process is able to uniformly deposit coatings over large areas with excellent conformity and good reproducibility.
10 Thickness control is simple and precise since the deposition is `pulsed' and each pulse deposits the same thickness increment. High quality films can be deposited at low temperatures. There is a downside, in that the deposition rate is low (less than 5000A/hr) but the
15 quality of the film may be so high that thinner layers are as effective as thick layers from `cruder' processes. However, since this is a gaseous-based process, large volumes of materials can be uniformly coated at one time, so the throughput in terms of the number of parts coated
20 per hour could be competitive or better than other techniques that are more difficult to scale up.

The metalorganic chemical vapor deposition technique uses liquid metalorganic precursors which vaporize in a carrier gas stream before reaching the
25 substrate surface. The carrier gas can be either oxidizing (air, oxygen) or non-oxidizing such as hydrogen, nitrogen or argon. The formation of the desired compound occurs via the pyrolysis of the metalorganics and the subsequent recombination of the
30 atomic or molecular species at or near the heated substrate. Liquid metalorganic precursors with relatively high vapor pressures are preferred if they are safe, especially if no toxic byproducts are produced. In metalorganic chemical vapor deposition, the deposition
35 rates can be as high as 10 μm/h. The metalorganic chemical vapor deposition chamber can be optimized to deposit over large areas.

As a further alternative, open-atmosphere

combustion chemical vapor deposition (CCVD) technology may be used. Advantages include an order-of-magnitude reduction in operating and capital costs, improved materials quality and performance characteristics, and the ability to tailor-make materials for specific applications (including multi-layered structures). In addition, combustion chemical vapor deposition's relative ease-of-use permits rapid development of new coating/substrate combinations.

The combustion chemical vapor deposition (CCVD) process has demonstrated its potential to address the aforementioned requirements. Combustion chemical vapor deposition technology has significant promise to overcome many of the shortcomings of traditional vapor deposition techniques while yielding equal and/or better quality coatings at a lower cost.

One advantage of the CCVD technology is its ability to deposit thin films in the open atmosphere using inexpensive precursor chemicals in solution. This obviates the need for costly furnaces, vacuum equipment, reaction chambers, and post-deposition treatment (e.g. annealing). As a result, capital requirements and operating costs are reduced at least tenfold when compared to competing vacuum-based technologies (e.g. sputtering and metalorganic chemical vapor deposition). The ability to deposit thin films in the open atmosphere enables continuous, production-line manufacturing. Consequently, throughput potential is far greater than with conventional thin-film technologies, most of which are generally restricted to batch processing.

In practice, precursors are dissolved in a solvent, which typically also acts as the combustible fuel. This solution is atomized to form submicron droplets by means of NANOMISER technology, owned by MCT. The droplets are then convected by an oxygen stream to a flame where they are combusted. A substrate is coated by simply drawing it over the flame plasma. The heat from the flame provides the energy required to evaporate the

droplets and for the precursors to reac
on the substrates. Although flame temperatures can be in excess of 800 °C, the substrate may dwell in the flame zone only briefly thus remaining cool (< 100 °C).
5 Alternatively, the substrate can be actively cooled. Substrate temperature is therefore an independent process parameter that can be varied to actively control the film's microstructure. The process generally takes no more than two hours from set-up to post-deposition
10 cleaning. Multiple experimental runs using the same solution require less than 30 additional minutes per run. Therefore, coatings and their properties can be optimized quickly in an iterative manner. Combustion chemical vapor deposition technology is drastically different from spray
15 pyrolysis: in spray pyrolysis, a liquid-vapor mixture is sprayed onto a heated substrate, while combustion chemical vapor deposition atomizes a precursor solution into sub-micron droplets followed by vaporization of said droplets. Thus, CCVD qualifies as a true vapor deposition
20 process.

By adjusting solution concentrations and constituents, a wide range of coating stoichiometries and compositions can be achieved. This is especially valuable for achieving the desired composition and thin film
25 characteristics. Conventional chemical vapor deposition requires precursors with sufficiently high vapor pressures. This frequently necessitates the use of expensive materials and often produces toxic fumes which must be carefully treated ("scrubbed"). In contrast, the
30 combustion chemical vapor deposition technique uses inexpensive, soluble precursors that do not need to have a high vapor pressure. Hence, precursors for the combustion chemical vapor deposition process tend to be between 10 and 100 times less expensive than those used
35 in traditional chemical vapor deposition processes. Physical structure and chemical composition of the deposited films can be tailored to the specific

application requirements.

The combustion chemical vapor deposition process is well-suited for high-rate deposition (up to 1 μm/min.) of dielectrics such as SiO_2.

5 As yet a further alternative, diamond-like carbon (DLC) shows a great deal of promise. It can be deposited to present either a hydrophobic or a hydrophilic surface to the 'outside world'.

The exterior ends of the leads, where 10 electrical contact will subsequently be made, are masked against coating or the coating can be mechanically removed from these areas afterwards.

Masking can be tedious and time consuming and will have to be done correctly since the proposed coating 15 methods are capable of depositing on minute unmasked areas. GORE-TEX in a fluorocarbon foam tape that conforms by flowing tightly around irregular surfaces (such as rectangular cross section leads on integrated semiconductor circuit die devices) when compressed may be 20 used as a masking material. This material may be too expensive, however, unless it can be sufficiently reusable. Reusable cast rubber molds (commercially available to protect connectors during soldering operations) can provide a more cost effective 25 alternative, as can polyamide tape, laytex tape, organic maskants, metal masks, rubber masks, and plastic masks.

Mechanical or chemical stripping of the coating on the contacts is also an option. A UV laser may provide one mechanism for stripping the coating, by ablating the 30 coating from the leads.

Any ceramic or glassy material is suitable as the first layer of the duplex coating. Preferably the material should be electrically insulating, e.g., greeter than 10^8 ohm-meters; able to be deposited as a conformal 35 film around all the constituent assembled parts of the device; able to be deposited as an essentially pin-hole-free coating, e.g., having a moisture permeability of less than 10^{-10} g/cm-sec-torr; able to be deposited at a

temperature low enough to avoid detrimental effects to the device and constituents, e.g., at less than 300 °C for 0.1 hours, or equivalent energy input; adherent to the constituent parts of the device so as to resist or prevent delamination or blistering during use of the plastic package device in the presence of moisture, ions and thermal cycling; impervious to moisture, alkali metal ions and halogen ions; non-reactive and otherwise compatible (electrically, physically and mechanically) to the constituent parts of the device and to subsequent processing.

Preferred ceramic materials are oxide ceramics (including alumina, titania and zirconia) silicon-based ceramics (including silicon nitride, silicon oxide and silicon oxynitrides) and diamond-like carbons in amorphous or crystalline forms.

Any thickness able to reliably produce a coherent, essentially pin-hole-free film is satisfactory (typically in excess of 500-1000 Angstroms). Thicker films improve the degree of hermeticity (unless they self-destruct from internal stresses). 5000-10,000 Angstroms is a practical upper limit for economic reasons.

Referring next to FIG. 4 (and step ___ in FIG. 6), shown is an assembly made up of the integrated semiconductor circuit die, the wires, the wire bonds, the leads, and the first later of the duplex coating. Also shown is a second layer of the duplex coating. The second layer of the duplex coating is a layer of an organic overcoat applied so as to encapsulate the integrated semiconductor circuit die, the wire bonds, the wires, the interior ends of the leads, and the first layer of the duplex coating.

Encapsulation of the integrated semiconductor circuit die, the wires, the wire bonds, the leads and the first layer of the duplex coating with the second layer of the duplex coating, i.e., the organic overcoat is

preferably effected by applying a layer of PARYLENE C, a form of pary-xylylene.

PARYLENE C has many ideal properties for this part of the duplex coating. Other PARYLENE formulations may also be suitable in various embodiments. The thickness of the coating should preferably be optimized. Thicker coatings will increase the rigidity of the bond wires, be a better cushion against the abrasive and stress effects of the molding compound and provide better physical protection of the ceramic layer. However, thicker coatings are more expensive to apply and will reduce the heat dissipation of the die through the package when applied internally.

As an alternative, a new class of materials offers such an alternative, sol-gel hybrids (or sol-gel derivative materials, or fluoropolymer-silica hybrids), which differ significantly from conventional sol-gels. These materials may be applied thick enough to act as a compliant layer or external scratch resistant layer as an alternative to PAYLENE, since they should have a significantly lower permeability and be harder than PARYLENE. Sol-gel hybrid coatings can also be applied as a hard thin layer, one that may even qualify as a barrier layer, but also as a leveling layer, should one become necessary or desirable before application of the first layer. As a leveling layer, it should be far superior to FOx (flowable oxide) since it can be cured in minutes at 40 to 80°C in air as opposed to hours at 250-450°C or higher (in a nitrogen atmosphere) for the FOx coating.

The fluoropolymer-silica hybrids are a new generation of super-adherent coatings having the combined properties of the constituent coating materials: good chemical and excellent water resistance, polymer flexibility, hydrophobicity (water repellency), low surface energy, low dielectric constant and thermal stability (above 200 °C), combined with high transparency, hardness and mechanical strength of the silica network

Note that while in the figure shown herein the second layer extends beyond the first play, such layers may not overlap in practice so that masking efficiency can be achieved, i.e., so that the mask does not have to be removed and repositioned between coatings.

The exterior ends of the leads, where electrical contact will subsequently be made, are masked against coating or the coating can be mechanically removed from these areas afterwards. Masking techniques are described above in reference to the first layer and are substantially the same for the second layer.

Note that while in the figure shown herein the second layer extends beyond the first play, such layers may not overlap in practice so that masking efficiency can be achieved, i.e., so that the mask does not have to be removed and repositioned between coatings.

The inorganic ceramic-like material of the first layer of the duplex coating serves as a primary barrier layer to moisture and ionic contamination. The organic overcoat of the second layer of the duplex coating also has some barrier properties but it also provides a physical protective layer for the thinner, more brittle inorganic ceramic-like material of the first layer of the duplex coating. Both layers are electrically insulating.

Any organic material is suitable as the organic overcoat of the second layer of the duplex coating. Preferably the material should be electrically insulating, e.g., greater than 10^8 ohm-m resistivity; able to be deposited as a conformal film around all the

constituent assembled parts of the device without damage to the first layer; able to be deposited as an essentially pin-hole-free coating, e.g., less than 0.5 g-mil/100 in^2 moisture barrier transmission rate; able to be deposited at a temperature low enough to avoid detrimental effects to the device and constituents; able to be readily built up into thicknesses to at least 0.5 mils, e.g., preferably between 1 and 3 mils; adherent to the first layer so as not to delaminate or bubble in the presence of moisture or ions; compliant and tear resistant, e.g., having an elongation ability of 10% or more; impervious to moisture, alkali metal ions and halogen ions; non-reactive and otherwise compatible (electrically, physically and mechanically) to the constituent parts of the device and to subsequent processing.

The second layer of the duplex layer is applied directly over the to of the first layer and, as mentioned above, is preferably PARYLENE C, other grades of PARYLENE, sol-gel hybrids, or other condensed or plasma polymerized organic films. PARYLENE C is an excellent moisture and ion barrier for an organic material, is an electrical insulator, is pinhole free in sub-micron thick films yet can easily be deposited in layers over 25-75 microns thick. Thick films over 25 microns thick provide rigidity to fragile bond wires during molding and its malleability provides protection from abrasive particles in the molding resin and decouples stresses between components and the molding compound.

While specific examples of materials for the first layer and the second layer are described, it will be appreciated by the skilled artisan that each layer serves a distinct and important purpose. The first layer is a barrier layer and has as its primary function the prevention of moisture or ion passage. The second layer is a compliant or protective layer and has as its primary function the protection of the more brittle first layer

during handling and manufacture, sucn as ınjectıon molding.

As shown, the duplex coating is preferably applied to partially assembled lead frames containing attached dice and wire bonds, i.e. at the stage just prior to when the parts are transfer molded in standard commercial practices.

Referring next to FIG. 5 (and step ___ in FIG. 6), shown is a completed plastic package device made up of the integrated semiconductor circuit die, the wires, the wire bonds, the leads, the first later of the duplex coating, the second layer of the duplex coating, and a die attach substrate, Also shown is a plastic package having been injection molded in a convention manner over the integrated semiconductor circuit die, the wires, the wire bonds, the leads, the first later of the duplex coating, the second layer of the duplex coating, and a die attach substrate.

While the plastic package is applied in a convention manner is it noted that conventional additives, added to protect against moisture and ions may not be needed in plastic packages with which the present embodiment or other embodiments described herein are employed.

Thus, as can be seen, the duplex coating of the present embodiment provides a hermetic barrier that protects the integrated semiconductor circuit die, the wires, and the wire bonds from contaminants, such as water and oxygen that enter the plastic package. As will be appreciated, the present embodiment, thus provides a plastic packaged, yet hermetic integrated semiconductor circuit device, thereby achieving the economic advantages associated with plastic package devices, while achieving the high-reliability and long-life advantages of ceramic packaged devices.

Further the embodiments described herein provide much greater packaging flexibility than

conventional ceramic packaging designs, while allowing operation in chemically sever environments.

Referring next to FIG. 1 and FIG. 7 through 9, this same duplex coating, as described above, can also be applied, in another embodiment, over the plastic package of a convention plastic packed system in order to provide much of the same protection as is provided by application of the duplex coating to bare assembly of the integrated semiconductor circuit die, the wire bonds, the wires, and the lead of the lead frame.

Referring to FIG. 7 (and to steps ___, ___, and ___ in FIG. 9), a cross-sectional view is shown of a plastic package structure, such as in FIG. 1, including the plastic package, the die attach substrate, the integrated semiconductor circuit die, the wires, the wire-bonds and the leads. Also shown is the first layer of the duplex coating. As above, the first layer of the duplex coating is a layer of an inorganic ceramic-like material applied, however, so as to encapsulate the plastic package, and the proximal portion of the exterior ends of the leads. Application and composition of the first layer of the duplex coating is substantially as described above in reference to FIG. 3, except of course in the present embodiment, the first layer is applied so as to encapsulate the plastic package and its contents, as opposed to just the integrated semiconductor circuit die, wire bonds, wires, and interior ends of the leads.

Thus, first the assembly comprising the integrated semiconductor circuit die, wire bonds, wires, and leads is formed in a conventional manner as described above. Next, the assembly, with the exception of the exterior ends of the leads, is encapsulated in the plastic package, as also described above. And then the first layer of the duplex coating is applied, substantially as described above, but so as to encapsulate the plastic package and its contents, as opposed to just the integrated semiconductor circuit die, wire bonds, wires, and interior ends of the leads. The

thickness of the second layer may also be greater in the present embodiment in that more handling of the second coating would be expected than in the prior embodiment.

5 Referring next to FIG. 8 (and step ___ in FIG. 9), is a cross-sectional view is shown of a plastic package structure, such as in FIG. 1, including the plastic package, the die attach substrate, the integrated semiconductor circuit die, the wires, the wire-bonds and 10 the leads. Also shown is the first layer of the duplex coating as in FIG. 7. And, also shown is the second layer of the duplex coating. As above, the second layer of the duplex coating is a layer of an organic overcoat applied, however, so as to encapsulate the plastic 15 package, and the proximal portion of the exterior ends of the leads, and the first layer of the duplex coating. Application and composition of the second layer of the duplex coating is substantially as described above in reference to FIG. 4, except of course in the present 20 embodiment, the second layer is applied so as to encapsulate the plastic package and its contents as well as the first layer of the duplex coating, as opposed to just the integrated semiconductor circuit die, wire bonds, wires, interior ends of the leads, and the first 25 layer of the duplex coating.

Referring next to FIG. 10, shown is an assembly view of a plastic case structure in which the principles described herein may be incorporated. Shown in a plastic cap, a first epoxy seal, a lead frame, an integrated 30 semiconductor circuit die, wires and wire bonds, a second epoxy seal, and a plastic base. In all respects the illustrated assembly is conventional in structure and manufacturing except that prior to assembly, the duplex coating described above is applied to the integrated 35 semiconductor circuit die, the wire bonds, the wires, and interior ends of leads of the lead frame. Masking of or removal of the duplex coating from exterior ends of the leads of the lead frame is effected as described above in

order to maintain the exterior ends of the leads for electrical connection.

Referring next to FIG. 11, shown is an assembly view of another plastic case structure in which the principles described herein may be incorporated. Shown in a plastic cap, a first epoxy seal, a plastic side wall, a second epoxy seal, a lead frame, an integrated semiconductor circuit die, wires and wire bonds, a third epoxy seal, and a plastic base. In all respects the illustrated assembly is conventional in structure and manufacturing except, as with the embodiment of FIG. 10, prior to assembly, the duplex coating described above is applied to the integrated semiconductor circuit die, the wire bonds, the wires, and interior ends of leads of the lead frame. As in FIG. 10, masking of or removal of the duplex coating from exterior ends of the leads of the lead frame is effected as described above in order to maintain the exterior ends of the leads for electrical connection.

Referring to FIG. 12, a perspective view is show, partially in cross section, of a device having both the coating approach of FIGS. 2 through 6 and the coating approach of FIG. 7 through 9 applied thereto. As the approach of the illustrated embodiment is identical to the individual approaches described in reference to these groups of figures, except that both approaches are applied to the same device, further explanation of these approaches is not made herein. The skilled artisan will appreciate, however, that for particularly sensitive applications, the illustrated embodiment may provide even greater hermeticity that either of the approaches described above in their numerous variations.

While the invention herein disclosed has been described by means of specific embodiments and applications thereof, numerous modifications and variations could be made thereto by those skilled in the art without departing from the scope of the invention set forth in the claims.

CLAIMS

What is claimed is:

5 1. A hermetically coated device comprising:
an integrated semiconductor circuit die;
a first layer comprising an inorganic material, the first layer enveloping the integrated semiconductor circuit die; and
10 a second layer, the second layer enveloping the integrated semiconductor circuit die.

2. The hermetically coated device of Claim 1 wherein the first layer is in contact with the integrated
15 semiconductor circuit die.

3. The hermetically coated device of Claim 1 further comprising:
a plastic package enveloping the integrated
20 semiconductor circuit die.

4. The hermetically coated device of Claim 3 wherein the plastic coating is in contact with the second layer.
25

5. The hermetically coated device of Claim 3 wherein said plastic package comprises a plastic cap.

6. The hermetically coated device of Claim 1
30 further comprising:
a lead, the lead having an interior end and an exterior end;
a wire;
a bonding pad on a surface of the integrated
35 semiconductor circuit die;
a first wire bond between a first end of the wire and the bonding pad; and

a second wire bond between a second end of the wire and the interior end of the lead;

wherein the wire, the bonding pad, the first wire bond and the second wire bond are in contact with
5 and enveloped by the first layer.

7. The hermetically coated device of Claim 1 further comprising:

a plastic package enveloping the integrated
10 semiconductor circuit die;

wherein the first layer is in contact with and envelops the plastic package.

8. The hermetically coated device of Claim 1
15 wherein the first layer comprises a material selected from the group of inorganic materials consisting of

_______________________________________.

9. The hermetically coated device of Claim 1
20 wherein the second layer comprises a material selected from the group of organic materials consisting of

_______________________________________.

10. A method of making a hermetically coated
25 device comprising:

providing an integrated semiconductor circuit die;

applying a first layer comprising an inorganic material, the first layer enveloping the integrated
30 semiconductor circuit die; and

applying a second layer, the second layer enveloping the integrated semiconductor circuit die.

11. The method of Claim 10 wherein applying of
35 the first layer comprising contacting the integrated semiconductor circuit die with the first layer.

12. The method of Claim 10 further comprising:

enveloping the integrated semiconductor circuit die within a plastic package.

5

13. The method of Claim 12 wherein the enveloping within the plastic package comprises contacting the second layer with the plastic package.

10 14. The method of Claim 12 wherein said enveloping within the plastic package comprises placing a plastic cap over the integrated semiconductor circuit die.

15 15. The method hermetically coated device of Claim 10 further comprising:

forming a first wire bond between a first end of a wire and a bonding pad on a surface of the integrated semiconductor circuit die; and

20 forming a second wire bond between a second end of the wire and the interior end of the lead;

wherein the applying of the integrated semiconductor circuit die within the first layer comprises applying the first layer to the wire, the

25 bonding pad, the first wire bond and the second wire bond.

16. The method of Claim 10 further comprising:

enveloping the enveloping the integrated

30 semiconductor circuit die within a plastic package;

wherein the applying of the first layer includes enveloping the plastic package with the first layer.

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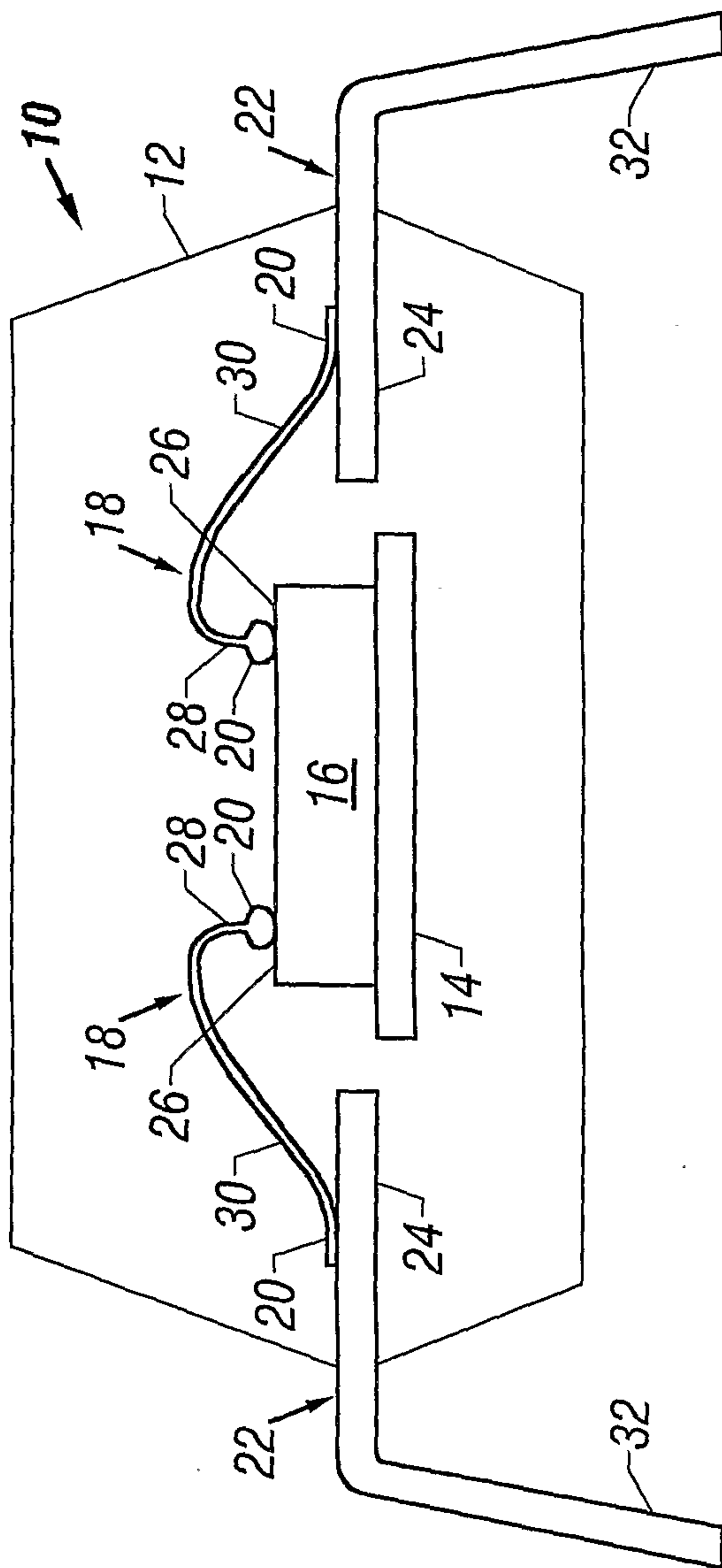


FIG. 1A

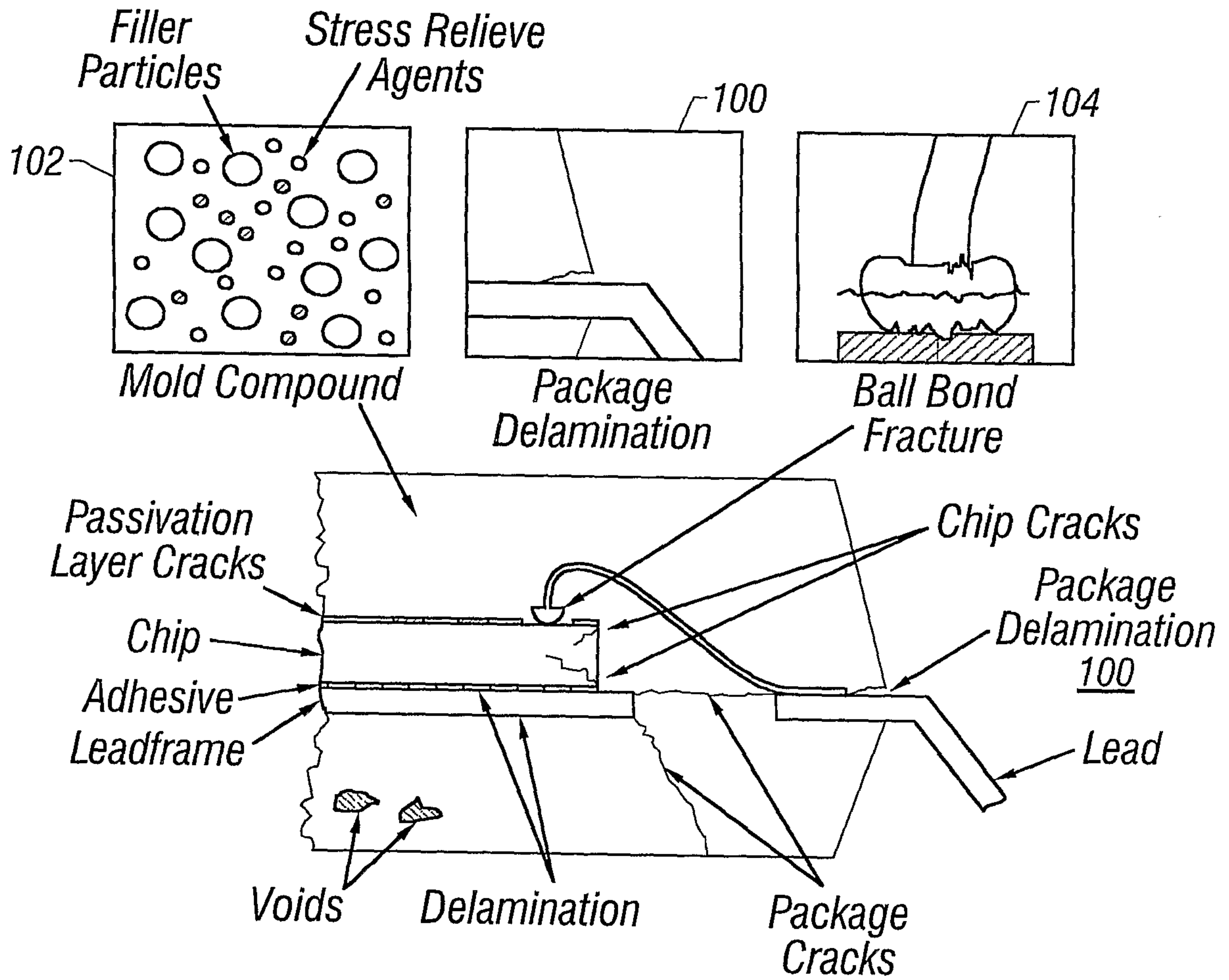


FIG. 1B

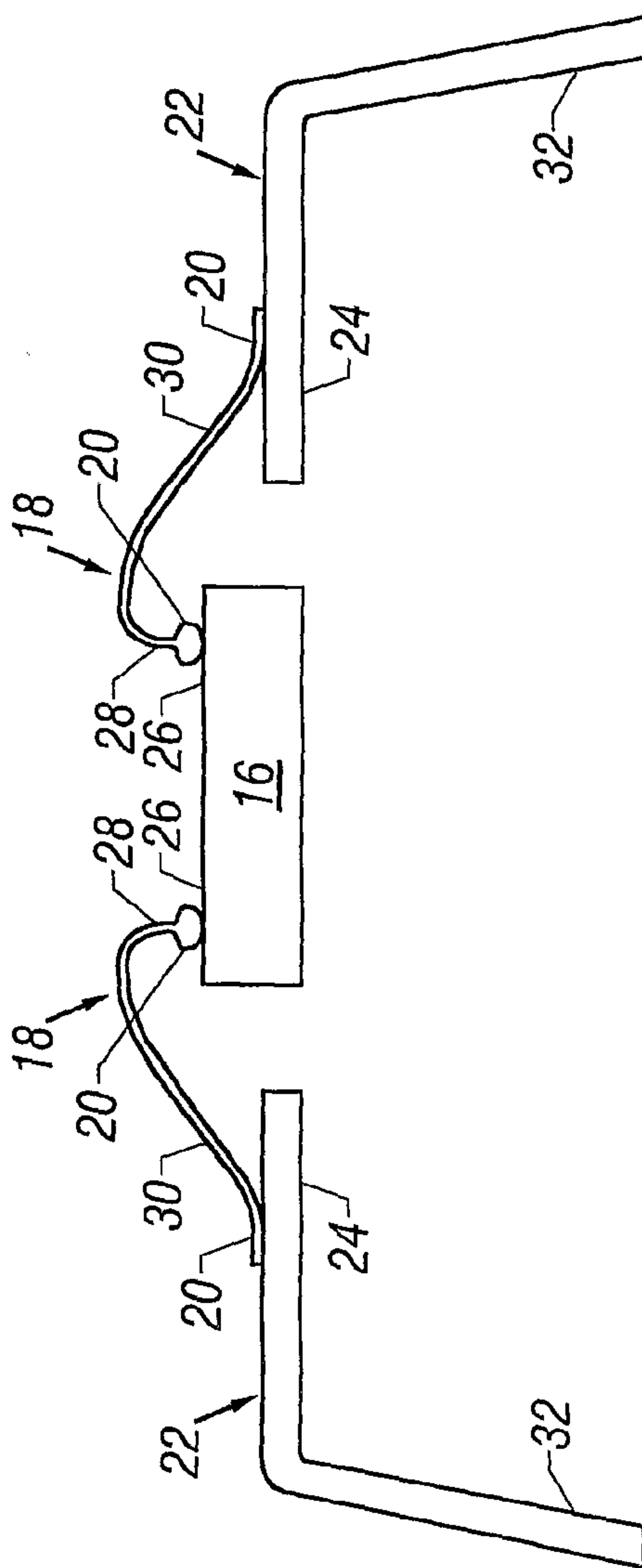


FIG. 2

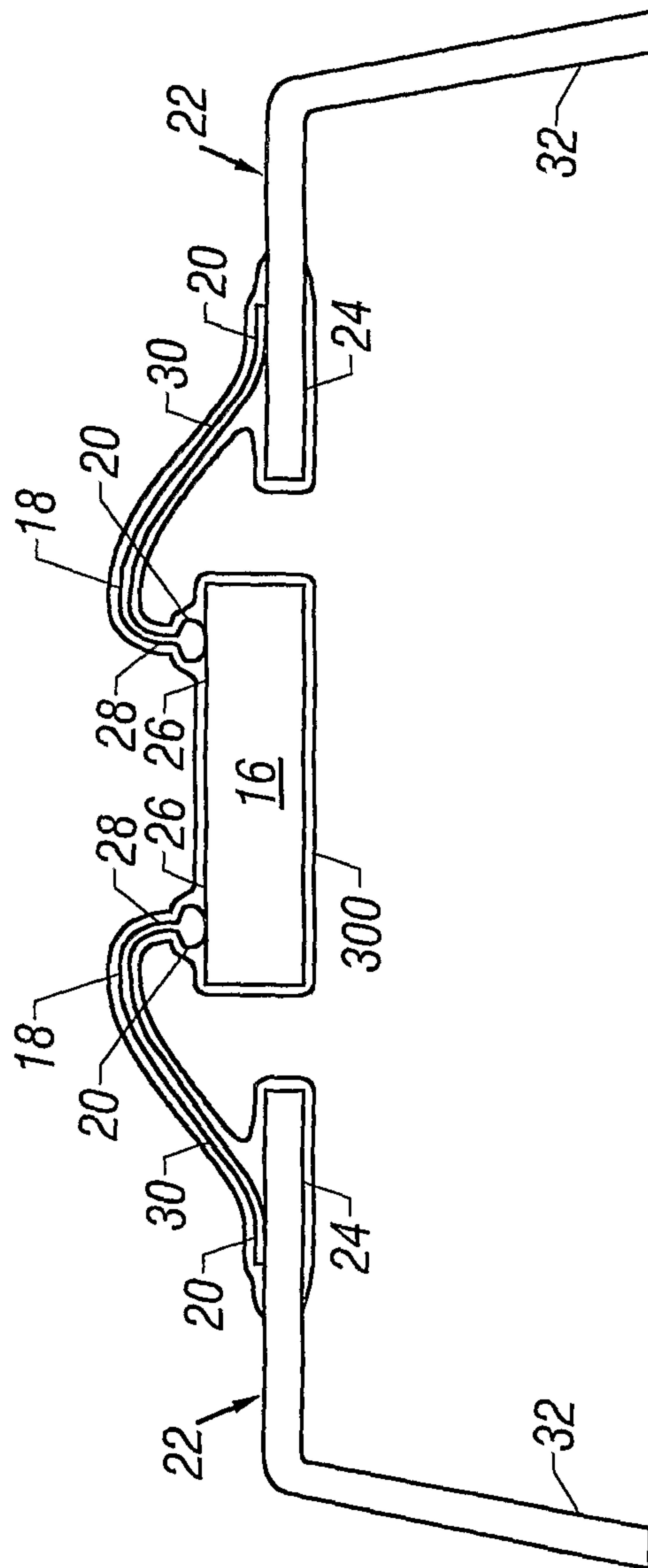


FIG. 3

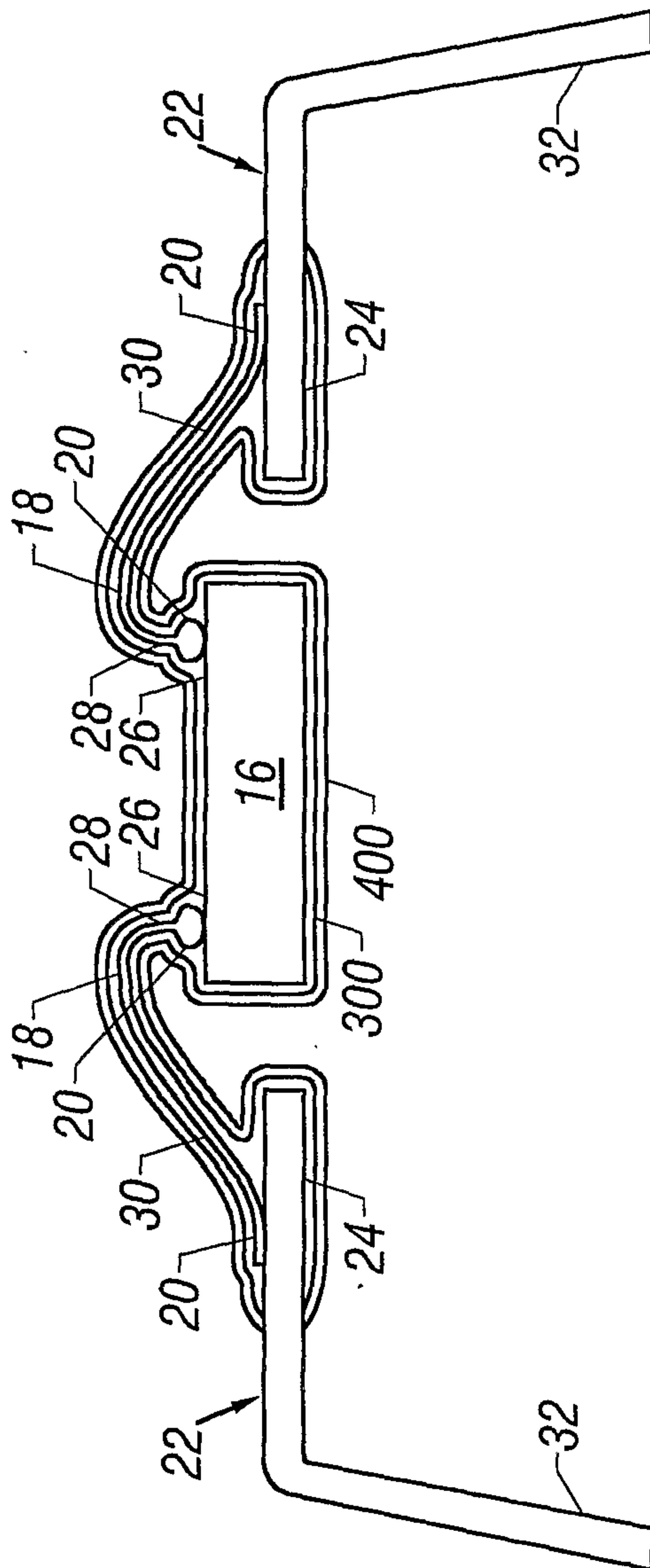


FIG. 4

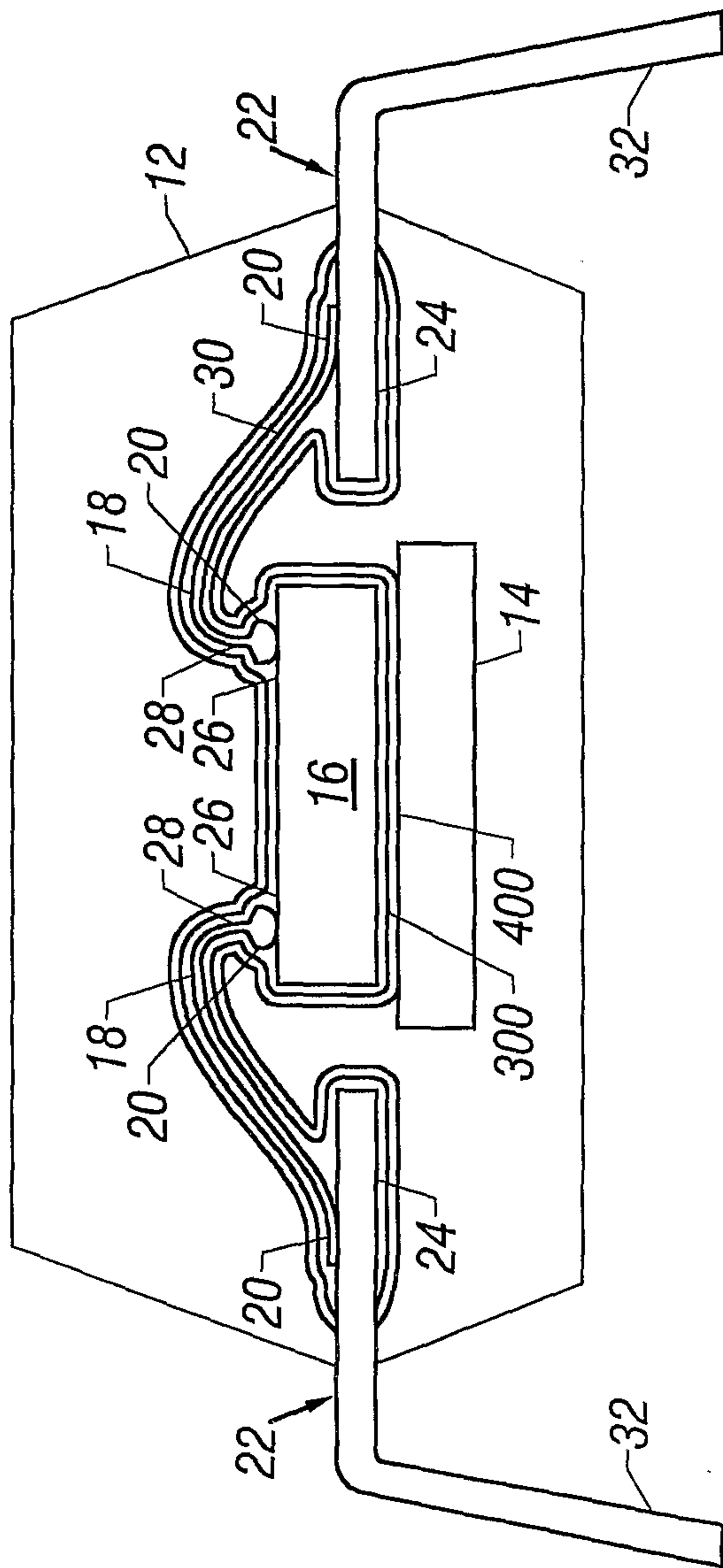


FIG. 5

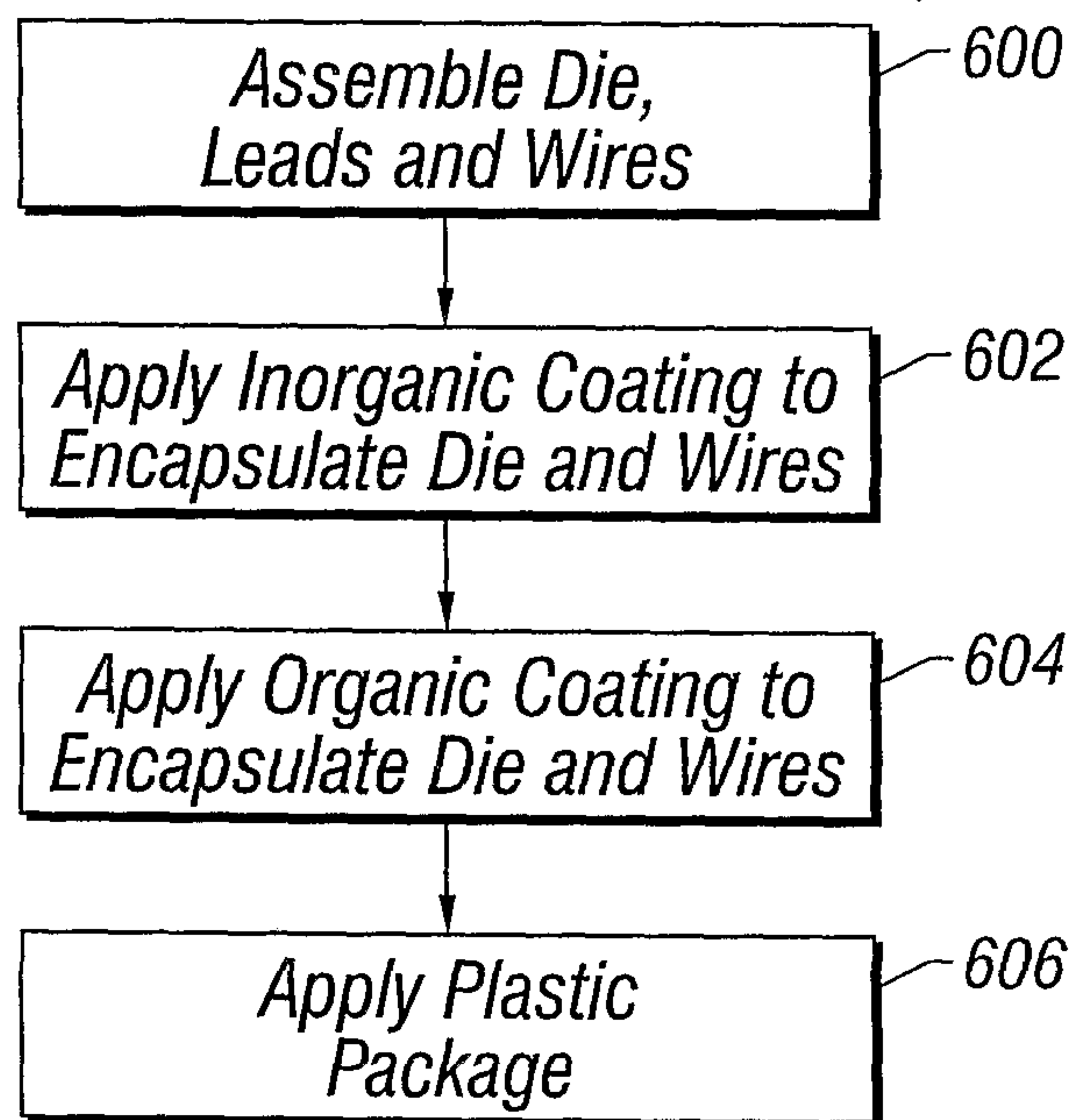


FIG. 6

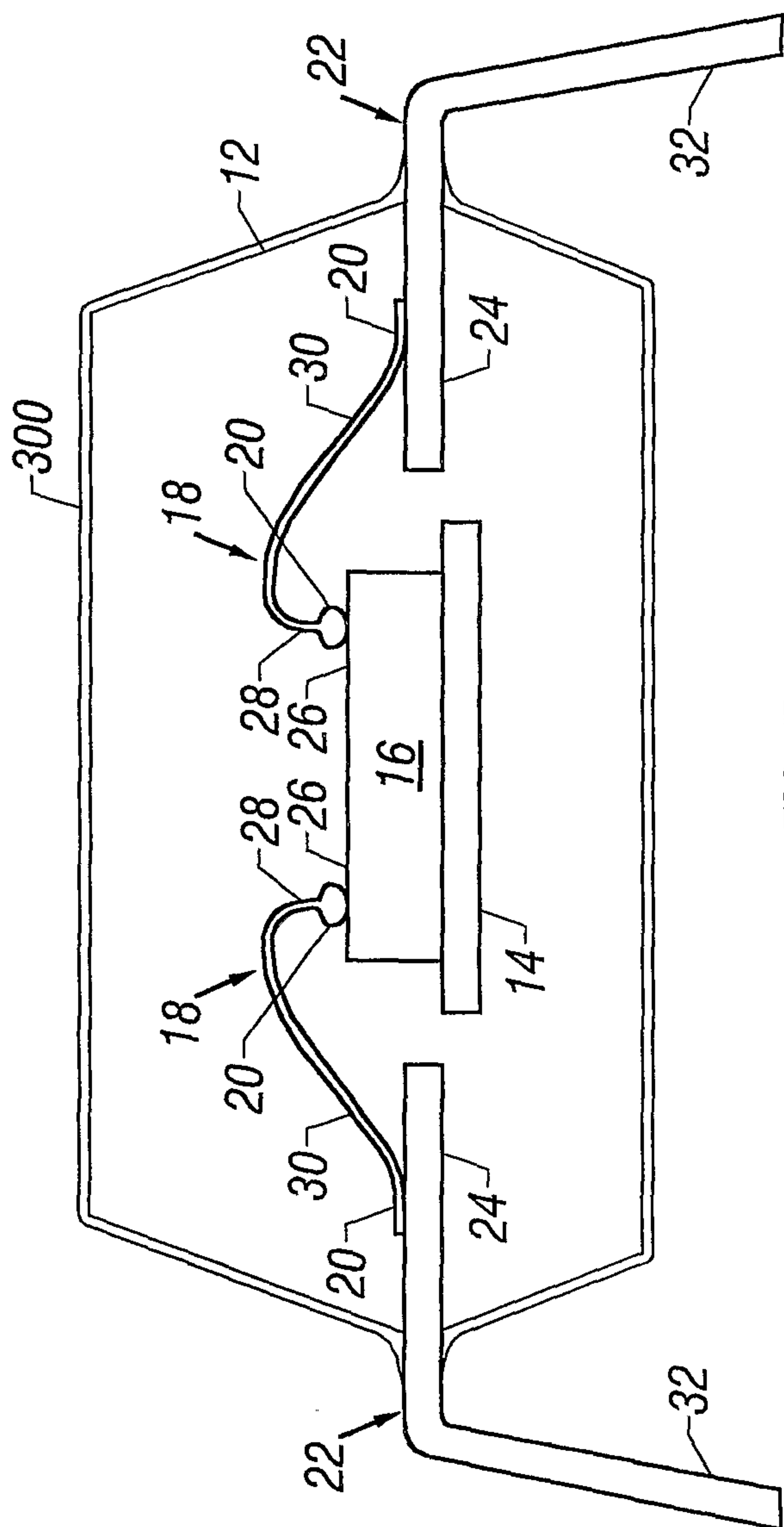


FIG. 7

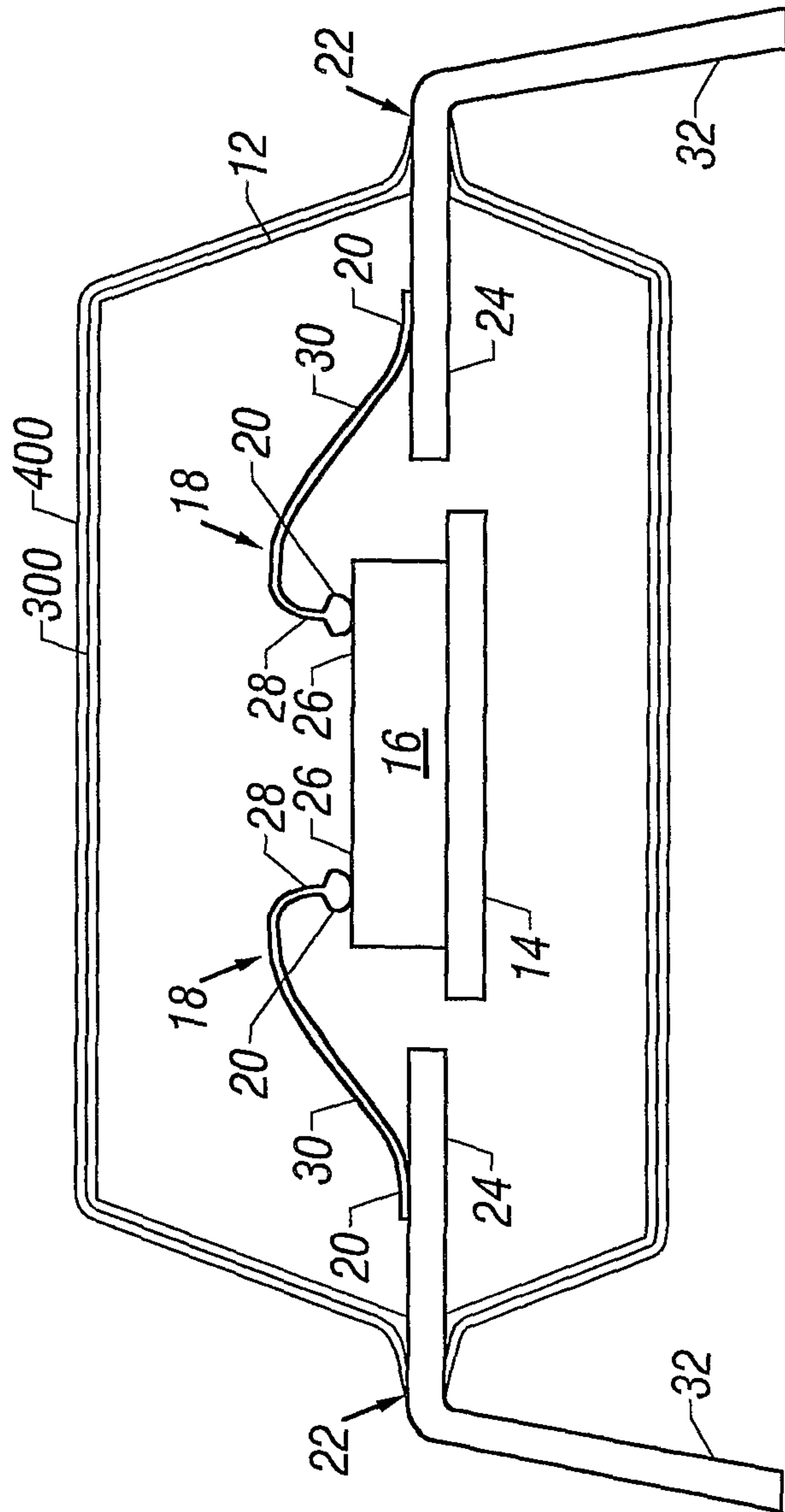


FIG. 8

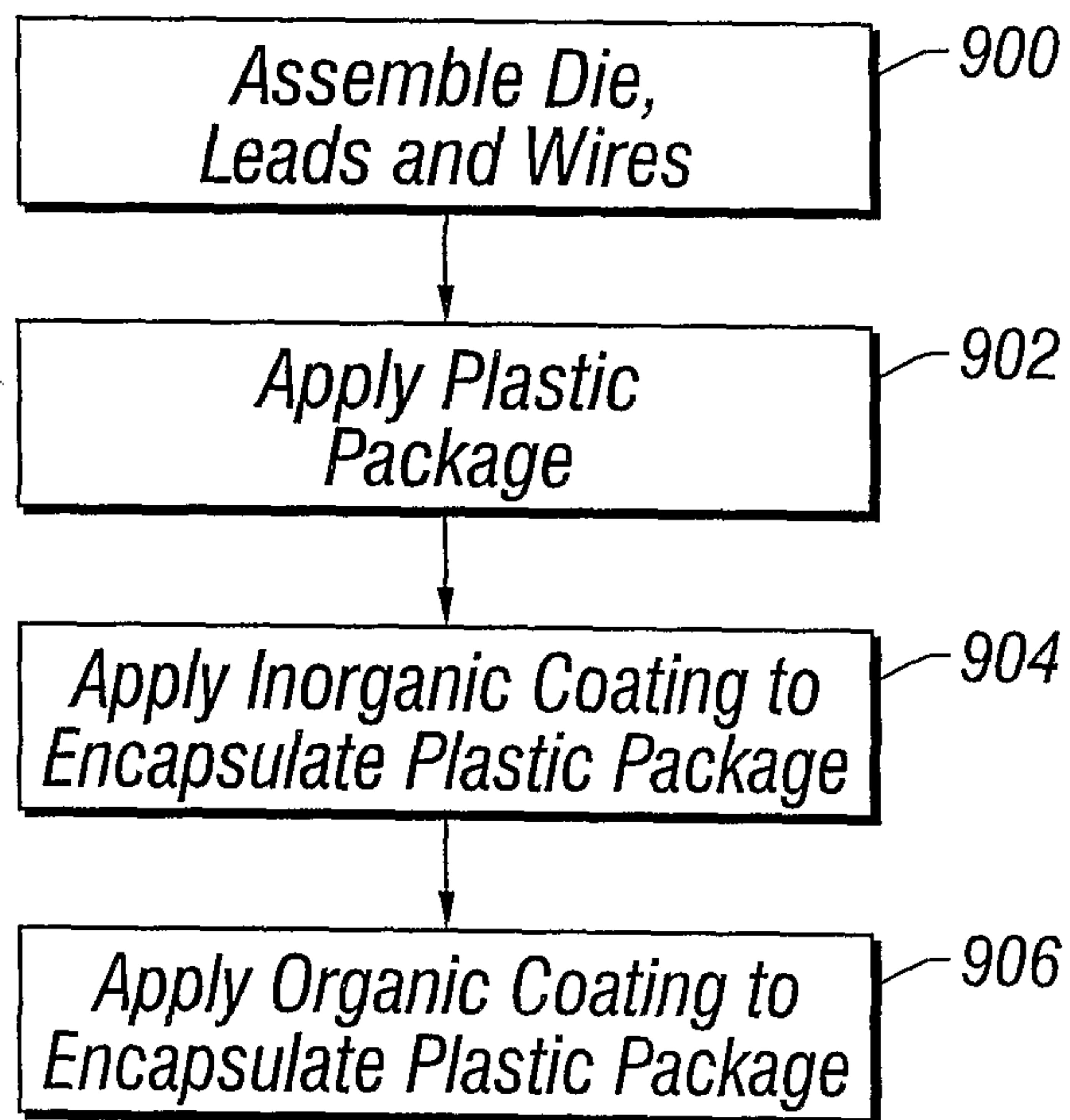
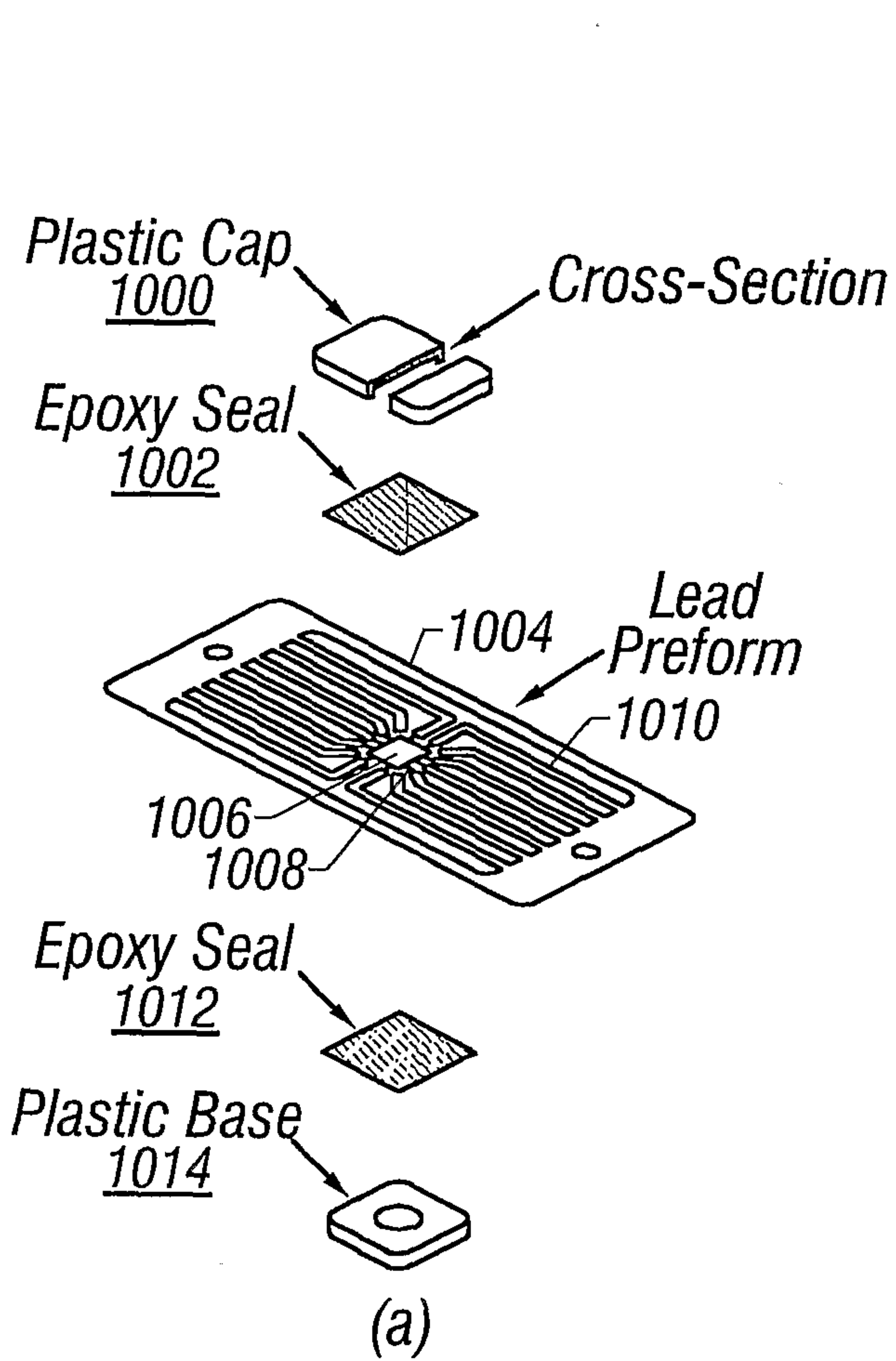
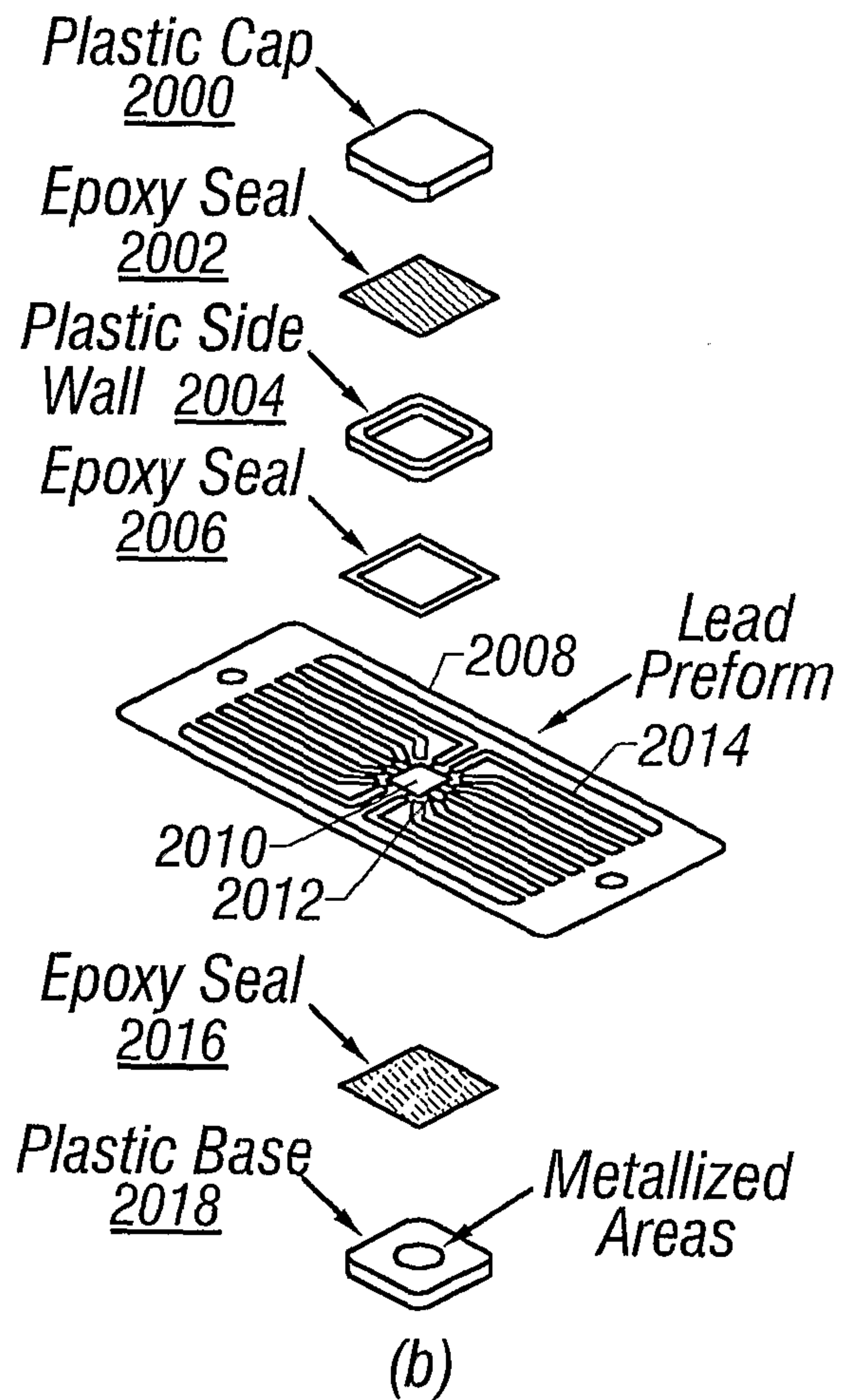


FIG. 9



(a)

FIG. 10



(b)

FIG. 11

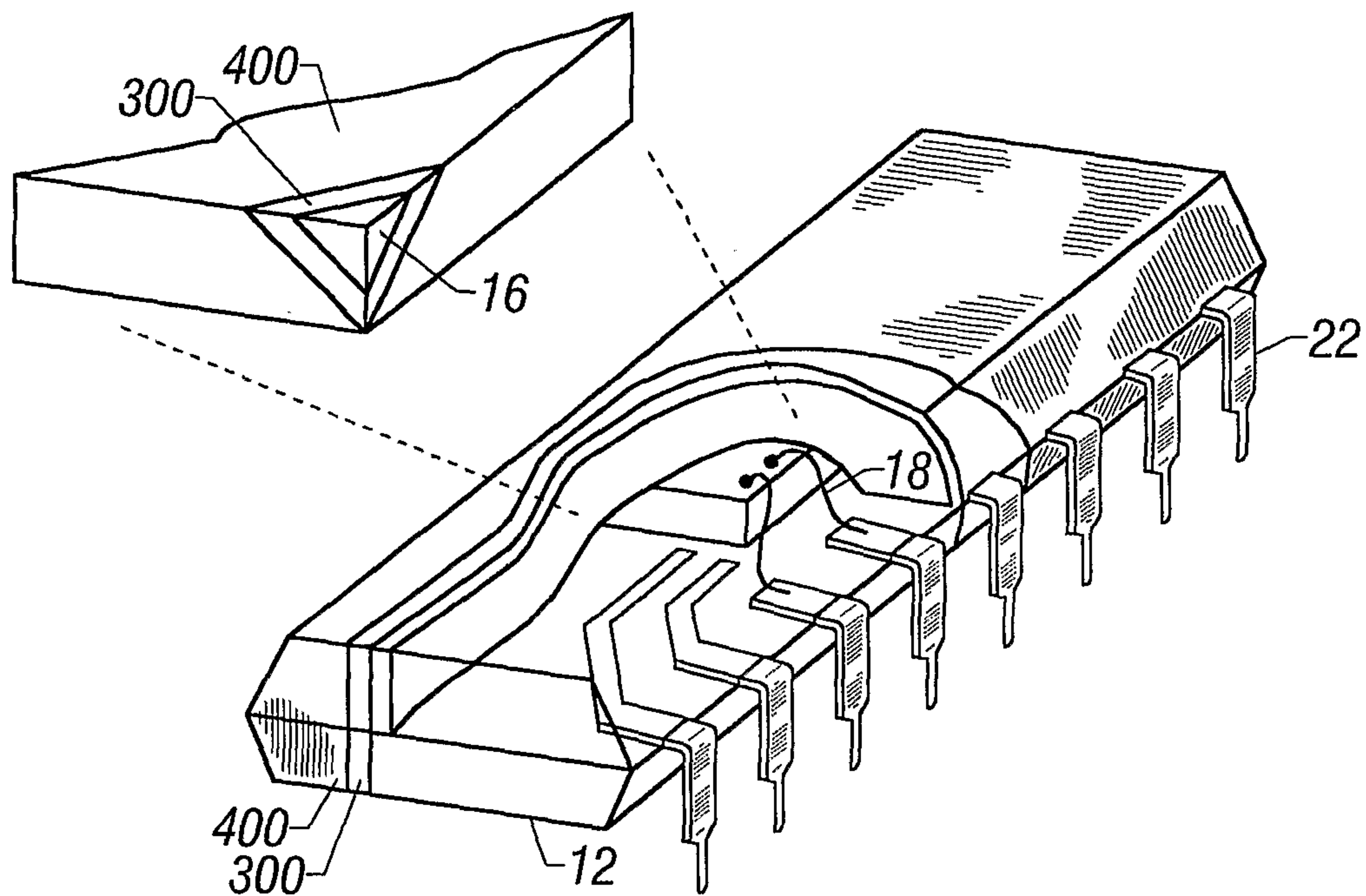
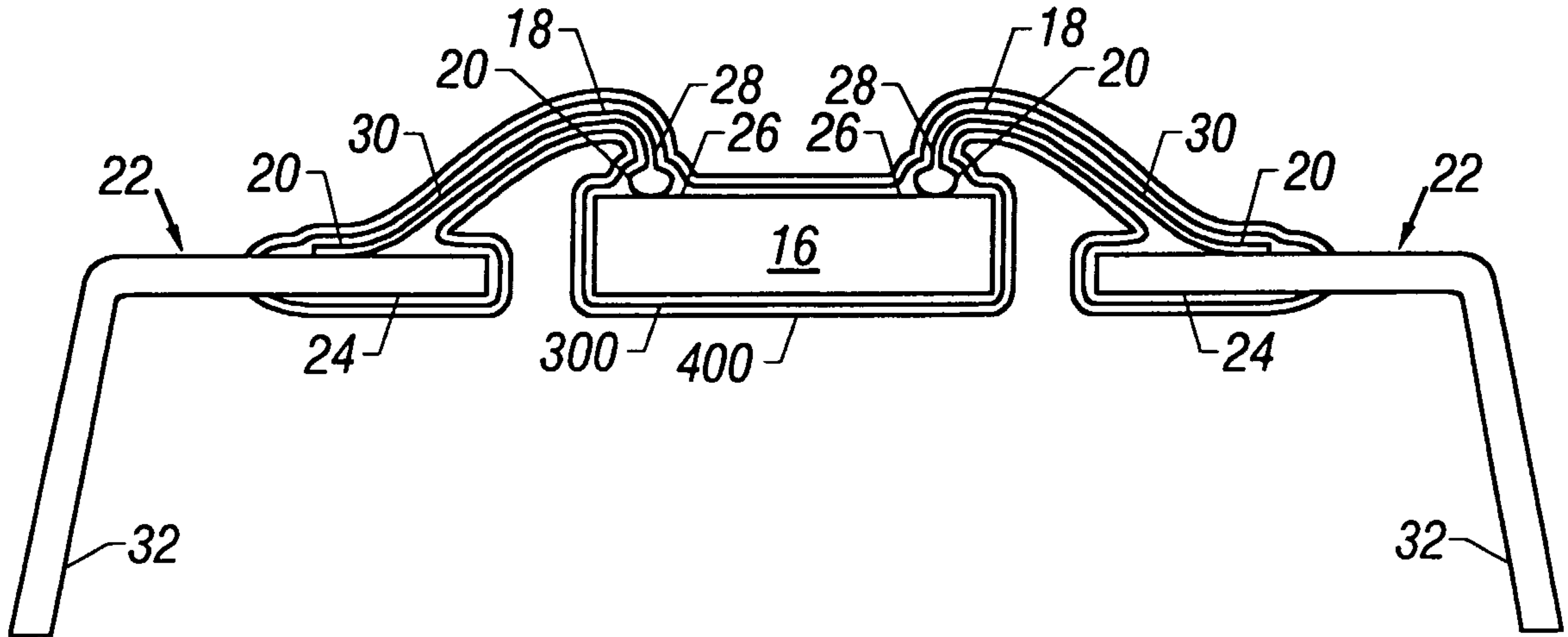


FIG. 12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