(12) UK Patent Application (19) GB (11) 2 295 722 (13) A

(43) Date of A Publication 05.06.1996

(21) Application No 9424178.3

(22) Date of Filing 30.11.1994

(51) INT CL[6]
H01L 21/56

(52) UK CL (Edition O)
H1K KPF K5A5 K5BX K5C3D

(56) Documents Cited
EP 0258098 A1 US 5097317 A US 5019419 A
US 4784872 A US 4163072 A

(58) Field of Search
UK CL (Edition N) H1K KPF
INT CL[6] H01L

(71) Applicant(s)
Motorola Limited

(Incorporated in the United Kingdom)

Jays Close, Viables Industrial Estate, Basingstoke, Hampshire, RG22 4PD, United Kingdom

(72) Inventor(s)
Derek Thomson
Andrew Beaumont

(74) Agent and/or Address for Service
Christopher Stanislaw Hirsz
Motorola Limited, European Intellectual Property Operation, Midpoint, Alencon Link, BASINGSTOKE, Hampshire, RG21 7PL, United Kingdom

(54) Packaging integrated circuits

(57) An integrated circuit (12) is mounted on a flag portion (11) of a leadframe. The leadframe also includes lead posts (10) to which are connected electrical connectors or bond wires (13) extending between the posts (10) and the integrated circuit (12). A plastic package (A) is moulded around the lead posts (10), the flag (11), the integrated circuit (12) and the bond wires (13). A polymer material is coated on all surfaces exposed prior to moulding of the package (A). The polymer material used for this encapsulation is is of very low molecular weight and viscosity and provides protection of the integrated circuit from corrosion by being chemisorbed onto its surface. This effectively seals any problem in the integrity of the passivation layer preventing moisture ingress, collection and therefore corrosion.

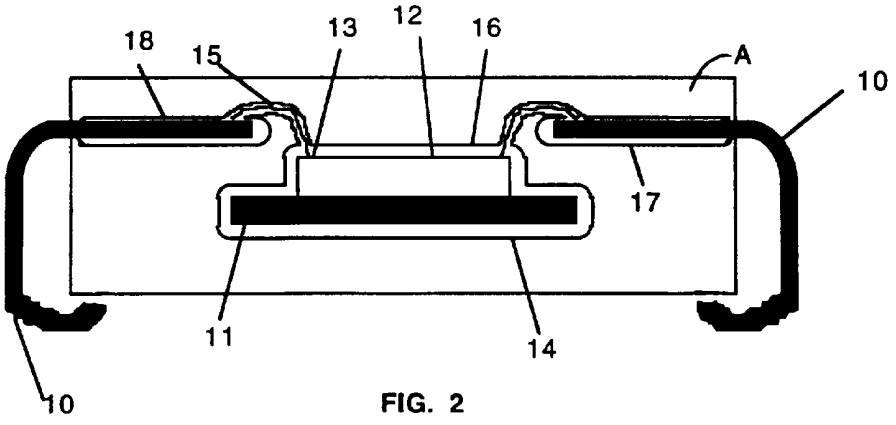

FIG. 2

GB 2 295 722 A

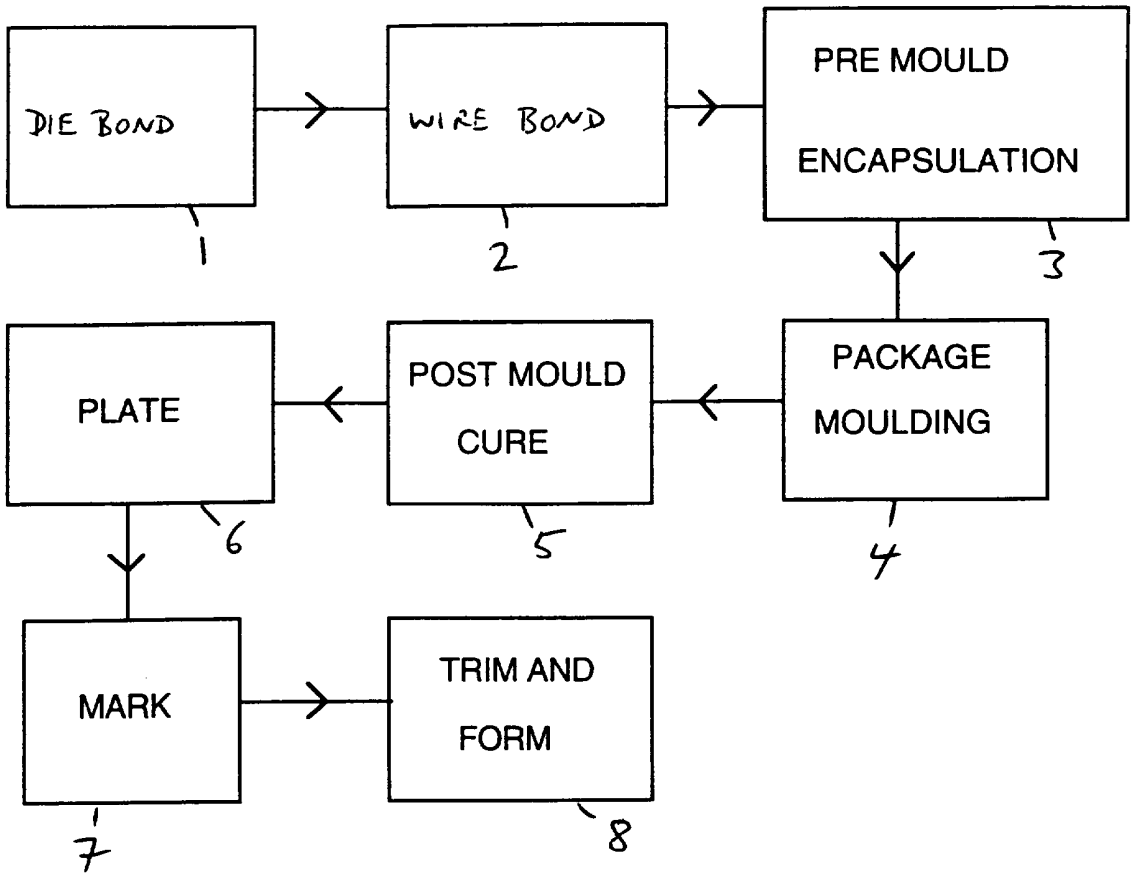
DIE BOND
WIRE BOND
PRE MOULD
ENCAPSULATION
PACKAGE
MOULDING
POST MOULD
CURE
PLATE
MARK
TRIM AND
FORM
1
2
3
4
5
6
7
8

FIG.1

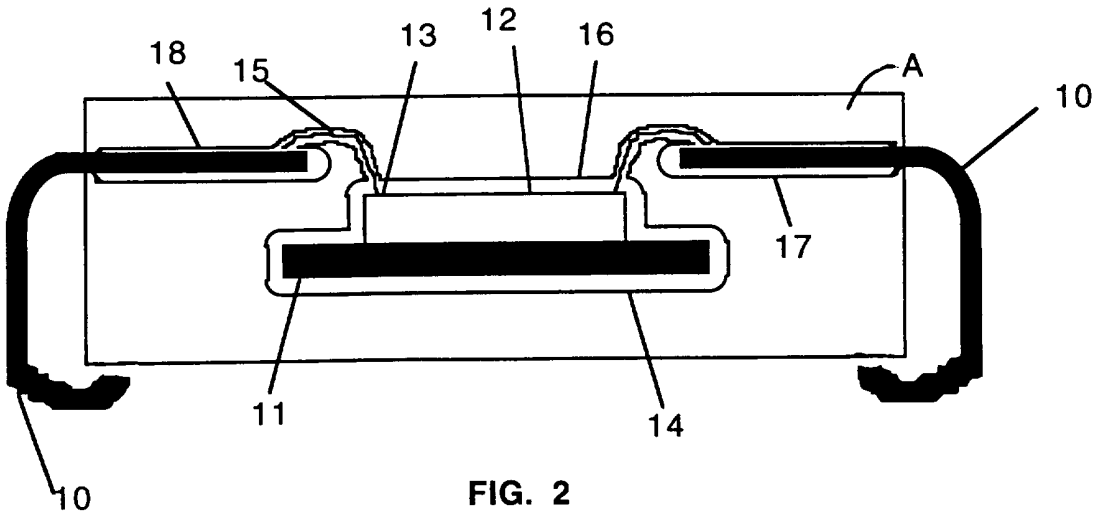
18
15
13
12
16
A
10
17
11
14
10

FIG. 2

2295722

METHOD OF PACKAGING INTEGRATED CIRCUITS

Field Of The Invention

This invention relates to a method of packaging integrated circuits, and more particularly to a method of encapsulating integrated circuits in plastics packages.

Background Of The Invention

Plastic packaged semiconductor devices whilst being markedly less expensive than hermetically packaged alternatives have historically being hindered by drawbacks such as increased susceptibility to moisture induced corrosion and damage caused by temperature cycling. More recently with the advent of thinner packages the phenomenon of "pop-corn" has forced extra processing steps on semiconductor manufacturers and restrictions on those who mount the devices onto printed circuit boards.

In plastic assembled packages moisture can penetrate directly through the epoxy leading to corrosion of the metallisation layer of the integrated circuit. Corrosion occurs particularly on the bond pads, but if there are problems in the integrity of the passivation layer then the entire integrated circuit is at risk, even in the absence of delamination of the interface between the plastic package and the integrated circuit. Slight delamination, even if not leading to non-functionality, can lead to increased susceptibility to moisture ingress and so corrosion. Delamination of any of the interfaces between the plastic package and the integrated circuit, connecting medium (ie. bond wires) and leadframe (ie. the bonding flag and the lead posts) can create a moisture path which increases corrosion susceptibility.

The most common problem that occurs as a result of moisture in plastic packaged semiconductor devices is due to the soldering processes used in connecting the component onto a printed circuit board. Certain package types and lead frame / die size combinations are more susceptible to the problem, but in simple terms, moisture absorbed by the the package is made to rapidly expand by the sharp rise in temperature experienced in all forms of soldering. The resulting pressure causes the interfaces between the plastic package and the integrated circuit, leadframe and connecting medium to experience a stress. If the adhesion between any, or all, of the before mentioned interfaces is not sufficiently robust then they can delaminate, ie. the plastic package and the substrate become separated. This effect is commonly known as "popcorn". At present

packages which are susceptible to this problem are given an extra bake and then dry-packed to prevent moisture ingress. However, the time between removing the package from dry pack and performing the solder process must be controlled to prevent a level of moisture building up which can cause "popcorn". The "popcorn" issue can give functional failure of the device due to forces exerted on the connecting medium, ie. the bond wires.

In plastic packaged integrated circuits there is an inherent mismatch between the coefficients of thermal expansion of the plastic package and the integrated circuit, leadframe and connecting medium. This mismatch creates stress on the integrated circuit when the package experiences any form of temperature cycling. This stress can crack the integrated circuit causing reliability issues which can lead to non-functionality.

Another form of damage which can also occur is caused by the filler particles in the plastic material used to create the package. Although essential to the physical properties of the plastic package they can damage the passivation layer of the integrated circuit.

Techniques have been employed to tackle to above problems with degrees of success. However, at present there is no single solution which deals with all the problems effectively. Modified leadframes have been employed to reduce the risks of delamination of the bonding flag underside. Polyimide top layers on integrated circuits do provide protection against the problems associated with the different thermal expansion coefficients of the plastic package and integrated circuit. Polyimide is also an effective barrier which prevents damage from the filler particles contained in the package plastic and delamination of the integrate circuit to package interface is also less likely to occur. However, the bond pads are still exposed to moisture and hence corrosion.

The polyimide layer discussed above is produced during the wafer fabrication process and the production of this layer requires a photolithography step and an etching step. Both of these involve volatile materials which require special handling. The etching process clears the bond pads of polyimide to allow the integrated circuit to be tested at probe and bonded during assembly. In EPROM devices full testing takes place at probe and to return the devices to their unprogrammed state by erasing them using ultra violet (UV) light. This erase step is not possible through the polyimide and therefore two sets of tests must be carried out at probe,

one prior to polyimide deposition and the other after. This involves moving the wafers in and out of the wafer fab which can create difficulties.

It is therefore an object of the present invention to mitigate the above-mentioned disadvantages of known packaging techniques.

Brief Summary Of The Invention

Accordingly, the invention provides a method of packaging an integrated circuit, comprising the steps of:

bonding an integrated circuit die on to a flag portion of a lead frame;

connecting at least one conductor between the integrated circuit die and a post portion of the lead frame;

covering the integrated circuit die, the flag portion, the conductor and the post portion in a fluid polymer material;

at least partly curing/solidifying the polymer material so as to encapsulate the integrated circuit die, the flag portion, the conductor and the post portion;

forming a plastics package around the encapsulated integrated circuit die, flag portion, conductor and post portion.

In a preferred embodiment, the plastics package extends completely over the polymer material.

The polymer material is preferably an epoxy or epoxy acrylate material. Preferably, the polymer material is only partly cured so that it provides a surface with good adhesive properties for the plastics package to attach to.

Brief Description Of The Drawings

One embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a flow diagram of a packaging process according to the invention; and

FIG. 2 shows a cross-sectional schematic view through an integrated circuit packaged using the process of FIG. 1.

Detailed Description

Referring firstly to FIG.2, a schematic cross sectional view of the packaged integrated circuit 12 is shown. The integrated circuit 12 is mounted on a flag portion 11 of a leadframe. The leadframe also includes lead posts 10 to which are connected electrical connectors or bond wires 13 extending between the posts 10 and the integrated circuit 12. A plastic package A is shown moulded around the lead posts 10, the flag 11, the integrated circuit 12 and the bond wires 13. A polymer material is coated

on all surfaces exposed prior to moulding of the package A. The material thus coats the flag 11, as shown at 14, the integrated circuit 12, as shown at 16, the bond wires 13, as shown at 15, and the lead posts 10, as shown at 17. The material extends only to the edge of the plastic package A.

Thus, as shown FIG. 1, the assembly operation involves the steps of die bonding 1 the integrated circuit die 12 to the flag 11 of the leadframe; electrically connecting the die 12 to the leadframe by way of a wire bond operation 2, performing a pre mould encapsulation process 3, followed by a package moulding operation 4. This is followed by a thermally cured post mould operation 5, after which plating 6 of the exposed leadframe takes place. Package marking 7 then takes place, and finally a trim and form operation 8 shapes the package to it's final state.

The pre mould encapsulation step 3 provides the integrated circuit 12 including the bond pads, the bond wires 13, and the post 10 and flag 11 portions of the leadframe with a coating of polymer material prior to moulding of the plastic package A. In a preferred embodiment the polymer coating is of very low molecular weight and viscosity and wets the integrated circuit, flag and post portions of the leadframe and the bond wires easily. The coating material provides protection of the integrated circuit from corrosion by being chemisorbed onto its surface. This effectively seals any problem in the integrity of the passivation layer preventing moisture ingress, collection and therefore corrosion. The bond pads and bond wires are also protected in a similar way. This protection is not offered by any current technique.

The mould compound used in the production of plastic coated integrated circuits contains various waxes which ensure that the package is easily removed from the mould tool. These waxes coat all metal surfaces which the molten plastic contacts and prevents it adhering to them when cured. The leadframe flag, bond wire and posts are all metal and therefore coated by these waxes preventing good adhesion between them and the plastic package. By coating all metal surfaces contained within the package using the polymer material prior to the moulding process taking place, the waxes contained in the molten plastic do not coat the metal surfaces allowing a good adhesive joint to be created.

In a preferred embodiment the coating is only partially cured prior to moulding and is therefore adhesive in nature forming chemical and physical bonds with all of the coated surfaces. The completion of the curing of the coating occurs during the curing of the molten plastic used to

create the package ensuring that a good chemical physical adhesive joint is created as the coating chemically bonds to the curing moulding plastic. The greater adhesive strength of the interfaces between the plastic package and the leadframe flag, posts, and the bond wires provides much greater resistance to the "popcorn" phenomenon described earlier. Prevention of delamination of the posts and bond wires prevents any direct route for moisture ingress.

In a preferred embodiment the coating maintains a degree of flexibility after curing and during the formation of the plastic package. The stress created by the difference in the thermal expansion coefficients of the plastic and the integrated circuit and the associated problems discussed earlier are therefore resolved in a similar way to the use of polyimide, that is the flexibility of the coating relieves the stress built up during any temperature cycling or increase that the package experiences. However, since the pre mould encapsulation is part of the assembly flow and negates the need for a polyimide passivation layer, the problems discussed with the testing of EPROM devices earlier involving the return of wafers to the wafer fab after probe and erase are eliminated. The coating also provides protection of the integrated circuit from filler particle damage acting as a physical barrier in a similar way to a polyimide layer.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. A method of packaging an integrated circuit, comprising the steps of:

bonding an integrated circuit die on to a flag portion of a lead frame;

connecting at least one conductor between the integrated circuit die and a post portion of the lead frame;

covering the integrated circuit die, the flag portion, the conductor and the post portion in a fluid polymer material;

at least partly curing/solidifying the polymer material so as to encapsulate the integrated circuit die, the flag portion, the conductor and the post portion;

forming a plastics package around the encapsulated integrated circuit die, flag portion, conductor and post portion.

2. A method of packaging an integrated circuit according to claim 1, wherein the plastics package is formed so as to extend completely over the polymer material.

3. A method of packaging an integrated circuit according to either claim 1 or claim 2, wherein the polymer material is either an epoxy or epoxy acrylate material.

4. A method of packaging an integrated circuit according to any preceding claim, wherein the polymer material is only partly cured so that it provides a surface with good adhesive properties for the plastics package to attach to.

5. A method of packaging an integrated circuit substantially as hereinbefore described with reference to the drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report)	Application number GB 9424178.3
Relevant Technical Fields (i) UK Cl (Ed.N) H1K-KPF (ii) Int Cl (Ed.6) H01L	Search Examiner S J DAVIES Date of completion of Search 23 FEBRUARY 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii)	Documents considered relevant following a search in respect of Claims :- ALL

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X,Y	EP 0258098 A1	(FUJITSU) see eg column 4, line 60 to column 5, line 13	X: 1-3 Y: 4
X,Y	US 5097317	(FUJIMOTO ET AL) see eg column 2, lines 48-61, column 4, line 64 to column 5 line 4	X: 1-3 Y: 4
Y	US 5019419	(MATSUMOTO ET AL) see eg column 2, line 52 to column 3, line 13	4
X,Y	US 4784872	(MOELLER ET AL) see eg column 3, lines 28-41	X: 1-3 Y: 4
X,Y	US 4163072	(SOOS) see whole document	X: 1-3 Y: 4

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).