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(54) **CODEBOOK GENERATION SYSTEM AND ASSOCIATED METHODS**

continuation of application No. 11/036,906, filed on Jan. 13, 2005, now Pat. No. 7,778,826.

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(57) **ABSTRACT**

(63) Continuation of application No. 12/584,009, filed on Aug. 28, 2009, now Pat. No. 8,428,937, which is a

A codebook generation system and associated methods are generally described herein.

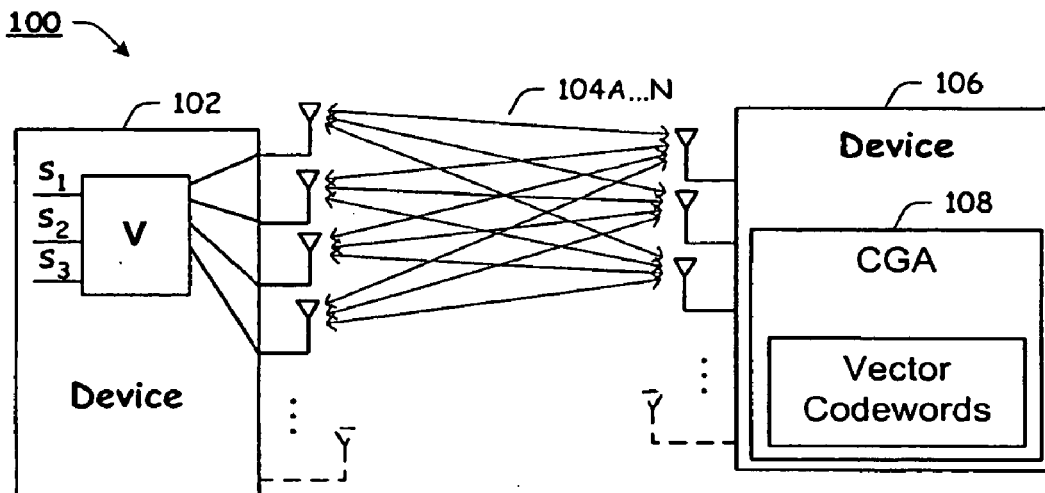


FIG. 1

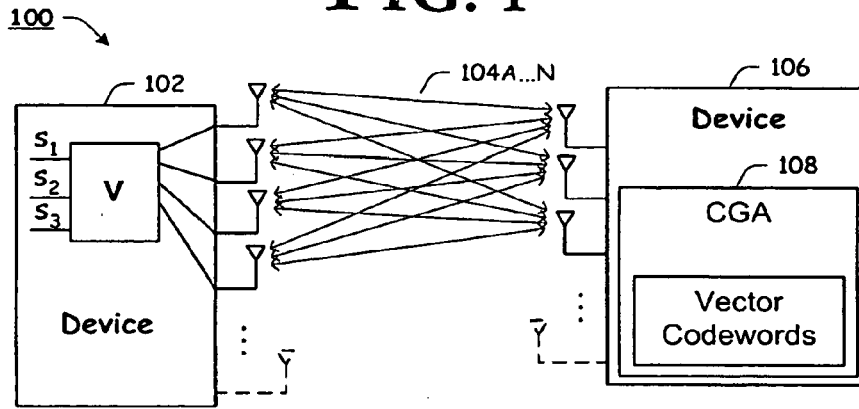


FIG. 2

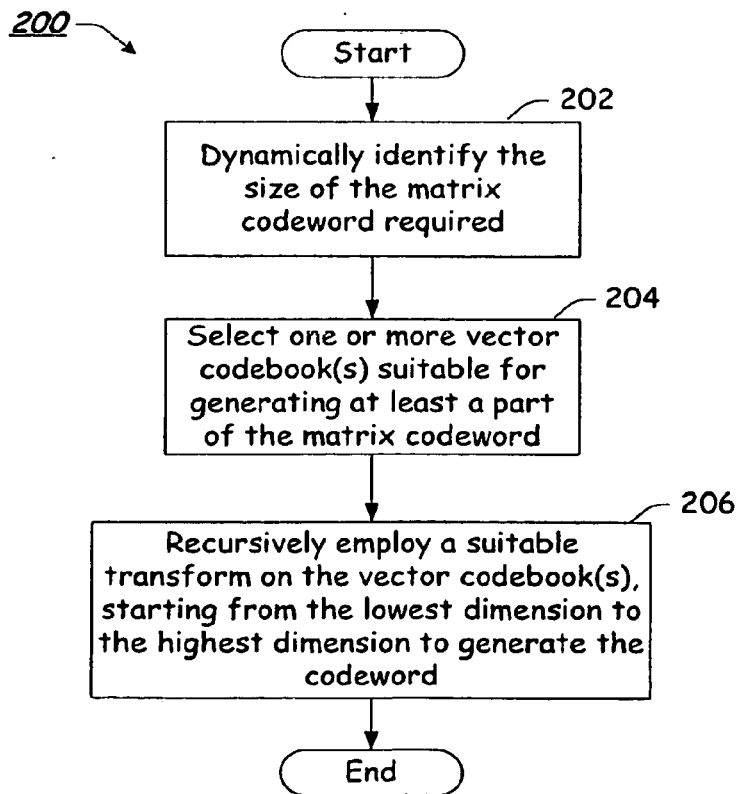


FIG. 3

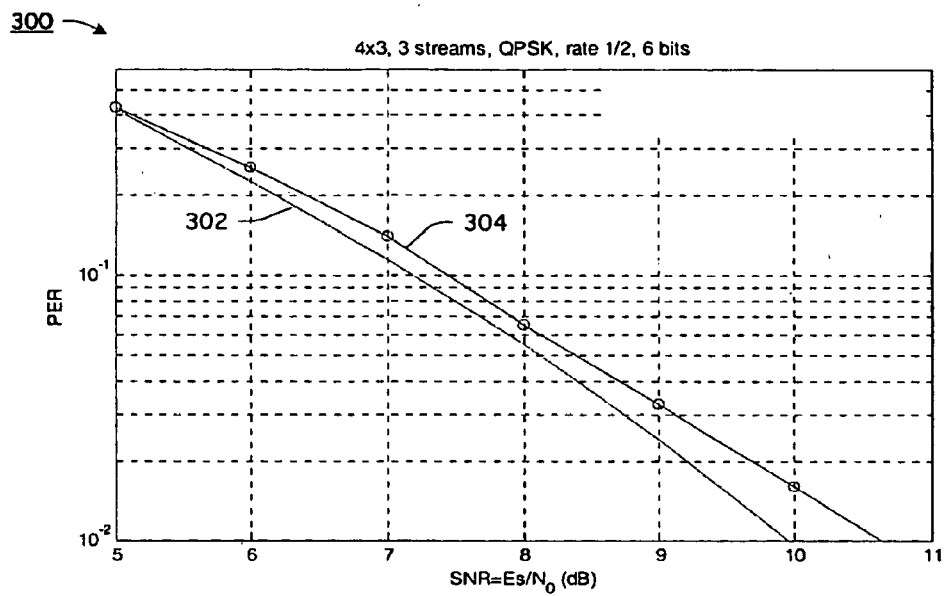


FIG. 4

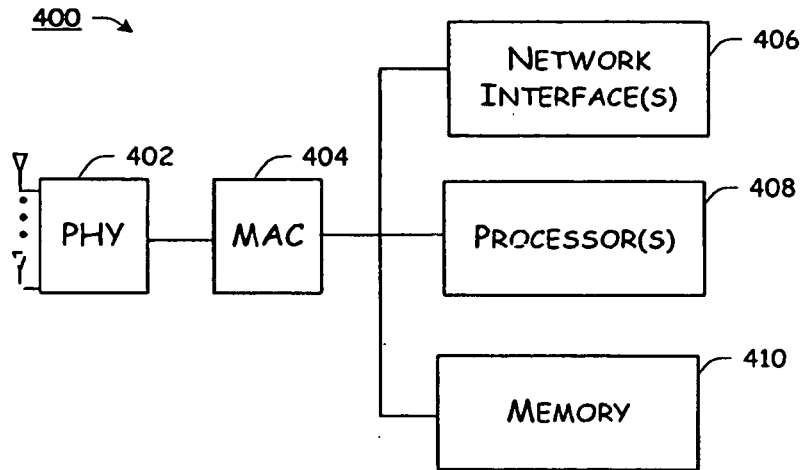
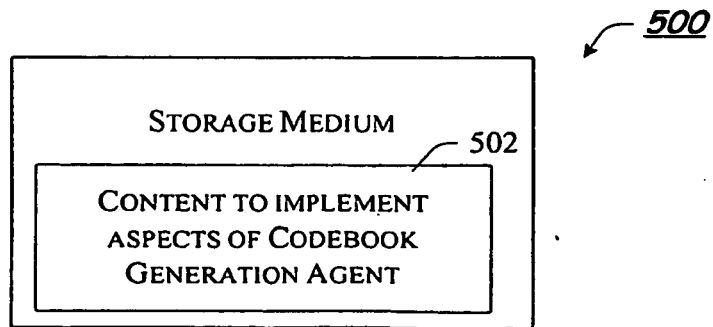


FIG. 5



CODEBOOK GENERATION SYSTEM AND ASSOCIATED METHODS

CROSS-REFERENCE OF RELATED APPLICATIONS

[0001] This application claims the benefit of, and priority to, previously filed U.S. patent application Ser. No. 12/584,009 entitled “Codebook Generation System and Associated Methods” filed on Aug. 28, 2009, a continuation of U.S. patent application Ser. No. 11/036,906, entitled “Codebook Generation System and Associated Methods” filed on Jan. 13, 2005, the subject matter of both of the above are hereby incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] Embodiments of the invention are generally directed to communication systems and, more particularly, to a codebook generation system and associated methods.

BACKGROUND

[0003] Closed loop multiple-input-multiple-output (MIMO) systems typically transmit channel state information from a receiver to a transmitter. Transmitting the channel state information consumes bandwidth that might otherwise be available for data traffic.

[0004] Illustratively, conventional frequency division duplex (FDD) systems that employ beamforming (or, closed loop multiple input, multiple output (MIMO), the beamforming matrix (referred to herein as a codeword) generated in response to perceived channel conditions is computed and quantized at the receiver first, and then is provided to the source transmitter (e.g., via feedback). A conventional approach to reduce the overhead associated with this feedback is to provide matrix codebook(s) at each of the transmitter and the receiver, each of the codebook(s) comprising a plurality, or set, of potential beamforming matrixes that may be used depending on the channel conditions perceived at the receiver. When the receiver has identified the appropriate matrix codebook(s), the receiver will typically feed back only an index (instead of the actual matrix entries) that points to the appropriate codeword in the codebook(s) stored at the transmitter.

[0005] Thus, for a different combination of transmit antenna(e) (N_t) and data streams (N_s), a different matrix codebook is required. Conventionally, the size of the codebook is based on the number of transmit antennae and the number of data streams: $N_t \times N_s$. For some systems, e.g., one implementing the developing 802.16e¹, N_t and N_s are currently less than five (5) but are likely to increase to eight (8). Therefore, a substantial number of N_t by N_s combinations are anticipated, requiring a significant amount of memory within mobile communication devices in order to store such a large number of codebooks.

¹See, e.g., the ANSI/IEEE Std 802.16-2001 Standard for Local and Metropolitan area networks Part 16: Air Interface for Fixed Broadband Wireless Access Systems, its progeny and supplements thereto (e.g., 802.16a, .16d, and .16e).

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements and in which:

[0007] FIG. 1 is a block diagram of an example communication system within which embodiments of the invention may be practiced;

[0008] FIG. 2 is a flow chart of an example method for generating codebook(s), according to one embodiment;

[0009] FIG. 3 provides a graphical representations of the performance of embodiments of the invention versus a conventional techniques;

[0010] FIG. 4 is a block diagram of an example communications device incorporating one or more embodiments of the invention; and

[0011] FIG. 5 is a block diagram of an example article of manufacture including content which, when executed by an accessing machine, causes the machine to implement one or more aspects of embodiment(s) of the invention.

DETAILED DESCRIPTION

[0012] Embodiments of a codebook generation system and associated methods are generally presented. According to one embodiment, described more fully below, a codebook generation agent (CGA) is presented which may implement a method for generating one or more matrix codebooks from vector codebooks.

[0013] According to one embodiment, the CGA is implemented in mobile devices (e.g., stations, subscriber units, handsets, laptops, etc.), although the invention is not limited in this regard. As developed more fully below, the CGA may develop one or more matrix codebook(s) from matrix code-words that are dynamically generated from vector codebook (s) for 2-, 3-, 4-, . . . , N-unit vectors already resident on the device in support of other features (e.g., single data stream beamforming). In this regard, the use of the vector codebook (s) for 2-, 3- and 4-unit vectors does not add any extra complexity or memory drain to the mobile device. On the contrary, by dynamically generating the matrix codebooks rather than having them stored on the mobile device, enables the mobile device to utilize the memory normally consumed by the matrix codebooks in support of other features and/or services.

[0014] More particularly, as developed more fully below, the CGA may implement one or more of four (4) disclosed techniques for generating the matrix codebooks. According to some embodiments, the codebook generation agent may leverage the Householder reflection and an appropriate one or more vector codebook(s) of 2-, 3- and/or 4-unit vector matrix (ces) to generate one or more suitable matrix codeword(s) for compilation into a matrix codebook for a given set of channel conditions.

[0015] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

[0016] Technical detail regarding some of the operating characteristics of the mobile devices and/or the wireless communication network(s) in which the CGA may be implemented may be found in, e.g., the IEEE 802.11, 1999 Edition; Information Technology Telecommunications and Information Exchange Between Systems—Local and Metropolitan

Area Networks—Specific Requirements, Part 11: WLAN Medium Access Control (MAC) and Physical (PHY) Layer Specifications, its progeny and supplements thereto (e.g., 802.11a, .11g and .11n). See, also, the IEEE Std 802.16-2001 IEEE Std. 802.16-2001 IEEE Standard for Local and Metropolitan area networks Part 16: Air Interface for Fixed Broadband Wireless Access Systems, its progeny and supplements thereto (e.g., 802.16a, .16d, and .16e).

Example Communications Environment

[0017] In FIG. 1, a block diagram of an example wireless communication environment **100** is depicted within which embodiments of the invention may well be practiced. In accordance with the illustrated example embodiment of FIG. 1, an example communications environment **100** is depicted comprising one wireless communications device **102** in communication with another wireless communications device **106** through a wireless communication link **104**. As used herein, communication environment **100** is intended to represent any of a wide range of wireless communication networks including, but not limited to, a near-field communication (NFC) network, a wireless local area network (WLAN), a wireless metropolitan area network (WMAN), a cellular radiotelephony network, a personal communication system (PCS) network, and the like.

[0018] According to one embodiment, communication network **100** is an 802.16x communication network, and device **102** is a base station while device **106** is a subscriber station, although the scope of the invention is not limited in this regard. In a closed-loop MIMO (or, as above, a beamforming system) the data signal is first weighted by a beamforming matrix V , and then selectively transmitted by a plurality of antennae, as shown. According to one embodiment, the data signal may comprise a number of data streams ($N_1 \dots N_s$), although the invention is not limited in this regard. The number of data streams may represent the number of spatial channels, with appropriate bit-loading, power weighting and sub-carrier assignments, although the invention is not limited in this regard.

[0019] According to one embodiment, with four (4) transmit antennae and three (3) data streams (for ease of illustration), the transmitted signal (x) transmitted via the N_t antennae may be represented as:

$$x = V \times s \quad (1)$$

$$\text{where } V = \begin{bmatrix} v_{11} & v_{12} & v_{13} \\ v_{21} & v_{22} & v_{23} \\ v_{31} & v_{32} & v_{33} \\ v_{41} & v_{42} & v_{43} \end{bmatrix}, \text{ and } s = \begin{bmatrix} s_1 \\ s_2 \\ s_3 \end{bmatrix}$$

[0020] As shown, s is an N_s -vector of data symbols, and V is the N_t by N_s beamforming matrix developed from information (e.g., matrix codebook(s) and/or indices thereto) fed back from a remote receiver. According to one embodiment, the beamforming matrix V is typically unitary, and power/bit loading is applied on vector s , as introduced above.

[0021] Device **106** is depicted comprising a codebook generation agent (CGA) **108** to dynamically generate one or more matrix codebook(s) from which channel state information may be characterized and fed back to the base station, **102**. As introduced above, rather than storing one or more

matrix codebooks, CGA **108** compiles the matrix codebooks necessary to characterize the channel state information from matrix codeword(s) dynamically generated from one or more vector codebook(s) for 2-, 3-, 4-, . . . , N -unit vectors. As discussed more fully below, the vector codebook(s) are recursively applied to a suitable transform (e.g., a Householder reflection) from the lowest-order codebook to the highest order codebook, as necessary to generate the desired size matrix codeword(s) from which the matrix codebook(s) are assembled.

[0022] It will be appreciated that but for the introduction of the CGA **108**, device **106** is intended to represent any of a wide variety of electronic device(s) with wireless communication capability. In some embodiments, CGA **108** may well be implemented within a receiver element of a device. In other embodiments, CGA **108** is responsive to a communicatively coupled receiver to perform the functions described herein. According to some embodiments, CGA **108** may well be implemented in hardware, software, firmware and/or any combination thereof.

Example Operation

[0023] As introduced above, CGA **108** may generate the matrix codebook(s) from the one or more vector codebooks according to a number of techniques, each described more fully below. The first technique disclosed offers the closest approximation to the conventional technique of using stored matrix codebooks. The second through fourth technique disclosed also offer very good results, although with decreased computational complexity. In either case, the computational complexity is more than offset by the reduced memory that need be allocated to the storage of the matrix codebooks.

[0024] Turning to FIG. 2, a flow chart of an example method for dynamically generating one or more matrix codebook(s) is generally presented, according to one embodiment. As shown, the method begins with block **202** by dynamically identifying the size of the matrix codeword(s) required. More particularly, according to one embodiment CGA **108** disposed within, or otherwise responsive to a receiver (e.g., **106**) may be invoked to determine the size of the matrix codebook necessary. According to one embodiment, the size of the codeword required is dependent upon the number of transmit antennae (N_t) and/or the number of spatial data streams (N_s) utilized in the communication channel, although other parameters may be considered as a supplement to, or in place of, N_t and/or N_s . According to one embodiment, the necessary parameters are either supplied to, or perceived by the receiver and/or CGA **108** for use in determining the size of the matrix codeword to generate.

[0025] As shown, CGA **108** is depicted comprising vector codebooks for 2-, 3-, 4-, . . . , N -unit (or, parameter) vectors. Accordingly, CGA **108** dynamically selects the vector codebook(s) suitable for a particular element of the recursive process for generating an element of the matrix codeword(s), as provided more fully below.

[0026] In response to determining the necessary size of the matrix codeword, CGA **108** may dynamically select an appropriate one or more vector codebook(s) suitable for generating at least an element of the matrix codeword, block **204**. According to one embodiment, the vector codebook(s) selected by CGA **108** may depend on which of the techniques will be employed to generate the matrix codeword(s). According to one embodiment, the technique to be used is dynamically selected by CGA **108** and may depend on any of

a number of factors including, but not limited to, the current processing load of the receiver and/or CGA 108, the perceived quality of the channel, and the like. That is, the current processing load of the receiver and/or CGA 108 may be such that a lower complexity codebook generation technique is required. Similarly, if the perceived quality of the channel (e.g., through signal-to-noise ratio, received power level, etc.) is high, CGA 108 may determine that a lower complexity codebook generation technique will provide suitable results, whereas a poorer channel may benefit from use of a more complex technique that more closely approximates the use of conventional (stored) codebooks.

[0027] Once the matrix codebook is generated, conventional techniques for computation and quantization of the proposed beamforming matrix may be employed, such as the one described in co-pending U.S. patent application Ser. No. 10/937,097 entitled Recursive Reduction of Channel State Feedback by Li, et al., commonly assigned to the Assignee of this application, and incorporated by reference herein for all purposes.

[0028] Returning to block 206, as provided above CGA 108 may employ one or more of at least four (4) techniques for recursively generating one or more matrix codeword(s) from vector codebook(s) for 2-, 3-, 4-, . . . N-unit vectors. It will be appreciated that other techniques for generating a matrix codeword from vector codebooks may well be used without deviating from the scope and spirit of the claims, below. Each of the four techniques are presented, as follows.

Technique 1

[0029] According to one embodiment, CGA 108 may generate a matrix codeword, column by column, using vector codebooks starting from the smallest dimension of the matrix codeword and working towards the largest dimension. For example, to generate a 4x3 matrix codeword, CGA 108 may employ unit vectors of dimensions 2, 3, and 4 sequentially, starting from the most inner-most parentheses (or, lowest dimension) and working out towards higher dimensions of the codeword, as shown:

$$V(l_{N_t}, \dots, l_{N_t-N_s+1}) =$$

$$\begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & P_{N_t-1} & & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & P_{N_t-N_s+2} & \begin{bmatrix} 1 & 0 \\ 0 & v_{N_t-N_s+1}(l_{N_t-N_s+1}) \\ 0 & 0 \end{bmatrix} \end{bmatrix}$$

$$P_i = I - \frac{2}{\|w^H w\|} w w^H$$

$$w = e^{-j\phi_1} v_i(l_i) - e_1$$

In the special case, $v_i = e_1$, the householder reflection can be computed as $P_i = I$. Without unnecessary repetition, it is understood that this special treatment is implied in all the following description.

[0030] The N_t by N_s matrix codeword is constructed from the last column recursively, where the iteration starts from the lower, right hand side corner. Successive iteration(s) adds one column and one row to the constructing matrix codeword. In this regard, let $\{v_i(l_i)\}_{l_i=1}^{L_i}$ denote the codebook of i -dimension unit vectors with L_i codewords (i.e. vectors), where l_i is the codeword index. Let $\{v_1(l_1)\}_{l_1=1}^{L_1} = \{1\}$, i.e. $v_1(1) = 1$ and $L_1 = 1$. Let $\{V_{N_t \times N_s}(l)\}_{l=1}^L$ denote the matrix codebook of dimension N_t by N_s with L codewords, where

$$L = \prod_{i=1}^{N_s} L_i.$$

The matrix codebook $\{V_{N_t \times N_s}(l)\}_{l=1}^L$ can be constructed by N_s vector codebooks according to the following pseudo-code:

```

I. FOR  $l_{N_t-N_s+1} = 1:L_{N_t-N_s+1}$ 
I.1. IF  $N_t > N_s$ 
I.1.1.  $V_t = v_{N_t-N_s+1}(l_{N_t-N_s+1})$ 
I.2. ELSE
I.2.1.  $V_t = 1$ 
I.3. END
II. FOR  $l_{N_t-N_s+2} = 1:L_{N_t-N_s+2}$ 
II.1.  $w = e^{-j\phi_1} v_{N_t-N_s+2}(l_{N_t-N_s+2}) - e_1$ ,
      where  $\phi_1$  is the phase of the first entry of  $v_{N_t-N_s+2}(l_{N_t-N_s+2})$  and
       $e_1 = [1, 0, \dots, 0]^T$ .
II.2.  $P_{N_t-N_s+2} = I - \frac{2}{\|w^H w\|} w w^H$ 
II.3.  $V_t = P_{N_t-N_s+2} \begin{bmatrix} 1 & 0 \\ 0 & V_t \end{bmatrix}$ 
III. FOR  $l_{N_t-N_s+3} = 1:L_{N_t-N_s+3}$ 
...
 $N_s$ . FOR  $l_{N_t} = 1:L_{N_t}$ 
 $N_s$ .1.  $w = e^{-j\phi_1} v_{N_t}(l_{N_t}) - e_1$ ,
      where  $\phi_1$  is the phase of the first entry of  $v_{N_t}(l_{N_t})$ .
 $N_s$ .2.  $P_{N_t} = I - \frac{2}{\|w^H w\|} w w^H$ 

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-continued

$$N_{s,3}. \quad V(l) = P_{N_t} \begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & & & \\ \vdots & & V_t & \\ 0 & & & \end{bmatrix},$$

$$\text{where } l = l_{N_t} + \sum_{i=N_t-N_s+1}^{N_t-1} l_i \prod_{j=i+1}^{N_t} L_j$$

N_{s,4.} END

II.4. END

I.4. END

[0031] As shown above, CGA 108 may generate a matrix from the most inner core with the smallest dimension (the lowest dimension) to the full matrix. The lowest dimension core is either 1, or a vector of size N_t-N_s+1. Each expansion, or recursive iteration, effectively increases the size of the matrix by one row and one column. There are N_s FOR loops for N_t>N_s, and there are N_t-1 FOR loops for N_t=N_s. Each FOR loop corresponds to one expansion of the matrix code-word, each expansion generally comprising:

- [0032]** 1) picking an appropriate vector from the vector codebook;
- [0033]** 2) removing the phase of the first element of the vector by e^{-jΦ₁}v_{N_s}(l_{N_t}) and subtract one from the first element of the phase corrected vector w=e^{-jΦ₁}v_{N_s}(l_{N_t})-e₁;
- [0034]** 3) generating a Householder matrix

$$P = I - \frac{2}{\|w\|^2} w w^H;$$

- [0035]** 4) padding zeros and a one in the previous expanded matrix V as

$$\begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & & & \\ \vdots & & V_t & \\ 0 & & & \end{bmatrix};$$

and

- [0036]** 5) multiplying the Householder matrix with the padded matrix to finish one expansion.

[0037] Since the vector steps through the vector codebook, the number of runs for each FOR loop is equal to the number of vectors in the corresponding vector codebook. The index/is the index for the matrix finally generated. It increases as 1, 2, . . . , L_{N_t}*L_{N_t-1} . . . *L_{N_t-N_s+1}, where L_t is the number of vectors in the vector codebook of dimension t.

[0038] To reduce complexity and speed up computation, the phase of the first entry of each vector may be removed when CGA 108 stores each vector codebook as e^{-jΦ₁}v_{N_s}(l_{N_t}). Namely, each first element of each vector in each vector codebook is real (not complex). The real number

$$\frac{2}{\|w\|^2}$$

may also be pre-computed and stored for each vector.

Technique 2

[0039] According to one embodiment, CGA 108 may well implement a second technique to generate one or more matrix codeword(s) from vector codebook(s) for 2-, 3-, 4-, . . . N-unit vectors. In this technique, CGA 108 employs the complementary property of unitary matrix as follows. Instead of generating a N_t by N_s matrix directly, it first generates a N_t by N_t matrix first and then cut a submatrix of dimension N_t by N_s from it.

[0040] This technique is the most efficient when it generates matrix codebook of dimension N_t by (N_t-1). As specified above, the stored N_t-vector codebook has the property that the N_t-vector codewords are spread over the complex N_t-sphere as uniformly as possible, where the minimum angle between any two vectors is maximized. Note that each vector has a complementary, orthogonal subspace, spanned by (N_t-1) orthogonal vectors, and is orthogonal to the vector. The property of the vector codebook implies that the subspaces (i.e. N_t by (N_t-1) matrixes) are uniformly spread, where the minimum angle between any two subspaces is maximized. This maximum minimum angle is a desirable property for N_t by (N_t-1) matrix codebook. The major advantage of scheme 2 is that only one vector codebook is required to generate the N_t by (N_t-1) codebook, while (N_t-1) vector codebooks are required in Technique 1.)

[0041] Technique 2 is also efficient to generate matrix codebook of dimension N_t by N_s, where

$$N_s > \frac{N_t}{2}.$$

For this case, the CGA 108 first generates an N_t×N_t matrix, and then cuts a N_t by N_s submatrix from it as a matrix code-word. The pseudo code of the scheme is as follows, where the notations are already defined, above, in Technique 1. It is assumed that

$$N_s > \frac{N_t}{2}.$$

One advantage of this scheme is that only $N_t - N_s$ vector codebooks are required to generate the $N_t \times N_s$ codebook, while N_s vector codebooks may be required for Technique 1.

I. FOR $l_{N_s+1} = 1:L_{N_s+1}$

$$I.1. w = e^{-j\phi_1} v_{N_s+1}(l_{N_s+1}) - e_1$$

where ϕ_1 is the phase of the first entry of $v_{N_t-N_s+2}(l_{N_t-N_s+2})$

$$\text{and } e_1 = [1, 0 \dots 0]^T.$$

$$I.2. V_t = I - \frac{2}{\|w^H w\|} w w^H$$

II. FOR $l_{N_s+2} = 1:L_{N_s+2}$

$$II.1. w = e^{-j\phi_1} v_{N_s+2}(l_{N_s+2}) - e_1,$$

where ϕ_1 is the phase of the first entry of $v_{N_s+2}(l_{N_s+2})$

$$\text{and } e_1 = [1, 0 \dots 0]^T.$$

$$II.2. P_{N_s+2} = I - \frac{2}{\|w^H w\|} w w^H$$

$$II.3. V_t = P_{N_s+2} \begin{bmatrix} 1 & 0 \\ 0 & V_t \end{bmatrix}$$

III. FOR $l_{N_s+3} = 1:L_{N_s+3}$

... ..

N_s . FOR $l_{N_t} = 1:L_{N_t}$

$$N_s.1. w = e^{-j\phi_1} v_{N_t}(l_{N_t}) - e_1,$$

where ϕ_1 is the phase of the first entry of $v_{N_t}(l_{N_t})$.

$$N_s.2. P_{N_t} = I - \frac{2}{\|w^H w\|} w w^H$$

$$N_s.3. V_t = P_{N_t} \begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & & & \\ \vdots & & & V_t \\ 0 & & & \end{bmatrix}.$$

$N_s.4. V(l)$ = last N_s columns of V_t ,

$$\text{where } l = l_{N_t} + \sum_{i=N_s+1}^{N_t-1} l_i \sum_{j=i+1}^{N_t} L_j$$

$N_s.5.$ END

... ..

II.4. END

I.3. END

Technique 3

[0042] According to one embodiment, CGA 108 may well implement a third technique to generate one or more matrix codeword(s) from vector codebook(s) for 2-, 3-, 4-, ... N-unit vectors. This technique represents a further simplification over technique 2, above. For the generation of an N_t by $(N_t - 1)$ codebook, techniques 2 and 3 are very similar in terms of computational complexity. However, when generating an N_t by N_s codebook with L codewords, this third technique pro-

vides for the use of only one vector codebook with L codewords and span each vector into a N_t by N_t matrix using Householder reflection. The N_t by N_s matrix codebook is formed by taking a N_s by N_s submatrix from each spanned N_t by N_t matrix. Example pseudo code of for technique 3 is as follows:

1. FOR $l = 1:L$

$$2. w = e^{-j\phi_1} v_{N_t}(l) - e_1$$

where ϕ_1 is the phase of the first entry of $v_{N_t}(l)$ and

$$e_1 = [1, 0 \dots 0]^T.$$

$$3. V_t = I - \frac{2}{\|w^H w\|} w w^H$$

4. $V(l)$ = last N_s columns of V_t

5. END

Technique 4

[0043] According to one embodiment, CGA 108 may employ yet a fourth technique to generate matrix codeword(s) from vector codebook(s) for 2, 3, 4 ... N-unit vectors, according to one embodiment. According to one embodiment, the fourth technique represents a further simplification of technique three, above. In particular, in step 4 of technique 3, CGA 108 may take any N_s columns of V_t , such as the first N_s columns, or N_s columns extracted for the N_t columns.

[0044] It should be appreciated that combinations of techniques 1-4 are possible, without deviating from the scope and spirit of the invention. For example, techniques 1 and 2 expand the matrix from a small core to a big matrix iteratively as shown above. According to one embodiment, the small core (or, lowest dimension) may be generated using other techniques. For example, to generate a 4x3 matrix, the core (lowest dimension) used in technique 1 may be generated by technique 3. In this regard, CGA 108 may use technique 3 to generate a core matrix of size 3x2 using a 3-vector codebooks, and then use the remaining teachings of technique 1 to finish the generation of 4x3 using the 3x2 core as the lowest dimension.

[0045] To illustrate the algorithm, we use an example of 3/6 bits vector codebooks to generate all the necessary matrix codebooks. In 802.16e, it may be desirable to implement codebooks, whose size $L=3n$ bits, where n is integer.

[0046] Since there are many combinations of N_t , N_s , and L and each of them requires a corresponding codebook, the storage of all codebooks are burdensome. A set of codebooks is proposed, which can be dynamically generated with low complexity.

[0047] For small size codebooks, i.e. 2x1, 3x1, and 4x1 with 3 bit index, three optimized, random codebooks are stored. For 3x1 and 4x1 with 6 bit index, two structured codebooks are proposed, which can be dynamically generated using an improved Hochwald method. For all the other matrix codebooks such as 3x2 and 4x2, structured codebooks are proposed, which can also be dynamically generated with low complexity.

[0048] An example of stored vector codebooks for 2x1, 3x1, and 4x1 with 3 bit index are listed below in Table 1, Table 2, and Table 3. The notation $v(N_t, L)$ denotes the vector codebook (i.e. the set of complex unit vectors), which consists of 2^L unit vectors of a dimension N_t . The number L is the number of bits required for the feedback index that can indicate any vector in the codebook.

TABLE 1

v(2,3)								
Vector index	1	2	3	4	5	6	7	8
v ₁	1	0.794	0.794	0.794	0.794	0.329	0.511	0.329
v ₂	0	-0.580 + 0.182i	0.058 + 0.605i	-0.298 - 0.530i	0.604 + 0.069i	0.661 + 0.674i	0.475 - 0.716i	-0.878 - 0.348i

TABLE 2

v(3,3)								
Vector index	1	2	3	4	5	6	7	8
v ₁	1	0.500	0.500	0.500	0.500	0.495	0.500	0.500
v ₂	0	-0.720 - 0.313i	-0.066 + 0.137i	-0.006 + 0.653i	0.717 + 0.320i	0.482 - 0.452i	0.069 - 0.139i	-0.005 - 0.654i
v ₃	0	0.248 - 0.268i	-0.628 - 0.576i	0.462 - 0.332i	-0.253 + 0.263i	0.296 - 0.480i	0.620 + 0.585i	-0.457 + 0.337i

TABLE 3

v(4,3)								
Vector index	1	2	3	4	5	6	7	8
v ₁	1	0.378	0.378	0.378	0.378	0.378	0.378	0.378
v ₂	0	-0.270 - 0.567i	-0.710 + 0.133i	0.283 - 0.094i	-0.084 + 0.648i	0.525 + 0.353i	0.206 - 0.137i	0.062 - 0.333i
v ₃	0	0.596 + 0.158i	-0.235 - 0.147i	0.070 - 0.826i	0.018 + 0.049i	0.412 + 0.183i	-0.521 + 0.083i	-0.346 + 0.503i
v ₄	0	0.159 - 0.241i	0.137 + 0.489i	-0.280 + 0.049i	-0.327 - 0.566i	0.264 + 0.430i	0.614 - 0.375i	-0.570 + 0.211i

The matrix codebooks for multiple stream transmission are constructed from the vector codebooks in the previous section using three operations depicted next. We assume that all unit vectors in the section are complex with unit norm and the first entry of each vector is real. The first operation is called Householder reflection transformation. It is to generate a unitary N by N matrix H(v) using a unit N vector v as:

$$H(v) = \begin{cases} I, & v = e_1 \\ I - pw w^H, & \text{otherwise,} \end{cases} \quad (1)$$

where w=v-e₁ and e₁=[1 0 . . . 0]^T;

$$p = \frac{2}{\|w^H w\|}$$

and it is a real number that can be pre-computed and stored for each vector in the tables; I is the N by N identity matrix; ^H denotes the conjugate transpose operation.

[0049] The other two operations are built on Householder transformation. One of them is called H-concatenation, and the other is called H-expansion, where the ‘‘H’’ stands for Householder. The H-concatenation (HC) generates a N by M+1 unitary matrix from a unit N vector and a unitary N-1 by M matrix using Householder transformation as

$$HC(v_N, A_{(N-1) \times M})H(v_N) = \begin{bmatrix} 1 & 0 & \dots & 0 \\ 0 & & & \\ \vdots & & A_{(N-1) \times M} & \\ 0 & & & \end{bmatrix}, \quad (3)$$

where N-1 ≥ M; the N-1 by M matrix unitary matrix has property A^HA=I. Since both terms on the left are unitary the output of HC is a unitary matrix. The H-expansion (HE) generates a N by l matrix from a unit N vector, v_N, by taking the last M columns of H(v) as

$$HE(v_N, l) = H(v_N)_{:,N-l+1:N}, \quad (4)$$

[0050] CGA 108 may selectively employ one or more of the operations defined in (2), (3), and (4) to jointly generate matrix codebooks as follows. In Table, by K bit codebook we mean the codebook has 2^K matrixes, which requires a K bit feedback index.

TABLE 4

Construction operations for N _t by N _s beamforming matrix with 3, 6, and 9 bit codebooks.			
		N _s	
N _t		3	4
2 ant., 3 bit codebook	H(v(2, 3))		
3 ant., 3 bit codebook	HE(v(3, 3), 2)	H(v(3, 3))	
4 ant., 3 bit codebook	HE(v(4, 3), 2)	HE(v(4, 3), 3)	H(v(4, 3))

TABLE 4-continued

Construction operations for N_r by N_t beamforming matrix with 3, 6, and 9 bit codebooks.			
N_r	N_t		
	2	3	4
3 ant., 6 bit codebook	HC(v(3, 3), v(2, 3))	HC(v(3, 3), H(v(2, 3)))	
4 ant., 6 bit codebook	HC(v(4, 3), v(3, 3))	HE(v(4, 6), 3)	H(v(4, 6))
3 ant., 9 bit codebook	HC(v(3, 6), v(2, 3))	HC(v(3, 6), H(v(2, 3)))	
4 ant., 9 bit codebook	HC(v(4, 6), v(3, 3))	HC(v(4, 3), HC(v(3, 3), (2, 3)))	HC(v(4, 3), HC(v(3, 3), H(v(2, 3))))

The set notation $v(N_r, L)$ in the input parameter of the operations (i.e. H, HC, and HE) denotes that each vector in the codebook $v(N_r, L)$ is sequentially taken as an input parameter to the operations. The feedback index is constructed by concatenating all the indexes of the input argument vector codebooks in binary format. For example, the feedback index of HC(v(4,6), v(3,3)) is constructed as i_2j_2 , where i_2 and j_2 are the indexes of the vectors in codebook v(4,6) and v(3,3) in binary format respectively.

Performance Analysis

[0051] Turning briefly to FIG. 3, a graphical representation of the performance improvements achieved through use of the codebook generation agent is depicted, according to one embodiment of the invention. The proposed codebook generation techniques were simulated and compared to conventional techniques. The frequency permutation is Band AMC in 802.16e D5 standard. ITU Pedestrian B, LOS channel model with 0.2 transmit antenna correlation is employed. Perfect channel estimation and slow speed are assumed. The amount of feedback from the mobile device (e.g., **106**) to the base station (e.g., **102**) is 6 bits per AMC band. With reference to FIG. 3, the feedback is the codebook index pointing a matrix codeword in a 64-codeword codebook. Packet error rate (PER) at the downlink is simulated, where packet size is 1000 bytes. As shown in FIG. 3, the simulation results demonstrate that the proposed technique(s) **302** provide similar or better performance with much lower storage complexities than conventional technique(s) **304**.

[0052] Having introduced the communication environment and operating characteristics of CGA **108** with respect to FIGS. 1 and 2, above, reference is now directed to FIG. 4 which provides an example electronic device architecture within which the CGA **108** may be practiced.

[0053] FIG. 4 illustrates a block diagram of an example architecture of an electronic device within which the teachings of the present invention may be practiced, according to one embodiment. Electronic device **400** includes antennas, physical layer (PHY) **402**, media access control (MAC) layer **404**, network interface(s) **406**, processor(s) **408**, and memory **410**. In some embodiments, electronic device **400** may be a station capable of generating one or more matrix codebook(s) from matrix codeword(s) dynamically generated from vector codebook(s) for 2, 3, 4, . . . N-unit vectors by selectively performing Householder transformations as described above. In other embodiments, electronic device **400** may be a station that receives quantized column vectors, and performs beamforming in a MIMO system. For example, electronic device

400 may be utilized in a wireless network as station **102** or station **104** (FIG. 1). Also for example, electronic device **400** may be a station capable of performing the calculations shown in any of the equations above.

[0054] In some embodiments, electronic device **400** may represent a system that includes an access point, a mobile station, a base station, or a subscriber unit as well as other circuits. For example, in some embodiments, electronic device **400** may be a computer, such as a personal computer, a workstation, or the like, that includes an access point or mobile station as a peripheral or as an integrated unit. Further, electronic device **400** may include a series of access points that are coupled together in a network.

[0055] In operation, device **400** may send and receive signals using one or more of the antennas, wherein the signals are processed by the various elements shown in FIG. 4. As used herein, the antennae may be an antenna array or any type of antenna structure that supports MIMO processing. Device **400** may operate in partial compliance with, or in complete compliance with, a wireless network standard such as, e.g., the 802.11 or 802.16 standards introduced above.

[0056] Physical layer (PHY) **402** is selectively coupled to one or more of the antennae to interact with a wireless network. PHY **402** may include circuitry to support the transmission and reception of radio frequency (RF) signals. For example, in some embodiments, PHY **402** may include an RF receiver to receive signals and perform "front end" processing such as low noise amplification (LNA), filtering, frequency conversion or the like. Further, in some embodiments, PHY **402** may include transform mechanisms and beamforming circuitry to support MIMO signal processing. Also for example, in some embodiments, PHY **402** may include circuits to support frequency up-conversion, and an RF transmitter.

[0057] Media access control (MAC) layer **404** may be any suitable media access control layer implementation. For example, MAC **404** may be implemented in software, or hardware or any combination thereof. In some embodiments, a portion of MAC **404** may be implemented in hardware, and a portion may be implemented in software that is executed by processor **408**. Further, MAC **404** may include a processor separate from processor **408**.

[0058] In operation, processor **408** may read instructions and data from memory **410** and perform actions in response thereto. For example, processor **408** may access instructions from memory **410** and perform method embodiments of the present invention, such as method **200** (FIG. 2) or other methods described herein. In this regard, processor **408** is intended to represent any type of processor, including but not limited to, a microprocessor, a digital signal processor, a microcontroller, or the like.

[0059] Memory **410** represents an article that includes a machine readable medium. For example, memory **410** represents a random access memory (RAM), dynamic random access memory (DRAM), static random access memory (SRAM), read only memory (ROM), flash memory, or any other type of article that includes a medium readable by processor **408**. Memory **410** may store instructions for performing the execution of the various method embodiments of the present invention. Memory **410** may also store vector codebooks of 2, 3, 4, . . . N-unit vectors, although the invention is not limited in this respect.

[0060] Network interface **406** may provide communications between electronic device **400** and other systems. For

example, in some embodiments, electronic device **400** may be an access point that utilizes network interface **406** to communicate with a wired network or to communicate with other access points. In some embodiments, electronic device **400** may be a network interface card (NIC) that communicates with a computer or network using a bus or other type of port. **[0061]** As used herein, embodiments of CGA **108** may well be implemented in one or more of PHY **402**, MAC **404**, processor(s) **408**, and/or combinations thereof. As introduced above, CGA **108** may well be implemented in hardware, software, firmware or combinations thereof.

[0062] Although the various elements of device **400** are depicted as disparate elements in FIG. **4**, embodiments are envisioned that may combine one or more elements, or that may contain more elements. For example, the circuitry of processor **408**, memory **410**, network interface **406**, and MAC **404** may well be integrated into a single integrated circuit. Alternatively, memory **410** may be an internal memory within processor **408**, or may be a microprogram control store within processor **410**. In some embodiments, the various elements of device **400** may be separately packaged and mounted on a common circuit board. In other embodiments, the various elements are separate integrated circuit dice packaged together, such as in a multi-chip module, and in still further embodiments, various elements are on the same integrated circuit die.

Alternate Embodiment(s)

[0063] FIG. **5** illustrates a block diagram of an example storage medium comprising content which, when invoked, may cause an accessing machine to implement one or more aspects of the codebook generation agent **108** and/or associated methods **300**. In this regard, storage medium **500** may include content **502** (e.g., instructions, data, or any combination thereof) which, when executed, causes an accessing appliance to implement one or more aspects of the codebook generation agent **262** described above.

[0064] The machine-readable (storage) medium **500** may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, magnet or optical cards, flash memory, or other type of media/machine-readable medium suitable for storing electronic instructions. Moreover, the present invention may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a modem, radio or network connection). As used herein, all of such media is broadly considered storage media.

[0065] It should be understood that embodiments of the present invention may be used in a variety of applications. Although the present invention is not limited in this respect, the circuits disclosed herein may be used in many apparatuses such as in the transmitters and receivers of a radio system. Radio systems intended to be included within the scope of the present invention include, by way of example only, wireless local area networks (WLAN) devices and wireless wide area network (WWAN) devices including wireless network interface devices and network interface cards (NICs), base stations, access points (APs), gateways, bridges, hubs, cellular radiotelephone communication systems, satellite communication systems, two-way radio communication systems, one-way pagers, two-way pagers, personal communication sys-

tems (PCS), personal computers (PCs), personal digital assistants (PDAs), sensor networks, personal area networks (PANs) and the like, although the scope of the invention is not limited in this respect. Such devices may well be employed within any of a variety of

[0066] Embodiments of the present invention may also be included in integrated circuit blocks referred to as core memory, cache memory, or other types of memory that store electronic instructions to be executed by the microprocessor or store data that may be used in arithmetic operations. In general, an embodiment using multistage domino logic in accordance with the claimed subject matter may provide a benefit to microprocessors, and in particular, may be incorporated into an address decoder for a memory device. Note that the embodiments may be integrated into radio systems or hand-held portable devices, especially when devices depend on reduced power consumption. Thus, laptop computers, cellular radiotelephone communication systems, two-way radio communication systems, one-way pagers, two-way pagers, personal communication systems (PCS), personal digital assistants (PDA's), cameras and other products are intended to be included within the scope of the present invention.

[0067] The present invention includes various operations. The operations of the present invention may be performed by hardware components, or may be embodied in machine-executable content (e.g., instructions), which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the operations. Alternatively, the operations may be performed by a combination of hardware and software. Moreover, although the invention has been described in the context of a computing appliance, those skilled in the art will appreciate that such functionality may well be embodied in any of number of alternate embodiments such as, for example, integrated within a communication appliance (e.g., a cellular telephone).

[0068] In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. Any number of variations of the inventive concept are anticipated within the scope and spirit of the present invention. In this regard, the particular illustrated example embodiments are not provided to limit the invention but merely to illustrate it. Thus, the scope of the present invention is not to be determined by the specific examples provided above but only by the plain language of the following claims.

What is claimed is:

1. An apparatus, comprising:

a processor circuit arranged to select a precoding matrix based on an index received from a remote device over a communication channel of a closed-loop multiple-input and multiple-output (MIMO) orthogonal frequency-division multiple access (OFDMA) system, the precoding matrix constructed by applying a transform to one or more vectors, and precode information with the precoding matrix for transmission over multiple transmitter antennae.

2. The apparatus of claim **1**, the processor circuit arranged to select a vector from a codebook, and apply a transform to the selected vector to form the precoding matrix.

3. The apparatus of claim 1, the processor circuit arranged to apply a Householder reflection transform to a vector to form a matrix of multiple columns.

4. The apparatus of claim 1, the processor circuit arranged to apply a transform to a vector to form an $N \times N$ matrix.

5. The apparatus of claim 1, the processor circuit arranged to apply a transform to a vector to form a 4×4 matrix.

6. The apparatus of claim 1, the processor circuit arranged to select a subset of columns from a matrix of multiple columns as the precoding matrix.

7. The apparatus of claim 1, comprising:

a memory communicatively coupled to the processor circuit, the memory to store the one or more vectors; and
a physical layer (PHY) communicatively coupled to the processor circuit and the multiple transmitter antennae to interact with the remote device.

8. A device, comprising:

a receiver arranged to receive an index for a precoding matrix over a communication channel of a closed-loop multiple-input and multiple-output (MIMO) orthogonal frequency-division multiple access (OFDMA) system; and

a processor circuit communicatively coupled to the receiver, the processor circuit arranged to select a precoding matrix based on the received index, the precoding matrix constructed by applying a transform to one or more vectors, and precode information with the precoding matrix; and

a radio frequency (RF) transmitter communicatively coupled to the processor circuit, the RF transmitter arranged to transmit electromagnetic representations of the precoded information over multiple transmitter antennae.

9. The device of claim 8, the processor circuit arranged to select a vector from a codebook, and apply a transform to the selected vector to form the precoding matrix.

10. The device of claim 8, the processor circuit arranged to apply a Householder reflection transform to a vector to form a matrix of multiple columns.

11. The device of claim 8, the processor circuit arranged to apply a transform to a vector to form an $N \times N$ matrix.

12. The device of claim 8, the processor circuit arranged to apply a transform to a vector to form a 4×4 matrix.

13. The device of claim 8, the processor circuit arranged to select a subset of columns from a matrix of multiple columns as the precoding matrix for the RF transmitter.

14. The device of claim 8, wherein the RF transmitter utilizes two transmitter antennae (N_t).

15. The device of claim 8, wherein the RF transmitter utilizes four transmitter antennae (N_t).

16. A communications device, comprising:

a storage medium comprising content; and

a processor circuit, communicatively coupled with the storage medium, to select a precoding matrix based on an index received from a remote device over a communication channel of a closed-loop multiple-input and multiple-output (MIMO) orthogonal frequency-division multiple access (OFDMA) system, the precoding matrix constructed by applying a transform to one or more vectors, and precode information with the precoding matrix for transmission over multiple transmitter antennae.

17. The communications device of claim 16, the processor circuit arranged to select a vector from a codebook, and apply a transform to the selected vector to form the precoding matrix.

18. The communications device of claim 16, the processor circuit arranged to apply a Householder reflection transform to a vector to form a matrix of multiple columns.

19. The communications device of claim 16, the processor circuit arranged to select a subset of columns from a matrix of multiple columns as the precoding matrix.

20. The communications device of claim 16, comprising a radio frequency (RF) transmitter communicatively coupled to the processor circuit, the RF transmitter arranged to transmit electromagnetic representations of the precoded information over the multiple transmitter antennae, wherein the RF transmitter utilizes an even number of transmitter antennae (N_t).

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