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(54) **LATERAL ELECTROCHEMICAL ETCHING OF III-NITRIDE MATERIALS FOR MICROFABRICATION**

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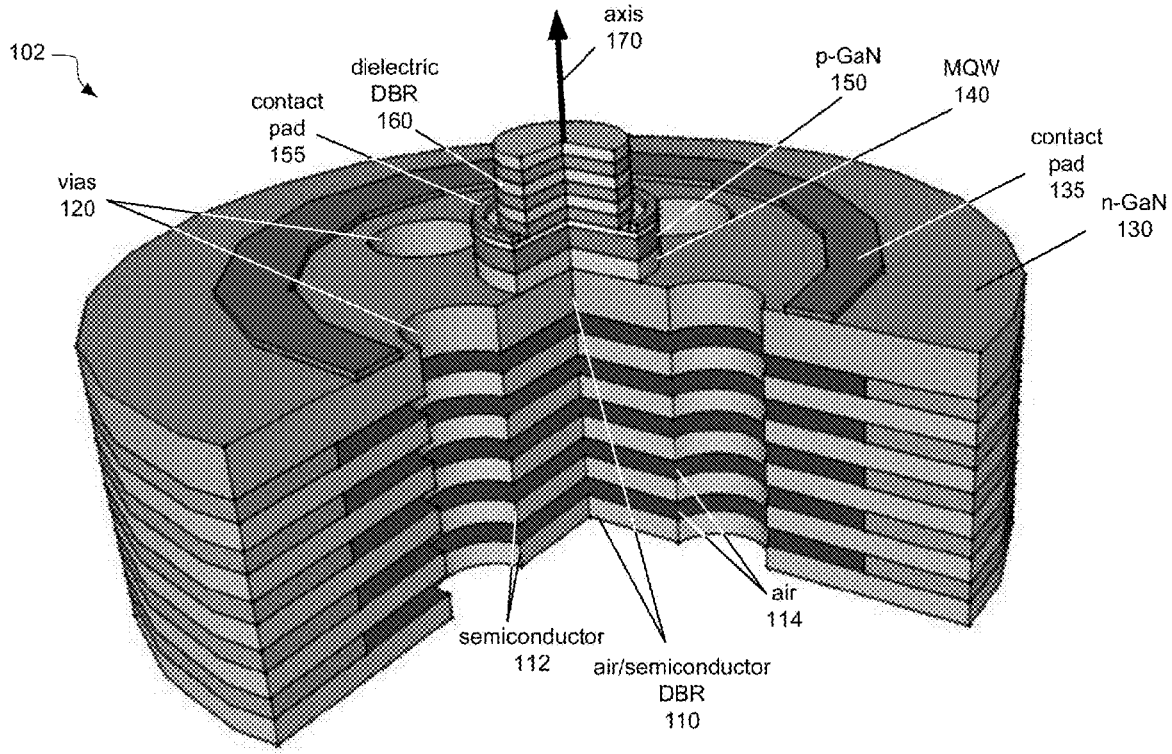
H01S 5/187	(2006.01)

(52) **U.S. Cl.**

CPC ***H01S 5/34333*** (2013.01); ***H01S 5/187*** (2013.01); ***H01S 5/18363*** (2013.01); ***H01S 5/18341*** (2013.01)

(57) **ABSTRACT**

Conductivity-selective lateral etching of III-nitride materials is described. Methods and structures for making vertical cavity surface emitting lasers with distributed Bragg reflectors via electrochemical etching are described. Layer-selective, lateral electrochemical etching of multi-layer stacks is employed to form semiconductor/air DBR structures adjacent active multiple quantum well regions of the lasers. The electrochemical etching techniques are suitable for high-volume production of lasers and other III-nitride devices, such as lasers, HEMT transistors, power transistors, MEMs structures, and LEDs.



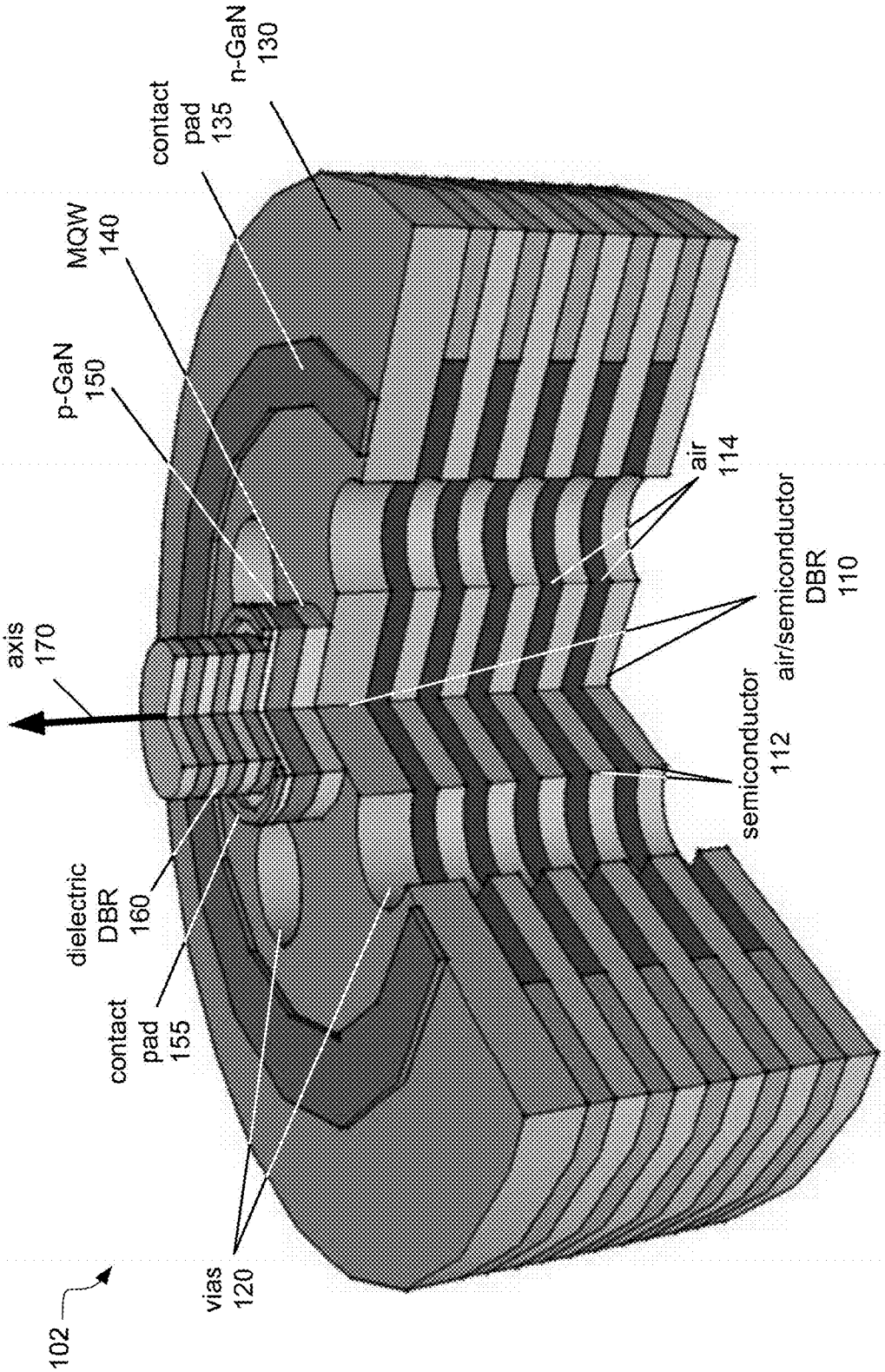

n-GaN 130
contact pad 135
MQW 140
p-GaN 150
air 114
air/semiconductor DBR 110
axis 170
semiconductor 112
dielectric DBR 160
contact pad 155
vias 120
102

FIG. 1

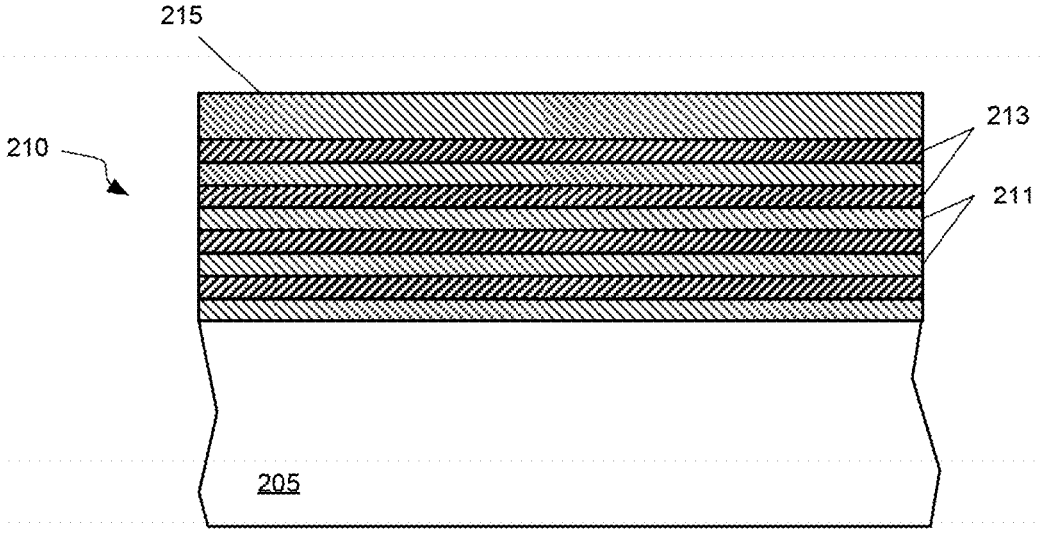


FIG. 2A

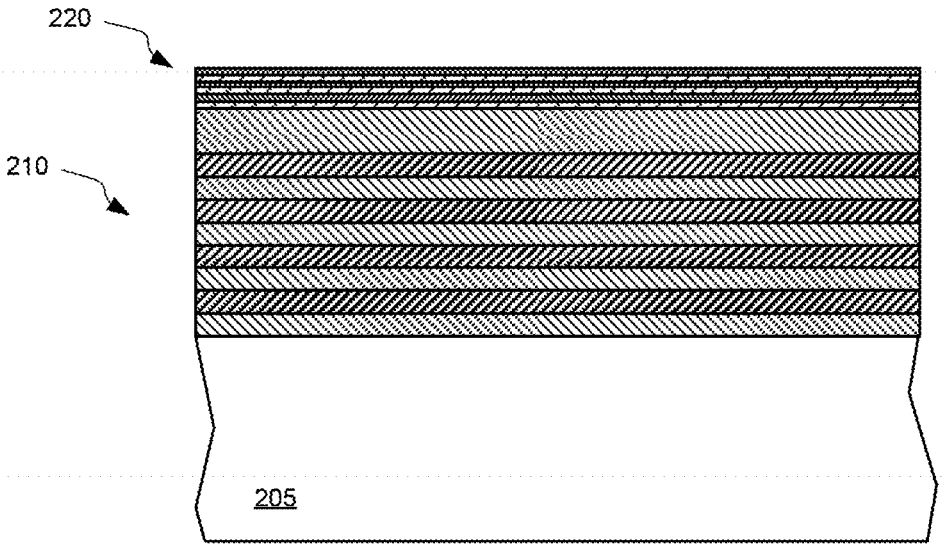


FIG. 2B

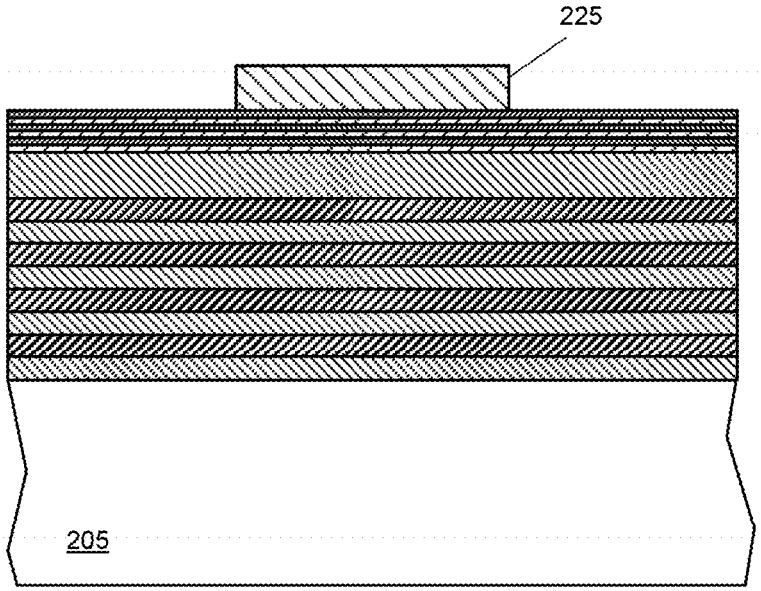


FIG. 2C

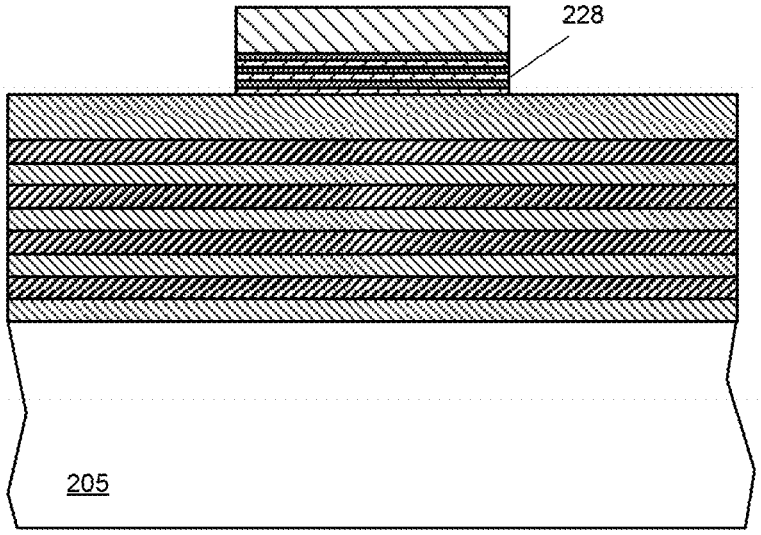


FIG. 2D

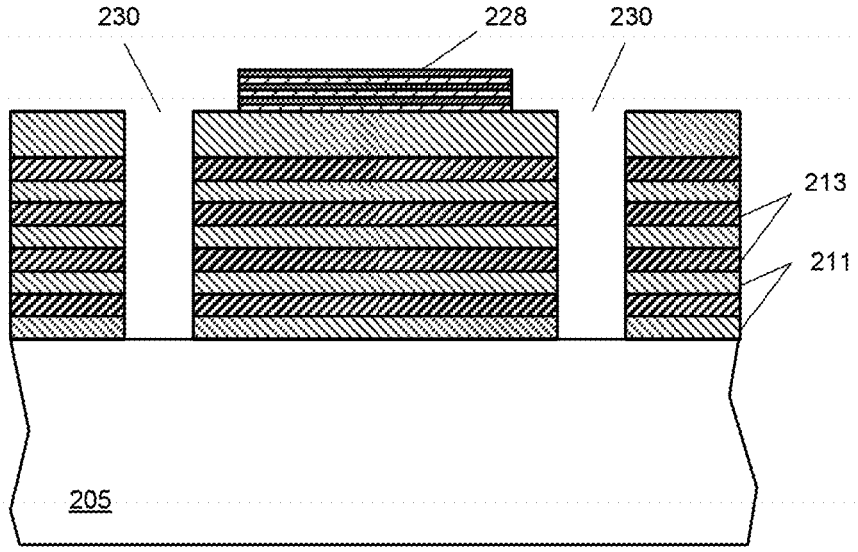


FIG. 2E

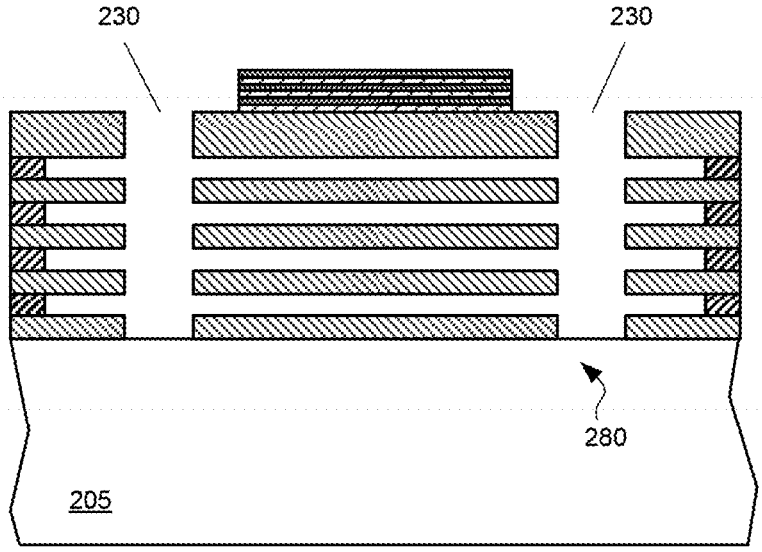


FIG. 2F

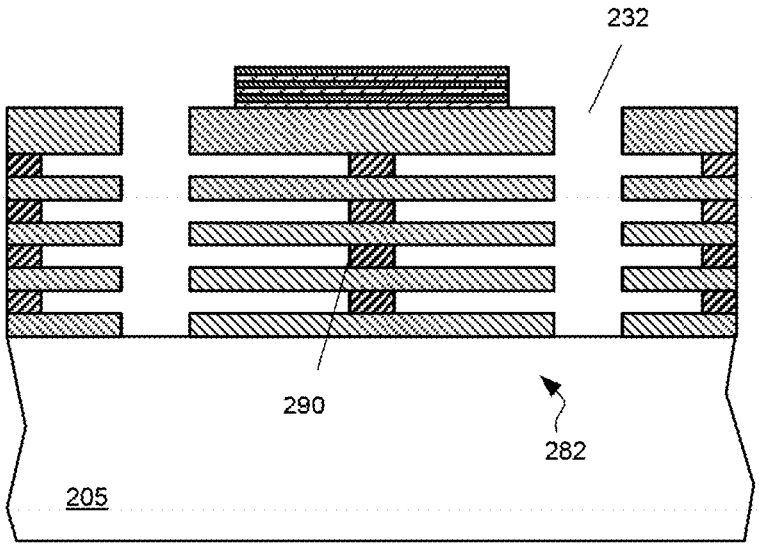


FIG. 2G

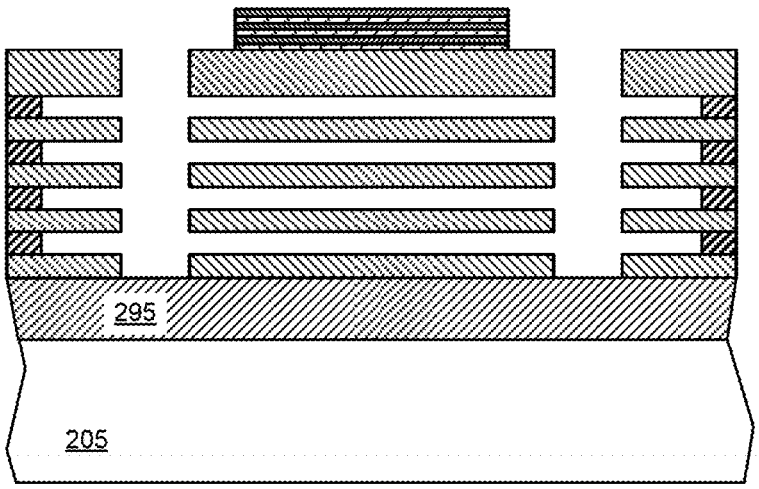


FIG. 2H

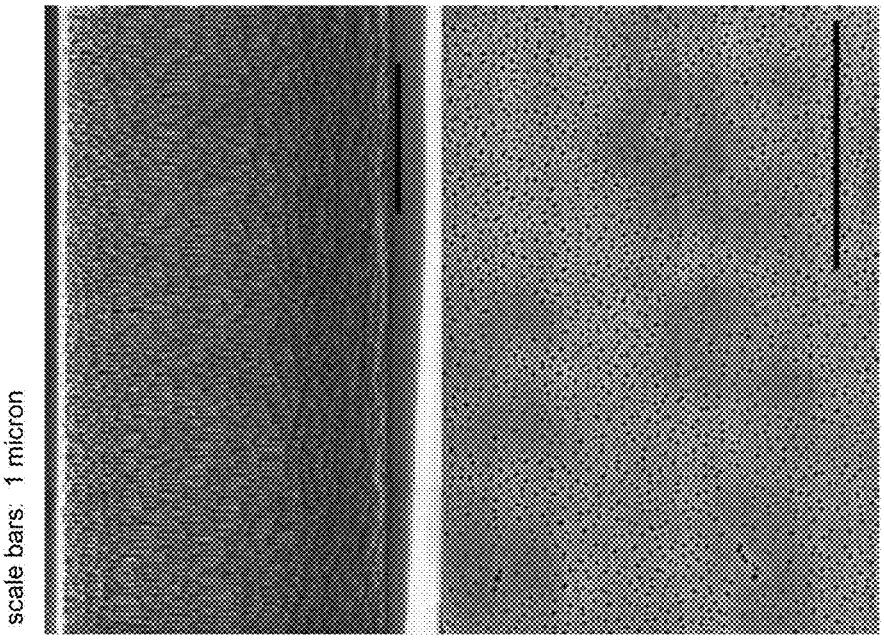

scale bars: 1 micron

FIG. 3B

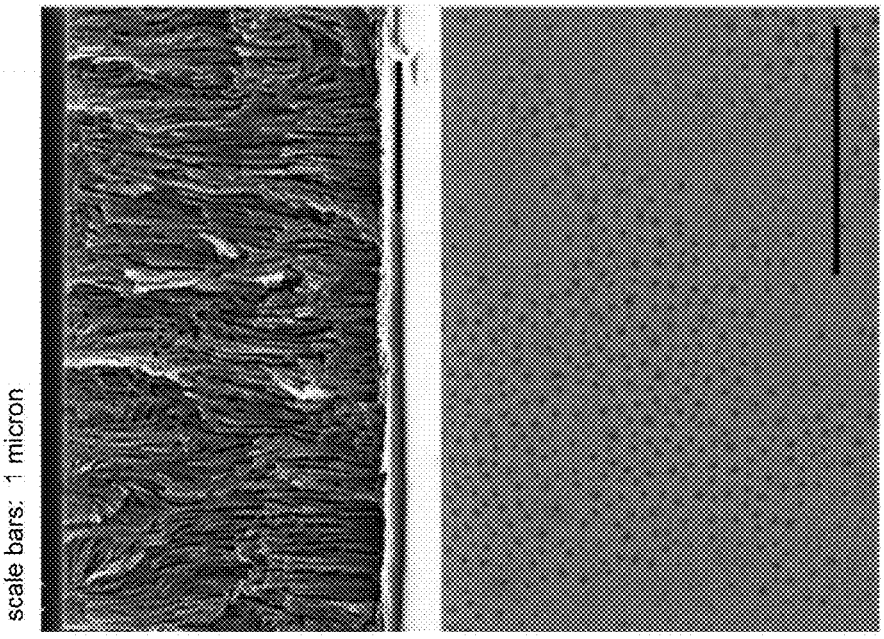

scale bars: 1 micron
cross-section
plan view

FIG. 3A

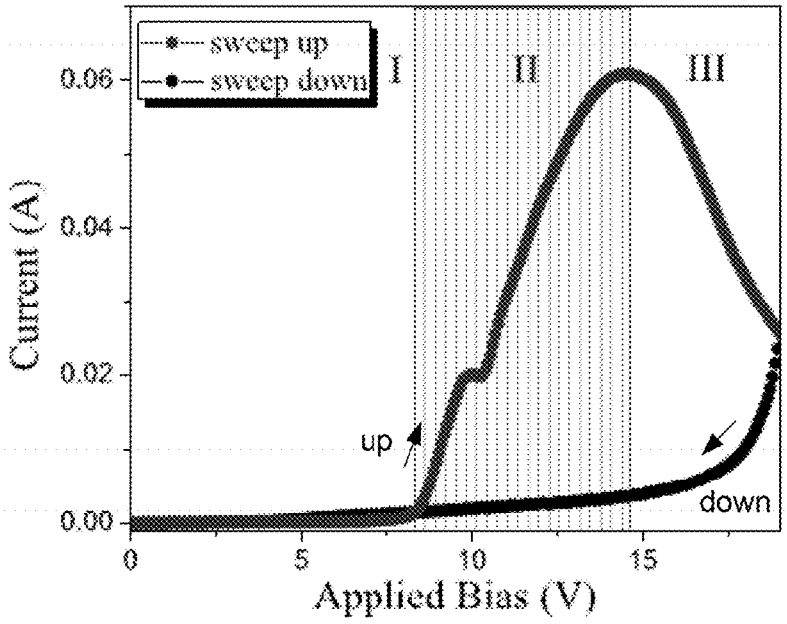


FIG. 4

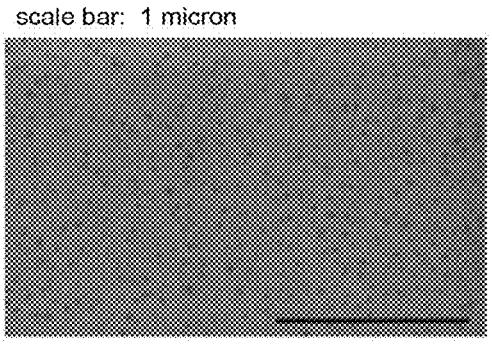


FIG. 5A

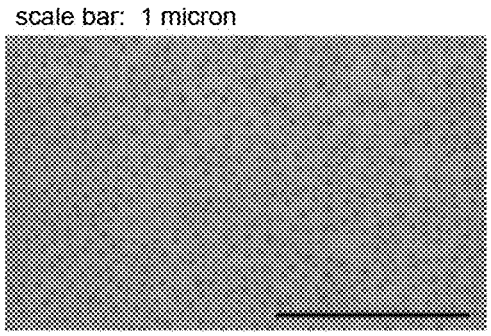


FIG. 5B

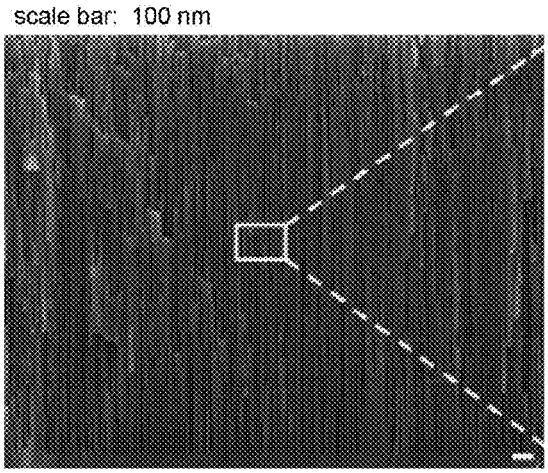


FIG. 6A

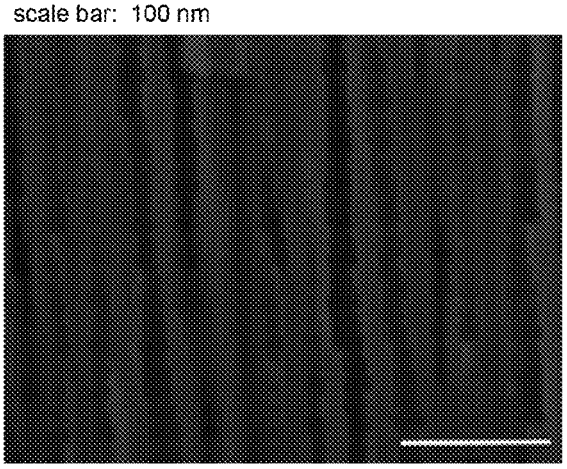


FIG. 6B

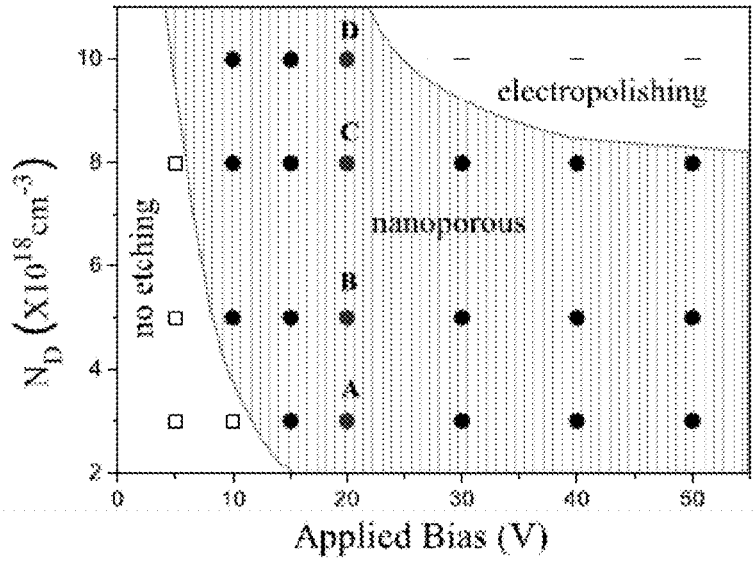


FIG. 7

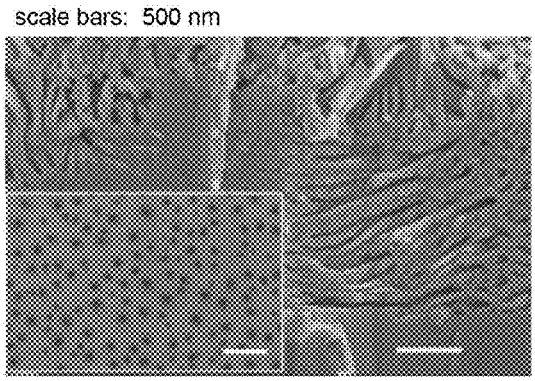


FIG. 8A

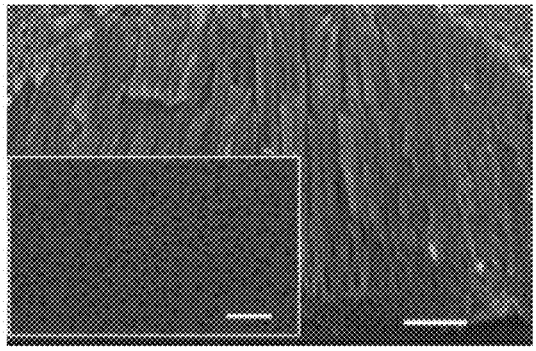


FIG. 8B

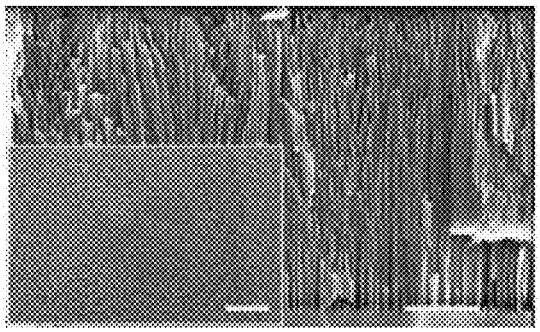


FIG. 8C

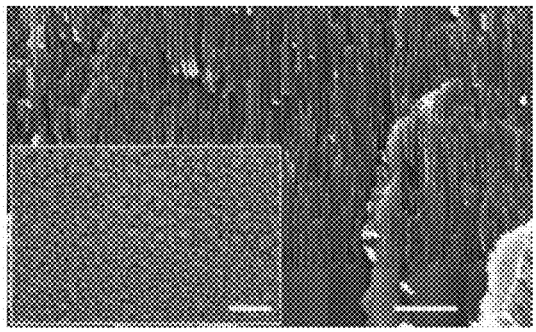


FIG. 8D

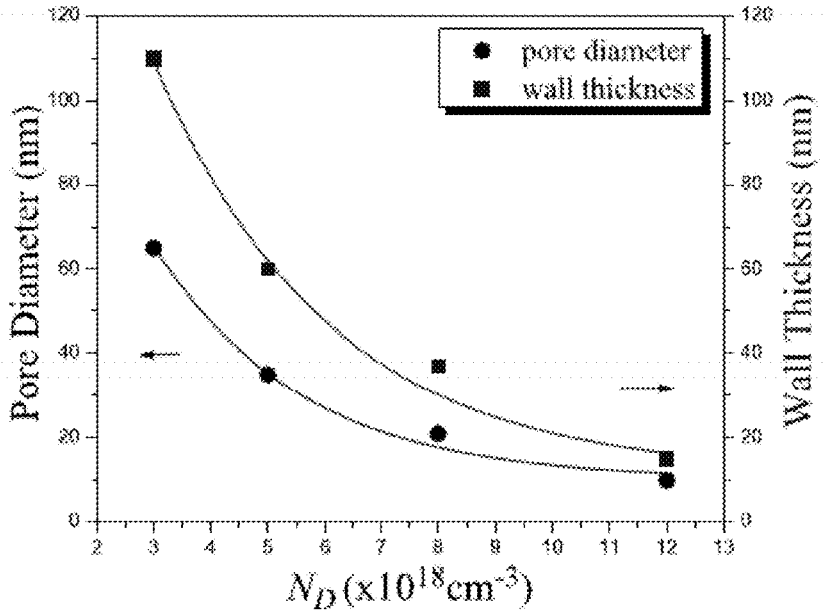


FIG. 9

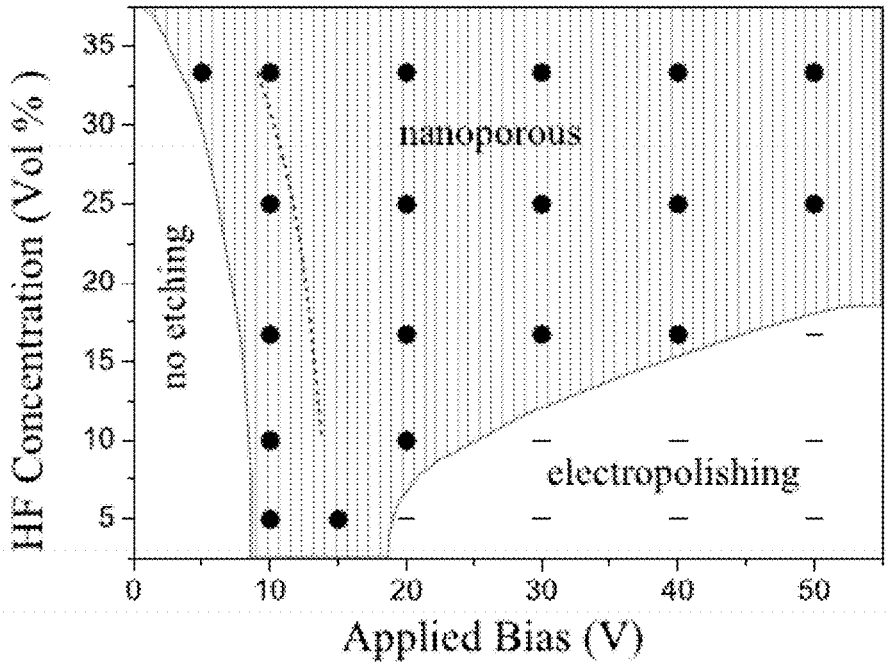

HF Concentration (Vol %)
Applied Bias (V)
nanoporous
no etching
electropolishing
0
10
20
30
40
50
5
10
15
20
25
30
35

FIG. 10

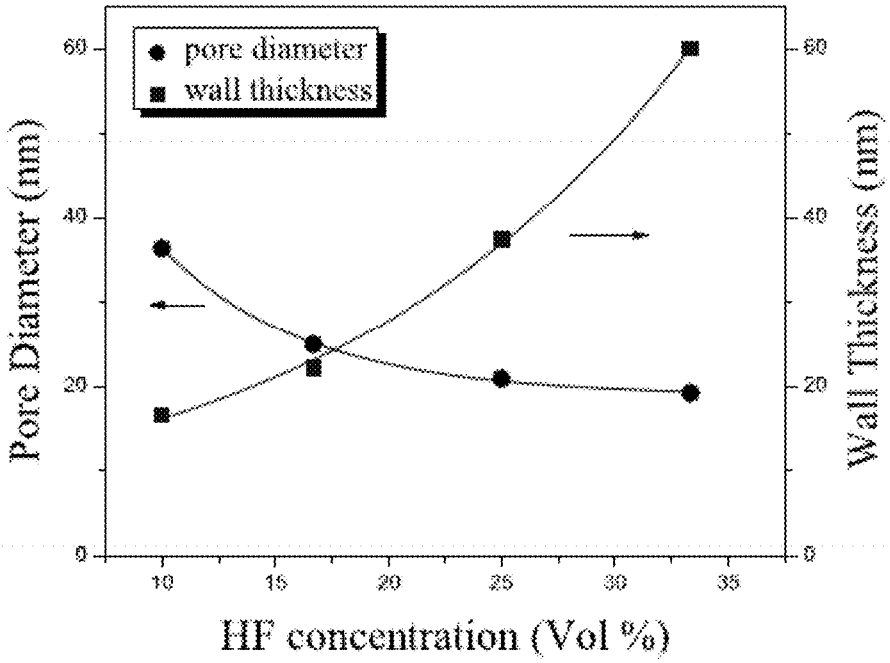

pore diameter
wall thickness
Pore Diameter (nm)
Wall Thickness (nm)
HF concentration (Vol %)
0
20
40
60
10
15
20
25
30
35

FIG. 11

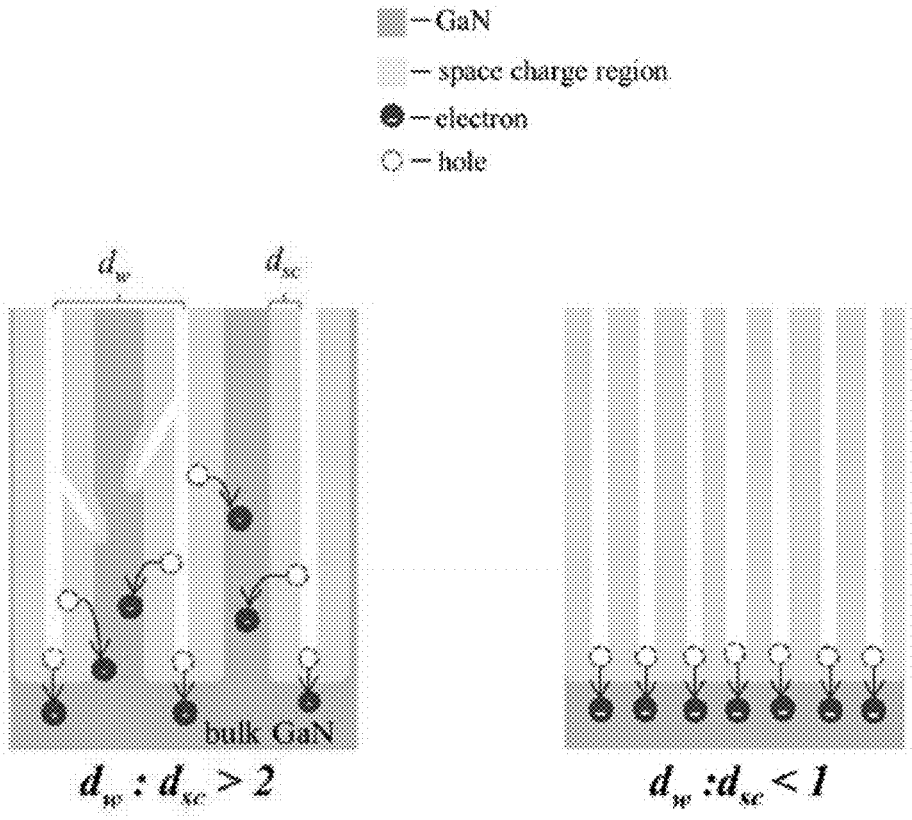


FIG. 12A

FIG. 12B

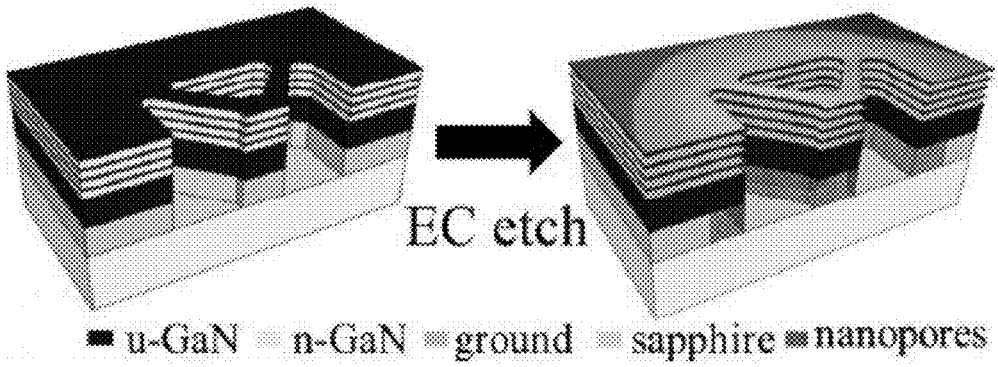


FIG. 13A

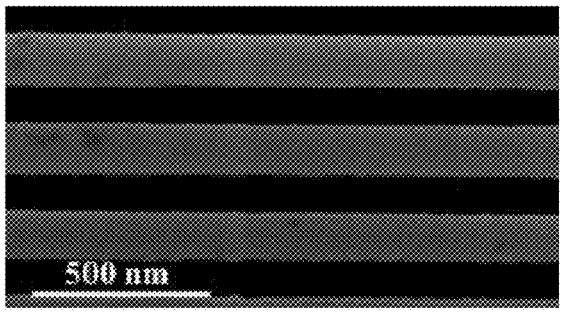


FIG. 13B

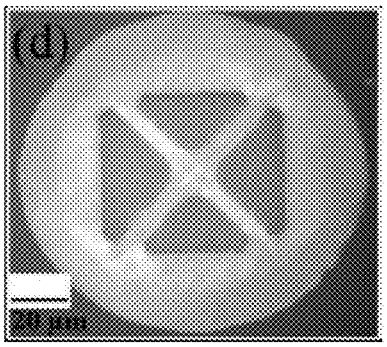


FIG. 13D

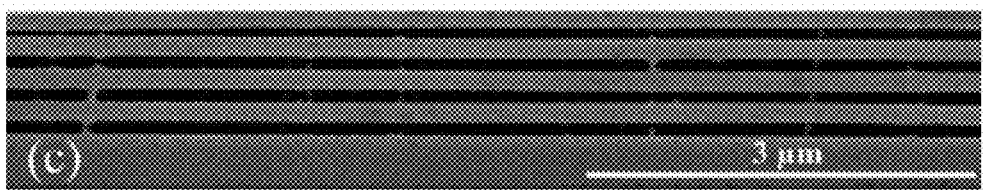


FIG. 13C

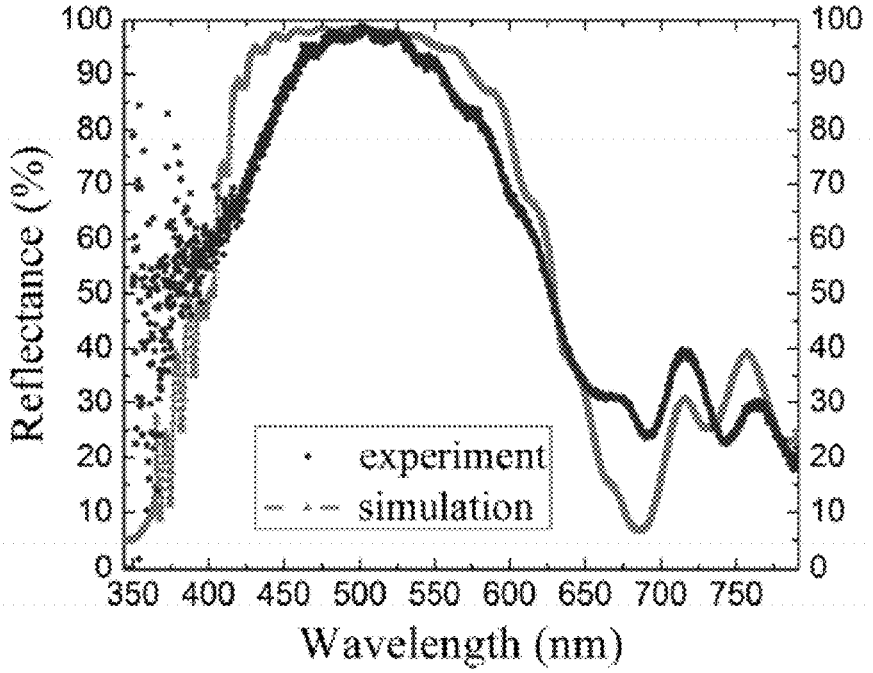

Reflectance (%)
Wavelength (nm)
experiment
simulation
100
90
80
70
60
50
40
30
20
10
0
350 400 450 500 550 600 650 700 750

FIG. 14

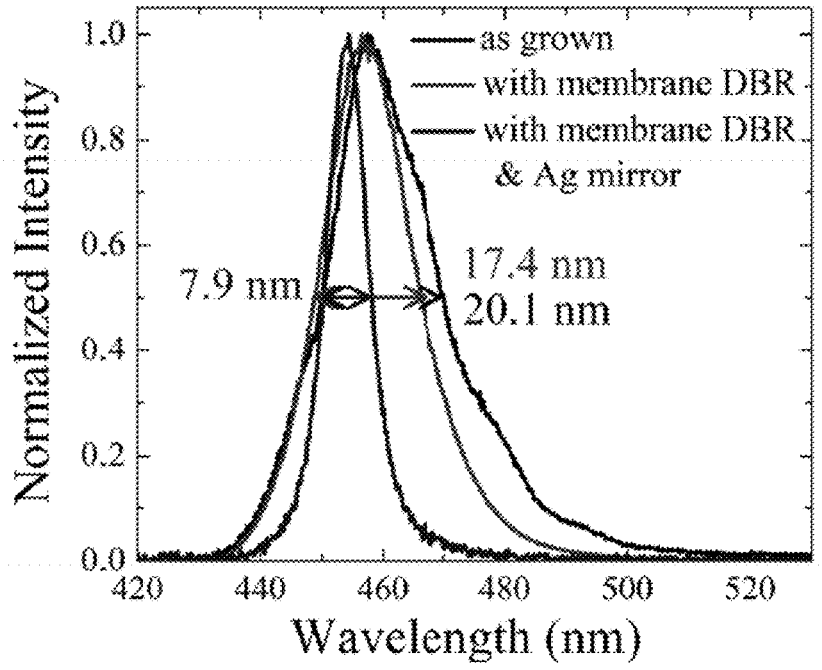

Normalized Intensity
Wavelength (nm)
as grown
with membrane DBR
with membrane DBR
& Ag mirror
7.9 nm
17.4 nm
20.1 nm
1.0
0.8
0.6
0.4
0.2
0.0
420 440 460 480 500 520

FIG. 15

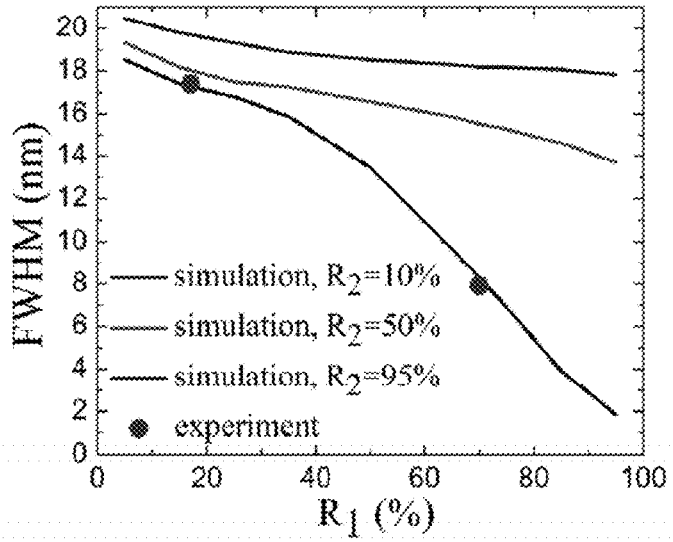


FIG. 16

FIG. 17A

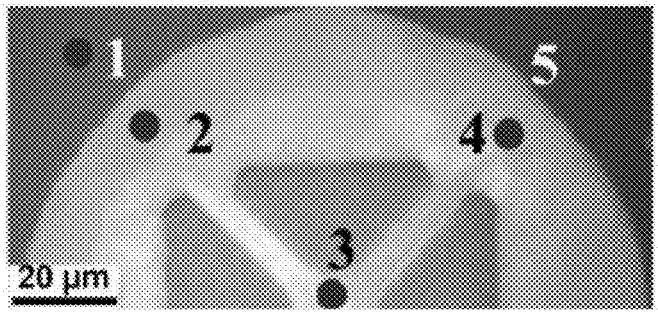
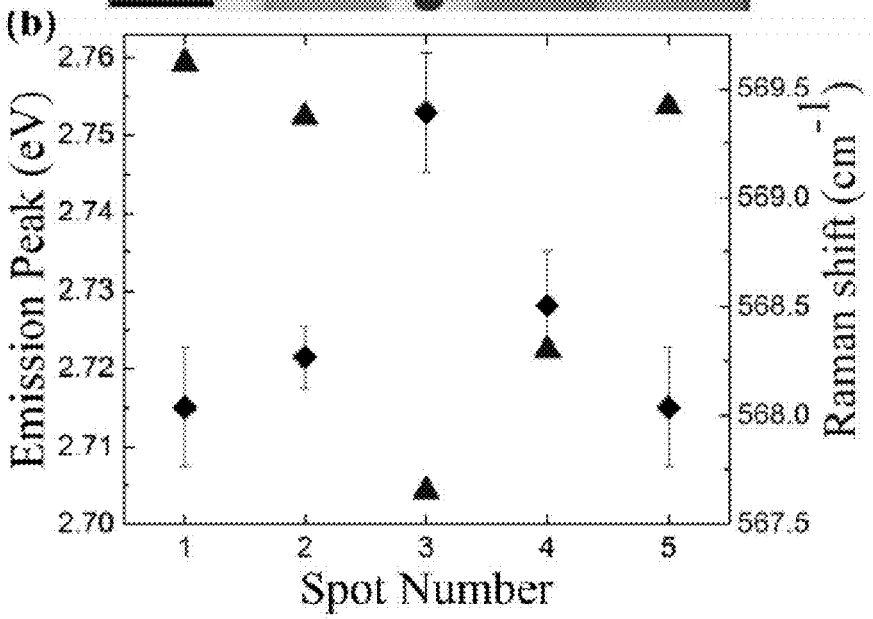


FIG. 17B



LATERAL ELECTROCHEMICAL ETCHING OF III-NITRIDE MATERIALS FOR MICROFABRICATION

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. provisional application Ser. No. 61/665,617 titled "III-Nitride Vertical Cavity Surface Emitting Lasers (VCSEL) with GaN/air DBR by Electrochemical Etching," filed on Jun. 28, 2012, which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Technical Field

[0003] The technology relates to methods and structures for performing etching of sacrificial layers of III-nitride material. The etching techniques may be used for micro- and nano-fabrication of integrated devices, such as vertical cavity surface emitting lasers (VCSELs) based on III-nitride semiconductor material. The VCSELs may include air/semiconductor, distributed Bragg reflector (DBR) structures formed adjacent to the VCSEL using lateral, electrochemical etching techniques.

[0004] Discussion of the Related Art

[0005] The etching of semiconductor materials is an important technique that is used in microfabrication processes. Various kinds of etching recipes have been developed for many materials used in semiconductor manufacturing. For example, Si and certain oxides may be routinely etched using dry (e.g., reactive-ion etching) or wet chemical etching techniques that yield desired etch rates and etch morphologies. III-nitride materials have recently emerged as attractive materials for semiconductor manufacturing, however these materials can be chemically inert to standard wet etchants.

[0006] Some attractive applications for III-nitride materials include micro-photonic devices, such as LEDs and lasers. Some existing methods of making III-nitride VCSELs involve forming structures that comprise alternating layers of AlGaN/GaN or AlInN/GaN. However, these structures are difficult to produce and do not exhibit high refractive index contrast between the alternating layers. Accordingly, to obtain a suitable reflectivity for a laser cavity, the number of layers must be increased (e.g., to about 40) making the overall cavity thick. Additionally, it is difficult to match the cavity mode with an active layer emission wavelength. Another approach to making a VCSEL with a DBR structure is to form dielectric DBRs at two ends of the cavity using layer lift-off techniques. However, this approach is complex to implement and suffers from low yield during manufacture.

[0007] As InGaN light emitting diodes (LEDs) gradually approach technological maturity in performance for blue/green emissions, microcavity based LEDs (resonant-cavity LED, RCLED) and laser diodes (vertical-cavity surfaceemitting laser, VCSEL) become appealing alternatives that may offer advantages in enhancing radiative recombination rates, improving beam directionality, and possibly reducing the cost in manufacturing due to their planar configuration.

[0008] The encasing of the optical active region into a cavity of a few wavelengths may be done using distributed Bragg reflectors (DBRs) with minimum absorption and high reflectivity. For nitride-based emitters, top p-side DBRs may be prepared by depositing dielectric, quarter-wavelength stacks as a last step of device fabrication. The bottom (n-side) DBRs may be implemented using either dielectric stacks or epitaxially grown (Ga,Al,In)N/GaN periodic heterostructures. However, challenges still exist in both approaches toward ultimate manufacturability. The dielectric approach can require complicated thin-film lift-off and wafer bonding in order to expose the n-type GaN. For epitaxial DBRs, 20 to 40 pairs of heterostructures are needed for good peak reflectance (above 95%) due to the small contrast of refractive indices. Such a thick DBR structure causes a narrow stopband (<50 nm), creates issues in stress management on the device, and reduces the benefit of the Purcell effect.

[0009] Semiconductor/air structures have been pursued using a photo-assisted electrochemical (PEC) etch where minority-holes are photo-generated and confined in narrower-bandgap sacrificial layers to facilitate selective etching. Also, selective chemical etching has been identified for the AlInN/GaN system. The membrane structures prepared by the two techniques generally suffer from etched surface roughness that contributes to scattering losses in the optical devices. The maximum reflectance in the blue/green range from GaN/air DBRs, prepared by either PEC or selective wet etching, has not exceeded 75%.

SUMMARY

[0010] The described technology relates to methods and structures for lateral electrochemical etching of III-nitride materials to produce optically smooth surfaces, and for controllably forming porous III-nitride material. The etching processes are compatible with InGaN based light emitters and integrated devices. The etching techniques may be used for manufacturing various microstructures and microdevices. For example, the etching techniques may be used for making vertical cavity surface emitting lasers (VCSELs) that include distributed Bragg reflector (DBR) structures. According to some embodiments, the VCSELs and DBR structures comprise III-nitride semiconductor materials that may be deposited in multiple layers on a substrate, and the formed DBR structure comprises a limited number of alternating III-nitride/air layers. In various embodiments, the electrochemical etching of a DBR structure laterally removes alternating layers in a multilayer structure, and leaves optically smooth air/semiconductor interfaces. The electrochemical etching may be highly selective to the conductivity of the materials. The conductivity (and resulting etching properties) may be controlled by doping the materials during their deposition. By modulating the doping of epitaxial layers, highly-doped n-type layers may be laterally etched over large distances (>10 microns) in confined regions (<500 nm layer thickness sandwiched between non-etched layers) at high etch rates (>5 microns/min). The etching techniques may be used to fabricate other III-nitride devices, e.g., LEDs, high electron mobility transistors, high-power tranistors, and MEMs devices

[0011] The electrochemical etching may be controlled to form optically smooth surfaces or nanoporous structures wherein the pores may have selected properties. The etching may be controlled to produce a desired etching morphology by controlling etching parameters that include one or more

of: etchant solution, electrical bias between the sample to be etched and the etchant solution, and dopant concentration of the material to be etched.

[0012] According to some embodiments, a method for laterally etching III-nitride material comprises depositing a first layer of III-nitride material having a first conductivity on a substrate, and depositing a second layer of material over the first layer. The method may further include forming a via in the second layer to expose a surface area of the first layer, and electrochemically and laterally etching at least a portion of the first layer using a hydrofluoric-based etchant. The portion of the first layer etched may undercut the second layer.

[0013] In some embodiments, a method for etching III-nitride material may comprise depositing a first layer of III-nitride material having a first conductivity on a substrate, and depositing a second layer of material adjacent the first layer. The method may further include electrochemically etching at least a portion of the first layer using a hydrofluoric-based etchant. The etched portion of the first layer may be a component of an LED device.

[0014] In some embodiments, a method for forming a distributed Bragg reflector (DBR) laser comprising III-nitride material comprises depositing a first multi-layer structure on a substrate, wherein the first multi-layer structure comprises first and second layers. The first layers may have a conductivity different than that of the second layers. The method may further include depositing a multiple quantum well (MQW) active structure adjacent the first multi-layer structure, and forming vias into the first multi-layer structure so as to provide access for an etchant to the second layers. The method for forming a distributed Bragg reflector (DBR) laser may further comprise laterally and electrochemically etching the second layers, so as to remove at least a portion of the second layers and form a DBR structure adjacent the MQW region. The DBR structure may comprise at least two first layers separated by one or more layers of air.

[0015] Structures related to the methods are also contemplated. In some implementations, a III-nitride DBR device manufactured according to the disclosed techniques may comprise a multi-layer structure having first and second layers formed of III-nitride material, wherein a conductivity of the first layers is different from a conductivity of the second layers. The device may further comprise a MQW structure formed adjacent the multi-layer structure, wherein the MQW structure comprises an active region of the device, and vias formed into the multi-layer structure proximal to the MQW structure. The DBR device may further include regions adjacent the vias in which portions of the second layers have been completely removed to form at least two first layers separated by one or more layers of air.

[0016] The foregoing and other aspects, embodiments, and features of the present teachings can be more fully understood from the following description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The skilled artisan will understand that the figures, described herein, are for illustration purposes only. It is to be understood that in some instances various aspects of the embodiments may be shown exaggerated or enlarged to facilitate an understanding of the embodiments. In the drawings, like reference characters generally refer to like features, functionally similar and/or structurally similar elements throughout the various figures. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the teachings. Where the drawings relate to microfabrication of integrated devices, only one device may be shown of a large plurality of devices that may be fabricated in parallel. The drawings are not intended to limit the scope of the present teachings in any way.

[0018] FIG. **1** depicts a III-nitride DBR laser with a MQW active region, according to some embodiments;

[0019] FIGS. **2**A-**2**H depict methods for fabricating structures that include laterally-etched III-nitride materials, according to some embodiments;

[0020] FIG. **3**A-**3**B are SEM micrographs of nanoporous GaN formed by electrochemical etching in HF-based etchant, according to some embodiments;

[0021] FIG. **4** depicts anodic current-voltage relationship for n-GaN etching in HF; according to some embodiments;

[0022] FIGS. **5**A-**5**B are SEM micrographs showing a change in pore density as a function of etching time;

[0023] FIGS. **6**A-**6**B are SEM micrographs showing synchronized pore diameter oscillation;

[0024] FIG. **7** depicts results of etching phases for varying dopant densities as a function of applied etching bias; according to some embodiments;

[0025] FIGS. **8**A-**8**D are SEM micrographs illustrating different pore morphologies as a function of dopant density;

[0026] FIG. **9** plots pore diameter and wall thickness as a function of dopant density, according to some embodiments;

[0027] FIG. **10** depicts results of etching phases for varying HF concentration as a function of applied etching bias; according to some embodiments;

[0028] FIG. **11** plots pore diameter and wall thickness as a function of HF concentration, according to some embodiments;

[0029] FIGS. **12**A-**12**B are representations of possible pore morphologies based on the ratio of space charge region thickness and pore separation;

[0030] FIG. **13**A depicts an embodiment of an air/semiconductor DBR structure, according to some embodiments;

[0031] FIGS. **13**B-**13**C show SEM micrographs of air/GaN layers of a DBR structure fabricated using electrochemical etching, according to some embodiments;

[0032] FIG. **13**D shows a DIC image of a DBR structure after electrochemical etching, where the formation of air gaps between layers results in a circular pattern;

[0033] FIG. **14** shows measured and simulated reflectance spectra for a DBR structure; according to some embodiments;

[0034] FIG. **15** shows emission spectra of MQWs samples (1) without DBRs, (2) with bottom DBRs, and (3) with bottom DBRs and silver capping layer, where significant linewidth narrowing can be seen for samples with DBRs;

[0035] FIG. **16** illustrates FWHM linewidths from experiment and from simulated spectra of emitters in a cavity, where agreement between experiments and simulation of high reflectance bottom DBRs indicates membrane DBRs can be used to improve spectral purity via optical cavity modes;

[0036] FIG. **17**A shows a DIC image of the measurement spots on an EC etched sample with MQWs; and

[0037] FIG. **17**B illustrates the corresponding emission peak and Raman shift at the measured spot locations.

[0038] The features and advantages of the embodiments will become more apparent from the detailed description set forth below when taken in conjunction with the drawings.

DETAILED DESCRIPTION

[0039] Because III-nitride materials can be chemically inert to wet etchants, microfabrication of integrated optical or integrated electronic devices based on these materials poses manufacturing challenges. Although some etching techniques (e.g., dry reactive-ion etching or photochemical etching) have been developed to etch these materials, these processes can be costly and/or difficult to implement. Described herein are methods that may be used to readily etch III-nitride materials at high etch rates (e.g., at rates up to 10 microns/minute) and with uniform and controllable surface properties and etch morphologies.

[0040] The etching processes are based on electrochemical etching of III-nitride materials that have been selectively doped to tune the etching properties of the materials. The merits of conductivity-based wet etching include, but are not limited to (1) high scalability to large areas—the etching does not require UV illumination and therefore does not suffer from problems related to uniformity of illumination, (2) improved manufacturability—the electrochemical etch rate can be several orders of magnitude faster than chemical wet etch, (3) controllable etching morphology—the etching morphology may be controlled by controlling the doping profile(s) in the material(s) to be etched. For example, modulation of dopant can define complex structures in a single material.

[0041] The etching techniques may be used for various microfabrication applications, e.g., the manufacture of microstructures that include III-nitride materials. Examples of microstructures include microcavity lasers, DBR lasers, microcavity LEDs, resonant cavity LEDs, enhanced emission LEDs, transistors, and MEMs devices. In some embodiments, the electrochemical etching may be used in the preparation of highly reflective distributed Bragg reflectors (DBRs) from III-nitride materials. These DBR structures may provide a useful building block for integrated photonics, such as the manufacture of DBR lasers, microcavity structures, and enhanced emission structures. Other devices fabricated from III-nitrides may comprise detectors and emitters in the blue/green region of the optical spectrum, as well as transistors that may be used in high power and/or high electron mobility devices. For integrated optical applications, an integrated DBR structure may be used to provide tailored reflectance or transmission bands for integrated photonic structures.

[0042] Research on porous semiconductors has drawn much attention, since the discovery of intense luminescence from porous silicon. The creation of nanopores through electrochemical (EC) anodization transforms conventional semiconductors into three-dimensional meshed networks or foams that are inherently single crystalline. Applications of porous III-V semiconductors in microelectronics, optics, sensing, and light harvesting have been demonstrated. Extension of the porosification study to wide-bandgap GaN is especially appealing due to its demonstrated importance in light emitting diodes and high power electronics. GaN is chemically inert with no available wet etching process at room temperature. Accordingly, an electrochemical etching process for III-nitride materials will have attractive technological implications.

[0043] GaN epilayers are typically prepared with a high density of dislocations. Porous GaN can conceivably influence and block the propagation of dislocations. Additionally, it has been shown that the surface states of GaN tend to have a much slower recombination velocity than those from conventional As- and P-based III-V compounds, making it possible to consider the usage of porous GaN as an active medium.

[0044] By way of explanation, methods for making integrated DBR structures for integrated photonic devices are described below to exemplify how the etching techniques may be used to form advanced integrated optical structures. However, the invention is not limited to the formation of DBR structures for VCSELs only. The etching techniques may be applied to other microfabrication processes involving III-nitride materials. For example, the etching techniques may be used to form LEDs, transistors, cantilevers, or microelectromechanical structures based on III-nitride materials. In some embodiments, the etching techniques may be used to form thin membranes. In some implementations, the etching techniques may be used to release membranes or devices from a substrate.

[0045] FIG. **1** shows one example of an integrated photonic DBR laser **102** that includes a highly reflective DBR structure **110** that may be fabricated using electrochemical etching of sacrificial III-nitride layers. The highly reflective DBR structure **110** may form a wavelength-selective mirror at a first end of a cavity of the DBR laser **102**. The active or gain region of the laser may comprise a multiple quantum well (MQW) structure **140**. The MQW **140** may be sandwiched between a layer of n-type semiconductor material **130**, which may inject electrons into the MQW region, and a p-type semiconductor material **150**, which may inject holes into the MQW region. The holes and electrons may recombine in the MQW region to produce photons. There may be a first contact pad **135** formed on the n-type semiconductor material **130** and a second contact pad **155** formed on the p-type semiconductor material **150**.

[0046] In some embodiments, a second end of the DBR laser cavity may comprise a dielectric DBR structure **160** that functions as a wavelength-selective mirror. In other embodiments, a dielectric DBR structure may not be used, and a reflective or semi-reflective layer of material (e.g., a thin film of metal such as silver, chrome, or gold) may be deposited at the second end of the laser cavity. The reflectivity of the dielectric DBR **160** or deposited material may be less that the reflectivity of the highly reflective DBR **110**, such that the majority of light from the laser emits from the second end of the cavity along the optical axis **170**, as depicted in the drawing.

[0047] In the depicted embodiment, the highly reflective DBR structure **110** comprises an air/semiconductor multilayer stack. The semiconductor may be a III-nitride semiconductor (e.g., GaN, InGaN, InAlGaN). According to various embodiments, the layers of semiconductor **112** are separated by layers of air **114**. According to some embodiments, the layers of air may be continuous and uniform where the sacrificial layers have been removed, e.g., there are no remnants of the sacrificial layer protruding into the air layers. In some embodiments, the regions shown as air layers may comprise highly porous sacrificial material, e.g., the regions may contain a sparse density of filaments remaining from the sacrificial layer. The structure may

further include vias **120**, which may be formed for etching purposes, as described further below.

[0048] FIGS. **2**A-**2**G outline methods that may be used to fabricate a structure like that shown in FIG. **1**. For brevity, not all fabrication steps are shown in the drawings. Steps omitted as not being necessary for understanding the methods will be readily deduced by those skilled in the art of microfabrication. According to some embodiments, a method for fabricating an integrated photonic device (e.g., a DBR laser) with a highly reflective DBR structure may comprise preparing or obtaining a substrate **205** with a multi-layer stack **210** of III-nitride semiconductor material formed on the substrate. The substrate may be any suitable substrate, e.g., a semiconductor, a glass, crystalline material, a ceramic, a polymer. In some embodiments, the substrate **205** may be formed from sapphire.

[0049] The stack **210** may comprise alternating layers of III-nitride material, wherein first layers **211** have a different electrical conductivity than second layers **213**. The III-nitride materials may comprise (Ga,Al,In)N materials where the constituents may be present in any III-nitride combination. In some embodiments, the stack **210** may comprise (Ga,Al,In)N/GaN periodic heterostructures. In some implementations, any one layer may comprise $Al_xIn_yGa_{1-x-y}N$ where x and y may range between 0 and 1 in a manner such that $0 \leq 1-x-y \leq 1$. The layers may be deposited by one or a combination of deposition techniques, e.g., chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), metal organic CVD (MOCVD), hydride vapor phase epitaxy (HVPE), molecular beam epitaxy (MBE) or atomic layer deposition (ALD), according to some embodiments. The first and second layers may alternate in the stack, as depicted, according to some embodiments. In other embodiments, the first and second layers may be arranged in other orders within the stack, or there may be only two layers present. In some embodiments, additional layers may be deposited that may comprise materials other than III-nitrides.

[0050] The thicknesses of the layers **211**, **213** may be selected to satisfy optical design parameters for a DBR structure, according to some embodiments. For example, the thicknesses of the first layers **211** may be approximately one-quarter and/or three-quarter of a selected emission wavelength from the laser. In some embodiments, all first layers may have approximately the same thickness. In other embodiments, at least one of the first layers **215** may have a thickness different than other first layers. The thicknesses of the layers **211**, **213** may be between approximately 50 nm and approximately 500 nm.

[0051] Some of the layers, e.g., second layers **213**, may be designated as sacrificial layers. These sacrificial layers may be removed in whole, or in part, during an etching step. The conductivity, or dopant concentration, of the sacrificial layers may be selected such that these layers will etch at a significantly higher rate than the first layers **211**. In some embodiments, the dopant concentration of the sacrificial layers may be selected such that these layers etch so as to provide a particular morphology.

[0052] During deposition, a dopant may be added to yield a selected conductivity of the layers. For example, the second layers **213** may be doped with an n-type dopant (e.g., Si) at a dopant concentration between approximately 10^{17} to approximately 10^{20} cm^{-3}. The inventors have found that electrochemical etching of n-type III-nitride material in HF-based etchants can occur at high etch rates (e.g., greater than 10 microns/minute) for materials doped in this range. Additionally, the etched surface can exhibit high smoothness that may be beneficial for photonic devices, or the etched material may be made porous, depending on the selected etching conditions. The first layers **211** may be lightly doped as n-type material, in some embodiments, or may be undoped in other embodiments. Modulation of the doping in the multi-layer stack can define the etchant profiles and morphologies.

[0053] According to some embodiments, an additional layer (a ground layer, not shown) may be deposited proximal to the multi-layer stack **210**. The ground layer may comprise a conductive layer formed from doped III-nitride material or other conductive material. The ground layer may provide uniform current spreading for an electrochemical etching process. For example, a potential bias or reference potential may be applied to the ground layer during electrochemical etching, and the ground layer may aid in uniformly spreading the electric field across the region to be etched.

[0054] With reference to FIG. **2**B, active layers **220** for a laser or LED may be formed adjacent the multi-layer stack **210**. In some embodiments, the active layers **220** may form a multiple quantum well (MQW) structure or a superlattice (SL). The active layers may comprise multiple layers of semiconductor materials, e.g., layers of III-nitride materials. Additional layers of other materials, e.g., insulators, metals, polymers, may be included with the active layers in some implementations.

[0055] The active layers **220** may be patterned using lithography and etching techniques, as depicted in FIGS. **2**C-**2**D. A resist may be applied uniformly over the active layers **220**, and subsequently patterned, e.g., via photolithography, to provide a resist mask **225**. The exposed regions of the active layers **220** may be etched away using an anisotropic dry etching process, e.g., reactive ion etching, to form an active MQW region **228** of a device.

[0056] The resist mask **225** may be stripped from the substrate, and another resist mask formed to define vias **230** in the multi-layer stack **210**, as depicted in FIG. **2**E. The vias may be proximal the active region **228**, and may be formed using a dry anisotropic etch process. There may be multiple vias around the active region, as depicted in FIG. **1** for example, and the vias may or may not be circular in cross section. The vias **230** along their sidewalls may expose surface regions of the first and second layers **211**, **213**. The resist may be stripped from the substrate to yield the structure shown in FIG. **2**E.

[0057] After formation of the vias, the substrate and multi-layer stack **210** may be subjected to electrochemical etching in an HF-based etchant. The etching may take place in an etchant bath, wherein a potential bias is applied between the etchant solution and the multi-layer stack. Arrangements for etching may include those described in U.S. patent application Ser. No. 13/559,199 filed Jul. 26, 2012, which is incorporated herein by reference in its entirety. The applied bias may be between approximately 5V and approximately 60V, according to some embodiments. In some embodiments, the applied bias may be controllably varied during the etching steps, for example as described in "Nanopores in GaN by electrochemical anodization in hydrofluoric acid: formation and mechanism," by D. Chen et al., J. App. Phys., 112 (2012) p. 064303, which is incorporated herein by reference in its entirety.

[0058] According to some embodiments, the HF-based etchant may be substantially non-aqueous. The inventors have found that an aqueous solution of HF can contribute to a swelling, deformation, or increased stress of the remaining, unetched layers. In some implementations, an HF/ethanol etchant solution may be used, in which any water content is minimized in the etchant to less than about 10%.

[0059] In some implementations, the HF may be aqueous, e.g., ~50% in water, which is then diluted with ethanol and/or glycerol. In some cases, the volume ratio of ethanol to HF (~50%) may be between approximately 0.5:1 and approximately 9:1. In some embodiments, the water content of the etchant may be reduced by adding ethanol and/or glycerol to between 5% and 15%.

[0060] The inventors have also found that adding glycerol to the HF/ethanol etchant can improve lateral etching rates and smoothness of the etched surfaces. In some embodiments, the etchant comprises ethanol/glycerol added to HF acid. According to some embodiments, the etchant may comprise ~10% HF, ~10% water, ~32% ethanol, and ~48% glycerol, where the percentages refer to volume. In some embodiments, these percentages may be varied by up to ±5% from the values listed. In other embodiments, these percentages may be varied by ±5% or more from the values listed. The etching may be carried out at room temperature, in some embodiments. In some implementations, the etching may be carried out between approximately 10° C. and approximately 40° C. The bias applied during the electrochemical etching may be between approximately 10V and approximately 30V, in some implementations. The dopant concentration may be between approximately 1×10^{19} cm^{-3} and approximately 5×10^{19} cm^{-3}, in some cases. In some embodiments, the dopant concentration may be between approximately 3×10^{18} cm^{-3} and approximately 2×10^{19} cm^{-3}. With these etchant parameters, lateral etch rates of between about 2 microns/min and about 10 microns/minute may be achieved. According to some embodiments, etching rates in this range can be achieved in closed-space configurations (approximately 200 nm layer separation). The etching may yield surface smoothness of approximately 5 nm RMS over an etched area of 25 square microns.

[0061] If porous GaN is desired, other etching parameters may be used. Parameters for forming porous GaN are discussed below in connection with Example 1. Porous GaN may be used for the manufacture of III-nitride LEDs. In some embodiments, a DBR structure may be formed using highly porous GaN intermediate layers in the DBR stack. The highly porous layers may provide significant refractive index contrast and also provide support for uniform spacing of the unetched DBR layers.

[0062] As a result of electrochemical etching and removal of the second layers **213**, a DBR structure **280** as depicted in FIG. **2**F may be formed. The lateral etching may remove portions of the second layers to form continuous layers of air between layers of semiconductor. With the layer thicknesses chosen to be approximately one-quarter of a target emission wavelength, the DBR structure can provide high reflectivity (e.g., >70%) over a wide wavelength band (e.g., ~150 nm) with six or fewer semiconductor layers. According to some embodiments, a peak reflectance of more than 98% may be achieved with as few as four semiconductor layers.

[0063] FIG. **2**G depicts another embodiment of a DBR structure **282** formed adjacent an active MQW region. In this embodiment, the sacrificial layers are not completely removed beneath the MQW structure. A pillar **290** may remain to provide uniform spacing of the first, unetched layers. The pillar may be sub-wavelength in cross-sectional dimension in some embodiments, and may or may not be circular in cross section. In some embodiments, the pillar **290** may have a cross-section that is approximately as wide as the MQW active region. In some embodiments where a pillar **290** is formed, the via **232** may comprise an annular ring surrounding the MQW region. The discs of the first layer material formed by etching may be supported entirely by the pillar structure.

[0064] The inventors have found that stresses in the unetched layers **211** can lead to warping, buckling, or out-of-plane deformations when the sacrificial layers **213** are removed. A structure shown in FIG. **2**G may mitigate out-of-plane deformations. In other embodiments, one or more stress-compensating layers **295** may be deposited proximal the etched regions, as depicted in FIG. **2**H. The stress compensating layer **295** or layers may impart a stress opposite to that of the unetched first layers **211** to the etched region, and thereby compensate for the stresses of the first layers **211**. In some implementations, stress compensating layers may be included as multiple thin layers in the multilayer stack **210**, e.g., each adjacent the a respective first layer.

[0065] A DBR laser cavity may be completed by capping the MQW structure with a dielectric DBR structure (as depicted in FIG. **1**) or a reflective material, e.g., a thin metallic film such as a layer of silver. The dielectric DBR or reflective material may be deposited after the active layers **220**, and may be patterned before or at the same time as the patterning of the MQW region. According to some embodiments, a second mirror for the cavity may be formed using techniques developed for the manufacture of LEDs.

[0066] Electrochemical etching techniques may also be employed during the fabrication of LED devices. For example, an air/semiconductor DBR structure as described above may be formed adjacent a planar III-nitride LED to reflect emission from a substrate to a direction away from the substrate, e.g., towards a viewer. In some implementations, air/semiconductor DBR structures may be formed adjacent an LED to make resonant cavity and/or microcavity LED emitters. The DBR structures may enhance emission from the LEDs. Additionally or alternatively, a portion of the LED device may be made porous using electrochemical etching. Porosification of the LED may enhance photon emission from the devices active region. Selection and control of pore morphology, as described in the following example, may improve LED emissions.

EXAMPLES

Example 1. Controlled Porosification of GaN

[0067] This example describes the use of hydrofluoric acid (HF) as a versatile electrolyte for preparing porous GaN with a wide range of morphology from curved to highly parallel pores. The interplay among different electro-chemical processes may be elucidated using cyclic voltammetry. Under suitable conditions, a record-high rate of porosification (up to 150 μm/min) is observed. The influence of electrolyte concentration, sample conductivity (doping), and anodization potential is investigated. The rich variety of pore morphology can be explained by a depletion-region model where the available current flow pathways in GaN, deter-

mined by the ratio of inter-pore spacing and the width of depletion region, define the directions of pore propagation and branching.

[0068] Electrochemical porosification experiments were conducted in a two-electrode cell at room temperature with n-type GaN as the anode and a platinum wire as the counter electrode (cathode). Ga-polar Si doped GaN of 2 μm thickness was grown on c-plane sapphire by metal-organic chemical vapor deposition (MOCVD) with a doping range of 10^{17}-10^{19} cm^{-3} and defect density range 10^{8}-10^{9} cm^{-2}. Underneath the Si-doped layer, an undoped GaN layer of 500 nm was used as an etch stop. An n-GaN layer (5×10^{18} cm^{-3}) with a thickness of 500 nm was grown prior to the etch stop and contacted with conductive tape to ensure uniform distribution of the anodization bias across the sample (~1×1 cm^2). The electrolytes were prepared by adding ethanol to HF (49%) with a volume ratio from 0.5:1 to 9:1. The anodization process was carried out in a potentiostatic (constant voltage) mode controlled by a Keithley 2400 source meter, while etching current is recorded under room light without UV illumination. After anodization, samples were rinsed with deionized (DI) water and dried in N_2. Scanning electron microscopy (Hitachi SU-70) was used to study the pore morphology. Representative cross-section and plan-view images of GaN are shown in FIGS. **3**A-**3**B. In the cyclic voltammetry experiment, the source meter is programmed to provide a constant sweep rate of 6 V/s. The scale bars for these SEM images is 1 μm. For the sample shown in FIG. **3**A, the bias was 8V. For the sample shown in FIG. **3**B, the bias was 18V.

[0069] The morphology of porous textures and patterns may be determined by the highly inhomogeneous etching process, which consists of successive steps including carrier transport in the space-charge (SC) layer, oxidation at the semiconductor surface, transport of ions in the oxide layer (OL), field-enhanced dissolution of oxide at the oxide-electrolyte interface, and ionic transport within the interfacial double layer (DL). The local electric field within each layer plays a role in regulating or facilitating the aforementioned process. The richness in porous morphology is derived from (1) the curvature-driven electrochemical etching due to the concentration of electric field near surface undulations/defects, with a statistical nature not dissimilar to nucleation, and (2) the competing dynamics in the growth and dissolution of intermediate oxide, resulting in different distributions of electric field in SC, OL, and DL layers, which can alter the rate-limiting steps in the EC etching and the final morphology. To gain insight into the underlying redox process over a wide range of anodization potential, cyclic voltammetry (or voltammogram) was performed.

[0070] FIG. **4** shows a typical cyclic current-voltage (CV) characteristic for n-type GaN in aqueous HF ($N_D=8\times10^{18}$ cm^{-3}, [HF]=25%). In the forward direction, three regions with different CV slopes are distinguished, reflecting differences in the underlying rate-limiting steps. Region I corresponds to low bias, pre-breakdown conditions. Leakage current across the reverse-biased electrolyte/n-GaN junction is responsible for the etching and the formation of surface pits (see FIG. **5**A). Surface pits formed under region I do not propagate into GaN layers to become nanopores due to a lack of a consistent supply of holes from thermalization only. This region is subsequently denoted as "no etching."

[0071] The stochastic nature of such an etching mechanism is manifested by a linear increase of pit density with etching time, as seen in the SEM images of FIGS. **5**A-**5**B. The n-type dopant density for this sample was 1.2×10^{19} cm^{-3}, and the sample was etched in 25% HF for 10 min (FIG. **5**A) and 25 min (FIG. **5**B). The corresponding surface pore densities were found to be 9.5×10^{9} cm^{-2} (FIG. **5**A) and 2.0×10^{10} cm^{-2} (FIG. **5**B).

[0072] In region II, the electric field is sufficient to induce local breakdown in reverse biased GaN, providing holes for the redox reaction and etching. Porous GaN can be formed consistently in this region, and the process is rate-limited by carrier transport (SC). The appearance of multiple current peaks in this region implies the emergence of a multi-step redox reaction involving intermediate oxidation states. At the onset of pore formation, (structural) defect-assisted etching prevails such that the pore density remains unchanged during etching and comparable to the dislocation density. Increasing the anodization bias beyond the first oxidation peak (~10 V), an additional dissolution process emerges that causes the etching front to propagate very rapidly. An etch rate as high as 2.5 μm/s has been obtained under a bias of 20V ($N_D=8\times10^{18}$ cm^{-3}, [HF]=25%). This etch rate is one to two orders of magnitude faster than previously reported results. When the static anodic potential is between the first and second oxidation peaks, synchronized oscillations in pore diameter with a spatial coherence over tens of microns were observed, as shown in FIG. **6**. Such a phenomenon has been observed in other III-V system and has been explained by a "current burst" model. According to this model, the self-induced oscillation is attributed to the formation and dissolution of an intermediate OL, causing a dynamic modulation of resistance, current, and consequently the pore diameter.

[0073] In region III, the dissolution of oxide occurs homogeneously across all GaN/electrolyte interfaces, and electropolishing rather than porosification is observed. The decrease of current with an increasing bias is due to the depletion of ions near the interface and the corresponding increase in the thickness of the diffusive layer (also known as Guoy layer). The redox process in region III may then be limited by ion diffusion (DL). The asymmetry in the up-sweep and down-sweep traces (i.e., the absence of reduction peaks) suggests that the reverse electron transfer rate is negligible, unlike the conventional cases with metallic anodes, and indicates the porosification process of GaN is irreversible.

[0074] A wide variety of pore morphologies can be created in GaN by electrochemical etching with HF. The effects of doping level and electrolyte concentration are discussed below. N-GaN with four different doping levels (3×10^{18} cm^{-3}, 5×10^{18} cm^{-3}, 8×10^{18} cm^{-3}, and 1.2×10^{19} cm^{-3}) were anodized in 25% HF with an applied bias ranging from 5V to 50 V. FIG. **7** summarizes the phase diagram of the observed morphology, consisting of mainly no etching, nanoporous etching, and electro-polishing regions. (These three regions are delineated by solid lines as a visual guide.)

[0075] Within the nanoporous region, the doping level has a profound effect on the pore morphology, as shown in FIGS. **8**A-**8**D. These SEM images show cross-sectional and plan-view (inset) images of samples having different doping levels. The doping levels were: sample A, $N_D=3\times10^{18}$ cm^{-3}, sample B $N_D=5\times10^{18}$ cm^{-3}, sample C $N_D=8\times10^{18}$ cm^{-3}, and sample D $N_D=1.2\times10^{19}$ cm^{-3}. All samples were etched in 25% HF at 20 V.

[0076] Under same etching conditions, an increase in doping, corresponding to an upward move in FIG. **7**, results in (i) an increase in pore density, (ii) a decrease in pore diameter, and (iii) the pores being from horizontal/tree-branch-like to highly vertically aligned. The trends of (i) and (ii) are summarized quantitatively in FIG. **9**. The dopant used for the results of FIG. **7** and FIG. **9** was silicon. The samples were etched in 25% HF.

[0077] Keeping the doping level constant, we have investigated the effects of electrolyte concentration using HF:ethanol mixtures. Again, three regions are mapped out in FIG. **10** in a manner similar to the doping-bias study in FIG. **7**. Additionally, a dashed line is used to delineate the observed first oxidation peak extracted from voltammetry. Two notable trends were observed as the HF concentration increases: (1) a decrease in the breakdown potential and the first oxidation potential, and (2) the delayed onset for electropolishing to occur or the widening of the window for porous etching. As the HF concentration increases (to no more than 35%), the ion concentration in Helmholtz and diffusive layers increases, the effective capacitance increases, and the voltage drop in the electrolyte decreases, giving rise to an apparent reduction in the breakdown potential (the boundary between no-etching and porous regions in FIG. **10**) and the first oxidation peak. Under a higher anodization bias, on the other hand, a higher HF concentration increases the oxide dissolution rate, making it less likely for oxide-induced, homogeneous electropolishing to take place, effectively broadening the window of the porous region.

[0078] The graph shown in FIG. **11** plots the geometric parameters (pore diameter and wall thickness) at various HF concentrations, which shows that high HF concentration produces smaller pores with thicker sidewalls. A high HF concentration can be used to fine tune the structure of the pores, while a low HF concentration is more effective in electropolishing GaN surfaces. Electropolishing of GaN to produce optically smooth surfaces may be between HF concentrations of about 5% and 15%, in some embodiments. For the data of FIG. **11**, the n-GaN was doped at N_D~8×10^{18} cm^{-3} and etched at 20 V.

[0079] Several models have been developed for the variations in pore morphology in Si and other III-V semiconductor materials. The depletion layer model treats porous media as a reverse-biased Schottky diode and explains the morphology by the curvature-induced concentration of the electric field. Lehmann and Gosele proposed a quantum wire model to explain the difficulties in hole transport for micropores (diameters from below 2 nm to 20 nm). The rates of carrier transport in Si and mass transport in the electrolyte are thought to be responsible for the observed fractal morphology of macropores in the diffusion limited model. Additionally, as has been briefly described in FIG. **6**, the oscillation in pore diameters has been attributed to current burst.

[0080] Based on the above findings, ion diffusion does not appear to be a rate limiting step once the HF electrolyte exceeds a certain concentration. The porous morphology in the majority of region II depends on the availability of minority carriers (holes) created by impact ionization. The trajectory of the pore can be considered as a mapping of the electric field/carrier flow contours. The possible current flowing pathway is determined by the inter-pore spacing d_w, and the thickness of space charge region d_{sc}. The measured d_w and calculated d_{sc} are listed in Table I for the four samples of different doping levels. Correlating Table I with the observed morphologies (FIGS. **8**A-**8**D), a consistent model emerges where the pore morphology is determined by the presence and pinch-off of the conduction paths in-between pores, quantifiable in terms of a ratio d_w/d_{sc}.

TABLE I

Comparison of space charge region thickness and pore separation in samples A-D, etched in 25% HF at 20 V.

Sample[a]	N_D ($\times10^{18}$ cm^{-3})	d_w (nm)[b]	d_{sc} (nm)[c]	d_w:d_{sc}
A	3	175	81.5	2.15
B	5	95	63.1	1.51
C	8	58	50.1	1.16
D	12	25	40.7	0.61

[a]Corresponds to samples in FIG. 5 and FIG. 6.

[b]d_w is deduced from the diameter and wall thickness of pores.

[c]$d_{sc}=\sqrt{2\epsilon\epsilon_o U_{sc}/(qN_D)}$, where ϵ is the dielectric constant, ϵ_o is the permittivity of GaN, U_{sc} is the drop across the depletion region (deduced from reference electrode), q is the charge of an electron, and N_D is the donor density.

[0081] The modeling of conduction paths in the three-dimensional porous structure is a complicated case. Here, a simplified planar model is illustrated in FIGS. **12**A-**12**B to give the trend. When $d_w>2d_{sc}$ (FIG. **12**A), there are sufficient current pathways between pores; reverse breakdown takes place in between pores and at the tips, causing horizontal widening, branching of the pores in addition to vertical downward propagation as observed in FIG. **8**A. Conversely, when $d_w<d_{sc}$, as sketched in FIG. **12**B, the space between pores is completely depleted due to coalescence of the space charge layers surrounding two adjacent pores. Carriers can only be supplied from underneath the pore tip, forcing the pores to propagate vertically as observed in FIG. **8**D. Samples B and C represent anodization under an intermediate condition with a mixed character of vertical and inclined pores (FIGS. **8**B and **8**C). It is worth noting that the critical d_w/d_{sc} ratio presented in this planar model is subject to modification when largely curved interface is involved, in which case this model should serve only as a qualitative guide. Except in the cases of low concentrations of electrolyte and semiconductor doping, the observed nanoporous morphology can be interpreted and rationally controlled by the depletion model $d_{sc}=\sqrt{2\epsilon\epsilon_o U_{sc}/(qN_D)}$ where more sophisticated porosity profiles can be engineered through real-time modulation of anodization bias (U_{sc}) and/or the employment of doping control (N_D).

[0082] This example demonstrates the use of HF as a versatile and effective electrolyte in etching or porosifying n-type GaN. Rate limiting steps for this electrochemical process were investigated and identified by cyclic voltammetry. A record-high rate of porosification (>100 μm/min) was observed. A detailed mapping of the etching and porosity phase-diagrams was conducted that includes parameters such as doping level, electrolyte concentration, and anodization bias. The morphology of the nanoporous region can be understood quantitatively by a depletion-layer model. These findings can enable the rational control of porous morphology towards the fabrication of GaN structures having the desired optical, mechanical, and/or electrical properties.

Example 2. Fabrication of a MQW/Air-Semiconductor DBR Structure

[0083] This example describes in further detail the fabrication of a membrane-based GaN/air-gap DBR for blue/

green light emitting devices. The formation of membrane DBRs and microcavities may employ electrochemical etching described above in which selective lateral etching of layers is achieved by adjusting the conductivity of layers rather than chemical composition. This can relieve greatly the burden in creating epitaxial DBRs. The lateral-etching process is found to be compatible with InGaN based light emitters.

[0084] The emission of InGaN multiple quantum wells (MQWs) was modified successively with the formation of a DBR underneath the MQW and the capping of the MQW with a silver top mirror. Micro-reflectance measurements of a fabricated DBR structure shows over 98% peak reflectance and a wide stopband (over 150 nm) with only four pairs of GaN/air-gap layers. Micro-photoluminescence spectra of InGaN multiple quantum wells (MQWs) on DBRs show reduced linewidth and improved emission efficiency. After capping the MQWs on DBRs with a silver reflective layer, a significant linewidth narrowing indicates the modification of spontaneous emission due to the presence of a planar microcavity. The reduction of PL linewidth from 20 to 8 nm agrees well with the theoretical prediction of the distribution of cavity modes, indicating that the GaN/air gap DBRs can be a viable building block for III-nitride photonics.

[0085] In this example, the DBR structures were grown on sapphire by metalorganic chemical vapor deposition (MOCVD) using a standard two-step growth process described in F. Bernardini et al., *Phys. Rev. B,* 56 (1997) R10024, which is incorporated herein by reference in its entirety. To facilitate lateral etching, windows were opened by inductively coupled plasma reactive-ion etching (ICP-RIE, Oxford Plasmalab 100) with a Ni mask to form vias in DBR stack and expose sidewalls.

[0086] The sample was then subjected to an electrochemical etch that was carried out in a potentiostatic (constant voltage) mode without UV illumination. The electrolyte was prepared by adding ethanol/glycerol to equal part of hydrofluoric acid (HF, 49%). It was found that replacing ~⅔ of ethanol with glycerol could reduce the roughness of the etched surfaces. The formation and quality of the membrane were examined by scanning electron microscopy (SEM, Hitachi SU-70), atomic force microscopy (AFM, Veeco MultiMode), and differential interference contrast (DIC) microscopy (Nikon Optiphot). As the membrane DBRs were formed laterally with a finite spatial extent, μ-reflectance, μ-photoluminescence (μ-PL, excitation wavelength=405 nm), and μ-Raman (HORIBA Jobin Yvon, confocal LabRAMVR Raman 300) measurements were carried out with a spatial resolution of 4, 2, and 4 μm in diameter, respectively. FIGS. **13**A and **13**B provide conceptual sketches of the formation of a GaN membrane DBR structure using the EC etching. Four pairs of undoped (u-GaN)/n-type GaN (n-GaN, 1.2×10^{19} cm^{-3}) were grown where the n-GaN region becomes the air gap during subsequent EC etching. The thickness of the undoped (GaN membrane) layer was either ¼λ or ¾λ (where λ~500 nm), while the thickness of n-GaN was kept at ¼λ for mechanical stability. The use of a ¾λ membrane layer has the effect of reducing the width of the stopband from 320 nm to 140 nm based on modeling using transfer matrix method. Underneath the DBR layers, an undoped GaN layer of 500 nm was used as a spacer and an etch stop. An n-GaN layer (5×10^{18} cm^{-3}) with a thickness of 500 nm was grown prior to the etch stop (shaded in light grey in FIG. **13**A to ensure uniform distribution of the anodization bias across the sample (~1×1 cm^2). This lower n-GaN layer is referred to as the "ground plane" or "ground layer."

[0087] The optical quality of the finished membrane DBRs is affected by both the pattering dry etching and the EC etch. The roughness of the ICP-etched sidewall was found to be correlated with striations formed on the GaN membrane surface. The chlorine based ICP-RIE process needed to be adjusted to minimize corrugation of the via sidewall surfaces. The parameters of lateral HF EC etching have been explored in D. Chen et al., *J. App. Phys.,* 112 (2012) p. 064303. In general, a lower anodization voltage (<20 V) results in smoother surface and a reduced etching rate. We also note that the quality of EC etching in such a close-spaced configuration (0.2 μm) depends on the effective transport of electrolyte to the etching surface. The partial substitution of ethanol with glycerol was found useful in further improving the membrane smoothness. FIGS. **13**B-**13**C show cross-sectional SEM images, and a plan-view DIC picture (FIG. **13**D) with a pattern that correlates with the schematic of FIG. **13**A. The sharp transition between GaN membrane and air is clearly shown in FIGS. **13**B-**13**C demonstrates that good quality DBR can be maintained over a long distance. The surface roughness can be maintained under 5 nm (root mean square, RMS value) over an area of 5×5 μm^2 at a bias of approximately 12 V. The lateral etch rate at this bias was estimated to be 5 μm/min. The DBR regions were formed around the windows over a length of 10 to 30 μm. Substantial color contrast can be seen in FIG. **13**D. The outer, lighter circle defines the range where DBR structure was formed laterally. The inner (and somewhat non-uniform) circle is a result of unintentional porosification of the ground-plane at roughly half the rate.

[0088] The result from μ-reflectance measurement is shown in FIG. **14** (darker trace). Absolute reflectance value was obtained from calibration with a standard silver mirror (Thorlabs PF03-03-P0123) over 340-800 nm and the accuracy is further checked with a sapphire wafer. With four pairs of GaN/airgap layers, the peak reflectance exceeds 98% at λ=503 nm, and the width of the stopband is around 150 nm, which is three to five times wider than reported epitaxial DBR mirrors. The measured reflectance spectrum is also compared to a theoretical model (FIG. **14**, lighter trace) that is calculated using the transfer matrix method, taking into account the effect of oblique incident/collection angle (half angular range ~10°). Absorption of GaN is included through a wavelength-dependent, complex index of refraction. A scattering loss from surface roughness of 4 nm RMS is assumed. The discrepancy between the measured reflectance spectrum and the simulation is likely due to the fluctuation of the of air-gap thickness in the membrane-based DBRs.

[0089] Toward the fabrication of InGaN microcavity devices, an active region was prepared consisting of 30 pairs of $In_{0.06}Ga_{0.94}N$ (2 nm)/GaN (2 nm) superlattices (SLs) and 10 periods of $In_{0.17}Ga_{0.83}N$ (3 nm)/GaN (8 nm) MQWs, on top of four periods of undoped/n-type GaN designed to form ¾λ DBR for 460 nm emission. The sample was similarly patterned by ICP etching and EC etched to form the membranes of the DBR structure. The MQWs remained intact after the EC etching. The μ-PL spectra (spot diameter 2 μm) of as-grown (black, broad trace) and with/without membrane DBRs are shown in FIG. **15**. A significant linewidth narrowing effect of the MQWs with DBR can be seen. The

spectra of as grown sample (black) and after EC etching (middle, gray trace) are shown in FIG. **15**. Emission from the as-grown MQW exhibits typical fringes due to the interference effect of reflections at GaN/sapphire and GaN/air interfaces. The full-width-half-maximum (FWHM) of the spontaneous emission is around 20 nm and in good agreement with the reported data. After the EC etch, the μ-PL spectrum (middle, gray trace) shows a reduced linewdth (17 nm), a five to ten times increase in intensity, and the disappearance of interference fringes as the effective cavity width was reduced to 0.38 μm estimated by summing up the thicknesses of InGaN MQWs, InGaN SLs and the penetration depth into the DBR. We note that the linewidth reduction of less than 20% is due to the fact that the upper "mirror" has rather limited reflectivity (18%). To improve the quality of the micro-cavity, 50 nm of silver (with a measured reflectance at 460 nm=70%) was deposited on a piece of EC etched sample using e-beam evaporation. Normalized μ-PL spectrum in FIG. **15** (narrow, gray trace) shows a further reduction in linewidth to less than 8 nm.

[0090] To ascertain the optical quality of the bottom GaN/air membrane DBRs, we modeled the linewidth of the spontaneous emission by fitting the experimental linewidths with two different top mirrors (R1=18% and 70%), using the reflectivity of the bottom mirror (R2) as the fitting parameter. For each combination of R1 and R2, the predicted linewidth is obtained semi-empirically by convoluting the theoretical density of cavity modes with the measured spectrum of as-grown InGaN MQW sample assuming thick-cavity effect is negligible. The calculated linewidths versus R1 (top mirror) for three separate values of R2 (10%, 50%, and 95%) are shown in FIG. **16**, together with the experimental data. Qualitatively, a low-reflectivity top mirror (left part of FIG. **16**) will diminish the cavity effect, and the quality of the bottom mirror (R2) is best revealed with a highly reflective top mirror (R1, lower right part of FIG. **16**). Preparation of a dielectric top mirror is currently in progress. The good agreement between the experimental and simulated FWHM with highly reflective bottom DBR indicates that the high reflectance membrane DBR can be used to control the modes of spontaneous emission.

[0091] To ascertain the effect of underlying DBR formation on the optical emission, μ-PL measurement was performed on a sample prior to the silver coating, from a region unaffected by the EC etching (spot **1** in FIG. **17**A), to an area where the membrane DBRs are formed underneath (spot **2**), then to the center of the etched pattern that can be considered freely suspended (spot **3**). The measurement continued along a separate branch (spots **4** and **5**) for a consistency check. FIG. **17**B plots the peak energy of μ-PL determined at each point. A systematic blue shift amounting to 35-40 meV was observed. Since the distances among all spots measured were within 100 μm, the inhomogeneity in composition or thickness due to growth is tentatively ruled out. The systematic emission peak shift can be a result of the reduced piezoelectric effect as InGaN/GaN MQWs undergo relaxation during the formation of membrane DBR. To determine the change of strain, μ-Raman was carried out on the exact spots and summarized as triangles in FIG. **17**B. A shift of the E_2^H from 569.6 cm^{-1} (as grown) to 567.7 cm^{-1} (after EC etch) corresponds to the relief of a compressive strain of 0.104% as a result of EC lateral etching, in good agreement with the reported data of residual strain for GaN on sapphire. The corresponding change in piezoelectric field can be calculated with known parameters and the total electric field can be calculated. Solving the Schrödinger equation for electrons and heavy holes, the effective band gap of strain relaxed MQWs was found to be about 34 meV larger than the strained ones. The good agreement between experimental and theoretical results suggests that the piezoelectric effect is the dominant factor responsible for the observed emission shift. It is noteworthy that the emission peak of the silver coated sample exhibits a further blue-shift in FIG. **15**. Possible causes contributing to the blue-shift include coupling between the MQW emission and surface plasmons (SPs) and wavelength variation across sample (<2 nm).

[0092] This example demonstrates an embodiment of a method that may be used to produce highly reflective short-wavelength membrane DBRs (e.g., air/semiconductor DBRs) that may be used to fabricate innovative high performance GaN-based optical devices.

[0093] The technology described herein may be embodied as a method, of which at least one example has been provided. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments. Additionally, a method may include more acts than those illustrated, in some embodiments, and fewer acts than those illustrated in other embodiments.

[0094] Having thus described at least one illustrative embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A III-nitride DBR device comprising:

a multi-layer structure having first and second layers formed of III-nitride material, wherein a conductivity of the first layers is different from a conductivity of the second layers;

a MQW structure formed adjacent the multi-layer structure, wherein the MQW structure comprises an active region of the device;

vias formed into the multi-layer structure proximal to the MQW structure; and

regions adjacent the vias in which portions of the second layers have been completely removed to form at least two first layers separated by one or more layers of air.

2. The DBR device of claim **1**, wherein the MQW structure forms an active region of a laser.

3. The DBR device of claim **1**, wherein the first layers and second layers comprise GaN.

4. The DBR device of claim **3**, wherein the second layers comprise high n-type conductivity material.

5. The DBR device of claim **1**, wherein the thicknesses of the first layers are substantially the same.

6. The DBR device of claim **1**, wherein the thicknesses of the first layers correspond to approximately one-quarter of a selected emission wavelength for the laser.

7. The DBR device of claim 1, wherein the removed portions of the second layers and remaining first layers form a structure having periodic contrast of optical refractive index.

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