(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 April 2001 (05.04.2001)

PCT

(10) International Publication Number
WO 01/24466 A1

(51) International Patent Classification[7]: H04L 25/02, H03K 19/0175, 19/018

(21) International Application Number: PCT/US00/26991

(22) International Filing Date:
29 September 2000 (29.09.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/408,592 29 September 1999 (29.09.1999) US

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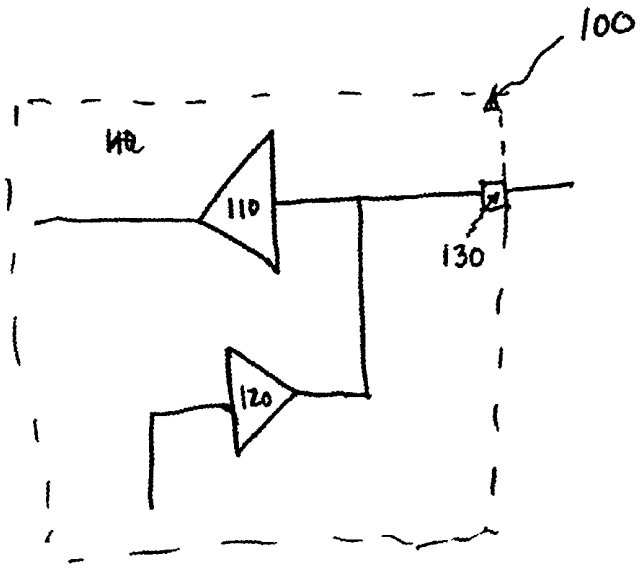
(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: COMMUNICATION INTERFACE WITH TERMINATED TRANSMISSION LINES



(57) Abstract: Structures and methods for providing more reliable communications between circuits within a given system and more flexible apparatus for implementation. In particular, an illustrative embodiment of the present invention includes a driver/receiver circuit that comprises a channel connection, a receiver and a driver. The receiver has a receiver input and a receiver output, and the receiver input is connected to the channel connection. The driver has a driver input and a driver output. The driver output is connected to the receiver input and to the channel connection and the driver provides a transmission line matching impedance to the channel connection when the driver is placed in an active state.

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COMMUNICATION INTERFACE WITH TERMINATED TRANSMISSION LINES

Technical Field of the Invention

The present invention relates generally to the field of integrated circuits and, in particular, to driver and receiver circuits.

Background of the Invention

As electronic circuit design technology continues to improve, the devices of yesterday can now be designed to be smaller, operate at lower power levels and communicate at ever faster speeds. Despite such technological advances, the electronics industry still struggles with problems creating various communication schemes that will allow integrated circuits to reliably communicate with other integrated circuits in an electrical system.

Many electrical systems utilize various application-specific integrated circuit (ASIC) packages and further depend on the reliable signaling between these ASIC packages to properly operate. Thus, the interconnection, design and overall communication schemes are critical to such system's functionality. Some communication schemes implement their interconnection drivers with both a pull-down and a pull-up driver, while others use a single pull-down driver, or an open drain pull-down driver, to drive the interconnection between devices. This open drain configuration, in particular, often presents circuit designers with the challenge of reducing undesirable reflections on the interconnect lines. To reduce the occurrence of transmission line effects such as reflection, it is necessary to control the impedance of the pull-down driver. A method often used to deal with this problem is to add a terminating resistor to the interconnection design. Usually, however, the terminating resistor is placed outside the integrated circuit package, creating a transmission line stub between the terminating resistor and the receiver.

Furthermore, the terminating resistor can cause transmission line integrity problems on high going transitions. This problem occurs because,

when the open drain driver is turned off, the time for the termination resistor to pull the line high can limit the transmission frequency of the channel. Furthermore, the unsymmetric driving capacity of an open drain driver has the undesirable effect of producing a fairly weak high going drive signal at the receiving end of the communication system.

Moreover, as a result of some of the technological advances mentioned above, it is increasingly difficult to create communication schemes that can incorporate both old and new technologies. Two performance parameters that sometimes prevent such incorporations within devices in many communication schemes are the differences in required operating voltage and speed. For example, as CMOS technologies continue to advance, the voltage requirements of devices implemented in CMOS continue to decrease. Of course, reduction in power dissipation is desirable, however, it can be very cost-inefficient to scrap operable, older devices simply because many current communication schemes cannot reconcile the two technologies.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for methods and means that permit more reliable communications between circuits within a given system and more flexible apparatus for implementation.

Summary of the Invention

The above mentioned problems with reflection on transmission lines, impedance matching schemes, backward compatibility, poor signal strength and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A method and means are described which permit more reliable communication between circuits within a given system and offers more flexible apparatus for implementing a communication scheme.

In particular, an illustrative embodiment of the present invention includes a driver/receiver circuit that comprises a channel connection, a receiver and a driver. The receiver has a receiver input and a receiver output, and the receiver

input is connected to the channel connection. The driver has a driver input and a driver output. The driver output is connected to the receiver input and to the channel connection and the driver provides a transmission line matching impedance to the channel connection when the driver is placed in an active state.

Another illustrative embodiment of the present invention provides a novel communications channel. The communication channel comprises a transmission line, a driver connected to the transmission line, wherein the driver drives a signal onto the transmission line, and a driver/receiver circuit connected to the transmission line. The driver/receiver circuit includes a receiver circuit and a driver circuit. An output of the driver circuit is connected to an input of the receiver circuit and to the transmission line and wherein the driver circuit provides a termination line matching impedance to the transmission line when the driver circuit is placed in an active state.

In yet another embodiment, the present invention shows a communications channel, comprising a transmission line, a driver connected to the transmission line and a receiver connected to the transmission line. The driver drives a signal on the transmission line and wherein the driver provides a transmission line matching impedance to the transmission line, and the receiver receives the signal from the transmission line.

Brief Description of the Drawings

Figure 1 is an illustration of a driver/receiver circuit according to the present invention.

Figure 2 is an illustration of a communications channel according to the present invention.

Figure 3 illustrates another communication channel according to the present invention.

Figure 4 illustrates a logic-level schematic of a driver/receiver circuit according to the present invention.

Figure 5 illustrates a schematic of a pre-driver circuit, which in one embodiment of the present invention is contained in the driver circuit.

Figure 6 illustrates a schematic of a output circuit, which together with the pre-driver circuit of circuit 5 comprises the driver component shown in figure 4.

Figure 7 illustrates a schematic representation of the p-fet driver units shown in figure 6.

Figure 8 illustrates a schematic representation of the n-fet driver units shown in figure 6.

Figure 9 illustrates a receiver circuit according to one embodiment of the present invention.

Detailed Description of the Invention

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

Figure 1 is an illustration of a driver/receiver circuit according to the present invention. The driver/receiver circuit 100 includes a receiver circuit 110, a driver circuit 120 and a channel connection 130. This novel driver/receiver circuit 100 receives a signal, driven by an external driving circuit, via the channel connection 130. Since, many communication schemes utilize driving circuits that produce unwanted reflection across communication lines, one function of driver circuit 120 is to "filter" the signal prior to the receiver circuit 110 by eliminating this reflection effect. In order for driver circuit 120 to reduce reflection, its impedance is set to be substantially equal to the impedance of the transmission line that will be connected to driver/receiver circuit 100 at channel connection 130. Therefore, in one embodiment driver circuit 120 acts as a terminating device for receiver circuit 110.

Figure 2 is an illustration of a communications channel according to the present invention. The novel communications channel includes athe receiving device 200, a transmission line 240 and a driving device. The receiving device 200 comprises a driver/receiver circuit according to the present invention and as shown illustrated in Figure 1. The driving device 250 comprises a driver circuit 260 which transmits its signal along transmission line 249 via a channel connection 270. Driver/receiver circuit 200 receives a signal, driven by external driving circuit via the channel connection 230. Since, many communication schemes utilize driving circuits that produce unwanted reflection across communication lines, one function of driver circuit 220 is to "filter" the signal prior to the receiver circuit 210 as discussed above.

In another embodiment, the driver circuit 260 is implemented as a driver circuit according to the present invention or in another embodiment the driver circuit can be implemented in some manner currently known in the art. However, implementing the driver circuit 260 according to the present invention offers the additional benefit of providing strong low-going and high going signals and impedance matching.

Figure 3 illustrates another communication channel according to the present invention. The communication channel comprises a driving device 300, a receiving device 350 and a transmission line 340. The driving device 300 contains a novel driver circuit 320 disclosed in the present invention and a channel connection 330, which allows the driver circuit 320 to communicate to external circuits. The receiving device 350 contains a receiver device 310 which receives signals, driven by the driver circuit 320, via the channel connection 370.

Figure 4 illustrates a logic-level schematic of a driver/receiver circuit according to the present invention. In this embodiment, the driver/ receiver circuit comprises a driver circuit 420 and a receiver circuit 410. In driver circuit 420, inverters 3 and 6 are serially connected such that inverter 3 is driven by a driver enable signal 421 and inverter 6 drives output node 424. Input nodes 422 and 423 drive a driver component 425, which in turn is connected to the channel connection 430. In the receiver circuit, inverters 2 and 5 are serially connected

such that inverter 2 is driving signal output node 411 and inverter 5 is being driven by signal input node 414. Signal input node 416 drives an input of the 2-input AND gate 440 and inverter 4, which is serially connected to inverter 1 and inverter 1 drives output signal node 413. The VREF node 415 drives an input of the 2-input operational amplifier 460. Operational amplifier 460 drives the other input to the 2-input AND gate 440. The channel connection 430 drives the remaining input of the 2-input operational amplifier and a buffer device 450, which in turn also is coupled to both an input to the 2-input AND gate 440 and the signal output node of the operational amplifier 460.

Figure 5 and Figure 6 together illustrate one embodiment of a driver component 425 referred to in Figure 4. Figure 5 illustrates a schematic of a pre-driver circuit 500, which in one embodiment of the present invention is contained in driver circuit 420. Figure 5 shows a pre-driver comprising transistors 1-18 operatively coupled with a first resistive device 19 and a second resistive device 20. The drain of transistors 7 and 8 are coupled to output signal node G1, which is coupled to output circuit 600 shown in Figure 6. The drain of transistors 13 and 14 are coupled to output signal node G2, which is also coupled to output circuit 600 as shown in Figure 6. The drain of transistor 17 drives output signal node ZDI, which is the same node as node 413 in Figure 4.

Figure 6 illustrates a schematic of an output circuit 600 that together with pre-driver circuit 500 of Figure 5 comprise the driver component. Output circuit 600 is driven by a signal on input signal nodes G1 and G2. Node G11 drives several PFET drivers, 603-1 through 603-4. Each PFET driver, 603-1 through 603-4, is coupled to a resistive device, 604-1 through 604-4, respectively. Likewise, node G2 drives several NFET driver, 605-1 through 605-4. Each NFET driver, 605-1 through 605-4, is coupled to PFET drivers, 603-1 through 603-4, and the resistive devices, 604-1 through 604-4, as shown in Fig. 6. The output node of each resistive device, 604-1 through 604-4, is coupled together and also coupled to the anode of a first diode 610 and the cathode of a second diode 620. The output node of the resistive devices also is coupled tosignal node 630 (the channel connection), which is the same node 430 as shown in Figure 4.

Figure 7 shows a schematic representation of the PFET drivers shown in Figure 6. Note that each such unit, 603-1 through 603-4 of Figure 6, is includes several electrically coupled p-type MOSFETs (PMOS), 702-1 through 702-8, to operate as a PFET driver. Each PMOS device 702 is driven by input signal node 701, which corresponds to 601 of Figure 6.

Figure 8 shows a schematic representation of the NFET driverS shown in Figure 6. Note that each such unit, 605-1 through 605-4 of Figure 6, is includes several pairs of electrically coupled n-type MOSFETs (NMOS), 803-1 through 803-5, to operate as an NFET driver. Each NMOS device is driven by input signal 802, which corresponds to 602 of Figure 6.

Figure 9 illustrates a receiver circuit according to one embodiment of the present invention. The receiver circuit shown in Figure 9 provides for three input nodes 916, 915 and 914 (each of which correspond to the input nodes shown in Figure 4, 416, 415 and 414, respectively). This receiver circuit also provides for three output nodes 911, 912 and 913 (each of which correspond to the output nodes shown in Figure 4, 411, 412 and 413, respectively). The receiver also provides for a bi-directional signal node 930, which corresponds to the channel connection 430 shown originally in Figure 4. Receiver circuit 900 includes transistors 1 through 35 electrically coupled together as shown in Figure 9.

In the embodiment shown in Figure 9, receiver circuit 900 is configured as a two stage differential receiver with self biasing. The first stage is a differential input stage composed of transistors 25 and 22. A significant portion of the gain provided by the first stage is achieved because the outputs of this stage go through a cross coupled PMOS network composed of transistors 20 and 26. In addition, this stage is biased with PMOS transistors 21 and 24.

The pair of PMOS transistors 31 and 34 comprise a differential amplifier within the second stage of receiver 900. They have a self bias load composed of transistors 35 and 32. The output is seen at the source of transistor 30.

So the key elements of the first stage are transistors 25 and 22 with the cross coupled PMOS load for high gain composed of transistors 20 and 26. The

first stage drives the second stage with PMOS transistors 31 and 34 which have a self biased pull down network composed of transistors 32 and 35.

In the embodiment shown in Figure 9, the first stage is self biased. Self-biasing is achieved with transistors 13 and 15, which drive the bias network composed of transistors 14 and 16. This is the bias circuit and it drives the pull down stage for the first part of the differential amplifier, which is driven by transistor 23. The other transistor's primary function is to shut off DC power to the circuit when it is not used. In other words, they are not key to the operation but they are added so the DC power can be shut off when this is not used. Transistors 7, 8, 9, 10, 18 and 19 are included for test purposes.

Conclusion

Thus, novel structures and methods for providing more reliable communications between circuits within a given system and more flexible apparatus for implementation has been described. By coupling the output node of the 120 to the input node of the receiver 110 and the channel connection 130, wherein the driver 120 provides a transmission line matching impedance to the channel connection 130 when the driver 120 is placed in an active state, the receiving device is protected from unwanted reflection across transmission lines. The configuration of the receiver 110 and driver 120 disclosed in the present invention allows for the driver 120 to act as a terminating device and thereby supporting increased signaling speeds. Often times practitioners use terminating resistors external to the package containing the communicating circuits, to deal with reflection problems but the novel driver/receiver circuit 100 brings the solution inside the package and thereby saves critical space. Implementing the communication scheme presented also helps to relax design constraints and reduce hard ware costs.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the

above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A driver/receiver circuit, comprising:

a channel connection;

a receiver having a receiver input and a receiver output, wherein the receiver input is connected to the channel connection; and

a driver having a driver input and a driver output, wherein the driver output is connected to the receiver input and to the channel connection and wherein the driver provides a transmission line matching impedance to the channel connection when the driver is placed in an active state.

2. The circuit according to claim 1, wherein the receiver input and the driver output are differential signals.

3. The circuit according to claim 1, wherein the termination line matching impedance is approximately 50 ohms.

4. The circuit according to claim 1, wherein the driver provides both pull-up and pull-down functionality.

5. The circuit according to claim 1, wherein the driver is configured so that it is always in an active state.

6. A communications channel, comprising:

a transmission line;

a driver connected to the transmission line, wherein the driver drives a signal onto the transmission line;

a driver/receiver circuit connected to the transmission line, wherein the driver/receiver circuit includes:

a receiver circuit; and

a driver circuit, wherein an output of the driver is connected to an input of the receiver and to the transmission line and wherein the driver

circuit provides a termination line matching impedance to the transmission line when the driver circuit is placed in an active state.

7. The circuit according to claim 6, wherein the transmission line, receiver input and the driver output are differential.

8. The circuit according to claim 6, wherein impedance of the transmission line and the termination line matching impedance are approximately 50 ohms.

9. The circuit according to claim 6, wherein the driver provides both a pull-up and pull-down functionality.

10. The circuit according to claim 6, wherein the driver is configured so that it is always in an active state.

11. A communications channel, comprising:

a transmission line;

a driver connected to the transmission line, wherein the driver drives a signal on the transmission line and wherein the driver provides a transmission line matching impedance to the transmission line; and

a receiver connected to the transmission line, wherein the receiver receives the signal from the transmission line.

12. The communication channel of claim 11, wherein the transmission line, the receiver and the driver are differential.

13. The communication channel of claim 11, wherein impedance of the transmission line and the transmission line matching impedance are approximately 50 ohms.

14. The communication channel of claim 11, wherein the driver provides both a pull-up and pull-down functionality.

15. The communication channel of claim 11, wherein the driver is configured so that it is always in an active state.

16. An integrated circuit, comprising:

a processor;

a memory, operatively coupled to the processor; and

a receiver/driver circuit; and

wherein the processor, the memory and the receiver/driver circuit are formed on the same semiconductor substrate.

17. A method for matching receiver and transmission line impedances, comprising:

forming a channel connection;

forming a receiver having a receiver input and a receiver output, wherein the receiver input is connected to the channel connection;

forming a receiver circuit, wherein providing at least a first input node and a first output node;

providing a driver having a driver input and a driver output, wherein the driver output is connected to the receiver input and to the channel connection and wherein the driver provides a transmission line matching impedance to the channel connection when the driver is placed in an active state.

18. The method of claim 17, wherein the receiver circuit formed is formed as a differential receiver.

19. The method of claim 17, wherein forming a differential receiver includes driving an input node with a reference voltage.

20. The method of 17, wherein providing a driver circuit further includes providing a driver circuit with pull-up and pull-down functionality.

21. The method of 17, wherein providing a driver circuit further includes biasing the driver circuit so that it is always in active mode.

22. A communications channel, comprising:

a transmission line;

means for driving a signal on the transmission line and for providing a transmission line matching impedance to the transmission line;

means for receiving the signal from the transmission line.

23. The communication channel of claim 22, wherein the transmission line, the means for driving the signal and the means for receiving the signal are differential.

24. The communication channel of claim 22, wherein impedance of the transmission line and the transmission line matching impedance are approximately 50 ohms.

25. The communication channel of claim 22, wherein the means for driving the signal provides both a pull-up and pull-down functionality.

26. The communication channel of claim 22, wherein the means for driving the signal is configured so that it is always in an active state.

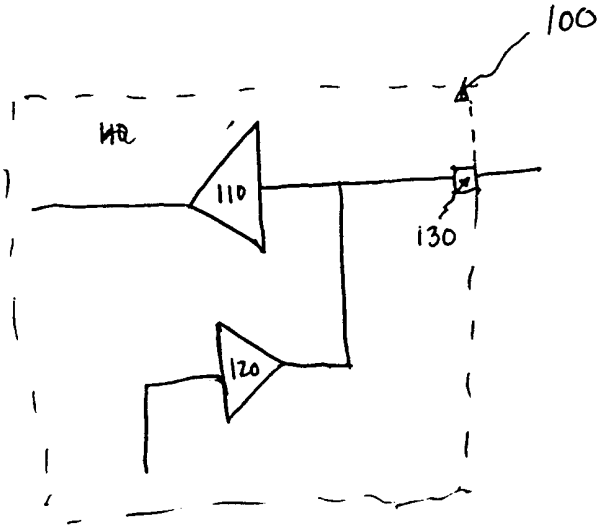

Figure 1

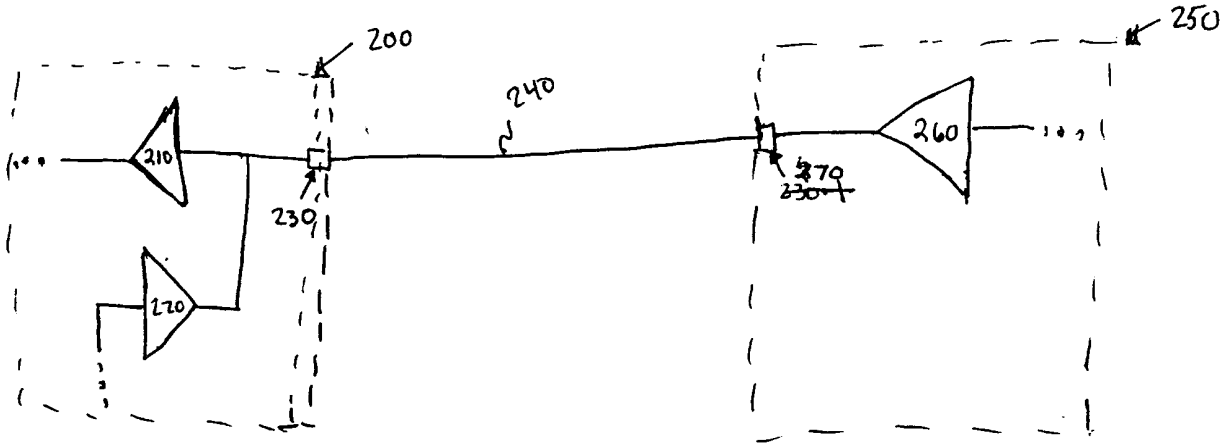

Figure 2

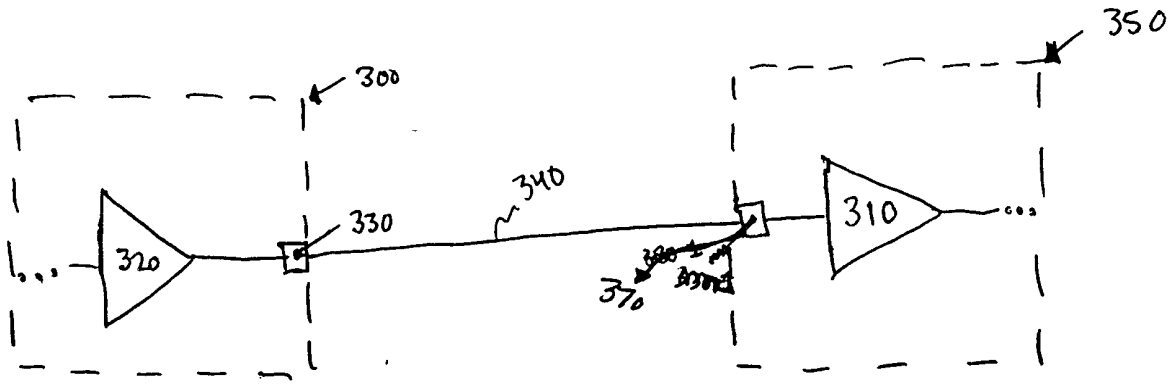

Figure 3

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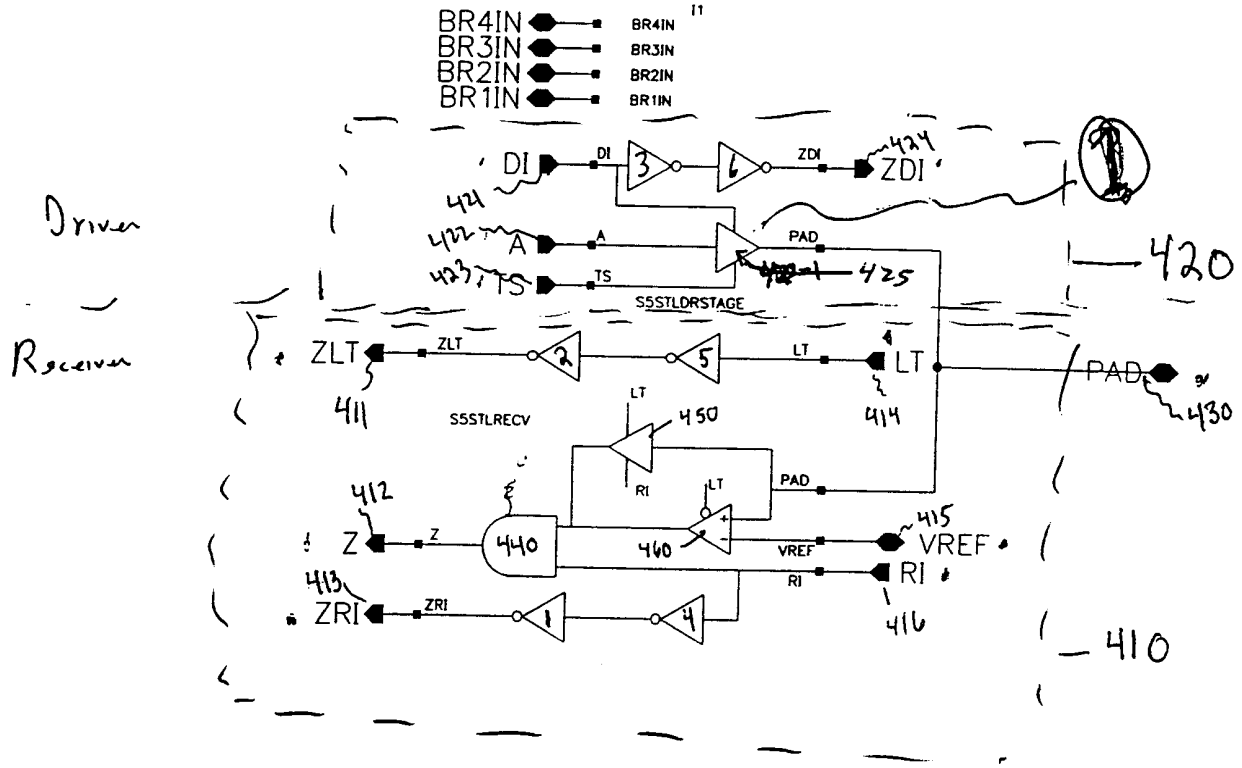

Figure 4

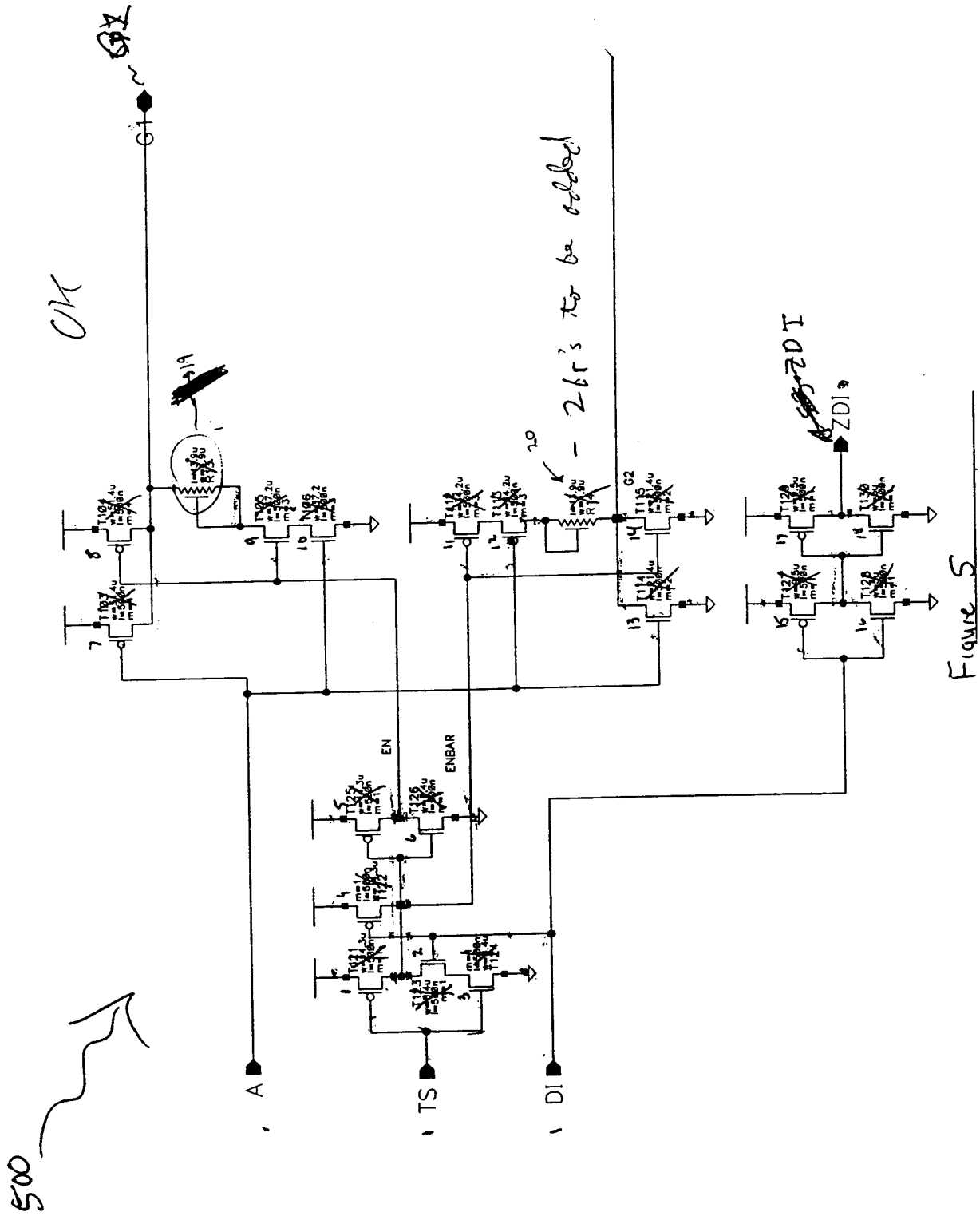

Figure 5

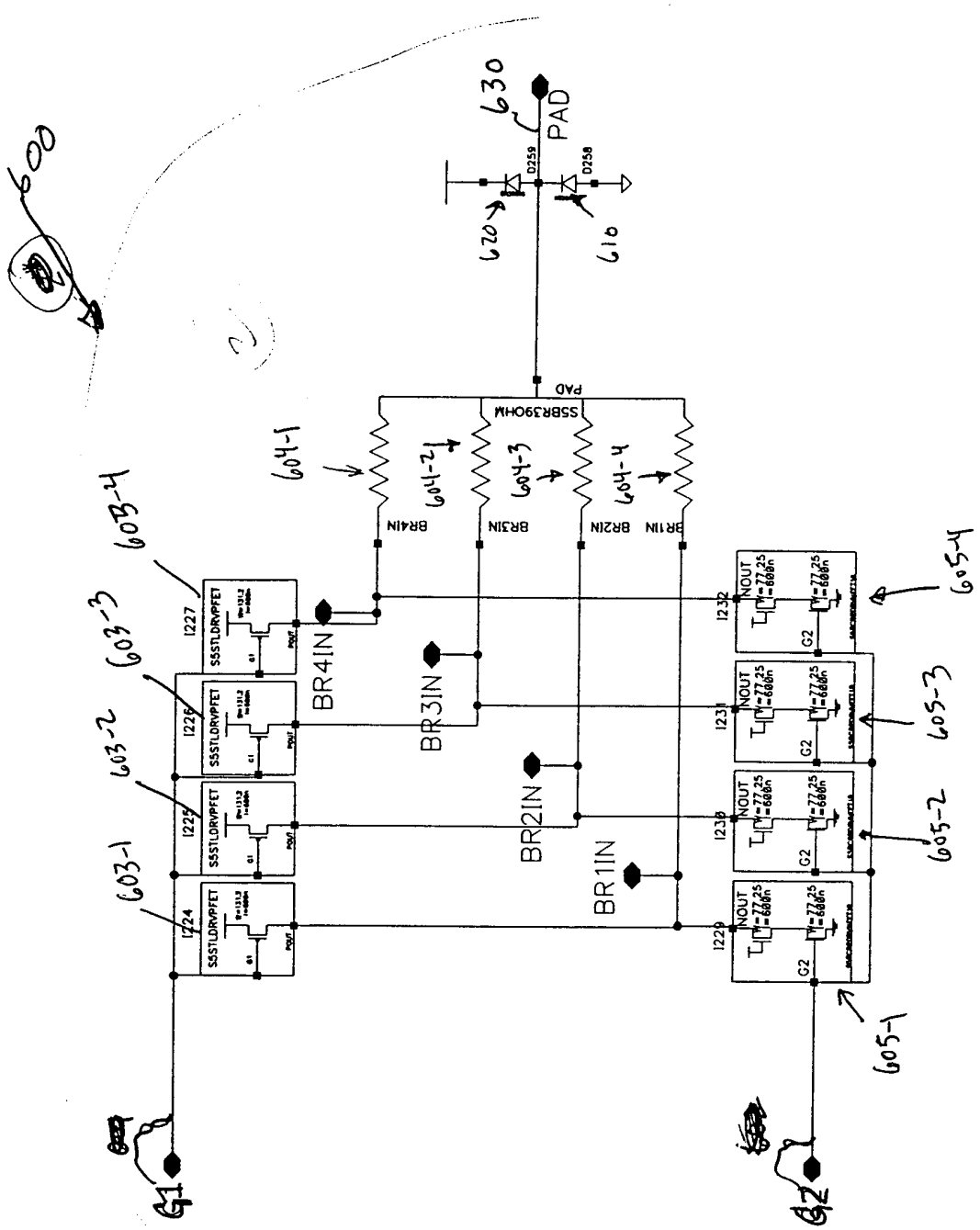
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Figure 6

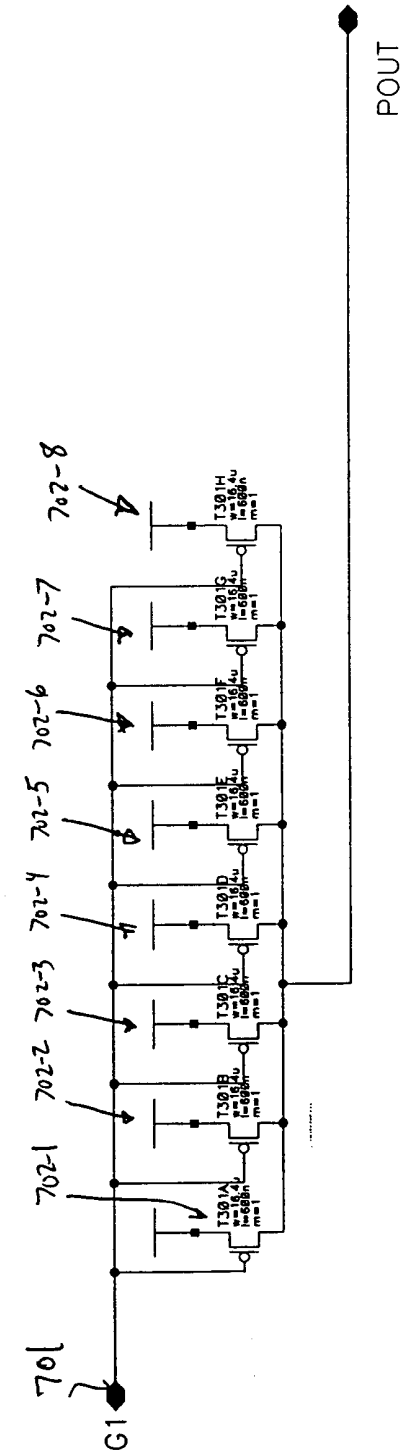

Figure 7

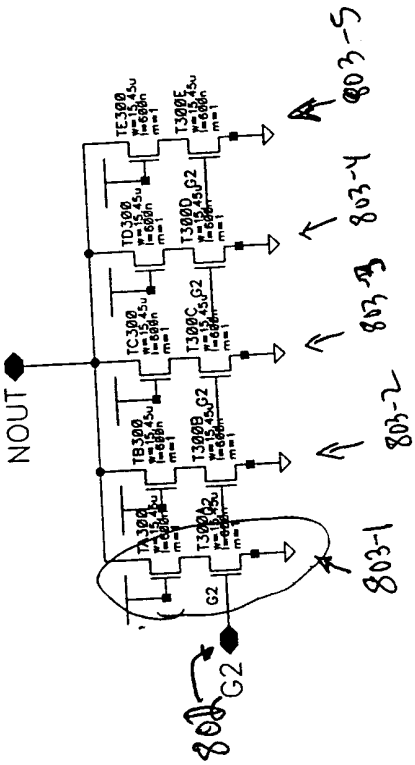

Figure 8

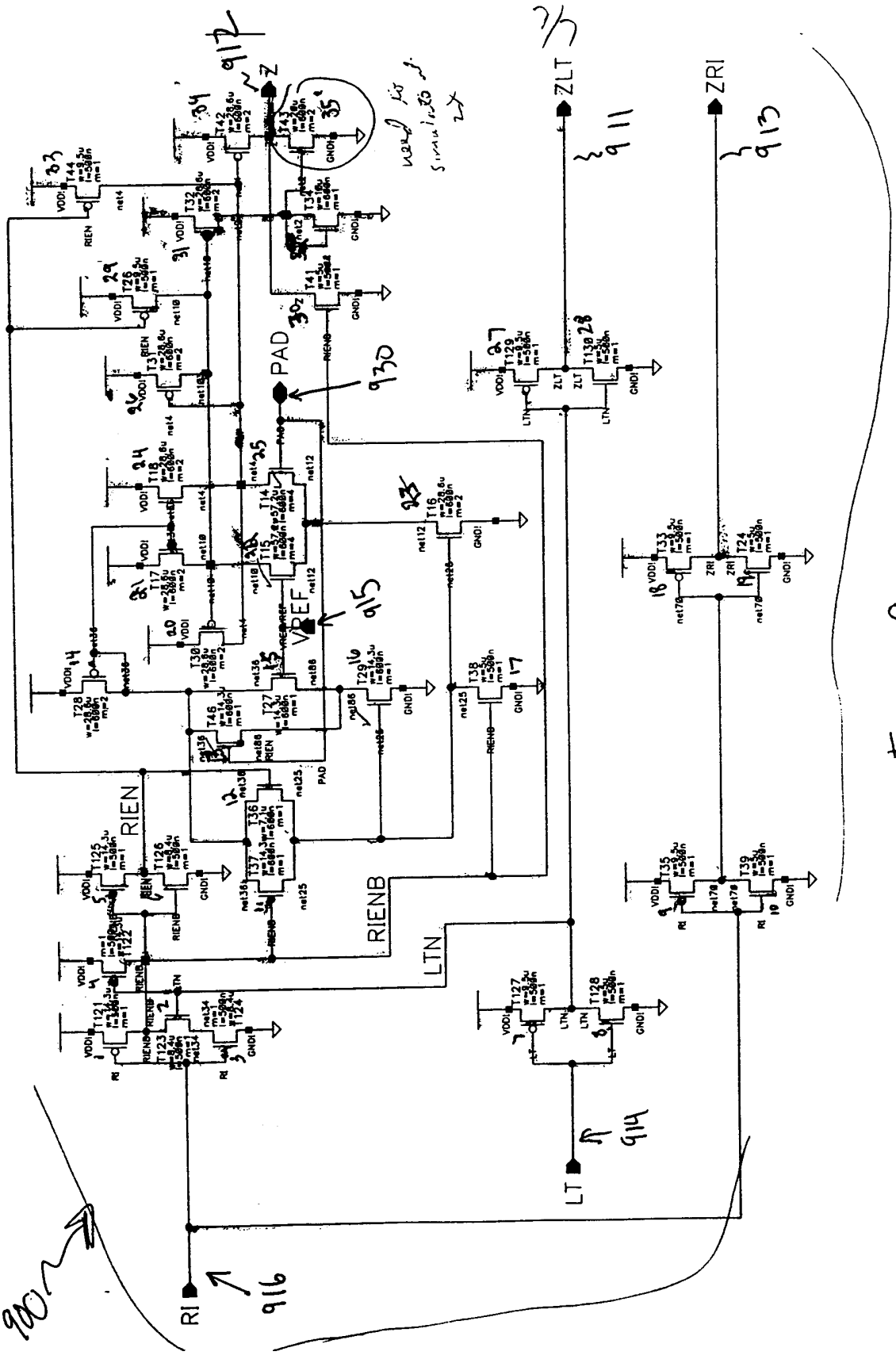

Figure 9

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/26991

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L25/02 H03K19/0175 H03K19/018

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03K H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 802 103 A (JEONG DEOG-KYOON) 1 September 1998 (1998-09-01) figures 4,8,9 column 6, line 57 -column 7, line 2 column 9, line 29 - line 52 column 9, line 60 - line 67 column 10, line 33 - line 48 ---	1-26
X	KYEONGHO LEE ET AL: "A CMOS SERIAL LINK FOR 1 GBAUD FULLY DUPLEXED DATA COMMUNICATION" SYMPOSIUM ON VLSI CIRCUITS,US,NEW YORK, IEEE, 9 June 1994 (1994-06-09), pages 125-126, XP000501054 ISBN: 0-7803-1919-2 page 125, left-hand column, line 45 -right-hand column, line 12; figure 3 --- -/--	1-3,5-8, 10-13, 15-19, 21-24,26

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
5 February 2001	12/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Papantoniou, A

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Interr ›nal Application No
PCT/US 00/26991

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 872 471 A (ISHIBASHI KENICHI ET AL) 16 February 1999 (1999-02-16) abstract; figures 8,9 column 12, line 21 - line 49 column 13, line 13 - line 27 column 13, line 40 - line 55	1-3,5-8, 10-13, 15-18, 21-24,26
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

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Inter...nal Application No
PCT/US 00/26991

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