

(21) Application No: **0328307.4**
(22) Date of Filing: **05.12.2003**

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(51) INT CL⁷:
H04L 1/00 , H03M 13/00

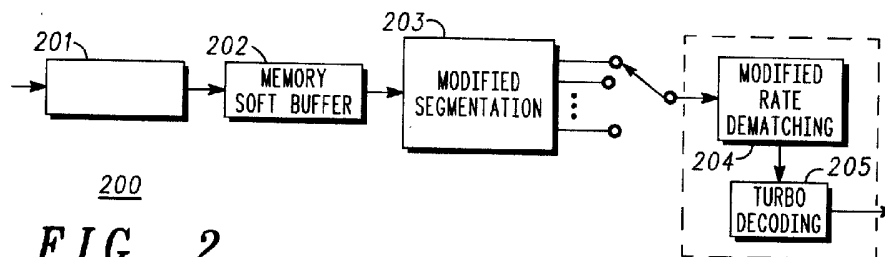
(52) UK CL (Edition X):
H4P PEP

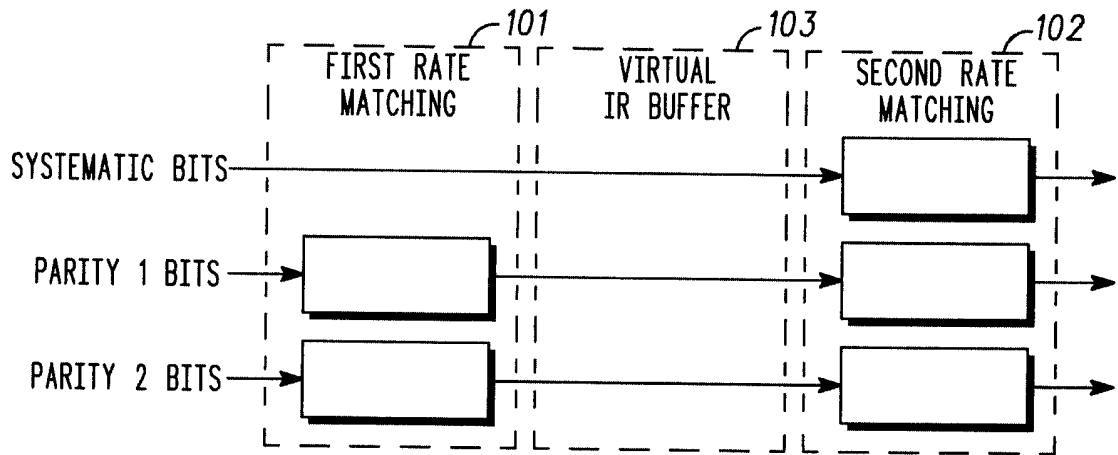
(56) Documents Cited:
EP 1261161 A1 **EP 0797307 A3**
WO 2002/084889 A3 **WO 2002/037698 A3**

(58) Field of Search:
UK CL (Edition W) **H4P**
INT CL⁷ **H03M, H04L**
Other: **Online: WPI, EPODOC, JAPIO**

(54) Abstract Title: **Receiver capable of rate de-matching data block-by-block**

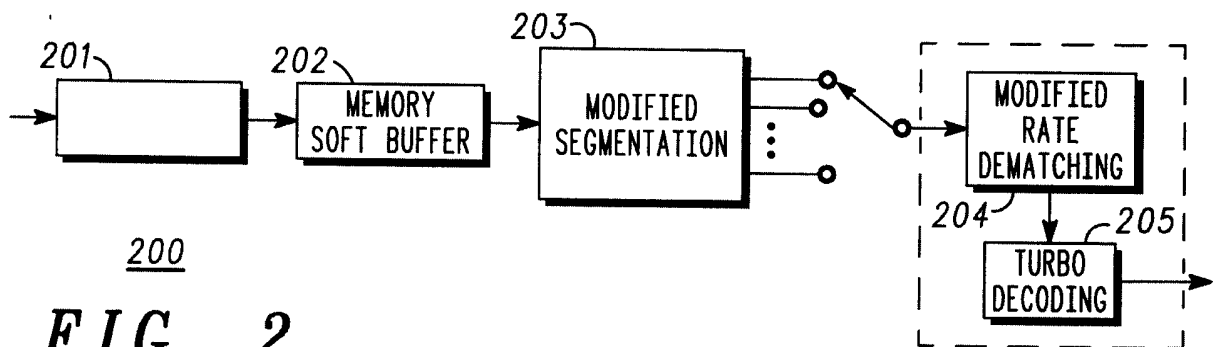
(57) A receiver for a wireless communication device receives data which has been rate-matched (by puncturing or bit repetition) and segments the data into blocks which correspond to the original coding blocks output by the transmitter's encoder, prior to rate matching. The receiver of the present invention is able to perform this segmentation on-the-fly to provide block-by-block rate de-matching and decoding, which reduces buffer capacity between rate de-matching the decoding. This segmentation is achieved by storing the received rate-matched address in a buffer 202 and determining the addresses in that buffer which contain data from the start of each of the original coding blocks. The addresses are preferably determined using rate matching parameters required in the transmitter's iterative rate matching process, for example by using the equation of claim 7.





100

FIG. 1



200

FIG. 2

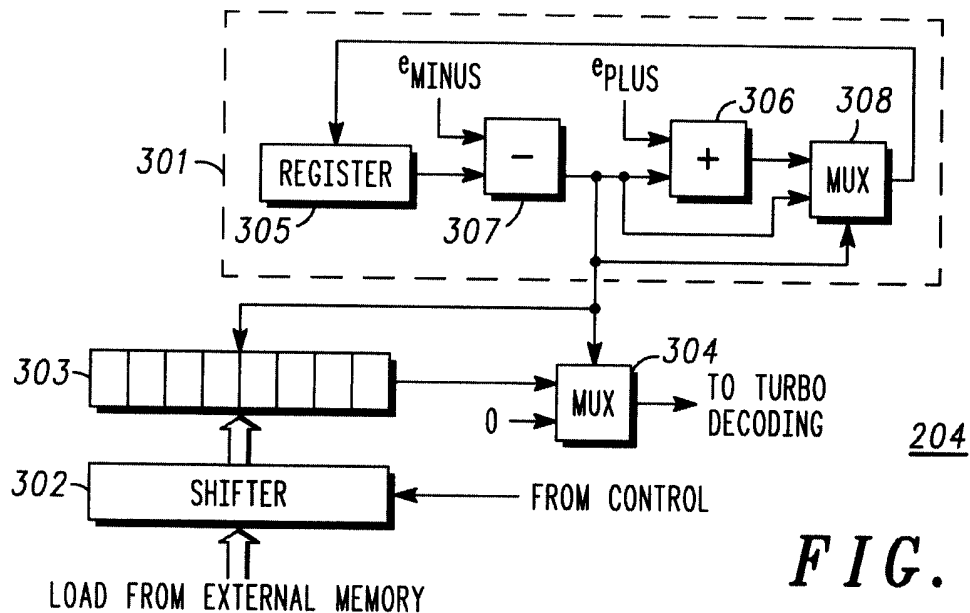


FIG. 3

5 **A RECEIVER FOR A WIRELESS COMMUNICATION DEVICE**

The present invention relates to a receiver for a wireless communication device.

10 Wireless communication systems are widely deployed to provide various types of communications such as voice and data. One such system is wideband code division multiple access WCDMA, which has been adopted in various competing wireless communication standards, for example 3rd generation partnership project 3GPP and 3GPP2.

15 The main physical data channel defined in the 3GPP standard is the high speed downlink shared channel HS-DSCH, which is used to provide high data rates in the downlink direction. The basic transmission unit that is defined for the HSDSCH is the time transmission interval TTI that corresponds to a radio sub-
20 frame of 3 slots.

As defined in the 3GPP TS 25.212 standard the coding for the HS-DSCH channel is performed on a transport block once every TTI (i.e. coding is performed on a block of data that corresponds to the data received during a TTI).

25 The coding involves segmenting a transport block into code blocks for encoding by a turbo encoder and concatenating the encoded data blocks back into transport blocks before passing the transport blocks to a hybrid-automatic repeat request module H-ARQ.

30 As shown in figure 1, the H-ARQ 100 consists of a first stage rate matching module 101, a second stage rate matching module 102 and a virtual buffer 103, with the H-ARQ 100 receiving data from a turbo encoder (not shown).

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During operation data, with CRC bits attached, is input into the turbo encoder, which would typically have a coding rate of 1/3. As the turbo encoder encodes data on a code block by code block basis, where a code block is smaller than a transport block, the transport block is segmented into code block prior to being input into the turbo encoder. The turbo encoder outputs systematic bits, the same data sequence provided to the encoder, and parity 1 bits and parity 2 bits, where the parity 1 and parity 2 bits represent redundancy bits. The systematic bits, the parity 1 bits and the parity 2 bits are provided to the H-ARQ 100 where the first stage rate matching module 101 performs rate matching on the parity 1 bits and parity 2 bits.

The purpose of the first stage rate matching module 101 is to reduce the size of the encoded transport block, by puncturing the code as defined in TS 25.212, to a size that will allow the punctured code (i.e. rate matched) to fit into a specified buffer on a wireless communication receiver.

For example, if the size of the data packet input to the turbo encoder, which corresponds to a transport block, is 100 bits, the output from the turbo encoder will be 300 bits (i.e. 100 systematic bits, 100 parity 1 bits and 100 parity 2 bits). If the receiving equipment has only a 240 bit buffer in the receiving chain, the first stage rate matching module 101 is arranged to reduce the number of bits from 300 to 240 by puncturing 60 bits from the parity 1 bits and parity 2 bits.

To enable the correct puncturing of bits rate-matching parameters (i.e. m_i , the number of bits in a block, e_{init} the rate matching parameter for the initial error e for determining the phase of the bit puncturing, e_{minus} the rate matching parameter that is a decrement of e , and e_{plus} is the rate matching parameter that is an increment of e) are computed based on the number of bits to be punctured for a TTI, as defined in TS 25.212.

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Once the rate matching parameters are computed the rate matching pattern (i.e. the puncturing scheme) can be determined in accordance with the defined algorithm within TS 25.212, which is as follows:

```

10      e = eini                - set initial value for error e

      X = 1                      - set initial value for bit index X

      do while (X ≤ mi)        - perform loop mi times for mi input bits

          e = e - eini          - update error e

          if (e ≤ 0) then        - check if bit mx should be punctured

15              set bit mx to δ    - puncture bit mx by setting it to δ

              e = e + eplus      - update error e after a puncture

          end if

          X = X + 1              - update bit index X for the next bit

      end do

```

20

By way of further illustration, if 18 bits need to be reduced to 16 bits the rate matching parameters would be initially computed as: $m_i = 18$, $e_{ini} = 1$, $e_{plus} = 36$ and $e_{minus} = 4$. Consequently, implementing the above algorithm using these rate matching parameters results in bits 1 and 10 being punctured.

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The virtual buffer 103 stores the rate matched code prior to being further rate matched by the second stage rate matching module 102 to rate match the data stored in the virtual buffer 103 to the actual physical channel size.

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On receipt by the receiving equipment the received rate matched encoded data is initially rate de-matched to remove the effects of the second stage rate matching process and stored in the specified buffer, corresponding in size to the virtual buffer. The receiver then performs rate de-matching on the stored encoded data to replace the bits removed during the first stage rate matching process with zero values. The rate de-matched encoded data, which will be the same size as the encoded transport block (i.e. approximately three times the size of the original transport block), is then stored in memory.

15 The rate de-matched encoded data is then segmented before being passed to a turbo decoder to decode the encoded data.

However, this process requires the use of a large memory to store the rate de-matched encoded data prior to decoding.

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It is desirable to improve this situation.

In accordance with a first aspect of the present invention there is provided a receiver for a wireless communication device according to claim 1.

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This provides the advantage of allowing a receiver for a wireless communication device to have less memory and to save power consumption by requiring less memory accesses as well as reducing processor MIPS.

30 In accordance with a second aspect of the present invention there is provided a method for decoding encoded data in a wireless communication system according to claim 10.

5 An embodiment of the invention will now be described, by way of example, with reference to the drawings, of which:

Figure 1 illustrates a prior art hybrid-automatic repeat request module;

10 Figure 2 illustrates a receiver according to an embodiment of the present invention;

Figure 3 illustrates a rate de-matching stage according to an embodiment of the present invention.

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Figure 2 illustrates a decoding stage 200 of a wireless receiver, for use in a 3GPP W-CDMA radiotelephone.

The decoding stage 200 includes a second stage rate de-matching module
20 201, a buffer 202, a segmentation module 203, a first stage rate de-matching module 204 and a turbo decoder 205.

The decoding stage 200 receives rate matched encoded data transmitted by a 3GPP compliant transmitter and inputs the data to the second stage rate de-
25 matching module 201. The second stage rate de-matching module 201 reverses the effects of the second stage rate matching performed by the H-ARQ 100 within the transmitter to generate data that represents the first stage rate matched encoded data generated by the first stage rate matching module 101 within the H-ARQ 100.

30

The replicated first stage rate matched encoded data is input into the buffer 202, which is typically a ratio of the size of the virtual buffer 103 in the transmitter

- 5 H-ARQ 100. For example, if each bit in the transmitter corresponds to a byte being received by the receiver the buffer 202 will be eight times the virtual buffer 103.

As the rate matching process involves the puncturing of data the size of a rate matched encoded data block will be smaller than the corresponding rate de-
10 matched encoded block (i.e. the original pre rate matched data). Consequently, the code block boundaries for the rate matched encoded data stored in the buffer 202 will no longer correspond to the original code block boundaries of the encoded data prior to rate matching performed by the first stage rate matching module 101. Accordingly, if the rate de-matching module 204 extracted the rate matched
15 encoded data from the buffer 202 using the original code block base addresses and provided the corresponding rate de-matched encoded data to the turbo decoder 205 on a block by block basis incorrect results would be obtained.

To allow the first rate de-matching module 204 to extract the rate matched
20 encoded data from the buffer 202 such that the first rate de-matching module 204 is able to rate de-match the encoded data and provide the data to the turbo decoder 205 on a block by block basis (i.e. on the fly) the segmentation module 203 is arranged to determine the locations in the rate matched encoded data stored in the buffer 202 that correspond to the original base addresses for the pre
25 rate matched encoded data (i.e. the rate matched block base addresses).

Accordingly, using the rate matched block base addresses the first stage rate de-matching module 204 extracts the rate matched encoded data and performs rate de-matching on segments of data that correspond to the original code blocks,
30 thereby allowing the turbo decoder 205 to decode the encoded code blocks on the fly from data received from the first stage rate de-match module 204 and thus avoiding the need to store rate de-matched data prior to decoding by the decoder 205.

- 5 The rate de-matching algorithm used by the first rate de-matching module 204 to recover the punctured data (i.e. data replication) is:

	$e = e_{ini}$	- set initial value for error e
	$X = 1$	- set initial value for bit index X
10	do while ($X \leq m_i$)	- perform loop m_i times for m_i input bits
	$e = e - e_{minus}$	- update error e
	if ($e \leq 0$) then	- check if bit X should be repeated
	repeat bit m_x	- repeat bit m_x
	$e = e + e_{plus}$	- update error e after a repetition
15	end if	
	$X = X + 1$	- update bit index X for the next bit
	end do	

- 20 The basis for the derivation of the rate matched base addresses generated by the segmentation module 203 is as follows:

From the rate de-matching algorithm described above, and as specified in TS 25.212, it can be concluded that the value of e after i iterations of the algorithm can be defined as

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$$e = e_{init} - ie_{minus} + N_{punc}e_{plus} \quad (1.1)$$

5 where N_{punc} is the number of inserted zero values in the rate de-matching process after i iterations.

As $e_{int} \leq e_{plus}$ then e must be greater than 0 and e must be smaller or equal to e_{plus} after a complete iteration of the rate matching algorithm.

10

Accordingly equation 1.1 can be written

$$0 < e_{int} - ie_{minus} + N_{punc}e_{plus} \leq e_{plus} \quad 1.2)$$

15 Therefore,

$$\frac{-e_{int} + ie_{minus}}{e_{plus}} < N_{punc} \leq \frac{-e_{int} + ie_{minus}}{e_{plus}} + 1 \quad 1.3)$$

Since N_{punc} has to be an integer it follows that

20

$$N_{punc} = \left\lfloor \left[\frac{ie_{minus} - e_{int}}{e_{plus}} + 1 \right] \right\rfloor \text{ where } \lfloor x \rfloor \text{ is the floor of the function 'x'}$$

As such, N_{punc} represents the number of bits that will be inserted after i iterations of the algorithm.

25

Accordingly to find the equivalent base addresses of the original encoded code blocks (i.e. pre-rate matched data) within the rate matched encoded data stored in the buffer 202 i is replaced with the original encoded code block base

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addresses (i.e. 0, B, 2B, 3B etc) and N_{punc} is subtracted from the original code block base address.

Consequently, the base address for the first code block will be zero. The
10 base address for the second code block will be:

$$B - \left[\left[\frac{Be_{\text{minus}} - e_{\text{mit}}}{e_{\text{plus}}} + 1 \right] \right]$$

The base address for the third code block will be:

$$2B - \left[\left[\frac{2Be_{\text{minus}} - e_{\text{mit}}}{e_{\text{plus}}} + 1 \right] \right]$$

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and so on.

The above calculations are performed independently for both parity 1 bits
and parity 2 bits – which are both rate matched by the first rate matching module
20 101. As the systematic bits are not rate matched by the first rate matching module
101 the original code block base addresses can be used when reading the data
out of the buffer 202.

To compensate for the change in the determination of code block boundary base
25 addresses, the rate de-matching module 204 is arranged to calculate e_{mit} for each
received block of rate matched encoded data where e_{mit} is set equal to the initial
value of e_{mit} for the first block and for subsequent code blocks

$$e_{\text{mit}} = e_{\text{mit}} - Be_{\text{minus}} + \left[\frac{Be_{\text{minus}} - e_{\text{mit}}}{e_{\text{plus}}} + 1 \right] e_{\text{plus}}$$

5 where B corresponds to the location that would equate to the start of a code block for a given rate de-matched block number.

Figure 3 illustrates the rate de-matching module 204. The rate de-matching
10 module 204 includes a circuit 301 for implementing the de-puncturing algorithm specified above, a shifter 302, a data shift register 303 (e.g. a FIFO) and a first multiplexer 304.

The circuit 301 for implementing the de-puncturing algorithm includes a
15 register 305, an adder 306, a subtractor 307, and a second multiplexer 308. The register 305 holds the value of e after each rate dematching cycle (i.e. iteration). The value of e stored in the register 305 is provided to the subtractor 307 where the value of e_{minus} is subtracted from e . The result of the subtraction determines whether a current bit should be de-punctured (i.e. if a zero value should be
20 inserted into the code block). If a zero should be inserted into the code block a control signal is sent from the subtractor 307 to the first multiplexer 304. In addition, the result of the subtraction is provided to the adder 306 where the value of e_{plus} is added to the result, which is provided to the second multiplexer 308. If the value of $e - e_{\text{minus}}$ is positive the multiplexer 308 stores $e - e_{\text{minus}}$ in the register
25 305, if the values of $e - e_{\text{minus}}$ is negative the multiplexer 308 stores $e - e_{\text{minus}} + e_{\text{plus}}$ in the register 305.

Once the segmentation module 203 has calculated the code block boundaries, as described above, the data stored in the buffer 202 is loaded into
30 the shifter 302, which is used to shift the input data to that the data is aligned with the end of the FIFO 303 (i.e. the data shift register) queue. The shifter 302 receives a control signal indicating the current length of the queue (i.e. the number of valid bits in the queue), thereby allowing the shifter 302 to place new received data at the end of the queue.

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5 The data loaded into the shifter 302 is then loaded into the data shift register 303, which feeds the data to the first multiplexer 304. If no control signal is received from the subtractor 307 the first multiplexer 304 outputs a bit from the FIFO 303 to the decoder 205 for decoding, if a control signal is received from the subtractor 307 a zero is added to the data stream and output to the decoder 205.

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 It will be apparent to those skilled in the art that the disclosed subject matter may be modified in numerous ways and may assume many embodiments other than the preferred forms specifically set out as described above, for example the above embodiments could be arranged such that the rate de-matching module 204
15 could be arranged to determine the equivalent base addresses of the pre rate matched encoded code blocks within the rate matched encoded code blocks stored in the buffer 202, which the rate de-matching module 204 uses to allow the rate de-matching module 204 and turbo decode 205 to rate de-match and decode respectively on the fly on a code block by code block basis.

5 CLAIMS

- 10 1. A receiver for a wireless communication device comprising means for determining a sequence of code block addresses for received rate matched encoded data to allow rate de-matching and decoding to be performed on a code block by code block basis for the received rate matched encoded data.
- 15 2. A receiver according to claim 1, wherein the means for determining a sequence of code block addresses is performed by a segmentation module.
- 20 3. A receiver according to any preceding claim, further comprising a rate de-matching module for rate de-matching the received rate matched encoded data on a code block by block basis using the code block addresses derived by the segmentation module, thereby generating rate de-matched data on a block by block basis.
- 25 4. A receiver according to claim 3, further comprising a buffer for storing received rate matched encoded data, wherein the rate de-matching module is arranged to rate de-match the rate matched encoded data on the fly from the buffer.
- 30 5. A receiver according to claim 3 or 4, further comprising a decoder for decoding the rate de-matched data generated by the rate de-matching module on a block by block basis.

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6. A receiver according to any preceding claim, wherein the means for determining is arranged to derive the sequence of code block addresses for the received rate matched encoded data using rate matching parameters used to rate match the received rate matched encoded data.

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7. A receiver according to any preceding claim, wherein the means for determining is arranged to derive the sequence of code block addresses using:

$$B - \left\lceil \left[\frac{Be_{\text{minus}} - e_{\text{init}}}{e_{\text{plus}}} + 1 \right] \right\rceil$$

- 15 where B corresponds to the location that would equate to the start of a code block for a given rate de-matched block number;

e_{init} is the rate matching parameter for the initial value of e for determining the phase of bit puncturing ;

e_{minus} is the rate matching parameter that is a decrement of e;

- 20 e_{plus} is the rate matching parameter that is an increment of e.

8. A receiver according to claim 7, wherein the rate de-matching module is arranged to calculate e_{init} for each received block of rate matched encoded data.

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9. A receiver according to claim 8, wherein the rate de-matching module is arranged to derive the e_{init} value for block of received rate de-matched encoded data using:

5 $e_{int} = e_{int}$ for the first block and

$$e_{int} = e_{int} - Be_{minus} + \left[\frac{Be_{minus} - e_{int}}{e_{plus}} + 1 \right] e_{plus}$$

for the second and subsequent blocks, where B corresponds to the location that would equate to the start of a code block for a given rate de-matched block number.

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10. A method for decoding encoded data in a wireless communication system, the method comprising receiving rate matched encoded data; determining a sequence of code block addresses for the received rate matched encoded data; rate de-matching the received rate matched encoded data on a block by block basis using the sequence of code block addresses to determine block boundaries within the received rate matched encoded data; and decoding rate de-matched data on a block by block basis.

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11. A receiver substantially as hereinbefore described with reference to the figures.

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12. A method for rate de-matching substantially as hereinbefore described with reference to the figures.

25

5 **CLAIMS**

10 1. A wireless communication device comprises a receiver comprising means for determining a sequence of code block addresses for received rate matched encoded data, wherein the means identifies a code block boundary of pre-rate matched data and performs rate de-matching and decoding independently on a code block by code block basis for the received rate matched encoded data.

15 2. A wireless communication device according to claim 1, wherein the means for determining a sequence of code block addresses is performed by a segmentation module.

20 3. A wireless communication device according to claim 2, further comprising a rate de-matching module for rate de-matching the received rate matched encoded data on a code block by block basis using the code block addresses derived by the segmentation module, thereby generating rate de-matched data on a block by block basis.

25 4. A wireless communication device according to claim 3, further comprising a buffer for storing received rate matched encoded data, wherein the rate de-matching module is arranged to rate de-match the rate matched encoded data on the fly from the buffer.

30 5. A wireless communication device according to claim 3 or 4, further comprising a decoder for decoding the rate de-matched data generated by the rate de-matching module on a block by block basis.

- 5 6. A wireless communication device according to any preceding claim, wherein the means for determining is arranged to derive the sequence of code block addresses for the received rate matched encoded data using rate matching parameters used to rate match the received rate matched encoded data.

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7. A wireless communication device according to claim 2, wherein the segmentation module determines an address of first data in each code block independently.

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8. A wireless communication device according to claim 7, wherein the segmentation module determines an address of end data of each code block independently of determining the address of first data.

9. A wireless communication device according to any preceding claim, wherein the means for determining is arranged to derive the sequence of code block addresses using:

$$B - \left[\left[\frac{Be_{\text{minus}} - e_{\text{init}}}{e_{\text{plus}}} + 1 \right] \right]$$

where B corresponds to the location that would equate to the start of a code block for a given rate de-matched block number;

- 25 e_{init} is the rate matching parameter for the initial value of e for determining the phase of bit puncturing ;

e_{minus} is the rate matching parameter that is a decrement of e;

e_{plus} is the rate matching parameter that is an increment of e.

5 10. A wireless communication device according to claim 9, wherein the rate de-matching module is arranged to calculate e_{init} for each received block of rate matched encoded data.

10 11. A wireless communication device according to claim 10, wherein the rate de-matching module is arranged to derive the e_{init} value for block of received rate de-matched encoded data using:

$e_{init} = e_{init}$ for a first block and

$$e_{init} = e_{init} - Be_{minus} + \left[\frac{Be_{minus} - e_{init}}{e_{plus}} + 1 \right] e_{plus}$$

15 for second and subsequent blocks, where B corresponds to a location that would equate to a start of a code block for a given rate de-matched block number.

20 12. A method for decoding encoded data in a wireless communication system, the method comprising receiving rate matched encoded data; determining a sequence of code block addresses for a received rate matched encoded data; identifying a code block boundary of pre-rate matched data; rate de-matching the received rate matched encoded data on a block by block basis using the code block block boundary; and decoding rate de-matched data independently on a block by block basis.

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13. A receiver substantially as hereinbefore described with reference to the figures.

14. A method for rate de-matching substantially as hereinbefore described with reference to the figures.



Application No: GB0328307.4

Examiner: John Cullen

Claims searched: 1-12

Date of search: 22 April 2004

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular reference
X	1-5, 10	EP 0797307 A3 (KENWOOD) See whole document, but particularly lines 35-45 of col.4 and line 38 of col. 6 to line 47 of col. 7.
X	1, 6, 10	WO 02/037698 A3 (QUALCOMM) See abstract, Figs. 8 and 10, and line 17 of p20 to line 20 of p29.
X	1-5 and 10	EP 1261161 A1 (MITSUBISHI) See Fig. 4 and paras 50-59.
A	---	WO 02/084889 A3 (INTERDIGITAL) See abstract, Fig. 4 and equation 28.

Categories:

X Document indicating lack of novelty or inventive step	A Document indicating technological background and/or state of the art.
Y Document indicating lack of inventive step if combined with one or more other documents of same category.	P Document published on or after the declared priority date but before the filing date of this invention.
& Member of the same patent family	E Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^W :

H4P

Worldwide search of patent documents classified in the following areas of the IPC⁰⁷

H03M; H04L

The following online and other databases have been used in the preparation of this search report

Online: WPI, EPODOC, JAPIO