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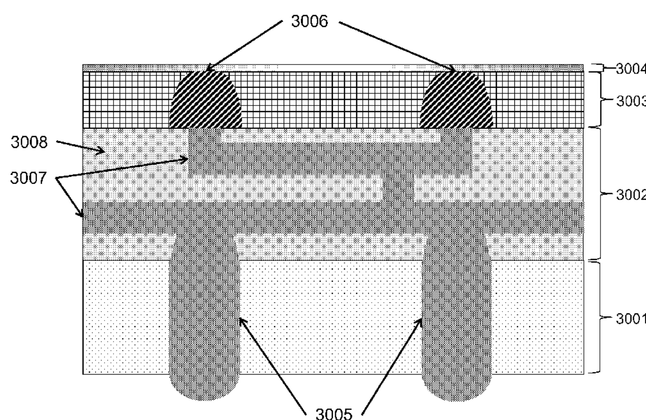

Figure 3

(57) **Abstract**: A photovoltaic device includes a semiconductor layer having photovoltaic solar cells formed therein, a handle substrate; and an interconnect layer disposed between the semiconductor layer and the handle substrate. The interconnect layer includes electrically conductive paths electrically connected to the photovoltaic solar cells in the semiconductor layer. A process forms photovoltaic devices in a semiconductor substrate; forms a planar interconnect layer having insulated, electrically conductive paths, the planar interconnect layer being formed on one of the semiconductor substrate and a planar handle substrate; bonds the other of the semiconductor substrate and the planar handle substrate to the interconnect layer to form a bonded stack in which the electrically conductive paths are electrically connected to the photovoltaic devices; and thins the semiconductor substrate to at least reduce the thickness of the semiconductor substrate between a face and the photovoltaic devices to improve the efficiency of the photovoltaic devices.

A PHOTOVOLTAIC DEVICE AND A PROCESS FOR PRODUCING A PHOTOVOLTAIC DEVICE

TECHNICAL FIELD

The present invention relates to a photovoltaic device and a process for producing a
5 photovoltaic device.

BACKGROUND

High energy loss processes in conventional, homo-junction solar cells effectively limit the useful portion of the solar spectrum in these devices to photons with energies in a
10 narrow range above the band-gap of the semiconductor material. The lateral field *p-i-n* solar cells described in International Patent Application No. PCT/AU2010/000453 ("the lateral field device patent application") seek to overcome this difficulty by adopting a device configuration that results in essentially all photo-generated carriers, including those with high energies, being collected. In practice, where these devices are formed in
15 a semiconductor layer attached to a transparent substrate/superstrate, their conversion efficiency is limited by two substrate-related effects. First, up to 20% of the incident photons are absorbed in the supporting substrate. Second, where the semiconductor layer is epitaxially grown on a transparent, single crystal substrate (*e.g.*, sapphire), defects arising from crystal mismatch and trapped states at the interface between the
20 semiconductor layer and the supporting substrate significantly reduce the diffusion length of carriers within these devices, significantly reducing the energy conversion efficiency.

It is desired to provide a photovoltaic device and a process for producing a photovoltaic
25 device that alleviate one or more difficulties of the prior art, or at least provide a useful alternative.

SUMMARY

In accordance with some embodiments of the present invention, there is provided a process for forming a photovoltaic device, including:

forming photovoltaic devices in a first face of a planar semiconductor substrate having opposed first and second faces;

forming a planar interconnect layer having electrically conductive paths with electrically insulating regions therebetween, the planar interconnect layer being formed on one of the semiconductor substrate and a planar handle substrate;

bonding the other of the semiconductor substrate and the planar handle substrate to the interconnect layer to form a bonded stack wherein the electrically conductive paths in the planar interconnect layer are electrically connected to the photovoltaic devices in the semiconductor substrate; and

thinning the semiconductor substrate from its second face to at least reduce the thickness of the semiconductor between the second face and the photovoltaic devices in the semiconductor substrate to improve the efficiency of the photovoltaic devices.

In some embodiments, the process includes selecting the reduced thickness of the semiconductor to provide a balance between absorption of incident photons and allowing charge carriers generated by the absorbed photons to be collected.

In some embodiments, the process includes selecting the reduced thickness of the semiconductor to provide sufficient heat extraction from the device.

In some embodiments, said thinning removes substantially all of the semiconductor between the second face of the semiconductor substrate and the photovoltaic solar cells therein.

In some embodiments, the photovoltaic devices are lateral field photovoltaic devices.

In some embodiments, the electrically conductive paths of the interconnect layer include one or more electrically conductive paths extending to one or more edges of the interconnect layer to provide one or more electrical contacts to the photovoltaic devices.

5 In some embodiments, the handle substrate is electrically insulating, and the process includes forming one or more electrically conductive paths through the handle substrate, wherein the electrically conductive paths of the interconnect layer include one or more electrically conductive paths that electrically connect one end of each electrically conductive path through the handle layer to the photovoltaic devices, the 10 other end of each electrically conductive path through the handle layer providing an external electrical contact to the photovoltaic devices.

In some embodiments, the process includes forming electronic circuitry in the handle substrate to process output of the photovoltaic devices.

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In some embodiments, the handle substrate is made from a material having a high thermal conductivity to provide cooling to the photovoltaic device.

In accordance with some embodiments of the present invention, there is provided a 20 photovoltaic device, including:

a semiconductor layer having photovoltaic solar cells formed therein;

a handle substrate; and

an interconnect layer disposed between the semiconductor layer and the handle substrate and including electrically conductive paths electrically 25 connected to the photovoltaic solar cells in the semiconductor layer.

In some embodiments, the semiconductor layer has opposed first and second faces, the semiconductor layer is attached to the interconnect layer by the first face, and the photovoltaic devices are formed in the first face.

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In some embodiments, the photovoltaic devices are spaced from the second face of the semiconductor layer by a thickness of semiconductor.

In some embodiments, the semiconductor between the second face and the photovoltaic devices has a thickness that provides a balance between absorption of photons incident on the second face and allowing charge carriers generated by the absorbed photons to be collected.

In some embodiments, the interconnect layer includes a plurality of metal layers.

In some embodiments, the photovoltaic devices are lateral field photovoltaic devices.

In some embodiments, the electrically conductive paths of the interconnect layer include one or more electrically conductive paths extending to one or more edges of the interconnect layer to provide one or more electrical contacts to the photovoltaic devices.

In some embodiments, the handle substrate is electrically insulating but includes one or more electrically conductive paths through the handle substrate, and the electrically conductive paths of the interconnect layer include one or more electrically conductive paths that electrically connect one end of each electrically conductive path through the handle layer to the photovoltaic devices, and the other end of each electrically conductive path through the handle layer provides an external electrical contact to the photovoltaic devices.

In some embodiments, the handle substrate includes electronic circuitry configured to process output of the photovoltaic devices.

In some embodiments, the device includes an integrated circuit chip that is flip chip bonded to conductive paths of the handle substrate.

In some embodiments, the handle substrate is made from a material having a high thermal conductivity to provide cooling to the photovoltaic device.

In accordance with some embodiments of the present invention, there is provided a process for forming a photovoltaic device, including:

forming a plurality of mutually spaced recesses in a face of a semiconductor layer;

5 doping at least the sidewalls of the recesses in the semiconductor layer and filling the recesses with a conductive material to form sets of conductive regions having respective opposite doping polarities;

wherein each pair of adjacent and oppositely doped conductive regions forms a corresponding space charge region having a corresponding electric field therein, 10 the space charge region extending substantially from the surface of the semiconductor layer and into the semiconductor layer such that electron-hole pairs created substantially at the surface of the semiconductor layer by photons entering the space charge region are separated in opposing directions by the electric field and collected by the corresponding pair of doped regions, thereby 15 providing an electrical current to be conducted from the device.

In some embodiments, the doped regions extend into the semiconductor layer in a direction substantially orthogonal to the face of the semiconductor layer, where the depth of each doped region is greater than its width.

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In some embodiments, the depth of each doped region is at least twice its width.

In some embodiments, each pair of adjacent and oppositely doped conductive regions and the region therebetween forms a corresponding p-i-n diode.

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In some embodiments, the sets of conductive regions having respective opposite doping polarities have an interdigitated configuration.

In some embodiments, the mutually spaced recesses include a first set of mutually 30 spaced recesses extending into the semiconductor layer to a first depth, and a second set of mutually spaced recesses extending into the semiconductor layer to a second depth greater than the first depth, at least the sidewalls of the first set of mutually spaced

recesses being doped to a first polarity, and at least the sidewalls of the second set of mutually spaced recesses being doped to a second polarity opposite to the first polarity.

In some embodiments, the sidewalls and bases of the second set of recesses are doped to form a corresponding set of mutually spaced doped regions that extend through the semiconductor layer to a doped layer of the second polarity.

In some embodiments, the process includes forming electrical contacts to the conductive regions, and bonding the electrical contacts to corresponding electrical contacts of a support.

In some embodiments, the semiconductor layers are semiconductor wafers, and the process includes applying the process of any one of claims 21 to 27 to a plurality of semiconductor wafers, forming electrical contacts to the conductive regions of the processed semiconductor wafers, and bonding the electrical contacts of the processed semiconductor wafers to corresponding electrical contacts of a support so that the processed semiconductor wafers are supported by and electrically interconnected by the support.

In some embodiments, the semiconductor layers are semiconductor-on-insulator wafers.

In some embodiments, the sets of conductive regions are spaced from a second face of the semiconductor layer opposite to the face in which the recesses were formed, and the process includes removing a portion of the semiconductor layer from the second face to reduce the thickness of semiconductor between the conductive regions and the second face.

In some embodiments, the sets of conductive regions are spaced from a second face of the semiconductor layer opposite to the face in which the recesses were formed, and the process includes removing a portion of the semiconductor layer from the second face to remove the semiconductor between at least one of the sets of conductive regions and the second face.

In some embodiments, said removing reduces the thickness of an inner portion of the semiconductor layer while leaving a relatively thick peripheral portion of the semiconductor layer to act as a structural support for the processed semiconductor layer.

In some embodiments, the process includes:

directing an energetic beam of at least one species into the recesses in the face of the semiconductor layer to implant the at least one species into the semiconductor layer, the implantation being performed at a plurality of different relative orientations between the energetic beam and the semiconductor layer to form a buried non-planar defective layer within the semiconductor layer; and

heating the implanted layer so that the non-planar defective layer within the semiconductor layer causes the semiconductor layer to split into two layers, each of said layers having a non-planar surface corresponding to the non-planar defective layer.

In accordance with some embodiments of the present invention, there is provided a process for forming a photovoltaic device, including:

forming a plurality of mutually spaced recesses in a face of a semiconductor substrate;

directing an energetic beam of at least one species into the recesses in the face of the semiconductor substrate to implant the at least one species into the semiconductor substrate, the implantation being performed at a plurality of different relative orientations between the energetic beam and the substrate to form a buried non-planar defective layer within the semiconductor substrate; and

heating the implanted substrate so that the non-planar defective layer within the semiconductor substrate causes the substrate to split into two layers, each of said layers having a non-planar surface corresponding to the non-planar defective layer.

In some embodiments, the remaining portions of the face of the semiconductor substrate between the recesses have a masking layer thereover to substantially prevent those portions of the face from being implanted, the different relative orientations between the energetic beam and the substrate being selected so that the buried non-planar defective layer extends beneath the masked portions of the face.

In some embodiments, the process includes:

forming micro-electronic and/or micro-mechanical devices in the semiconductor substrate; and

bonding the semiconductor substrate to a support;

wherein said heating causes the substrate to split into two layers, one of which remains bonded to the support and includes the devices.

In some embodiments, the support includes electrically conductive paths that form electrical connections to the devices when the support is bonded to the semiconductor substrate.

In some embodiments, the devices are photovoltaic devices, and the electrically conductive paths interconnect the photovoltaic devices.

In some embodiments, the photovoltaic devices are lateral field *p-i-n* photovoltaic devices with high aspect ratio doped regions.

In some embodiments, the devices include dielectric and metal regions that cause light passing through the semiconductor layer without being absorbed to be redirected back into the semiconductor layer for absorption therein.

In some embodiments, the process includes forming an anti-reflection coating on the non-planar surface of one of the layers.

In some embodiments, the process includes forming a second non-planar semiconductor layer on the non-planar surface of one of the layers, the second semiconductor layer

having a larger bandgap than the other semiconductor layer to preferentially absorb high energy photons therein.

In some embodiments, the process includes forming an anti-reflection coating on the second non-planar semiconductor layer.

In some embodiments, the anti-reflection coating includes trapped charge to reduce surface recombination of charge carriers.

The non-planar surface may have advantageous optical properties for the photovoltaic device.

BRIEF DESCRIPTION OF THE DRAWINGS

Some embodiments of the present invention are hereinafter described, by way of example only, with reference to the accompanying drawings, wherein:

Figures 1A and 1B are schematic diagrams illustrating the operation of a standard prior art photovoltaic device having a planar space-charge region orthogonal to incident photons;

Figure 2 is a schematic diagram illustrating the operation of a lateral field photovoltaic device having a space-charge region parallel and coincident with incident photons;

Figure 3 is a schematic diagram illustrating an embodiment of a stacked photovoltaic device module having an interconnect layer disposed between a thin semiconductor device layer and a handle substrate;

Figures 4A to 4F are schematic diagrams illustrating the steps of a process for forming the stacked photovoltaic device module of Figure 3;

Figure 5 is a schematic diagram illustrating some different forms of recesses or trenches that can be formed in the surface of a semiconductor;

Figures 6A to 6F are schematic diagrams illustrating the steps of various processes for forming pairs of trenches having doped sidewalls with opposite doping polarities;

Figure 7 is a schematic diagram illustrating a method for forming electrical connections to the doped sidewalls of a trench;

Figures 8A to 8I are schematic diagrams illustrating the processes for forming high aspect ratio lateral field *p-i-n* solar cell modules in accordance with some
5 embodiments of the present invention;

Figures 9A and 9B are schematic diagrams illustrating different forms of *p-i-n* solar cells that can be produced by thinning the semiconductor substrate to different final thicknesses;

Figure 10 is a graph of the projected range of hydrogen ions in silicon as a
10 function of ion energy;

Figure 11 includes schematic diagrams illustrating the formation of buried defective regions by implanting ions into mutually spaced trenches formed in a semiconductor substrate, where the trenches are relatively wide (upper diagram) or narrow (lower diagram);

15 Figure 12 is a schematic diagram illustrating the effects of changing the relative orientation between the implanting ion beam and the semiconductor substrate on the buried defective regions;

Figure 13 is a schematic diagram illustrating how the relative orientation between the implanting ion beam and the semiconductor substrate can be changed
20 during implantation to cause the buried defective regions to overlap and thereby form a continuous non-planar defective layer;

Figures 14 to 16 are schematic diagrams illustrating how a semiconductor substrate containing the continuous non-planar defective layer can be flip-chip bonded to a handle substrate, and then thermally processed to cause the semiconductor substrate
25 to split into two layers along the defective layer to provide a thin semiconductor layer bonded to the handle substrate;

Figure 17 is a flow diagram of a layer transfer or 'zip-cut' process for forming the structures shown in Figures 14 to 16;

Figure 18 is a schematic diagram illustrating a complete photovoltaic device
30 incorporating high aspect ratio lateral field photovoltaic cells bonded to an interconnect layer and a handle substrate, and having a non-planar photon receiving surface formed by the zip-cut process;

Figure 19 is a schematic diagram illustrating a modification of the embodiment of Figure 18 in which a second, wide band gap semiconductor is deposited on the non-planar surface formed by the zip-cut process;

Figure 20 is a schematic diagram illustrating the spatial arrangement of energy bands in the embodiment of Figure 19; and

Figure 21 is a schematic diagram illustrating the spatial arrangement of energy bands in a modification of the embodiment of Figure 19 in which the initial semiconductor layer is thinned down to the doped regions so that the second, wide band gap semiconductor is immediately adjacent the doped regions.

DETAILED DESCRIPTION

Figure 1 is a schematic diagram of a standard prior art photovoltaic device in which incident photons 102 must travel through a doped surface layer 104 before reaching a relatively narrow depletion (or 'space charge') region 106 in the form of a thin sheet, layer or plane that extends in directions that are orthogonal to the direction of photon travel. Consequently, only electron-hole pairs generated within the narrow depletion region 106 or within a diffusion length of its edges can be collected by the electric field in the depletion region 106 and thereby contribute to the device photocurrent. For convenience of reference, such devices are referred to here in as vertical field or vertical junction devices because the electric field is oriented vertically when the photon receiving surface is oriented horizontally, which is usually the case when such devices are used or represented.

In particular, high energy (short wavelength) photons present in sunlight are strongly absorbed in the doped surface layer 104 and cannot reach the depletion region 106 and hence do not contribute to the photocurrent. Furthermore, when photons are absorbed in the depletion region 106, in most cases at least one of the generated carrier types must traverse a relatively large distance before collection, which requires long carrier lifetimes.

In these conventional devices, the large excess energy ($\Delta E_{th} = E_{\gamma} - E_G > 0$) of the hot carriers generated near the surface of the doped surface layer 104 is quickly thermalized

via interaction with lattice phonons and converted into heat before the carriers can traverse the relatively large distances (≥100 μm) to be collected, thereby increasing the cell temperature T_O and phase space filling available states. Consequently, the most efficient photons for photocurrent generation in vertical junction devices are those with energies at or in the immediate vicinity above the fundamental band gap E_G. Such losses have the cumulative effect of reducing the useful energy bandwidth of the solar spectrum above E_G that can be converted into useful charge carriers. That is, the high energy photon energy loss processes in vertical junction device topologies limits the useful solar energy bandwidth to only a small region above E_G, leaving the high energy portion of the solar spectrum unutilized.

Recently, a new form of semiconductor junction device has been developed in which the standard configuration shown in Figure 1A is turned on its side so that incident photons 102 travel *along* the depletion region 202, as shown in Figure 2, rather than across it. Consequently, a greater portion of the electron-hole pairs generated within the semiconductor body are generated within the depletion region 202 than would otherwise be the case, and can thus be collected. Moreover, by configuring the device so that the depletion region 202 extends to the surface 204 of the semiconductor body as shown in Figure 2 (or at least substantially to the surface 204), the efficiency of the device is even further enhanced. This enhancement is due not only to the resulting increase in the photon path length within the depletion region 202, but also to the fact that high energy (*i.e.*, short wavelength) photons are very strongly absorbed in the semiconductor body, as described above, thus generating electron-hole pairs (EHP) within the depletion region 202 with an exponentially and rapidly decaying generation rate 206 with distance *z* 208 from the surface 204, as shown by the graph in the right hand side of Figure 2. By arranging for the depletion region 202 to extend to the surface 204 (or at least very close to the surface 204), most if not all of these EHPs can be collected, whereas they would otherwise be largely or completely lost to energy conversion. Thus this configuration allows nearly all of the EHPs generated in the depletion region 202 to be collected. As will be appreciated by those skilled in the art, in addition to the EHPs formed within the depletion region 202, electrons or holes generated within the doped regions 210, 212, but also within the relevant diffusion

length of the corresponding edge of the depletion region 202 can diffuse to the depletion region 202 and be swept across the depletion region 202 by the electric field, thereby contributing to the device photocurrent.

5 Because the electric fields in the depletion regions of such devices are orthogonal to the direction of travel of the incident photons 102, such devices are referred to herein as lateral field or lateral junction devices.

Although only one lateral *pn* junction is shown in Figure 2 for the sake of clarity, in 10 practice a large array of such devices are formed in a single semiconductor wafer or thin film and interconnected to form a single device. This allows a far greater proportion of the semiconductor wafer to be used to form the depletion or space charge regions than would be the case for vertical field devices, where the depletion region is limited to a narrow buried band. By densely packing the lateral field devices, a majority 15 of the wafer or thin film can be used as active regions from which EHPs are collected. It will be apparent that the overall efficiency of the device is generally increased by forming the doped regions 210, 212 to be deep (to extend the space charge regions deeper into the semiconductor, and thereby capture more EHPs along the paths of the photons 1210) but narrow (to reduce or eliminate the proportion of EHPs created within 20 the doped regions 210, 212 and further than a diffusion length from the corresponding edge of the depletion region 202). For example, a series of parallel narrow sheets of doped semiconductor arranged vertically (*i.e.*, as stripes in plan view) can be formed in a semiconductor wafer using standard lithography and masked ion implantation, as will be apparent to those skilled in the art.

25

Although the lateral field structures described above allow the efficient collection of EHPs generated by photons with a wide range of wavelengths, in practice the width L_D 214 of the *p-n* junction depletion region 202 is limited to being about 1 μm or less, which limits the overall efficiency of the device.

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To improve the efficiency of these lateral field devices, an intrinsic or at least not intentionally doped (NID) region of relatively high resistivity is disposed between the

p-type 210 and *n*-type 212 doped regions to provide a lateral *p-i-n* photovoltaic device where the width L_D 214 of the space charge region for generating/collecting EHPs is substantially increased over the *p-n* lateral field device 200 described above, thus providing increased efficiency. In the context of the lateral field devices described herein, the terms "intrinsic region" and "NID region" refer to a region that is either undoped or is lightly doped relative to the p-type and n-type doped regions disposed on either side such that the doped regions establish an electric field across the intrinsic region to form a *p-i-n* diode structure or equivalent thereof. As described below, although the "intrinsic region" in such a structure is nominally undoped, or background doped only, in some cases it may be desirable to lightly dope the "intrinsic region" to increase carrier mobility and lifetime therein. Indeed, the p-i-n device can have an almost arbitrarily large "intrinsic" region, which enables the simultaneous optimization of optical absorption and EHP carrier extraction.

Further details of lateral field devices are provided in the lateral field device patent application.

Thin film semiconductor photovoltaic devices with interconnect and handle layers

Figure 3 is a schematic illustration of a cross-section of a portion of a high efficiency photovoltaic (PV) module in accordance with some embodiments of the present invention. The module includes (i) a handle substrate 3001, with through-vias and solder bumps 3005, (ii) an interconnect stack 3002, and (iii) a thin film semiconductor active layer 3003, with doping 3006 indicated schematically, and surface coatings 3004. It should be understood that Figure 3 provides only a simplified high level schematic view of the module for the purposes of explaining the roles of the handle substrate 3001, interconnect stack 3002, and semiconductor active layer 3003. For the sake of clarity, details of these three components in an actual module are not shown. In the description below, general methods for forming the three components and forming the resulting three-component stack are first described at a high level. Then, methods for forming lateral field devices within the semiconductor active layer 3003 are described, and finally, methods for forming a complete module are described.

The handle substrate 3001 provides mechanical support for the photovoltaic device; it can facilitate thermal management, and it can allow additional circuitry to be integrated with the photovoltaic device. Such circuitry can perform power conditioning functions and can transform the DC power generated by the photovoltaic device into AC power.
5 The handle substrate 3001 may be composed of any suitable material. Metal handles are used in concentrating photovoltaic systems in order to act as heat sinks. Glass handles are used in flat plate photovoltaic systems in order to reduce cost. Silicon (or other semiconductor) handles are used when it is advantageous to integrate electronic circuitry, such as power conditioning circuits, with the handle. Alternatively, silicon-on-
10 sapphire (SOS) handles can be used when it is advantageous for the integrated electronic circuitry to be radiation hard. Electrically insulating handles can also be used to integrate electronic circuitry with the device by providing conducting paths on the insulator to connect the semiconductor active layer 3003 with at least one separate die containing the electronic circuitry. The separate die may be flip chip bonded to the
15 insulating handle, which may be optically transparent.

The interconnect stack 3002 consists of one or more layers of conductors 3007 in a dielectric medium 3008. The conductors can be any low resistance material, including aluminium, copper or sp^2-bonded carbon. The dielectric medium 3008 can be any
20 compatible insulating material, including silicon dioxide, carbon-doped silicon dioxide or sp^3-bonded carbon. A good thermal conductor is typically used. The conductors 3007 interconnect the junction devices in the semiconductor active layer 3003 and also provide connections to external power lines. The connections to external power lines can be through vias 3005 formed in the handle substrate 3001, or by running the
25 conductors to the edge of the interconnect stack 3002 to provide electrical contacts, as shown.

The semiconductor active layer 3003 includes arrays of solar cell devices, which are not shown for the sake of clarity. In the described embodiments, these are lateral field *p-i-n*
30 solar cell devices as described above. However, a wide variety of different junction architectures are possible. Examples of additional device structures that are compatible

with the overall solar cell architecture described herein are described in US Patent Application Nos. 61/214,305 and 61/218,862.

The passivation layer 3004 consists of layers of coatings that act to passivate and
5 protect the semiconductor surface and to trap light within the semiconductor. Techniques for forming these layers are well known in the art.

Figure 4 illustrates a method for forming ultra-thin single crystal photovoltaic devices such as that shown in Figure 3. Not shown or described are standard steps known to
10 those skilled in the art for preparing a substrate for semiconductor processing, including cleaning and stripping steps.

In Step 4000, the process starts with a single crystal semiconductor substrate 3003 or alternatively a thin-film semiconductor-on-insulator (SOI) substrate. The single crystal
15 semiconductor substrate can be a conventional bulk, single-crystal silicon wafer. It can be of any available thickness, but is typically in the range of 400 to 600 microns. In embodiments where a thin-film SOI substrate is used rather than a bulk substrate, the thin-film SOI substrate can be an SOI wafer formed using any available and known process, including SIMOX processes and bonded wafer SOI processes known to those
20 skilled in the art. The silicon layer on a SOI wafer should be approximately equal to the desired thickness of the final silicon layer 3003 in the device, as described further below.

In Step 4001, n- and p-type impurities are introduced into selected regions 3006 of the
25 single crystal semiconductor using standard patterning and doping techniques well known in the art. It should be understood that the doped regions are represented schematically as regions 3006 in Figures 3 and 4 for the sake of simplicity, and further details of actual doping structures formed within the semiconductor are described below.

30

The impurities may be introduced by many techniques well known in the art. For example, impurities may diffuse into the semiconductor from a solid source deposited

on the surface of the semiconductor. For example, the n-type dopant phosphorus may be introduced by depositing a layer of phosphorus-doped silica glass (PSG) on the semiconductor surface. The impurities diffuse from the source into the semiconductor upon thermal processing. Typically, boron is used for the p-type dopant and phosphorus is used for the n-type dopant. The boron may be introduced before the phosphorus because boron is less mobile than phosphorus and therefore will not diffuse as significantly under further thermal processing. Patterned areas of dopant introduction can be obtained using techniques well known to one skilled in the art, such as depositing and selectively removing a barrier material, such as silicon nitride or undoped silicon dioxide, to allow dopant penetration only where desired.

In an alternative process not shown in the Figure, impurities are introduced through recesses or trenches formed in the surface of the semiconductor, as described further below.

In Step 4002, the interconnect stack 3002 is formed on the semiconductor substrate 3003 using conventional semiconductor processing techniques, although it will be apparent to those skilled in the art that the interconnect stack 3002 can alternatively be formed on the handle substrate 3001. The conductors 3007 can be formed of aluminium doped with copper and silicon in order to reduce electro-migration, and the dielectric 3008 can be formed of silicon dioxide, possibly doped with impurities such as carbon. For example, the dielectric can be formed from silicon dioxide glasses that are deposited by PECVD, spun onto the exposed surface, or applied using other well known techniques. The aluminium can be deposited using PVD and the deposited layer can be planarized using CMP, although sufficient planarity can often by achieved without the use of CMP. The aluminium layer can be patterned into wires by using conventional optical photolithography. Alternatively, the conductors can be formed of copper or conductive carbon in order to further reduce electromigration. Alternatively, the dielectric medium 3008 can be of an insulating material that is thermally conductive.

Upon the completion of Step 4002, a complete photovoltaic device has been formed.

In Step 4003, the completed photovoltaic device of Figure 4-B is bonded to the handle substrate 3001. Techniques for bonding two substrates are well-known in the art. In some embodiments, the exposed surface of the interconnect stack is planarised and bonded to an activated surface or layer disposed upon the handle substrate. In some embodiments, plasma nitridation of a silicon oxide layer is used to increase the bond energy between the two surfaces. In some embodiments, the substrates are bonded by fusion bonding, involving a first wafer bonding step and an optional second bond strengthening step. Prior to bonding, the surfaces to be bonded are cleaned so that they are sufficiently free of particles and are sufficiently flat to enable wafer fusion bonding to occur.

In some embodiments, the surfaces of the respective substrates further undergo one or more optional surface activation steps, such as chemical treatment or deposition of one or more layers, or physical treatment to improve the chemical bonding strength. As known by those skilled in the art, the surface energy (E_{surf}) depends on the chemical state of the surfaces and is typically around E_{surf}=0.1 J/m^2 for hydrogen bridge–bonded hydrophilic silicon surfaces including a thin silicon oxide and one or two monolayers of water. Alternatively, a hydrogen covered/terminated silicon surface exhibits a surface energy E_{surf}~0.02 J/m^2, involving a hydrophobic surface that results from a hydrofluoric acid wash to remove the native oxide from the underlying silicon.

Next, the substrates are aligned so that the surfaces to be bonded are substantially parallel, and localized pressure is then applied substantially at the center of the two articles to be bonded. This initiating localized pressure is typically applied to an external surface of one substrate while the other substrate is fixed, using a wafer bonding system such as those manufactured by the Electronic Visions Group and described at http://www.evgroup.com/en/products/bonding/waferbonding/. The bonding wavefront expands radially outward toward the periphery of the substrates and forms a first wafer bond. Alternatively, the bond may be initiated at the edge of the substrates aligned appropriately to form an initial wedge with bonding wavefront expanding to

close the gap between the two substrates. In some embodiments, the first bonding step is performed under vacuum.

After this initial bonding step, the strength of the bonds holding the two substrates
5 together via a first wafer bond can be strengthened via heating to a temperature of about 100-1000 °C, depending upon the materials utilized, and for a period of time ranging from 1 minute to several hours. Alternatively, laser assisted bonding can be utilized, wherein optical radiation is utilized to impart thermal energy or activate a chemical process that improves the bond strength of the surfaces. Optionally, localized or
10 substantially uniform bonding can be utilized via laser assisted bonding. For example, solders can be melted in specific regions such as interconnect paths between the active substrate and the handle. The general method of local bonding regions between the two articles can be used to manage stress. In other embodiments, semiconductor glues or waxes are be used to bond the two substrates together.
15

After the handle wafer or substrate 3001 has been bonded to the interconnect stack 3002, the semiconductor or SOI wafer is thinned from the backside in step 4004. For a bulk, single-crystal semiconductor wafer, backside removal is typically performed by a combination of grinding, polishing, and chemical etching, but other methods known in
20 the art may alternatively be used. The surface remaining after thinning does not need to be smooth. Indeed, a rough final surface can enhance the light-trapping capabilities of the device. In embodiments where the initial substrate at step 4000 is an SOI substrate with a thin oxide layer disposed between a thin silicon device layer and a supporting substrate layer, the substrate layer can be removed by a wet etch, with the oxide layer
25 acting as an etch-stop.

In Step 4005, contacts 3005 are made to the conductors in the interconnect stack of the solar cell device. In some embodiments, these are formed through the handle wafer (*e.g.*, by etching or by laser or ion beam machining) as shown in Figure 4-E, or by
30 running metal interconnects to the edge of the solar cell. In some embodiments, the contacts are formed in the handle prior to bonding.

In Step 4006, passivating, anti-reflective and protective coatings 3004 are formed on the exposed silicon surface, as described in the lateral field device patent application and/or using standard methods known to those skilled in the art.

5 **High aspect ratio photovoltaic devices**

As with standard semiconductor photovoltaic devices, the lateral field devices described above are formed by the selective introduction of dopant impurities, such as boron and phosphorus, into the semiconductor lattice. These impurities can be introduced using conventional semiconductor processing techniques, including implantation and 10 diffusion into the planar surface of a silicon wafer. However, these techniques are limited in their ability to form deep, high aspect ratio doped regions. The methods described below overcome these limitations by introducing the impurities through physical features or recesses etched into the surface of the semiconductor.

15 Figure 5 depicts various types of physical features that can be formed by using different methods for etching bulk single crystal semiconductors 5014. High aspect ratio features 5010, 5013 and 5015 can be produced via many techniques, including dry etching (e.g., the Bosch method, advanced silicon etch methods, and through silicon deep via technologies), laser micromachining and undercutting beneath a mask. Mask layers 20 5011 and 5012 are typically silicon-nitride and silicon oxide, respectively, although other materials may be used.

Figure 6 depicts several methods that can be used to form impurity doped regions through trenches etched into a semiconductor, including solid-phase diffusion (Figures 25 6a and 6b), ion implantation (Figures 6c and 6d), and a combination of solid-phase diffusion and ion implantation (Figures 6e and 6f).

In some embodiments, as shown in Figures 6a and 6b, impurities are introduced via diffusion from solid-phase materials deposited in the trenches, with an n-type impurity 30 source in trenches that are desired to be n-doped 6011 and a p-type impurity source in trenches that are desired to be p-type 6021. In some embodiments, the trenches that are to be doped n-type are first filled with the n-type dopant source material, and then the

trenches that are to be doped p-type are etched and filled with the p-type dopant source material. In some embodiments, all of the trenches are formed in a single etch step, with photo-resist used to selectively deposit impurity source material in the desired trenches. In any of these embodiments, once the impurity source material has been deposited, 5 thermal processing drives the impurities into the semiconductor, causing the trench sidewalls and bottoms to be selectively doped n-type 6012 or p-type 6022, as appropriate. If the dopant source material is poly-silicon deposited in a silicon substrate, then the polysilicon can be left in place and will partially crystallize during thermal processing. Alternatively, if the source material is a silica glass, the glass can be 10 removed with an HF wet etch and the trenches can then be filled with a conductive material.

Alternatively, as shown in Figures 6c and 6d, in other embodiments impurities are introduced by implantation. n- and p-type trenches are formed by the use of photo-resist 15 to select the trenches to be doped with the different species. To implant the sidewalls of the trenches, the ion implantation is performed at different angles, as represented schematically by the arrows in these Figures.

Alternatively, as shown in Figures 6e and 6f, in yet other embodiments the trenches are 20 selectively doped by a combination of diffusion from a solid source and ion implantation. This method has the advantage of using a single polysilicon deposition to fill both types of trench and to provide the doping for one type.

Figure 7 depicts a method for solid-phase doping through trenches, in which successive 25 (or alternative in some cases) processing steps are illustrated as adjacent trenches proceeding from left to right in each part of the Figure. Although the trenches are represented in Figure 7 as having substantially rectangular cross-sections, in practice the trenches may have rather different shapes. As shown at step 7001, an etched trench (left-hand trench of 7001) is filled with an impurity-containing glass 7050 capable of 30 diffusing a high concentration (10^{15}-10^{20} cm^{-3}) of a specified dopant species into the semiconductor layer. The wafer is annealed (center trench of 7001), driving impurities into the semiconductor. The doped glass 7050 is then stripped from all surfaces to

reveal a trench 7052 (right-hand trench of 7001) with doped sidewalls and bottoms. As shown at 7002, the diffused regions 7051 can be electrically contacted by complete 7053 or partial 7054 coverage and filling of the trench 7052 with metallic or semiconducting layers, such as poly-silicon. A deposited poly-silicon layer 7054 can be subsequently implanted to achieve a high dopant concentration, or can be deposited as an *in situ*-doped polysilicon layer. Alternatively, a contact layer such as Ti/TiN can be directly deposited forming a liner 7055, as shown in the right-hand trench of 7002. A low resistance electrode 7056 is then formed to contact the doped region. Lateral isolation can be achieved using a highly conformal chemical vapor deposition (CVD) of TEOS-oxide (not shown), with trench/via/plug metallization formed by MOCVD of tungsten, and with optional MOCVD-TiN as a barrier layer. Etch-back for metal plug formation is performed via dry etch or chemical mechanical polish (CMP). The lateral electrical connection of, for example, tungsten-filled trenches with an uppermost metal level of the device can be performed by standard Al metallization.

In some embodiments of the present invention, high aspect ratio, lateral field *p-i-n* photovoltaic devices are formed with doped regions extending deep into the interior of a bulk or thin-film semiconductor. Figure 8 shows the process flow for producing these devices in thin film, single-crystal silicon. However, it will be understood by those skilled in the art that these devices can be formed in other semiconductors, which may be in bulk or in thin-film form, including, for example, amorphous silicon (a-Si), cadmium telluride CdTe, copper-indium-gallium-sulfur-selenide (CIGS), gallium-indium-nitride (GaInN), and gallium arsenide (GaAs), to name but a few well-known semiconductors.

In Step 8001, a PADOX/nitride, comprising a thermally-grown silicon oxide layer 8112 and an overlying silicon nitride layer 8111, is formed on the surface of a prepared, clean single crystal silicon substrate 8114. During growth of the oxide 8112, the backside of the substrate 8104 may also be exposed to form an oxide layer 8100 on the backside of the substrate 8104.

In Step 8002, a set of mutually spaced high-aspect ratio trenches or features 8200 are formed in the substrate 8104, extending from the substrate surface to a depth D_1 below the surface. In the described embodiments, the depth D_1 depends on the final thickness of the silicon layer. In practice, trenches extending 60-80% into the final silicon layer have been found to provide good collection efficiency without punching through to the underlying oxide. For example, in embodiments where the final silicon layer thickness is selected to be about 5, 10, or 20 µm, the trench depth D_1 is selected to be about 4, 8, and 16 µm, respectively. The term "aspect ratio" when applied to a feature such as a trench or recess refers to the ratio of the depth of the feature to its width. In this specification, the term "high aspect ratio" refers to an aspect ratio greater than 1:1 (*i.e.*, the feature is deeper than it is wide), and typically greater than 2:1. Standard silicon dry etch tools and processes available today can form trenches with aspect ratios as high as 40:1, although this is generally limited by factors such as feature width, spacing between features, and the like.

In Step 8003, a doped layer 8201 is deposited on the entire front side of the patterned substrate. The doped layer 8201 can be a doped glass, polysilicon or other impurity-carrying material capable of altering the conductivity type of the semiconductor. Typically, the deposited layer 8201 is a phosphorous doped silicon oxide (PSO) deposited by plasma-enhanced chemical vapour deposition (PECVD).

In some embodiments, the thickness of the doped layer 8201 is selected to form a conformal coating lining the bases and sidewalls of the trenches 8200, as shown in Figure 8A, and at step 8004, a not-intentionally-doped silicon oxide (NSO) 8102 is deposited to fill the trenches 8200 and serve as a diffusion barrier and protective cap, also as shown in Figure 8A.

However, in other embodiments, as described in the following steps and as shown in the following Figures, the diffusion barrier layer 8102 is omitted, and the doped layer 8201 is deposited to fill the trenches 8200, as shown in Figure 8B (refer step 8005, for example). In Step 8005, a second set of high aspect ratio trenches 8300 interleaved with the first set 8200 is formed, extending deep into the interior of the substrate 8014. In the

embodiment shown in Figure 8B, the depth D_2 of the second set of trenches 8300 is equal to the depth D_1 of the first set of trenches 8200. However, in other embodiments, the second set of trenches may be deeper than, or shallower than, the first set of trenches 8200, as described further below.

5

In Step 8006, a doped layer 8301 capable of inducing the opposite conductivity type is disposed across the entire substrate surface, forming plugs 8302 that substantially fill the trenches 8300 with material that will induce conductivity of the opposite type of the preceding doped layer 8201. Typically, the material 8301 is boron-doped silicon oxide

10 (BSO). When used as the plugs 8202 and 8302, respectively, PSO and BSO are capable of diffusing phosphorus and boron impurities into the immediately surrounding silicon, with well defined penetration depth into the sidewalls and base of each trench.

In Step 8008, during thermal treatment, dopant impurities diffuse in all directions from

15 the filled trenches 8202 and 8302. Regions 8203 and 8303 formed after diffusion and activation annealing are thus composed of n-type phosphorus doped silicon (P:Si) and p-type boron-doped silicon (B:Si), respectively. The penetration depth and concentration of diffused species is controlled by: (i) the doping density in the initial doping layer deposited; (ii) the impurity species and its diffusivity in Si; (iii) the quality

20 of the doping layer/silicon interface; (iv) the diffusion vector relative to the Si crystallographic directions; (v) the temperature and thermal budget of the activation step; and (vi) point defect concentrations in the regions 8203 and 8303 during thermal processing.

25 Step 8009 shows the depleted doped-glasses 8200 and 8300 removed and stripped from the surface, where the (typically silicon nitride) barrier layer 8111 prevents the oxide 8112 from being removed.

In optional Steps 8010 and 8011, the initial PADOX/nitride layers 8111, 8112 can be

30 optionally removed and one or more high quality insulating dielectric layers 8120, 8121 formed as shown. Typically, two layers are formed: a first layer 8120 of high quality, low-trapped charge silicon-oxide, and a second, overlying layer 8121 of a not-

intentionally doped glass or an electrically insulating dielectric suitable for use with an electrical interconnect.

Irrespective of whether optional steps 8010 an 8011 are included in the process, in step
5 8012, a uniform metal contact layer 8123 is deposited and patterned to electrically isolate regions of opposite conductivity-type 8203 and 8303. Typically, this layer 8123 is composed of Ti or TiN, although other high quality contact materials can be alternatively used.

10 In step 8013, high conductivity electrical interconnect metal or alloy is deposited and patterned to produce low resistance Ohmic contacts 8125 and 8126 to the doped silicon regions 8203 and 8303, respectively. In the described embodiments, these electrical interconnect and doped regions are patterned to produce densely packed lateral field p-i-n devices using an inter-digitated electrode topology, as described in US Patent
15 Application Nos. 61/214,305 and 61/218,862. However, other electrode configurations can be used in other embodiments.

In step 8014, the electrodes 8125 and 8126 are encapsulated within an insulating dielectric material 8127 to produce the completed silicon device wafer 8130.

20

Although the p-type and n-type trenches have the same depth and aspect ratio in the embodiments described above, this need not be the case in other embodiments, as in the embodiments 8015 and 8016 shown in Figure 8F, which can provide improved operation where substantially different carrier mobilities and/or carrier lifetimes in the
25 semiconductor material of the substrate. For example, in the embodiment 8106 shown in the lower half of Figure 8F, another conductivity type layer 8162 is formed on the opposite face (*i.e.*, the backside) of the substrate to provide a region that is electrically connected to the doped regions 8161 having the same conductivity type. The resulting structure 8016 is a hybrid photovoltaic device capable of producing substantially high
30 conversion efficiency by utilizing a majority of the bulk semiconductor volume.

Returning to the process flow, in step 8017, the completed single crystal silicon devices are wafer bonded to a low cost electrical interconnect backplane, as shown in Figure 8G. The backplane comprises an insulating substrate 8173, an insulating dielectric 8172, electrical contacts 8171, and an electrical joining compound 8170. Compound 8170 may comprise solder or paste, enabling high integrity and uniform electrical interconnection between the processed silicon device substrate and the backplane. The resulting bonded article is shown in step 8018. The major benefit of this arrangement is the ability to produce a large array of processed silicon wafers that can be wafer bonded to a single large planar backplane. This enables large scale processing for subsequent steps such as silicon wafer thinning and optical coatings such as silicon-nitride, aluminium oxide, diamond or other protective coatings. Multiplex bonding of processed articles 8130 onto a single large area backplane is shown in steps 8019 and 8020 of Figure 8H.

Steps 8021 and 8022 depict one method of forming a thin film of single crystal silicon containing processed electrical devices and coupled to a handle substrate or backplane, where the bonding compound has been omitted for clarity. A relatively thick bulk silicon substrate 8180 is used for the initial CMOS style device processing, as shown in step 8021, followed by etching and/or grinding of a majority of the backside silicon surface to a depth X 8185. Optionally, an annular (or other peripheral shaped) portion 8182 of the bulk silicon substrate of width 8181 can be exempt from removal to provide a mechanically robust support for the device layer. If the handle layer 8173 is subsequently removed, the integrity and ease of handling the thinned device layer can be achieved by way of this annular portion 8182. A protective coating and or passivation layer 8184 can be deposited on the etched portion of the substrate, as shown in step 8022.

In some alternative embodiments, ion implantation is used to introduce impurity species into the semiconductor trench sidewalls and bases as an alternative to doped glasses, allowing the number of manufacturing steps to be reduced. Furthermore, when ion implantation is used, there is no need to remove glass from the deep trenches, which can be relatively difficult in very deep trenches with high aspect ratios.

Figure 9 shows the doped trenches created in the previous process after wafer thinning. Figure 9a shows the wafer thinned to the depth of the doped trench bases, with a surface passivation/anti-reflection coating (which may be provided by residual oxide if the semiconductor layer was originally part of an SOI wafer) on the photon-receiving surface of the semiconductor. This configuration provides a lateral electric field extending all the way to the silicon photon receiving surface. Figure 9b shows the wafer thinned to a smaller depth so as to leave some undoped silicon between the silicon surface the doped trench base regions. This provides 100% active photon collection area at the surface, at the expense of reduced electric field strength at the silicon surface.

Layer Transfer of Photovoltaic Devices

Optoelectronic, photovoltaic and/or electronic devices can attain higher performance in thin, single crystal silicon than in bulk, single crystal silicon. Thin, single crystal silicon SOI substrates are typically formed by bonding a silicon wafer to a support substrate and then thinning the bulk, single-crystal silicon wafer by etching, grinding and polishing, a process referred to in the art as bond and etch-back SOI, or BESOI. These conventional wafer thinning processes are slow, expensive and typically waste all of the silicon removed from the substrate. As described in M. Bruel *et. al.*, *Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding*, Jpn. J. Appl. Phys. 36 (1997) pp. 1636-1641, an alternative type of layer transfer process referred to as 'smart cut' has been developed in which light ions such as hydrogen and/or helium are implanted into a planar semiconductor wafer to form a buried defective layer that, when heated, forms a fracture zone, allowing the overlying semiconductor to be split apart from the remaining bulk silicon substrate. The latter can then be reclaimed and used repeatedly to form many such semiconductor thin films.

Described herein is a modification of the smart-cut process, in which ion implantation into the high aspect-ratio trench or recess features formed in the semiconductor surface and typically extending 0.1 to 100um into the semiconductor crystal is used to form a non-planar fracture zone that allows the top-most layer to be removed without

significant "kerf" loss. The resulting non-planar surface has desirable optical properties, as described below.

Relatively high energy implantation may be required to form a fracture zone deep
5 within the semiconductor. For example, Figure 10 shows the depth of the peak of the depth distribution of hydrogen ions (H+) beneath a bulk Si surface as a function of the hydrogen implant energy. An energy of greater than 100keV is required to form a peak ion distribution ~1 micron beneath the surface. An energy approaching 1MeV is required to form a peak 10 microns or deeper in the silicon.
10

Figures 11-16 illustrate the steps of the layer transfer process described herein. Figure 11 shows the implantation of H+ ions or other light ions (e.g., He, B or P) 3100 into patterned semiconductor substrates 3101, 3102 with features 3103, 3104 such as trenches of different widths formed in the respective substrates 3101, 3102. Protective
15 and implant mask layers 3105 and 3106 enable implanted species 3100 to penetrate into only the exposed portions of the substrates 3102, 3103, being limited to the trenches themselves in these embodiments 3001, 3002. The implanted species form defective regions 3108 and 3109. If the trenches or recessed features in the semiconductor surface are wider laterally (for example, as in the wider trenches 3103 in the upper embodiment
20 3101 of Figure 11), the implanted regions 3103 are commensurately wider than the regions 3109 and are substantially parallel to the remaining surface of the substrate 3101. However, if the substrate 3102 and ion beam 3100 are not mutually orthogonal but are inclined at an angle 3110 or 3111, then implanted regions 3112 and 3113 are formed that extend substantially beneath the protective cap layers 3105 and 3106.
25

If many such angles are used during implantation, or if the angle is substantially continuously varied so as to produce features 3114 and 3115 as shown in Figure 13, then defective regions can be induced to enable continuous layer separation of an active device layer from the bulk substrate. Steps 3005 and 3006 of Figure 13 show the effect
30 of increasing the angle of the trenches/substrate relative to the implant beam while keeping the lateral trench width constant.

The upper part of Figure 14 shows 3007 a silicon wafer with trenches 3120 following masked and angle-varied H+ implantation as described above to form a buried non-planar defective region 3122. The lower part of the Figure shows 3008 the wafer flip-bonded (*i.e.*, face down) onto a handle substrate 3123. As shown in Figure 15, thermal activation 3131 of the H+ implanted regions 3122 generates volume expansion of region 3122, producing a net force 3128 that separates the device layer 3126 from the remaining bulk substrate 3127. Due to the multi-angle implantation through the trenches, the separated surfaces 3129 are highly non-planar and may also exhibit roughness on a smaller length scale both of these non-planarities being advantageous for light scattering and light-trapping.

The layer transfer process described herein is referred to herein as the 'zip-cut' process, and can be represented by the flow diagram of Figure 17. First, a bulk silicon substrate is prepared using a standard cleaning process at step 1702 and then patterned at step 1704 using a standard lithography process. At step 1706, a standard subtractive process (*e.g.*, deep reactive ion etching) is applied to the patterned surface to form recessed features (*e.g.*, trenches), typically deep and/or high aspect ratio features, in the surface of the substrate. At step 1708, one or more light ion species capable of forming a buried fracture zone are then implanted into the recessed features at a plurality of different angles (*i.e.*, relative orientations) to produce a buried non-planar defect region due to the implantation angles and the shape or shapes of the recessed features. In order to ensure that the buried defect region is continuous or substantially continuous, in the described embodiments the ion implantation involves implantation at multiple energies and/or multiple implant species (in addition to the multiple implant angles). In some embodiments, a single ion species is implanted at two different energies; in other embodiments, two different ion species (*e.g.*, H and He ions) are implanted at either the same or different energies.

At step 1710, microelectronic devices are fabricated between the trenches using substantially standard MEMS and CMOS style processes, modified so that the thermal budget avoids premature layer separation. At step 1712, the top surface of the substrate is bonded to a low-cost handle substrate or backplane using a standard bonding process.

The bonding process can include fusion or anodic wafer bonding, or adhesive bonding. or other standard bonding processes known to those skilled in the art. At step 1714, the bonded pair is thermally processed to cause the defective region to form a continuous fracture zone so that the bulk silicon substrate splits into two portions, comprising the
5 thin layer (containing the devices) bonded to the handle backplane, and the bulk silicon below the fracture zone. The first of these provides the completed device wafer 1716, and the remaining portion of the bulk silicon substrate can be polished and reused at step 1718. The use of H+ ions for the implantation step 1708 provides the additional advantage of passivating defects in the active layer.
10

Figure 18 is a schematic illustration of an embodiment combining the zip-cut layer transfer process with the embodiment of step 8018 or 8021, incorporating high aspect ratio lateral field p-i-n photovoltaic devices and bonded interconnect backplane. Incident solar radiation 1802 enters the active region semiconductor 1804 through an
15 antireflection coating 1806 reducing reflected optical energy 1808 formed on the non-planar surface formed by the Zip-Cut interface. Laterally disposed high aspect ratio p-type 1810 and n-type 1812 regions collect photo-generated electrons and holes. Unabsorbed light 1814 is reflected from the backside metalized contacts 1816, metal electrodes 1818, and dielectric layers comprising the electrically insulating materials in
20 the interconnect stack. The regular pattern of in-plane and out-of-plane dielectric regions and metal contacts can also be used to form high efficiency reflective and diffractive function to aid in the light-trapping of solar radiation in the active semiconductor layer 1804, as described in US Patent Application Nos. 61/214,305 and 61/218,862.
25

In an alternative embodiment, as shown in Figure 19, a second semiconductor layer 1902 is formed over a first semiconductor layer 1904, where the first and second layers 1902, 1904 have respective band gap energies $E_{G1} < E_{G2}$ incident solar radiation 1906 enters the second active semiconductor layer 1902 through an antireflection coating
30 1908. Incident high energy photons with $E\gamma \geq E_{G2}$ are preferentially absorbed in the second semiconductor layer 1902, whereas most lower energy photon $E < E_{G2}$ will pass through this layer 1902 to the underlying first semiconductor layer 1904. Low energy

photons $E_{G2} > E\gamma \geq E_{G1}$ are preferentially absorbed in the first semiconductor layer 1904. Lateral field, high aspect ratio p-type 1910 and n-type 1912 regions collect photo-generated electrons and holes. As with the embodiment described above, unabsorbed light is reflected from backside metalized contacts 1914, metal electrodes 1916 and
5 dielectric layers comprising the electrically insulating materials in the interconnect stack. The regular pattern of in-plane and out-of-plane dielectric regions and metal contacts form high efficiency reflective and diffractive structures to aid in the trapping of solar radiation in the active semiconductor layers 1902, 1904. The interconnect stack can be bound to a handle substrate 1918. The handle can be of any suitable material,
10 including, metal, glass or silicon. Photo-generated carriers collected from the active region are conducted to external power circuitry via interconnects that run to the edge of the module or through the handle.

In the described embodiments, silicon is used as the first semiconductor 1904 and a
15 wide band-gap material is used as the second semiconductor 1902. Amorphous silicon or microcrystalline silicon can be used as the wide band-gap material. Techniques for depositing films of amorphous silicon and microcrystalline silicon are well-known in the art and include techniques based on plasma-enhanced CVD. Compound semiconductors, such as indium-aluminium-gallium-nitride (InAlGaN), gallium
20 phosphide (GaP), cadmium telluride (CdTe), compounds of cadmium telluride (CdZnTe or CdSSe) and copper-indium-gallium-sulphur-selenide (CIGS), can also be used as the wide band-gap materials. Techniques for depositing or growing these films are well-known in the art and include MOCVD, MBE and other epitaxial growth techniques. Vicinal surface orientations of silicon such as (111)- and (211)-orientations
25 favor the high quality epitaxy of CdTe and or CdZnTe and or CdSSe compositions. Copper-indium-gallium-sulphur-sellenide (CIGS) may also be utilized with the advantage of requiring only a high quality intrinsic epilayer upon a silicon backplane. Gallium phosphide (GaP) can also be used, as it possesses a larger band gap than silicon and it has very low lattice mismatch with crystalline silicon. Although GaP is an
30 indirect bandgap semiconductor, as known to those skilled in the art, it can be engineered to exhibit favourable absorption properties for solar cell operation. For

example, high doping levels can enhance the higher energy absorption due to phase space filling effects at the lowest lying indirect valley.

Figure 20 is a schematic diagram representing the spatial arrangement of energy bands
5 associated with the impurity doped regions 1910, 1912 of the first semiconductor 1904, the second, wide bandgap semiconductor 1902, and the sealing layer 1908. Doped regions 1910 are n-type and regions 1912 are p-type. The not-intentionally-doped (NID) regions between the doped regions 1910, 1912 have substantially the same carrier concentration as the initial semiconductor prior to processing. The resulting modulation
10 doping of the lateral field *p-i-n* structure along the x-direction 2001 acts to separate electrons and holes. Hot electron 2002 and hole 2004 pairs photo-created by direct absorption of high energy incident photons 2006 can drift and diffuse laterally along the surface or be transported across the heterojunction formed between the first and second semiconductors 1904, 1904. By appropriate choice of these semiconductors, the
15 heterojunction can have a large conduction or valence band offset. For example, a hot electron 2008 experiences a large energy step upon being transported along a vector substantially parallel to the Z-direction 2010 and toward the first semiconductor 1904 and is efficiently collected by the *p-i-n* devices.

20 Figure 21 illustrates an alternative embodiment, wherein the first semiconductor layer 1902 is no thicker than the doped regions 1910, 1912, so that a majority of the absorbed high energy species are generated in the second semiconductor 1902, enabling efficient carrier transport to the lateral field *p-i-n* backplane.

25 Figures 20 and 21 also show an environmental sealing layer 1908 that also functions as an antireflection coating. This layer 1908 is typically composed of stoichiometric or non-stoichiometric aluminium oxide (Al_2O_3), silicon-dioxide (SiO_2) and silicon nitride (Si_3N_4), although other materials can be alternatively used. Introducing trapped charges into the layer 1908 can be used to preferentially enhance the carrier transport in the
30 wide band gap semiconductor layer 1902. For example, trapped positive or negative charges can form an inversion, accumulation or depletion layer at the interface between the sealing layer 1908 and the wide bandgap semiconductor layer 1902. Such control

can be used as an effective field effect to modify the surface recombination velocity at and within the second semiconductor layer 1902. Depending upon the trap density in the sealing layer 1908 and the thickness of the wide band gap layer 1902, the photovoltaic device can be optimised in this respect.

5

For example, the first semiconductor layer 1904 is typically composed of high quality and high resistivity silicon. The thickness of this silicon layer 1904 is typically in the range of ~0.1-100μm, and is patterned and processed to form a plurality of lateral field *p-i-n* diodes electrically interconnected in series and/or parallel. The second
10 semiconductor 1902 is typically hydrogenated amorphous silicon having a band gap in the range of 1.5-2.0 eV. In other embodiments, the wide band gap semiconductor 1902 is GaP, InAlGaN, CIGS or CdTe. The environmental sealing layer 1908 is selected to provide a high degree of passivation of the second semiconductor layer 1902, and is selected to have a high bandgap energy substantially transparent to the incident solar
15 radiation.

It will be understood by those skilled in the art that a wide variety of variations of the structures described above and shown in Figures 19 to 21 are possible. For example, with reference to Figure 19, in some embodiments, one of the two sets of doped regions
20 1910, 1912 (for example, doped regions 1910) extends into the wide bandgap layer 1902, while the other set (for example, doped regions 1912) remains confined within the narrow bandgap layer 1904. In some embodiments, a graded bandgap semiconductor layer is disposed on the narrow bandgap layer 1904 instead of the wide bandgap layer 1902. In some embodiments, the trenches are alternately filled with
25 different semiconductors to form a lateral heterojunction device.

Compared to standard planar diffused emitter *p-n* junction photovoltaic devices, the photovoltaic devices described herein do not suffer from topside electrode obstruction of incident solar radiation and provide substantially greater effective depletion region
30 volumes capable of separating photo-created charge carriers.

The high-aspect ratio, lateral field *p-i-n* solar cells with thinned backsides described herein enable long carrier lifetimes by the defect-free, single crystal semiconductor active layer. Carrier diffusion lengths of more than 100 microns are typically achieved. This enables the majority of the carriers that are generated by absorbed photons to be
5 collected.

Many modifications will be apparent to those skilled in the art without departing from the scope of the present invention.

CLAIMS:

1. A process for forming a photovoltaic device, including:

   forming photovoltaic devices in a first face of a planar semiconductor substrate having opposed first and second faces;

   forming a planar interconnect layer having electrically conductive paths with electrically insulating regions therebetween, the planar interconnect layer being formed on one of the semiconductor substrate and a planar handle substrate;

   bonding the other of the semiconductor substrate and the planar handle substrate to the interconnect layer to form a bonded stack wherein the electrically conductive paths in the planar interconnect layer are electrically connected to the photovoltaic devices in the semiconductor substrate; and

   thinning the semiconductor substrate from its second face to at least reduce the thickness of the semiconductor between the second face and the photovoltaic devices in the semiconductor substrate to improve the efficiency of the photovoltaic devices.

2. The process of claim 1, including selecting the reduced thickness of the semiconductor to provide a balance between absorption of incident photons and allowing charge carriers generated by the absorbed photons to be collected.

3. The process of claim 1 or 2, including selecting the reduced thickness of the semiconductor to provide sufficient heat extraction from the device.

4. The process of claim 1, wherein said thinning removes substantially all of the semiconductor between the second face of the semiconductor substrate and the photovoltaic solar cells therein.

5. The process of any one of claims 1 to 4, wherein the photovoltaic devices are lateral field photovoltaic devices.

6. The process of any one of claims 1 to 5, wherein the electrically conductive paths of the interconnect layer include one or more electrically conductive paths

extending to one or more edges of the interconnect layer to provide one or more electrical contacts to the photovoltaic devices.

7. The process of any one of claims 1 to 6, wherein the handle substrate is electrically insulating, and the process includes forming one or more electrically conductive paths through the handle substrate, wherein the electrically conductive paths of the interconnect layer include one or more electrically conductive paths that electrically connect one end of each electrically conductive path through the handle layer to the photovoltaic devices, the other end of each electrically conductive path through the handle layer providing an external electrical contact to the photovoltaic devices.

8. The process of any one of claims 1 to 6, including forming electronic circuitry in the handle substrate to process output of the photovoltaic devices.

9. The process of any one of claims 1 to 7, wherein the handle substrate is made from a material having a high thermal conductivity to provide cooling to the photovoltaic device.

10. A photovoltaic device, including:

a semiconductor layer having photovoltaic solar cells formed therein;

a handle substrate; and

an interconnect layer disposed between the semiconductor layer and the handle substrate and including electrically conductive paths electrically connected to the photovoltaic solar cells in the semiconductor layer.

11. The device of claim 10, wherein the semiconductor layer has opposed first and second faces, the semiconductor layer is attached to the interconnect layer by the first face, and the photovoltaic devices are formed in the first face.

12. The device of claim 10 or 11, wherein the photovoltaic devices are spaced from the second face of the semiconductor layer by a thickness of semiconductor.

13. The device of claim 12, wherein the semiconductor between the second face and the photovoltaic devices has a thickness that provides a balance between absorption of photons incident on the second face and allowing charge carriers generated by the absorbed photons to be collected.

14. The device of any one of claims 10 to 13, wherein the interconnect layer includes a plurality of metal layers.

15. The device of any one of claims 10 to 14, wherein the photovoltaic devices are lateral field photovoltaic devices.

16. The device of any one of claims 10 to 15, wherein the electrically conductive paths of the interconnect layer include one or more electrically conductive paths extending to one or more edges of the interconnect layer to provide one or more electrical contacts to the photovoltaic devices.

17. The device of any one of claims 10 to 16, wherein the handle substrate is electrically insulating but includes one or more electrically conductive paths through the handle substrate, and the electrically conductive paths of the interconnect layer include one or more electrically conductive paths that electrically connect one end of each electrically conductive path through the handle layer to the photovoltaic devices, and the other end of each electrically conductive path through the handle layer provides an external electrical contact to the photovoltaic devices.

18. The device of any one of claims 10 to 17, wherein the handle substrate includes electronic circuitry configured to process output of the photovoltaic devices.

19. The device of any one of claims 10 to 18, including an integrated circuit chip that is flip chip bonded to conductive paths of the handle substrate.

20. The device of any one of claims 10 to 19, wherein the handle substrate is made from a material having a high thermal conductivity to provide cooling to the photovoltaic device.

21. A process for forming a photovoltaic device, including:

forming a plurality of mutually spaced recesses in a face of a semiconductor layer;

doping at least the sidewalls of the recesses in the semiconductor layer and filling the recesses with a conductive material to form sets of conductive regions having respective opposite doping polarities;

wherein each pair of adjacent and oppositely doped conductive regions forms a corresponding space charge region having a corresponding electric field therein, the space charge region extending substantially from the surface of the semiconductor layer and into the semiconductor layer such that electron-hole pairs created substantially at the surface of the semiconductor layer by photons entering the space charge region are separated in opposing directions by the electric field and collected by the corresponding pair of doped regions, thereby providing an electrical current to be conducted from the device.

22. The process of claim 21, wherein the doped regions extend into the semiconductor layer in a direction substantially orthogonal to the face of the semiconductor layer, where the depth of each doped region is greater than its width.

23. The process of claim 21 or 22, wherein the depth of each doped region is at least twice its width.

24. The process of any one of claims 21 to 23, wherein each pair of adjacent and oppositely doped conductive regions and the region therebetween forms a corresponding p-i-n diode.

25. The process of any one of claims 21 to 24, wherein the sets of conductive regions having respective opposite doping polarities have an interdigitated configuration.

26. The process of any one of claims 21 to 25, wherein the mutually spaced recesses include a first set of mutually spaced recesses extending into the semiconductor layer to a first depth, and a second set of mutually spaced recesses extending into the semiconductor layer to a second depth greater than the first depth, at least the sidewalls of the first set of mutually spaced recesses being doped to a first polarity, and at least the sidewalls of the second set of mutually spaced recesses being doped to a second polarity opposite to the first polarity.

27. The process of claim 26, wherein the sidewalls and bases of the second set of recesses are doped to form a corresponding set of mutually spaced doped regions that extend through the semiconductor layer to a doped layer of the second polarity.

28. The process of any one of claims 21 to 27, including forming electrical contacts to the conductive regions, and bonding the electrical contacts to corresponding electrical contacts of a support.

29. The process of claim 28, wherein the semiconductor layers are semiconductor wafers, and the process includes applying the process of any one of claims 21 to 27 to a plurality of semiconductor wafers, forming electrical contacts to the conductive regions of the processed semiconductor wafers, and bonding the electrical contacts of the processed semiconductor wafers to corresponding electrical contacts of a support so that the processed semiconductor wafers are supported by and electrically interconnected by the support.

30. The process of claim 29, wherein the semiconductor layers are semiconductor-on-insulator wafers.

31. The process of any one of claims 21 to 30, wherein the sets of conductive regions are spaced from a second face of the semiconductor layer opposite to the face in which the recesses were formed, and the process includes removing a portion of

the semiconductor layer from the second face to reduce the thickness of semiconductor between the conductive regions and the second face.

32. The process of any one of claims 21 to 30, wherein the sets of conductive regions are spaced from a second face of the semiconductor layer opposite to the face in which the recesses were formed, and the process includes removing a portion of the semiconductor layer from the second face to remove the semiconductor between at least one of the sets of conductive regions and the second face.

33. The process of claim 31 or 32, wherein said removing reduces the thickness of an inner portion of the semiconductor layer while leaving a relatively thick peripheral portion of the semiconductor layer to act as a structural support for the processed semiconductor layer.

34. The process of any one of claims 21 to 33, including:

directing an energetic beam of at least one species into the recesses in the face of the semiconductor layer to implant the at least one species into the semiconductor layer, the implantation being performed at a plurality of different relative orientations between the energetic beam and the semiconductor layer to form a buried non-planar defective layer within the semiconductor layer; and

heating the implanted layer so that the non-planar defective layer within the semiconductor layer causes the semiconductor layer to split into two layers, each of said layers having a non-planar surface corresponding to the non-planar defective layer.

35. A process for forming a photovoltaic device, including:

forming a plurality of mutually spaced recesses in a face of a semiconductor substrate;

directing an energetic beam of at least one species into the recesses in the face of the semiconductor substrate to implant the at least one species into the semiconductor substrate, the implantation being performed at a plurality of different relative orientations between the energetic beam and the substrate to

form a buried non-planar defective layer within the semiconductor substrate; and

heating the implanted substrate so that the non-planar defective layer within the semiconductor substrate causes the substrate to split into two layers, each of said layers having a non-planar surface corresponding to the non-planar defective layer.

36. The process of claim 35, wherein the remaining portions of the face of the semiconductor substrate between the recesses have a masking layer thereover to substantially prevent those portions of the face from being implanted, the different relative orientations between the energetic beam and the substrate being selected so that the buried non-planar defective layer extends beneath the masked portions of the face.

37. The process of claim 35 or 36, including:

forming micro-electronic and/or micro-mechanical devices in the semiconductor substrate; and

bonding the semiconductor substrate to a support;

wherein said heating causes the substrate to split into two layers, one of which remains bonded to the support and includes the devices.

38. The process of claim 37, wherein the support includes electrically conductive paths that form electrical connections to the devices when the support is bonded to the semiconductor substrate.

39. The process of claim 38, wherein the devices are photovoltaic devices, and the electrically conductive paths interconnect the photovoltaic devices.

40. The process of claim 39, wherein the photovoltaic devices are lateral field *p-i-n* photovoltaic devices with high aspect ratio doped regions.

41. The process of claim 39 or 40, wherein the devices include dielectric and metal regions that cause light passing through the semiconductor layer without being

absorbed to be redirected back into the semiconductor layer for absorption therein.

42. The process of any one of claims 35 to 41, including forming an anti-reflection coating on the non-planar surface of one of the layers.

43. The process of any one of claims 35 to 41, including forming a second non-planar semiconductor layer on the non-planar surface of one of the layers, the second semiconductor layer having a larger bandgap than the other semiconductor layer to preferentially absorb high energy photons therein.

44. The process of claim 43, including forming an anti-reflection coating on the second non-planar semiconductor layer.

45. The process of claim 42 or 44, wherein the anti-reflection coating includes trapped charge to reduce surface recombination of charge carriers.

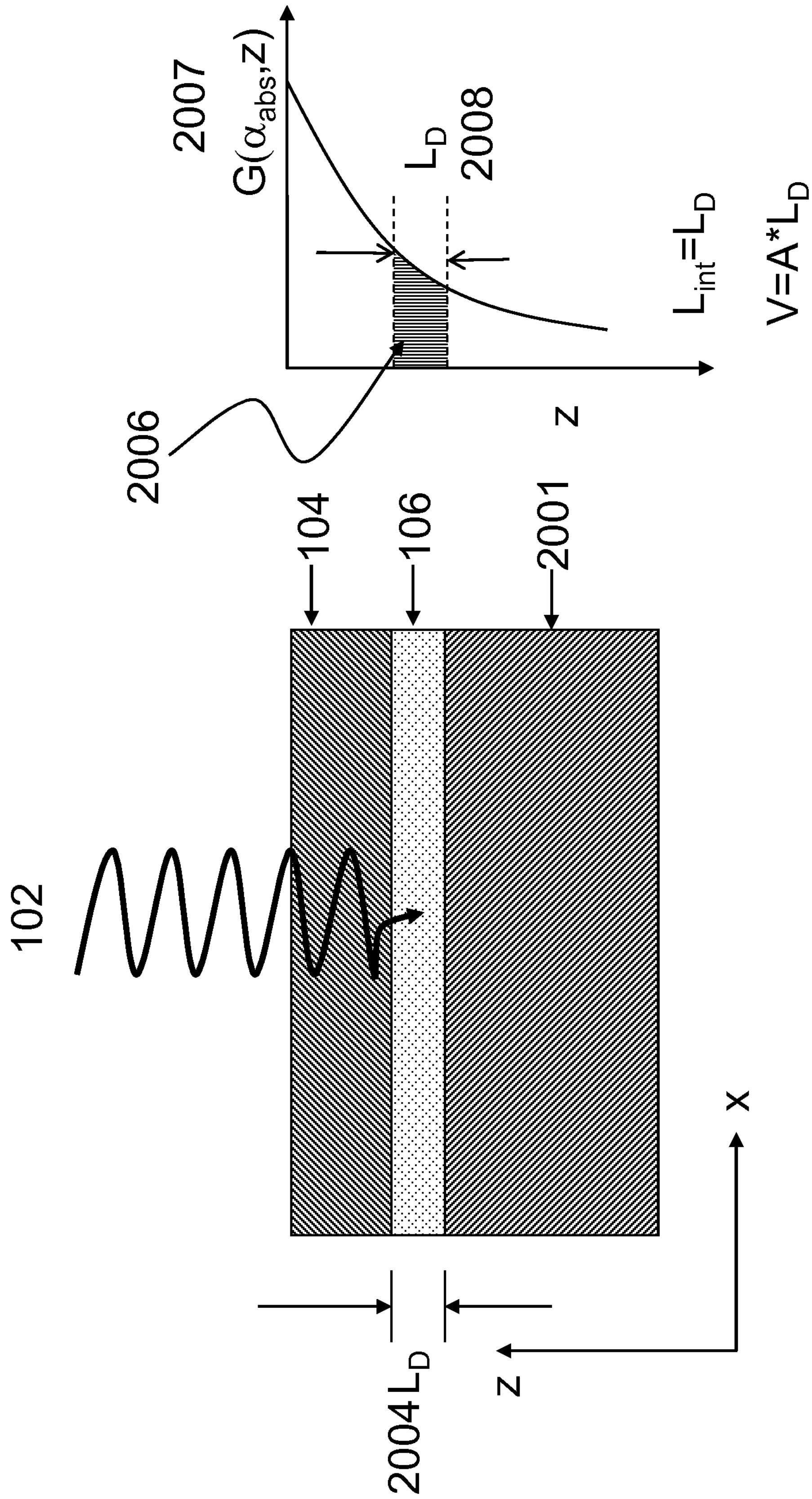

Figure 1A

Figure 1B

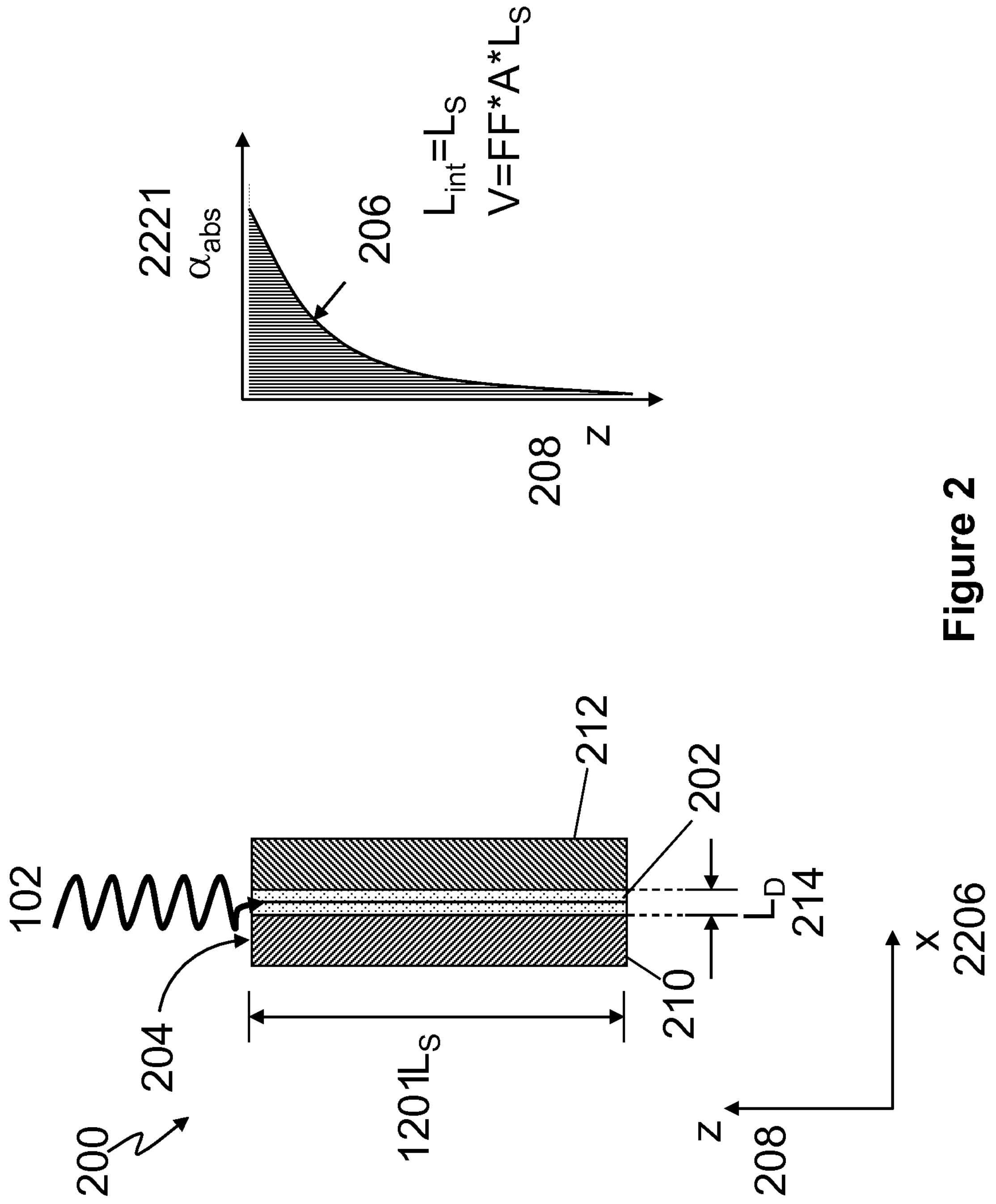

Figure 2

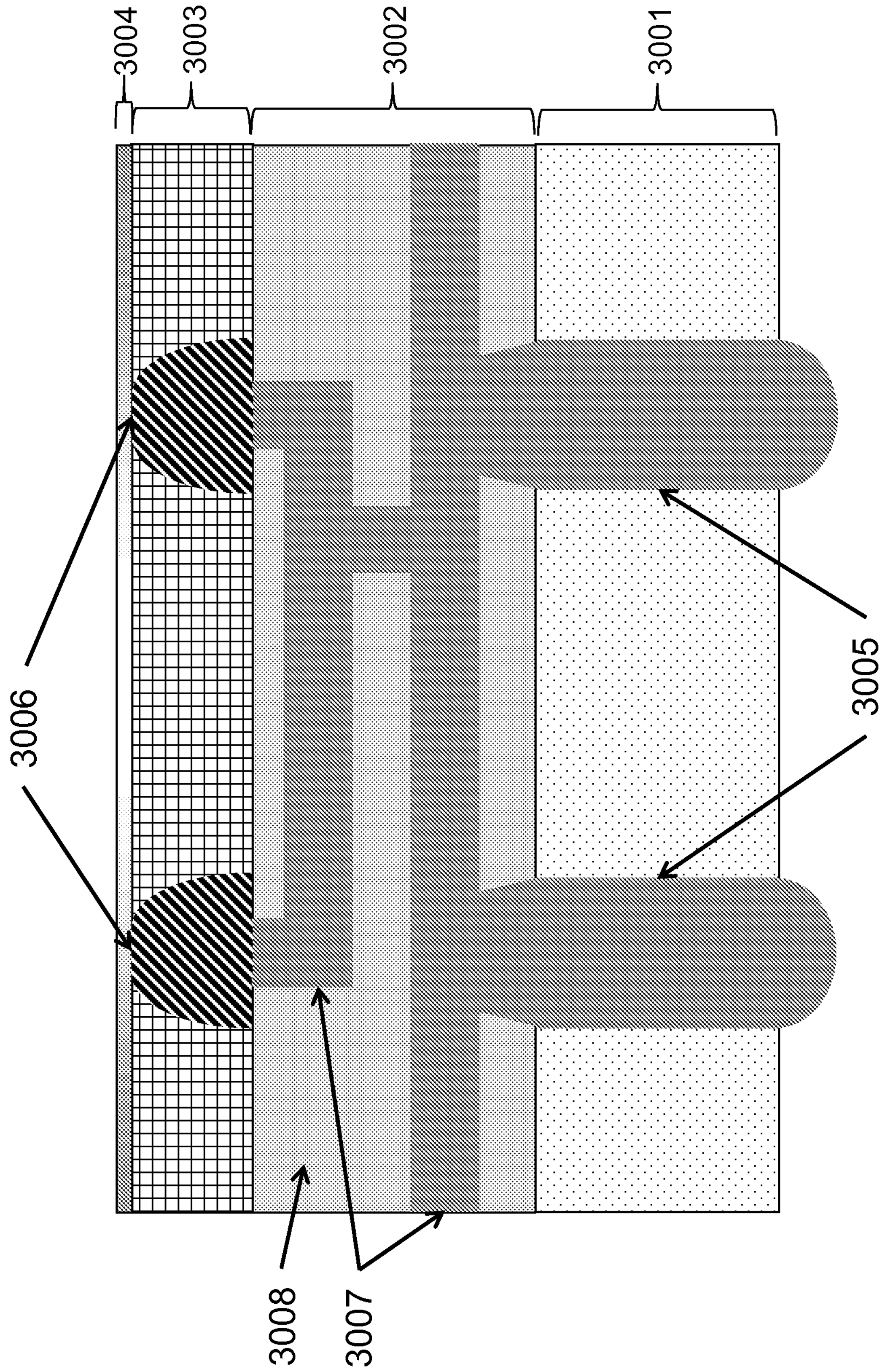

Figure 3

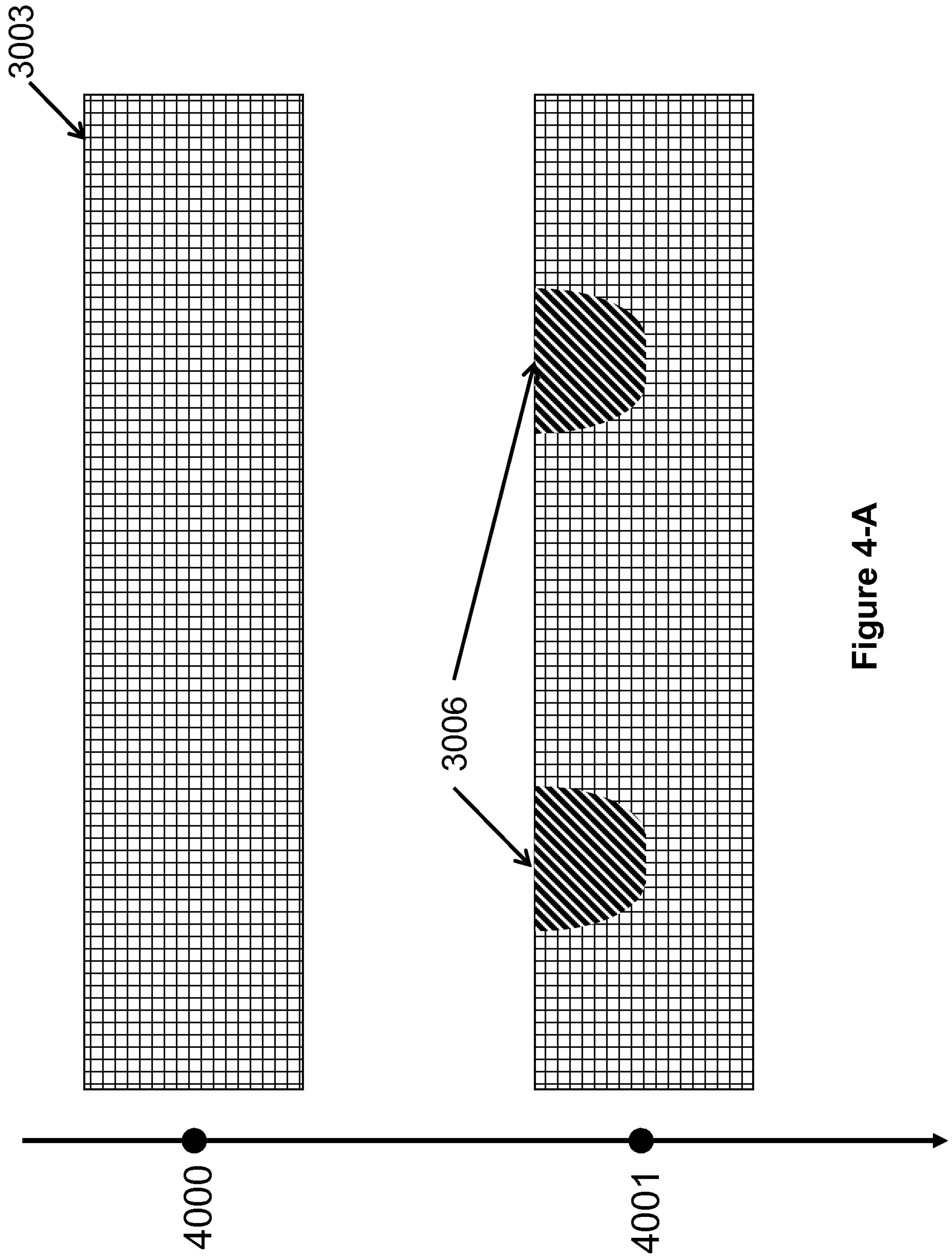

Figure 4-A

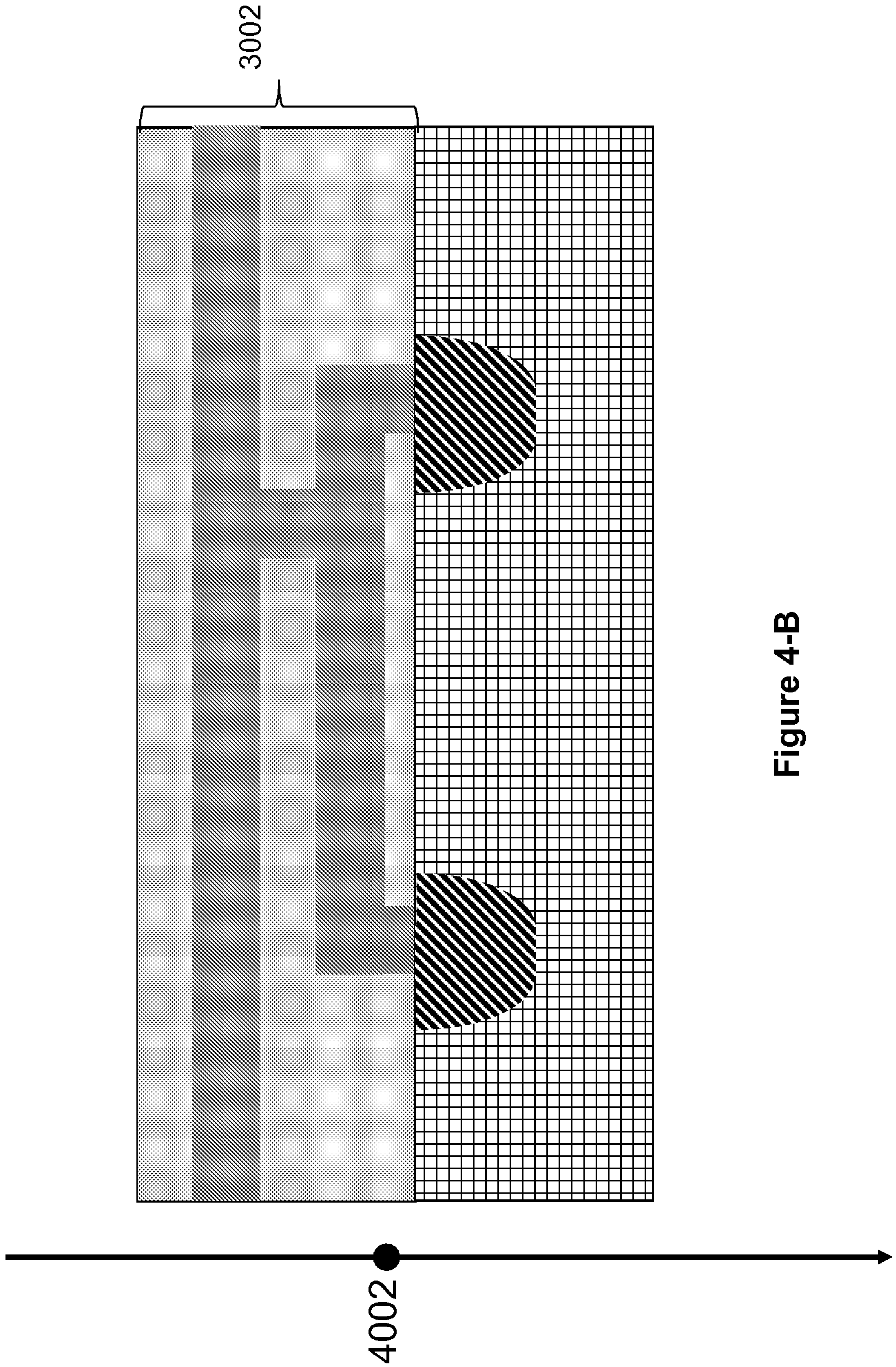

Figure 4-B

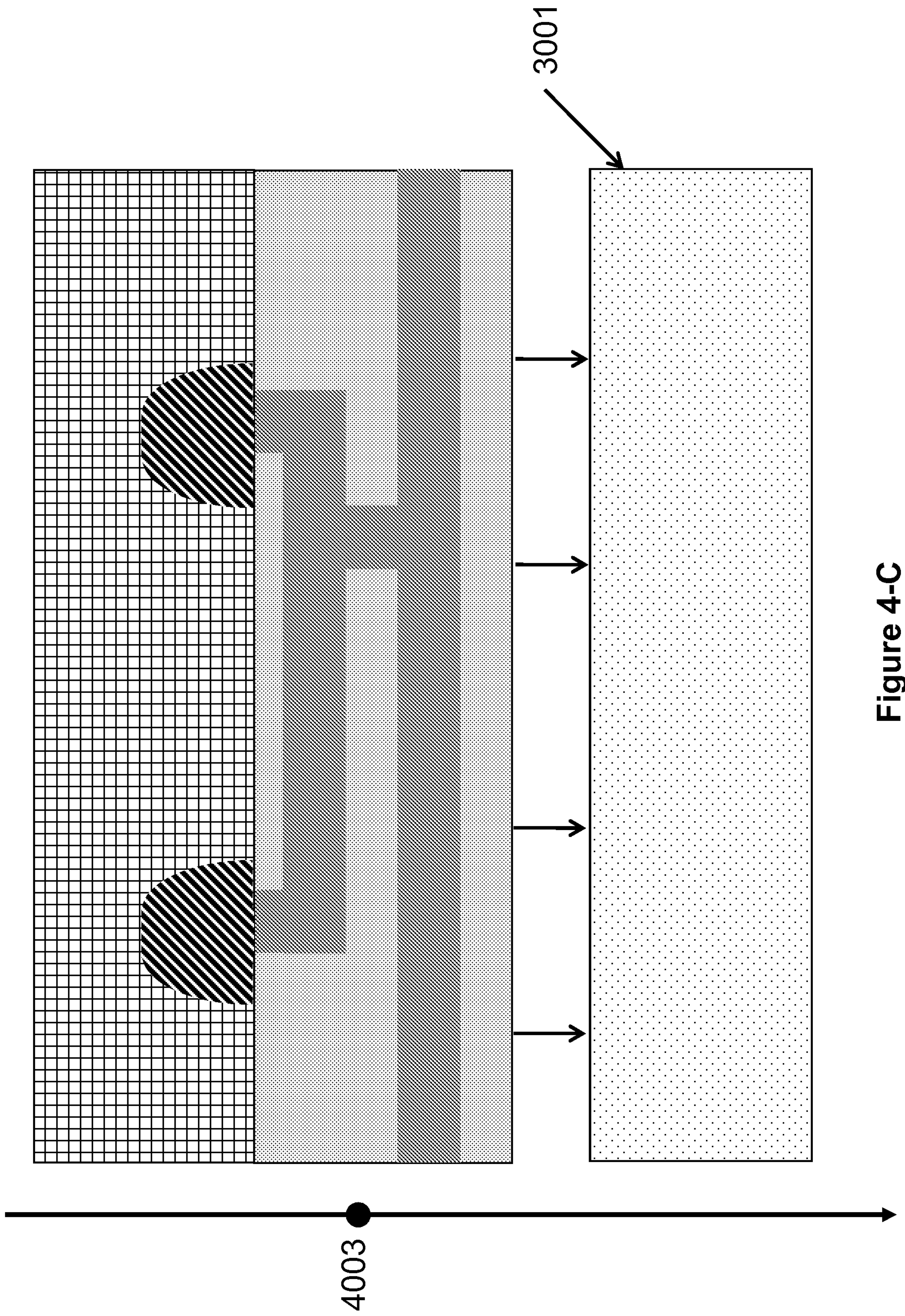

Figure 4-C

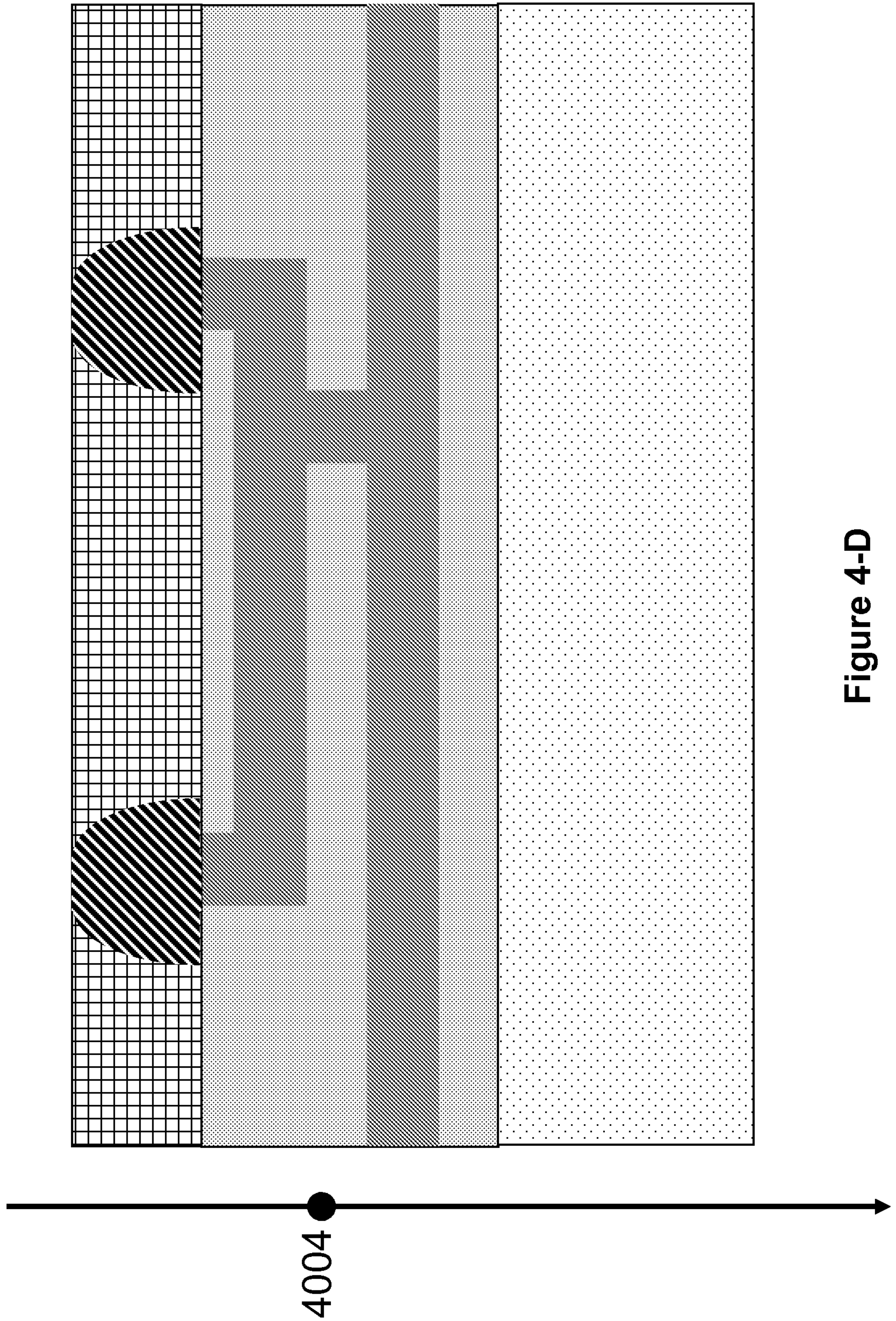

Figure 4-D

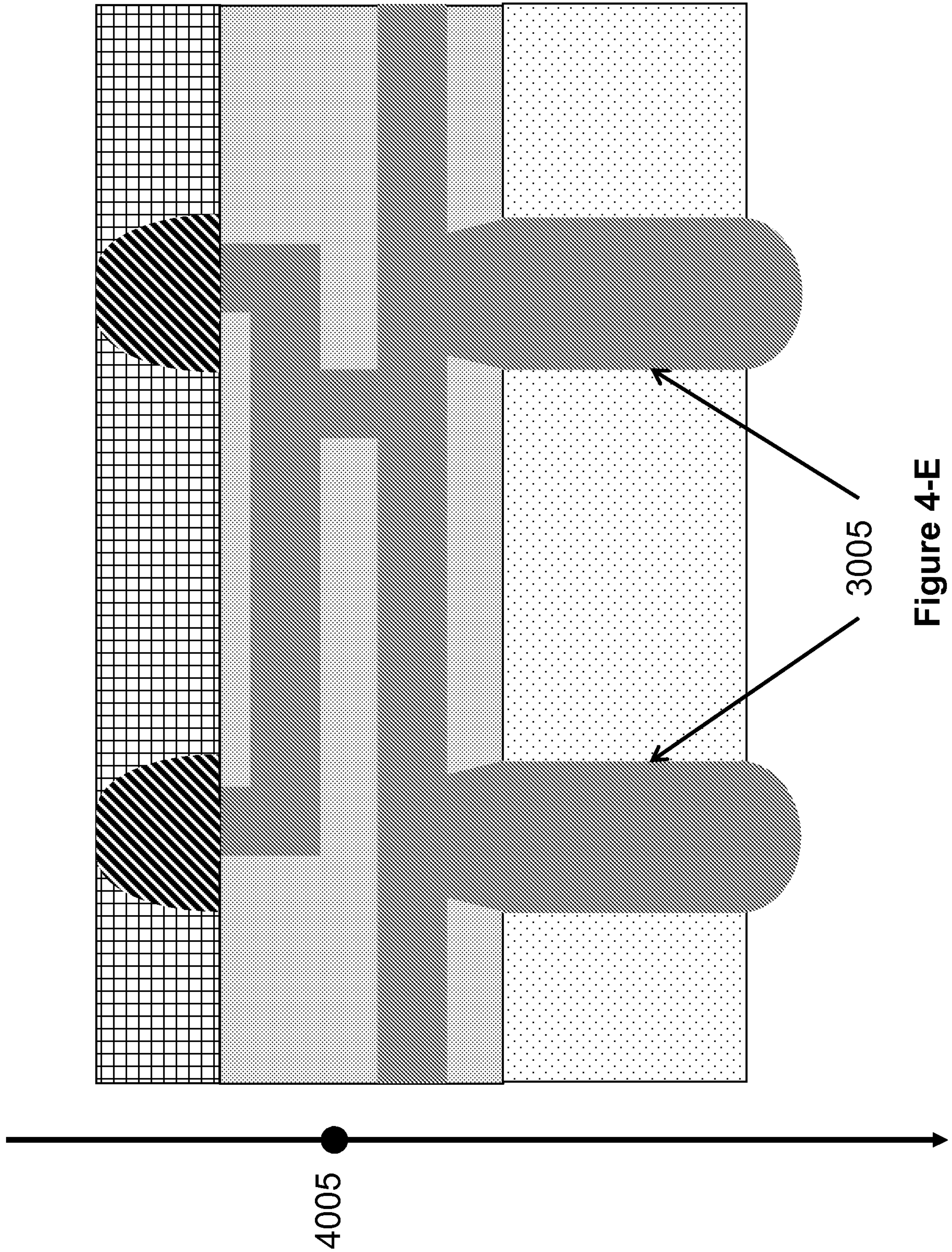

Figure 4-E

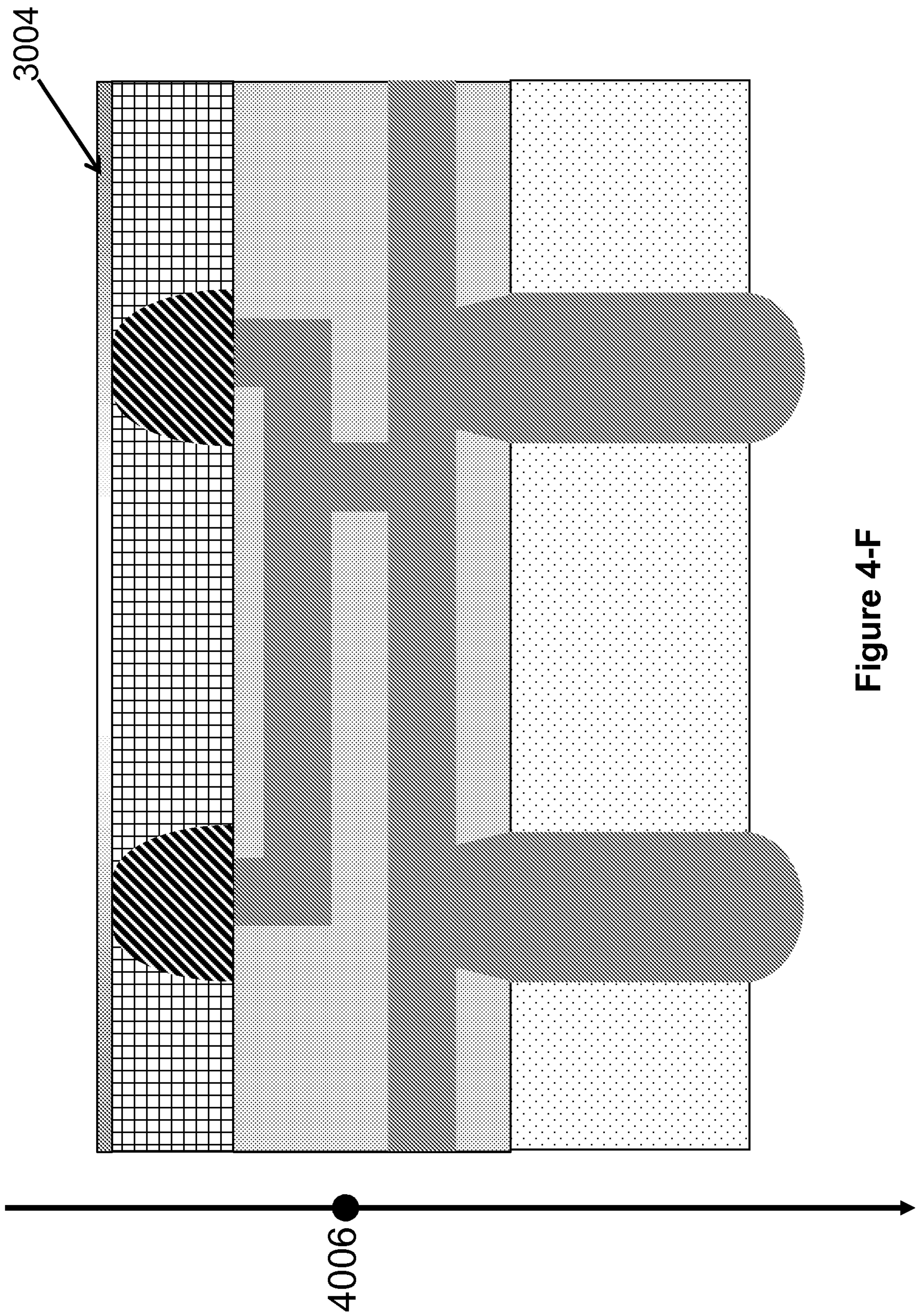

Figure 4-F

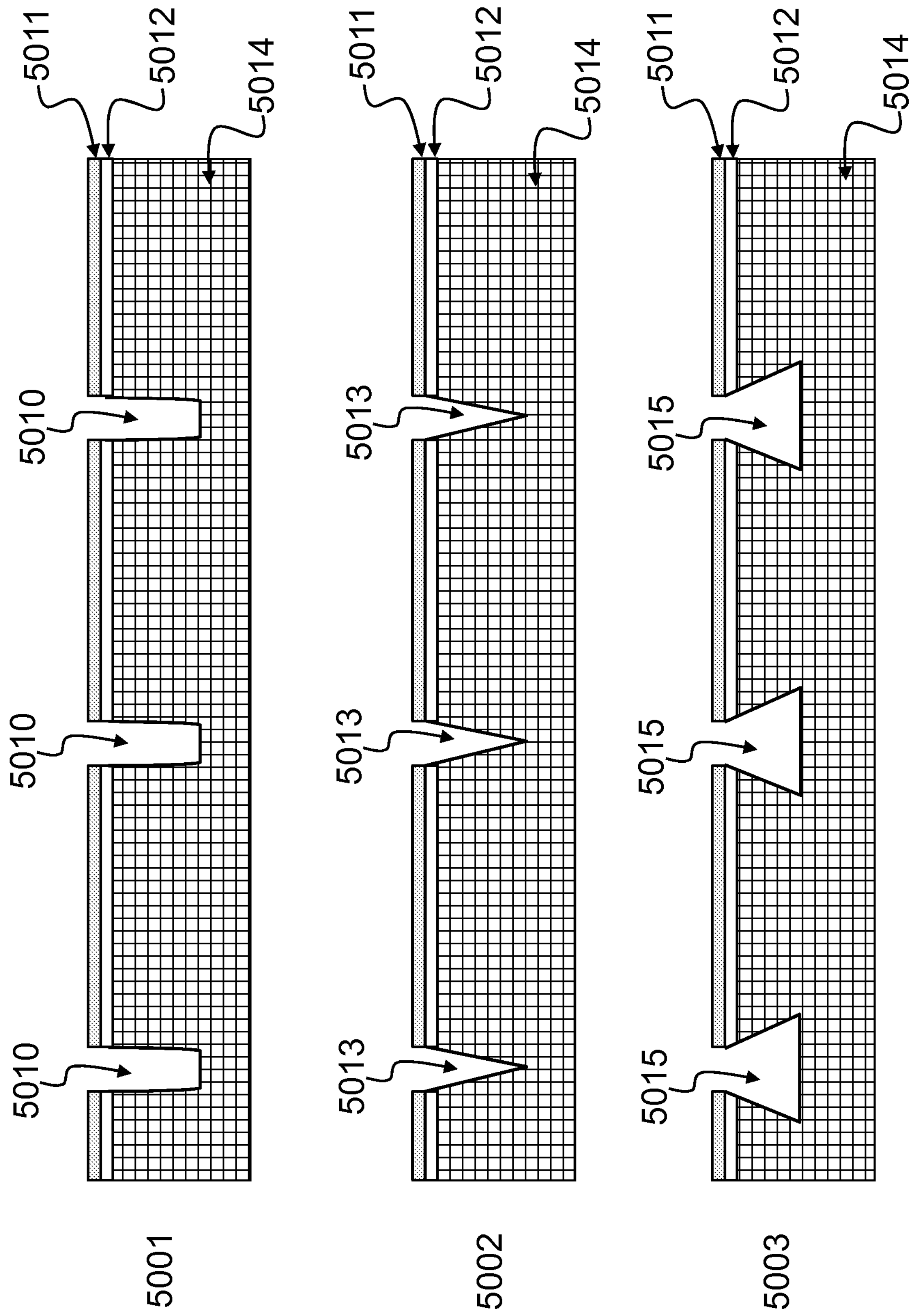

Figure 5

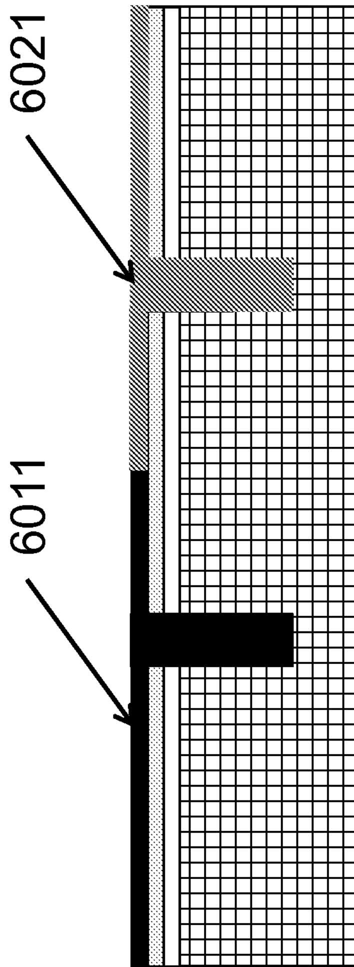

Figure 6a

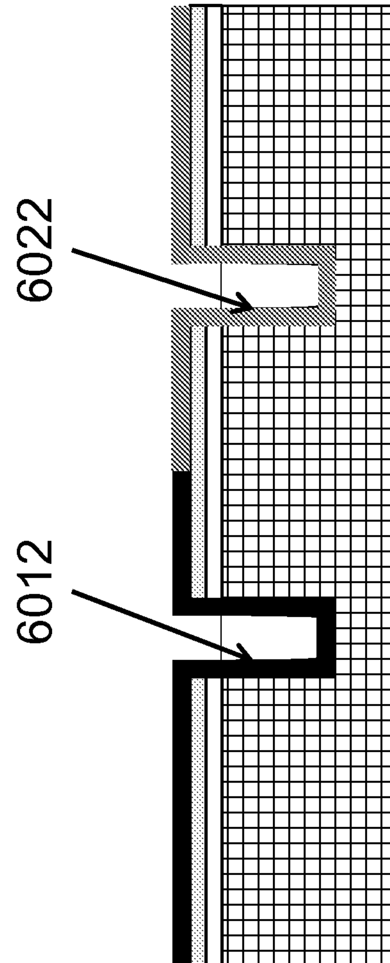

Figure 6b

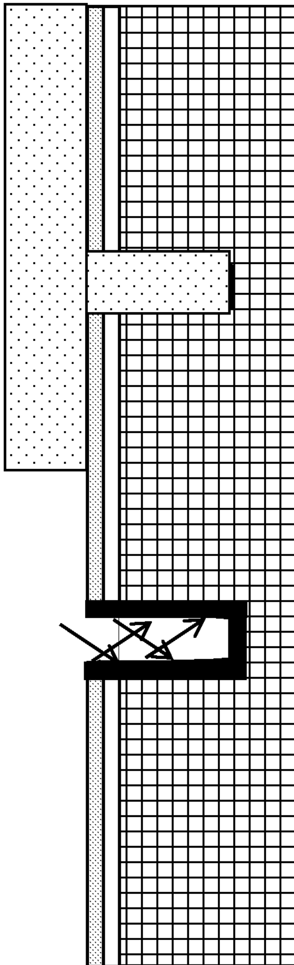

Figure 6c

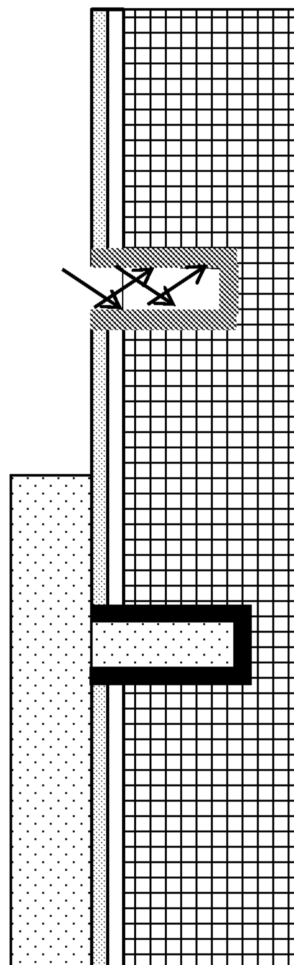

Figure 6d

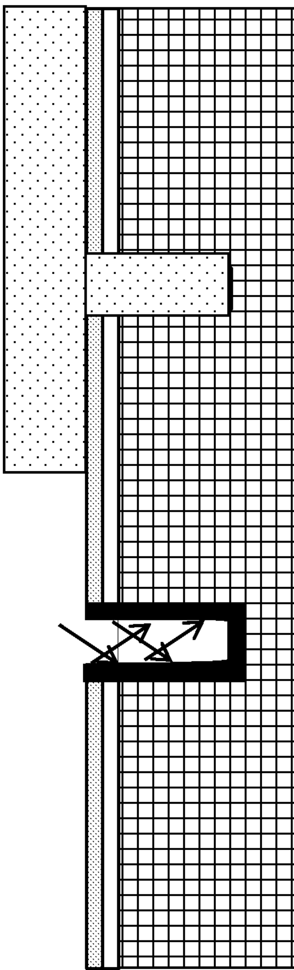

Figure 6e

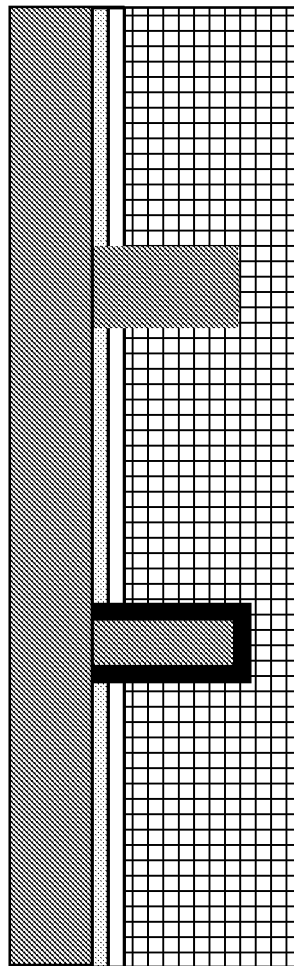

Figure 6f

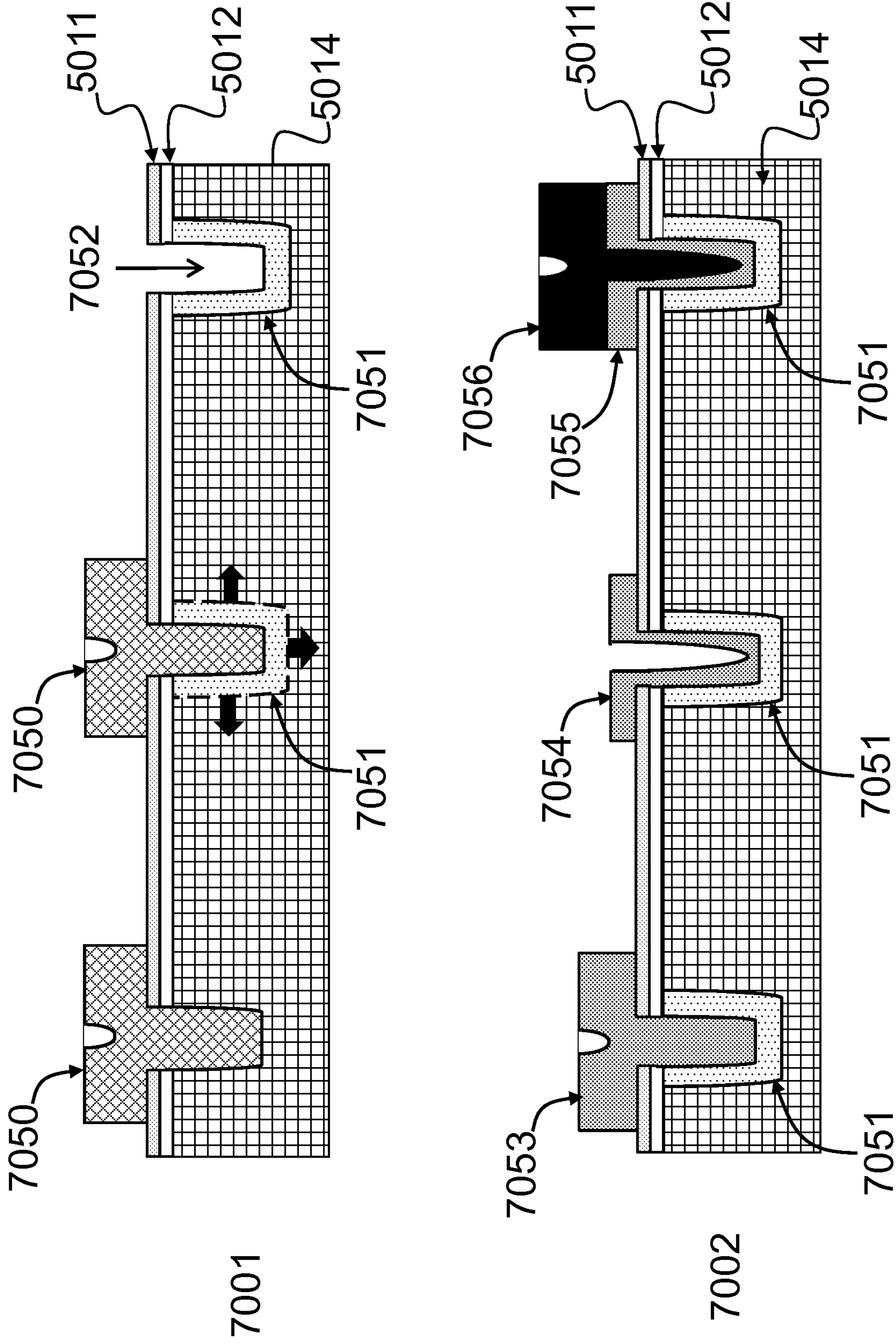

Figure 7

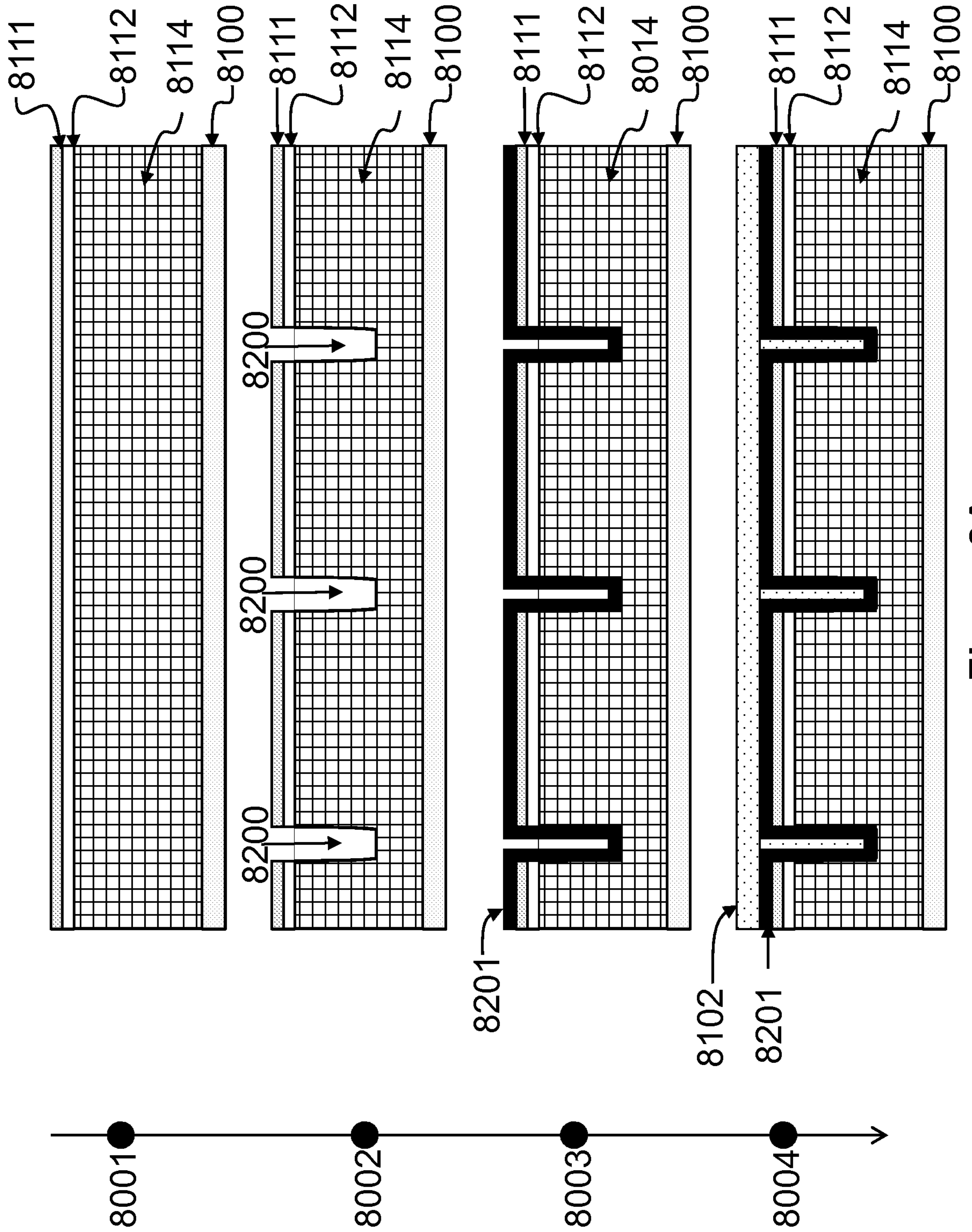

Figure 8A

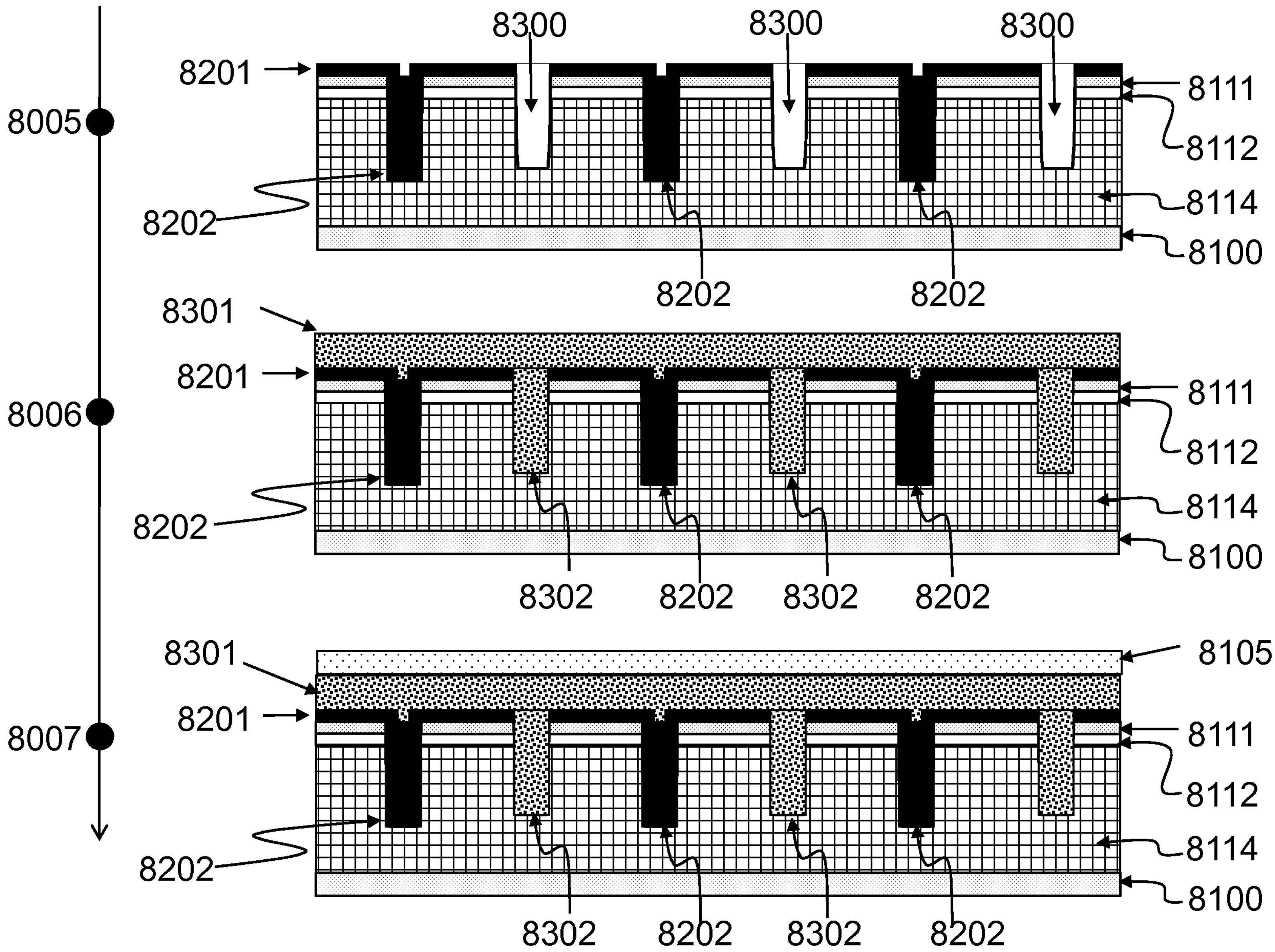

Figure 8B

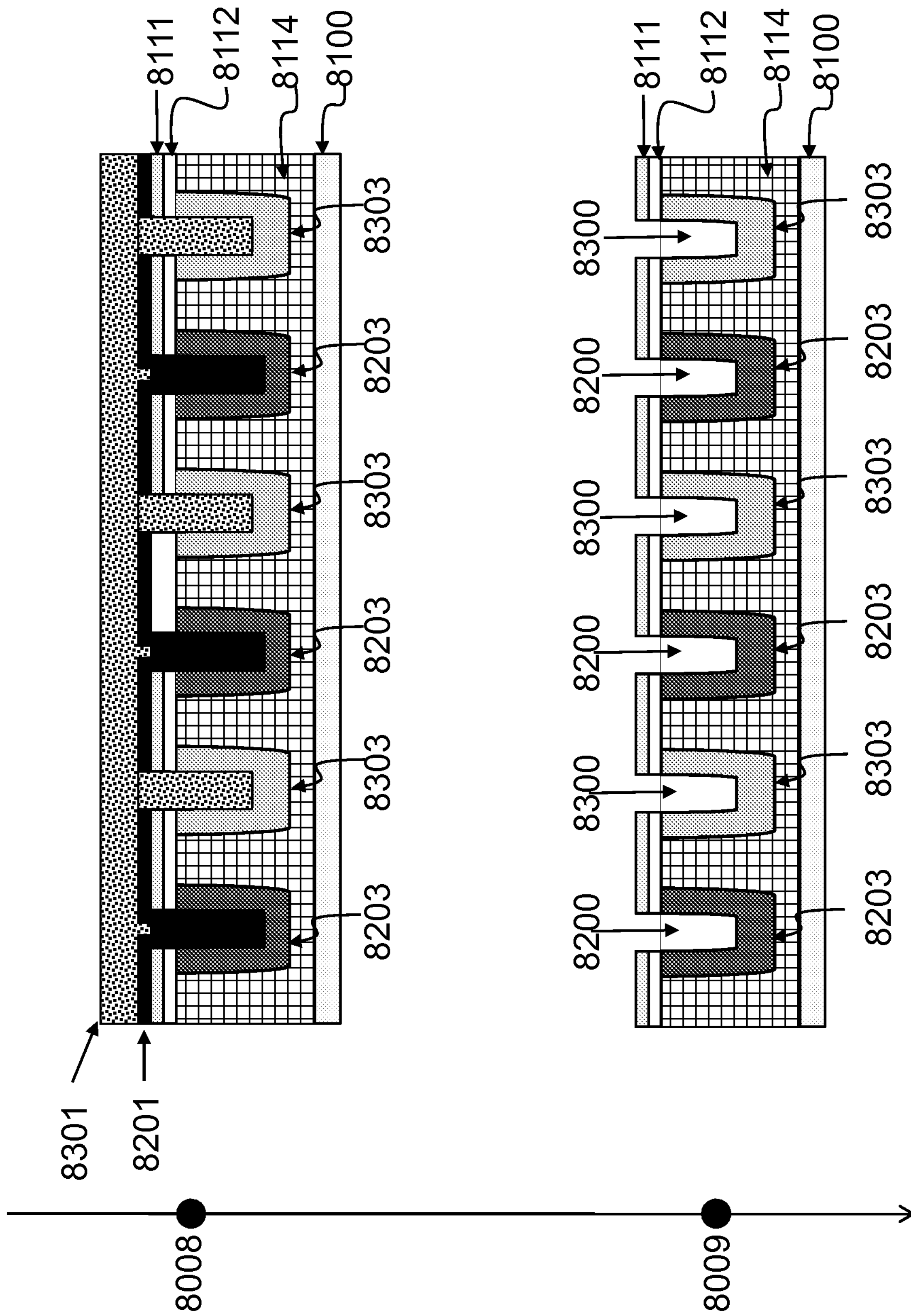

Figure 8C

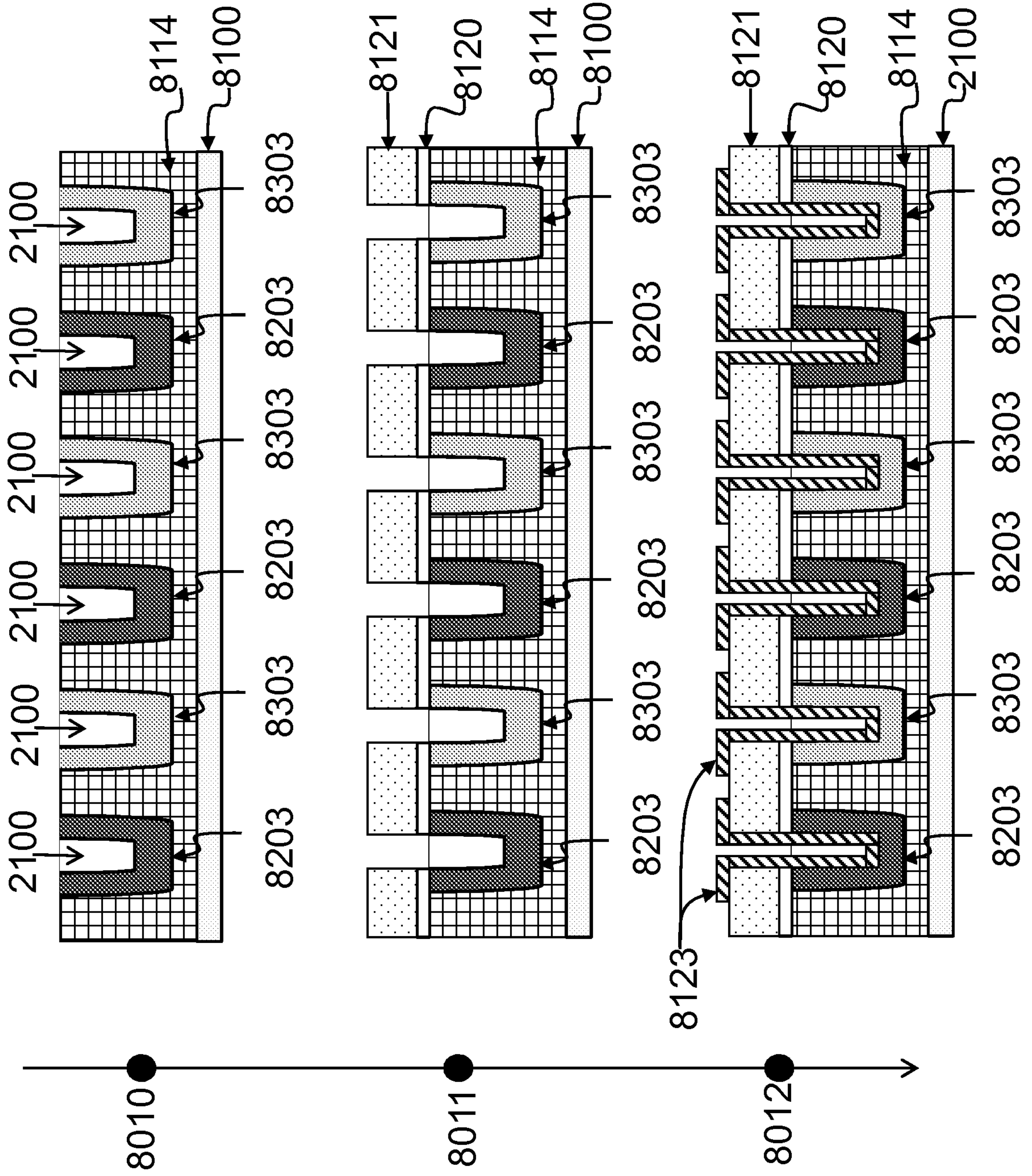

Figure 8D

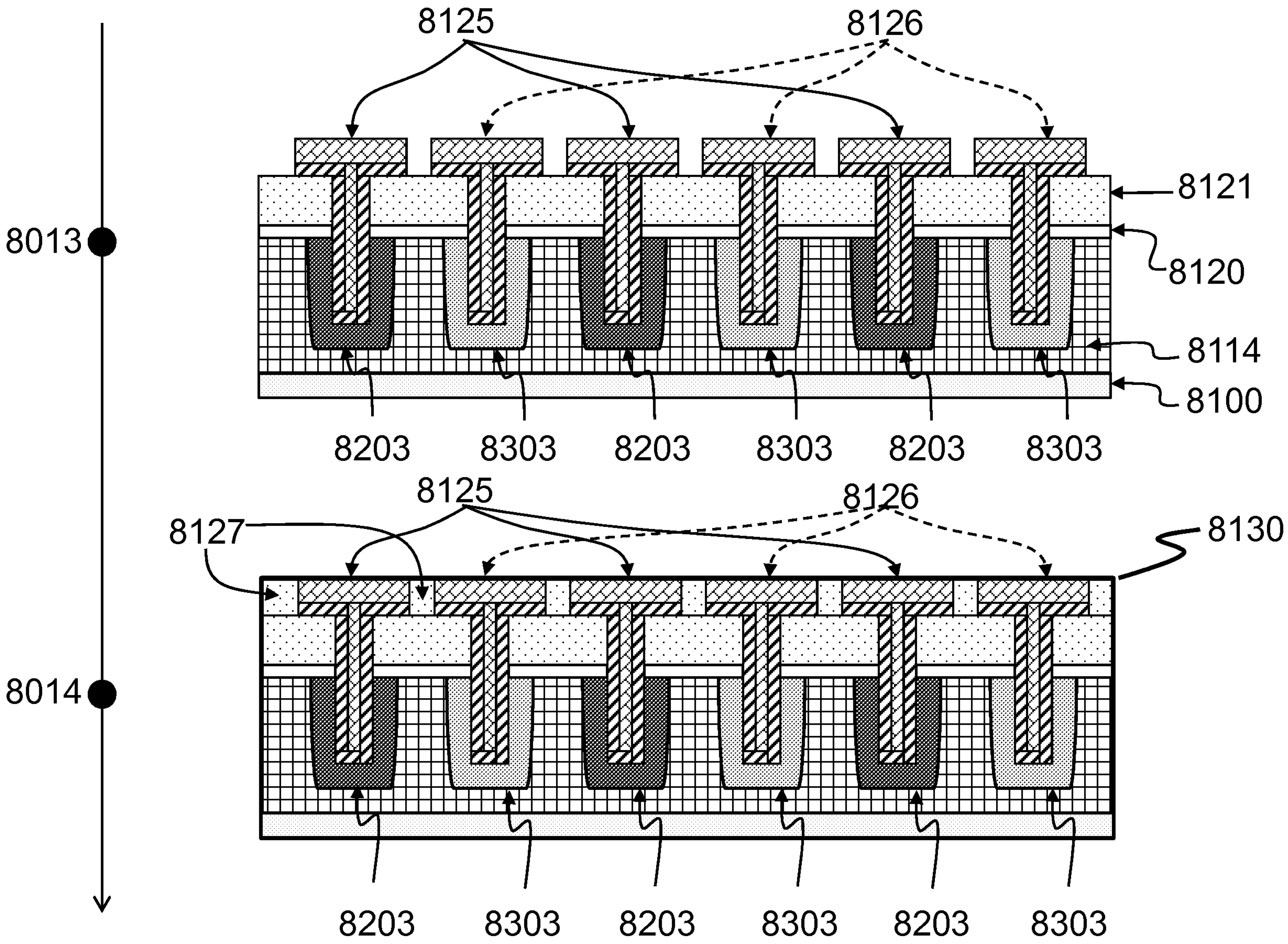

Figure 8E

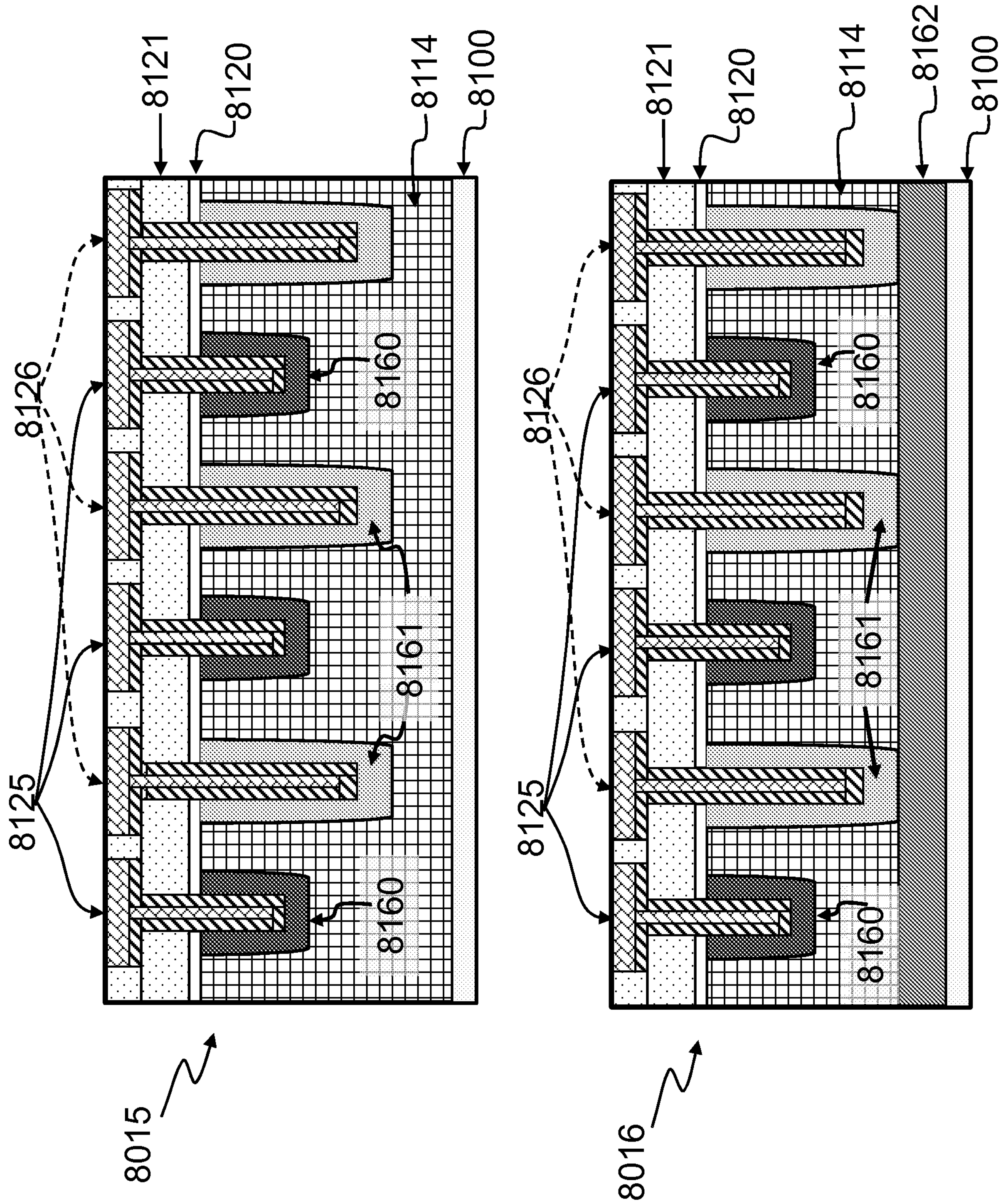

Figure 8F

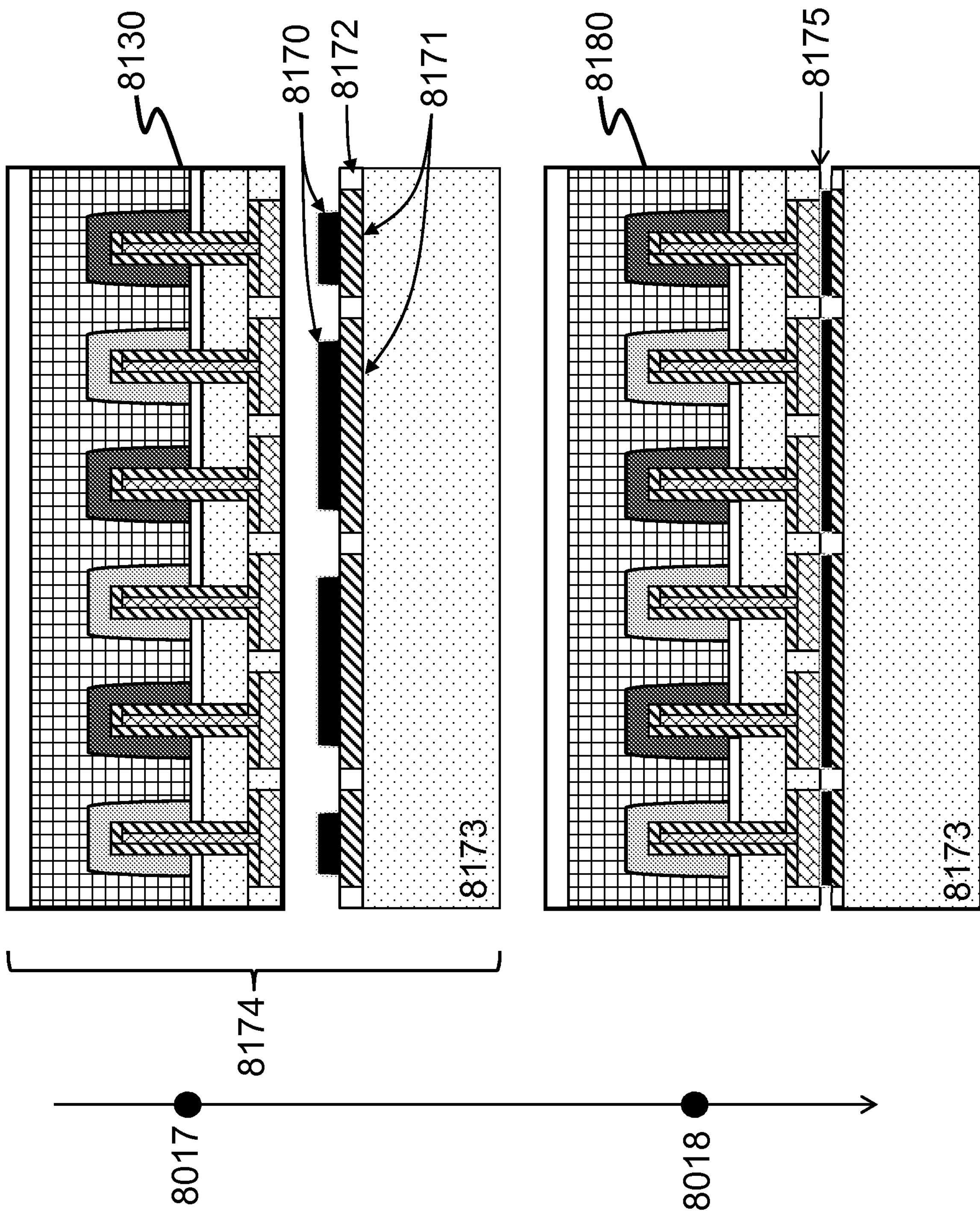

Figure 8G

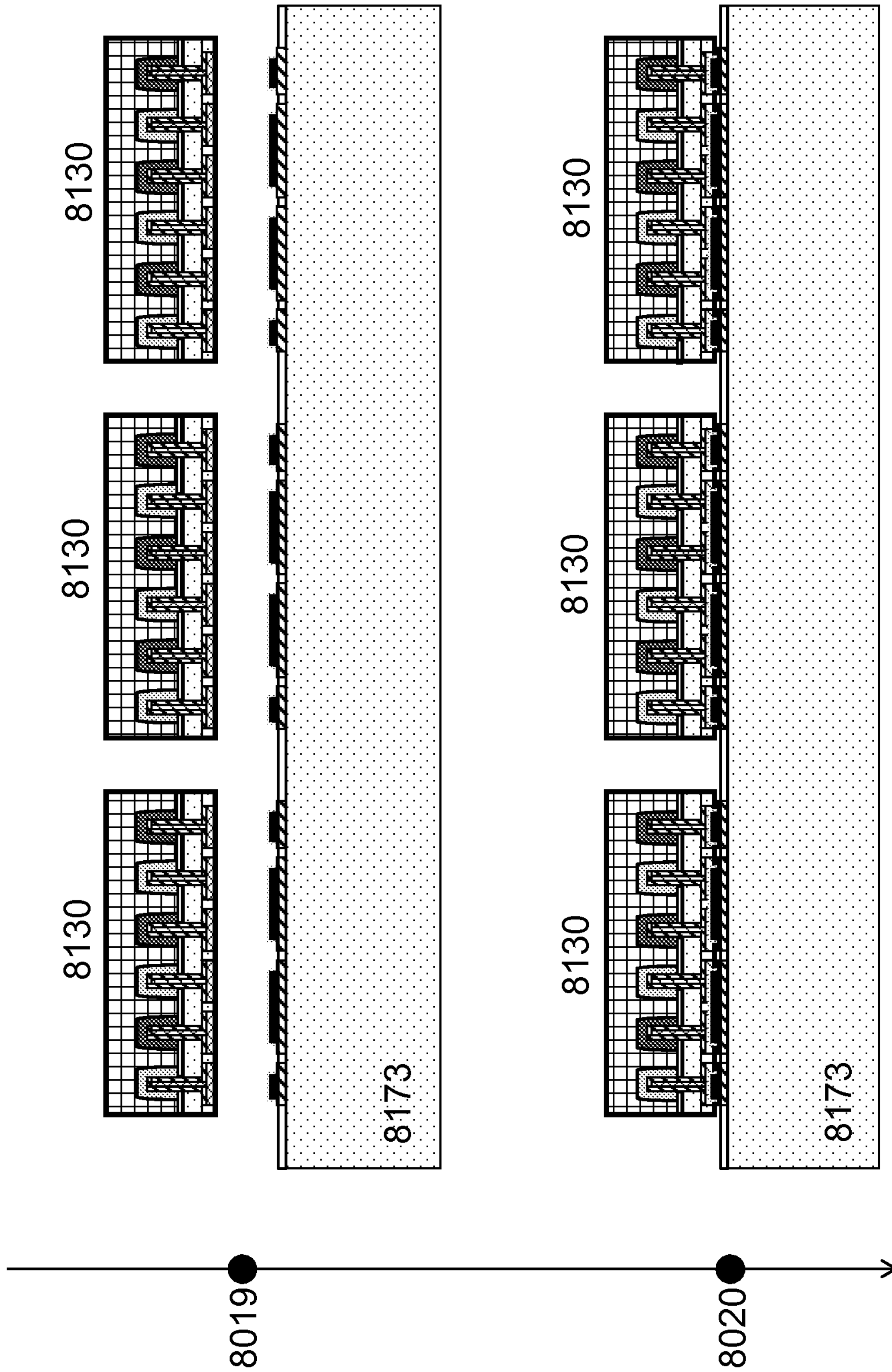

Figure 8H

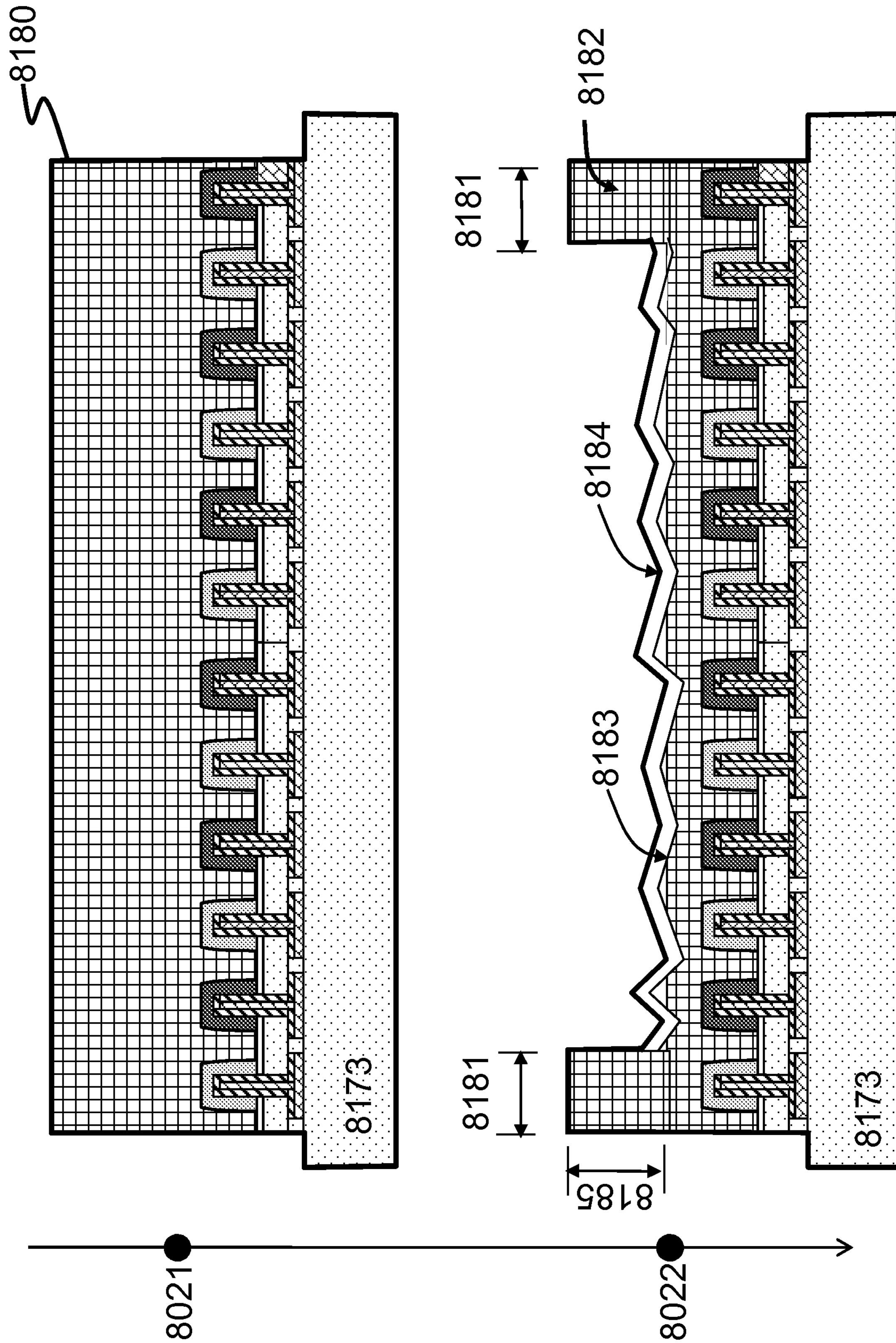

Figure 8I

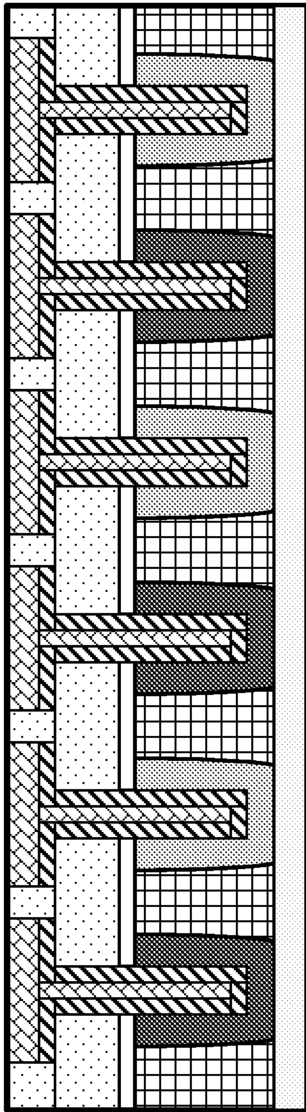

Figure 9a

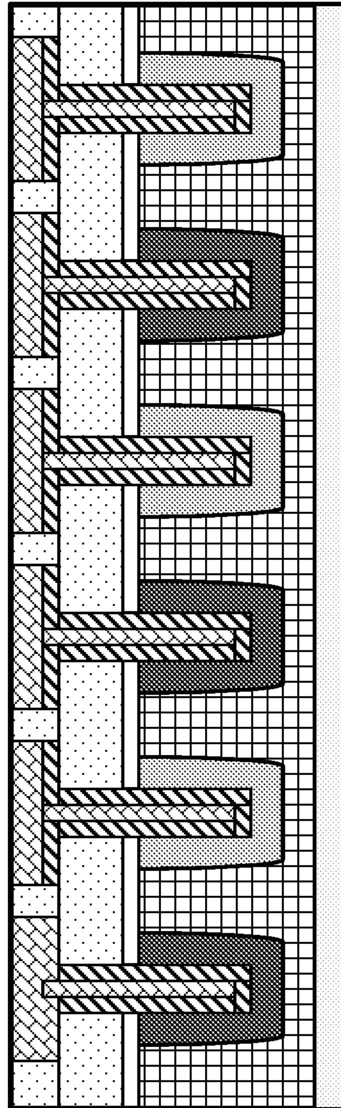

Figure 9b

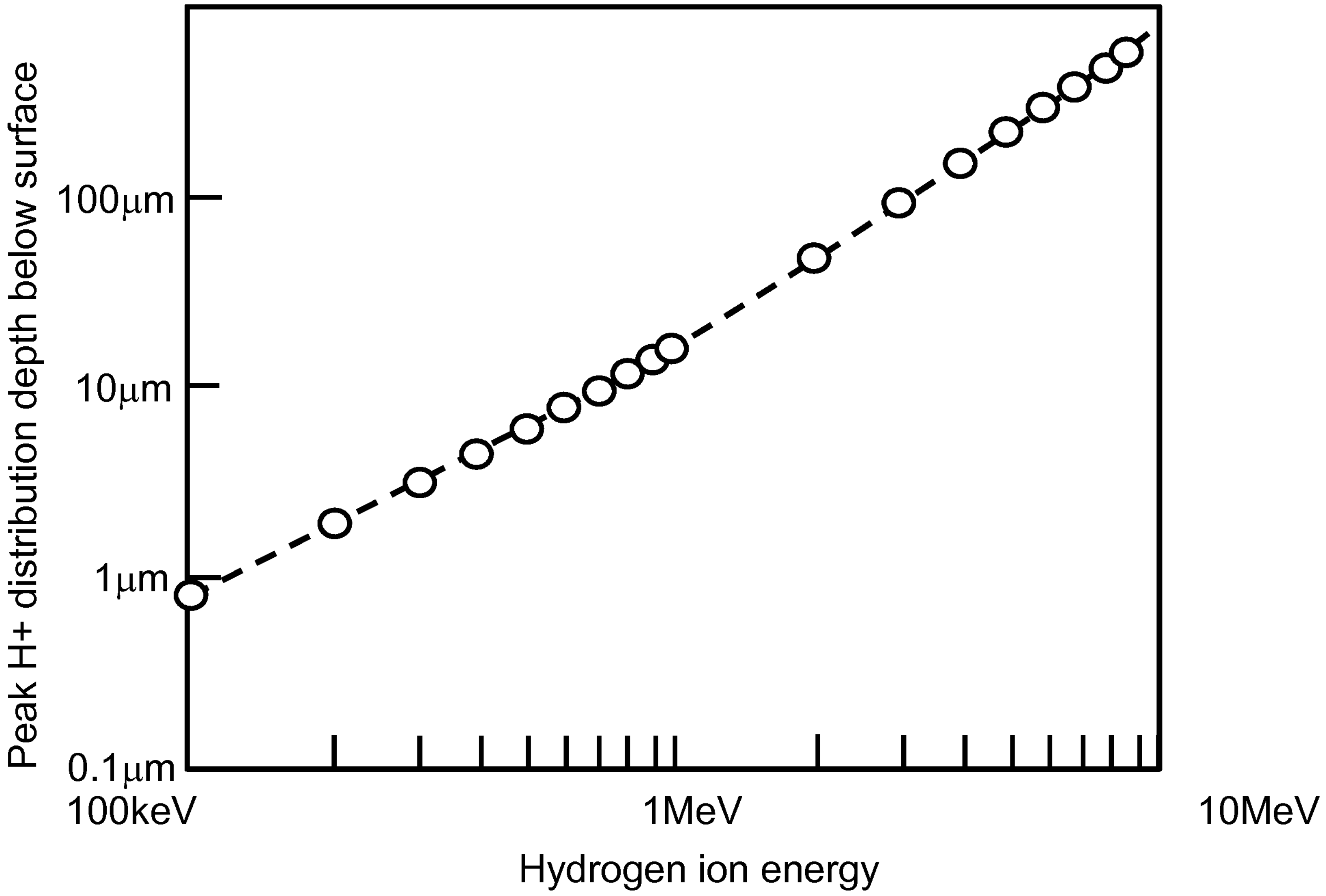

Figure 10

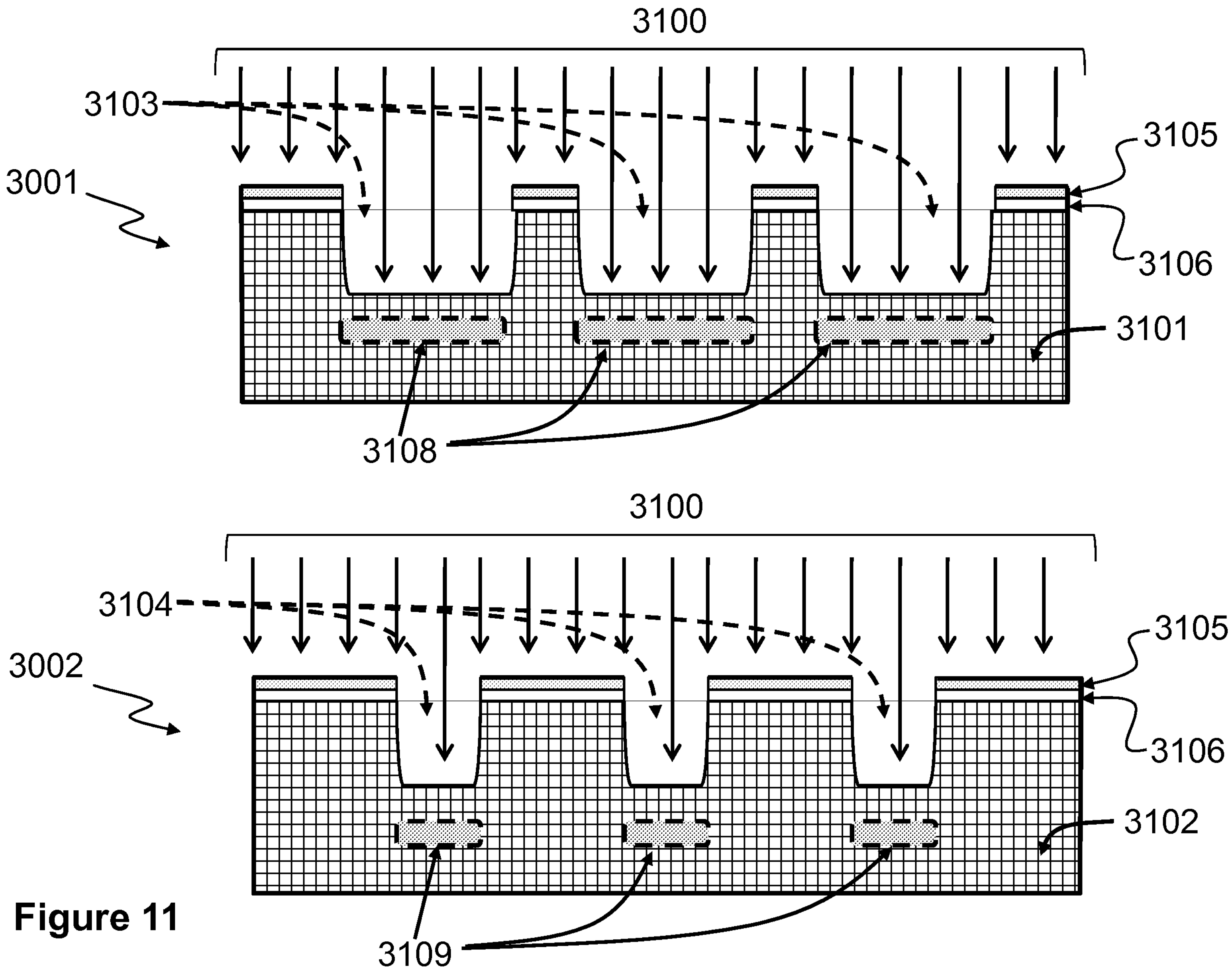

Figure 11

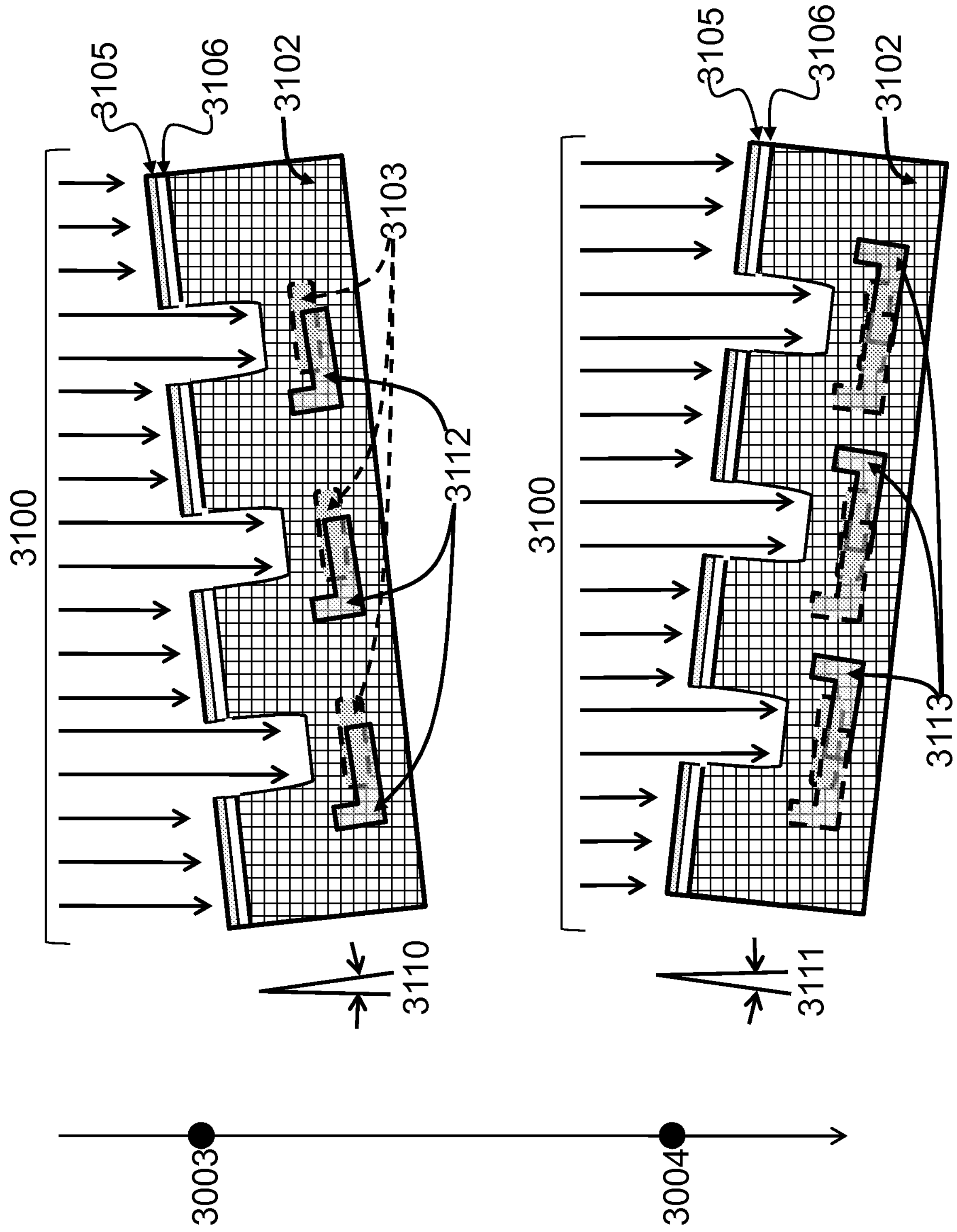

Figure 12

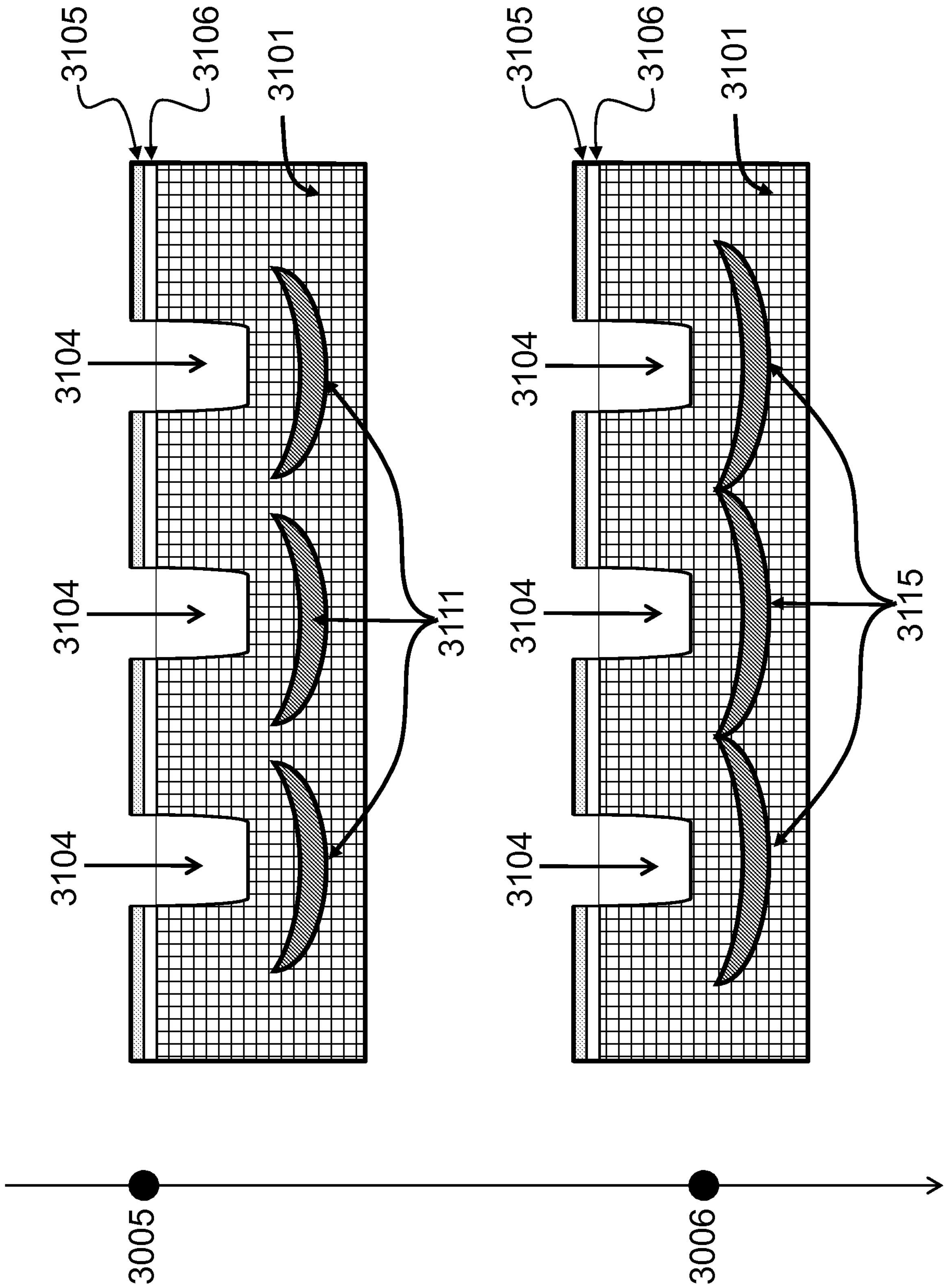

Figure 13

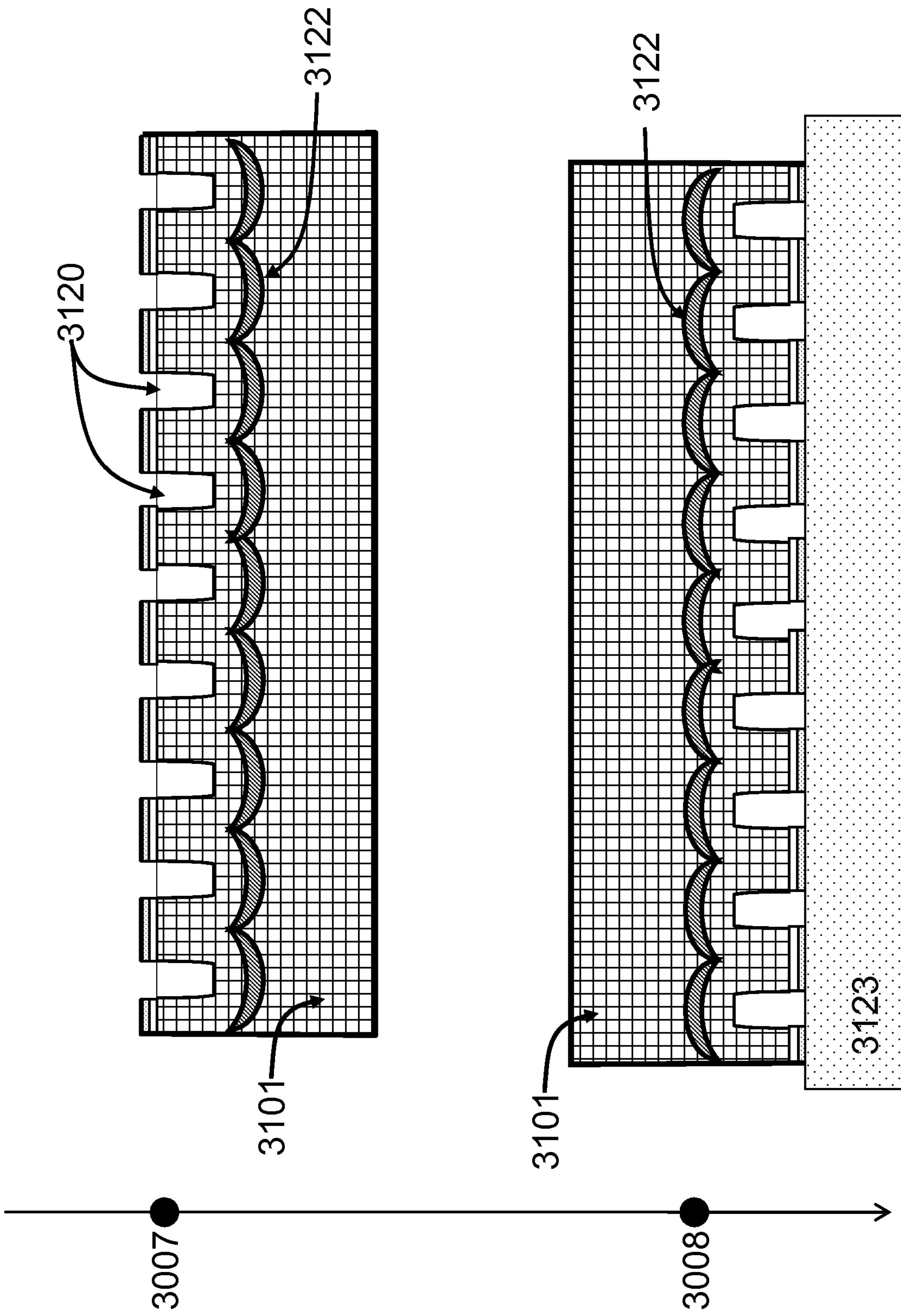

Figure 14

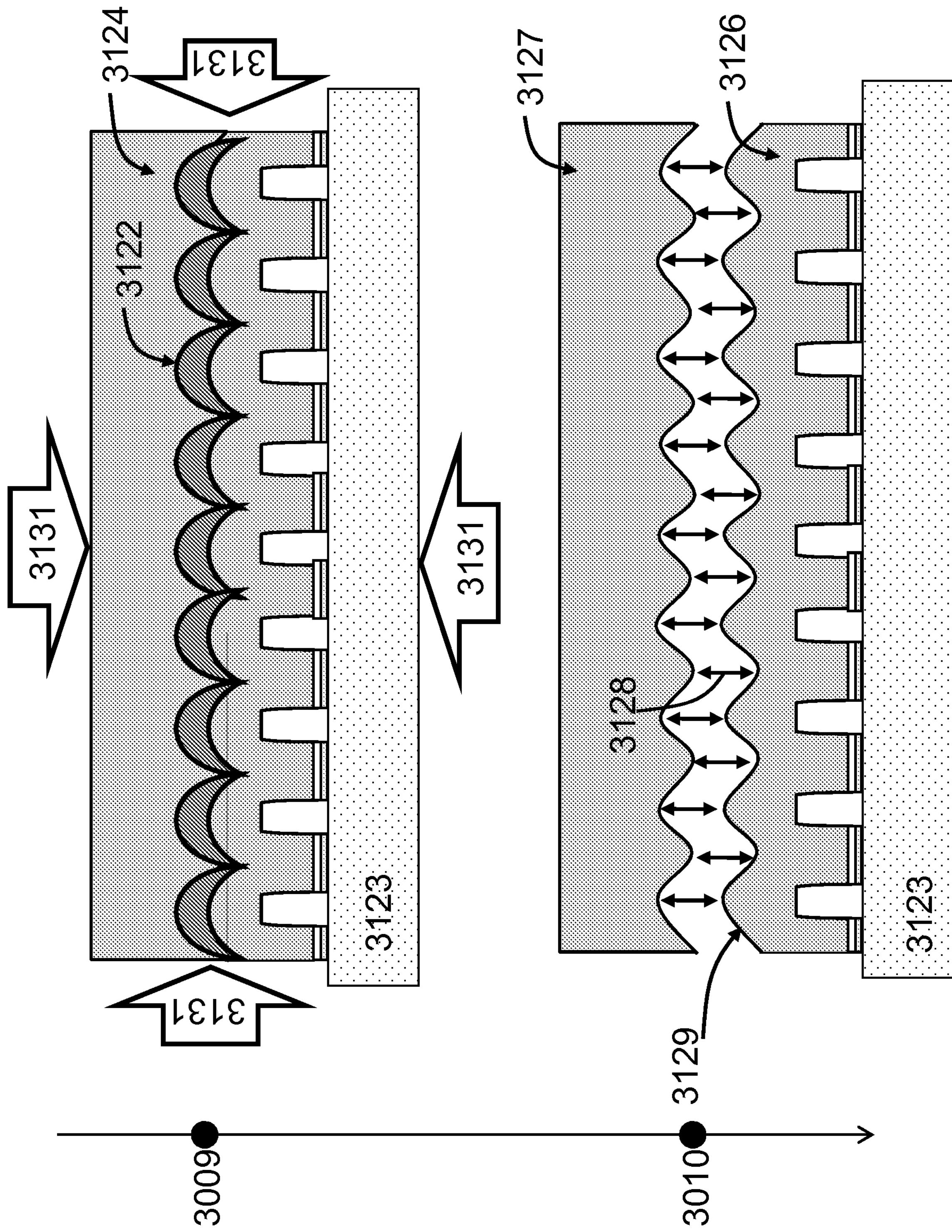

Figure 15

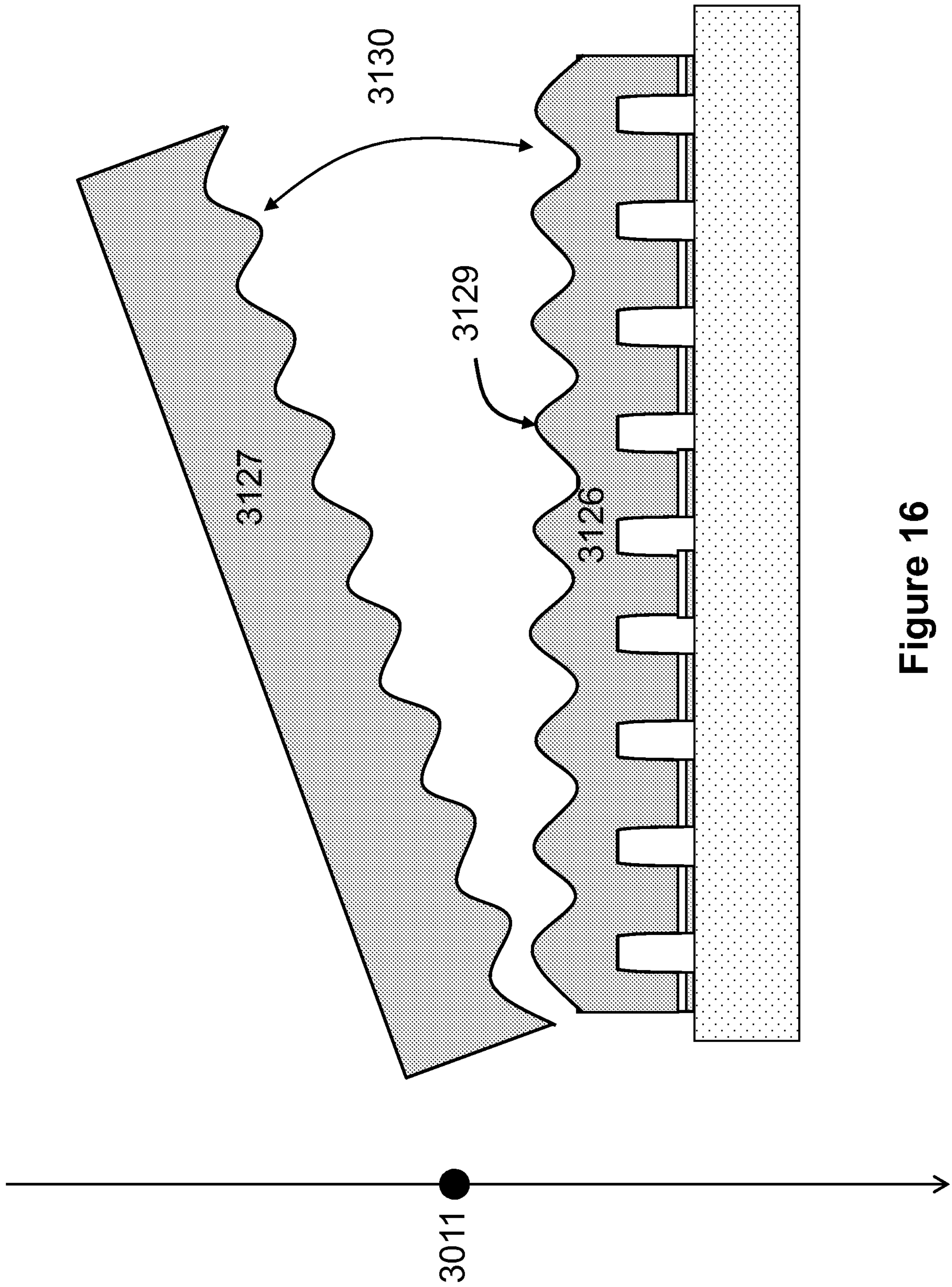

Figure 16

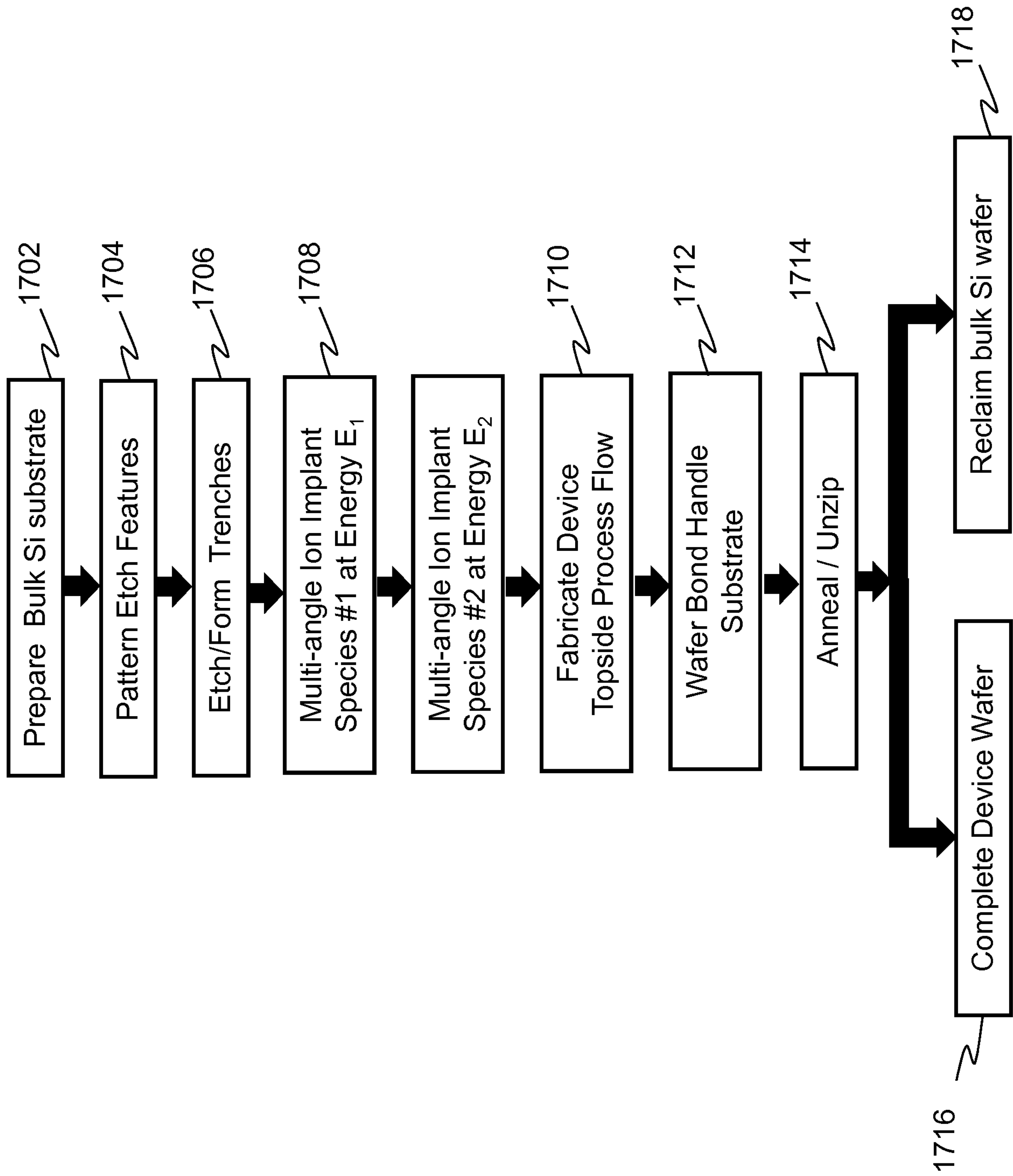

Figure 17

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Figure 18

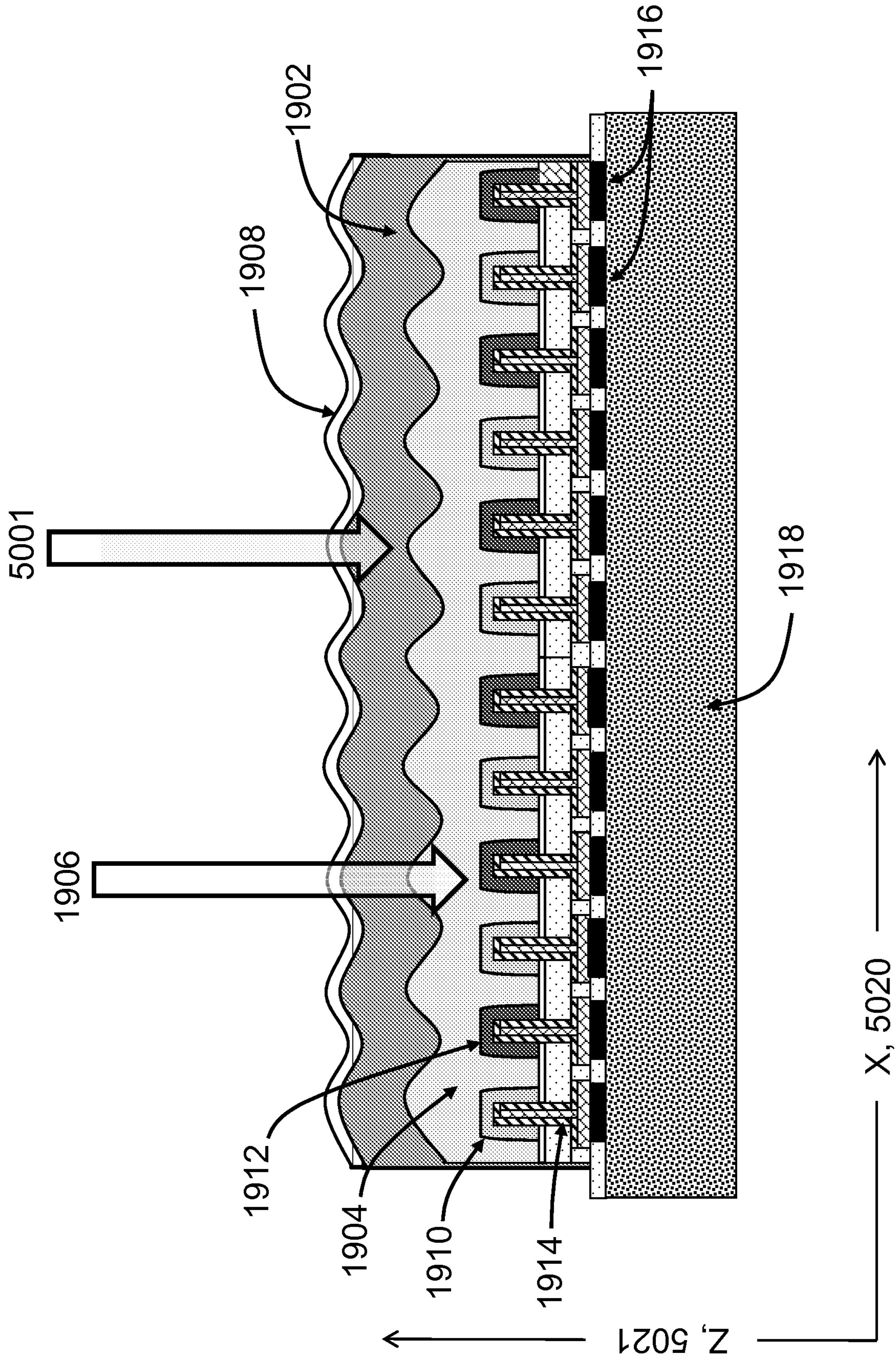


Figure 19

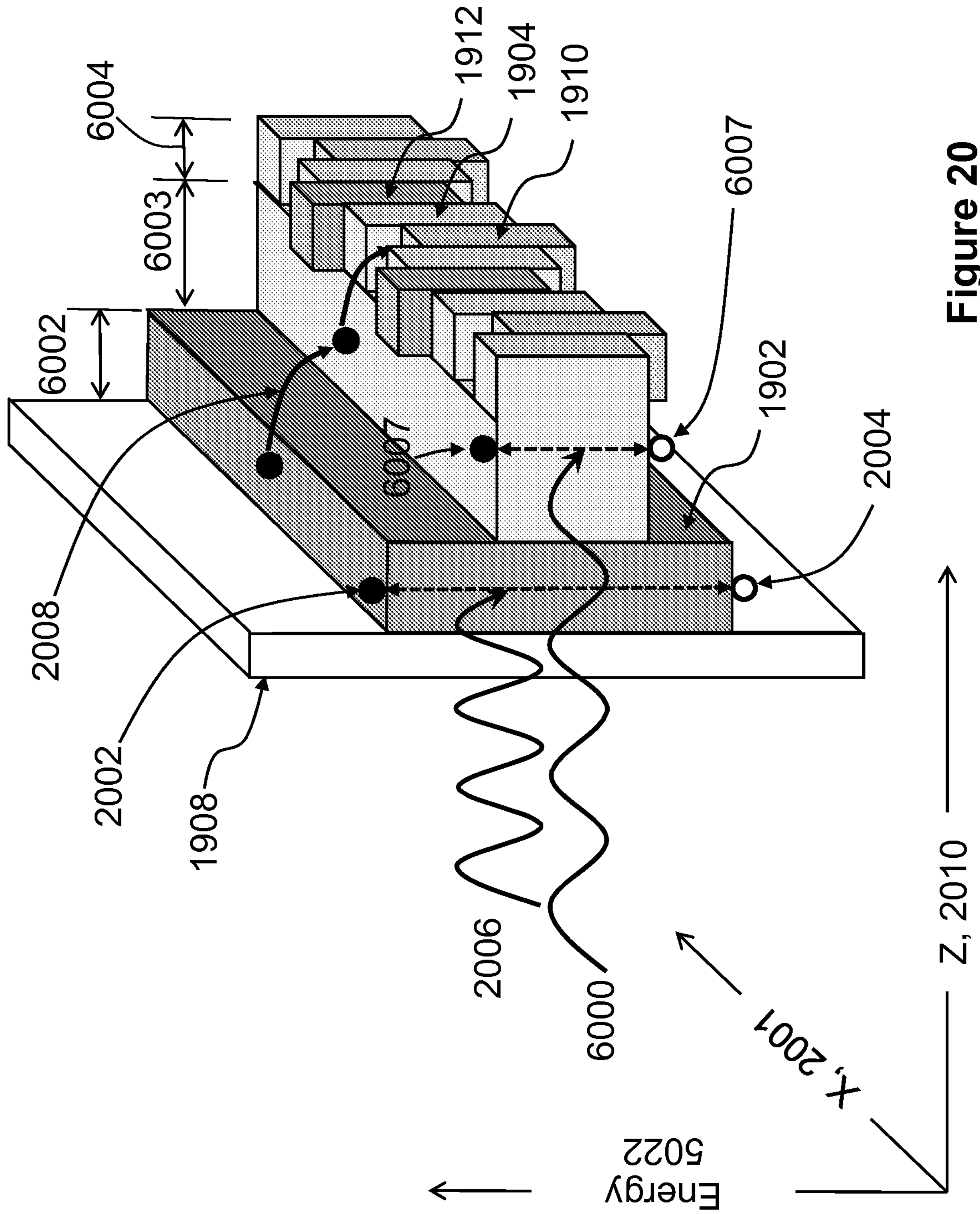


Figure 20

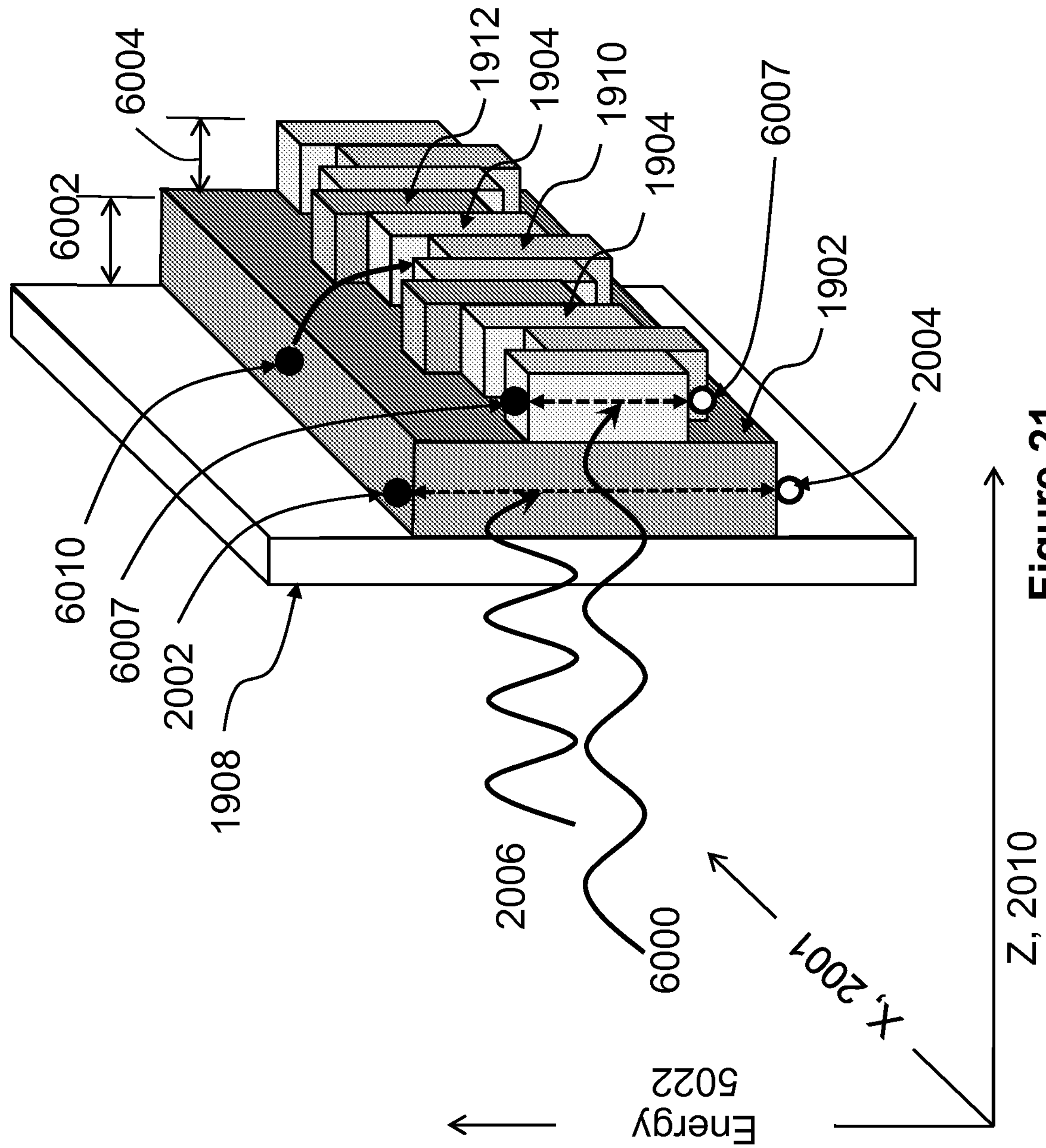


Figure 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051264

A. CLASSIFICATION OF SUBJECT MATTER

H01L 31/18(2006.01)i, H01L 31/042(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 31/18; H01L 31/02; H01L 31/06; B01J 17/00; H01L 31/042

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: interconnect, photovoltaic, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,352,948 A (ROY KAPLOW et al.) 5 October 1982 See column 5, line 22 - column 6, line 17 and figure 4.	10-18
A	US 2011/0120531 A1 (MARTIN NESE et al.) 26 May 2011 See paragraphs [80]-[81] and figure 6.	1-45
A	US 4,131,984 A (ROY KAPLOW et al.) 2 January 1979 See column 8, line 60 - column 11, line 6.	1-45

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 AUGUST 2012 (20.08.2012)	**20 AUGUST 2012 (20.08.2012)**

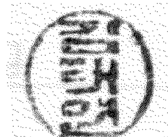
Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Tae Yeon



Telephone No. 82-42-481-8547

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/051264

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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