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# (54) DUAL-FREQUENCY PATCH ANTENNAS

DOPPELFREQUENZ-PATCHANTENNEN

ANTENNES À PLAQUE DE BI-FRÉQUENCE

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- **SEKI T ET AL: "A THREE-DIMENSIONAL ACTIVE ANTENNA FOR A HIGH-SPEED WIRELESS COMMUNICATION APPLICATION", 1997 IEEE MTT-S INTERNATIONAL MICROWAVE SYMPOSIUM DIGEST. DENVER, JUNE 8 - 13, 1997; [IEEE MTT-S INTERNATIONAL MICROWAVE SYMPOSIUM DIGEST], NEW YORK, NY : IEEE, US, 8 June 1997 (1997-06-08), pages 975-978, XP000767662, ISBN: 978-0-7803-3815-9**

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## Description

### FIELD OF THE INVENTION

**[0001]** Embodiments described herein relate generally to dual-frequency patch antennas and methods for forming parts of dual-frequeticy patch antennas using printed circuit board assembly (PCBA) processes.

### BACKGROUND

**[0002]** Patch (or microstrip) antennas typcially include a flat metal sheet mounted over a larger metal ground plane. The flat metal sheet usually has a rectangular shape, and the metal layers are generally separated using a dielectric spacer. The flat metal sheet has a length of approximatley $\lambda/2$, and width can be optimized to provide a desired imput impedance. Patch antennas can be configured to provide linear or circular polarization.

**[0003]** Dual-frequency patch antennas typically include two flat metal sheets mounted over a larger ground plane. Dual-frequency patch antennas exhibit a dual-resonant behavior in a single radiating structure, and they are often used in applications where increased bandwidth is needed or for operating at two separate subbands. Global navigation satellite system (GNSS) receivers often use right-handed circularly polarized (RHCP) dual-frequency patch antennas to receive GNSS signals at different frequencies (e.g., L1, L2, L2C, L3, L4, L5, and other GNSS frequencies).

**[0004]** Patch antennas are popular because of their simple design, low profile, light weight, and low cost. Improved designs are constantly sought to improve performance and further reduce cost.

**[0005]** US 7 277 056 B1 discloses an antenna assembly that includes a first patch antenna and a second patch antenna. The first patch antenna includes a first feed point and is tuned to a first frequency. The second patch antenna includes a second feed point and is tuned to a second frequency.

**[0006]** US 2014/292570 A1 discloses a vehicle-based radio frequency (RF) hardware component that comprises first and second antennas, a digitizer, a serializer, and a serial output.

**[0007]** US 2003/146872 A1 discloses a stacked patch antenna having a plurality of patch antennas having respective operating frequency bands arranged in a stack, each antenna comprising a radiating conductive patch and a first cable comprising a plurality of coaxial conductors separated from each other by dielectric.

**[0008]** WO 99/59223 A2 discloses a dual-band antenna array for use in a base station for mobile telephone communications. The antenna array consists of a first linear array of microstrip or patch antennas for use over the GSM band and a second linear array of crossed dipoles for use over the PCN band.

**[0009]** Seki T et al.: "A Three-Dimensional Active Antenna for a High-Speed Wireless Communication Application", IEEE MTT-S International Microwave Symposium Digest (June, 1997), pages 975-978, discloses a three dimensional active antenna configuration for a front-end module of a high-speed wireless communication system at millimeter and quasi-millimeter-wave frequencies.

**[0010]** US 2003/043086 A1 discloses an antenna system including a Luneburg Lens having a spherically shaped outer surface and a spherically shaped focal surface spaced from its outer surface with a plurality of patch antenna elements disposed along the focal surface of the Luneburg Lens; and a power combiner for combining signals received by said plurality of patch antenna elements.

**[0011]** US 4 070 676 A discloses a multiple resonance microstrip antenna radiator which includes a plurality of stacked electrically conductive element surfaces disposed above an electrically conductive reference surface with each element surface dimensioned so as to resonate at a different radio frequency.

**[0012]** US 6 118 406 A discloses a broadband phased antenna that is comprised of multiple patches which are directly fed.

### SUMMARY

**[0013]** The present invention provides a dual-frequency patch antenna according to claim 1, and a method of forming the same according to claim 10. Preferred embodiments are defined in the dependent claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]**

FIGS. 1A-1E are simplified diagrams of dual-frequency patch antennas in accordance with some examples;

FIGS. 2A-2C are simplified diagrams of a dual-frequency patch antenna in accordance with an example;

FIGS. 3A-3B are simplified diagrams of a dual-frequency patch antenna in accordance with another example;

FIGS. 4A-4C are simplified diagrams of a dual-frequency patch antenna in accordance with another example;

FIGS. 5A-5C are simplified diagrams of a dual-frequency patch antenna in accordance with another example;

FIG. 6 is a simplified cross-sectional view of a dual-frequency patch antenna in accordance with a first embodiment; and

FIGS. 7A-7C are simplified block diagrams showing signal processing operations performed by circuitry of dual-frequency patch antennas and by a processor of a communication device in accordance with some embodiments.

## DETAILED DESCRIPTION

**[0015]** Embodiments described herein provide dual-frequency patch antennas and methods for forming parts of dual-frequency patch antennas using PCBA processes. In some embodiments, a dual-frequency patch antenna that includes circuitry for frequency selection, down conversion, and/or digitization may be formed using a vertical stack of dielectric layers, condutcive layers, and circuitry. One or more of the dielectric layers and conductive layers, as well as the circuitry, may be formed using PCBA processes.

**[0016]** In some embodiments, the circuitry may include elements to filter, amplify, downconvert, and digitize GNSS signals, but may not include elements to perform pseudorange and carrier phase measurements. In these embodiments, the pseudorange and carrier phase measurements, as well as the application of any corrections, may be performed by a communication device that is configured with a software-defined GNSS receiver (soft GNSS receiver). The dual-frequency patch antenna may be removably coupled with the communication device.

**[0017]** The communication device is not limited and may be any device such as a cell phone, a tablet computer, or the like with computing capabilities for processing digitized baseband signals at typical sampling rates. The communication device may be configured in accordance with known techniques to perform conventional GNSS measurements and determine position fixes associated with the dual-frequency patch antenna.

**[0018]** The soft GNSS receiver may run as software on one or more processors that are part of the communication device. A digital cable, such as a USB cable, an Ethernet cable, or the like, may be used to provide digitized baseband signals from the circuitry of the patch antenna to the soft GNSS receiver of the communication device.

**[0019]** FIG. 1A is a simplified perspective view of a dual-frequency patch antenna in accordance with an example. The patch antenna includes a first conductive element 102 configured to receive GNSS signals at a first frequency band and a second conductive element 106 configured to receive GNSS signals at a second frequency band.

**[0020]** A first dielectric material 104 is coupled to a backside of the first conductive element 102, and the second conductive element 106 is coupled to a backside of the first dielectric material 104. A second dielectric material 108 is coupled to a backside of the second conductive element 106. The dielectric materials 104, 108 may be coupled to the conductive elements 102, 106 using known PCBA processes and adhesives.

**[0021]** FIG. 1B is a simplified plan view of the dual-frequency patch antenna shown in FIG. 1A. This figure shows the conductive elements 102, 106 and the dielectric materials 104, 108. In this example, the second conductive element 106 has a topside with an area that is larger than a topside of the first conductive element 102, but in other examples, the second conductive element 106 may have a topside with an area that is approximately the same size as the topside of the first conductive element 102.

**[0022]** As shown in the cross-sectional views of FIGS. 1C-1E, the patch antenna also includes a ground plane 110 coupled to a backside of the second dielectric material 108, a third dielectric material 112 coupled to a backside of the ground plane 110, and a routing and placement layer 114 with circuitry 121 coupled to a backside of the third dielectric layer coupled to a backside of the third dielectric layer. The ground plane 110 typically has a topside with an area at least as large or larger than a topside of the second conductive element 106. In some examples, the second dielectric material 108 has a topside with an area that is at least as large as the topside of the ground plane 110.

**[0023]** The dielectric materials 104, 108, 112 are not limited and may include any solid or laminate dielectric materials such as ceramics, printed circuit board (PCB) cores, pre-preg layers, or the like. Thickness and dielectric constant of the dielectric materials 104, 108 may be determined in accordance with known techniques based on desired operating conditions of the patch antenna (e.g., radiation patterns, coupling between patches, etc.). The dielectric materials 104, 108, 112 may each have the same or different thicknesses and dielectric constants. In some examples, the second dielectric material 108 has a topside with an area that is larger than a topside of the first dielectric material 104.

**[0024]** Although not shown, the third dielectric material 112 may include one or more conductive routing layers each disposed between adjacent dielectric layers (e.g., pre-preg layers). Each of the conductive routing layers may be electrically coupled to other conductive routing layers, the routing and placement layer 114, the circuitry 121, and/or one or more feeds. The routing layers may include vias and/or conductive traces that provide electrical coupling between the circuitry 121 (or components of the circuitry 121) and the first conductive element 102 and/or the second conductive element 106. The electrical coupling is provided via the routing and placement layer 114 and one or more feeds (e.g., feeds 115, 116, 117, 118, 119 - described more fully below).

**[0025]** The conductive elements 102, 106 and the ground plane 110 are not limited and may include any conductive material such as a metal, alloy, or the like. In some examples, the conductive elements 102, 106 and the ground plane 110 may be thin copper sheets that are formed in a desired shape using known PCBA processes and etching techniques. The conductive elements 102, 106 and the ground plane 110 are typically rectangular shaped, but may be other shapes including circular. The size and shape of the conductive elements 102, 106 are determined in accordance with known techniques based on desired operating conditions of the patch antenna (e.g., operating frequencies, bandwidths, input impedances, etc.).

**[0026]** In some examples, the first conductive element 102 is configured to receive L1 GNSS signals and the second conductive element 106 is configured to receive either L2 GNSS signals (where the L2 GNSS signals may be either L2 or L2C GNSS signals), L5 GNSS signals, or any other GNSS signals (e.g., L3 or L4 GNSS signals). The conductive elements 102, 106 are not limited, however, and each conductive clement may be configured to receive signals at any particular GNSS frequency. For example, the second conductive element 106 may be configured to receive L1 GNSS signals, and the first conductive element 102 may be configured to receive signals at another GNSS frequency.

**[0027]** FIGS. 1C-1E are simplified cross-sectional views along line A-A in FIG. 1B and show different examples of dual-frequency patch antennas. Each of the examples shown in FIGS. 1C-1E include the conductive elements 102, 106 and the dielectric materials 104, 108 as shown in FIGS. 1A-1B, as well as the ground plane 110, the third dielectric material 112, the routing and placement layer 114, and the circuitry 121 described above.

**[0028]** The circuitry 121 may include conventional electronic components for providing at least frequency selection of GNSS signals received by the conductive elements 102, 106. In some examples, the circuitry 121 may also include conventional electronic components for providing down conversion of the GNSS signals, and in other examples, the circuitry 121 may also include conventional electronic components for providing down conversion and digitization of the GNSS signals. The electronic components may be mounted on a circuit board in accordance with known techniques. Although not specifically shown in the figures, the electronic components may include one or more known components such as filters, low noise amplifiers (LNAs), down converters, analog to digital (A/D) converters, processors, and/or the like. The one or more processors may be configured to package the GNSS signals for output from the circuitry 121 at output 120. Also, the routing and placement layer 114 may include one or more layers of conductive traces that provide electrical coupling between the components of the circuitry 121 and the conductive elements 102, 106. Although the routing and placement layer 114 shown in these examples is approximately the same size (in cross section) as the ground plane 110, a surface area of the routing and placement layer 114 is not limited and may be either smaller, the same size, or larger than that of the ground plane 110.

**[0029]** The output 120 may provide an interface between the circuitry 121 and a soft GNSS receiver separate from the dual-frequency patch antenna. As described previously, the soft GNSS receiver may run as software on a separate communication device. The output 120 may provide the GNSS signals using known wireless techniques (e.g., Bluetooth) or via a digital cable 122 as shown in FIG. 1C. The digital cable may include a USB cable (e.g., USB 2.0 high speed, USB 3.0, etc.), an Ethernet cable, of the like, and may be used to provide the GNSS signals from the circuitry 121 of the patch antenna to the soft GNSS receiver of the communication device. Although not specifically shown in some of the figures, each of the examples of dual-frequency patch antennas described herein may provide the GNSS signals from the circuitry either wirelessly or via a digital cable. Depending on the example the GNSS signals output from the circuitry 121 may be either frequency selected and amplified GNSS signals; frequency selected, amplified, and downconverted GNSS signals; or frequency selected, amplified, downconverted, and digitized GNSS signals (digitized baseband signals).

**[0030]** The examples shown in FIGS. 1C-1E also include one or more feeds (feeds 115, 116, 117, 118, 119). The feeds are for electrically coupling the circuitry 121 to the first conductive element 102 and/or the second conductive element 106 via the routing and placement layer 114. For example, the example shown in FIG. 1C includes a first feed 115 coupling the circuitry 121 to the second conductive clement 106 and a second feed 116 coupling the circuitry 121 to the first conductive element 102. The feeds 115, 116 provide energy from the conductive elements 102, 106 to the circuitry 121.

**[0031]** The example shown in FIG. 1D includes a first feed 117 coupling the circuitry 121 to the second conductive element 106 and a second feed 118 coupling the circuitry 121 to the first conductive element 102. In this example, the feeds 117, 118 terminate in the third dielectric material 112 and are coupled to the circuitry 121 by one or more routing layers (not shown).

**[0032]** The example shown in FIG. IE includes a single feed 119 coupling the circuitry 121 to the first conductive element 102. While the second conductive element 106 is electrically isolated from the circuitry 121 in this example, the second conductive element is capacitively coupled to the first conductive element 102 (and hence capacitively coupled to the circuitry 121). In other examples, a single feed may be used in a similar manner to couple the circuitry 121 to the second conductive clement 106 leaving the first conductive element 102 electrically isolated from, but capacitively coupled to, the circuitry 121. Polarization of the dual-frequency patch antenna may be determined in accordance with known techniques based on feed location on the conductive elements 102, 106.

**[0033]** The feeds 115, 116, 117, 118, 119 arc shown merely as examples of some of the feed configurations that may be used with examples of dual-frequency patch antennas described herein. The dual-frequency patch antennas described herein, however, are not limited to these or any other feed configurations. For example, one or both of the conductive elements may have dual feeds in some embodiments. Further, many details associated with the feeds are not included in the figures. For example, the feeds typically pass through a hole or aperture in the ground plane that provides isolation from the ground plane. Also, the feeds that are coupled to the top conductive element (the first conductive element 102) may pass through a hole or aperture in the bottom conductive element (the second conductive element 106) that provides isolation from the bottom conductive element. Additionally, the feeds may be coupled with the conductive elements at different locations in accordance with known techniques based on desired polarization characteristics. Also, the feeds may be coupled at various points (e.g., top or bottom) of the conductive elements and the routing and placement layer, and the feeds may extend horizontally before extending vertically through the dielectric layers or even wrap around the dielectric layers in some embodiments. Thus, the examples shown in FIGS. 1C-1E merely provide some of the general feed configurations that may be used with the embodiments of dual-frequency patch antennas that are within the scope of this disclosure. And while all of the examples may include feeds, the feeds are not specifically shown in any of the other figures.

**[0034]** FIGS. 2A-2C are simplified diagrams of a dual-frequency patch antenna in accordance with an example. These figures show a first conductive element 202, a first dielectric material 204, a second conductive element 206, and a second dielectric material 208. FIG. 2C, which is a cross-sectional view along line B-B in FIG. 2B, also shows a ground plane 210, a third dielectric material 212, routing and placement layer 114, circuitry 221, and an output 220. Each of the layers and/or components may include features similar to those described above with regard to FIGS. 1A-1E. As can be seen from the dotted line in FIG. 2A, and in the cross section of FIG. 2C, the second conductive element 206 in this example is approximately the same size as the first conductive element 202. The sizes of the first conductive element 202 and the second conductive element 206 may be determined in accordance with known techniques and may depend at least in part on dielectric constants of the dielectric materials 204, 206.

**[0035]** FIGS. 3A-3B are sitnplified diagrams of a dual-frequency patch antenna in accordance with another example. In this example, edges of a first conductive clement 302 and a first dielectric material 304 are rotated relative to edges of a second conductive element 306 and a second dielectric material 308. Rotation can provide improved isolation between the conductive elements 302, 306 in some configurations and operating conditions. In some examples, the first conductive element 302 and the first dielectric material 304 may be rotated by about 45° (or between about 30° and 60°). Also, the first conductive element 302 and the first dielectric material 304 may be larger than shown in FIGS. 3A-3B, so that corners of the first conductive element 302 and the first dielectric material 304 extend past edges of the second conductive element 306. Although not specifically shown, this example may also include a ground plane, third dielectric material, routing and placement layer, circuitry, and output similar the examples shown in FIGS. 1C-1E and FIG. 2C. Each of the layers and/or components may include features similar to those described above with regard to FIGS. 1A-1E.

**[0036]** FIGS. 4A-4C are simplified diagrams of a dual-frequency patch antenna in accordance with another example. These figures show a first conductive element 402, a first dielectric material 404, a second conductive element 406, and a second dielectric material 408. FIG. 4C, which is a cross-sectional view along line C-C in FIG. 4B, also shows a ground plane 410, a third dielectric material 412, routing and placement layer 414, circuitry 421, and an output 420. In this example, a first dielectric material 404 is approximately the same size as a second dielectric material 408. Also, as shown by the dotted line in FIGS. 4A-4B, the first conductive element 402 is smaller than the second conductive element 404 in this example, although as described with regard to other embodiments, the conductive elements 402, 406 may be approximately the same size. Each of the layers and/or components may include features similar to those described above with regard to FIGS. 1A-1E.

**[0037]** FIGS. 5A-5C are simplified diagrams of a dual-frequency patch antenna in accordance with another example. These figures show a conductive element 524 and a top dielectric material 504. FIG. 5C, which is a cross-sectional view along line D-D in FIG. 5B, also shows a ground plane 510, a bottom dielectric material 512, routing and placement layer 514, circuitry 521, and an output 520. Each of the layers and/or components may include features similar to those described above with regard to FIGS. 1A-1E. For example, the bottom dielectric material 512 may include one or more conductive routing layers each disposed between adjacent dielectric layers as described above with regard to the third dielectric material 112 in FIGS. 1C-1E. In this example, the conductive clement 524 is configured in accordance with known techniques to receive GNSS signals at both a first frequency band and a second frequency band. One advantage of this example is a lower height (because one dielectric layer and one conductive layer are eliminated). This can also reduce weight and cost.

**[0038]** FIG. 6 is a simplified cross-sectional view of a patch antenna in accordance with a first embodiment. This embodiment includes a first conductive element 602, a first dielectric material 604, a second conductive element 606, a second dielectric material 608, a ground plane 610, and a third dielectric material 612. Each of the layers may include features similar to those described above with regard to FIGS. 1A-1E. This embodiment also includes a first routing and placement layer 626, first circuitry 626, a second routing and placement layer 632, and second circuitry 632 coupled via an interface 630. The interface 630 may be, for example, a cable or trace configured to convey RF signals. Similar to the circuitry

121 described above with regard to FIGS. 1C-1E, the first circuitry 626 and the second circuitry 632 may include conventional electronic components for providing frequency selection, down conversion, and digitization of GNSS signals received by the first conductive element 602 and the second conductive element 606.

**[0039]** In some embodiments, the first circuitry 626 may be configured to provide amplified and filtered GNSS signals to the second circuitry 632, and the second circuitry 632 may be configured to provide down conversion and digitization of the amplified and filtered GNSS signals.

**[0040]** In other embodiments, the first circuitry 626 may be configured to provide amplified, filtered, and down converted GNSS signals to the second circuitry 632, and the second circuitry 632 may be configured to provide digitization of the amplified, filtered, and down converted GNSS signals.

**[0041]** In either case, digitized baseband signals may be provided at an output 634 for wireless or wired transmission. Wired transmission may be via a digital cable as described previously. The digitized baseband signals may be transmitted to a soft GNSS receiver on a communication device for typical GNSS measurements and determination of position fixes associated with the dual-frequency patch antenna.

**[0042]** This embodiment may allow for the first routing and placement layer 626 and first circuitry 626 to be smaller than the routing and placement layer with circuitry described above with regard to FIGS. 1C-1E (and thus reduce a size, weight, and/or cost of the dual-frequency patch antenna), and it may also allow for some of the GNSS signal processing to be performed at the second circuitry 632 that may be located in a more convenient location. The second routing and placement layer 632 with the second circuitry 632 may be located within the same housing as the first routing and placement layer 626 with the first circuitry 626 (part of the same device) or in a different housing (part of a different device).

**[0043]** At least a portion of each of the embodiments of dual-frequency patch antennas described herein may be formed using known PCBA processes, and in some embodiments, the entire dual-frequency patch antenna may be formed using PCBA processes. For example, with regard to FIGS. 1A-1E, the first conductive layer 102, the second conductive layer 106, the ground plane 110, and/or the routing and placement layer 114 (and/or part of the circuitry) may be formed from thin metal layers commonly used in PCBA processes. The various shapes and sizes of the conductive layers may be formed using known PCBA etching processes. Electronic components, including the output 120, may be mounted on the routing and placement layer 114 using known PCBA surface mount processes.

**[0044]** Also, the first dielectric layer 104, the second dielectric layer 108, and/or the third dielectric layer 112 may be formed from PCB cores or pre-preg layers using known PCBA processes. One or more feeds may be formed extending through one or more of the dielectric materials 104, 108, 112 and connecting to one or more conductive layers using known PCBA via etching and plating techniques.

**[0045]** FIGS. 7A-7C are simplified block diagrams showing signal processing operations performed by circuitry of dual-frequency patch antennas and by a processor of a communication device in accordance with some embodiments. For example, FIG. 7A shows in block diagram a dual-frequency patch antenna that includes two conductive elements 740, 742 for reception of signals at different GNSS frequencies. Frequency selection, down conversion, and digitization operations 744 are performed by circuitry of the dual-frequency patch antenna. Digitized baseband signals are output either wirelessly or via a digital cable 746. Processing of the digitized baseband signals at operation 748 is performed by one or more processors of a communication device.

**[0046]** FIG. 7B also shows in block diagram a dual-frequency patch antenna that includes two conductive elements 740, 742 for reception of signals at different GNSS frequencies. Frequency selection operations 752 arc performed by first circuitry, and down conversion and digitization operations 754 are performed by second circuitry. The first circuitry may be part of the dual-frequency patch antenna, and the second circuitry may be part of the dual-frequency patch antenna or it may be located separately. The first and second circuitry are coupled via an RF cable 750. Digitized baseband signals are output from the second circuitry either wirelessly or via a digital cable 746. Processing of the digitized baseband signals at operation 748 is performed by one or more processors of a communication device.

**[0047]** FIG. 7C also shows in block diagram a dual-frequency patch antenna that includes two conductive elements 740, 742 for reception of signals at different GNSS frequencies. Frequency selection and down conversion operations 756 are performed by first circuitry, and digitization operations 758 are performed by second circuitry. The first circuitry may be part of the dual-frequency patch antenna, and the second circuitry may be part of the dual-frequency patch antenna or it may be located separately. The first and second circuitry are coupled via an RF cable 750. Digitized baseband signals are output from the second circuitry either wirelessly or via a digital cable 746. Processing of the digitized baseband signals at operation 748 is performed by one or more processors of a communication device.

**[0048]** It should be appreciated that the specific steps illustrated in FIGS. 7A-7C provide particular operations and sequences according to some embodiments. Other operations and/or sequences may also be performed according to alternative embodiments. For example, alternative embodiments may perform the operations outlined above in a different order. Moreover, the individual operations illustrated in FIGS. 7A-7C may include multiple sub-steps that may be performed in various sequences. Furthermore, additional operations may be added or removed depending on the particular application.

**[0049]** It should be appreciated that some embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware, or microcode, the program code or code segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may be adapted to perform the necessary tasks. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, sim cards, other smart cards, and various other non-transitory mediums capable of storing, containing, or carrying instructions or data.

**[0050]** While the present invention has been described in terms of specific embodiments, it should be apparent to those skilled in the art that the scope of the present invention is not limited to the embodiments described herein. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. Thus, the scope of the present invention should be determined not with reference to the above description, but should be determined with reference to the appended claims.

## Claims

1. A dual-frequency patch antenna comprising:

   a first conductive element (602) configured to receive global navigation satellite system, GNSS, signals at a first frequency band;
   a second conductive element (606) configured to receive GNSS signals at a second frequency band;
   a ground plane (610);
   a first dielectric material (604) disposed between the first conductive element and the second conductive element;
   a second dielectric material (608) disposed between the second conductive element and the ground plane, the second dielectric material having a topside with an area at least as large as the topside of the ground plane; **characterised in that** the antenna further comprises
   circuitry (627; 631) electrically coupled to at least one of the first conductive element or the second conductive element, the circuitry configured to provide at least frequency selection of the GNSS signals at the first frequency band and the GNSS signals at the second frequency band; and
   a third dielectric material (612) disposed between the ground plane and the circuitry; and
   an output (634) coupled to the circuitry; wherein the circuitry comprises first circuitry (627) on a first routing and placement layer (626) and second circuitry (631) on a second routing and placement layer (632), the output (634) being coupled to the second routing and placement layer;
   the first circuitry being configured to provide amplified and filtered GNSS signals to the second circuitry, and the second circuitry being configured to provide digitization of the amplified and filtered GNSS signals, and either the first or the second circuitry being configured to provide down conversion of the GNSS signals;
   the dual-frequency patch antenna further comprising an interface (630) coupled to the first circuitry via the first routing and placement layer and to the second circuitry via the second routing and placement layer, the interface being configured to provide filtered, amplified, and optionally down converted GNSS signals from the first circuitry to the second circuitry, and the second circuitry being configured to provide the digitized baseband signals to the output.

2. The dual-frequency patch antenna of claim 1, wherein the circuitry includes elements to filter, amplify, downconvert, and digitize the GNSS signals at the first frequency band and the GNSS signals at the second frequency band, but does not include elements to perform pseudorange and carrier phase measurements.

3. The dual-frequency patch antenna of claim 1, further comprising one or more feeds electrically coupling the first conductive element to the circuitry.

4. The dual-frequency patch antenna of claim 3, wherein the second conductive element is electrically isolated from the circuitry and is capacitively coupled to the first conductive element.

5. The dual-frequency patch antenna of claim 1, wherein the first dielectric material has a topside with an area that is substantially the same size as the topside of the second dielectric material.

6. The dual-frequency patch antenna of claim 1, wherein the third dielectric material comprises one or more conductive routing layers each disposed between adjacent dielectric layers.

7. The dual-frequency patch antenna of any one of the preceding claims, wherein the first circuitry with the first routing and placement layer and the second circuitry with the second routing and placement layer are located at different locations.

8. The dual-frequency patch antenna of claim 7, wherein the first circuitry with the first routing and placement layer and the second circuitry with the second

routing and placement layer are located within the same housing.

**9.** The dual-frequency patch antenna of claim 7, wherein the first circuitry with the first routing and placement layer and the second circuitry with the second routing and placement layer are located in different housings.

**10.** A method of forming a dual-frequency patch antenna as defined in any one of the preceding claims, wherein
the first conductive layer, the second conductive layer, the ground plane, and/or the first routing and placement layer is/are formed from thin metal layers in a printed circuit board assembly, PCBA, process;
shapes and sizes of the conductive layers are formed using PCBA etching processes; and
electronic components are mounted on the first routing and placement layer using a PCBA surface mount process.

**11.** The method of claim 10, wherein
the first dielectric layer, the second dielectric layer and/or the third dielectric layer is formed from printed circuit board, PCB, cores or pre-preg layers using a PCBA process; and
one or more feeds, extending through one or more of the dielectric materials and connecting to one or more of the conductive layers, are formed using PCBA etching and plating techniques.

## Patentansprüche

**1.** Doppelfrequenz-Patchantenne, umfassend:

ein erstes leitfähiges Element (602), welches dafür konfiguriert ist, auf einem ersten Frequenzband Signale des Global Navigation Satellite System, GNSS, zu empfangen;
ein zweites leitfähiges Element (606), welches dafür konfiguriert ist, auf einem zweiten Frequenzband GNSS-Signale zu empfangen;
eine Masseebene (610);
ein erstes Dielektrikumsmaterial (604), welches zwischen dem ersten leitfähigen Element und dem zweiten leitfähigen Element angeordnet ist;
ein zweites Dielektrikumsmaterial (608), welches zwischen dem zweiten leitfähigen Element und der Masseebene angeordnet ist, wobei das zweite Dielektrikumsmaterial eine Oberseite mit einer Fläche aufweist, die mindestens so groß wie die Oberseite der Masseebene ist;
**dadurch gekennzeichnet, dass** die Antenne ferner umfasst:

ein Schaltungssystem (627; 631), welches mit mindestens einem aus dem ersten leitfähigen Element und dem zweiten leitfähigen Element elektrisch verbunden ist, wobei das Schaltungssystem dafür konfiguriert ist, zumindest für eine Frequenzauswahl der GNSS-Signale auf dem ersten Frequenzband und der GNSS-Signale auf dem zweiten Frequenzband zu sorgen; und
ein drittes Dielektrikumsmaterial (612), welches zwischen der Masseebene und dem Schaltungssystem angeordnet ist; und
einen Ausgang (634), der mit dem Schaltungssystem verbunden ist; wobei
das Schaltungssystem ein erstes Schaltungssystem (627) auf einer ersten Führungs- und Anordnungsschicht (626) und ein zweites Schaltungssystem (631) auf einer zweiten Führungs- und Anordnungsschicht (632) umfasst, wobei der Ausgang (634) mit der zweiten Führungs- und Anordnungsschicht verbunden ist;
das erste Schaltungssystem dafür konfiguriert ist, dem zweiten Schaltungssystem verstärkte und gefilterte GNSS-Signale bereitzustellen, und das zweite Schaltungssystem dafür konfiguriert ist, für eine Digitalisierung der verstärkten und gefilterten GNSS-Signale zu sorgen, und entweder das erste oder das zweite Schaltungssystem dafür konfiguriert ist, für eine Abwärtsumsetzung der GNSS-Signale zu sorgen;
die Doppelfrequenz-Patchantenne ferner eine Schnittstelle (630) umfasst, die über die erste Führungs- und Anordnungsschicht mit dem ersten Schaltungssystem und über die zweite Führungs- und Anordnungsschicht mit dem zweiten Schaltungssystem verbunden ist, wobei die Schnittstelle dafür konfiguriert ist, dem zweiten Schaltungssystem gefilterte, verstärkte und gegebenenfalls abwärtsumgesetzte GNSS-Signale aus dem ersten Schaltungssystem bereitzustellen, und das zweite Schaltungssystem dafür konfiguriert ist, dem Ausgang die digitalisierten Basisbandsignale bereitzustellen.

**2.** Doppelfrequenz-Patchantenne nach Anspruch 1, wobei das Schaltungssystem Elemente zum Filtern, Verstärken, Abwärtsumsetzen und Digitalisieren der GNSS-Signale auf dem ersten Frequenzband und der GNSS-Signale auf dem zweiten Frequenzband umfasst, aber keine Elemente zum Durchführen von Pseudostrecken- und Trägerphasenmessungen umfasst.

**3.** Doppelfrequenz-Patchantenne nach Anspruch 1, ferner umfassend eine oder mehrere Zuführungen, welche das erste leitfähige Element mit dem Schaltungssystem verbinden.

**4.** Doppelfrequenz-Patchantenne nach Anspruch 3, wobei das zweite leitfähige Element von dem Schaltungssystem elektrisch isoliert ist und mit dem ersten leitfähigen Element kapazitiv verbunden ist.

**5.** Doppelfrequenz-Patchantenne nach Anspruch 1, wobei das erste Dielektrikumsmaterial eine Oberseite mit einer Fläche aufweist, die im Wesentlichen gleich groß ist wie die Oberseite des zweiten Dielektrikumsmaterials.

**6.** Doppelfrequenz-Patchantenne nach Anspruch 1, wobei das dritte Dielektrikumsmaterial eine oder mehrere leitfähige Führungsschichten umfasst, die jeweils zwischen benachbarten Dielektrikumsschichten angeordnet sind.

**7.** Doppelfrequenz-Patchantenne nach einem der vorhergehenden Ansprüche, wobei das erste Schaltungssystem mit der ersten Führungs- und Anordnungsschicht und das zweite Schaltungssystem mit der zweiten Führungs- und Anordnungsschicht an verschiedenen Stellen angeordnet sind.

**8.** Doppelfrequenz-Patchantenne nach Anspruch 7, wobei das erste Schaltungssystem mit der ersten Führungs- und Anordnungsschicht und das zweite Schaltungssystem mit der zweiten Führungs- und Anordnungsschicht in demselben Gehäuse angeordnet sind.

**9.** Doppelfrequenz-Patchantenne nach Anspruch 7, wobei das erste Schaltungssystem mit der ersten Führungs- und Anordnungsschicht und das zweite Schaltungssystem mit der zweiten Führungs- und Anordnungsschicht in verschiedenen Gehäusen angeordnet sind.

**10.** Verfahren zur Herstellung einer Doppelfrequenz-Patchantenne nach einem der vorhergehenden Ansprüche, wobei
die erste leitfähige Schicht, die zweite leitfähige Schicht, die Masseebene und/oder die erste Führungs- und Anordnungsschicht in einem Leiterplatten-Zusammenbauverfahren (Printed Circuit Board Assembly, PCBA) aus dünnen Metallschichten gebildet werden;
Formen und Größen der leitfähigen Schichten durch PCBA-Ätzverfahren gebildet werden; und
elektronische Komponenten über ein PCBA-Oberflächenmontageverfahren auf der ersten Führungs- und Anordnungsschicht montiert werden.

**11.** Verfahren nach Anspruch 10, wobei
die erste Dielektrikumsschicht, die zweite Dielektrikumsschicht und/oder die dritte Dielektrikumsschicht über ein PCBA-Verfahren aus Leiterplatten(PCB)-Kernen oder Prepreg-Schichten gebildet werden; und
eine oder mehrere Zuführungen, die sich durch eines oder mehrere der Dielektrikumsmaterialien erstrecken und mit einer oder mehreren der leitfähigen Schichten verbinden, über PCBA-Ätz- und -Plattierungstechniken gebildet werden.

## Revendications

**1.** Antenne à plaque de bi-fréquence comprenant :

un premier élément conducteur (602) configuré pour recevoir des signaux de système satellite de navigation global, GNSS, à une première bande de fréquence ;
un deuxième élément conducteur (606) configuré pour recevoir des signaux GNSS à une deuxième bande de fréquences ;
un plan de sol (610) ;
un premier matériau diélectrique (604) disposé entre le premier élément conducteur et le deuxième élément conducteur ;
un second matériau diélectrique (608) disposé entre le deuxième élément conducteur et le plan de sol, le second matériau diélectrique ayant une face supérieure avec une aire au moins aussi grande que la face supérieure du plan de sol ;
**caractérisé en ce que** l'antenne comprend en outre
une circuiterie (627 ; 631) couplée électriquement à au moins un du premier élément conducteur ou du deuxième élément conducteur, la circuiterie configurée pour fournir au moins une sélection de fréquence des signaux GNSS à la première bande de fréquence et des signaux GNSS à la deuxième bande de fréquence ; et
un troisième matériau diélectrique (612) disposé entre le plan de sol et la circuiterie ; et
une sortie (634) couplée à la circuiterie ; dans laquelle
la circuiterie comprend une première circuiterie (627) sur une première couche d'acheminement et de placement (626) et une deuxième circuiterie (631) sur une deuxième couche d'acheminement et de placement (632), la sortie (634) étant couplée à la deuxième couche d'acheminement et de placement ;
la première circuiterie étant configurée pour fournir des signaux GNSS amplifiés et filtrés à la deuxième circuiterie, et la deuxième circuiterie étant configurée pour fournir une numérisation des signaux GNSS amplifiés et filtrés, et soit la première soit la deuxième circuiterie étant

configurée pour une transposition par abaissement de fréquence des signaux GNSS ;
l'antenne à plaque de bi-fréquence comprenant en outre une interface (630) couplée à la première circuiterie par la première couche d'acheminement et de placement et à la deuxième circuiterie par la deuxième couche d'acheminement et de placement, l'interface étant configurée pour fournir des signaux GNSS filtrés, amplifiés et en option transposés par abaissement de fréquence de la première circuiterie vers la deuxième circuiterie, et la deuxième circuiterie étant configurée pour fournir les signaux de bande de base numérisés vers la sortie.

**2.** Antenne à plaque de bi-fréquence selon la revendication 1, dans laquelle la circuiterie inclut des éléments pour filtrer, amplifier, transposer par abaissement de fréquence et numériser les signaux GNSS à la première bande de fréquence et les signaux GNSS à la deuxième bande de fréquence mais n'inclut pas d'éléments pour exécuter des mesures de pseudo-distance et de phase de la porteuse.

**3.** Antenne à plaque de bi-fréquence selon la revendication 1, comprenant en outre une ou plusieurs alimentations couplant le premier élément conducteur à la circuiterie.

**4.** Antenne à plaque de bi-fréquence selon la revendication 3, dans laquelle le deuxième élément conducteur est isolé électriquement de la circuiterie et est couplé de manière capacitive au premier élément conducteur.

**5.** Antenne à plaque de bi-fréquence selon la revendication 1, dans laquelle le premier matériau diélectrique a une face supérieure avec une aire qui est essentiellement de la même taille que la face supérieure du deuxième matériau diélectrique.

**6.** Antenne à plaque de bi-fréquence selon la revendication 1, dans laquelle le troisième matériau diélectrique comprend une ou plusieurs couche(s) d'acheminement conductrice(s) disposées chacune entre des couches diélectriques adjacentes.

**7.** Antenne à plaque de bi-fréquence selon l'une quelconque des revendications précédentes, dans laquelle la première circuiterie avec la première couche d'acheminement et de placement et la seconde circuiterie avec la deuxième couche d'acheminement et de placement sont situées à différents emplacements.

**8.** Antenne à plaque de bi-fréquence selon la revendication 7, dans laquelle la première circuiterie avec la première couche d'acheminement et de placement et la seconde circuiterie avec la deuxième couche d'acheminement et de placement sont situées à l'intérieur du même logement.

**9.** Antenne à plaque de bi-fréquence selon la revendication 7, dans laquelle la première circuiterie avec la première couche d'acheminement et de placement et la seconde circuiterie avec la deuxième couche d'acheminement et de placement sont situées dans différents logements.

**10.** Procédé de formation d'une antenne à plaque de bi-fréquence tel que défini dans l'une quelconque des revendications précédentes, dans laquelle
la première couche conductrice, la deuxième couche conductrice, le plan de sol et/ou la première couche d'acheminement et de placement sont est/sont formé(e)(s) de fines couches métalliques dans un procédé d'ensemble de carte de circuit imprimé PCBA ;
des formes et tailles des couches conductrices sont formées en utilisant des procédés de gravure PCBA ; et
des composants électroniques sont montés sur la première couche d'acheminement et de placement en utilisant un procédé de montage de surface PCBA.

**11.** Procédé selon la revendication 10, dans lequel
la première couche diélectrique, la deuxième couche diélectrique et/ou la troisième couche diélectrique est formée de noyaux ou de couches pré-imprégnées de carte de circuit imprimé, PCB en utilisant un procédé PCBA ; et
une ou plusieurs alimentation(s), s'étendant à travers un ou plusieurs des matériaux diélectriques et se connectant à une ou plusieurs des couches conductrices, est/sont formée(s) en utilisant des techniques de gravure et de plaquage PCBA.

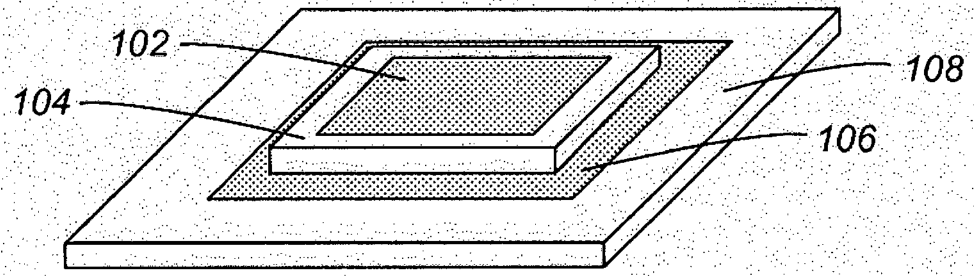

FIG. 1A

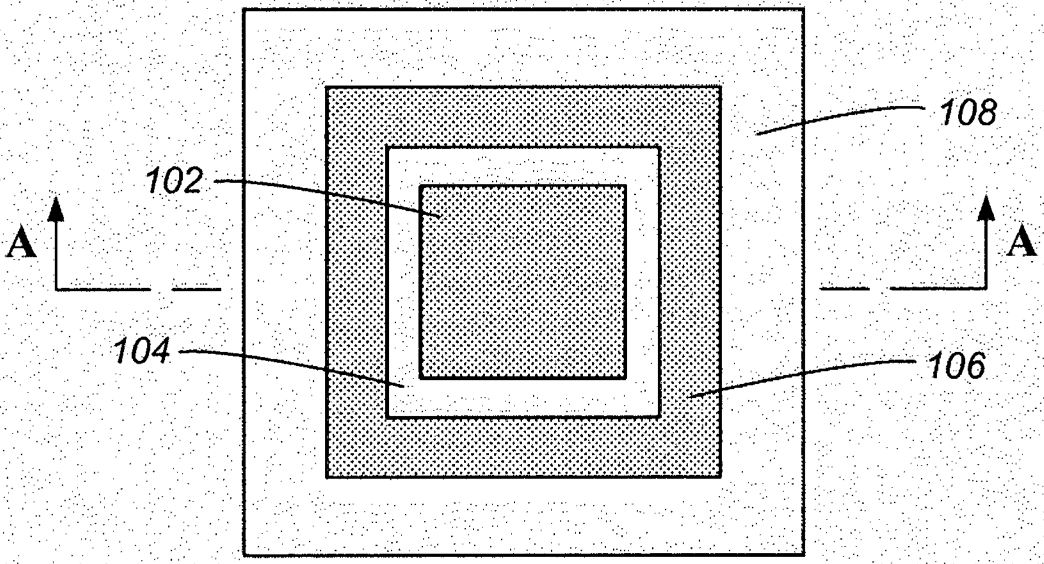

FIG. 1B

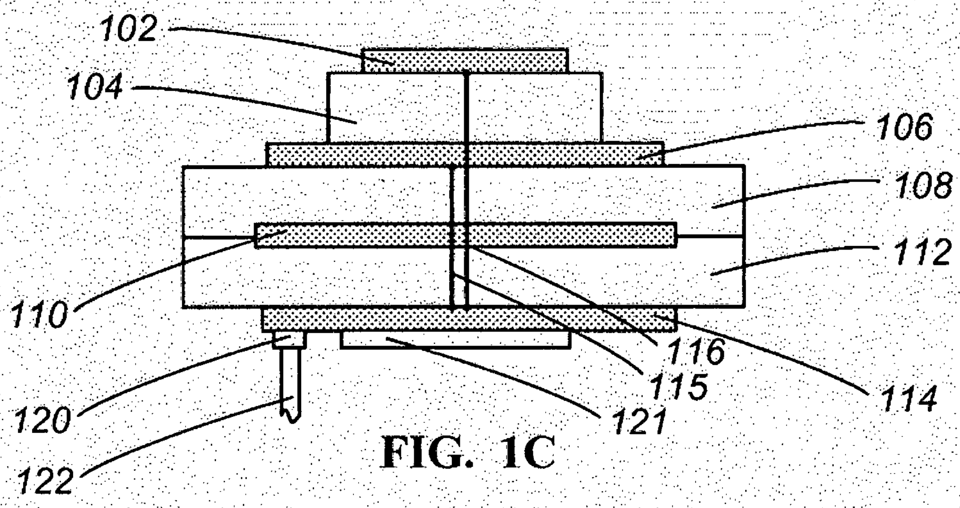

FIG. 1C

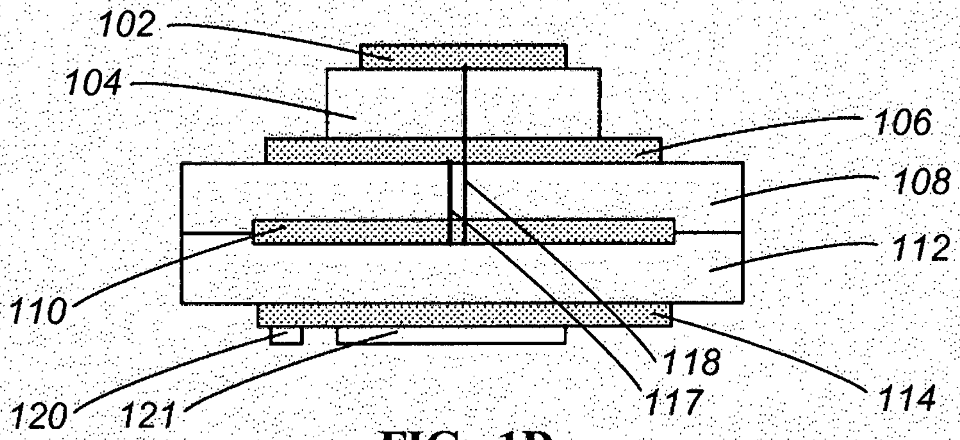

FIG. 1D

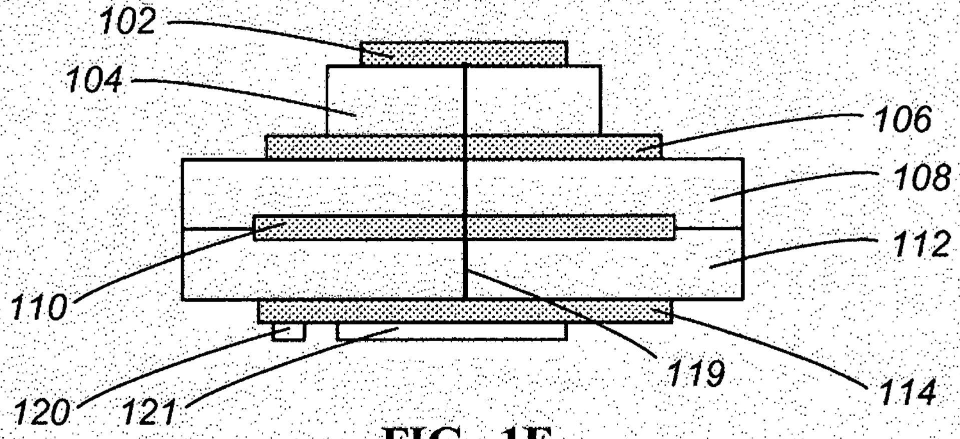

FIG. 1E

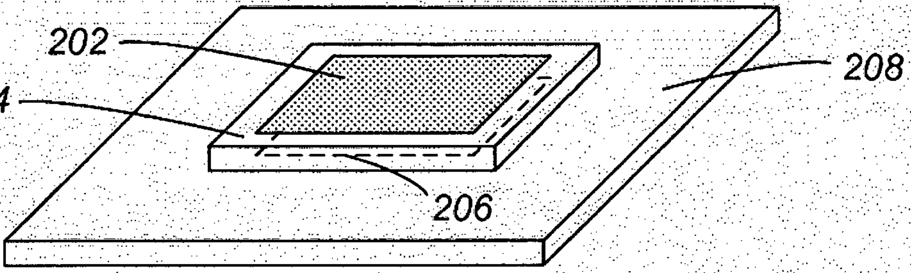

FIG. 2A

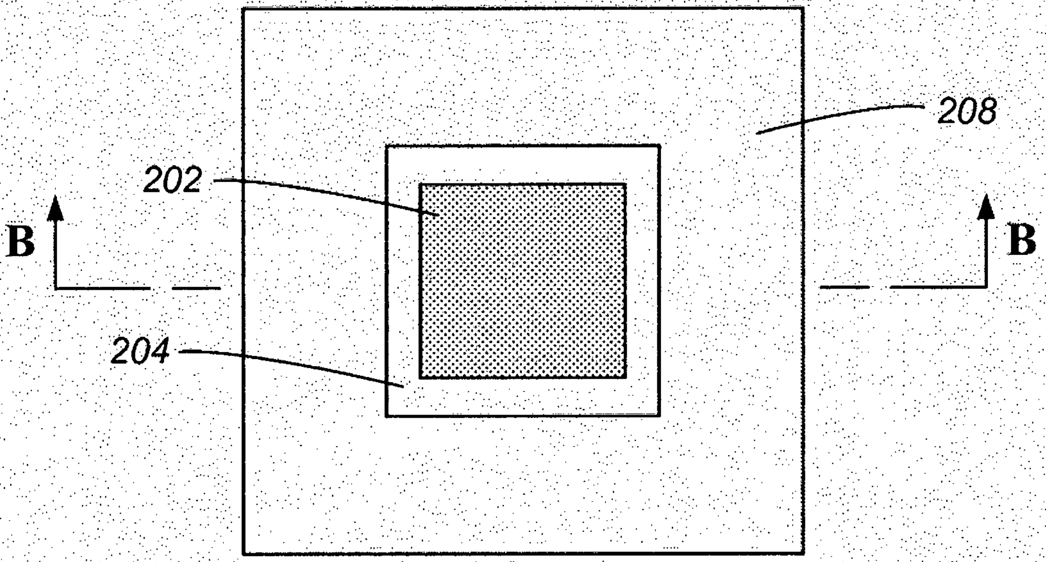

FIG. 2B

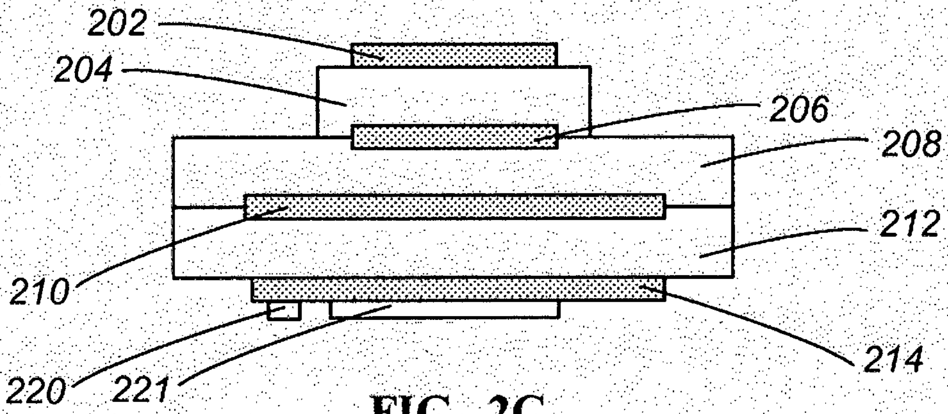

FIG. 2C

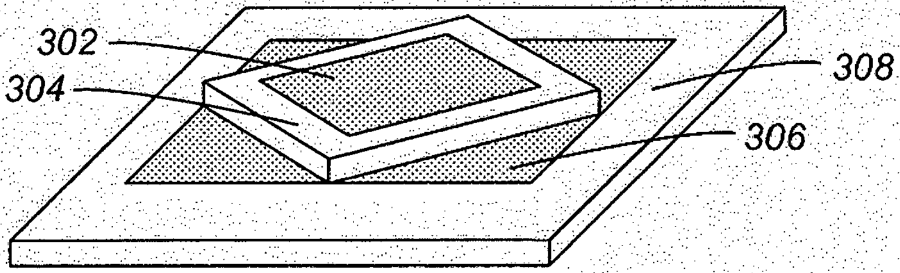

FIG. 3A

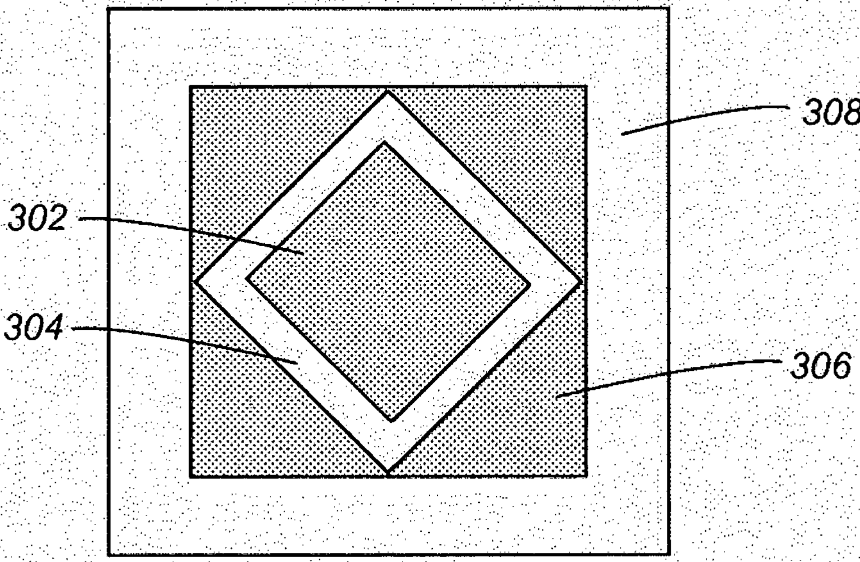

FIG. 3B

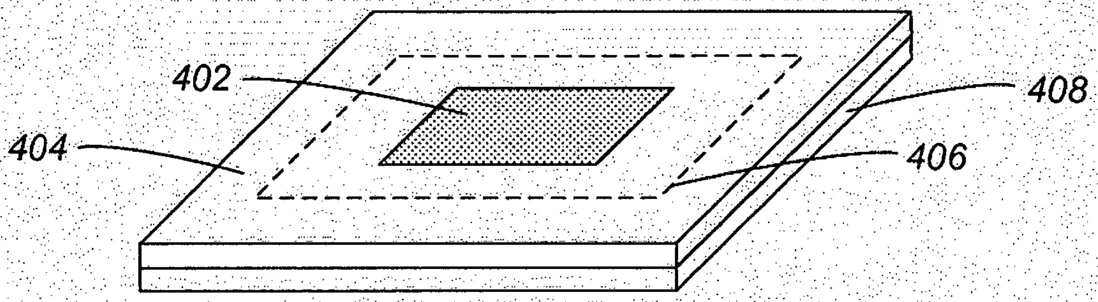

FIG. 4A

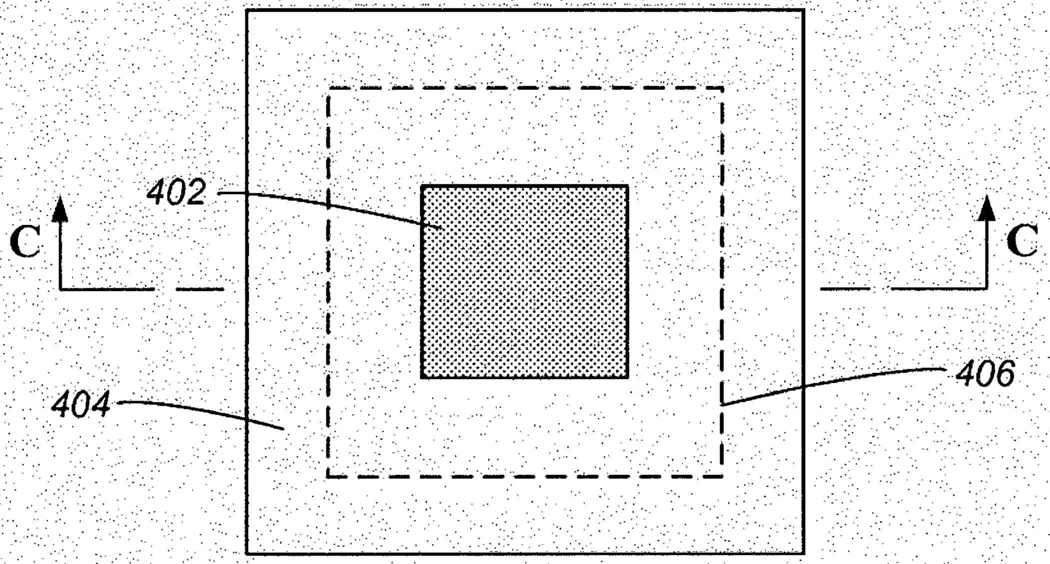

FIG. 4B

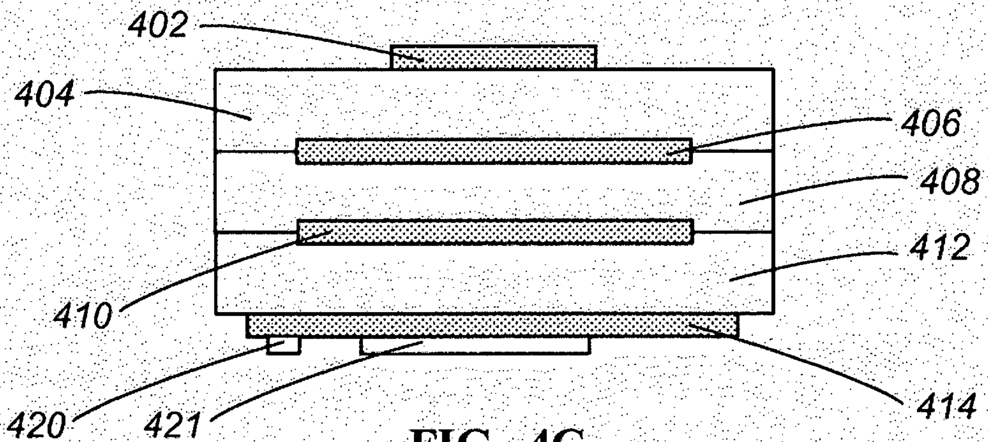

FIG. 4C

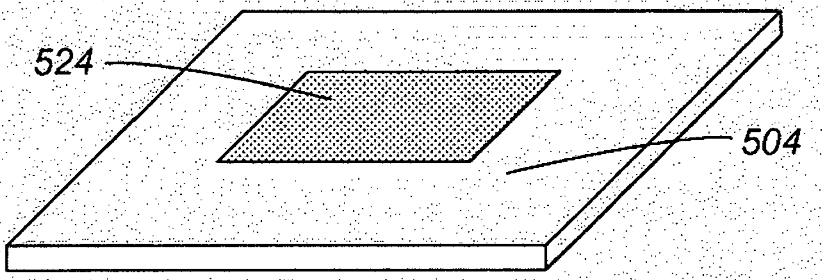

FIG. 5A

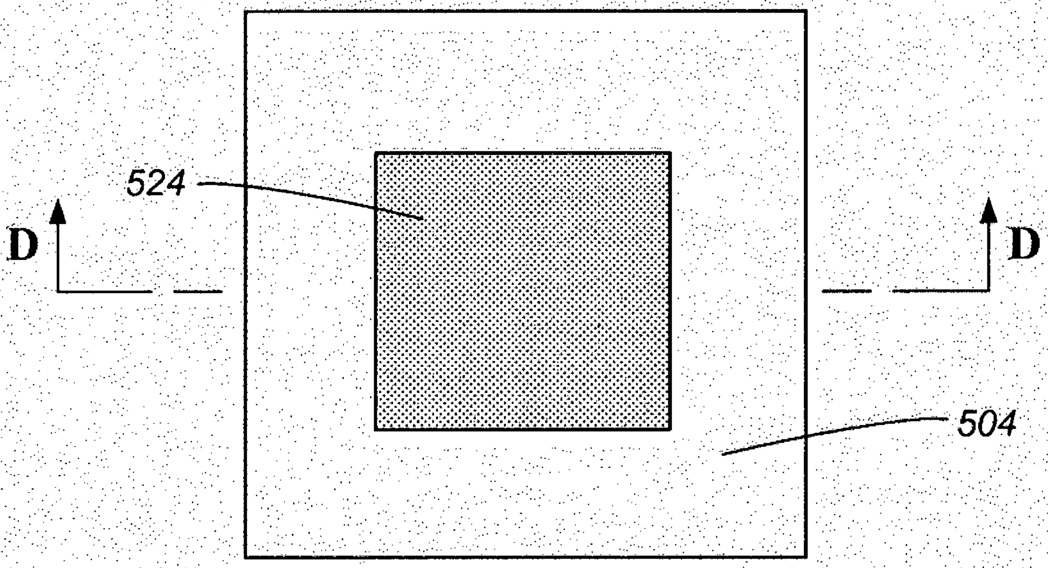

FIG. 5B

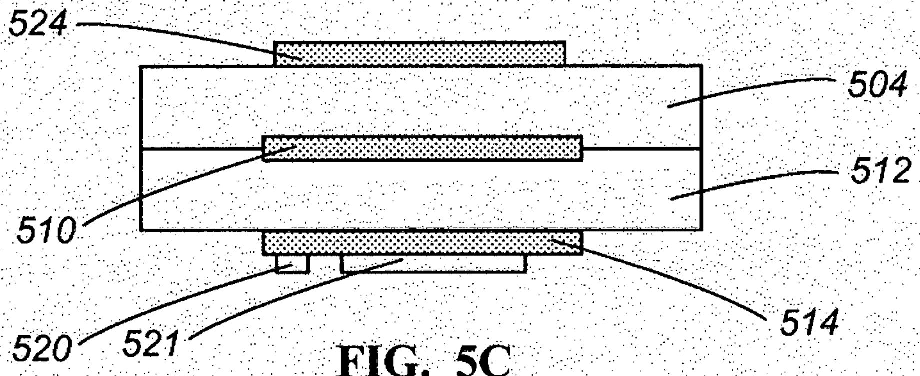

FIG. 5C

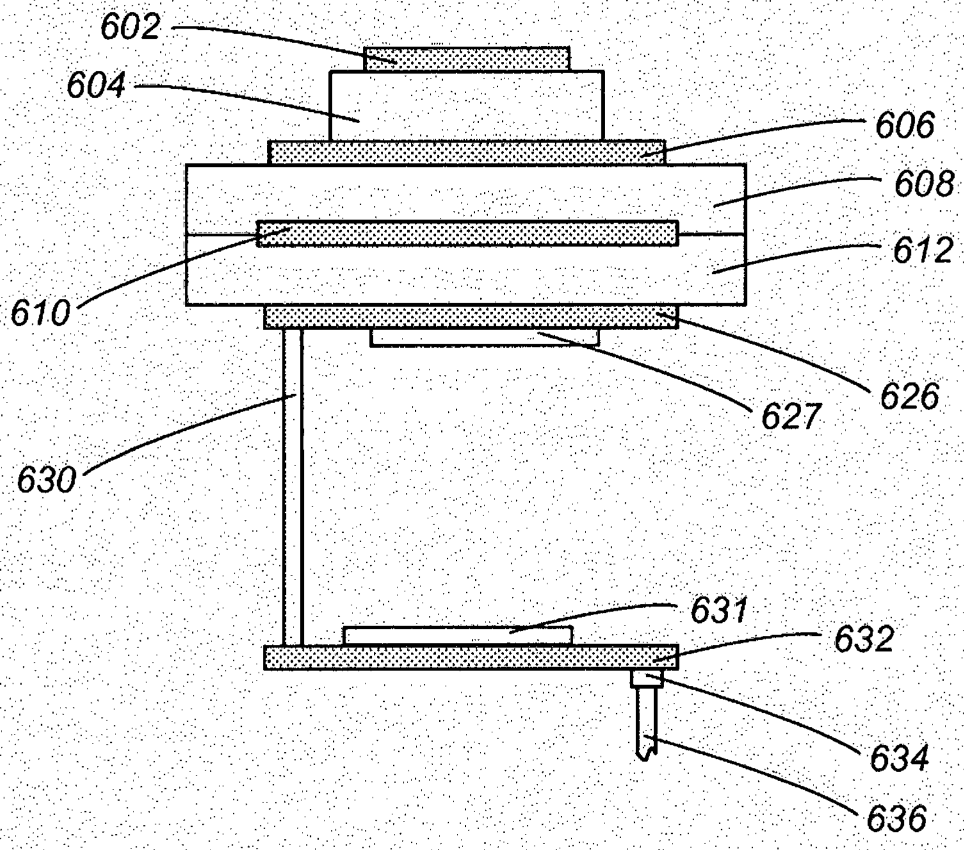

FIG. 6

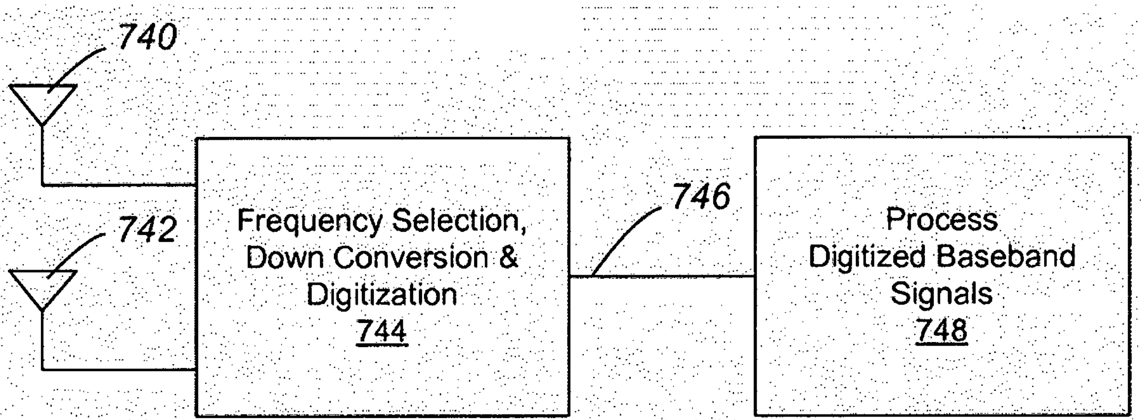

FIG. 7A

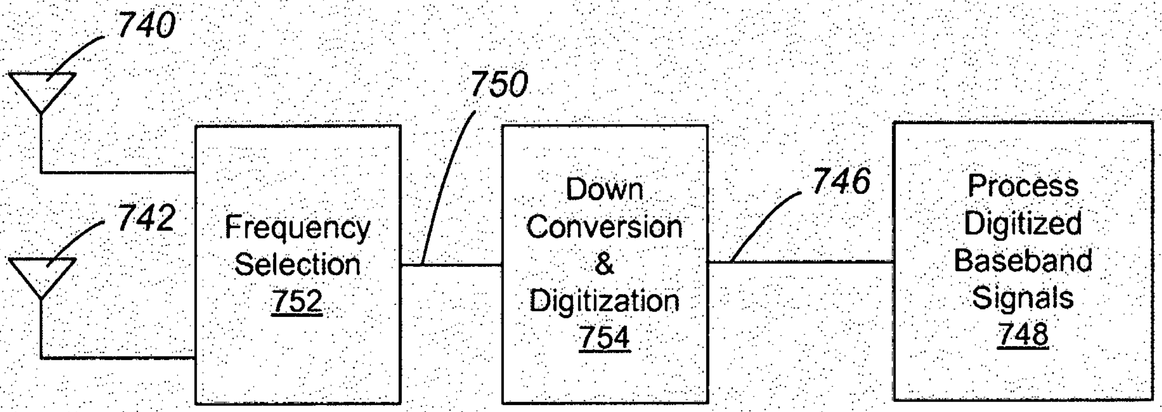

FIG. 7B

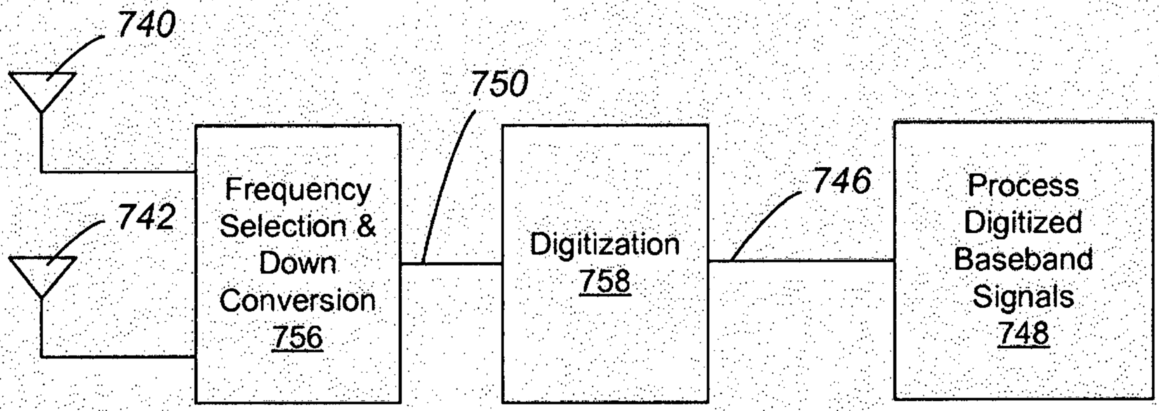

FIG. 7C

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