# United States Patent

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## [54] TELEPHONE-SIGNALING UNIT


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[51] **Int. Cl.** ..... **H04m 7/16**

[58] **Field of Search** ..... 179/16 E, 16 EA, 16 EC, 15 BY, 179/15 FD, 15 R



[56] **References Cited**

UNITED STATES PATENTS

| | | | |
|---|---|---|---|
| 3,312,784 | 4/1967 | Draper | 179/16 E |
| 3,452,220 | 6/1969 | Fritschi | 179/16 E |
| 3,544,724 | 12/1970 | Pento | 179/16 E |



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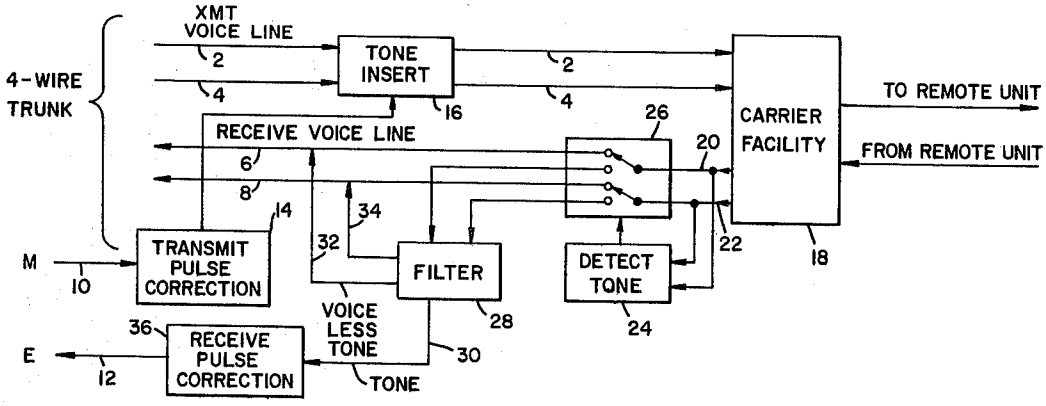
[57] **ABSTRACT**

An in-band telephone-signaling unit of the type useful in carrier trunk systems is disclosed having receive and transmit pulse correction circuits and a band stop/band-pass filter for using an idle channel for supervisory purposes. The transmit pulse correction circuit provides constant length pulses in response to varying length pulses; the receive pulse correction circuit looks for pulses longer than a predetermined length and generates pulses having a constant duty cycle. The band-stop/band-pass filter employs a resonant arm in an active resistance bridge configuration.


**14 Claims, 6 Drawing Figures**



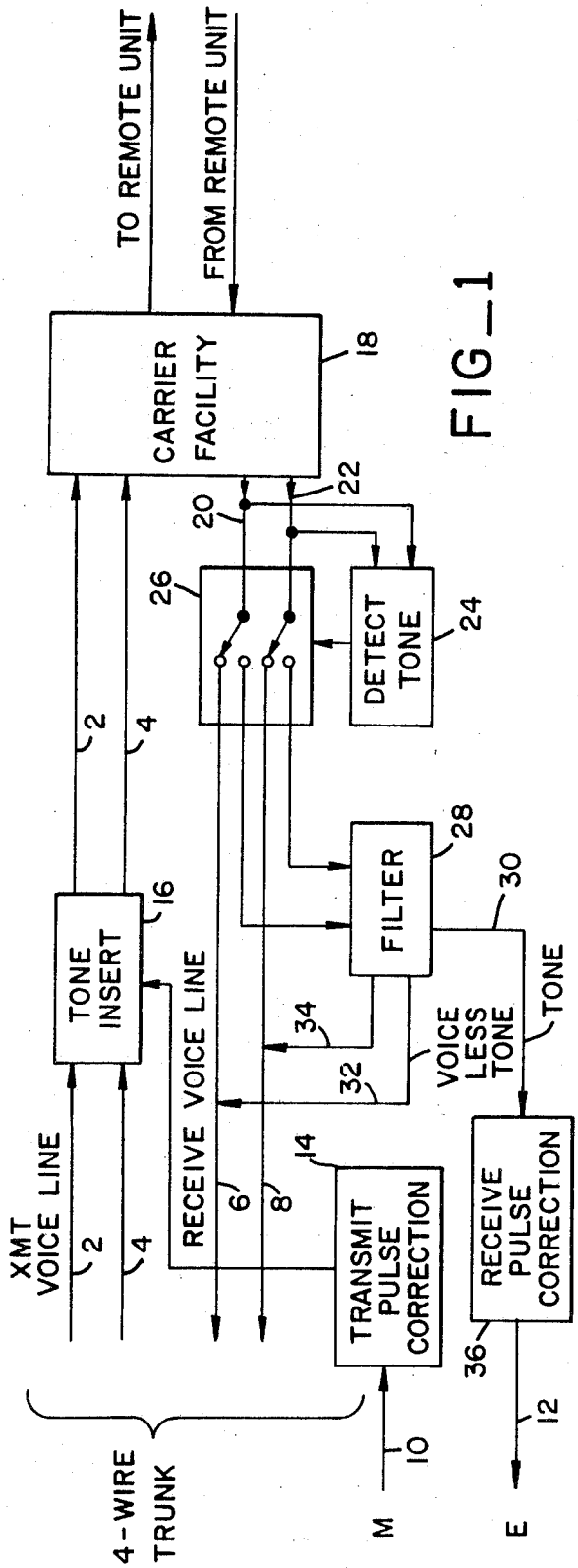



FIG_1

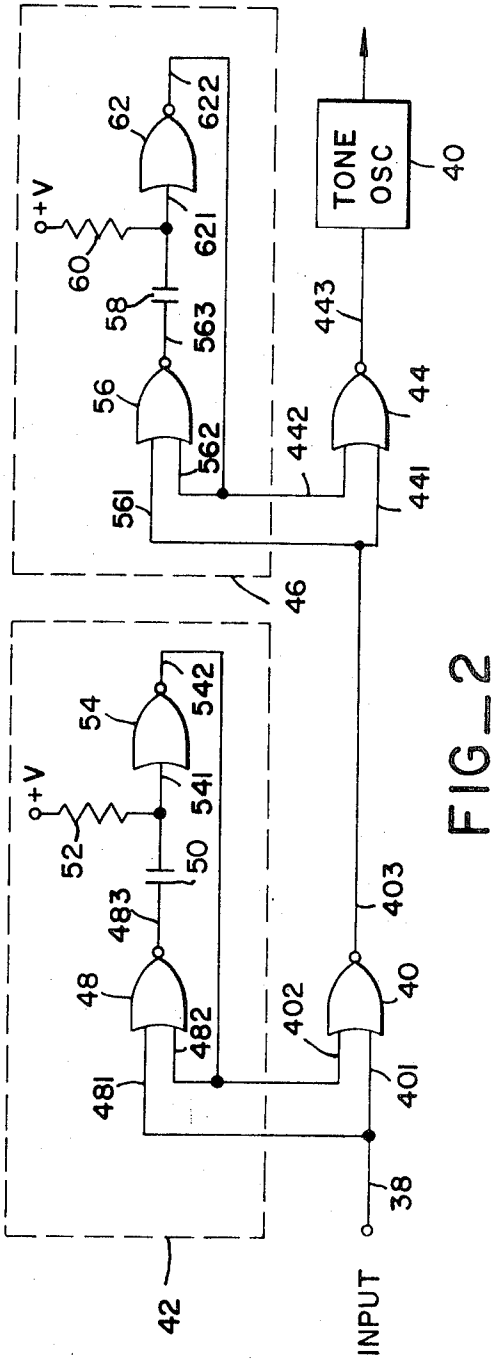



FIG_2

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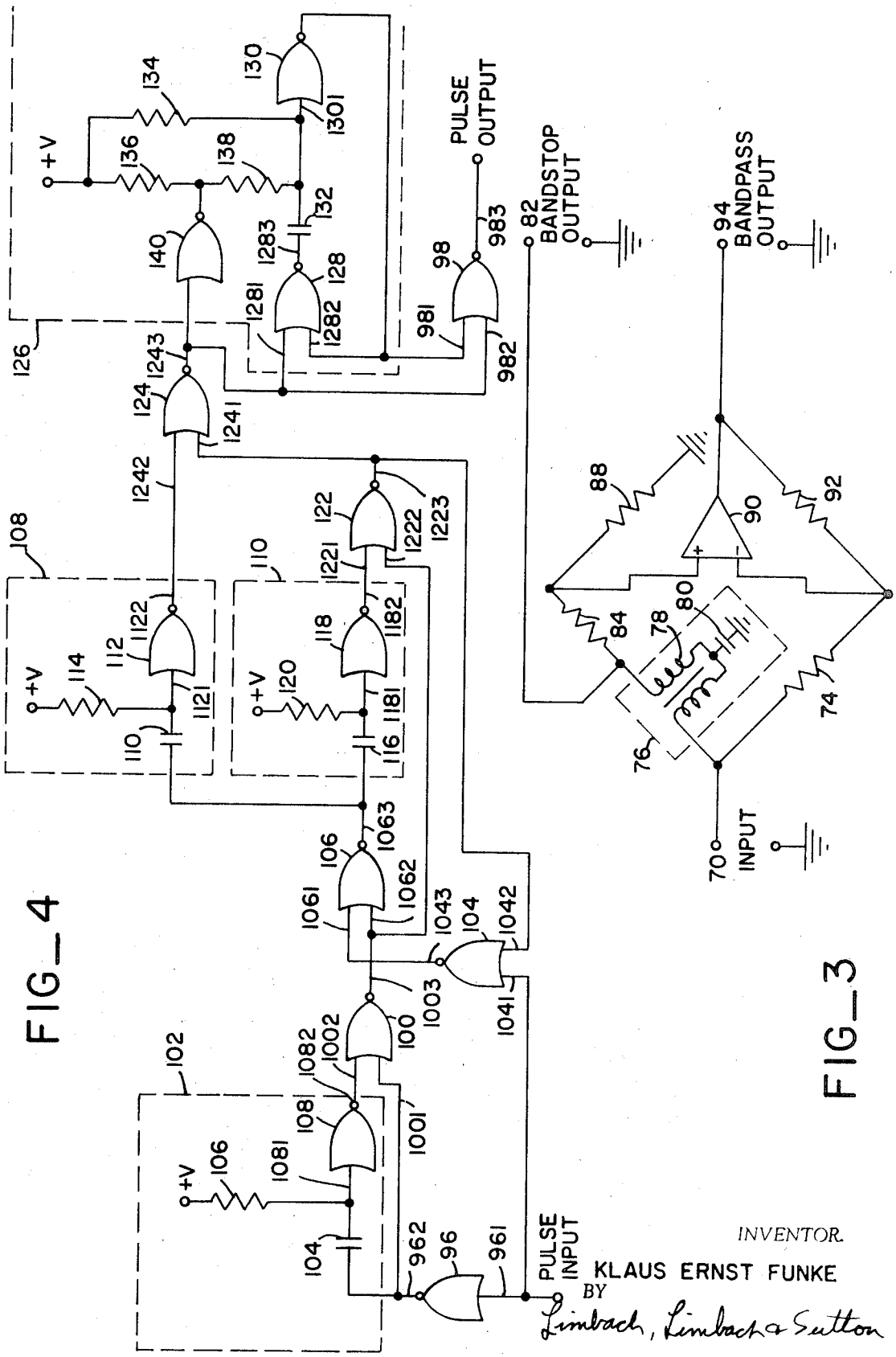


FIG_4

FIG_3

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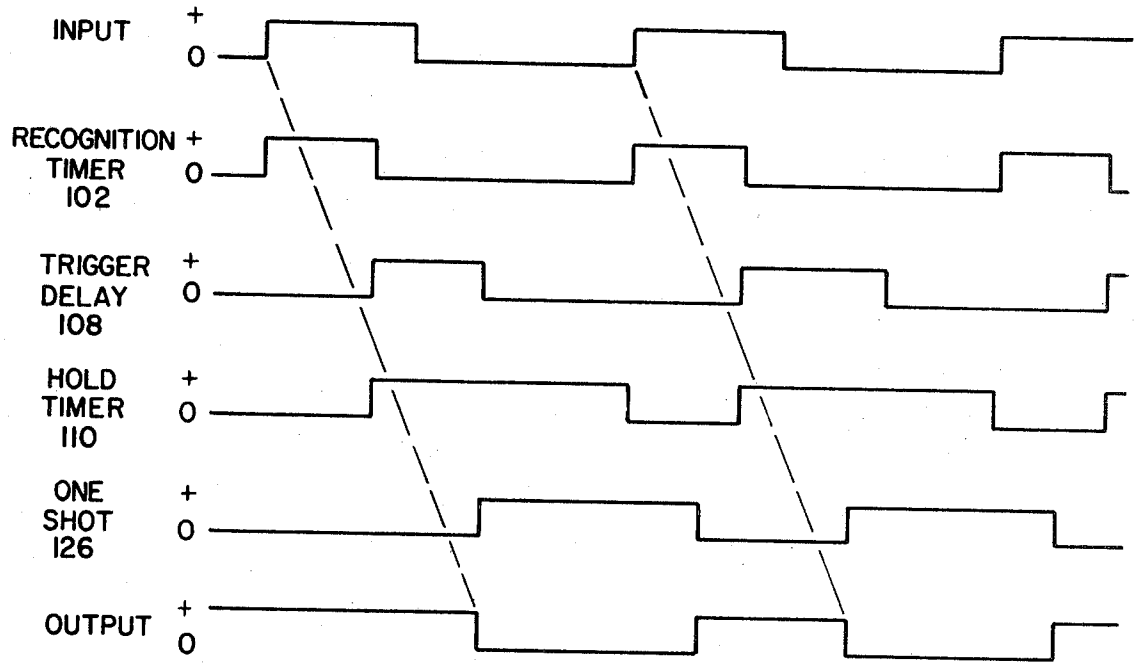


FIG_5

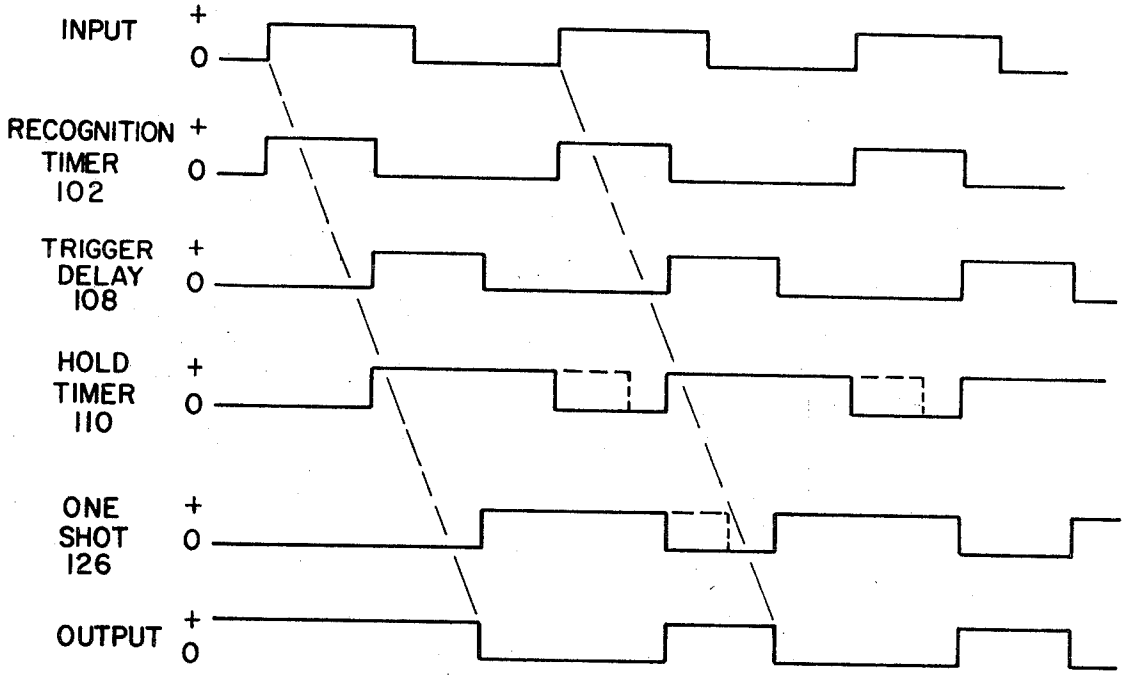


FIG_6

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# TELEPHONE-SIGNALING UNIT

## BACKGROUND OF THE INVENTION

This invention relates generally to telephone systems and more particularly to a telephone-signaling unit.

In many modern telephone systems the trunk interconnection between central offices uses carrier transmission. Consequently, the signaling or control information necessary to establish telephone connections is transmitted as an in-band single frequency tone. In-band means a frequency lying within the normal voice-frequency band. Ordinarily, a continuous low amplitude tone is transmitted in a channel to indicate that it is idle; dialing pulses are transmitted as interrupted tones at a higher amplitude level.

Dialing pulses are generated over a DC circuit known as an "M"-lead, in telephone parlance. The pulses are negative voltages ordinarily −21 volts to −56 volts. The dialing pattern is reproduced at the remote end of the channel on an "E"-lead that opens and closes a relay. Because of various factors including variations in dial pulse length and pulse rate generated by the telephone itself and noise on the telephone lines it is often necessary to correct the dialing pulses by varying their length in order that the switching equipment receiving the pulses operate properly. This is particularly a problem when two systems are interfacing with each other over a carrier system; dial pulse timing that is acceptable in one system may not be acceptable in the other. Because a signaling unit may be working end-to-end with other signaling units which do not provide dial pulse correction it is desirable to provide correction circuits in both the transmit and receive signaling paths.

In the case of an idle channel, it is desirable to be able to use the voice path for supervision while the low amplitude constant signaling tone is present.

In accordance with the invention, a signaling unit is provided with a receive pulse correction circuit, a transmit pulse connection circuit, and a bandstop/band-pass filter for permitting supervisory use of an idle channel despite the presence of the constant tone.

According to one embodiment of the invention a transmit pulse correction circuit is provided that compensates for variations in the length of input dial pulses. The circuit provides for a constant output pulse length over a wide variation in input pulse rates and pulse lengths by an arrangement of two series connected NOR gates. A one shot is associated with each gate; the second one shot assures a constant output pulse length, the first one shot tends to provide a constant pulse-off time in order that a generally constant duty cycle results.

The invention further provides a bandstop/band-pass filter. If signaling tone is recognized on the incoming line, the receive voice path is routed through the filter to provide a tone output and a voice minus tone output. The filter is essentially an active resistance bridge with a sharp resonance at the tone frequency in one of the arms. By this arrangement, the tone output may be taken at one point in the bridge and the voice less tone at another.

In addition, the invention contemplates in the signaling unit, a receive pulse correction circuit. Since the received signaling tones are more likely to be incorrect because of noise and other variations, the correction circuit is more complex than the transmit correction circuit. The receive pulse correction circuit will act only on pulses exceeding a minimum time duration, in order to eliminate false pulses caused by noise. The circuit operates to provide a fixed output duty cycle for any particular input pulse rate no matter how the input duty cycle may vary. Adjustments for fast pulse rates are provided. The output pulses thus are adapted to optimally operate switching units that desirably require constant dial pulse duty cycles.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an embodiment of the signaling unit according to the present invention.

FIG. 2 is a schematic diagram of an embodiment of the transmit pulse correction circuit according to the present invention.



FIG. 3 is a schematic diagram of an embodiment of the bandstop/band-pass filter according to the present invention.

FIG. 4 is a schematic diagram of an embodiment of the receive pulse correction circuit according to the present invention.

FIG. 5 is a waveform diagram useful in understanding the circuit of FIG. 4.

FIG. 6 is a further waveform diagram useful in understanding the circuit of FIG. 4.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1 of the drawings, a block diagram of the signaling unit according to one embodiment of the invention is shown. The unit is designed to connect to a standard four-wire trunk via lines 2, 4, 6, and 8; two wires for the transmitted voice (2 and 4) and two for the received voice (6 and 8). By using a conventional hybrid the four wires may be connected to a two-wire trunk. In addition, standard "E" and "M" DC signaling lines 10 and 12, respectively, are provided. Dialing pulses, in the form of negative voltages, applied to to the M-lead will cause contact closure on the E-lead at a remote signaling unit similar to that shown in FIG. 1. Since the units are essentially identical, only one is shown. The E-lead contact closures reproduce the dialing pattern applied to the remote M-lead.

M-lead negative dialing pulses on line 10 are applied to a transmit pulse correction circuit 14. Circuit 14 looks for positive- or negative-going transitions greater than a predetermined minimum time, 14 milliseconds for example. Once a transition has been recognized, a timing circuit controls a tone oscillator having a single tone frequency in the voice band, 2,600 Hz., for example, to ensure that the tone-on/tone-off ratio will be acceptable over a wide range of dialing speeds, for example, 8 to 14 pulses per second. The tone-on/tone-off ratio is important to ensure that the dialing pulses will properly actuate remote switching equipment.

Correction pulse tones from circuit 14 are applied to a tone insert unit 16 that applies the tones to the transmit voice line 2 and 4 for connection to a carrier facility 18. Ordinarily voice inputs on lines 2 and 4 are inhibited during dialing by circuitry not shown or forming part of the invention. Also, when the line is not being used for voice communication, a tone, having a constant level, lower than the dialing pulse tone, is applied to the carrier facility 16. The carrier facility may be any type of carrier system, employing any type of modulation known in the art. For example, frequency division multiplex frequency modulation (FDM–FM) may be used. Also, cables, microwaves, satellites, lasers or any other type of link may be used to connect separate units. The details of the carrier system forms no part of the present invention.

A pair of receive lines 20 and 22 from the carrier facility 18 are connected to a tone detector unit 24 and a double-pole double-throw switch 26 that is controlled by unit 24. Tone detector 24 looks for the signaling tones. Because the tones are in the voice band, the detector must be able to distinguish between signal tones (of 2,600 Hz. for example) and 2,600 Hz. components in speech or noise in the voice-frequency band. A suitable circuit compares the spectral energy present at the signaling frequency with the energy in the rest of the voice band. The 2,600 Hz. components will be recognized as signaling tone only if their energy level is significantly higher than the energy level in the rest of the voice band, and then only if this difference is maintained for a sufficient period of time. The details of such a circuit are within the ordinary skill in this art and, forming no specific part of the invention, will not be disclosed here.

If no tone is detected, switch 26 is positioned to connect lines 20 and 22 directly to the receive voice line 6 and 8. This is the normal talking condition of the unit. If, however, a tone is detected, then lines 20 and 22 are connected to a filter unit 28. Filter 28 sharply filters out the signal tone for application to line 30. On lines 32 and 34 the voice band with the signal frequency rejected is provided from filter 28. This arrange-

ment permits the receive voice path to be used for supervision while the low level signal tone is present during the idle channel condition. When high amplitude level signal tones, representing dial pulses are received, supervisory "talk-over" is not provided.

A receive pulse correction circuit **36** receives the signal tone on line **30** and recognizes transitions from off to on of greater than a preset minimum time. Thus noise is not recognized as a tone burst or space between tone bursts. Once transitions are recognized, the circuit ensures that the E-lead contact, line **12**, will be closed for a substantially constant proportion of the time during dialing despite variations in dialing rates and variations in the duty cycle of the dialing pulses. The receive correction circuit is necessary even if the remote unit is equipped with a transmit pulse correction circuit because of variable signal tone burst length from the transmit equipment.

In FIG. **2** the transmit pulse correction circuit is shown in greater detail as including six RTL (resistor transistor logic) NOR gates. A NOR gate provides a logic "1" (positive) output only when both inputs are a logic "0" (ground). For all other combinations of inputs the output is "0." Dialing pulses are applied on input line **38**; a ground or "0" represents a pulse and positive or "1" represents a space between pulses. In general, a "0" on input line **38** turns on tone oscillator **40** and a "1" turns the oscillator off.

The pulses on line **38** are applied to input **401** of gate **40** and to a first one-shot circuit **42**. The gate output at **403** is applied to input **441** of gate **44** and to a second one-shot circuit **46**. Output **443** of gate **44** controls the tone oscillator **40**; a "0" at **443** turns the oscillator on, a "1" turns it off.

One-shots **42** and **46** function identically except for their time constants. In the steady-state condition inputs **481** and **482** of gate **48** are "0." Input **481** is connected to line **38** and is the input of one-shot **42**. When a transition from "0" to "1" occurs at input **481**, the output **483** of gate **48** goes from "1" to "0" thus instantaneously clamping one side of capacitor **50**, which is connected to output **483**, to ground. The opposite side of capacitor **50** which is connected to a positive voltage source +v. through resistor **52** and to input **541** of gate **54**, must also drop to ground. The output **542** of gate **54** will thus be "1"; this output is fed back to input **482** of gate **48** and provides the one-shot output to input **402** of gate **40**. As capacitor **50** charges through resistor **52** according to the RC-time constant of those components, the voltage at input **541** rises and eventually becomes sufficiently positive to flip gate **54** to provide a "0" at output **542**. Thus a "0" to "1" transition at input **481** initiates a time period during which the one shot provides a "1" output. During that time period the input **481** may change to any value because the "1" is fed back to input **482** of gate **48** thus forcing output **483** to remain "0."

In the same manner, the second one shot has an input **561** to a gate **56**. The gate output **563** is connected to a capacitor **58** that is in turn connected first to a positive voltage source +v through a resistor **60** and to an input **621** of a gate **62**. Gate **62** has its output **622** fed back to input **562** of gate **56** and to input **442** of gate **44** to provide the one-shot output.

In order to better appreciate the operation of the circuit, the following table is presented, showing the four possible operations a time before an input transition ($t_n$) and a time after an input transition ($t_{n+1}$):

| Input Condition at 401 | | First One Shot | | Second One Shot | | Tone |
|---|---|---|---|---|---|---|
| $t_n$ | $t_{n+1}$ | 402 | 403/441 | 442 | 443 | Osc. |
| 0 | 0 | 0 | 1 | 0 | 0 | tone |
| 0 | 1 | 1 | 0 | 0 | 1 | no tone |
| 1 | 1 | 0 | 0 | 0 | 1 | no tone |
| 1 | 0 | 0 | 1 | 1 | 0 | tone |

Conditions 1 and 3 are steady-state conditions; 2 and 4 are states after a transition.

In operation, the following events can occur. If the duration of a "0" input is longer than the time of the second one shot, the tone-on time is the same length as input "0." This is condition 1. If the following "1" is in duration longer than the time of the first one shot, the tone-off time will be the same length as the "1" input. This is condition 3. In both cases, the one shots are timed out and the input is directly controlling the output.

In condition 2, a minimum tone-off time is provided equal to the time of the first one-shot **42** in some cases, as will be apparent hereinafter. Thus, when a "0" to "1" transition occurs the first one-shot **42** starts timing to keep **403** a "0" even if the input "1" switches state back to "0." As long as **403** is "0," the second one-shot **46** is prevented from turning on and the tone oscillator is kept off.

In condition 4, a minimum tone-on time is provided equal to the time of the second one-shot **46**. The new "0" will not turn on the first one-shot **42**, thus **401** and **402** are "0" and **403** is "1" turning on the second one-shot **46** causing the tone oscillator to go on. Even if the input "0" switches to "1" the second one shot remains on, keeping the oscillator **40** on.

It will be apparent that the second one-shot **46** can override the first one-shot **42**. Thus even if a "1" closely follows a "0," the fact that the first one shot begins timing will have no effect on the second one shot. Thus, it is possible that the first one-shot time will not affect the output if the second one shot is still on. When the second one shot finishes timing, the first one shot, if it is still timing will provide a shortened no tone output. The practical result is that the tone-on spaces are always at least a minimum length, equal to the time of the second one-shot **46**, but the tone-off times may be shortened. This is a desirable result, because the tone-on periods must be of a fixed minimum duration to assure proper switching at remote units. If a sacrifice must be made, it is more desirable to shorten the tone-off period when necessary.

In FIG. **3** an embodiment of the band-pass and bandstop filter **28** of FIG. **1** is shown in greater detail. To facilitate understanding of the filter, it is shown in a bridge configuration. The combined voice and tone signals are applied at the left-hand corner of the bridge at input terminal **70**. Terminal **70** is connected to the junction of a resistor **74** and a passive LC filter **76**. Filter **76** is a transformer-type LC series resonant filter, resonated at the signal tone frequency, consisting of a transformer **78** having first and second windings connected together at one end and to a capacitor **80**. The other end of the capacitor is grounded. The ends of the windings not connected together are connected to input **70** and to the bandstop output terminal **82**, respectively. A resistor **84** is connected between the bandstop output **82** and the top of the bridge. A resistor **88** is connected between the top of the bridge and ground. An operational amplifier has its positive input connected to the top of the bridge; its negative input is connected through a resistor **92** to the amplifier **90** output and to the band-pass output terminal **94**. A resistor **74** is connected between the bottom of the bridge (and the amplifier **90** negative input) and the input terminal **70**.

In operation, when the bridge is balanced R84/R88=R74/R92 and the output is at a virtual ground. The input voltage is divided by R84 and R88 and applied to the positive input of amplifier **90**. The amplifier output will change its state in order to make the negative input as high as the positive input. If a high Q rejection filter, such as filter **76** is placed in the arm of the bridge containing R84, the bridge will be unbalanced for the rejected frequency and the amplifier becomes a unity gain amplifier if R74 equals R92.

In FIG. **4** an embodiment of the receive pulse correction circuit **36** of FIG. **1** is shown in greater detail. The circuit has 13 NOR gates that are connected to provide four timing functions. A NOR gate provides a logic "1" output only when both inputs are "0."

In the steady-state condition, the circuit input at **961** of gate **96** is "0" and the circuit output at **983** of gate **98** is "1." A "0" input indicates no received pulse. Upon receipt of an incoming pulse, **961** goes to "1," causing **962** to go to "0." Thus input **1001** of gate **100** and the input of recognition timer **102** to to "0." Recognition timer **102**, "looks" to see if the pulse

exceeds a predetermined minimum time; it consists of an input capacitor 104 that is connected to a positive voltage source +v. through a resistor 106. The resistor 106, capacitor 104 junction is connected to input 1081 of gate 108. When one side of the capacitor 104 instantaneously goes to "0," so must the other side causing 1081 to be "0" and output 1082 of gate 108 to be "1." As capacitor 104 charges through resistor 106, input 1081 rises in voltage until gate 108 flips to provide a "0" output. Thus after the predetermined recognition time, 1082 becomes "0." If and only if there is still a pulse input at 961, then inputs 1001 and 1002 of gate 100 will both be "0" thus making output 1003 a "1." The pulse at 961 is also applied to input 1041 of gate 104, making output 1043 be "0." Thus gate 106 receives at input 1061 a "0" from gate 104 and at input 1062 a "1" from gate 100. Gate 106 is therefore "0" at its output 1063.

A "0" at output 1063 of gate 106 initiates two timing circuits: a trigger delay 108 and a hold timer 110. Both function in a way similar to recognition timer 102. Hold timer 110 becomes a one shot when the input signal changes state and closes the feedback path via gate 122 and gate 104. Trigger delay 108 includes an input capacitor 110 connected to an inverter gate 112, and a charging resistor 114 connected between the junction of capacitor 110 and the input 1121 of gate 112 and a positive voltage source +v. Hold timer 110 includes an input capacitor 116 connected to an inverter gate 118 and a charging resistor 120 connected to the junction of capacitor 116 and the input 1181 of gate 118.

If the positive input pulse at 961 changes state after starting hold timer 110, a feedback path including a gate 122 and gate 104 keeps the hold timer operating. Output 1182 of gate 118 is connected to input 1221 of gate 122; input 1062 of gate 106 and input 1222 of gate 122 are tied together. The output 1223 of gate 122 is applied to input 1042 of gate 104 and to input 1241 of a gate 124. Thus 1221 is "1," 1223 and 1042 are "0" and 1041 is "0" making 1043 "1."

If, however, a new pulse comes along, 1041 becomes "1" and 1043 goes to "0" causing 1061 to go to "0." The recognition timer will be on, hence 1062 is "0" and thus 1063 is "1" and the timers are turned off ("0") because the capacitors and inverter gate inputs are forced to "1." If the trigger delay has not timed out by the time the new pulse arrives, it will be seen that there is no output pulse.

If a new pulse does not arrive before the hold timer times out, the feedback path is opened when the hold timer times out.

After timing out of the trigger delay, the input 1242 of gate 124 goes to "0." Input 1241 will also be "0" and hence its output 1342 is "1." The "1" initiates a variable one-shot 126 that includes an input gate 128 having two inputs 1281 which are connected to 1243, and 1283 that is connected to the output 1302 of gate 130. The output of gate 128 is connected to a capacitor 132 that is further connected to the input 1301 of gate 130. The junction of capacitor 132 and input 1301 has a resistor 134 connected between there and positive voltage source +v and also a series connection of resistors 136 and 138 connected between the junction and +v. The junction of resistors 136 and 138 is connected to the output 1402 of a gate 140. Input 1401 of gate 140 is connected to the input 1281 of gate 128. Output gate 98 has its input 981 connected to 1302 and has its input 982 connected to 1281. Hence, at the end of the trigger delay period, the hold timer is allowed to begin its control of the variable one-shot 126. If the trigger delay is interrupted by the early arrival of an input pulse, the one shot will not be initiated.

As long as the hold timer 110 runs or a positive pulse is present at 961 one-shot 126 will determine the output pulse duration (1221 is "1" when the hold timer is on; 1222 is "1" when there is an input pulse—either condition causes 1223 to be "0" thus 1241 and 1242 are both "0" and 1243 is "1" starting one-shot 126). So long as one-shot 126 runs, 981 will be "1" causing the output 983 to be "0" and generating a pulse.

Initially one-shot 126 will have only resistor 134 active in the charging circuit because 1402 is at "0" and the resistor 136, resistor 138 junction is grounded. When the next positive pulse arrives, the hold timer is stopped, if it is still running, and consequently 1402 goes to "1" thus placing series resistor 136, 138 in parallel to resistor 134 decreasing the resistance and time constant, hence shortening the output pulse length.

The operation of the receive pulse correction circuit may be better understood by reference to the waveforms in FIGS. 5 and 6. It should be borne in mind that the circuit is acting to provide a fixed output duty cycle for any input pulse rate despite variations in the input duty cycle.

In FIG. 5, the input pulses actuate the recognition timer. Since the input is still present at the end of the recognition time, the trigger delay 108 and hold timer 110 are actuated. At the conclusion of the trigger delay one-shot 126 begins running. Thus recognition timer 102 and trigger delay 108 provide a phase shifting effect. One-shot 126 has a time constant due to resistor 134 during the time hold timer is running, when the hold timer ceases to run resistor 136 and 138 are switched in parallel to resistor 134 and the time constant increases. For the example of FIG. 5 the hold timer runs its normal full time and the output, which is the negative of the one-shot output, is of normal pulse length. For input pulse rates no shorter than in the example of FIG. 5 the output pulse length will be of this fixed length, even though the input pulses may vary in length (duty cycle).

Referring to FIG. 6, the case of a faster input pulse rate is shown. In order to accommodate this condition and yet maintain a usable output duty cycle, the output pulses are shortened. This action occurs in the hold timer; the normal hold time period is interrupted by a new input pulse, thereby switching the one-shot 126 time constant sooner than normal to shorten the output pulse. Thus, the pulse correction circuit has essentially two functions: the input pulse edge is shifted in phase so that the input pulse rate may be taken account of. Depending on the input pulse rate, the output pulse is controlled by controlling the variable one shot.

It is understood that the above-described embodiments are illustrative of the principles of the invention. Numerous other arrangements may be derived by those skilled in the art without departing from the spirit and scope of the invention.

I claim:

1. In a telephone system, a receive signaling pulse correction circuit responsive to bilevel DC dialing pulse signals representing interrupted tones received from remote signaling units in a carrier trunk system for providing a constant duty cycle output for a range of input pulse rates having varying duty cycles comprising:

recognition timer means, responsive to input dialing pulses, having a predetermined time period initiated by each input dialing pulse, for providing a recognition signal when an input dialing pulse length exceeds said predetermined time period;

trigger delay means, responsive to said recognition timer means and said input dialing pulses, having a predetermined time period initiated by each recognition signal for providing a trigger delay signal at the end of said time period if a second dialing pulse is not received during said trigger delay time period, and

output means responsive to said input dialing pulses and said trigger signal for providing an output pulse.

2. The circuit of claim 1 wherein said output means comprises:

hold timer means responsive to said recognition timer means and said input dialing pulses, having a predetermined hold time period longer than said trigger delay means predetermined time and initiated by each recognition signal for providing a hold signal during said predetermined hold time and for interrupting said hold signal if a second input dialing pulse is received during said predetermined hold time, and variable one-shot means responsive to said hold timer means for providing

an output signal having a time period length dependent on the time length of said hold signal.

3. The circuit of claim 2 wherein said variable one-shot means has a first time constant that is operative when said hold signal is present and a second time constant that is substituted for said first time constant when said hold signal is interrupted.

4. In a telephone system, a receive signaling pulse correction circuit responsive to bilevel DC dialing pulse signals representing interrupted tones received from remote signaling units in a carrier trunk system for providing a constant duty cycle output for a range of input pulse rates having varying duty cycles comprising:

means for generating a constant length pulse in response to an input dialing pulse and for delaying said constant length pulse in phase when said input dialing pulse exceeds a minimum predetermined length and when a second pulse does not follow said dialing pulse within a predetermined time period,

means responsive to an input dialing pulse exceeding said minimum predetermined length for providing an output signal until a predetermined time period has elapsed or a second input dialing pulse is received,

pulse output means having first and second time constants and responsive to said phase shifted constant length pulse and said output signal initiating a pulse output when said constant length pulse ends, said pulse output length determined by said first time constant when said output signal is applied, and determined by said second time constant when said output signal is interrupted.

5. In a telephone system, a transmit signaling pulse correction circuit responsive to bilevel DC dialing pulse signals received from local switching circuits for altering the duty cycle of said dialing pulse signals comprising:

first timing means having a time period selected to equal a desired transmit pulse-on time length, means for actuating said first timing means upon receipt of a dialing pulse,

second timing means having a time period selected to equal a desired transmit pulse-off time length,

means for actuating said second timing means upon the termination of a received dialing pulse,

means responsive to said first and second timing means for providing output dialing signal pulses that are on during said first recited time period and are off during said second recited time period except when said first time period is still running.

6. In a telephone system, a transmit signaling pulse correction circuit responsive to bilevel DC dialing pulse signals received from local switching circuits for altering the duty cycle of said dialing pulse signals comprising:

first NOR gate means having two inputs and an output,

a first one shot with a predetermined time having an input, and an output,

means for applying said dialing pulse signals to one of the inputs of said first gate means and to said first one-shot input,

means for applying the output of said one shot to the other input of said first gate,

second NOR gate means having two inputs and an output,

a second one shot with a predetermined time having an input and an output,

means for applying the output of said first gate means to one of the inputs of said second gate means and to the input of said second one shot,

means for applying the output of said second one shot to the other input of said second gate means, and

output terminal means connected to the output of said second gate means.

7. The circuit of claim 6 wherein said first and second one shots, respectively comprise:

an input NOR gate having two inputs and an output,

means for applying the one-shot input to one of said input gate inputs,

capacitance means,

resistance means,

an inverter gate having an input and an output,

means for connecting said capacitance means between the output of said input gate and in input of said inverter gate,

means for connecting said resistance means between a source of potential and the input to said inverter gate,

feedback means for connecting said inverter gate output to the other input of said input gate, and

means for taking said one-shot output at said inverter gate output,

and said first and second NOR gate means comprise first and second NOR gates, respectively.

8. In a telephone system, a receive signaling pulse correction circuit responsive to bilevel DC dialing pulse signals representing interrupted tones received from remote signaling units in a carrier trunk system for providing a constant duty cycle output for a range of input pulse rates having varying duty cycles comprising:

recognition timer means receiving said dialing pulse signals for providing a recognition signal output when a pulse exceeds a predetermined minimum time length,

first NOR gate means having two inputs and an output,

means for applying said recognition timer output to one of the inputs of said first gate means,

second NOR gate means having two inputs and an output,

means for applying said dialing pulse signals to one of the inputs of said gate means,

means for connecting said second gate means output to the other input of said first gate means,

trigger delay timer means for providing an output signal when an input signal has been applied for a predetermined time,

hold timer means for providing an output signal when an input signal has been applied for a predetermined time,

third NOR gate means having two inputs and an output,

means for applying the output of said hold timer to one of the inputs of said third gate means,

means for applying said recognition timer output to the other input of said third gate means,

fourth NOR gate means having two inputs and an output,

means for connecting the output of said third gate means to the other input of said second gate means and to one of the inputs of said fourth gate means,

means for connecting the output of said trigger delay means to the other input of said fourth gate means,

variable time constant one-shot means, fifth NOR gate means having two inputs and an output,

means for connecting the output of said fourth gate means to the input of said variable one-shot means and to one of the inputs of said fifth gate means,

means for connecting the output of said variable one-shot means to the other input of said fifth gate means, and

means for taking the corrected pulse output at the output of said fifth gate means.

9. The circuit of claim 8 wherein said first through fifth NOR gate means are NOR gates, respectively.

10. The circuit of claim 9 wherein said recognition timer means comprises:

a sixth NOR gate having two inputs and an output,

a first inverter gate having an input and an output,

first capacitance means,

second resistance means,

a first input terminal for receiving said dialing pulse signals,

means connecting said first input terminal to one of the inputs of said sixth NOR gate,

means for connecting said capacitance means between said input terminal and the input of said inverter gate,

means for connecting said resistance means between said inverter gate input and a source of potential,

means for connecting said inverter gate output to the other input of said sixth NOR gate, and

means for taking said recognition timer output at the output of said sixth NOR gate.

11. The circuit of claim 10 wherein said trigger delay means comprises:

a second input terminal,
a second inverter gate having an input and an output,
second capacitance means,
second resistance means,
means for connecting said capacitance means between said second input terminal and the input of said second inverter gate,
means for connecting said resistance means between a source of potential and the input of said second inverter gate, and
means for taking said trigger delay means output at the output of said second inverter gate.

12. The circuit of claim 11 wherein said hold timer comprises:
a third input terminal,
a third inverter gate,
third capacitance means,
means for connecting said capacitance means between said third input terminal and the input of said third inverter gate,
means for connecting said resistance means between a source of potential and the input of said third inverter gate, and
means for taking said hold timer output at the output of said third inverter gate.

13. The circuit of claim 12 wherein said variable time constant one-shot means comprises:
a fourth inverter gate having an input and an output,
a fifth inverter gate having an input and an output,
a seventh NOR gate having two inputs and an output,
a fourth input terminal,
fourth resistance means,
fifth resistance means,
sixth resistance means,
fourth capacitance means,
means for connecting said input terminal to the input of said fourth inverter gate and to one of the inputs of said seventh NOR gate,
means for connecting said fourth and fifth resistance means in series between a source of potential and the input to said fifth inverter gate,
means for connecting the output of said fourth inverter gate to the junction of said fourth and fifth resistance means,
means for connecting said sixth resistance means between said source of potential and the input to said fifth inverter gate,
means for connecting said capacitance means between the output of said seventh NOR gate and the input of said fifth inverter gate,
means for connecting the output of said fifth inverter gate to the other input of said seventh NOR gate, and
means for taking said variable one-shot output at the output of said fifth inverter gate.

14. In a telephone system, a transmit signaling pulse correction circuit responsive to bilevel DC dialing pulse signals received from local switching circuits for altering the duty cycle of said dialing pulse signals comprising:
first timing means for generating a first signal having a time period selected to equal a desired transmit pulse-off time length upon receipt of an initiating signal,
means for applying an initiating signal to said first timing means upon the termination of a received dialing pulse;
second timing means for generating a second signal having a time period selected to equal a desired transmit pulse-on time length upon receipt of an initiating signal,
means for applying an initiating signal to said second timing means upon receipt of a dialing pulse when said first timing means is not generating a first signal, and
means responsive to said first and second signals for providing output dialing pulses that are on when said second signal is generated and that are off when said first signal is generated and said second signal is not generated.

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