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(54) **POLAR TRANSMITTER AND METHOD FOR GENERATING A TRANSMIT SIGNAL USING A POLAR TRANSMITTER**

POLARSENDER UND VERFAHREN ZUR ERZEUGUNG EINES SENDESIGNALS ÜBER EINEN POLARSENDER

ÉMETTEUR POLAIRE ET PROCÉDÉ PERMETTANT DE GÉNÉRER UN SIGNAL D'ÉMISSION AU MOYEN D'UN ÉMETTEUR POLAIRE

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Description

Technical field

[0001] The present disclosure relates to a polar transmitter provided for transmitting a phase/frequency modulated and amplitude modulated transmit signal, and to a method for generating a transmit signal using a polar transmitter.

Background art

[0002] A typical polar transmitter, such as for example described in [3], and shown schematically in Figure 1, consists of a phase/frequency modulating phase-locked loop 4, PLL, and an amplitude modulating digital power amplifier 16, DPA, as a digital amplitude modulator, DAM. These two blocks are connected serially as shown in Figure 1.

[0003] Such polar transmitters have the disadvantage that they are limited by the noise in the system, PLL and DPA bandwidth, both, phase/frequency modulator and DPA linearity. Furthermore, the DPA amplitude modulation can induce parasitic phase/frequency modulation, i.e. AM-to-PM distortion. Also, phase/frequency modulation can result in unwanted amplitude modulation, i.e. PM-to-AM distortion.

[0004] WO-A-01/24356 discloses a PLL for phase modulation in radio transmitters. The PLL comprises a DAM and a limiter to remove amplitude information from signal that is fed back into the phase detector in the PLL.

Summary of the disclosure

[0005] It is an aim of the present disclosure to provide a polar transmitter wherein typical PLL bandwidth limitations are overcome while maintaining optimal phase-noise filtering, and allows on-line calibration of the DAM linearity, phase-error detector linearity and on-line suppression of PM-to-AM and AM-to-PM distortion.

[0006] This aim is achieved according to the disclosure with a polar transmitter showing the technical characteristics of the first independent claim.

[0007] As used herein, "phase/frequency modulation" is intended to mean phase modulation or frequency modulation of a signal. Hence, a "phase/frequency modulated signal" means a signal which has been modulated in phase or frequency.

[0008] The present disclosure provides a polar transmitter provided for transmitting or outputting a phase/frequency modulated and amplitude modulated transmit signal. The polar transmitter comprises a phase locked loop, PLL, for generating a phase/frequency modulated precursor of the transmit signal. The PLL comprises at its input a phase error detection unit for detecting a phase error of a feedback signal which is fed back from the output of the PLL to the phase error detection unit. The polar transmitter comprises a digital amplitude modulator, DAM, for amplitude modulation of the precursor, resulting in transmit signal. The digital amplitude modulator is arranged within the PLL for amplitude modulation of the precursor before being output by the PLL and the feedback signal is the transmit signal or a derivation thereof. The digital amplitude modulator may for example be a digital power amplifier, DPA. The phase error detection unit is further provided for detecting the amplitude of the feedback signal.

[0009] Integrating the digital amplitude modulator into the PLL and providing the phase error detection unit for detecting or sensing the amplitude of the feedback signal offers the advantage that instead of only the phase/frequency modulation and any imperfections of the PLL components also the amplitude modulation and any imperfections of the DAM are fed back from the output of the PLL to the phase error detection unit. As such, iterative calibration of the precursor, and thus finally the transmit signal for, for example, nonlinearities in digital to phase/frequency and digital to amplitude conversion and for Phase Modulation to Amplitude Modulation, PM-to-AM, and Amplitude Modulation to Phase Modulation, AM-to-PM, distortions may readily be implemented into the polar transmitter, preferably in the background while the polar transmitter operates normally.

[0010] The feedback signal is preferably the transmit signal. Alternatively, the feedback signal may also be a useful derivation of the transmit signal, for example a filtered signal. An example is a sharp band-pass filter around the fundamental local oscillator frequency with bandwidth equal to the modulation bandwidth, so that the phase error detection unit only senses the part of the spectrum of interest. Another example of a block that could be used in the feedback path is another amplitude modulator which would compensate for the amplitude modulation of the output signal through the DPA. This block would then apply an inverse of the DPA modulation signal so that the phase error detection unit always senses the same amplitude.

[0011] In the present invention the digital amplitude modulator is arranged at the output of the PLL.

[0012] Arranging the digital amplitude modulator at the output of the PLL offers the advantage that the amplitude modulated precursor, thus the transmit signal, may directly be fed back to the phase detection unit at the input of the PLL, without any further amplitude modulation of the transmit signal, which might introduce additional errors further complicating any calibration of the transmit signal within the PLL.

[0013] In the present invention the phase error detection unit is provided for sub-sampling at a reference rate of the feedback signal.

[0014] Sub-sampling at a reference rate of the feedback signal is a beneficial and easy means of obtaining both phase error information and amplitude information from the feedback signal, and thus the transmit signal, without requiring separate detection mechanisms.

[0015] In the present invention the phase error detection unit comprises an analog-to-digital convertor, ADC, for generating a phase error code proportional to the phase error and the amplitude of the feedback signal.

[0016] In an embodiment of the polar transmitter according to the present disclosure the PLL is a sub-sampling PLL. The PLL comprises a controllable oscillator for generating the precursor by means of a frequency modulation input signal. The PLL comprises the digital amplitude modulator for amplitude modulation of the precursor by means of an amplitude modulation signal. The PLL comprises a phase error detection unit. The phase error detection unit is provided for sub-sampling at a reference rate of the feedback signal. The phase error detection unit is provided for generating a phase error code proportional to the sub-sampled feedback signal by means of an ADC. The phase error code is used for adjusting the phase of the precursor generated by the controllable oscillator. Preferably, the phase error detection unit comprises a Digital-to-Time Converter, DTC, for delaying the sub-sampling of the feedback signal to enable phase modulation of the precursor and/or fractional residue compensation. Preferably, the DTC is a DTC with a known quantization accuracy, hence a known Least-Significant-Bit, LSB expressed in seconds.

[0017] The use of the sub-sampling PLL arranged as such offers the advantage that calibration of the transmit signal may readily be implemented in the digital domain and run in the background while the polar transmitter operates normally.

[0018] In the polar transmitter according to the present invention the PLL is arranged for rescaling the phase error code by means of the amplitude modulation signal.

[0019] This embodiment offers the advantage that the a constant loop gain is maintained in the part of the PLL following the phase error detection unit, such that the operating range of the part of the PLL following the phase error detection unit does not need to be adapted to the amplitude changes of the precursor caused by the amplitude modulation by means of the digital amplitude modulator.

[0020] In an embodiment of the polar transmitter according to the present disclosure the polar transmitter comprises a calibration loop for calibration of the transmit signal for predetermined phase shifts. The calibration loop is provided for calculating the phase error detection gain defined by the controllable oscillator output amplitude, the DAM gain and the ADC gain. The phase error detection gain is iteratively calculated from the correlation between the predetermined phase shift and an error signal. The error signal is derived from the phase error code by subtracting the predetermined phase shift scaled by the calculated phase error detection gain. Preferably, the correlation between the predetermined phase shift and the error signal is obtained by multiplying the predetermined phase shift with the error signal and by integrating the multiplication result.

[0021] Advantageously, the phase error detection gain can be estimated in the background while the polar transmitter operates normally by using the correlation between the predetermined phase shift and the error signal. The error signal is calculated in every reference cycle as the phase error code from the ADC corrected for the predetermined phase shift scaled by an estimate of the phase error detection gain. In case the correct estimate for the phase error detection gain is known, there is no correlation between the predetermined phase shift and the error signal from which the predetermined phase shift is removed. If the correct estimate of the phase error detection gain is, however, not known, correlation between the predetermined phase shift and the error signal does exist. This correlation can be used to calculate phase error detection gain in the background while the polar transmitter operates normally. The phase error detection gain is iteratively calculated by multiplying the predetermined phase shift with the error signal and by integrating the multiplication result. Iterative repetition of this process results in an accurate estimate of the phase error detection gain and hence to an effective removal of any predetermined phase shift present in the error signal.

[0022] In an embodiment of the polar transmitter according to the present disclosure the predetermined phase shift is one of a known quantization error of a component of the polar transmitter and a phase shift especially induced by a phase modulating component of the polar transmitter for the purpose of calibrating the transmit signal.

[0023] In an embodiment of the polar transmitter according to the present disclosure the calibration loop is provided for calibration of the transmit signal for DAM nonlinearity. Therefore, the amplitude modulation signal is corrected with a DAM nonlinearity correction value from DAM nonlinearity correction values stored in a DAM nonlinearity look-up-table, LUT. The DAM nonlinearity correction values are derived from the amplitude modulation signal and the product of the predetermined phase shift and the error signal. The DAM nonlinearity LUT is iteratively updated by means of the product of the predetermined phase shift and the error signal. The amplitude modulation signal is used for continuous addressing of the DAM nonlinearity LUT.

[0024] Advantageously, the DAM nonlinearity can be estimated in the background while the polar transmitter operates normally by using the correlation between the product of the predetermined phase shift and the error signal on the one side and the amplitude modulation signal on the other side for updating a DAM nonlinearity LUT. The DAM nonlinearity LUT may be used to retrieve a DAM nonlinearity correction value for a certain amplitude modulation signal. This DAM

nonlinearity correction value is then used for pre-distorting the amplitude modulation signal to remove the influence from the DAM nonlinearity from the transmit signal. In case of a linear DAM and if the correct value for the phase error detection gain is known, the product of the predetermined phase shift and the error signal for updating the LUT is completely independent of a particular amplitude modulation signal and has a zero mean value. Hence, no correction is applied to the amplitude modulation signal. In case of a nonlinear DAM, however, the product updates the LUT with a non-zero stream, and hence the amplitude modulation signal is pre-distorted by the DAM nonlinearity correction value retrieved from the LUT.

[0025] The use of the LUT and the simple calculation for updating the LUT offers the advantage that the transmit signal may be calibrated for DAM nonlinearity in the background, without thereby disturbing the normal operation of the polar transmitter.

[0026] In an embodiment of the polar transmitter according to the present disclosure the calibration loop is provided for calibration of the transmit signal for ADC nonlinearity. Therefore, the error signal is corrected with an ADC nonlinearity correction value from ADC nonlinearity correction values stored in an ADC nonlinearity LUT. The ADC nonlinearity correction values are derived from the phase error code and the corrected error signal. The ADC nonlinearity LUT is iteratively updated by means of the corrected error signal. The phase error code is used for continuous addressing of the ADC nonlinearity LUT.

[0027] Advantageously, the ADC nonlinearity can be estimated in the background while the polar transmitter operates normally by using the correlation between the error signal corrected for ADC nonlinearity and the phase error code output of the ADC for updating an ADC nonlinearity LUT. The ADC nonlinearity LUT may be used to retrieve an ADC nonlinearity correction value for a certain phase error code. This ADC nonlinearity correction value is then used for post-distorting the error signal to remove the influence from the ADC nonlinearity from the transmit signal. In case of a linear ADC the corrected error signal for updating the LUT is completely independent of a particular phase error code and has a zero mean value. Hence, no correction is applied to the error signal. In case of a nonlinear ADC, however, the corrected error signal updates the LUT with a non-zero stream, and hence the error signal is post-distorted by the ADC nonlinearity correction value retrieved from the LUT.

[0028] The use of the LUT and the simple calculation for updating the LUT offers the advantage that the transmit signal may be calibrated for ADC nonlinearity in the background, without thereby disturbing the normal operation of the polar transmitter.

[0029] In an embodiment of the polar transmitter according to the present disclosure the calibration loop is provided for calibration of the transmit signal for amplitude modulation to phase modulation distortion, AM-to-PM distortion. Therefore, the frequency modulation signal is corrected by a frequency modulation correction value from frequency modulation correction values stored in an AM-to-PM distortion LUT. The frequency modulation correction values are derived from the amplitude modulation signal and the error signal. The AM-to-PM distortion LUT is iteratively updated by means of the error signal. The amplitude modulation signal is used for continuous addressing of the AM-to-PM distortion LUT.

[0030] Advantageously, the AM-to-PM transfer function can be estimated in the background while the polar transmitter operates normally by using the correlation between the error signal and the amplitude modulation signal for updating an AM-to-PM distortion LUT. The AM-to-PM distortion LUT may be used to retrieve a frequency modulation correction value for a certain amplitude modulation signal. This frequency modulation correction value is then used for pre-distorting the frequency modulation signal to remove the influence from the DAM on the frequency modulation of the transmit signal. In case the DAM has no influence on the frequency modulation of the precursor, and thus the transmit signal, then the error signal for updating the LUT is completely independent of a particular amplitude modulation signal and has thus a zero mean value. Hence, no correction is applied to the frequency modulation signal. In case of the DAM having an influence on the frequency modulation of the precursor, and thus the transmit signal, however, the error signal updates the LUT with a non-zero stream, and hence the frequency modulation signal is pre-distorted by the frequency modulation correction value retrieved from the LUT.

[0031] The use of the LUT and the simple calculation for updating the LUT offers the advantage that the transmit signal may be calibrated for AM-to-PM distortion in the background, without thereby disturbing the normal operation of the polar transmitter.

[0032] In an embodiment of the polar transmitter according to the present disclosure the calibration loop is provided for calibration of the transmit signal for phase modulation to amplitude modulation distortion, PM-to-AM distortion. Therefore, the amplitude modulation signal is corrected by an amplitude modulation correction value from amplitude modulation correction values stored in a PM-to-AM distortion LUT. The amplitude modulation correction values are derived from the frequency modulation signal and the product of the predetermined phase shift and the error signal. The PM-to-AM distortion LUT is iteratively updated by means of the product of the predetermined phase shift and the error signal. The frequency modulation signal is used for continuous addressing of the PM-to-AM distortion LUT.

[0033] Advantageously, the PM-to-AM transfer function can be estimated in the background while the polar transmitter operates normally by using the correlation between the product of the predetermined phase shift and error signal on the one side and the frequency modulation signal on the other side for updating a PM-to-AM distortion LUT. The PM-to-AM

distortion LUT may be used to retrieve an amplitude modulation correction value for a certain frequency modulation signal. This amplitude modulation correction value is then used for pre-distorting the amplitude modulation signal to remove the influence from the controllable oscillator on the amplitude modulation of the precursor, and thus the transmit signal. In case the controllable oscillator has no influence on the amplitude modulation of the precursor, and thus transmit signal, the product of the predetermined phase shift and the error signal for updating the LUT is completely independent of a particular frequency modulation signal and has thus a zero mean value. Hence, no correction is applied to the amplitude modulation signal. In case of the controllable oscillator having an influence on the amplitude modulation of the precursor, and thus the transmit signal, however, the product of the predetermined phase shift and the error signal updates the LUT with a non-zero stream, and hence the amplitude modulation signal is pre-distorted by the amplitude modulation correction value retrieved from the LUT.

[0034] The use of the LUT and the simple calculation for updating the LUT offers the advantage that the transmit signal may be calibrated for PM-to-AM distortion in the background, without thereby disturbing the normal operation of the polar transmitter.

[0035] In an embodiment of the polar transmitter according to the present disclosure the correlation value for calculating the phase error detection gain and/or the value for updating the LUT is scaled by a scaling factor for controlling the convergence speed of the calibration of the transmit signal. The correlation value for calculating the phase error detection gain is the correlation between the predetermined phase shift and the error signal. The value for updating the LUT is the product of the predetermined phase shift and the error signal in case of the DAM nonlinearity LUT, the corrected error signal in case of the ADC nonlinearity LUT, the error signal in case of the AM-to-PM distortion LUT, and the product of the predetermined phase shift and the error signal in case of the PM-to-AM distortion LUT.

[0036] The use of the scaling factor offers the advantage of a simple and quick control on the speed with which the transmit signal may be calibrated.

[0037] Furthermore, the present disclosure provides a method for generating a phase/frequency modulated and amplitude modulated transmit signal by means of a polar transmitter according to claim 9.

[0038] The advantages of the method according to the present disclosure and its embodiments are similar to those discussed with respect to the polar transmitter according to the present disclosure and its embodiments.

[0039] In an embodiment of the method according to the present disclosure the amplitude modulation of the precursor by means of the digital amplitude modulator is done at the output of the PLL.

[0040] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the transmit signal is calibrated for predetermined phase shifts by calculating the error signal by subtracting from the phase error code the predetermined phase shift scaled by a first estimate of the phase error detection gain defined by the controllable oscillator output amplitude, the DAM gain and the ADC gain, by calculating a further estimate of the phase error detection gain from the correlation between the predetermined phase shift and the error signal, and by iteratively repeating the above steps using the further estimate of the phase error detection gain until saturation, i.e. when the product of the predetermined phase shift and the error signal becomes a zero mean signal.

[0041] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the predetermined phase shift is one of a known quantization error of a component of the polar transmitter and a phase shift especially induced by a phase modulating component of the polar transmitter for the purpose of calibrating the transmit signal.

[0042] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the transmit signal is further calibrated for DAM nonlinearity by retrieving a DAM nonlinearity correction value by addressing a DAM nonlinearity LUT with the amplitude modulation signal, by correcting the amplitude modulation signal by subtracting the retrieved DAM nonlinearity correction value, by updating the DAM nonlinearity LUT by means of the product of the predetermined phase shift and the error signal, and by iteratively repeating the above steps until saturation of the DAM nonlinearity LUT. The DAM nonlinearity LUT stores DAM nonlinearity correction values derived from the amplitude modulation signal and the product of the predetermined phase shift and the error signal.

[0043] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the transmit signal is further calibrated for ADC nonlinearity by retrieving an ADC nonlinearity correction value by addressing an ADC nonlinearity LUT with the phase error code, by correcting the error signal by subtracting the retrieved ADC nonlinearity correction value, by updating the ADC nonlinearity LUT by means of the corrected error signal, and by iteratively repeating the above steps until saturation of the ADC nonlinearity LUT. The ADC nonlinearity LUT stores ADC nonlinearity correction values derived from the phase error code and the corrected error signal.

[0044] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the transmit signal is further calibrated for AM-to-PM distortion by retrieving a frequency modulation correction value by addressing an AM-to-PM distortion LUT with the amplitude

modulation signal, by correcting the frequency modulation signal by subtracting the retrieved frequency modulation correction value, by updating the AM-to-PM distortion LUT by means of the error signal, and by iteratively repeating the above steps until saturation of the AM-to-PM distortion LUT. The AM-to-PM distortion LUT stores frequency modulation correction values derived from the amplitude modulation signal and the error signal.

[0045] In an embodiment of the method according to the present disclosure for operating the polar transmitter according to the present disclosure comprising the calibration loop, the transmit signal is further calibrated for PM-to-AM distortion by retrieving an amplitude modulation correction value by addressing a PM-to-AM distortion LUT (28) with the frequency modulation signal, by correcting the amplitude modulation signal by subtracting the retrieved amplitude modulation correction value, by updating the PM-to-AM distortion LUT by means of the product of the predetermined phase shift and the error signal, and by iteratively repeating the above steps until saturation of the PM-to-AM distortion LUT. The PM-to-AM distortion LUT stores amplitude modulation correction values derived from the frequency modulation signal and the product of the predetermined phase shift and the error signal.

[0046] In an embodiment of the method according to the present disclosure the correlation value for calculating the phase error detection gain and/or the value for updating the LUT is scaled by a scaling factor for controlling the convergence speed of the calibration of the transmit signal.

Brief description of the drawings

[0047] The disclosure will be further elucidated by means of the following description and the appended figures.

Figure 1 shows a polar transmitter according to prior art.
Figure 2 shows an embodiment of a polar transmitter according to the present invention.
Figure 3 shows a representation of the polar transmitter of Figure 2 in the phase domain.
Figure 4 shows a further embodiment of the polar transmitter of Figure 3.
Figure 5 shows a further embodiment of the polar transmitter of Figure 4.
Figure 6 shows a further embodiment of the polar transmitter of Figure 5.
Figure 7 shows a further embodiment of the polar transmitter of Figure 6.
Figure 8 shows a further embodiment of the polar transmitter of Figure 7.
Figure 9 shows test results of the polar transmitter of Figure 8.

Detailed description of preferred embodiments

[0048] The present disclosure will be described with respect to particular embodiments and with reference to certain drawings but the disclosure is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not necessarily correspond to actual reductions to practice of the disclosure.

[0049] Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. The terms are interchangeable under appropriate circumstances and the embodiments of the disclosure can operate in other sequences than described or illustrated herein.

[0050] Moreover, the terms top, bottom, over, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. The terms so used are interchangeable under appropriate circumstances and the embodiments of the disclosure described herein can operate in other orientations than described or illustrated herein.

[0051] Furthermore, the various embodiments, although referred to as "preferred" are to be construed as exemplary manners in which the disclosure may be implemented rather than as limiting the scope of the disclosure.

[0052] The term "comprising", used in the claims, should not be interpreted as being restricted to the elements or steps listed thereafter; it does not exclude other elements or steps. It needs to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising A and B" should not be limited to devices consisting only of components A and B, rather with respect to the present disclosure, the only enumerated components of the device are A and B, and further the claim should be interpreted as including equivalents of those components.

[0053] A simplified block diagram of a Digital Sub-Sampling Polar Transmitter 1, DSSTx, according to an embodiment of the present disclosure is depicted in Figure 2. The transmitter 1, TX, is based on a digitized Fractional-N Sub-Sampling PLL 4 (FNSSPLL) and a digitally tuneable gain power amplifier 16, DPA, as a digital amplitude modulator. Preferably, the DPA is placed at the output of the PLL 4, and thus serves to close the PLL 4.

[0054] The transmitter 1 operates as a Sub-Sampling PLL 4, SSPLL, when there is no modulation. The high frequency output sinewave of the voltage controlled oscillator 5, VCO, is first amplified by a constant gain DPA 16 and then directly (no division) sub-sampled at the low-frequency reference rate. If there is no mismatch between the input and the output phase, the VCO output sinewave zero-crossings are sub-sampled, i.e. the ADC 10 outputs a zero. If, however, there is some mismatch between the output and the input phase, a non-zero voltage is sub-sampled, and the ADC 10 produces as output code a phase error code 11, linearly proportional to the phase error. This phase error code 11 is digitally low-pass filtered by the low-pass filter 13, LPF, and sent through a digital-to-analog converter 31, DAC, to adjust the VCO output phase (forcing a zero phase offset condition). The Digital-to-Time Converter 12, DTC, is completely transparent during integer-N PLL operation (integer multiplication of the input frequency), while, in fractional-N operation mode, it serves for fractional residue compensation [2]. In other words, the DTC 12 delays the sampling instant by a predetermined delay to force near-to-zero voltage sample during a fractional-N lock.

[0055] Notably, the proposed architecture has a linear phase error detection gain defined by:

$$G_{PD} = AVCO \cdot G_{DPA} \cdot G_{ADC}, \qquad (1)$$

where AVCO is the VCO output sinewave amplitude, G_{DPA} is the DPA gain and G_{ADC} is the gain of the ADC 10. The G_{PD} can be set high enough to suppress the in-loop phase-noise (sampler noise) well below the reference and the VCO phase noise contribution. Advantageously, a sub-sampling PLL 4 has no divider (and hence no divider originated noise) which results in a better phase noise performance compared to classical analog or digital PLL. The high detection gain imposes no issues with loop stability since the digital low-pass filter 13 is easily adjusted (the analog filter equivalent would potentially need a large, area consuming capacitor).

[0056] PLL architectures based on a fractional-N sub-sampling phase error detection, for example as described in [1], have been used up to now for phase/frequency modulation only. In those architectures the phase/frequency modulation bandwidth is not limited by the PLL filtering since a two point-injection scheme similar to [4] can be used. This is achieved by sending the same frequency modulation data, but with an opposite sign, expressed as accumulated phase, to the DTC which then re-adjusts the delay for zero-crossing sampling (letting the modulated phase/frequency through). Namely, the frequency modulation data sent to the PLL output is ignored by the phase-error detector, i.e. the sampler. This also allows to background calibrate for potential DTC/DAC gain mismatch [4], delay spread [4] and DTC/DAC integral non-linearity, INL [5].

[0057] Herein, it is proposed to use this architecture for amplitude modulation also. This is achieved by including a DPA 16 in the SSPLL 4, as shown in Figure 2, wherein DPA acts as an amplitude modulator. The sampled voltage hence contains both amplitude and phase information, partly from intended AM and PM modulation, and partly from imperfections in the system. As a result, the phase detection mechanism in the SSPLL 4 becomes sensitive to the amplitude of the output signal as well, and it can also be used to monitor, control, and/or correct the amplitude modulation of a polar transmitter 1 in addition to the phase/frequency modulation.

[0058] Advantageously, the proposed polar transmitter allows to use the information available in the output signal 11 of the phase detector 8 to monitor and control the gain of the blocks in the transmitter, and to characterize and correct imperfections such as nonlinearities, AM-to-PM distortion, PM-to-AM distortion, etc. For this purpose, several algorithms are described herein, which may be run either in background or in foreground, thereby ensuring a high-quality modulated output 2.

[0059] Figure 3 depicts a phase-domain model of the Digital Sub-Sampling Polar Transmitter 1 of Figure 2. The VCO 5 is modeled as a digital integrator that is driven by a DAC 31. The sub-sampling of the VCO output ϕ_{VCO} is modeled as subtraction of the VCO phase (ϕ_{VCO}) and the reference phase ($\phi_{REF} + \phi_{DTC}$). In actual implementation, the sub-sampling is carried out at the DPA output, but for the phase-domain model it is assumed that the DPA 16 does not change the instantaneous VCO phase, i.e. that the $\phi_{VCO} - \phi_{DPA} \cdot \phi_{DTC}$ represents the phase modulation signal plus the fractional residue compensation signal (necessary during a fractional lock). If there is no mismatch between the input and the output phase, ideally, the result of this subtraction is zero, however, since the DTC 12 has limited resolution, a phase quantization error 19 is produced.

[0060] The phase quantization error 19 (which may contain a random, noise originated phase error) is then transferred into the voltage domain by sub-sampling. The sub-sampling is modelled with the following expression (V_{sample} is the voltage value received at the ADC input):

$$V_{sample} = AVCO \cdot G_{DPA} * \sin(\phi_{VCO} - \phi_{REF} - \phi_{DTC}). \qquad (2)$$

The DPA gain, G_{DPA}, is constant if there is no amplitude modulation in the transmitter 1. However, during amplitude modulation, the DPA gain is changing (w.r.t. the DPA Gain code 17, i.e. the amplitude modulation signal), which results

in scaling of the sub-sampled voltage 9, accordingly. The ADC 10 quantizes the sub-sampled voltage level - producing a digital code 11. To maintain a constant loop gain (during amplitude modulation) the ADC digital output 11 is rescaled with (i.e. divided by) the amplitude of the modulation data 17, as shown in the Figure 3. Finally, the rescaled ADC output is filtered through the digital low-pass-filter 13. The frequency modulation data 6 (equivalent to the DTC phase modulation data input, with opposite sign) is added to the LPF output. The resulting signal drives a DAC 31, which adjust the DPA output in a zero phase offset condition w.r.t. the input phase.

1. Background calibration mechanisms

a. Estimation and calibration of the phase-error detection gain

[0061] The phase-error detection gain, G_{PD}, is a value dependent on analog settings of the PLL 4, which are difficult to accurately determine in the design phase. Added to Figure 4 with respect to Figure 3, the calibration loop 181 is shown which enables tracking of the phase-error detection gain (G_{PD}) in the background, while the polar transmitter 1 operates normally.

[0062] The phase-error detector gain estimation is based on correlation of a predetermined phase shift 19, in this case the DTC quantization error 19, with the ADC output data stream, i.e. the error signal 20. The predetermined phase shift may, however, be any other suitable phase shift that is present or especially induced for calibration purposes in the signals of the polar transmitter 1. The predetermined phase shift may, for example, also be a DAC quantization error or a quantization error of another component of the polar transmitter 1. The predetermined phase shift may, for example, also be a phase shift especially induced for calibration purposes by phase modulating components of the polar transmitter 1, such as the DAC 31 of the DTC 12.

[0063] The algorithm is based on the following: since the exact quantization error 19 introduced by the DTC 12 (in every sampling event) is known (in the digital domain), it is possible to simply subtract the same phase-error 19 (appropriately scaled by G_{PD}) from the ADC output 11 (as depicted in Figure 4). The error signal 20 is then "clean" of the DTC quantization error 19, and contains just the random noise originated phase error information. Hence, if the G_{PD} factor is determined accurately, the error signal 20 in Figure 4 is completely uncorrelated with the DTC quantization error 19. If this is not the case, i.e. if there exists some correlation between the DTC quantization error 19 and the error signal 20, the value of the G_{PD} needs to be re-adjusted. To estimate G_{PD} in the background, the quantization error 19 is multiplied with the error signal 20 and the multiplication result is integrated, which directly realizes correlation estimation between the two signals. The integrator output is set to an initial G_{PD} estimate, and then changes towards the positive, or negative infinity (depending on the initial estimate error sign), until it saturates in the real G_{PD} value. Advantageously, the multiplication result may be scaled with a factor g 41 which controls the convergence speed of the G_{PD} estimation. The settled G_{PD} estimate is a measure of the phase error detection gain. An unwanted G_{PD} value can be corrected by rescaling the ADC output with a fixed value, by changing the VCO oscillation amplitude or by readjusting the DPA gain.

b. Calibration of DPA nonlinearity

[0064] A nonlinear DPA 26 can significantly degrade the overall transmitter performance. A DSSTx 1 allows background calibration of the DPA nonlinearity, since, in this architecture specifically, the phase error detector gain depends also on the DPA gain,since the DPA 26 is within the phase-locked loop 4.

[0065] The integral nonlinearity ,INL, of the DPA is estimated based on correlation of the DTC quantization error 19 and the product of the phase error signal 20 with a particular DPA code 17. A possible way to realize the estimation is by application of a DPA INL look-up-table ,LUT. The multiplication product of the DTC quantization error 19 and the phase error signal 20 is accumulated in every reference cycle to a particular DPA INL LUT 21 address (see parts added in Figure 5 with respect to Figure 4). The LUT address to which the new value is accumulated in every reference cycle is determined with the instantaneous DPA code.

[0066] In case of a correct G_{PD} (this is inherent since the previous calibration algorithm is turned on) and a linear DPA 16, the DTC quantization error 19 and the error signal 20 product has a zero mean value per particular DPA Gain 17. This results in a LUT 21 which accumulates zeros to every of the LUT addresses. For a nonlinear DPA 16, however, the LUT 21 is updated in every cycle with non-zero mean values per particular address (or DPA Gain). Therefore, the values in the LUT 21 drift towards more positive or negative numbers depending on the DPA INL error sign and saturate at an appropriate INL estimate. The LUT values are simultaneously used for estimation and correction (digital pre-distortion) of the DPA nonlinearity. This is realized by subtracting the INL error 22 for the respective DPA code 17 (i.e. the INL value stored at the corresponding LUT address) from the original DPA code 17 (see Figure 5), hence, removing the nonlinearity of the DPA 16 in the digital domain (pre-distortion).

[0067] Each value used to update the appropriate LUT address, i.e. each value accumulated to the appropriate LUT address for INL estimation, may be scaled with a factor a 42 which controls the convergence speed of the DPA INL error

estimation. The estimation of the DPA INL and the correction/pre-distortion may be run in the background or in the foreground, together with the previous calibration algorithm, while the transmitter 1 operates normally.

c. Calibration of the ADC nonlinearity

[0068] The ADC 10 in the DSSTx 1 is part of the phase-error detection chain 8 and can be nonlinear as well, which results in a potential performance degradation, e.g. because of unwanted PLL gain/bandwidth modulation and/or potential calibration accuracy degradation. For this reason there is proposed herein an on-line ADC nonlinearity calibration (see parts of Figure 6 added with respect to Figure 5).

[0069] The calibration is based on estimating the correlation between the corrected error signal 25 and appropriate ADC output codes 11. In the case of a linear ADC 10 the error signal 20 and hence the corrected error signal 25 are independent of the particular ADC output code 11, without the correction being applied at all. This is because the DTC quantization error 19 gets accurately removed from the ADC output code 11 and only zero mean random noise and zero mean ADC quantization noise remain in the error signal 20 per particular ADC output code 11.

[0070] In case of a nonlinear ADC 10, the error signal 20 is influenced by the ADC INL. Indeed, subtracting the DTC quantization error 19 from the ADC output code 11 does not result in the error signal 20 being a random zero mean signal per particular ADC output code 11. In fact, the resulting signal is heavily influenced by a nonlinear ADC. Herein, it is proposed to use a LUT 23 which stores values that represent the ADC INL, to compensate for this effect. The correction values stored in the ADC INL LUT 23 at appropriate addresses defined with ADC output code 11 are subtracted from the error signal 20. In case of a perfect INL error cancellation, i.e. in case of an accurate ADC INL estimate in the ADC INL LUT 23, the corrected error signal 25 is a zero-mean signal per particular ADC output code 11. For an imperfect cancellation this is not true and, hence, the LUT 23 needs to be updated. In every cycle, the instantaneous corrected error signal value 25 is added at the appropriate write address in the ADC INL LUT 23. The write address is calculated based on the DTC quantization error 19 scaled by the phase error detection gain. This forces a drift of the LUT coefficients towards values which represent the ADC INL correctly.

[0071] Advantageously, the corrected error signal 25 value may be scaled with a factor b 43, before its addition to the appropriate address, to control the algorithm convergence speed. Again, the calibration algorithm runs in the background, together with the calibrations described above while the DSSTx 1 runs normally. Alternatively, the ADC nonlinearity calibration may also be run in the foreground.

d. Suppression of the AM-to-PM distortion

[0072] For the phase-domain model of the transmitter 1, it was assumed that the DPA 16 modulates the amplitude and has no influence on phase. In an actual implementation, this is not the case, because the amplitude modulation typically induces some unwanted phase/frequency modulation. This effect is known as amplitude-to-phase distortion (AM-to-PM distortion) and can significantly degrade the transmitting quality.

[0073] The proposed DSSTx 1 architecture is capable of on-line AM-to-PM distortion calibration (see parts added in Figure 7 with respect to Figure 6). The calibration is based on observation of the error signal 20, which is correlated with the DPA gain 17 in case of pronounced AM-to-PM distortion. Similarly to the calibration techniques of the present disclosure described above, this effect is exploited in order to estimate the AM-to-PM transfer function, and to cancel the distortion effect by DAC input code 6 re-modulation. In other words, if the parasitic phase shift introduced by the DPA 16 is known, then the VCO 5 and DAC 31 can be pre-distorted to compensate for it.

[0074] The AM-to-PM distortion LUT 26 is populated with coefficients which represent the AM-to-PM distortion function. If the compensation is ideal, the error signal 20 is independent of the DPA Gain 17, i.e. the error signal 20 is a zero-mean stream per particular DPA Gain code 17. This is not true in case of an imperfect cancellation. Therefore, the instantaneous error signal value 20 (optionally scaled by a factor c 44) has to be added to the appropriate address in the AM-to-PM distortion LUT 26 (address defined by DPA Gain 17) to update the LUT cancellation coefficients. The LUT coefficients propagate towards values which accurately represent the AM-to-PM transfer function and then saturate, since this results in accurate distortion cancellation. Cancellation is realized by subtracting the LUT coefficient 27 from the $\omega_{modulation}$ signal 6, before the application to the DAC 31. It is important to note that the error signal 20 is observed in phase domain (at the output of the phase detector 8), while the correction is carried out in the frequency domain (at the DAC 31 input). For that, it is necessary to send a derivative of the LUT correction value 27 (not represented in the figure for higher clarity) to the modulation DAC 31. Furthermore, it is important to take care of any cycle delays during two point modulation (for example, VCO 5 acts as an integrator - which means that the correction applied by the DAC 31 appears as accumulated phase and not instantaneously).

[0075] Advantageously, the error signal 20 may be scaled with a factor c 44, before its addition to the appropriate address, to control the algorithm convergence speed. The calibration algorithm runs in the background, together with the calibration loops 181-183 described earlier while the DSSTx 1 runs normally.

e. Suppression of the PM-to-AM distortion

[0076] An additional effect which degrades the overall transmitting performance is the PM-to-AM distortion. In the context of the DSSTx 1 for example, the following can happen: changing the VCO operating frequency can result in a parasitic VCO amplitude shift.

[0077] Since the DSSTx 1 is capable of sensing the phase error detector gain, i.e. the amplitude of the output signal, it is possible to correct for parasitic effects such as this one (see parts added in Figure 8 with respect to Figure 7). The idea is to correlate the error signal 20 and the DTC quantization error 19 product with the frequency modulation signal 6. If there is no correlation between the two, there is no distortion as well, i.e. the phase detector gain is kept constant and independent of frequency modulating signal 6. If this is not true, and the correlation exists, a PM-to-AM distortion LUT 28 can be used to estimate the AM-to-PM distortion transfer function, and cancel it by redefining the DPA input code 17 (as depicted in Figure 8).

[0078] In every cycle, the product of the error signal 20 and the DTC quantization error 19 is added to the value at the appropriate LUT address (frequency modulation data 6 is used for addressing). This event repeats itself in every cycle, adjusting the LUT coefficients until the error signal 20 and DTC quantization error 19 product becomes a zero mean signal w.r.t. particular frequency modulation code 6, i.e. until the DPA input code 17 creates just the expected amplitude change, without phase distortion.

[0079] Advantageously, the product signal value may be scaled with a factor d 45, before its addition to the appropriate LUT address, to control the algorithm convergence speed. The calibration algorithm runs in the background, together with the calibration loops 181-184 described earlier while the DSSTx 1 runs normally.

2. Calibration results

[0080] Test results of the calibration of the polar transmitter 1 of Figure 8 are shown in Figure 9. During this test the calibration runs in the background, while the transmitter operates normally.

[0081] Figure 9 shows background calibration loops 181-185 settling within approximately 50 ms. The left column represents correction coefficients detection progress, while the right column shows the final correction estimates (-*-) and ideal correction estimates (+). From top to bottom, the progress of the DPA nonlinearity correction, ADC nonlinearity correction, AM-to-PM distortion correction, and PM-to-AM distortion correction are shown respectively.

[0082] As the calibration loops 181-185 operate independently of one another, all or some of them can be enabled to operate simultaneously. After a calibration reaches convergence, the respective calibration continues to run in the background tracking possible Process-Voltage-Temperature (PVT) variations. The estimated calibration coefficients may be stored in a memory before switching the transmitter off to speed-up the convergence next time when the transmitter 1 is turned on.

References

[0083]

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Claims

1. A polar transmitter (1) provided for transmitting a phase/frequency modulated and amplitude modulated transmit signal (2), the polar transmitter comprising:

a phase locked loop (4), PLL, for generating a phase/frequency modulated precursor (3) of the transmit signal (2) using a controllable oscillator (5), the PLL comprising at its input a phase error detection unit (8) for detecting a phase error of a feedback signal (15) which is fed back from the output of the PLL (4) to the phase error detection unit (8), and

a digital amplitude modulator (16), DAM, arranged within the PLL (4) for amplitude modulation of the precursor (3) by means of an amplitude modulation signal (17) before being output by the PLL (4), resulting in the transmit signal (2), the feedback signal (15) being the transmit signal (2) or being derived therefrom,

characterized in that the phase error detection unit (8) is further provided for sub-sampling at a reference rate of the feedback signal (15), thereby obtaining both phase error information and amplitude information from the feedback signal (15), **in that** the phase error detection unit (8) comprises an analog-to-digital convertor (10), ADC, for generating a phase error code (11) proportional to the phase error and the amplitude sub-sampled feedback signal, and **in that** the PLL (4) is arranged for rescaling the phase error code (11) by means of the amplitude modulation signal (17).

2. The polar transmitter (1) according to claim 1, wherein the PLL (4) is a sub-sampling PLL (4) comprising:

the controllable oscillator (5) for generating the precursor (3) and for frequency modulation of the precursor (3) by means of a frequency modulation signal (6);
the digital amplitude modulator (16);
the phase error detection unit (8)
wherein the phase error code (11) is used for adjusting the phase of the precursor (3) generated by the controllable oscillator (5), the phase error detection unit (8) comprising a digital-to-time converter (12), DTC, for delaying the sub-sampling of the feedback signal (15) to enable phase modulation of the precursor (3) and/or fractional residue compensation.

3. The polar transmitter (1) according to claim 2, comprising a calibration loop (181) for calibration of the transmit signal (2) based on predetermined phase shifts (19), wherein the calibration loop (181) is provided for calculating a phase error detection gain defined by the controllable oscillator output amplitude, a gain of said DAM (16) and a gain of said ADC (10), wherein the phase error detection gain is iteratively calculated from the correlation between a predetermined phase shift (19) and an error signal (20) derived from the phase error code (11) by subtracting the predetermined phase shift (19) scaled by the calculated phase error detection gain.

4. The polar transmitter (1) according to claim 3, wherein the predetermined phase shift (19) is one of a known quantization error (19) of a component of the polar transmitter (1) and a phase shift especially induced by a phase modulating component of the polar transmitter (1) for the purpose of calibrating the transmit signal (2).

5. The polar transmitter (1) according to claim 3 or 4, wherein the calibration loop (182) is provided for calibration of the transmit signal (2) for DAM nonlinearity, wherein the amplitude modulation signal (17) is corrected with a DAM nonlinearity correction value (22) from DAM nonlinearity correction values (22) stored in a DAM nonlinearity look-up-table (21), LUT, and derived from the amplitude modulation signal (17) and the product of the predetermined phase shift (19) and the error signal (20), wherein the DAM nonlinearity LUT (21) is iteratively updated by means of the product of the predetermined phase shift (19) and the error signal (20), and wherein the amplitude modulation signal (17) is used for continuous addressing of the DAM nonlinearity LUT (21).

6. The polar transmitter (1) according to any one of the claims 3-5, wherein the calibration loop (183) is provided for calibration of the transmit signal (2) for ADC nonlinearity, wherein the error signal (20) is corrected with an ADC nonlinearity correction value (24) from ADC nonlinearity correction values (24) stored in an ADC nonlinearity LUT (23) and derived from the phase error code (11) and the corrected error signal (25), wherein the ADC nonlinearity LUT (23) is iteratively updated by means of the corrected error signal (25), and wherein the phase error code (11) is used for continuous addressing of the ADC nonlinearity LUT (23).

7. The polar transmitter (1) according to any one of the claims 3-6, wherein the calibration loop (184) is provided for calibration of the transmit signal (2) for amplitude modulation to phase modulation distortion, AM-to-PM distortion, wherein the frequency modulation signal (6) is corrected by a frequency modulation correction value (27) from frequency modulation correction values (27) stored in an AM-to-PM distortion LUT (26) and derived from the amplitude modulation signal (17) and the error signal (20), wherein the AM-to-PM distortion LUT (26) is iteratively updated by means of the error signal (20), and wherein the amplitude modulation signal (17) is used for continuous addressing of the AM-to-PM distortion LUT (26).

8. The polar transmitter (1) according to any one of the claims 3-7, wherein the calibration loop (185) is provided for calibration of the transmit signal (2) for phase modulation to amplitude modulation distortion, PM-to-AM distortion, wherein the amplitude modulation signal (17) is corrected by an amplitude modulation correction value (29) from amplitude modulation correction values (29) stored in a PM-to-AM distortion LUT (28) and derived from the frequency modulation signal (6) and the product of the predetermined phase shift (19) and the error signal (20), wherein the PM-to-AM distortion LUT (28) is iteratively updated by means of the product of the predetermined phase shift (19) and the error signal (20), and wherein the frequency modulation signal (6) is used for continuous addressing of the PM-to-AM distortion LUT (28).

9. A method for generating a phase/frequency modulated and amplitude modulated transmit signal (2) by means of a polar transmitter (1), wherein a phase/frequency modulated precursor (3) of the transmit signal (2) is generated by means of a controllable oscillator in a phase locked loop (4), PLL, of the polar transmitter (1), wherein a phase error detection unit (8) of the PLL (4) is used for detecting a phase error of a feedback signal (15) which is being fed back from the output of the PLL (4) to the phase error detection unit (8), wherein amplitude modulation of the precursor (3) is done by means of an amplitude modulation signal (17) by a digital amplitude modulator (16), DAM, within the PLL (4) of the polar transmitter (1), resulting in the transmit signal (2), the feedback signal (15) being the transmit signal (2) or derived therefrom, **characterized in that** the phase error detection unit (8) is further used for sub-sampling at a reference rate of the feedback signal (15) in order to obtain both phase error information and amplitude information from the feedback signal (15), **in that** an analog-to-digital convertor, ADC, within the phase error detection unit (8) is used for generating a phase error code (11) proportional to the sub-sampled feedback signal, and **in that** the amplitude modulation signal (17) is used for rescaling the phase error code (11).

10. The method according to claim 9, using a polar transmitter (1) according to any one of the claims 3-8, wherein the transmit signal (2) is calibrated for predetermined phase shifts (19) by:

    (i) calculating the error signal (20) by subtracting from the phase error code (11) the predetermined phase shift (19) scaled by a first estimate of the phase error detection gain defined by the controllable oscillator output amplitude, the DAM gain and the ADC gain,
    (ii) calculating a further estimate of the phase error detection gain from the correlation between the predetermined phase shift (19) and the error signal (20), and

    iteratively repeating the steps (i) to (ii) using the further estimate of the phase error detection gain until saturation.

11. The method according to claim 10, wherein the predetermined phase shift is one of a known quantization error (19) of a component of the polar transmitter (1) and a phase shift especially induced by a phase modulating component of the polar transmitter (1) for the purpose of calibrating the transmit signal (2).

12. The method according to claim 10 or 11, preferably using a polar transmitter according to claim 5, wherein the transmit signal (2) is calibrated for DAM nonlinearity by:

    (iii) retrieving a DAM nonlinearity correction value (22) by addressing a DAM nonlinearity LUT (21) with the amplitude modulation signal (17), the DAM nonlinearity LUT (21) storing DAM nonlinearity correction values (22) derived from the amplitude modulation signal (17) and the product of the predetermined phase shift (19) and the error signal (20),
    (iv) correcting the amplitude modulation signal (17) by subtracting the retrieved DAM nonlinearity correction value (22),
    (v) updating the DAM nonlinearity LUT (21) by means of the product of the predetermined phase shift (19) and the error signal (20), and

    iteratively repeating the steps (iii) to (v) until saturation of the DAM nonlinearity LUT (21).

13. The method according to any one of the claims 10-12, preferably using a polar transmitter according to claim 6, wherein the transmit signal (2) is further calibrated for ADC nonlinearity by:

    (vi) retrieving an ADC nonlinearity correction value (24) by addressing an ADC nonlinearity LUT (23) with the phase error code (11), the ADC nonlinearity LUT (23) storing ADC nonlinearity correction values (24) derived from the phase error code (11) and the corrected error signal (25),
    (vii) correcting the error signal (20) by subtracting the retrieved ADC nonlinearity correction value (24),

(viii) updating the ADC nonlinearity LUT (23) by means of the corrected error signal (25), and

iteratively repeating the steps (vi) to (viii) until saturation of the ADC nonlinearity LUT (23).

14. The method according to any one of the claims 10-13, preferably using a polar transmitter according to claim 7, wherein the transmit signal (2) is further calibrated for AM-to-PM distortion by:

(ix) retrieving a frequency modulation correction value (27) by addressing an AM-to-PM distortion LUT (27) with the amplitude modulation signal (17), the AM-to-PM distortion LUT (27) storing frequency modulation correction values (27) derived from the amplitude modulation signal (17) and the error signal (20),
(x) correcting the frequency modulation signal (6) by subtracting the retrieved frequency modulation correction value (27),
(xi) updating the AM-to-PM distortion LUT (26) by means of the error signal (20), and

iteratively repeating the steps (ix) to (xi) until saturation of the AM-to-PM distortion LUT (26).

15. The method according to any one of the claims 10-14, preferably using a polar transmitter according to claim 9, wherein the transmit signal (2) is further calibrated for PM-to-AM distortion by:

(xii) retrieving an amplitude modulation correction value (29) by addressing a PM-to-AM distortion LUT (28) with the frequency modulation signal (6), the PM-to-AM distortion LUT (28) storing amplitude modulation correction values (29) derived from the frequency modulation signal (6) and the product of the predetermined phase shift (19) and the error signal (20),
(xiii) correcting the amplitude modulation signal (17) by subtracting the retrieved amplitude modulation correction value (29),
(xiv) updating the PM-to-AM distortion LUT (28) by means of the product of the predetermined phase shift (19) and the error signal (20), and

iteratively repeating the steps (xii) to (xiv) until saturation of the PM-to-AM distortion LUT (28).

Patentansprüche

1. Ein Polarsender (1), der zum Senden eines phasen-/frequenzmodulierten und amplitudenmodulierten Sendesignals (2) vorgesehen ist, wobei der Polarsender folgendes aufweist:

einen Phasenregelkreis (4), PLL, zur Erzeugung einer phasen-/frequenzmodulierten Vorstufe (3) des Sendesignals (2) über einen steuerbaren Oszillator (5), wobei der PLL an seinem Eingang eine Phasenfehlererfassungseinheit (8) zur Erfassung eines Phasenfehlers eines Rückkopplungssignals (15) aufweist, das von dem Ausgang des PLL (4) an die Phasenfehlererfassungseinheit (8) rückgekoppelt wird, und
einen digitalen Amplitudenmodulator (16), DAM, der in dem PLL (4) zur Amplitudenmodulation der Vorstufe (3) mithilfe eines Amplitudenmodulationssignals (17) angeordnet ist, bevor es durch den PLL (4) ausgegeben wird, was zu dem Sendesignal (2) führt, wobei das Rückkopplungssignal (15) das Sendesignal (2) ist oder von diesem abgeleitet wird,

dadurch gekennzeichnet, dass die Phasenfehlererfassungseinheit (8) weiterhin zur Unterabtastung mit einer Referenzgeschwindigkeit des Rückkopplungssignals (15) vorgesehen ist, wodurch sowohl Phasenfehlerinformationen als auch Amplitudeninformationen aus dem Rückkopplungssignal (15) gewonnen werden, dass die Phasenfehlererfassungseinheit (8) einen Analog-Digital-Wandler (10), ADC, zur Erzeugung eines Phasenfehlercodes (11) proportional zu dem Phasenfehler- und dem Amplitudenunterabgetasteten Rückkopplungssignal, aufweist und dass der PLL (4) zur Neuskalierung des Phasenfehlercodes (11) mithilfe des Amplitudenmodulationssignals (17) angeordnet ist.

2. Der Polarsender (1) nach Anspruch 1, wobei der PLL (4) ein Unterabtast-PLL (4) ist, mit:

dem steuerbaren Oszillator (5) zur Erzeugung der Vorstufe (3) und zur Frequenzmodulation der Vorstufe (3) mithilfe eines Frequenzmodulationssignals (6);
dem digitalen Amplitudenmodulator (16);

der Phasenfehlererfassungseinheit (8),
wobei der Phasenfehlercode (11) zum Einstellen der Phase der durch den steuerbaren Oszillator (5) erzeugten Vorstufe (3) verwendet wird, wobei die Phasenfehlererfassungseinheit (8) einen Digital-Zeit-Wandler (12), DTC, zum Verzögern der Unterabtastung des Rückkopplungssignals (15) aufweist, um Phasenmodulation der Vorstufe (3) und/oder fraktionierte Restkompensation zu ermöglichen.

3. Der Polarsender (1) nach Anspruch 2, mit einem Kalibrierkreis (181) zur Kalibrierung des Sendesignals (2) auf der Basis von vorgegebenen Phasenverschiebungen (19), wobei der Kalibrierkreis (181) zur Berechnung einer durch die steuerbare Oszillatorausgangsamplitude definierten Phasenfehlererfassungsverstärkung, einer Verstärkung des DAM (16) und einer Verstärkung des ADC (10) vorgesehen ist, wobei die Phasenfehlererfassungsverstärkung aus der Korrelation zwischen einer vorgegebenen Phasenverschiebung (19) und einem Fehlersignal (20) iterativ berechnet wird, das von dem Phasenfehlercode (11) durch Subtrahieren der vorgegebenen Phasenverschiebung (19) abgeleitet wird, die durch die berechnete Phasenfehlererfassungsverstärkung skaliert ist.

4. Der Polarsender (1) nach Anspruch 3, wobei die vorgegebene Phasenverschiebung (19) entweder ein bekannter Quantifizierungsfehler (19) einer Komponente des Polarsenders (1) oder eine Phasenverschiebung ist, die speziell durch eine phasenmodulierende Komponente des Polarsenders (1) zum Zwecke der Kalibrierung des Sendesignals (2) induziert wird.

5. Der Polarsender (1) nach Anspruch 3 oder 4, wobei der Kalibrierkreis (182) zur Kalibrierung des Sendesignal (2) für DAM Nichtlinearität vorgesehen ist, wobei das Amplitudenmodulationssignal (17) mit einem DAM Nichtlinearitäts-Korrekturwert (22) aus DAM Nichtlinearitäts-Korrekturwerten (22) korrigiert wird, die in einer DAM Nichtlinearitäts-Nachschlagetabelle (21), LUT, gespeichert und von dem Amplitudenmodulationssignal (17) und dem Produkt aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) abgeleitet sind, wobei die DAM Nichtlinearitäts-LUT (21) mithilfe des Produkts aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) iterativ aktualisiert wird, und wobei das Amplitudenmodulationssignal (17) zur kontinuierlichen Adressierung der DAM Nichtlinearitäts-LUT (21) verwendet wird.

6. Der Polarsender (1) nach einem der Ansprüche 3-5, wobei der Kalibrierkreis (183) zur Kalibrierung des Sendesignals (2) zur ADC Nichtlinearität vorgesehen ist, wobei das Fehlersignal (20) mit einem ADC Nichtlinearitäts-Korrekturwert (24) aus ADC Nichtlinearitäts-Korrekturwerten (24) korrigiert wird, die in einer ADC Nichtlinearitäts-LUT (23) gespeichert und von dem Phasenfehlercode (11) und dem korrigierten Fehlersignal (25) abgeleitet sind, wobei die ADC Nichtlinearitäts-LUT (23) mithilfe des korrigierten Fehlersignals (25) iterativ aktualisiert wird, und wobei der Phasenfehlercode (11) zur kontinuierlichen Adressierung der ADC Nichtlinearitäts-LUT (23) verwendet wird.

7. Der Polarsender (1) nach einem der Ansprüche 3-6, wobei der Kalibrierkreis (184) zur Kalibrierung des Sendesignals (2) zur Amplitudenmodulations- zu Phasenmodulations-Verzerrung, AM-PM Verzerrung, vorgesehen ist, wobei das Frequenzmodulationssignal (6) durch einen Frequenzmodulations-Korrekturwert (27) aus Frequenzmodulations-Korrekturwerten (27) korrigiert wird, die in einer AM-PM Verzerrungs-LUT (26) gespeichert und von dem Amplitudenmodulationssignal (17) und dem Fehlersignal (20) abgeleitet sind, wobei die AM-PM Verzerrungs-LUT (26) mithilfe des Fehlersignals (20) iterativ aktualisiert wird, und wobei das Amplitudenmodulationssignal (17) zur kontinuierlichen Adressierung der AM-PM Verzerrungs-LUT (26) verwendet wird.

8. Der Polarsender (1) nach einem der Ansprüche 3-7, wobei der Kalibrierkreis (185) zur Kalibrierung des Sendesignals (2) zur Phasenmodulations- zu Amplitudenmodulations-Verzerrung, PM-AM-Verzerrung, vorgesehen ist, wobei das Amplitudenmodulationssignal (17) durch einen Amplitudenmodulations-Korrekturwert (29) aus Amplitudenmodulations-Korrekturwerten (29) korrigiert wird, die in einer PM-AM Verzerrungs-LUT (28) gespeichert und von dem Frequenzmodulationssignal (6) und dem Produkt aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) abgeleitet sind, wobei die PM-AM Verzerrungs-LUT (28) mithilfe des Produkts aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) iterativ aktualisiert wird, und wobei das Frequenzmodulationssignal (6) zur kontinuierlichen Adressierung der PM-AM Verzerrungs-LUT (28) verwendet wird.

9. Ein Verfahren zur Erzeugung eines phasen-/frequenzmodulierten und amplitudenmodulierten Sendesignals (2) mithilfe eines Polarsenders (1), wobei eine phasen-/frequenzmodulierte Vorstufe (3) des Sendesignals (2) mithilfe eines steuerbaren Oszillators in einem Phasenregelkreis (4), PLL, des Polarsenders (1) erzeugt wird, wobei eine Phasenfehlererfassungseinheit (8) des PLL (4) zur Erfassung eines Phasenfehlers eines Rückkopplungssignals (15) verwendet wird, das von dem Ausgang des PLL (4) an die Phasenfehlererfassungseinheit (8) rückgekoppelt wird, wobei Amplitudenmodulation der Vorstufe (3) mithilfe eines Amplitudenmodulationssignals (17) durch einen

digitalen Amplitudenmodulator (16), DAM, in dem PLL (4) des Polarsenders (1) erfolgt, woraus das Sendesignal (2) resultiert, wobei das Rückkopplungssignal (15) das Sendesignal (2) ist oder von diesem abgeleitet ist, **dadurch gekennzeichnet, dass** die Phasenfehlererfassungseinheit (8) weiterhin zur Unterabtastung mit einer Referenzgeschwindigkeit des Rückkopplungssignals (15) verwendet wird, um sowohl Phasenfehlerinformationen als auch Amplitudeninformationen aus dem Rückkopplungssignal (15) zu gewinnen, dass ein Analog-Digital-Wandler, ADC, in der Phasenfehlererfassungseinheit (8) zur Erzeugung eines Phasenfehlercodes (11) proportional zu dem unterabgetasteten Rückkopplungssignal verwendet wird, und dass das Amplitudenmodulationssignal (17) zur Neuskalierung des Phasenfehlercodes (11) verwendet wird.

10. Das Verfahren nach Anspruch 9, unter Verwendung eines Polarsenders (1) nach einem der Ansprüche 3-8, wobei das Sendesignal (2) für vorgegebene Phasenverschiebungen (19) kalibriert wird durch:

(i) Berechnen des Fehlersignals (20) durch Subtrahieren der vorgegebenen Phasenverschiebung (19), die durch eine erste Schätzung der durch die steuerbare Oszillatorausgangsamplitude definierten Phasenfehlererfassungsverstärkung, der DAM Verstärkung und der ADC Verstärkung skaliert wird, von dem Phasenfehlercode (11),
(ii) Berechnen einer weiteren Schätzung der Phasenfehlererfassungsverstärkung aus der Korrelation zwischen der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20), und

iteratives Wiederholen der Schritte (i) bis (ii) unter Verwendung der weiteren Schätzung der Phasenfehlererfassungsverstärkung bis zur Sättigung.

11. Das Verfahren nach Anspruch 10, wobei die vorgegebene Phasenverschiebung entweder ein bekannter Quantifizierungsfehler (19) einer Komponente des Polarsenders (1) oder eine Phasenverschiebung ist, die speziell durch eine Phasenmodulationskomponente des Polarsenders (1) zum Zwecke der Kalibrierung des Sendesignals (2) induziert ist.

12. Das Verfahren nach Anspruch 10 oder 11, vorzugsweise über einen Polarsender nach Anspruch 5, wobei das Sendesignal (2) zur DAM Nichtlinearität kalibriert wird durch:

(iii) Abrufen eines DAM Nichtlinearitätskorrekturwerts (22) durch Adressierung einer DAM Nichtlinearitäts-LUT (21) mit dem Amplitudenmodulationssignal (17), wobei die DAM Nichtlinearitäts-LUT (21) DAM Nichtlinearitätskorrekturwerte (22) speichert, die von dem Amplitudenmodulationssignal (17) und dem Produkt aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) abgeleitet sind,
(iv) Korrigieren des Amplitudenmodulationssignals (17) durch Subtrahieren des abgerufenen DAM Nichtlinearitätskorrekturwerts (22),
(v) Aktualisieren der DAM Nichtlinearitäts-LUT (21) mithilfe des Produkts aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20), sowie

iteratives Wiederholen der Schritte (iii) bis (v) bis zur Sättigung der DAM Nichtlinearitäts-LUT (21).

13. Das Verfahren nach einem der Ansprüche 10-12, vorzugsweise über einen Polarsender nach Anspruch 6, wobei das Sendesignal (2) weiterhin zur ADC Nichtlinearität kalibriert wird durch:

(vi) Abrufen eines ADC Nichtlinearitätskorrekturwerts (24) durch Adressierung einer ADC Nichtlinearitäts-LUT (23) mit dem Phasenfehlercode (11), wobei die ADC Nichtlinearitäts-LUT (23) ADC Nichtlinearitätskorrekturwerte (24) speichert, die von dem Phasenfehlercode (11) und dem korrigierten Fehlersignal (25) abgeleitet sind,
(vii) Korrigieren des Fehlersignals (20) durch Subtrahieren des abgerufenen ADC Nichtlinearitätskorrekturwerts (24),
(viii) Aktualisieren der ADC Nichtlinearitäts-LUT (23) mithilfe des korrigierten Fehlersignals (25), sowie

iteratives Wiederholen der Schritte (vi) bis (viii) bis zur Sättigung der ADC Nichtlinearitäts-LUT (23).

14. Das Verfahren nach einem der Ansprüche 10-13, vorzugsweise über einen Polarsender nach Anspruch 7, wobei das Sendesignal (2) weiterhin zur AM-PM Verzerrung kalibriert wird durch:

(ix) Abrufen eines Frequenzmodulations-Korrekturwerts (27) durch Adressierung einer AM-PM Verzerrungs-LUT (27) mit dem Amplitudenmodulationssignal (17), wobei die AM-PM Verzerrungs-LUT (27) Frequenzmo-

dulations-Korrekturwerte (27) speichert, die von dem Amplitudenmodulationssignal (17) und dem Fehlersignal (20) abgeleitet sind,
(x) Korrigieren des Frequenzmodulationssignals (6) durch Subtrahieren des abgerufenen Frequenzmodulations-Korrekturwerts (27),
(xi) Aktualisieren der AM-PM Verzerrungs-LUT (26) mithilfe des Fehlersignals (20), sowie

iteratives Wiederholen der Schritte (ix) bis (xi) bis zur Sättigung der AM-PM Verzerrungs-LUT (26).

15. Das Verfahren nach einem der Ansprüche 10-14, vorzugsweise über einen Polarsender nach Anspruch 9, wobei das Sendesignal (2) weiterhin zur PM-AM Verzerrung kalibriert wird durch:

(xii) Abrufen eines Amplitudenmodulations-Korrekturwerts (29) durch Adressierung einer PM-AM Verzerrungs-LUT (28) mit dem Frequenzmodulationssignal (6), wobei die PM-AM Verzerrungs-LUT (28) Amplitudenmodulations-Korrekturwerte (29) speichert, die von dem Frequenzmodulationssignal (6) und dem Produkt aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20) abgeleitet sind,
(xiii) Korrigieren des Amplitudenmodulationssignals (17) durch Subtrahieren des abgerufenen Amplitudenmodulations-Korrektursignals (29),
(xiv) Aktualisieren der PM-AM Verzerrungs-LUT (28) mithilfe des Produkts aus der vorgegebenen Phasenverschiebung (19) und dem Fehlersignal (20), sowie

iteratives Wiederholen der Schritte (xii) bis (xiv) bis zur Sättigung der PM-AM Verzerrungs-LUT (28).

Revendications

1. Un émetteur polaire (1) destiné à transmettre un signal d'émission (2) modulé en phase/fréquence et modulé en amplitude, l'émetteur polaire comportant :

une boucle à phase asservie (4), PLL, pour générer un précurseur modulé en phase/fréquence (3) du signal d'émission (2) en utilisant un oscillateur pouvant être commandé (5), la PLL comportant à son entrée une unité de détection d'erreur de phase (8) pour détecter une erreur de phase d'un signal de rétroaction (15) qui est réinjecté à partir de la sortie de la PLL (4) dans l'unité de détection d'erreur de phase (8), et
un modulateur d'amplitude numérique (16), DAM, agencé à l'intérieur de la PLL (4) pour une modulation d'amplitude du précurseur (3) au moyen d'un signal de modulation d'amplitude (17) avant d'être délivré en sortie par la PLL (4), ayant pour résultat le signal d'émission (2), le signal de rétroaction (15) étant le signal d'émission (2) ou étant dérivé de celui-ci,
caractérisé en ce que l'unité de détection d'erreur de phase (8) est en outre destiné à un sous-échantillonnage à une cadence de référence du signal de rétroaction (15), en obtenant ainsi à la fois des informations d'erreur de phase et des informations d'amplitude à partir du signal de rétroaction (15), **en ce que** l'unité de détection d'erreur de phase (8) comporte un convertisseur analogique-numérique (10), ADC, pour générer un code d'erreur de phase (11) proportionnel à l'erreur de phase et au signal de rétroaction sous-échantillonné en amplitude, et **en ce que** la PLL (4) est conçue pour remettre à l'échelle le code d'erreur de phase (11) au moyen du signal de modulation d'amplitude (17).

2. L' émetteur polaire (1) selon la revendication 1, dans lequel la PLL (4) est une PLL de sous-échantillonnage (4) comportant :

l'oscillateur pouvant être commandé (5) pour générer le précurseur (3) et pour une modulation de fréquence du précurseur (3) au moyen d'un signal de modulation de fréquence (6) ;
le modulateur d'amplitude numérique (16) ;
l'unité de détection d'erreur de phase (8) ;
dans lequel le code d'erreur de phase (11) est utilisé pour ajuster la phase du précurseur (3) générée par l'oscillateur pouvant être commandé (5), l'unité de détection d'erreur de phase (8) comportant un convertisseur de données numériques en temps (12), DTC, pour retarder le sous-échantillonnage du signal de rétroaction (15) pour permettre une modulation de phase du précurseur (3) et/ou une compensation de résidu fractionnaire.

3. L' émetteur polaire (1) selon la revendication 2, comportant une boucle d'étalonnage (181) pour un étalonnage du signal d'émission (2) basé sur des déphasages prédéterminés (19), dans lequel la boucle d'étalonnage (181) est

destiné à calculer un gain de détection d'erreur de phase défini par l'amplitude de sortie de l'oscillateur pouvant être commandé, un gain dudit DAM (16) et un gain dudit ADC (10), dans lequel le gain de détection d'erreur de phase est calculé de manière itérative à partir de la corrélation entre un déphasage prédéterminé (19) et un signal d'erreur (20) dérivé du code d'erreur de phase (11) en soustrayant le déphasage prédéterminé (19) mis à l'échelle par le gain de détection d'erreur de phase calculé.

4. L' émetteur polaire (1) selon la revendication 3, dans lequel le déphasage prédéterminé (19) est un élément parmi une erreur de quantification connue (19) d'un composant de l'émetteur polaire (1) et un déphasage spécialement induit par un composant de modulation de phase de l'émetteur polaire (1) dans le but d'étalonner le signal d'émission (2).

5. L' émetteur polaire (1) selon la revendication 3 ou 4, dans lequel la boucle d'étalonnage (182) est destinée à un étalonnage du signal d'émission (2) pour une non-linéarité de DAM, dans lequel le signal de modulation d'amplitude (17) est corrigé avec une valeur de correction de non-linéarité de DAM (22) pour des valeurs de correction de non-linéarité de DAM (22) stockées dans une table de consultation de non-linéarité de DAM (21), LUT, et dérivées du signal de modulation d'amplitude (17) et du produit du déphasage prédéterminé (19) et du signal d'erreur (20), dans lequel la LUT de non-linéarité de DAM (21) est mise à jour de manière itérative au moyen du produit du déphasage prédéterminé (19) et du signal d'erreur (20), et dans lequel le signal de modulation d'amplitude (17) est utilisé pour l'adressage continu de la LUT de non-linéarité de DAM (21).

6. L' émetteur polaire (1) selon l'une quelconque des revendications 3 à 5, dans lequel la boucle d'étalonnage (183) est destinée à un étalonnage du signal d'émission (2) pour la non-linéarité d'ADC, dans lequel le signal d'erreur (20) est corrigé avec une valeur de correction de non-linéarité d'ADC (24) à partir de valeurs de correction de non-linéarité d'ADC (24) stockées dans une LUT de non-linéarité d'ADC (23) et dérivées du code d'erreur de phase (11) et du signal d'erreur corrigé (25), dans lequel la LUT de non-linéarité d'ADC (23) est mise à jour de manière itérative au moyen du signal d'erreur corrigé (25), et dans lequel le code d'erreur de phase (11) est utilisé pour l'adressage continu de la LUT de non-linéarité d'ADC (23).

7. L' émetteur polaire (1) selon l'une quelconque des revendications 3 à 6, dans lequel la boucle d'étalonnage (184) est destinée à un étalonnage du signal d'émission (2) pour la distorsion de la modulation d'amplitude en modulation de phase, distorsion d'AM en PM, dans lequel le signal de modulation de fréquence (6) est corrigé par une valeur de correction de modulation de fréquence (27) à partir de valeurs de correction de modulation de fréquence (27) stockées dans une LUT de distorsion d'AM en PM (26) et dérivées du signal de modulation d'amplitude (17) et du signal d'erreur (20), dans lequel la LUT de distorsion d'AM en PM (26) est mise à jour de manière itérative au moyen du signal d'erreur (20), et dans lequel le signal de modulation d'amplitude (17) est utilisé pour l'adressage continu de la LUT de distorsion d'AM en PM (26).

8. L' émetteur polaire (1) selon l'une quelconque des revendications 3 à 7, dans lequel la boucle d'étalonnage (185) est destinée à un étalonnage du signal d'émission (2) pour la distorsion de modulation de phase en modulation d'amplitude, distorsion de PM en AM, dans lequel le signal de modulation d'amplitude (6) est corrigé par une valeur de correction de modulation d'amplitude (29) à partir de valeurs de correction de modulation d'amplitude (29) stockées dans une LUT de distorsion de PM en AM (28) et dérivées du signal de modulation de fréquence (6) et du produit du déphasage prédéterminé (19) et du signal d'erreur (20), dans lequel la LUT de distorsion de PM en AM (28) est mise à jour de manière itérative au moyen du produit du déphasage prédéterminé (19) et du signal d'erreur (20), et dans lequel le signal de modulation de fréquence (6) est utilisé pour l'adressage continu de la LUT de distorsion de PM en AM (28) .

9. Un procédé pour générer un signal d'émission (2) modulé en phase/fréquence et modulé en amplitude au moyen d'un émetteur polaire (1), dans lequel un précurseur modulé en phase/fréquence (3) du signal d'émission (2) est généré au moyen d'un oscillateur pouvant être commandé dans une boucle à phase asservie (4), PLL, de l'émetteur polaire (1), dans lequel une unité de détection d'erreur de phase (8) de la PLL (4) est utilisée pour détecter une erreur de phase d'un signal de rétroaction (15) qui est réinjecté à partir de la sortie de la PLL (4) dans l'unité de détection d'erreur de phase (8), dans lequel une modulation d'amplitude du précurseur (3) est réalisée au moyen d'un signal de modulation d'amplitude (17) par un modulateur d'amplitude numérique (16), DAM, à l'intérieur de la PLL (4) de l'émetteur polaire (2), le résultat étant le signal d'émission (2), le signal de rétroaction (15) étant le signal d'émission (2) ou dérivé de celui-ci, **caractérisé en ce que** l'unité de détection d'erreur de phase (8) est en outre utilisée pour un sous-échantillonnage à au moins une cadence de référence du signal de rétroaction (15) afin d'obtenir à la fois des informations d'erreur de phase et des informations d'amplitude à partir du signal de rétroaction

(15), **en ce qu'**un convertisseur analogique-numérique, ADC, à l'intérieur de l'unité de détection d'erreur de phase (8) est utilisé pour générer un code d'erreur de phase (11) proportionnel au signal de rétroaction sous-échantillonné, et **en ce que** le signal de modulation d'amplitude (17) est utilisé pour remettre à l'échelle le code d'erreur de phase (11).

10. Le procédé selon la revendication 9, utilisant un émetteur polaire (1) selon l'une quelconque des revendications 3 à 8, dans lequel le signal d'émission (2) est étalonné pour des déphasages prédéterminés (19) par les étapes consistant à :

(i) calculer le signal d'erreur (20) en soustrayant du code d'erreur de phase (11) le déphasage prédéterminé (19) mis à l'échelle par une première estimation du gain de détection d'erreur de phase défini par l'amplitude de sortie de l'oscillateur pouvant être commandé, le gain du DAM et le gain de l'ADC,
(ii) calculer une estimation supplémentaire du gain de détection d'erreur de phase à partir de la corrélation entre le déphasage prédéterminé (19) et le signal d'erreur (20), et

répéter de manière itérative les étapes (i) à (ii) en utilisant l'estimation supplémentaire du gain de détection d'erreur de phase jusqu'à saturation.

11. Le procédé selon la revendication 10, dans lequel le déphasage prédéterminé est un élément parmi une erreur de quantification connue (19) d'un composant de l'émetteur polaire (1) et un déphasage spécialement induit par un composant de modulation de phase de l'émetteur polaire (1) dans le but d'étalonner le signal d'émission (2).

12. Le procédé selon la revendication 10 ou 11, utilisant de préférence un émetteur polaire selon la revendication 5, dans lequel le signal d'émission (2) est étalonné pour la non-linéarité de DAM par les étapes consistant à :

(iii) récupérer une valeur de correction de non-linéarité de DAM (22) en adressant une LUT de non-linéarité de DAM (21) avec le signal de modulation d'amplitude (17), la LUT de non-linéarité de DAM (21) stockant des valeurs de correction de non-linéarité de DAM (22) dérivées du signal de modulation d'amplitude (17) et du produit du déphasage prédéterminé (19) et du signal d'erreur (20),
(iv) corriger le signal de modulation d'amplitude (17) en soustrayant la valeur de correction de non-linéarité de DAM récupérée (22),
(v) mettre à jour la LUT de non-linéarité de DAM (21) au moyen du produit du déphasage prédéterminé (19) et du signal d'erreur (20), et

répéter de manière itérative les étapes (iii) à (v) jusqu'à saturation de la LUT de non-linéarité de DAM (21).

13. Le procédé selon l'une quelconque des revendications 10 à 12, utilisant de préférence un émetteur polaire selon la revendication 6, dans lequel le signal d'émission (2) est en outre étalonné pour une non-linéarité d'ADC par les étapes consistant à :

(vi) récupérer une valeur de correction de non-linéarité d'ADC (24) en adressant une LUT de non-linéarité d'ADC (23) avec le code d'erreur de phase (11), la LUT de non-linéarité d'ADC (23) stockant des valeurs de correction de non-linéarité d'ADC (24) dérivées du code d'erreur de phase (11) et du signal d'erreur corrigé (25),
(vii) corriger le signal d'erreur (20) en soustrayant la valeur de correction de non-linéarité d'ADC récupérée (24),
(viii) mettre à jour la LUT de non-linéarité d'ADC (23) au moyen du signal d'erreur corrigé (25), et

répéter de manière itérative les étapes (vi) à (viii) jusqu'à saturation de la LUT de non-linéarité d'ADC (23).

14. Le procédé selon l'une quelconque des revendications 10 à 13, utilisant de préférence un émetteur polaire selon la revendication 7, dans lequel le signal d'émission (2) est en outre étalonné pour la distorsion d'AM en PM par les étapes consistant à :

(ix) récupérer une valeur de correction de modulation de fréquence (27) en adressant une LUT de distorsion d'AM en PM (27) avec le signal de modulation d'amplitude (17), la LUT de distorsion d'AM en PM (27) stockant des valeurs de correction de modulation de fréquence (27) dérivées du signal de modulation d'amplitude (17) et du signal d'erreur (20),
(x) corriger le signal de modulation de fréquence (6) en soustrayant la valeur de correction de modulation de fréquence récupérée (27),

(xi) mettre à jour la LUT de distorsion d'AM en PM (26) au moyen du signal d'erreur (20), et

répéter de manière itérative les étapes (ix) à (xi) jusqu'à saturation de la LUT de distorsion d'AM en PM (26).

15. Le procédé selon l'une quelconque des revendications 10 à 14, utilisant de préférence un émetteur polaire selon la revendication 9, dans lequel le signal d'émission (2) est en outre étalonné pour la distorsion de PM en AM par les étapes consistant à :

(xii) récupérer une valeur de correction de modulation d'amplitude (29) en adressant une LUT de distorsion de PM en AM (28) avec le signal de modulation de fréquence (6), la LUT de distorsion de PM en AM (28) stockant des valeurs de correction de modulation d'amplitude (29) dérivées du signal de modulation de fréquence (6) et du produit du déphasage prédéterminé (19) et du signal d'erreur (20),
(xiii) corriger le signal de modulation d'amplitude (17) en soustrayant la valeur de correction de modulation d'amplitude récupérée (29),
(xiv) mettre à jour la LUT de distorsion de PM en AM (28) au moyen du produit du déphasage prédéterminé (19) et du signal d'erreur (20), et

répéter de manière itérative les étapes (xii) à (xiv) jusqu'à saturation de la LUT de distorsion de PM en AM (28) .

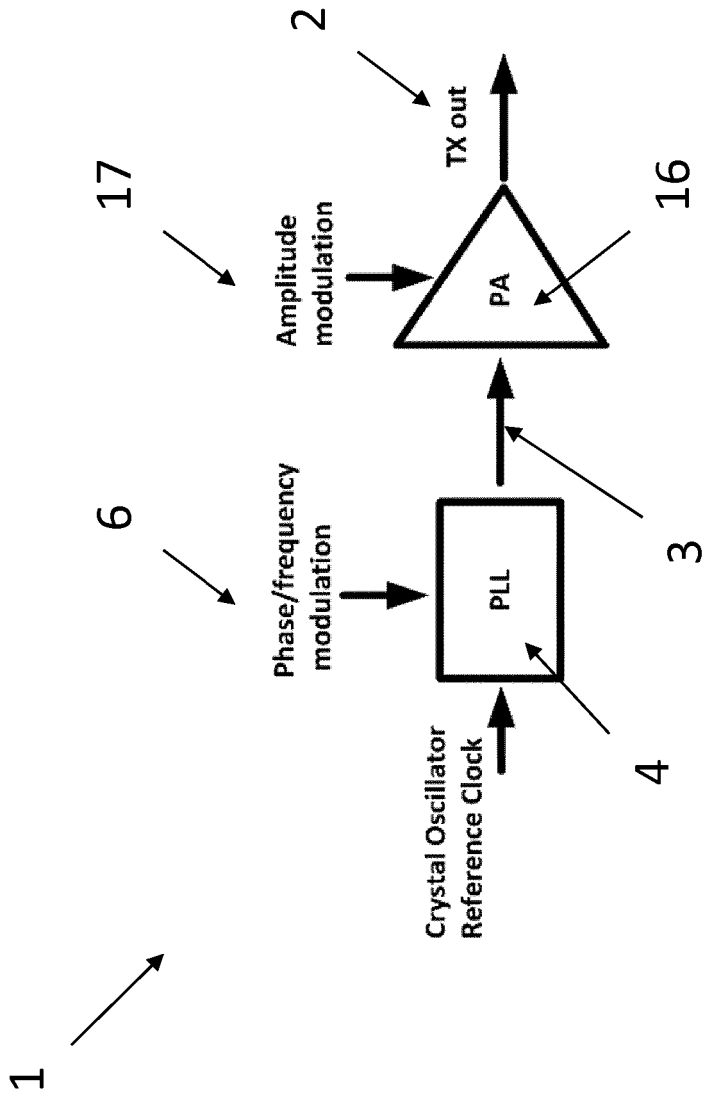
1
2
TX out
17
Amplitude modulation
16
PA
6
Phase/frequency modulation
PLL
3
4
Crystal Oscillator Reference Clock

FIG. 1

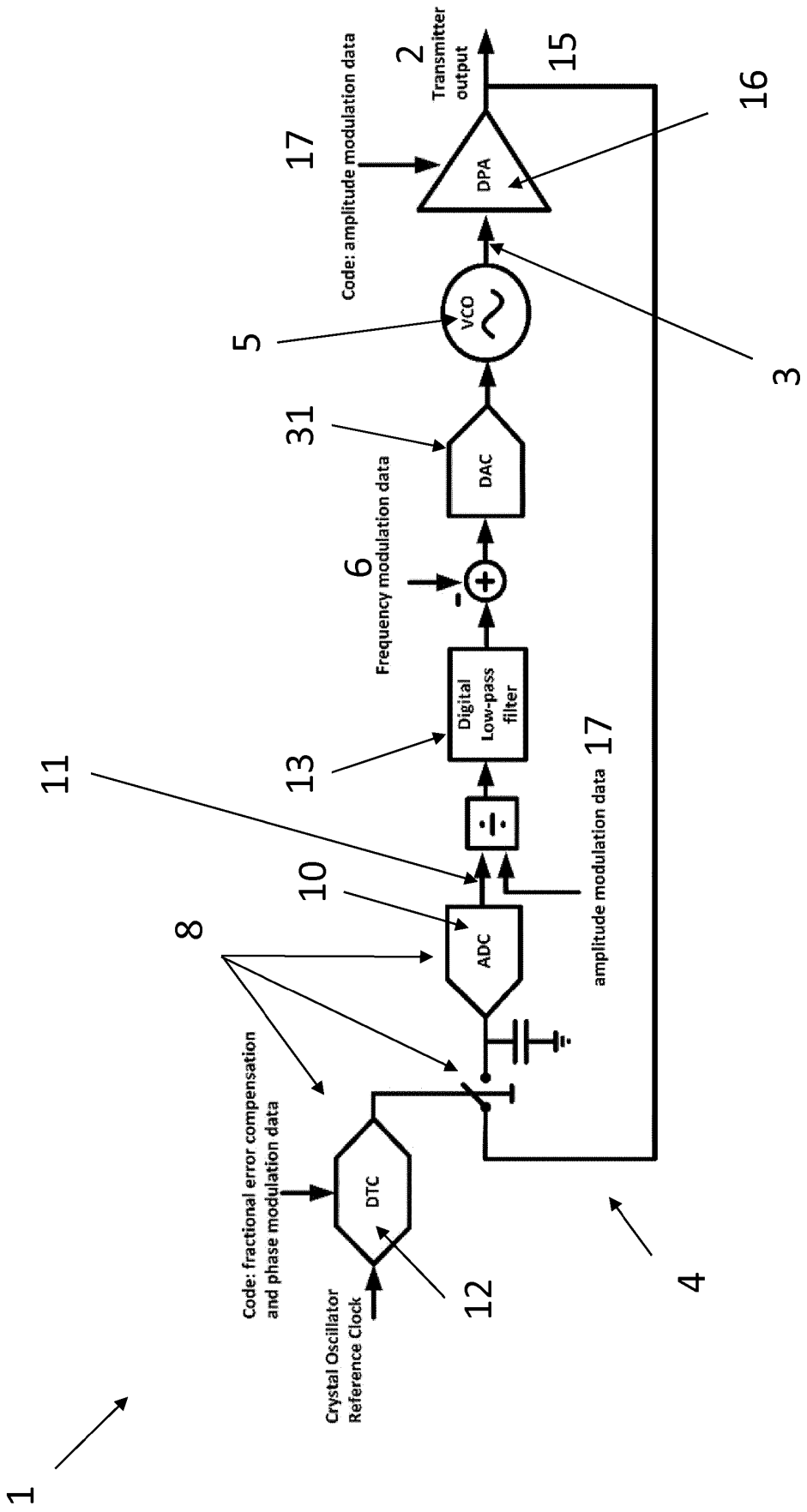
1
2
Transmitter output
3
4
5
6
Frequency modulation data
8
10
11
12
13
15
16
17
Code: amplitude modulation data
amplitude modulation data
Code: fractional error compensation and phase modulation data
Crystal Oscillator Reference Clock
DTC
ADC
Digital Low-pass filter
DAC
VCO
DPA
31

FIG. 2

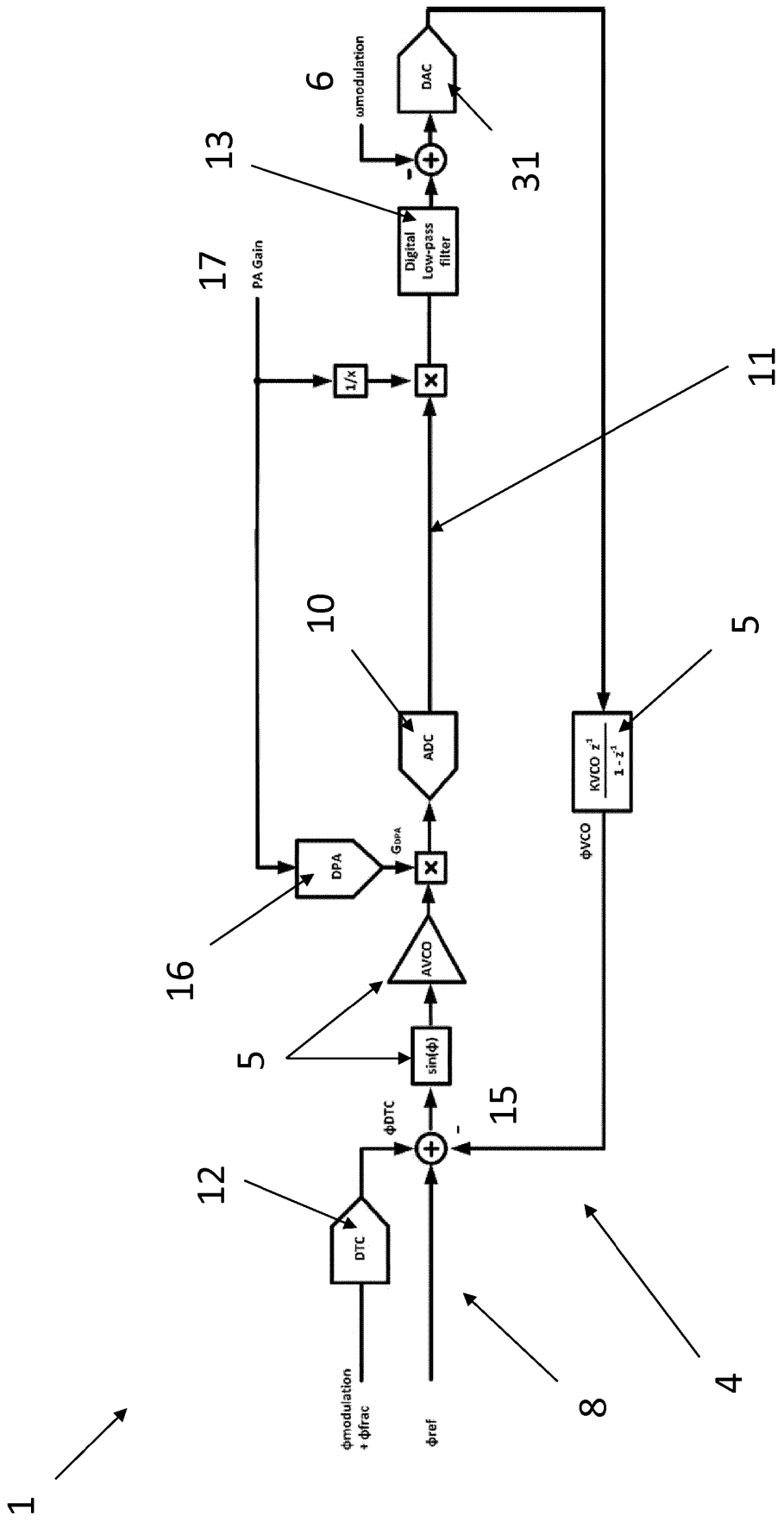
1
ϕmodulation + ϕfrac
ϕref
DTC
12
ϕDTC
sin(ϕ)
AVCO
5
DPA
16
GDPA
ADC
10
1/x
PA Gain
17
Digital Low-pass filter
13
ωmodulation
6
DAC
31
KVCO z-1 / 1 - z-1
ϕVCO
5
11
15
8
4

FIG. 3

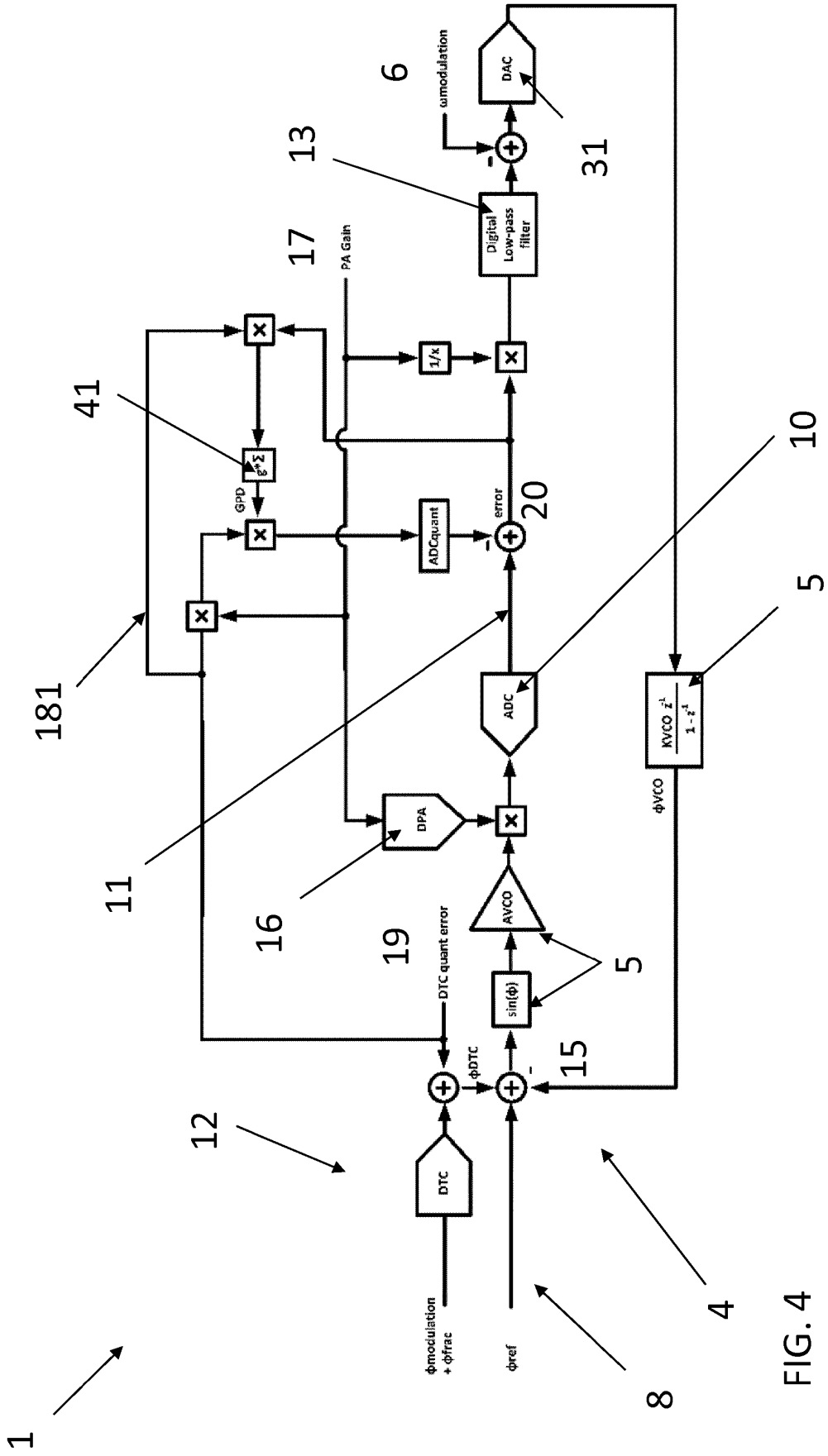
1
181
41
11
16
19
12
13
17
6
31
10
5
20
15
4
8
DAC
ωmodulation
Digital Low-pass filter
PA Gain
1/x
ADCquant
error
GPD
ADC
DPA
AVCO
sin(Φ)
DTC quant error
ΦDTC
DTC
Φmodulation + Φfrac
Φref
ΦVCO
KVCO z⁻¹ / 1 - z⁻¹

FIG. 4

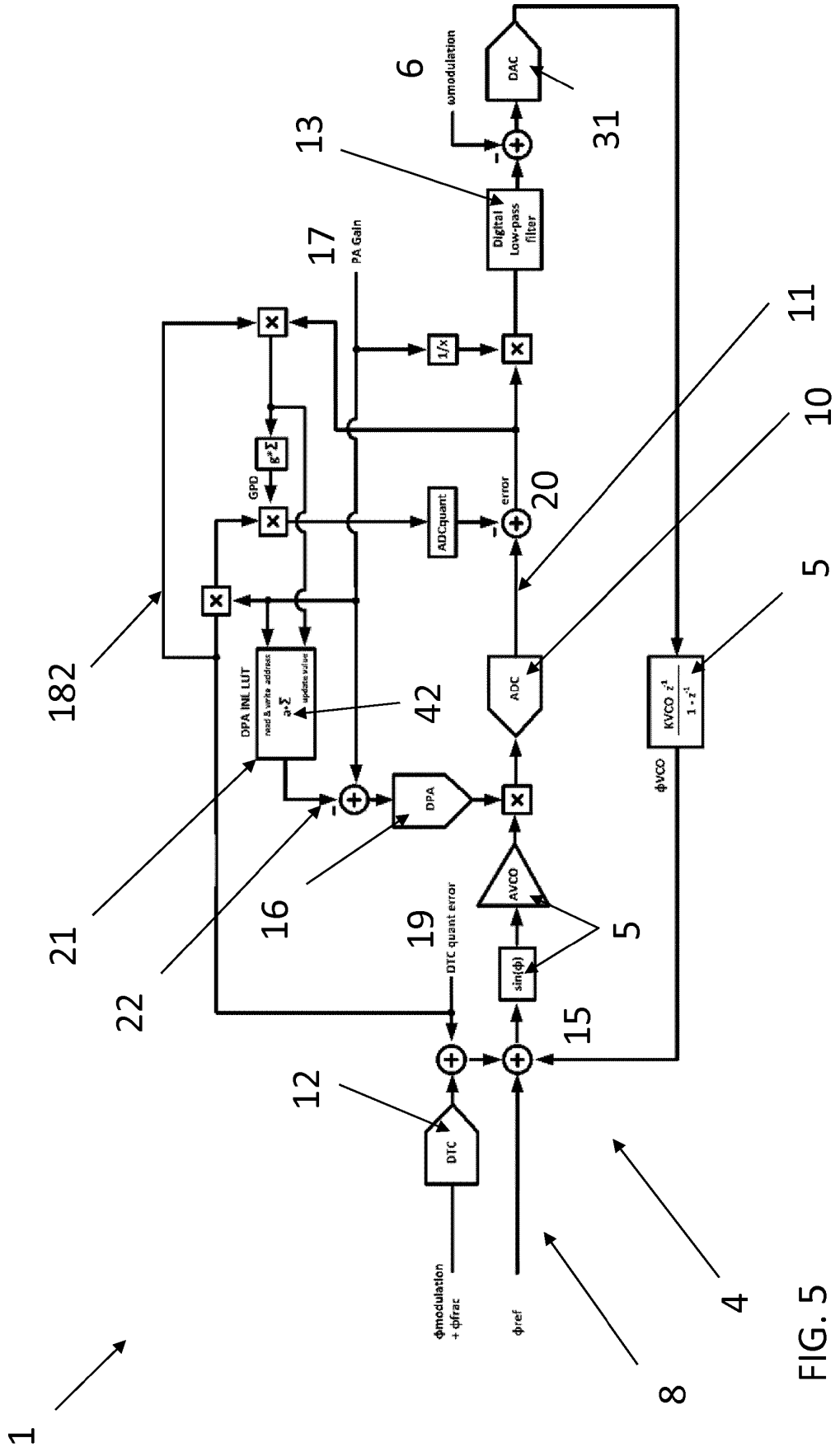
1
182
21
22
16
19
DTC quant error
12
DTC
ϕmodulation + ϕfrac
ϕref
8
15
sin(ϕ)
AVCO
5
4
ϕVCO
KVCO z⁻¹ / 1 - z⁻¹
ADC
5
42
DPA INL LUT
read & write address
update value
DPA
GPD
g*Σ
ADCquant
error
20
1/x
PA Gain
17
13
Digital Low-pass filter
ωmodulation
6
DAC
31
11
10

FIG. 5

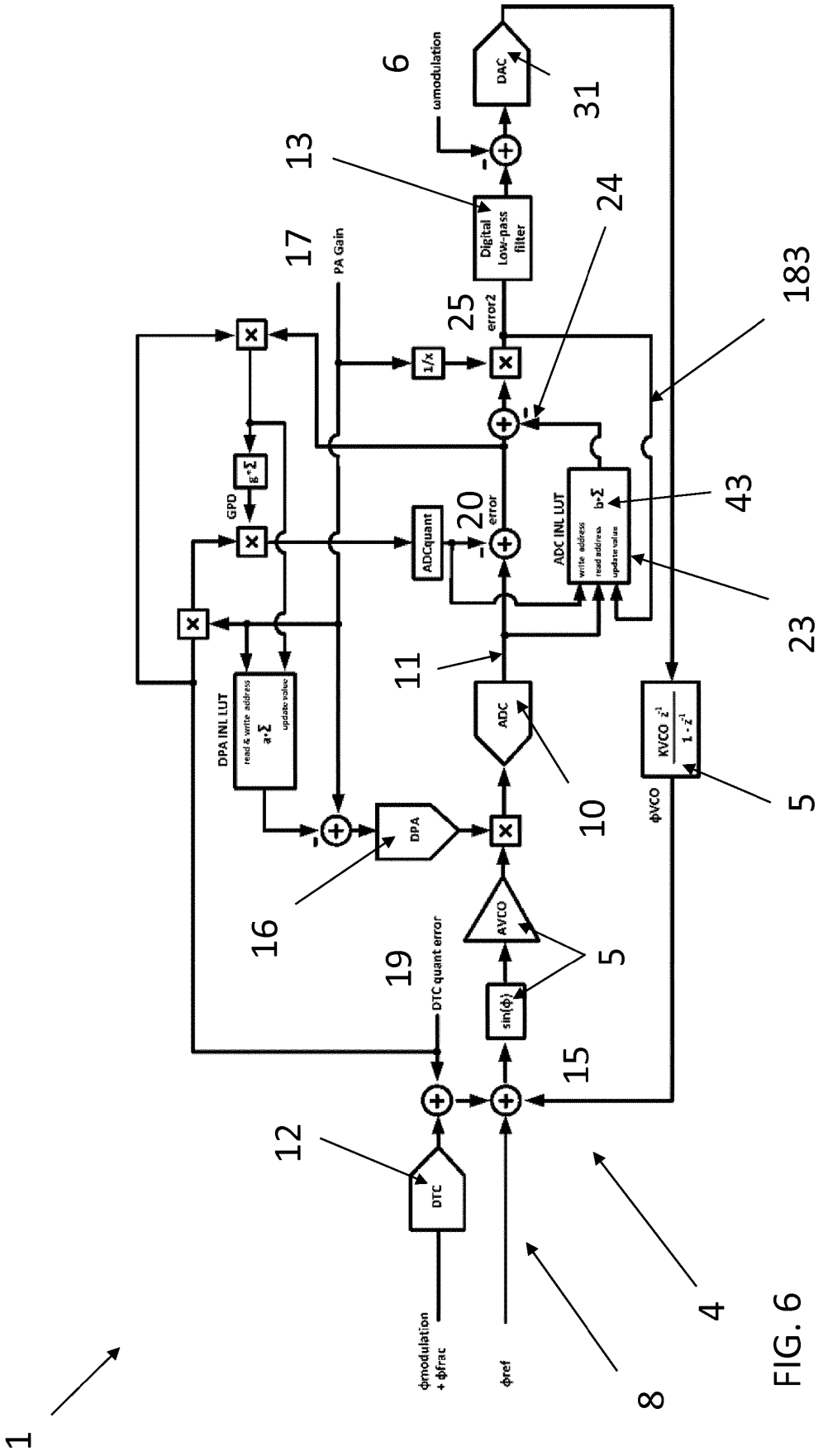
1
ϕmodulation + ϕfrac
ϕref
8
4
12
DTC
15
19
DTC quant error
16
DPA
DPA INL LUT
read & write address
update value
GPD
17
PA Gain
1/x
ADCquant
20
error
ADC INL LUT
write address
read address
update value
43
11
ADC
10
AVCO
sin(ϕ)
5
ϕVCO
KVCO
5
23
25
error2
Digital Low-pass filter
24
13
6
ωmodulation
DAC
31
183

FIG. 6

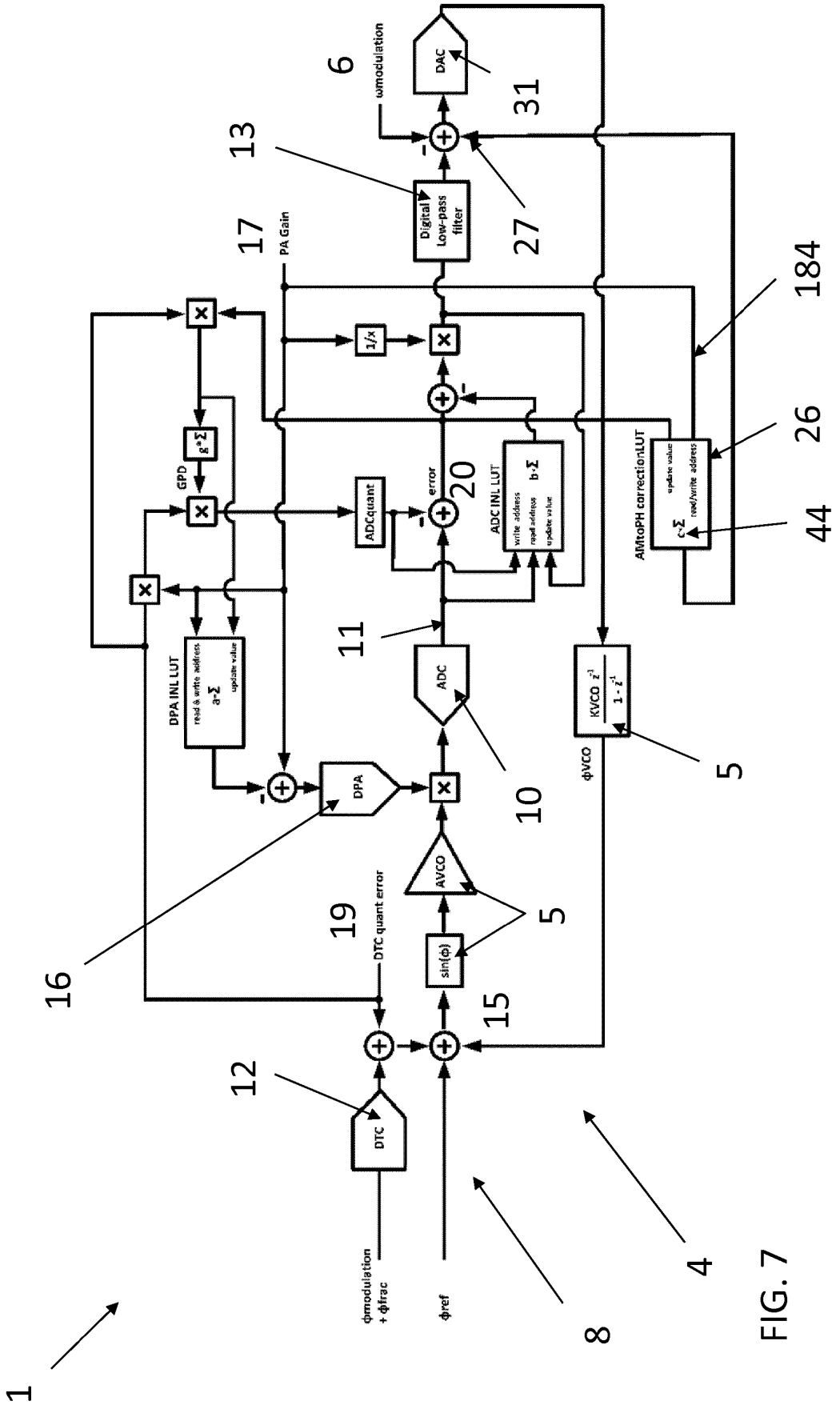
1
6
ωmodulation
DAC
31
13
Digital Low-pass filter
27
17
PA Gain
184
1/x
GPD
g*Σ
ADCquant
error
20
ADC INL LUT
write address
read address
update value
b+Σ
AMtoPH correction LUT
update value
c+Σ
read/write address
26
44
DPA INL LUT
read & write address
a+Σ
update value
11
ADC
KVCO z^-1 / 1 - z^-1
ϕVCO
5
16
DPA
10
AVCO
sin(ϕ)
5
19
DTC quant error
15
12
DTC
ϕmodulation + ϕfrac
ϕref
8
4

FIG. 7

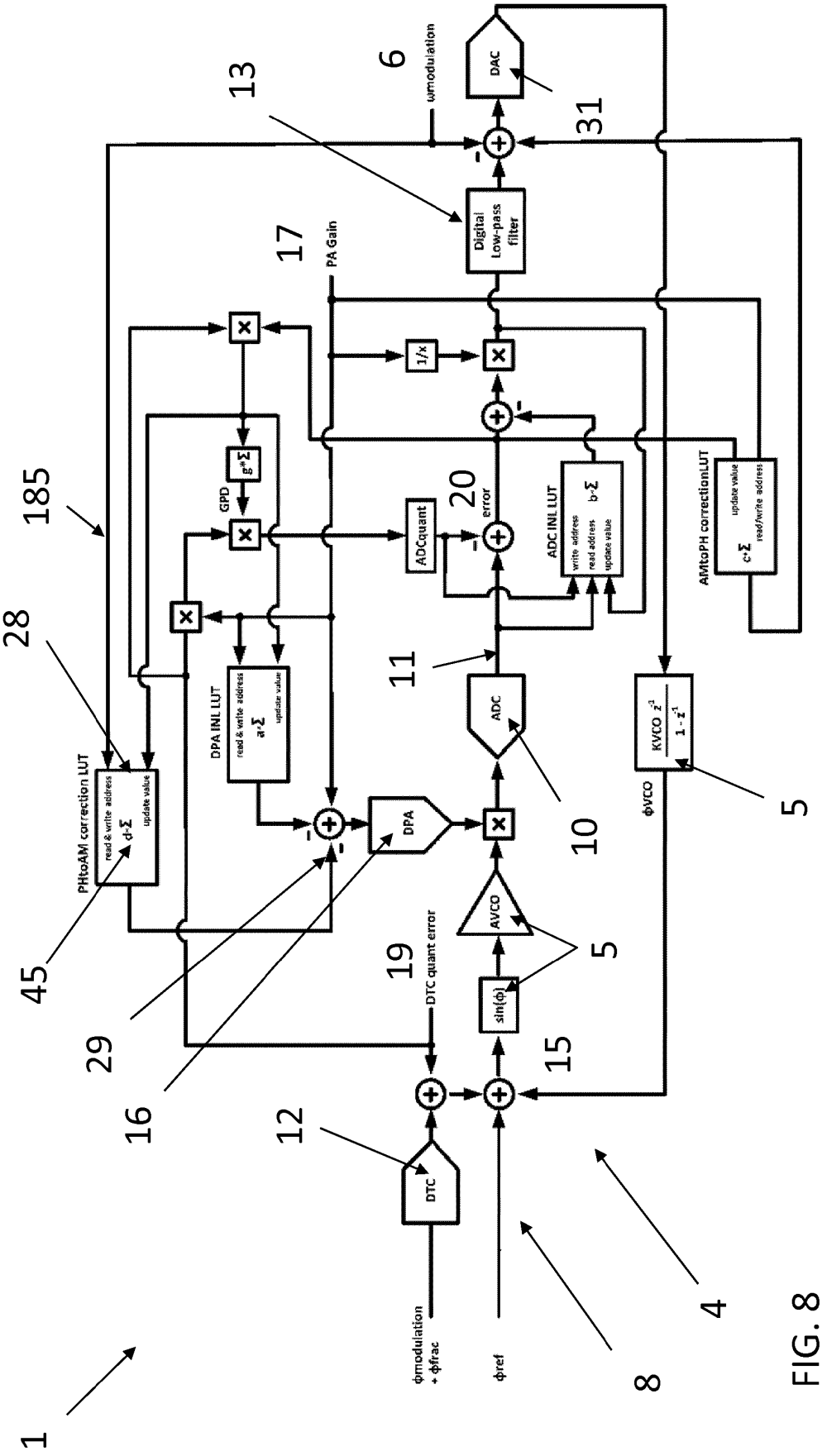
1
13
6
ωmodulation
DAC
31
Digital Low-pass filter
17
PA Gain
185
28
GPD
ADCquant
20
error
ADC INL LUT
write address
read address
update value
AMtoPH correctionLUT
update value
read/write address
11
DPA INL LUT
read & write address
update value
ADC
PHtoAM correction LUT
read & write address
update value
DPA
10
KVCO
ϕVCO
5
45
29
16
AVCO
19
DTC quant error
sin(ϕ)
15
12
DTC
ϕmodulation + ϕfrac
ϕref
8
4

FIG. 8

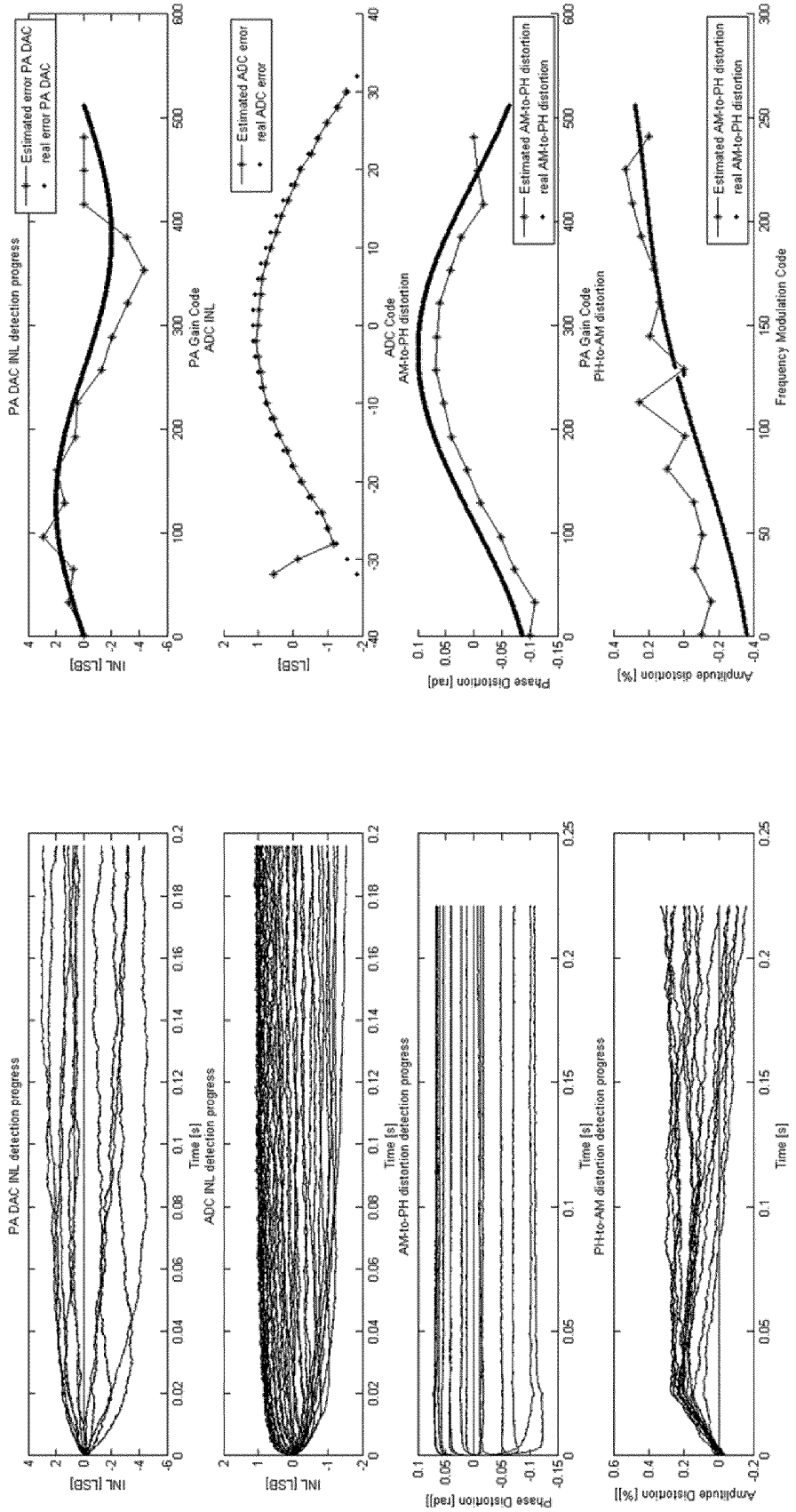
PA DAC INL detection progress
INL [LSB]
Time [s]
ADC INL detection progress
INL [LSB]
Time [s]
AM-to-PH distortion detection progress
Phase Distortion [rad]
Time [s]
PH-to-AM distortion detection progress
Amplitude Distortion [%]
Time [s]
PA DAC INL detection progress
Estimated error PA DAC
real error PA DAC
INL [LSB]
PA Gain Code
ADC INL
Estimated ADC error
real ADC error
[LSB]
ADC Code
AM-to-PH distortion
Estimated AM-to-PH distortion
real AM-to-PH distortion
Phase Distortion [rad]
PA Gain Code
PH-to-AM distortion
Estimated AM-to-PH distortion
real AM-to-PH distortion
Amplitude distortion [%]
Frequency Modulation Code

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 0124356 A **[0004]**

Non-patent literature cited in the description

- **K. RACZKOWSKI ; N. MARKULIC ; B. HERSHBERG ; J. VAN DRIESSCHE ; J. CRANINCKX.** A 9.2-12.7 GHz Wideband Fractional-N Subsampling PLL in 28 nm CMOS with 280 fs RMS jitter. *Radio Frequency Integrated Circuits Symposium,* 2014 **[0083]**
- **N. MARKULIC ; K. RACZKOWSKI ; P. WAMBACQ ; J. CRANINCKX.** A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS. *European Solid State Circuits Conference (ESSCIRC), Venice,* 2014 **[0083]**
- **X. GAO ; E. KLUMPERINK ; M. BOHSALI ; B. NAUTA.** A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N2. *IEEE Journal of Solid-State Circuits,* 2003, vol. 44 (12), 3253-3263 **[0083]**
- **G. MARZIN ; S. LEVANTINO ; C. SAMORI ; A. L. LACAITA.** A 20 Mb/s phase modulator based on a 3.6 GHz digital PLL with- 36 dB EVM at 5 mW power. *IEEE Journal of Solid-State Circuits,* 2012, vol. 47 (12), 2974-2988 **[0083]**
- **S. LEVANTINO ; G. MARZIN ; C. SAMORI.** An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs. *IEEE Journal of Solid-State Circuits,* 2014, vol. 49 (8), 1762-1772 **[0083]**