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A setting flow for delay time of an initiating device and a controlling flow for an electronic detonator in an electronic detonator initiating system

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(54) **Title**: SETTING FLOW FOR DELAY TIME OF A BLASTING DEVICE AND CONTROLLING FLOW FOR AN ELECTRONIC DETONATOR IN AN ELECTRONIC DETONATOR BLASTING SYSTEM

(54) **发明名称** : 电子雷管起爆系统中的起爆装置延期时间设定流程和电子雷管控制流程

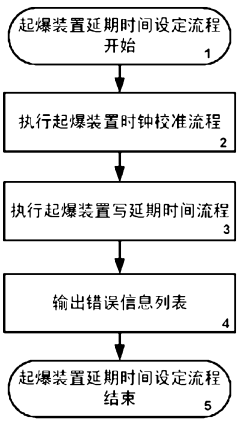

图 5 /Fig.5

1 .. STARTING A SETTING FLOW FOR DELAY TIME OF A BLASTING DEVICE
2 .. EXECUTING A CLOCK CALIBRATING PROCEDURE OF THE BLASTING DEVICE
3 .. EXECUTING A DELAY TIME WRITING PROCEDURE OF THE BLASTING DEVICE
4 .. OUTPUTTING AN ERROR INFORMATION LIST
5 .. ENDING THE SETTING FLOW FOR DELAY TIME OF THE BLASTING DEVICE

(57) **Abstract**: A setting flow for delay time of a blasting device in an electronic detonator blasting system performs steps as follows: Step A1, executing a clock calibrating procedure (2) of the blasting device; Step A2, executing a delay time writing procedure (3) of the blasting device; Step A3, outputting an error information list to a human-computer interaction module which displays the error information list (4); Step A4, ending the setting flow for delay time of the blasting device (5). The system is comprised of the blasting device and one or more electronic detonators. One or more electronic detonators is connected to a signal bus derived from the blasting device in parallel. The blasting device includes a control module, a human-computer interaction module, a power supply management module, a signal modulating and transmitting module, a signal modulating and receiving module and a power suppy. The control module includes a CPU and a timer. An alternate design of the setting flow for delay time of the blasting device is executing a clock calibrating procedure during a delay time writing procedure. A controlling flow for an electronic detonators in an electronic detonator blasting system performs a clock calibrating procedure and a delay time writing procedure respectively according to an outer command.

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(57) 摘要:

一种电子雷管起爆系统中的起爆装置延期时间设定流程按照以下步骤进行：步骤 A1，执行起爆装置时钟校准流程（2）；步骤 A2，执行起爆装置写延期时间流程（3）；步骤 A3，向所述人机交互模块输出错误信息列表（4），由所述人机交互模块显示；步骤 A4，结束本起爆装置延期时间设定流程（5）。该系统由起爆装置与一个或多个电子雷管构成，一个或多个电子雷管并联连接在由所述起爆装置引出的信号总线上，起爆装置包括控制模块、人机交互模块、电源管理模块、信号调制发送模块、信号调制接收模块和电源，控制模块包含中央处理器和定时器。该起爆装置延期时间设定流程的另一方案是在写延期时间流程的过程中执行时钟校准流程。一种电子雷管起爆系统中的电子雷管控制流程根据外部命令分别执行时钟校准流程和写延期时间流程。

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DESCRIPTIONS

A Setting Flow for Delay Time of an Initiating Device and a Controlling Flow for an Electronic Detonator in an Electronic Detonator Initiating System

Technical Field

The present invention relates to the field of the initiation controlling technology of initiating explosive materials, in particular to the design of a delay-time-setting method in the electronic detonator initiating system, including an initiating device delay-time-setting flow, an electronic detonator controlling flow, and the cooperation between them.

Background of the Invention

Since 1980's, research on electronic detonator technologies has been commenced in Japan, Australia, Europe and some other developed countries or districts. Great progress in the electronic detonator technology has been made with rapid development of electronic technology, micro-electronics technology, and information technology. Application experiment and market promotion of the electronic detonator have been carried out since the late 1990s.

As the core component of the electronic detonator, the performance of the electronic detonator control chip directly affects the performance of the electronic detonator. The electronic detonator control chip disclosed in Chinese Patent ZL200820111269.7, ZL200820111270.X and ZL03156912.9 has realized the basic functions of two-wire non-polarity connection, bidirectional communication between the electronic detonator and its initiating device, identity code built-in, controllability of detonation process, electronic delay and so on, which has already achieved essential advancement comparing with traditional detonators.

The embodiments of the electronic detonator disclosed in Chinese Patent ZL200420034635.5, ZL98210324.7, ZL200420034635.5 and ZL200620094002.2 use the crystal oscillator outside the electronic delay module as the reference clock. The main defects of such technical solution lie in: in the practical blasting application of the electronic detonators, the delay time of each detonator may be different, so the exploded detonators will bring blasting shocks to the unexploded detonators; since the crystal generates clocks according to its frequency output steadily from its mechanical resonance, if the crystal oscillator is chosen to be the reference clock, the blasting shock wave will affect the resonance frequency of the crystal, thereby affecting the delay precision of the electronic detonator. In some worse situation, the crystal may be destroyed by the blasting shock wave, thus the clock circuit may stop working, resulting in misfire of the detonator. In addition, the crystal in the crystal oscillator can not be integrated into the electronic detonator control chip, which will increase the size and the cost of the electronic detonator.

Because of the aforementioned defects of the crystal oscillator, it becomes necessary to use a clock circuit with anti-shock performance in the application situation with shock wave. In addition, an integratable clock circuit will be necessary in order to decrease the size of the electronic detonator as much as possible.

So the RC oscillator can be used as the clock circuit to supply reference clock for the detonator chip. On the one hand, the integratability of the electronic

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detonator control components can be improved by using the RC oscillator; on the other hand, the adaptability for the shock wave situation of the entire electronic detonator can be improved with the anti-shock performance of the RC oscillator.

However, the factors such as temperature excursion, clock excursion, and parameter changes of the RC oscillator may easily cause some problems such as frequency excursion or frequency difference, thus affecting the delay accuracy of the electronic detonator initiating system.

Throughout this specification the word "comprise", or variations such as "comprises", "comprised" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present disclosure as it existed before the priority date of each claim of this application.

Summary of the Invention

The present invention is further improved based on the prior art, and is used to supply a chip controlling flow and an initiating device controlling flow which can accomplish the function of calibrating the clock and setting the delay time. With the cooperation of the two aforementioned flows, the effect on the delay precision resulting from the problems of the RC oscillator such as frequency excursion and frequency difference can be avoided, realizing an electronic detonator initiating network with both better anti-shock performance and higher delay time precision which meets the application requirements.

There is provided an initiating device delay-time-setting flow in an electronic detonator initiating system which is comprised of an initiating device and at least one electronic detonator, at least one said electronic detonator is connected in parallel between the signal bus extending from the initiating device, the initiating device includes a control module, a man-machine interacting module, a power supply management module, a signal modulating and transmitting module, a signal demodulating and receiving module and a power supply, and the control module further includes a first CPU and a timer, wherein:

the initiating device delay-time-setting flow is carried out in accordance with the following steps:

Step A1, executing an initiating device clock-calibrating flow;

Step A2, executing an initiating device delay-time-writing flow;

Step A3, outputting an error information list to the man-machine interacting module for displaying; and

Step A4, ending the present initiating device delay-time-setting flow;

wherein

Step A1 is carried out in accordance with the following steps:

Step B1, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and the cycle number W1 into the cache of the control module; wherein the value of the variable E1 is equal to the value of the number N;

Step B2, the control module judging whether the value of the cycle number

W1 and the variable E1 is 0: if the value of the cycle number W1 or the value of the variable E1 is 0, ending the present initiating device clock-calibrating flow; if not, continuing with Step B3;

Step B3, executing an initiating device clock-calibrating process; and

Step B4, subtracting 1 from the value of the cycle number W1, and rendering the result to be a new value of the cycle number W1, that is, W1=W1-1; then returning to Step B2.

The electronic detonator may include an electronic detonator control chip, and the chip includes a non-volatile memory, a logic control circuit and a clock circuit; wherein the aforementioned logic control circuit further includes a programmable delay module, an input/output interface, a serial communication interface, a prescaler, a counter, and a second CPU. And the clock circuit mentioned above maybe an RC oscillator.

In the first technical solution of the initiating device delay-time-setting flow, before the initiating device delay-time-writing flow, the initiating device executes the initiating device clock-calibrating flow to calibrate the clock frequency of the electronic detonator, which ensures the delay time precision of every electronic detonator in the initiating network. In Step A3, the delay-setting error information list is sent to the man-machine interacting module for displaying, so that, according to the delay-setting error information and the importance degree of the blasting hole where the electronic detonator is, the operators of the initiating device can judge whether to re-execute the initiating device delay-time-setting flow to ensure that all the electronic detonators have been set the delay time, or to proceed with the following operation to the electronic detonators in the initiating network which have been set the delay time completely. Such solution has improved the control flexibility of the blasting operation.

In the initiating device delay-time-setting flow mentioned above, the initiating device clock-calibrating flow in Step A1 can be carried out in accordance with the following steps:

Step B1, initializing the present initiating device clock-calibrating flow, that is, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and the cycle number W_1 into the cache of the control module; wherein the value of the variable E_1 is equal to the value of the number N;

Step B2, the control module judging whether the value of the cycle number W_1 and the variable E_1 is 0: if the value of the cycle number W_1 or the value of the variable E_1 is 0, ending the present initiating device clock-calibrating flow; if not, continuing with Step B3;

Step B3, executing an initiating device clock-calibrating process;

Step B4, subtracting 1 from the value of the cycle number W_1, and rendering the result to be a new value of the cycle number W_1, that is, $W_1=W_1-1$; then returning to Step B2.

In the initiating device delay-time-setting flow mentioned above, the initiating device delay-time-writing flow in Step A2 can be carried out in accordance with the following steps:

Step E1, initializing the present initiating device delay-time-writing flow, that is, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating

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network, the variable E_2 which represents the number of the electronic detonators which contain errors in the process of delay-time-writing, and the cycle number W_2 into the cache of the control module; wherein the value of the variable E_2 is equal to the value of the number N;

Step E2, the control module judging whether the value of the cycle number W_2 and the value of the variable E_2 is 0: if the value of the cycle number W_2 or the value of the variable E_2 is 0, executing Step E5; if not, continuing with Step E3;

Step E3, executing an initiating device delay-time-writing process;

Step E4, subtracting 1 from the value of the cycle number W_2, and rendering the result to be a new value of the cycle number W_2, that is, $W_2=W_2-1$; then returning to Step E2;

Step E5, ending the present initiating device delay-time-writing flow.

In the initiating device clock-calibrating flow and the initiating device delay-time-writing flow mentioned above, the variables of the cycle number W_1 and the cycle number W_2 are designed to respectively control the running times of the initiating device clock-calibrating process and the initiating device

delay-time-writing process; the mode that one time's execution of the initiating device delay-time-setting flow once can automatically cause several times' circular execution of the clock-calibrating process and the delay-time-writing process has simplified the operation steps, thereby decreasing the misoperation resulting from people's complex and repetitious operations and improving the operating reliability of the device. Every time after the initiating device delay-time-setting flow is executed completely, an error information list will be output to prompt the choice for the next operation, and the possibility of clock-calibrating error or delay-time-writing error resulting from the instantaneous fault of the network does exist in the initiating system, therefore the solution in which the initiating device automatically executes the clock-calibrating process for W_1 times as predetermined and executes the delay-time-writing process for W_2 times as predetermined can simplify the operation of the operator and improve the operating reliability of the initiating device. When the initiating device has accomplished the clock-calibrating process for W_1 times as predetermined or there is no electronic detonator with any clock-calibrating error in the system, the initiating device clock-calibrating flow will end; and when the initiating device has accomplished the delay-time-writing process for W_2 times as predetermined or there is no electronic detonator with any delay-time-writing error in the system, the initiating device delay-time-writing flow will end.

In the initiating device clock-calibrating flow mentioned above, the first embodiment of the initiating device clock-calibrating process in Step B3 can be carried out in accordance with the following steps:

Step C1, the control module transmitting a first clock-calibrating instruction to all the electronic detonators in the initiating network;

Step C2, the control module waiting for a time T_0 which represents a predetermined delay: if reaching the time, executing Step C3; if not, continuing waiting;

Step C3, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, that is, $L=E_1$;

Step C4, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step C5, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step C6, judging whether the present electronic detonator is in the calibrated state according to the state information of the detonator: if the judgement is positive, executing Step C13; if not, executing Step C7;

Step C7, transmitting a state-reading-back instruction to the present electronic detonator;

Step C8, the control module executing a signal receiving process: if receiving the information returned by the present electronic detonator, executing Step C9; if not, executing Step C12;

Step C9, the control module storing the information returned by the present electronic detonator, and judging whether the clock-calibrating indication digit of the electronic detonator is in the calibrated state: if the judgement is positive, executing Step C10; if not, executing Step C12;

Step C10, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device and is corresponding to the

present electronic detonator;

Step C11, subtracting 1 from the value of the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$; then continuing with Step C13;

Step C12, setting the clock-calibrating error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator; and then executing Step C13;

Step C13, subtracting 1 from the value of the variable L which represents the number of electronic detonators that are to be calibrated, and rendering the result to be a new value of the variable L, that is, L=L-1;

Step C14, judging whether the value of the variable L which represents the number of electronic detonators that are to be calibrated is 0: if the judgement is positive, continuing with Step C15; if not, returning to Step C4;

Step C15, ending the present initiating device clock-calibrating process.

In the first embodiment of the initiating device clock-calibrating process mentioned above, the first clock-calibrating instruction which is sent to all the electronic detonators in the initiating network in Step C1 is a global instruction. The first clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and a down stream calibrating waveform; and the down stream calibrating waveform consists of a string of down stream calibrating impulses, the period of which is a predetermined period T_B and the sum of which is a predetermined number n_B. The initiating device sends the synchronous studying heads and the down stream calibrating waveform with the steady and accurate clock source of itself to the chip, so that the counter in the chip can count the down stream calibrating waveform in sections, thereby figuring out the clock frequency of the chip itself.

Specially, the down stream calibrating waveform mentioned above is sent by the control module executing the initiating device calibrating-waveform-transmitting flow described as follows:

Step D1, setting the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted to be the same as the value of the variable n_B which represents the predetermined number of the down stream calibrating impulses, that is, $n=n_B$;

Step D2, writing the value of the variable v_B which represents the predetermined low level breadth of the down stream calibrating impulse into the timer;

Step D3, transmitting a control signal to the signal modulating and transmitting module to render it output a down edge signal;

Step D4, transmitting a control signal to the timer to start it;

Step D5, the first CPU monitoring whether the length of the low level signal output by the signal modulating and transmitting module has reached the predetermined low level breadth v_B: if the judgement is positive, executing Step D6; if not, continuing monitoring;

Step D6, transmitting a control signal to the timer to stop it;

Step D7, writing the value of the variable u_B which represents the predetermined high level breadth of the down stream calibrating impulse into the timer;

Step D8, transmitting a control signal to the signal modulating and

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transmitting module to render it output an up edge signal;

Step D9, transmitting a control signal to the timer to start it;

Step D10, the first CPU monitoring whether the length of the high level signal output by the signal modulating and transmitting module has reached the predetermined high level breadth u_B: if the judgement is positive, executing Step D11; if not, continuing monitoring;

Step D11, transmitting a control signal to the timer to stop it;

Step D12, subtracting 1 from the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted, and rendering the result to be a new value of the variable n, that is, n=n-1;

Step D13, judging whether the value of the variable n is 0: if the judgement is positive, executing Step D14; if not, returning to Step D2;

Step D14, ending the present initiating device calibrating-waveform-transmitting flow.

In the initiating device calibrating-waveform-transmitting flow, the value of the variable u_B which represents the predetermined high level breadth of the down stream calibrating impulse is higher than the value of the variable v_B which represents the predetermined low level breadth of the down stream calibrating impulse, and the sum of the value of the variable u_B and the value of the variable v_B equals the value of the predetermined period T_B. The advantages lie in: when sending the high level calibrating impulse to the electronic detonator, the initiating device is in the state of supplying positive voltage to the detonator; while sending the low level calibrating impulse to the electronic detonator, the initiating device is in the state of supplying no power or supplying negative voltage to the detonator. So increasing the high level breadth of the calibrating impulse can extend the time of sending the high level signal, thereby the time during which the initiating device supplies power to the detonator can be extended and the energy consumed from the storage unit in the electronic detonator can be decreased, which is beneficial to improve the operating reliability of the control chip in the electronic detonator, to decrease the current noises of the bus in the initiating network, and to improve the stability of the initiating network.

In the first embodiment of the initiating device clock-calibrating process mentioned above, the state-reading-back instruction in Step C7 which is sent to a certain electronic detonator is a single instruction for the present detonator. The state-reading-back instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the state-reading-back command word, and the identity code of the present electronic detonator. By sending the present instruction to the electronic detonator, the initiating device can obtain the state information of the electronic detonator, thus the initiating device can control the operation of the detonator more reliably.

Corresponding to the first embodiment of the initiating device clock-calibrating process, in the initiating device delay-time-setting flow mentioned above, Step E3, the initiating device delay-time-writing process in the initiating device delay-time-writing flow can be carried out in accordance with the following steps:

Step F1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step F2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step F3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step F4, judging whether the present electronic detonator is in the calibrated state according to the state information of the detonator: if the judgement is negative, executing Step F9; if the judgement is positive, executing Step F5;

Step F5, reading the value D_0 of the delay time data stored in the initiating device corresponding to the present electronic detonator;

Step F6, transmitting a delay-time-writing instruction including the value D_0 of the delay time data to the present electronic detonator;

Step F7, the control module executing a signal receiving process: if receiving the delay-time-writing-completed signal returned by the present electronic detonator, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, and then executing Step F8; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, and then executing Step F9;

Step F8, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

Step F9, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, R=R-1;

Step F10, judging whether the value of the variable R is 0: if the judgement is positive, executing Step F11; if not, returning to Step F2;

Step F11, ending the present initiating device delay-time-writing process.

In the initiating device delay-time-writing process mentioned above, the delay-time-writing instruction in Step F6 sent to a certain electronic detonator in the initiating network is a single instruction for the present electronic detonator. The delay-time-writing instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the delay-time-writing command word, the identity code of the present electronic detonator and the delay time data D_0 of the present corresponding electronic detonator. The initiating device can write in the delay time data for every electronic detonator in the network one by one by executing the initiating device delay-time-writing process, thereby accomplish designing the delay time of the detonator network.

In the initiating device delay-time-setting flow mentioned above, the second embodiment of Step B3, the initiating device clock-calibrating process in the initiating device clock-calibrating flow can be carried out in accordance with the following steps:

Step G1, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, that is, $L=E_1$;

Step G2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step G3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step G4, judging whether the present electronic detonator is in the calibrated

state according to the state information of the present detonator: if the judgement is positive, executing Step G12; if not, executing Step G5;

Step G5, transmitting a second clock-calibrating instruction to the present electronic detonator;

Step G6, the control module executing the signal receiving process: if receiving the up stream calibrating waveform returned by the present electronic detonator, executing Step G7; if not, setting the clock-calibrating error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, then executing Step G12;

Step G7, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator;

Step G8, subtracting 1 from the value of the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$;

Step G9, counting the up stream calibrating waveform consisting of a string of up stream calibrating impulses, the period of which is a predetermined period T_D and the sum of which is a predetermined number n_D; representing the counting result as a value F_B;

Step G10, calculating the clock frequency f_B of the present electronic detonator according to the value of the variable n_D, the variable T_D and the variable F_B;

Step G11, storing the clock information of the present electronic detonator and the clock information includes the value of the clock frequency f_B;

Step G12, subtracting 1 from the value of the variable L which represents the number of electronic detonators that are to be calibrated, and rendering the result to be a new value of the variable L, that is, L=L-1;

Step G13, judging whether the value of the variable L is 0: if the judgement is positive, continuing with Step G14; if not, returning to Step G2;

Step G14, ending the present initiating device clock-calibrating process.

Corresponding to the second embodiment of the initiating device clock-calibrating process mentioned above, in the initiating device delay-time-setting flow, Step E3, the initiating device delay-time-writing process in the initiating device delay-time-writing flow can be carried out in accordance with the following steps:

Step H1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step H2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step H3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step H4, judging whether the present electronic detonator is in the calibrated state according to the state information of the present detonator: if the judgement is negative, executing Step H10; if the judgement is positive, executing Step H5;

Step H5, reading the value D_0 of the delay time data stored in the initiating device corresponding to the present electronic detonator; and reading the value of the clock frequency f_B stored in the control module corresponding to the present

electronic detonator;

Step H6, executing an initiating device delay-time-data-adjusting flow to figure out a new value D_f of the delay time data according to the value of the clock frequency f_B;

Step H7, transmitting a delay-time-writing instruction including the variable D_f to the present electronic detonator;

Step H8, the control module executing the signal receiving process: if receiving the delay-time-writing-completed signal returned by the present electronic detonator, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, and then executing Step H9; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, and then executing Step H10;

Step H9, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

Step H10, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, R=R-1;

Step H11, judging whether the value of the variable R is 0: if the judgement is positive, executing Step H12; if not, returning to Step H2;

Step H12, ending the present initiating device delay-time-writing process.

In the second embodiment of the initiating device clock-calibrating process, the second clock-calibrating instruction in Step G5 which is sent to a certain electronic detonator is a single instruction for the present electronic detonator. The second clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and the identity code of the present electronic detonator. After sending the clock-calibrating instruction to the present electronic detonator, the initiating device waits to receive the up stream calibrating waveform which is returned by the electronic detonator according to the predetermined high/low level breadth of the up stream calibrating impulse and the predetermined number of the period of the up stream calibrating impulse. The electronic detonator transmits the up stream calibrating waveform in the form of changes of current consumption. After receiving the up stream calibrating waveform, the initiating device will calculate the clock frequency f_B of the present detonator, then execute the initiating device delay-time-data-adjusting flow according to the clock frequency f_B, and finally obtain the adjusted delay time data D_f which should be written into the present detonator.

In the initiating device delay-time-writing process, the form of the delay-time-writing instruction transmitted in Step H7 is the same as the form of the delay-time-writing instruction transmitted in Step F6. The difference between the two lies in that the delay time data in the delay-time-writing instruction in Step H7 is the adjusted delay time data D_f obtained from the execution of the initiating device delay-time-data-adjusting flow.

There is provided an initiating device delay-time-setting flow in an electronic detonator initiating system which includes an initiating device and at least one electronic detonator, at least one said electronic detonator is connected in parallel between the signal bus extending from the initiating device, the initiating device includes a control module, a man-machine interacting module, a power supply management module, a signal modulating and

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transmitting module, a signal demodulating and receiving module and a power supply, wherein the control module further includes a first CPU and a timer, wherein:

Step L1 (initializing the present initiating device delay-time-setting flow, that is,) storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, the variable E_2 which represents the number of the electronic detonators that contain errors in the process of delay-time-writing, and the cycle number W into the cache of the control module; wherein both the value of the variable E_1 and the value of the variable E_2 are equal to the value of the number N;

Step L2, judging whether the value of the cycle number W and the value of the variable E_2 is 0: if the value of the cycle number W or the value of the variable E_2 is 0, executing Step L5; if not, continuing with Step L3;

Step L3, the control module executing the initiating device delay-time-setting process;

Step L4, subtracting 1 from the value of the cycle number W, and rendering the result to be a new value of the cycle number W, that is, W=W-1; then returning to Step L2;

Step L5, the control module outputting an error information list to the man-machine interacting module for displaying;

Step L6, ending the present initiating device delay-time-setting flow.

In the solution mentioned above, if all the detonators in the network have been set the delay time successfully, the initiating device delay-time-setting flow will end. In addition, if the initiating device delay-time-setting process has been executed for W times as predetermined, the control module will end the execution cycle and output an error information list to show to the operators no matter whether there are still some detonators which have not been set the delay time successfully. The cycle number W is designed to control the running times of the initiating device delay-time-setting process in Step L3, and the mode that one time's execution of the initiating device delay-time-setting flow will automatically cause several times' circular execution of the initiating device delay-time-setting process can also simplify the operation steps.

In the second technical solution of the initiating device delay-time-setting flow mentioned above, wherein Step L3 can be carried out in accordance with the following steps:

Step M1, setting the value of the variable S which represents the number of the electronic detonators that are to be set the delay time to be the same as the value of the variable E_1, that is, $S=E_1$;

Step M2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step M3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step M4, judging whether the present electronic detonator is in the state that the delay time has been set according to the state information of the present detonator: if the judgement is positive, executing Step M15; if not, executing Step M5;

Step M5, transmitting a second clock-calibrating instruction to the present electronic detonator;

Step M6, the control module executing the signal receiving process: if

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receiving the up stream calibrating waveform returned by the present electronic detonator, the control module will set the clock-calibrating succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, then executing Step M7; if not, the control module will set the clock-calibrating error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, then executing Step M15;

Step M7, subtracting 1 from the value of the variable E_1, and rendering the result to be a new value of the variable E_1, that is, $E_1 = E_1 - 1$;

Step M8, the control module counting the up stream calibrating waveform consisting of a string of up stream calibrating impulses, the period of which is a predetermined period T_D and the sum of which is a predetermined number n_D, and representing the counting result as a value F_B;

Step M9, calculating the clock frequency f_B of the present electronic detonator according to the value of the variable n_D, the variable T_D and the variable F_B;

Step M10, reading the value D_0 of the delay time date stored in the initiating device corresponding to the present electronic detonator;

Step M11, executing the initiating device delay-time-data-adjusting flow, to figure out a new value D_f of the delay time data according to the value of the clock frequency f_B;

Step M12, transmitting a delay-time-writing instruction including the value D_f to the present electronic detonator;

Step M13, the control module executing the signal receiving process: if receiving the delay-time-writing-completed signal returned by the present electronic detonator, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, and then executing Step M14; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, then executing Step M15;

Step M14, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2 = E_2 - 1$;

Step M15, subtracting 1 from the value of the variable S, and rendering the result to be a new value of the variable S, that is, S= S-1;

Step M16, judging whether the value of the variable S is 0: if the judgement is positive, executing Step M17; if not, returning to Step M2;

Step M17, ending the present initiating device delay-time-setting process.

In the initiating device delay-time-setting process mentioned above, the initiating device writes the delay time for a certain electronic detonator immediately after the clock of the present detonator is calibrated. In this way, the initiating device can accomplish the delay-time-setting process for all the electronic detonators in the initiating network one by one, which can omit the storage for the detonator clock frequency f_B which is figured out, so it is beneficial to simplify the design.

In the initiating device delay-time-setting process mentioned above, the second clock-calibrating instruction in Step M5 which is sent to a certain electronic detonator is a single instruction for the present electronic detonator. The second clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and the identity code of the present

electronic detonator.

In the initiating device delay-time-setting process mentioned above, the delay-time-writing instruction in Step M12 which is sent to a certain detonator in the initiating network is a single instruction for the present detonator. The delay-time-writing instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the delay-time-writing command word, the identity code of the present electronic detonator and the delay time data of the present corresponding electronic detonator. The delay time data in the present delay-time-writing instruction is the adjusted delay time data D_f which is obtained from the initiating device delay-time-data-adjusting flow.

There is provided an electronic detonator controlling flow in an electronic detonator initiating system which includes an initiating device and at least one electronic detonator, at least one said electronic detonator is connected in parallel between the signal bus extending from the initiating device, the electronic detonator includes an electronic detonator control chip, and the chip includes a non-volatile memory, a logic control circuit and a clock circuit;

wherein the logic control circuit further includes a programmable delay module, an input/output interface, a serial communication interface, a prescaler, a counter, and a second CPU, and the clock circuit is an RC oscillator,

wherein:

the electronic detonator controlling flow is carried out in accordance with the following steps:

Step N1, the second CPU sending a control signal to the programmable delay module, rendering the programmable delay module output a signal to cut off the firing control circuit and to make it in the fire-forbidden state;

Step N2, the second CPU reading the identity code stored in the non-volatile memory corresponding to the present electronic detonator;

Step N3, the second CPU waiting to receive the synchronous studying head sent by the electronic detonator initiating device: if the synchronous studying head is received, continuing with Step N4; if not, continuing waiting;

Step N4, the second CPU executing the synchronous studying process;

Step N5, the second CPU waiting to receive the command words sent by the electronic detonator initiating device:

if the clock-calibrating command word is received, entering the clock-calibrating state, then continuing with Step N6;

if the state-reading-back command word is received, entering the state-reading-back state, then continuing with Step N7;

if the delay-time-writing command word is received, entering the delay-time-writing state, then continuing with Step N8;

if the firing command word is received, entering the firing state, then continuing with Step N9;

Step N6, executing an electronic detonator clock-calibrating process; and then returning to Step N5;

Step N7, executing an electronic detonator state-reading-back process; and then returning to Step N5;

Step N8, executing an electronic detonator delay-time-writing process; and then returning to Step N5;

Step N9, executing an electronic detonator firing process;

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Step N10, ending the present electronic detonator controlling flow.

Step N4 may further comprise adjusting the clock number of the RC oscillator which will be written into the prescaler according to the received synchronous studying head, wherein the clock number is corresponding to the predetermined communication baud rate and the predetermined sampling phase.

The controlling flow mentioned above has realized the external on-line controllability of the clock-calibrating process, the state-reading-back process, the delay-time-writing process, and the firing process of the electronic detonator, which can be described as follows:

Firstly, with the accurate clock of itself, the electronic detonator initiating device can ensure the delay accuracy of the electronic detonator initiating network by the mode of calibrating the clock under the control of the on-line instruction. Calibrating the clock of the electronic detonator control chip can avoid the problem of delay accuracy resulting from the factors such as temperature excursion, clock excursion or parameter change of the RC oscillator.

Secondly, in the state-reading-back process, the electronic detonator initiating device mentioned above realizes the functions of reading back the state information of the electronic detonator, such as the state information of the clock-calibrating and the state information of the delay-time-writing, thereby controlling the operation of the detonators more reliably.

Thirdly, in the delay-time-writing process, the electronic detonator initiating device realizes the function of setting the delay time on-line for the electronic detonator. Furthermore, according to the exact clock information of the electronic detonator which is resulting from the execution of the clock-calibrating process, the initiating device can write the adjusted delay time data into the electronic detonator, thereby improving the flexibility of use of the electronic detonator.

Fourthly, the initiating device mentioned above realizes the control of the igniting of the electronic detonator by executing the firing process, which makes the igniting process more reliable.

In the controlling flow mentioned above, the synchronous studying process in Step N4 can be carried out in accordance with the following steps:

Step O1, the second CPU monitoring whether the edge signal sent by the electronic detonator initiating device is received: if the judgement is positive, executing Step O2; if not, continuing monitoring;

Step O2, sending a control signal to the counter to start it;

Step O3, the second CPU monitoring whether the edge signal sent by the electronic detonator initiating device is received: if the judgement is positive, executing Step O4; if not, continuing monitoring;

Step O4, the second CPU reading the value of the counter at the present moment, and storing the counting result;

Step O5, the second CPU judging whether the number of the received edge signals has reached as much as twice the predetermined number m which represents the number of the synchronous studying heads, that is, judging whether the number of the received edge signals has reached the value 2m: if the judgement is positive, executing Step O6; if not, returning to Step O3;

Step O6, sending a control signal to the counter to stop it;

Step O7, the second CPU calculating the clock number of the RC oscillator which will be written into the prescaler according to the counting results stored in the cache of the second CPU, wherein the clock number is corresponding to the predetermined communication baud rate and the predetermined sampling phase;

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Step O8, writing the clock number into the prescaler;

Step O9, ending the present synchronous studying process.

The synchronous studying process eliminates the effect on the reliability of data receiving of the electronic detonator caused by the frequency dispersal of the RC oscillator which is integrated in the chip. When transmitting an instruction to the chip, the initiating device transmits the synchronous studying heads, sum of which is a predetermined number m, before transmitting the command word. At the interior of the chip, when the edge signal of the synchronous studying head is received, the counter in the chip will be started to count the number of the synchronous studying heads. Then the second CPU will calculate the clock number of the RC oscillator which should be used by the serial communication interface and is respectively corresponding to the predetermined communication baud rate and the predetermined sampling phase, thereby adjusting the data receiving time and the counting interval of the electronic detonator. Therefore, it can be ensured that the electronic detonator control chip with a RC oscillator inside can still reliably receive the control instructions sent by the electronic detonator initiating device even if the problems such as temperature excursion, clock excursion and parameter changes still exist in the RC oscillator.

In the electronic detonator controlling flow mentioned above, the first embodiment of the electronic detonator clock-calibrating process in Step N6 can be carried out in accordance with the following steps:

Step P1, the second CPU monitoring whether the edge signal sent by the electronic detonator initiating device is received: if the judgement is positive, executing Step P2; if not, continuing monitoring;

Step P2, sending a control signal to the counter to start it;

Step P3, monitoring whether another edge signal sent by the electronic detonator initiating device is received: if the judgement is positive, executing Step P4; if not, continuing monitoring;

Step P4, reading the value of the counter at the present moment, and storing the counting result into the cache of the second CPU;

Step P5, the second CPU judging whether the number of the received edge signals has reached as much as twice the predetermined number n_B which represents the number of the down stream calibrating impulses, that is, judging whether the number of the received edge signals has reached the value $2n_B$: if the judgement is positive, executing Step P6; if not, returning to Step P3;

Step P6, sending a control signal to the counter to stop it;

Step P7, the second CPU calculating the value of the clock frequency f_D of the RC oscillator according to the counting results stored in the counter, the predetermined number n_B which represents the number of the down stream calibrating impulses, and the predetermined period T_B of the down stream calibrating impulses;

Step P8, the second CPU setting the clock-calibrating indication digit at the interior of the second CPU to be in the calibrated state;

Step P9, ending the present electronic detonator clock-calibrating process.

In the electronic detonator clock-calibrating process mentioned above, the clock-calibrating instruction sent by the electronic detonator initiating device to all the electronic detonators in the initiating network is corresponding to the first clock-calibrating instruction in Step C1 said above. The instruction is a global instruction, which includes the synchronous studying heads and the clock-calibrating command word in sequence, and the down stream calibrating

waveforms consisting of a string of down stream calibrating impulses, the period of which is a predetermined period T_B and the sum of which is a predetermined number n_B as well. The electronic detonator initiating device transmits the down stream calibrating waveform mentioned above with the steady and accurate clock source of itself for the counter in the chip to count the waveform in sections. The second CPU in the chip calculates the clock frequency f_D of the RC oscillator of the chip itself according to the counting results, the predetermined number n_B and the predetermined period T_B of the down stream calibrating impulse, and then stores the calculating result in the chip. The factors such as temperature excursion, clock excursion and parameter changes of the RC oscillator may result in individual differences in the clock frequency of each electronic detonator control chip, therefore using a uniform, steady and accurate clock source of the electronic detonator initiating device to calibrate the clock of the chip is beneficial to eliminate the effect on the delay precision of the initiating network resulting from individual differences of the electronic detonators, thus the delay precision of the initiating network can be improved.

Corresponding to the first embodiment of the electronic detonator clock-calibrating process mentioned above, in the electronic detonator controlling flow, the electronic detonator state-reading-back process in Step N7 can be carried out in accordance with the following steps:

Step R1, the second CPU judging whether to read back the state information of the present detonator according to the detonator identity code included in the state-reading-back instruction: if the detonator identity code in the state-reading-back instruction is corresponding to the identity code read in Step N2, executing Step R2; if not, executing Step R3;

Step R2, the second CPU sending the state information of the present detonator to the electronic detonator initiating device;

Step R3, ending the present electronic detonator state-reading-back process.

In the electronic detonator state-reading-back process mentioned above, the state-reading-back instruction sent by the electronic detonator initiating device to a certain electronic detonator in the initiating network is a single instruction for the present electronic detonator. The instruction includes the said synchronous studying heads and the said state-reading-back command word in sequence, and the identity code corresponding to the present electronic detonator as well. The design of the aforementioned process has realized the electronic detonator initiating device's obtainment of the state information of the electronic detonator, which makes the device control the operation of the detonator more reliably.

Corresponding to the first embodiment of the electronic detonator clock-calibrating process, in the electronic detonator controlling flow mentioned above, the electronic detonator delay-time-writing process in Step N8 can be carried out in accordance with the following steps:

Step S1, the second CPU judging whether to write the delay time for the present detonator according to the detonator identity code included in the delay-time-writing instruction: if the identity code in the delay-time-writing instruction is corresponding to the identity code read in Step N2, continuing with Step S2; if not, ending the present electronic detonator delay-time-writing process;

Step S2, executing the electronic detonator delay-time-data-adjusting process according to the delay time data D_0 in the delay-time-writing instruction, and thus obtaining an adjusted delay time data D_N;

Step S3, writing the adjusted delay time data D_N into the programmable delay

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module;

Step S4, the second CPU setting the delay-time-set state to the delay time setting indication digit at the interior of the second CPU; and the second CPU transmitting the delay-time-writing-completed signal to the electronic detonator initiating device;

Step S5, ending the present electronic detonator delay-time-writing process.

In the electronic detonator delay-time-writing process mentioned above, the delay-time-writing instruction sent by the electronic detonator initiating device to a certain electronic detonator is corresponding to the instruction sent by the initiating device in Step F6. The instruction is a single instruction for the present electronic detonator, which includes the said synchronous studying heads and the said delay-time-writing command word in sequence, and the identity code corresponding to the present electronic detonator and its delay time data D_0 as well. After receiving the delay time data D_0 sent by the electronic detonator initiating device, the second CPU firstly executes the electronic detonator delay-time-data-adjusting process to figure out the new delay time data D_N according to the clock frequency f_D of the present detonator which is the calculation result of the electronic detonator clock-calibrating process; then the second CPU will write the adjusted delay time data D_N into the programmable delay module, which realizes the function of setting the delay time of the electronic detonator on line, thereby improving the flexibility of using the electronic detonator. In addition, what is written into the programmable delay module is the adjusted delay time data which is adjusted from the delay time data D_0 sent by the electronic detonator initiating device according to the clock frequency f_D figured out in the electronic detonator clock-calibrating process, which ensures the delay precision of the electronic detonator.

In the electronic detonator controlling flow mentioned above, the second embodiment of the electronic detonator clock-calibrating process in step N6 can be carried out in accordance with the following steps:

Step Q1, setting the value of the variable k which represents the number of the up stream calibrating impulses that are to be sent to be the same as the value of the variable n_D which represents the predetermined number of the up stream calibrating impulses, that is, $k=n_D$;

Step Q2, the second CPU judging whether to calibrate the clock of the present detonator according to the detonator identity code included in the second clock-calibrating instruction: if the detonator identity code in the second clock-calibrating instruction is corresponding to the identity code read in Step N2, executing Step Q3; if not, executing Step Q16;

Step Q3, the second CPU writing the value of the variable u_D which represents the predetermined high level breadth of the up stream calibrating impulse into the counter;

Step Q4, the second CPU sending a control signal to the communication interface circuit via the serial communication interface to increase the current on the signal bus consumed by the communication interface circuit;

Step Q5, sending a control signal to the counter to start it;

Step Q6, the second CPU monitoring whether the predetermined value u_D has been reached: if the judgement is positive, executing Step Q7; if not, continuing monitoring;

Step Q7, sending a control signal to the counter to stop it;

Step Q8, the second CPU writing the value of the variable v_D which represents the predetermined low level breadth of the up stream calibrating impulse into the

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counter;

Step Q9, the second CPU sending a control signal to the communication interface circuit via the serial communication interface to decrease the current on the signal bus consumed by the communication interface circuit;

Step Q10, sending a control signal to the counter to start it;

Step Q11, the second CPU monitoring whether the predetermined value v_D has been reached: if the judgement is positive, executing Step Q12; if not, continuing monitoring;

Step Q12, sending a control signal to the counter to stop it;

Step Q13, subtracting 1 from the value of the variable k which represents the number of the up stream calibrating impulses that are to be sent, and rendering the result to be a new value of the variable k, that is, k=k-1;

Step Q14, judging whether the value of the variable k is 0: if the judgement is positive, executing Step Q15; if not, returning to Step Q3;

Step Q15, the second CPU setting the calibrated state to the clock-calibrating indication digit at the interior of the second CPU;

Step Q16, ending the present electronic detonator clock-calibrating process.

In the electronic detonator clock-calibrating process mentioned above, the clock-calibrating instruction sent by the electronic detonator initiating device to a certain electronic detonator in the initiating network is corresponding to the second clock-calibrating instruction sent by the initiating device in Step G5 or Step M5. The present instruction is a single instruction, which includes the said synchronous studying heads and the clock-calibrating command word in sequence, and the identity code corresponding to the present electronic detonator as well. After receiving the second clock-calibrating instruction, the detonator will transmit the up stream calibrating waveform to the electronic detonator initiating device according to the predetermined high level breadth u_D, the predetermined low level breadth v_D, and the predetermined period n_D of the up stream calibrating impulse. After receiving the up stream calibrating waveform, the electronic detonator initiating device will calculate the clock frequency f_B of the detonator, and then obtain the adjusted new delay time data D_f which should be written into the present detonator according to the clock frequency f_B and the initial delay time data D_0 corresponding to the detonator, which realizes the function of calibrating the RC oscillator on line. Comparing the second embodiment of the electronic detonator clock-calibrating process with the first embodiment, on the one hand, the second CPU in the detonator does not need the function of complicated calculation, thereby the logic design of the chip can be simplified; on the other hand, the adjusting process of the delay time data is executed in the electronic detonator initiating device, therefore the delay precision of the electronic detonator can be adjusted flexibly according to the application requirements in the blasting engineering, thereby improving the adaptability of the electronic detonator for different delay precision requirements.

In the second embodiment of the aforementioned electronic detonator clock-calibrating process, a preferred embodiment lies in: the value of the variable v_D which represents the predetermined low level breadth is higher than the value of the variable u_D which represents the predetermined high level breadth; and the sum of the value of the variable v_D and the value of the variable u_D equals the value of the variable T_D which represents the predetermined period of the up stream calibrating impulse. The advantages lie in:

1. The electronic detonator transmits data to the electronic detonator initiating device in the form of current consumption, and when the detonator is transmitting

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the signal at high level in the up stream calibrating impulse, the consumed current will increase, thus the electronic detonator will consume more energy stored in the electronic detonator initiating device. So the energy consumed from the electronic detonator initiating device during the process of clock calibrating can be decreased by decreasing the breadth of the high level signal.

2. When the electronic detonator control chip is sending the high level signal in the up stream calibrating impulse, the input terminal of its rectifier bridge circuit is in the state of short circuit; at this moment, the process of charging the storage unit at the exterior of the electronic detonator control chip will stop, and the digital logic circuit inside the chip will still need to consume the energy in the storage unit for operating. When the electronic detonator control chip is sending the low level signal in the up stream calibrating impulse, the input terminal of the rectifier bridge circuit is in the state of turnoff; and at this moment, the storage unit at the exterior of the chip can be supplied power continuing. So if the predetermined high level breadth u_D of the calibrating impulse is decreased and the predetermined low level breadth v_D of the calibrating impulse is increased when sending the up stream calibrating waveform, the energy consumed from the storage unit can be decreased and the time for supplying power to the storage unit can be increased, which thereby improves the operating reliability of the electronic detonator control chip, decreases the current noises on the bus in the initiating network, and improves the stability of the initiating network.

Corresponding to the second embodiment of the electronic detonator clock-calibrating process, in the electronic detonator controlling flow mentioned above, the electronic detonator delay-time-writing process in Step N8 can be carried out in accordance with the following steps:

Step T1, the second CPU judging whether to write the delay time for the present detonator according to the detonator identity code included in the delay-time-writing instruction: if the detonator identity code in the delay-time-writing instruction is corresponding to the identity code read in Step N2, continuing with Step T2; if not, ending the present electronic detonator delay-time-writing process;

Step T2, the second CPU writing the delay time data D_f included in the delay-time-writing instruction into the programmable delay module;

Step T3, the second CPU setting the delay-time-set state to the delay time setting indication digit at the interior of the second CPU; and the second CPU transmitting the delay-time-writing-completed signal to the electronic detonator initiating device;

Step T4, ending the present electronic detonator delay-time-writing process.

Corresponding to the second embodiment of the electronic detonator clock-calibrating process, since the adjusting process of the delay time data is executed in the electronic detonator initiating device, the chip in the present embodiment only needs to write the delay time data D_f included in the delay-time-writing instruction directly into the programmable delay module. Therefore there is no need to set an arithmetical logic operation unit in the second CPU of the chip, which greatly simplifies the design of the chip.

Brief Description of the Drawings

FIG.1 is a network composition diagrammatic sketch of the electronic detonator initiating system according to the invention;

FIG.2 is an integral diagrammatic sketch of the functional composition of the initiating device according to the invention;

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FIG.3 is an integral sketch of the electronic detonator control chip according to the invention;

FIG.4 is a composition diagram of the logic control circuit in the chip according to the invention;

FIG.5 shows the first technical solution of the initiating device delay-time-setting flow according to the invention;

FIG.6 is a flow chart of the initiating device clock-calibrating flow according to the invention;

FIG.7 is a flow chart of the initiating device delay-time-writing flow according to the invention;

FIG.8 is a flow chart of the first embodiment of the initiating device clock-calibrating process according to the invention;

FIG.9 is a flow chart of the first embodiment of the initiating device delay-time-writing process according to the invention;

FIG.10 is a composition diagrammatic sketch of the first clock-calibrating instruction according to the invention;

FIG.11 is a flow chart of the initiating device calibrating-waveform-transmitting flow according to the invention;

FIG.12 is a flow chart of the second embodiment of the initiating device clock-calibrating process according to the invention;

FIG.13 is a flow chart of the second embodiment of the initiating deviece delay-time-writing process according to the invention;

FIG.14 shows the second technical solution of the initiating device delay-time-setting flow according to the invention;

FIG.15 is a flow chart of the initiating device delay-time-setting process according to the invention;

FIG.16 is a composition diagrammatic sketch of the global instruction according to the invention;

FIG.17 is a diagrammatic sketch of the delay-time-writing instruction according to the invention;

FIG.18 is a composition diagrammatic sketch of the second clock-calibrating instruction according to the invention;

FIG.19 is a composition diagrammatic sketch of the state-reading-back instruction according to the invention;

FIG.20 is a diagrammatic sketch of the electronic detonator control chip controlling flow according to the invention;

FIG.21 is a flow chart of the synchronous studying process according to the invention;

FIG.22 is a flow diagrammatic sketch of the first embodiment of the electronic detonator clock-calibrating process according to the invention;

FIG.23 is a flow diagrammatic sketch of the second embodiment of the electronic detonator clock-calibrating process according to the invention;

FIG.24 is a flow sketch of the electronic detonator state-reading-back process according to the invention;

FIG.25 is a flow diagrammatic sketch of the first embodiment of the electronic detonator delay-time-writing process according to the invention;

FIG.26 is a flow diagrammatic sketch of the second embodiment of the electronic detonator delay-time-writing process according to the invention;

FIG.27 is a diagrammatic sketch which shows the voltage waveform output by the logic control circuit to the communication interface circuit when the chip is

sending the up stream calibrating waveform according to the invention;

FIG.28 is a diagrammatic sketch which shows the current waveform output by the communication interface circuit to the signal bus when the chip is sending the up stream calibrating waveform according to the invention;

FIG.29 is a diagrammatic sketch which shows the clock impulse output by the RC oscillator according to the invention;

FIG.30 is a flow diagrammatic sketch which shows the signal receiving process executed by the initiating device according to the invention.

Detailed Description of Embodiments

The following further describes the embodiments of the present invention in more details with reference to accompanying drawings.

The electronic detonator initiating system according to the present invention consists of an initiating device 300 and at least one electronic detonator 400, comprising the detonator network as shown in FIG.1; at least one electronic detonator 400 is connected in parallel between the signal bus 500 extending from the initiating device 300.

In the electronic detonator initiating system mentioned above, the design of the initiating device is based on the technical solution disclosed in the Patent Application 200810135028.0, in which the initiating device 300 includes a control module 301, a man-machine interacting module 302, a power supply management module 303, a signal modulating and transmitting module 304, a signal demodulating and receiving module 305 and a power supply 302, as shown in FIG.2. The control module 301 further includes a first CPU and a timer. The technical solution of the initiating device forms the basic frame of the electronic detonator initiating device and realizes the basic functions of the initiating device such as bidirectional communication with the electronic detonator and igniting the electronic detonator.

In the electronic detonator initiating system mentioned above, the chip in the electronic detonator 400 is further improved based on the Patent 200820111269.7 and Patent Application 200810211374.2, and an electronic detonator control chip 200 the clock of which can be calibrated is disclosed as FIG.3 shows. The chip 200 includes a rectifier bridge circuit 201, a firing control circuit 202, an energy management module 204, a communication interface circuit 203, a non-volatile memory 205, a clock circuit 206, a power supply management circuit 207, and a logic control circuit 208, wherein the RC oscillator 210 is chosen to be the clock circuit 206 to improve the anti-shock performance of the electronic detonator control chip 200. Wherein the energy management module 204 may consist of a charging circuit 401 and a safe discharging circuit 403, corresponding to the technical solution of the electronic detonator control chip disclosed in Patent 200820111270.X. The energy management module 204 may also consist of a charging circuit 401, a charging control circuit 402 and a safe discharging circuit 403 corresponding to the technical solution of the electronic detonator control chip disclosed in Paten 200820111269.7. Preferably, the energy management module 204 may consist of a charging circuit 401, a safe discharging circuit 403 and a detecting circuit corresponding to the technical solution of the electronic detonator control chip disclosed in Patent Application 200810108689.4. Or, the energy management module 204 may also consist of a charging circuit 401, a charging control circuit 402, a safe discharging circuit 403 and a detecting circuit corresponding to the technical solution of the electronic detonator control chip disclosed in Patent Application 200810108688.X. The logic control circuit 208 mentioned above can further include

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a programmable delay module 281, an input/output interface 282, a serial communication interface 283, a prescaler 284, a counter 287, and a CPU 285, as shown in FIG.4. One end of the counter 287 is connected with the power supply output terminal of the power supply management circuit 207, being powered by the power supply management circuit 207; one end is grounded; one end is connected to the CPU 285 via the internal bus 286, and the CPU 285 controls the operation of the counter 287 and reads the counting results in it; and the other end of the counter 287, the CPU 285, the programmable delay module 281 and the prescaler 284 connect together, and are jointly connected to the RC oscillator 210 which supplies the operating clock signals. The electronic detonator control chip 200 designed in the aforementioned way acts better in the anti-shock performance, and can realize the delay time precision that meets the demands. The chip 200 uses the RC oscillator as the clock circuit to improve the anti-shock performance of the detonator. To solve the problems of the RC oscillator such as the frequency excursion and the frequency difference, the present invention uses the initiating device 300 at the external of the chip 200 to calibrate the clock of the chip 200 by sending the control instruction to the chip 200, thereby increasing the delay time precision of the initiating system.

As one aspect of the present invention, there are two technical solutions of the initiating device delay-time-setting flow, wherein one of which can be carried out in accordance with the steps shown in FIG.5 as a reference.

Step A1, the control module 301 in the initiating device 300 executing an initiating device clock-calibrating flow;

Step A2, executing an initiating device delay-time-writing flow;

Step A3, outputting an error information list to the man-machine interacting module 302 for displaying;

Step A4, ending the present initiating device delay-time-setting flow.

In the first technical solution of the initiating device delay-time-setting flow shown in FIG.5, before the initiating device delay-time-writing flow, the initiating device executes the initiating device clock-calibrating flow to calibrate the clock frequency of the electronic detonator 400, which ensures the delay time precision of every electronic detonator 400 in the initiating network, thus improving the delay time precision of the whole initiating network. In Step A3, the delay-setting error information list is sent to the man-machine interacting module 302 for displaying, so that, according to the delay-setting error information and the importance degree of the blasting hole where the electronic detonator is, the operators of the initiating device can judge whether to re-execute the initiating device delay-time-setting flow to ensure that all the electronic detonators 400 have been set the delay time, or to proceed with the following operation to the electronic detonators 400 in the initiating network which have been set the delay time completely. Such solution has improved the control flexibility of the blasting operation.

Generally, combining the main control flow of the electronic detonator initiating device disclosed in Patent Application 200810135028.0, it is preferred to execute the initiating device delay-time-setting flow after the initiating preparation task and before the initiating network charging task, which makes the data exchange between the initiating device and the electronic detonator 400 during the whole present flow be carried out under the communication voltage, thereby ensuring the security of the delay-time-setting process.

In the initiating device delay-time-setting flow shown in FIG.5, the initiating device clock-calibrating flow in Step A1 can be carried out in accordance with the following steps as shown in FIG.6:

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Step B1, initializing the present initiating device clock-calibrating flow, that is, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and the cycle number W_1 into the cache of the control module; wherein the value of the variable E_1 is equal to the value of the number N;

Step B2, the control module 301 judging whether the value of the cycle number W_1 and the variable E_1 is 0: if the value of the cycle number W_1 or the value of the variable E_1 is 0, ending the present initiating device clock-calibrating flow; if not, continuing with Step B3;

Step B3, executing an initiating device clock-calibrating process;

Step B4, subtracting 1 from the value of the cycle number W_1, and rendering the result to be a new value of the cycle number W_1, that is, $W_1=W_1-1$; then returning to Step B2.

In the initiating device delay-time-setting flow shown in FIG.5, the initiating device delay-time-writing flow in Step A2 can be carried out in accordance with the following steps as shown in FIG.7:

Step E1, initializing the present initiating device delay-time-writing flow, that is, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_2 which represents the number of the electronic detonators which contain errors in the process of delay-time-writing, and the cycle number W_2 into the cache of the control module 301; wherein the value of the variable E_2 is equal to the value of the number N;

Step E2, the control module 301 judging whether the value of the cycle number W_2 and the value of the variable E_2 is 0: if the value of the cycle number W_2 or the value of the variable E_2 is 0, executing Step E5; if not, continuing with Step E3;

Step E3, executing an initiating device delay-time-writing process;

Step E4, subtracting 1 from the value of the cycle number W_2, and rendering the result to be a new value of the cycle number W_2, that is, $W_2=W_2-1$; then returning to Step E2;

Step E5, ending the present initiating device delay-time-writing flow.

In the initiating device clock-calibrating flow shown in FIG.6 and the initiating device delay-time-writing flow shown in FIG.7 mentioned above, the variables of the cycle number W_1 and the cycle number W_2 are designed to respectively control the running times of the initiating device clock-calibrating process in Step B3 and the initiating device delay-time-writing process in Step E3; the mode that one time's execution of the initiating device delay-time-setting flow once can automatically cause several times' circular execution of the clock-calibrating process and the delay-time-writing process has simplified the operation steps, thereby decreasing the misoperation resulting from people's complex and repetitious operations and improving the operating reliability of the device. Every time after the initiating device delay-time-setting flow shown in FIG.5 is executed completely, an error information list will be output to prompt the choice for the next operation, and the possibility of clock-calibrating error or delay-time-writing error resulting from the instantaneous fault of the network does exist in the initiating system, therefore the solution in which the initiating device 300 automatically executes the clock-calibrating process for W_1 times as predetermined and executes the delay-time-writing process for W_2 times as

predetermined can simplify the operation of the operator and improve the operating reliability of the initiating device. As shown in FIG.6 and FIG.7, when the initiating device 300 has accomplished the clock-calibrating process for W_1 times as predetermined or there is no electronic detonator with any clock-calibrating error in the system, the initiating device clock-calibrating flow will end; and when the initiating device has accomplished the delay-time-writing process for W_2 times as predetermined or there is no electronic detonator with any delay-time-writing error in the system, the initiating device delay-time-writing flow will end.

In the initiating device clock-calibrating flow shown in FIG.6, the first embodiment of the initiating device clock-calibrating process in Step B3 can be carried out in accordance with the following steps as shown in FIG.8:

Step C1, transmitting a first clock-calibrating instruction to all the electronic detonators 400 in the initiating network;

Step C2, the control module 301 waiting for a time T_0 which represents a predetermined delay: if reaching the time, executing Step C3; if not, continuing waiting;

Step C3, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, that is, $L=E_1$;

Step C4, reading the identity code stored in the initiating device 300 corresponding to a certain electronic detonator in the initiating network;

Step C5, reading the state information stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step C6, judging whether the present electronic detonator 400 is in the calibrated state according to the state information of the detonator: if the judgement is positive, executing Step C13; if not, executing Step C7;

Step C7, transmitting a state-reading-back instruction to the present electronic detonator 400;

Step C8, the control module 301 executing a signal receiving process: if receiving the information returned by the present electronic detonator 400, executing Step C9; if not, executing Step C12;

Step C9, the control module 301 storing the information returned by the present electronic detonator, and judging whether the clock-calibrating indication digit of the electronic detonator is in the calibrated state: if the judgement is positive, executing Step C10; if not, executing Step C12;

Step C10, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400;

Step C11, subtracting 1 from the value of the variable E_1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$; then continuing with Step C13;

Step C12, setting the clock-calibrating error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400; and then executing Step C13;

Step C13, subtracting 1 from the value of the variable L which represents the number of electronic detonators that are to be calibrated, and rendering the result to be a new value of the variable L, that is, $L=L-1$;

Step C14, judging whether the value of the variable L which represents the

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number of electronic detonators that are to be calibrated is 0: if the judgement is positive, continuing with Step C15; if not, returning to Step C4;

Step C15, ending the present initiating device clock-calibrating process.

Corresponding to the first embodiment of the initiating device clock-calibrating process shown in FIG.8, Step E3, the initiating device delay-time-writing process in the initiating device delay-time-writing flow shown in FIG.7 can be carried out in accordance with the following steps as shown in FIG.9:

Step F1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step F2, reading the identity code stored in the initiating device 300 corresponding to a certain electronic detonator 400 in the initiating network;

Step F3, reading the state information stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step F4, judging whether the present electronic detonator 400 is in the calibrated state according to the state information of the detonator: if the judgement is negative, executing Step F9; if the judgement is positive, executing Step F5;

Step F5, reading the value D_0 of the delay time data stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step F6, transmitting a delay-time-writing instruction including the value D_0 of the delay time data to the present electronic detonator 400;

Step F7, the control module 301 executing a signal receiving process: if receiving the delay-time-writing-completed signal returned by the present electronic detonator 400, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, and then executing Step F8; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, and then executing Step F9;

Step F8, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

Step F9, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, R=R-1;

Step F10, judging whether the value of the variable R is 0: if the judgement is positive, executing Step F11; if not, returning to Step F2;

Step F11, ending the present initiating device delay-time-writing process.

In the first embodiment of the initiating device clock-calibrating process shown in FIG.8, the first clock-calibrating instruction which is sent to all the electronic detonators 400 in the initiating network in Step C1 is a global instruction. The first clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and a down stream calibrating waveform; and the down stream calibrating waveform consists of a string of down stream calibrating impulses, the period of which is a predetermined period T_B and the sum of which is a predetermined number n_B,as shown in FIG.10. The initiating device 300 sends the synchronous studying heads and the down stream calibrating waveform with the steady and accurate clock source of itself to the chip, so that the counter 287 in the chip 200 can count the down stream calibrating waveform in sections, thereby figuring out the clock frequency of the chip 200 itself.

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The advantages of sending the synchronous studying heads before sending the instruction command word lie in: when the edge signal of the synchronous studying head is received by the electronic detonator control chip 200, the counter 287 in the chip 200 will be started to count the number of the synchronous studying heads. Then the CPU 285 in the chip 200 will calculate the clock number of the RC oscillator which should be used by the serial communication interface 283 and is respectively corresponding to the predetermined communication baud rate and the predetermined sampling phase, thereby adjusting the data receiving time and the counting interval of the electronic detonator, as the synchronous studying process of the electronic detonator 400 in FIG.21 shows.. Therefore, it can be ensured that the electronic detonator control chip 200 with a RC oscillator 210 inside can still reliably receive the control instructions sent by the electronic detonator initiating device even if the problems such as temperature excursion, clock excursion and parameter changes still exist in the RC oscillator.

The down stream calibrating waveform in the first clock-calibrating instruction shown in FIG.10 is sent by the control module 301 executing the following initiating device calibrating-waveform-transmitting flow as shown in FIG.11:

Step D1, setting the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted to be the same as the value of the variable n_B which represents the predetermined number of the down stream calibrating impulses, that is, $n=n_B$;

Step D2, writing the value of the variable v_B which represents the predetermined low level breadth of the down stream calibrating impulse into the timer;

Step D3, transmitting a control signal to the signal modulating and transmitting module 304 to render it output a down edge signal;

Step D4, transmitting a control signal to the timer to start it;

Step D5, the first CPU monitoring whether the length of the low level signal output by the signal modulating and transmitting module 304 has reached the predetermined low level breadth v_B: if the judgement is positive, executing Step D6; if not, continuing monitoring;

Step D6, transmitting a control signal to the timer to stop it;

Step D7, writing the value of the variable u_B which represents the predetermined high level breadth of the down stream calibrating impulse into the timer;

Step D8, transmitting a control signal to the signal modulating and transmitting module 304 to render it output an up edge signal;

Step D9, transmitting a control signal to the timer to start it;

Step D10, the first CPU monitoring whether the length of the high level signal output by the signal modulating and transmitting module 304 has reached the predetermined high level breadth u_B: if the judgement is positive, executing Step D11; if not, continuing monitoring;

Step D11, transmitting a control signal to the timer to stop it;

Step D12, subtracting 1 from the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted, and rendering the result to be a new value of the variable n, that is, n=n-1;

Step D13, judging whether the value of the variable n is 0: if the judgement is positive, executing Step D14; if not, returning to Step D2;

Step D14, ending the present initiating device

calibrating-waveform-transmitting flow.

In the initiating device calibrating-waveform-transmitting flow shown in FIG.11, the value of the variable u_B which represents the predetermined high level breadth of the down stream calibrating impulse is higher than the value of the variable v_B which represents the predetermined low level breadth of the down stream calibrating impulse, and the sum of the value of the variable u_B and the value of the variable v_B equals the value of the predetermined period T_B as the down stream calibrating waveform in FIG.10 shows. Considering the two embodiments that the master communication interface consists of the single-polarity communication interface or the dual-polarity communication interface disclosed in Patent Application 200810172410.9, the advantages of the present embodiment of the down stream calibrating impulse lie in: when sending the high level calibrating impulse to the electronic detonator 400, the initiating device 300 is in the state of supplying positive voltage to the detonator 400; while sending the low level calibrating impulse to the electronic detonator 400, the initiating device is in the state of supplying no power or supplying negative voltage to the detonator 400. So increasing the high level breadth of the calibrating impulse can extending the time of sending the high level signal, thereby the time during which the initiating device 300 supplies power to the detonator 400 can be extended and the energy consumption of the storage unit 600 in the electronic detonator 400 can be decreased, which is beneficial to improve the operating reliability of the control chip 200 in the electronic detonator 400, to decrease the current noises of the bus in the initiating network, and to improve the stability of the initiating network.

In the first embodiment of the initiating device clock-calibrating process shown in FIG.8 mentioned above, the state-reading-back instruction in Step C7 which is sent to a certain electronic detonator is a single instruction for the present detonator. The state-reading-back instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the state-reading-back command word, and the identity code of the present electronic detonator, as shown in FIG.19. By sending the present instruction to the electronic detonator 400, the initiating device 300 can obtain the state information of the electronic detonator 400, thus the initiating device can control the operation of the detonator more reliably.

In the initiating device delay-time-writing process shown in FIG.9, the delay-time-writing instruction in Step F6 sent to a certain electronic detonator in the initiating network is a single instruction for the present electronic detonator. The delay-time-writing instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the delay-time-writing command word, the identity code of the present electronic detonator and the delay time data D_0 of the present corresponding electronic detonator. The initiating device can write in the delay time data for every electronic detonator 400 in the network one by one by executing the initiating device delay-time-writing process shown in FIG.9; thereby accomplish designing the delay time of the detonator network. After receiving the delay time data sent by the electronic detonator initiating device 300, the CPU 285 in the electronic detonator control chip 200 will firstly execute the electronic detonator delay-time-data-adjusting process to figure out a new delay time data D_N according to the calculated clock frequency f_D of the present detonator which is the calculation result of the electronic detonator clock-calibrating process shown in FIG.22; then the CPU 285 writes the adjusted delay time data D_N into the programmable delay

module 281 in the chip 200.

The second embodiment of Step B3, the initiating device clock-calibrating process in the initiating device clock-calibrating flow shown in FIG.6 can be carried out in accordance with the following steps as shown in FIG.12:

Step G1, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, that is, $L=E_1$;

Step G2, reading the identity code stored in the initiating device 300 corresponding to a certain electronic detonator 400 in the initiating network;

Step G3, reading the state information stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step G4, judging whether the present electronic detonator 400 is in the calibrated state according to the state information of the present detonator: if the judgement is positive, executing Step G12; if not, executing Step G5;

Step G5, transmitting a second clock-calibrating instruction to the present electronic detonator 400;

Step G6, the control module 301 executing the signal receiving process: if receiving the up stream calibrating waveform returned by the present electronic detonator 400, executing Step G7; if not, setting the clock-calibrating error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, then executing Step G12;

Step G7, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400;

Step G8, subtracting 1 from the value of the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$;

Step G9, counting the up stream calibrating waveform consisting of a string of up stream calibrating impulses, the period of which is a predetermined period T_D and the sum of which is a predetermined number n_D; representing the counting result as a value F_B;

Step G10, calculating the clock frequency f_B of the present electronic detonator 400 according to the value of the variable n_D, the variable T_D and the variable F_B;

Step G11, storing the clock information of the present electronic detonator 400 and the clock information includes the value of the clock frequency f_B;

Step G12, subtracting 1 from the value of the variable L which represents the number of electronic detonators that are to be calibrated, and rendering the result to be a new value of the variable L, that is, $L=L-1$;

Step G13, judging whether the value of the variable L is 0: if the judgement is positive, continuing with Step G14; if not, returning to Step G2;

Step G14, ending the present initiating device clock-calibrating process.

Corresponding to the second embodiment of the initiating device clock-calibrating process shown in FIG.12, Step E3, the initiating device delay-time-writing process in the initiating device delay-time-writing flow shown in FIG.7 can be carried out in accordance with the following steps as shown in FIG.13:

Step H1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value

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of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step H2, reading the identity code stored in the initiating device 300 corresponding to a certain electronic detonator 400 in the initiating network;

Step H3, reading the state information stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step H4, judging whether the present electronic detonator is in the calibrated state according to the state information of the present detonator 400: if the judgement is negative, executing Step H10; if the judgement is positive, executing Step H5;

Step H5, reading the value D_0 of the delay time data stored in the initiating device 300 corresponding to the present electronic detonator 400; and reading the value of the clock frequency f_B stored in the control module 301 corresponding to the present electronic detonator 400;

Step H6, executing an initiating device delay-time-data-adjusting flow to figure out a new value D_f of the delay time data according to the value of the clock frequency f_B;

Step H7, transmitting a delay-time-writing instruction including the variable D_f to the present electronic detonator 400;

Step H8, the control module 301 executing the signal receiving process: if receiving the delay-time-writing-completed signal returned by the present electronic detonator 400, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, and then executing Step H9; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, and then executing Step H10;

Step H9, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

Step H10, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, R=R-1;

Step H11, judging whether the value of the variable R is 0: if the judgement is positive, executing Step H12; if not, returning to Step H2;

Step H12, ending the present initiating device delay-time-writing process.

In the initiating device clock-calibrating process shown in FIG.12, the second clock-calibrating instruction in Step G5 which is sent to a certain electronic detonator is a single instruction for the present electronic detonator. The second clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and the identity code of the present electronic detonator, as shown in FIG.18. After sending the clock-calibrating instruction to the present electronic detonator 400, the initiating device 300 waits to receive the up stream calibrating waveform which is returned by the electronic detonator 400 according to the predetermined high/low level breadth of the up stream calibrating impulse and the predetermined number of the period of the up stream calibrating impulse. Considering the operation principle of the slave data modulation module disclosed in Patent Application 200810172410.9, the electronic detonator 400 transmits the up stream calibrating waveform to the initiating device 300 in the form of current consumption changes. After receiving the aforementioned up stream calibrating waveform, the initiating device 300 will calculate the clock

frequency f_B of the present detonator 400. In the initiating device delay-time-writing process shown in FIG.13, the control module 301 executes the initiating device delay-time-data-adjusting flow according to the clock frequency f_B, and obtains the adjusted delay time data D_f which should be written into the present detonator 400. After receiving the delay time data D_f, the electronic detonator control chip 200 only needs to write the data D_f directly into the programmable delay module 281 in the chip 200. The principle of calculating the detonator clock frequency f_B in the initiating device 300 is nearly the same as the principle of calculating in the chip 200; and calculating the clock frequency in the initiating device 300 is beneficial to simplify the design of the electronic detonator control chip 200.

In the initiating device delay-time-writing process shown in FIG.13, the form of the delay-time-writing instruction transmitted in Step H7 is the same as the form of the delay-time-writing instruction transmitted in Step F6, as shown in FIG.17. The difference between the two lies in that the delay time data in the delay-time-writing instruction in Step H7 is the adjusted delay time data D_f obtained from the execution of the initiating device delay-time-data-adjusting flow.

The initiating device delay-time-data-adjusting flow in Step H6 can be carried out in accordance with the following principle: since the former delay time data D_0 stored in the initiating device 300 is calculated according to the predetermined clock frequency (represented as f_0) of the electronic detonator 400, and the time represented by the data D_0 is calculated by the formula D_0/f_0; therefore the delay time data D_f which is sent to the electronic detonator control chip 200 and is figured out according to the clock frequency f_B that is figured out in the initiating device clock-calibrating process shown in FIG.12 should satisfy the following formula: $D_0/f_0=D_f/f_B$. So the adjusted delay time data D_f can be obtained according to the following formula: $D_f=D_0 \times f_B/f_0$.

The initiating device delay-time-setting flow in the present invention can also be carried out in accordance with the following second embodiment as shown in FIG.14:

Step L1, initializing the present initiating device delay-time-setting flow, that is, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, the variable E_2 which represents the number of the electronic detonators that contain errors in the process of delay-time-writing, and the cycle number W into the cache of the control module; wherein both the value of the variable E_1 and the value of the variable E_2 are equal to the value of the number N;

Step L2, judging whether the value of the cycle number W and the value of the variable E_2 is 0: if the value of the cycle number W or the value of the variable E_2 is 0, executing Step L5; if not, continuing with Step L3;

Step L3, the control module 301 executing the initiating device delay-time-setting process;

Step L4, subtracting 1 from the value of the cycle number W, and rendering the result to be a new value of the cycle number W, that is, W=W-1; then returning to Step L2;

Step L5, the control module 301 outputting an error information list to the man-machine interacting module 302 for displaying;

Step L6, ending the present initiating device delay-time-setting flow.

In the solution shown in FIG.14, if all the detonators 400 in the network have

been set the delay time successfully, the initiating device delay-time-setting flow will end. In addition, if the initiating device delay-time-setting process has been executed for W times as predetermined, the control module will end the execution cycle and output an error information list to show to the operators no matter whether there are still some detonators which have not been set the delay time successfully. The cycle number W is designed to control the running times of the initiating device delay-time-setting process in Step L3, and the mode that one time's execution of the initiating device delay-time-setting flow will automatically cause several times' circular execution of the initiating device delay-time-setting process can also simplify the operation steps.

In the initiating device delay-time-setting flow shown in FIG.14, wherein Step L3 can be carried out in accordance with the following steps as shown in FIG.15:

Step M1, setting the value of the variable S which represents the number of the electronic detonators that are to be set the delay time to be the same as the value of the variable E_1, that is, $S=E_1$;

Step M2, reading the identity code stored in the initiating device 300 corresponding to a certain electronic detonator 400 in the initiating network;

Step M3, reading the state information stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step M4, judging whether the present electronic detonator 400 is in the state that the delay time has been set according to the state information of the present detonator: if the judgement is positive, executing Step M15; if not, executing Step M5;

Step M5, transmitting a second clock-calibrating instruction to the present electronic detonator 400;

Step M6, the control module 301 executing the signal receiving process: if receiving the up stream calibrating waveform returned by the present electronic detonator 400, the control module will set the clock-calibrating succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, then executing Step M7; if not, the control module will set the clock-calibrating error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, then executing Step M15;

Step M7, subtracting 1 from the value of the variable E_1, and rendering the result to be a new value of the variable E_1, that is, $E_1= E_1-1$;

Step M8, the control module 301 counting the up stream calibrating waveform consisting of a string of up stream calibrating impulses, the period of which is a predetermined period T_D and the sum of which is a predetermined number n_D, and representing the counting result as a value F_B;

Step M9, calculating the clock frequency f_B of the present electronic detonator according to the value of the variable n_D, the variable T_D and the variable F_B;

Step M10, reading the value D_0 of the delay time date stored in the initiating device 300 corresponding to the present electronic detonator 400;

Step M11, executing the initiating device delay-time-data-adjusting flow, to figure out a new value D_f of the delay time data according to the value of the clock frequency f_B;

Step M12, transmitting a delay-time-writing instruction including the value D_f to the present electronic detonator 400;

Step M13, the control module 301 executing the signal receiving process: if receiving the delay-time-writing-completed signal returned by the present

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electronic detonator 400, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, and then executing Step M14; if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device 300 and is corresponding to the present electronic detonator 400, then executing Step M15;

Step M14, subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2 = E_2 - 1$;

Step M15, subtracting 1 from the value of the variable S, and rendering the result to be a new value of the variable S, that is, S= S-1;

Step M16, judging whether the value of the variable S is 0: if the judgement is positive, executing Step M17; if not, returning to Step M2;

Step M17, ending the present initiating device delay-time-setting process.

In the initiating device delay-time-setting process mentioned above shown in FIG.15, the initiating device writes the delay time for a certain electronic detonator immediately after the clock of the present detonator is calibrated. In this way, the initiating device can accomplish the delay-time-setting process for all the electronic detonators 400 in the initiating network one by one, which can omit the storage for the detonator clock frequency f_B which is figured out, so it is beneficial to simplify the design.

In the initiating device delay-time-setting process mentioned above, shown in FIG.15, the second clock-calibrating instruction in Step M5 which is sent to a certain electronic detonator is a single instruction for the present electronic detonator. The second clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and the identity code of the present electronic detonator.

In the initiating device delay-time-setting process mentioned above shown in FIG.15, the delay-time-writing instruction in Step M12 which is sent to a certain detonator in the initiating network is a single instruction for the present detonator. The delay-time-writing instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the delay-time-writing command word, the identity code of the present electronic detonator and the delay time data of the present corresponding electronic detonator, as shown in FIG.17. The delay time data in the present delay-time-writing instruction is the adjusted delay time data D_f which is obtained from the initiating device delay-time-data-adjusting flow.

The signal receiving process in the aforementioned control flows can be carried out in accordance with the following embodiment disclosed in Patent Application 200810135028.0 shown in FIG.30 as a reference:

Step Ⅰ, transferring a predetermined signal receiving overtime value T' from the control module 301;

Step Ⅱ, detecting whether the time during which the control module 301 receives data sent from the electronic detonator has reached the predetermined signal receiving overtime value T': if the judgment is positive, ending the present signal receiving process; if not, continuing with step Ⅲ;

Step Ⅲ, detecting whether the control module 301 has received the serial signals sent by the signal conditioning circuit in the signal demodulating and receiving module 305: if the judgment is positive, sampling the serial signals and

obtaining the information of the electronic detonator, then going back to step II ; if not, going back to step II directly.

As the other aspect of the present invention, the controlling flow of the electronic detonator control chip 200 in the electronic detonator 400 can be carried out in accordance with the following steps, as shown in FIG.20:

Step N1, the CPU 285 in the interior of the chip 200 sending a control signal to the programmable delay module 281, rendering the programmable delay module 281 output a signal to cut off the firing control circuit 202 and to make it in the fire-forbidden state;

Step N2, the CPU 285 reading the identity code stored in the non-volatile memory 205 corresponding to the present electronic detonator 400;

Step N3, the CPU 285 waiting to receive the synchronous studying head sent by the electronic detonator initiating device 300: if the synchronous studying head is received, continuing with Step N4; if not, continuing waiting;

Step N4, the CPU 285 executing the synchronous studying process; and adjusting the clock number of the RC oscillator which will be written into the prescaler 284 according to the received synchronous studying head, wherein the clock number is corresponding to the predetermined communication baud rate and the predetermined sampling phase;

Step N5, the CPU 285 waiting to receive the command words sent by the electronic detonator initiating device 300: if the clock-calibrating command word is received, entering the clock-calibrating state, then continuing with Step N6; if the state-reading-back command word is received, entering the state-reading-back state, then continuing with Step N7; if the delay-time-writing command word is received, entering the delay-time-writing state, then continuing with Step N8; if the firing command word is received, entering the firing state, then continuing with Step N9;

Step N6, executing an electronic detonator clock-calibrating process; and then returning to Step N5;

Step N7, executing an electronic detonator state-reading-back process; and then returning to Step N5;

Step N8, executing an electronic detonator delay-time-writing process; and then returning to Step N5;

Step N9, executing an electronic detonator firing process;

Step N10, ending the present electronic detonator controlling flow.

The controlling flow mentioned above shown in FIG.20 has realized the external on-line controllability of the clock-calibrating process, the state-reading-back process, the delay-time-writing process, and the firing process of the electronic detonator 400, which can be described as follows:

Firstly, with the accurate clock of itself, the electronic detonator initiating device 300 can ensure the delay accuracy of the electronic detonator initiating network by the mode of calibrating the clock under the control of the on-line instruction. Calibrating the clock of the electronic detonator control chip 200 can avoid the problem of delay accuracy resulting from the factors such as temperature excursion, clock excursion or parameter change of the RC oscillator

Secondly, in the electronic detonator state-reading-back process, the electronic detonator initiating device 300 mentioned above realizes the functions of reading back the state information of the electronic detonator 400, such as the state information of the clock-calibrating and the state information of the delay-time-writing, thereby controlling the operation of the detonators 400 more reliably.

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Thirdly, in the electronic detonator delay-time-writing process, the electronic detonator initiating device 300 realizes the function of setting the delay time on-line for the electronic detonator 400. Furthermore, according to the exact clock information of the electronic detonator which is resulting from the execution of the electronic detonator clock-calibrating process, the initiating device can write the adjusted delay time data into the electronic detonator 400, thereby improving the flexibility of use of the electronic detonator 400.

Fourthly, the initiating device 300 mentioned above realizes the control of the igniting of the electronic detonator by executing the electronic detonator firing process, which makes the igniting process more reliable.

In the controlling flow mentioned above shown in FIG.20, the synchronous studying process in Step N4 can be carried out in accordance with the following steps, as shown in FIG.21:

Step O1, the CPU 285 monitoring whether the edge signal sent by the electronic detonator initiating device 300 is received: if the judgement is positive, executing Step O2; if not, continuing monitoring;

Step O2, sending a control signal to the counter 287 to start it;

Step O3, the CPU 285 monitoring whether another edge signal sent by the electronic detonator initiating device 300 is received: if the judgement is positive, executing Step O4; if not, continuing monitoring;

Step O4, the CPU 285 reading the value of the counter 287 at the present moment, and storing the counting result;

Step O5, the CPU 285 judging whether the number of the received edge signals has reached as much as twice the predetermined number m which represents the number of the synchronous studying heads, that is, judging whether the number of the received edge signals has reached the value 2m: if the judgement is positive, executing Step O6; if not, returning to Step O3;

Step O6, sending a control signal to the counter 287 to stop it;

Step O7, the CPU 285 calculating the clock number of the RC oscillator which will be written into the prescaler 284 according to the counting results stored in the cache of the CPU 285, wherein the clock number is corresponding to the predetermined communication baud rate and the predetermined sampling phase;

Step O8, writing the clock number into the prescaler 284;

Step O9, ending the present synchronous studying process.

The synchronous studying process shown in FIG.21 eliminates the effect on the reliability of data receiving of the electronic detonator caused by the frequency dispersal of the RC oscillator which is integrated in the chip 200. When transmitting an instruction to the chip 200, the initiating device 300 transmits the synchronous studying heads, sum of which is a predetermined number m, before transmitting the command word, as the instruction composition in FIG.16 to FIG.19 shows. At the interior of the chip 200, when the edge signal of the synchronous studying head is received, the counter 287 in the chip 200 will be started to count the number of the synchronous studying heads; since each synchronous studying head includes an up edge and a down edge, if the number of the received edge signals has reached the value 2m, it can be considered that the synchronous studying heads, the number of which is the value m, have been received. Then the CPU 285 will calculate the clock number of the RC oscillator which should be used by the serial communication interface 283 and is respectively corresponding to the predetermined communication baud rate and the predetermined sampling phase, thereby adjusting the data receiving time and the counting interval of the electronic detonator 400. Therefore,

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it can be ensured that the electronic detonator control chip with a RC oscillator 210 inside can still reliably receive the control instructions sent by the electronic detonator initiating device 300 even if the problems such as temperature excursion, clock excursion and parameter changes still exist in the RC oscillator.

In the electronic detonator controlling flow shown in FIG.20, the first embodiment of the electronic detonator clock-calibrating process in Step N6 can be carried out in accordance with the following steps as shown in FIG.22:

Step P1, the CPU 285 monitoring whether the edge signal sent by the electronic detonator initiating device 300 is received: if the judgement is positive, executing Step P2; if not, continuing monitoring;

Step P2, sending a control signal to the counter 287 to start it;

Step P3, monitoring whether another edge signal sent by the electronic detonator initiating device 300 is received: if the judgement is positive, executing Step P4; if not, continuing monitoring;

Step P4, reading the value of the counter 287 at the present moment, and storing the counting result into the cache of the CPU 285;

Step P5, the CPU 285 judging whether the number of the received edge signals has reached as much as twice the predetermined number n_B which represents the number of the down stream calibrating impulses, that is, judging whether the number of the received edge signals has reached the value $2n_B$: if the judgement is positive, executing Step P6; if not, returning to Step P3;

Step P6, sending a control signal to the counter 287 to stop it;

Step P7, the CPU 285 calculating the value of the clock frequency f_D of the RC oscillator according to the counting results stored in the counter, the predetermined number n_B which represents the number of the down stream calibrating impulses, and the predetermined period T_B of the down stream calibrating impulses;

Step P8, the CPU 285 setting the clock-calibrating indication digit at the interior of the CPU 285 to be in the calibrated state;

Step P9, ending the present electronic detonator clock-calibrating process.

In the electronic detonator clock-calibrating process mentioned above shown in FIG.22, the clock-calibrating instruction sent by the electronic detonator initiating device 300 to all the electronic detonators in the initiating network is corresponding to the first clock-calibrating instruction in Step C1 said above. The instruction is a global instruction for all the electronic detonators 400 in the initiating network, which includes the synchronous studying heads and the clock-calibrating command word in sequence, and the down stream calibrating waveforms consisting of a string of down stream calibrating impulses, the period of which is a predetermined period T_B and the sum of which is a predetermined number n_B as well, as shown in FIG.10. The electronic detonator initiating device 300 transmits the down stream calibrating waveform mentioned above with the steady and accurate clock source of itself for the counter 287 in the chip 200 to count the waveform in sections. The CPU 285 in the chip 200 calculates the clock frequency f_D of the RC oscillator 210 of the chip itself according to the counting results, the predetermined number n_B and the predetermined period T_B of the down stream calibrating impulse, as shown in FIG.29, and then stores the calculating result in the chip 200. The factors such as temperature excursion, clock excursion and parameter changes of the RC oscillator may result in individual differences in the clock frequency of each electronic detonator control chip 200, therefore using a uniform, steady and accurate clock source of the electronic detonator initiating device 300 to calibrate the clock of the chip 200 is beneficial to eliminate the effect on the delay precision of the initiating

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network resulting from individual differences of the electronic detonators, thus the delay precision of the initiating network can be improved.

The calculating principle of the clock frequency f_D can be described as follows:

The counting result N(N=N[1], N[2], N[3], ..., N[$2n_B$]) of the clock number in the chip corresponding to the time $n' \times T_B$(n'=1, 2, 3, ..., n_B) represented by the down stream calibrating waveform is in inverse proportion to the clock period 1/f of the RC oscillator 210, that is, in direct proportion to the clock frequency f of the RC oscillator 210, so the formula is expressed as $n' \times T_B = N/f$, thereby: $f = N/(n' \times T_B)$. Wherein the stored counting result N (N=N[1], N[2], N[3], ..., N[$2n_B$]) which is chosen for calculation should be corresponding to the value of the period number n' chosen for calculation of the down stream calibrating impulse. Taking example for the down stream calibrating impulse in the first period in the first clock-calibrating instruction, when the edge signal 1 is received, the counter 287 will start to count; when the edge signal 2 is received, the counting result N[1] at the present moment will be read and stored; when the edge signal 3 is received, the counting result N[2] at the present moment will be read and stored, thus accomplishing receiving and counting the down stream calibrating impulse in the first period. In the calculation of the clock frequency, the period number n' should be equal to 1, while the counting result N should be equal to N[2], and analogizing accordingly. During the actual process of calculating, in order to improve the precision of the calculated clock frequency, it is better to choose the average of several values of the clock frequency which are figured out in sections as the clock frequency f_D. The method of section division can be carried out by calculating a clock frequency at several period intervals, or some other methods basing on the aforementioned principle.

Corresponding to the first embodiment of the electronic detonator clock-calibrating process shown in FIG.22, in the electronic detonator controlling flow, the electronic detonator state-reading-back process in Step N7 can be carried out in accordance with the following steps, as shown in FIG.24:

Step R1, the CPU 285 judging whether to read back the state information of the present detonator according to the detonator identity code included in the state-reading-back instruction: if the detonator identity code in the state-reading-back instruction is corresponding to the identity code read in Step N2, executing Step R2; if not, executing Step R3;

Step R2, the CPU 285 sending the state information of the present detonator to the electronic detonator initiating device 300;

Step R3, ending the present electronic detonator state-reading-back process.

In the electronic detonator state-reading-back process shown in FIG.24, the state-reading-back instruction sent by the electronic detonator initiating device 300 to a certain electronic detonator in the initiating network is a single instruction for the present electronic detonator. The instruction includes the said synchronous studying heads and the said state-reading-back command word in sequence, and the identity code corresponding to the present electronic detonator as well, as shown in FIG.19. The design of the aforementioned process has realized the electronic detonator initiating device's obtainment of the state information of the electronic detonator, which makes the device control the operation of the detonator 400 more reliably. After receiving the state-reading-back instruction, the electronic detonator 400 will judge whether the identity code included in the instruction is corresponding to the identity code of the detonator itself: if the judgement is positive, the electronic detonator will send its state information including the information such as

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whether the clock has been calibrated and whether the delay time has been set to the initiating device 300 to make the initiating device 300 control the operation of the detonator 400 more reliably; if not, the electronic detonator will consider that the initiating device does not intend to obtain the state information of the present detonator 400 and will not perform any execution.

Corresponding to the first embodiment of the electronic detonator clock-calibrating process shown in FIG.22, in the electronic detonator controlling flow mentioned above, the electronic detonator delay-time-writing process in Step N8 can be carried out in accordance with the following steps, as shown in FIG.25:

Step S1, the CPU 285 judging whether to write the delay time for the present detonator according to the detonator identity code included in the delay-time-writing instruction: if the identity code in the delay-time-writing instruction is corresponding to the identity code read in Step N2, continuing with Step S2; if not, ending the present electronic detonator delay-time-writing process;

Step S2, executing the electronic detonator delay-time-data-adjusting process according to the delay time data D_0 in the delay-time-writing instruction, and thus obtaining an adjusted delay time data D_N;

Step S3, writing the adjusted delay time data D_N into the programmable delay module;

Step S4, the CPU 285 setting the delay-time-set state to the delay time setting indication digit at the interior of the CPU 285; and the CPU 285 transmitting the delay-time-writing-completed signal to the electronic detonator initiating device 300;

Step S5, ending the present electronic detonator delay-time-writing process.

In the electronic detonator delay-time-writing process mentioned above shown in FIG.25, the delay-time-writing instruction sent by the electronic detonator initiating device 300 to a certain electronic detonator is corresponding to the instruction sent by the initiating device 300 in Step F6. The instruction is a single instruction for the present electronic detonator, which includes the said synchronous studying heads and the said delay-time-writing command word in sequence, and the identity code corresponding to the present electronic detonator and its delay time data D_0 as well, as shown in FIG.17. After receiving the delay time data D_0 sent by the electronic detonator initiating device 300, the CPU 285 firstly executes the electronic detonator delay-time-data-adjusting process to figure out the new delay time data D_N according to the clock frequency f_D of the present detonator 400 which is the calculation result of the electronic detonator clock-calibrating process shown in FIG.23; then the CPU 285 will write the adjusted delay time data D_N into the programmable delay module 281, which realizes the function of setting the delay time of the electronic detonator 400 on line, thereby improving the flexibility of using the electronic detonator 400. In addition, what is written into the programmable delay module 281 is the adjusted delay time data which is adjusted from the delay time data D_0 sent by the electronic detonator initiating device 300 according to the clock frequency f_D figured out in the electronic detonator clock-calibrating process, which ensures the delay precision of the electronic detonator 400.

The electronic detonator delay-time-data-adjusting flow mentioned above can be carried out in accordance with the following principle: since the delay time data D_0 in the delay-time-writing instruction is calculated according to the predetermined clock frequency (represented as f_0) of the electronic detonator 400, and the time represented by the data D_0 is calculated by the formula D_0/f_0; therefore the delay

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time data D_N which is written into the programmable delay module 281 and is figured out according to the clock frequency f_D that is figured out in the electronic detonator clock-calibrating process should satisfy the following formula: $D_0/f_0=D_N/f_D$. So the adjusted delay time data D_N can be obtained according to the following formula: $D_N=D_0\times f_D/f_0$.

In the electronic detonator controlling flow shown in FIG.20, the second embodiment of the electronic detonator clock-calibrating-process in step N6 can be carried out in accordance with the following steps shown in FIG.23:

Step Q1, setting the value of the variable k which represents the number of the up stream calibrating impulses that are to be sent to be the same as the value of the variable n_D which represents the predetermined number of the up stream calibrating impulses, that is, $k=n_D$;

Step Q2, the CPU 285 judging whether to calibrate the clock of the present detonator according to the detonator identity code included in the second clock-calibrating instruction: if the detonator identity code in the second clock-calibrating instruction is corresponding to the identity code read in Step N2, executing Step Q3; if not, executing Step Q16;

Step Q3, the CPU 285 writing the value of the variable u_D which represents the predetermined high level breadth of the up stream calibrating impulse into the counter 287;

Step Q4, the CPU 285 sending a control signal to the communication interface circuit 203 via the serial communication interface 283 to increase the current on the signal bus 500 consumed by the communication interface circuit 203;

Step Q5, sending a control signal to the counter 287 to start it;

Step Q6, the CPU 285 monitoring whether the predetermined value u_D has been reached: if the judgement is positive, executing Step Q7; if not, continuing monitoring;

Step Q7, sending a control signal to the counter 287 to stop it;

Step Q8, the CPU 285 writing the value of the variable v_D which represents the predetermined low level breadth of the up stream calibrating impulse into the counter 287;

Step Q9, the CPU 285 sending a control signal to the communication interface circuit 203 via the serial communication interface 283 to decrease the current on the signal bus 500 consumed by the communication interface circuit 203;

Step Q10, sending a control signal to the counter 287 to start it;

Step Q11, the CPU 285 monitoring whether the predetermined value v_D has been reached: if the judgement is positive, executing Step Q12; if not, continuing monitoring;

Step Q12, sending a control signal to the counter 287 to stop it;

Step Q13, subtracting 1 from the value of the variable k which represents the number of the up stream calibrating impulses that are to be sent, and rendering the result to be a new value of the variable k, that is, k=k-1;

Step Q14, judging whether the value of the variable k is 0: if the judgement is positive, executing Step Q15; if not, returning to Step Q3;

Step Q15, the CPU 285 setting the calibrated state to the clock-calibrating indication digit in the CPU 285;

Step Q16, ending the present electronic detonator clock-calibrating process.

In the electronic detonator clock-calibrating process mentioned above shown in FIG.23, the clock-calibrating instruction sent by the electronic detonator initiating device 300 to a certain electronic detonator in the initiating network is

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corresponding to the second clock-calibrating instruction sent by the initiating device 300 in Step G5 or Step M5. The present instruction is a single instruction, which includes the said synchronous studying heads and the clock-calibrating command word in sequence, and the identity code corresponding to the present electronic detonator as well, as shown in FIG.18. After receiving the second clock-calibrating instruction, the present detonator 400 will transmit the up stream calibrating waveform to the electronic detonator initiating device 300 according to the predetermined high level breadth u_D, the predetermined low level breadth v_D, and the predetermined period n_D of the up stream calibrating impulse. After receiving the up stream calibrating waveform, the electronic detonator initiating device 300 will calculate the clock frequency f_B of the detonator 400, and then obtain the adjusted new delay time data D_f which should be written into the present detonator according to the clock frequency f_B and the initial delay time data D_0 corresponding to the present detonator. The initiating device 300 can adjust the delay time data of the present detonator immediately after calibrating the clock, and can firstly store the clock frequency f_B and then adjust the delay time data before writing the delay time to the present detonator as well.

The RC oscillator is calibrated on line with the execution of the electronic detonator clock-calibrating process shown in FIG.23. Comparing the embodiment of the electronic detonator clock-calibrating process shown in FIG.23 with the embodiment shown in FIG.22, on the one hand, the CPU 285 in the detonator 400 does not need the function of complicated calculation, thereby the logic design of the chip 200 can be simplified; on the other hand, the adjusting process of the delay time data is executed in the electronic detonator initiating device 300, therefore the delay precision of the electronic detonator 400 can be adjusted flexibly according to the application requirements in the blasting engineering, thereby improving the adaptability of the electronic detonator 400 for different delay precision requirements.

In the aforementioned electronic detonator clock-calibrating process shown in FIG.23, a preferred embodiment lies in: the value of the variable v_D which represents the predetermined low level breadth of the up stream calibrating impulse is higher than the value of the variable u_D which represents the predetermined high level breadth; and the sum of the value of the variable v_D and the value of the variable u_D equals the value of the variable T_D which represents the predetermined period of the up stream calibrating impulse, as shown in FIG.27 and FIG.28. The advantages lie in:

1. The electronic detonator 400 transmits data to the electronic detonator initiating device 300 in the form of current consumption, and when the detonator is transmitting the signal at high level in the up stream calibrating impulse, the consumed current will increase, thus the electronic detonator will consume more energy stored in the electronic detonator initiating device 300. So the energy consumed from the electronic detonator initiating device 300 during the process of clock calibrating can be decreased by decreasing the breadth of the high level signal.

2. When the electronic detonator control chip 200 is sending the high level signal in the up stream calibrating impulse, the input terminal of its rectifier bridge circuit 201 is in the state of short circuit; at this moment, the process of charging the storage unit 600 at the exterior of the electronic detonator control chip 200 will stop, and the digital logic circuit inside the chip 200 will still need to consume the energy in the storage unit 600 for operating. When the electronic detonator control chip is sending the low level signal in the up stream calibrating impulse, the input terminal of the rectifier bridge circuit 201 is in the state of turnoff; and at this moment, the

storage unit 600 at the exterior of the chip can be supplied power continuing. So if the predetermined high level breadth u_D of the calibrating impulse is decreased and the predetermined low level breadth v_D of the calibrating impulse is increased when sending the up stream calibrating waveform, the energy consumed from the storage unit 600 can be decreased and the time for supplying power to the storage unit 600 can be increased, which thereby improves the operating reliability of the electronic detonator control chip 200, decreases the current noises on the bus in the initiating network, and improves the stability of the initiating network.

Corresponding to the embodiment of the electronic detonator clock-calibrating process shown in FIG.23, in the electronic detonator controlling flow mentioned above shown in FIG.20, the electronic detonator delay-time-writing process in Step N8 can be carried out in accordance with the following steps, as shown in FIG.26:

Step T1, the CPU 285 judging whether to write the delay time for the present detonator according to the detonator identity code included in the delay-time-writing instruction: if the detonator identity code in the delay-time-writing instruction is corresponding to the identity code read in Step N2, continuing with Step T2; if not, ending the present electronic detonator delay-time-writing process;

Step T2, the CPU 285 writing the delay time data D_f included in the delay-time-writing instruction into the programmable delay module 281;

Step T3, the CPU 285 setting the delay-time-set state to the delay time setting indication digit at the interior of the CPU 285; and the CPU 285 transmitting the delay-time-writing-completed signal to the electronic detonator initiating device 300;

Step T4, ending the present electronic detonator delay-time-writing process.

Corresponding to the embodiment of the electronic detonator clock-calibrating process shown in FIG.23, since the adjusting process of the delay time data is executed in the electronic detonator initiating device 300, the chip 200 in the present embodiment only needs to write the delay time data D_f included in the delay-time-writing instruction directly into the programmable delay module 281. Therefore there is no need to set an arithmetical logic operation unit in the CPU 285 of the chip 200, which greatly simplifies the design of the chip 200.

In the electronic detonator controlling flow shown in FIG.20, the electronic detonator firing process in Step N9 is similar to the firing process disclosed in Patent Application 200810211374.2. That is, firstly, the CPU 285 sends a control signal to the programmable delay module 281 to start it; secondly, the CPU 285 waits to reach the predetermined delay time, if reaching the delay time, continuing with the next step, if not, continuing waiting; thirdly, the programmable delay module 281 outputs a single to the firing control circuit 202 to close it and render it in a firing state. Then the igniting of the detonator 400 is accomplished.

CLAIMS

1. An initiating device delay-time-setting flow in an electronic detonator initiating system which is comprised of an initiating device and at least one electronic detonator, at least one said electronic detonator is connected in parallel between the signal bus extending from the initiating device, the initiating device includes a control module, a man-machine interacting module, a power supply management module, a signal modulating and transmitting module, a signal demodulating and receiving module and a power supply, and the control module further includes a first CPU and a timer, wherein:

the initiating device delay-time-setting flow is carried out in accordance with the following steps:

Step A1, executing an initiating device clock-calibrating flow;

Step A2, executing an initiating device delay-time-writing flow;

Step A3, outputting an error information list to the man-machine interacting module for displaying; and

Step A4, ending the present initiating device delay-time-setting flow;

wherein

Step A1 is carried out in accordance with the following steps:

Step B1, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E1 which represents the number of the electronic detonators which contain errors in the process of clock-calibrating, and the cycle number W1 into the cache of the control module; wherein the value of the variable E1 is equal to the value of the number N;

Step B2, the control module judging whether the value of the cycle number W1 and the variable E1 is 0: if the value of the cycle number W1 or the value of the variable E1 is 0, ending the present initiating device clock-calibrating flow; if not, continuing with Step B3;

Step B3, executing an initiating device clock-calibrating process; and

Step B4, subtracting 1 from the value of the cycle number W1, and rendering the result to be a new value of the cycle number W1, that is, W1=W1-1; then returning to Step B2.

2. The initiating device delay-time-setting flow according to claim 1, wherein:

Step B3 is carried out in accordance with the following steps:

Step C1, the control module transmitting a first clock-calibrating instruction to all the electronic detonators in the initiating network;

Step C2, the control module waiting for a time T_0 which represents a predetermined delay: if reaching the time, executing Step C3; if not, continuing waiting;

Step C3, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1, that is, $L=E_1$;

Step C4, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step C5, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step C6, judging whether the present electronic detonator is in the calibrated state according to the state information of the detonator: if the judgement is positive,

executing Step C13; if not, executing Step C7;

Step C7, transmitting a state-reading-back instruction to the present electronic detonator;

Step C8, the control module executing a signal receiving process: if receiving the information returned by the present electronic detonator, executing Step C9; if not, executing Step C12;

Step C9, the control module storing the information returned by the present electronic detonator, and judging whether the clock-calibrating indication digit of the electronic detonator is in the calibrated state: if the judgement is positive, executing Step C10; if not, executing Step C12;

Step C10, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator;

Step C11, subtracting 1 from the value of the variable E_1, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$; then continuing with Step C13;

Step C12, setting the clock-calibrating error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator; and then executing Step C13;

Step C13, subtracting 1 from the value of the variable L, and rendering the result to be a new value of the variable L, that is, L=L-1;

Step C14, judging whether the value of the variable L is 0: if the judgement is positive, continuing with Step C15; if not, returning to Step C4;

Step C15, ending the present initiating device clock-calibrating process.

3. The initiating device delay-time-setting flow according to claim 2, wherein:

the first clock-calibrating instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the clock-calibrating command word, and a down stream calibrating waveform; and

the down stream calibrating waveform consists of a string of down stream calibrating impulses, the period of which is a predetermined period T_B and the sum of which is a predetermined number n_B.

4. The initiating device delay-time-setting flow according to claim 3, wherein:

the down stream calibrating waveform is transmitted by the control module executing an initiating device calibrating-waveform-transmitting flow as follows:

Step D1, setting the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted to be the same as the value of the variable n_B which represents the predetermined number of the down stream calibrating impulses, that is, $n=n_B$;

Step D2, writing the value of the variable v_B which represents the predetermined low level breadth of the down stream calibrating impulse into the timer;

Step D3, transmitting a control signal to the signal modulating and transmitting module to render it output a down edge signal;

Step D4, transmitting a control signal to the timer to start it;

Step D5, the first CPU monitoring whether the length of the low level signal output by the signal modulating and transmitting module has reached the predetermined low level breadth v_B: if the judgement is positive, executing Step D6;

if not, continuing monitoring;

Step D6, transmitting a control signal to the timer to stop it;

Step D7, writing the value of the variable u_B which represents the predetermined high level breadth of the down stream calibrating impulse into the timer;

Step D8, transmitting a control signal to the signal modulating and transmitting module to render it output an up edge signal;

Step D9, transmitting a control signal to the timer to start it;

Step D10, the first CPU monitoring whether the length of the high level signal output by the signal modulating and transmitting module has reached the predetermined high level breadth u_B: if the judgement is positive, executing Step D11; if not, continuing monitoring;

Step D11, transmitting a control signal to the timer to stop it;

Step D12, subtracting 1 from the value of the variable n which represents the number of the down stream calibrating impulses that are to be transmitted, and rendering the result to be a new value of the variable n, that is, n=n-1;

Step D13, judging whether the value of the variable n is 0: if the judgement is positive, executing Step D14; if not, returning to Step D2;

Step D14, ending the present initiating device calibrating-waveform-transmitting flow.

5. The initiating device delay-time-setting flow according to claim 4, wherein:

the value of the predetermined high level breadth u_B is higher than the value of the predetermined low level breadth v_B; and

the sum of the value of the variable u_B and the value of the variable v_B equals the value of the predetermined period T_B.

6. The initiating device delay-time-setting flow according to any one of claims 2 to 5, wherein:

the state-reading-back instruction consists of three parts in sequence which are respectively the synchronous studying heads, sum of which is a predetermined number m, the state-reading-back command word, and the identity code of a certain electronic detonator.

7. The initiating device delay-time-setting flow according to any one of the preceding claims, wherein:

Step B3 is carried out in accordance with the following steps:

Step G1, setting the value of the variable L which represents the number of electronic detonators that are to be calibrated to be the same as the value of the variable E_1 which represents the number of the electronic detonators that contain errors in the process of clock-calibrating, that is, $L=E_1$;

Step G2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step G3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step G4, judging whether the present electronic detonator is in the calibrated state according to the state information of the present detonator: if the judgement is positive, executing Step G12; if not, executing Step G5;

Step G5, transmitting a second clock-calibrating instruction to the present electronic detonator;

Step G6, the control module executing the signal receiving process: if receiving the up stream calibrating waveform returned by the present electronic detonator, executing Step G7; if not, setting the clock-calibrating error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator, then executing Step G12;

Step G7, setting the clock-calibrating succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator;

Step G8, subtracting 1 from the value of the variable E_1, and rendering the result to be a new value of the variable E_1, that is, $E_1=E_1-1$;

Step G9, counting the up stream calibrating waveform consisting of a string of up stream calibrating impulses, the period of which is a predetermined period T_D and the sum of which is a predetermined number n_D; representing the counting result as a value F_B;

Step G10, calculating the clock frequency f_B of the present electronic detonator according to the value of the variable n_D, the variable T_D and the variable F_B;

Step G11, storing the clock information of the present electronic detonator and the clock information includes the value of the clock frequency f_B;

Step G12, subtracting 1 from the value of the variable L, and rendering the result to be a new value of the variable L, that is, L=L-1;

Step G13, judging whether the value of the variable L is 0: if the judgement is positive, continuing with Step G14; if not, returning to Step G2;

Step G14, ending the present initiating device clock-calibrating process.

8. The initiating device delay-time-setting flow according to any one of the preceding claims, wherein:

Step A2 is carried out in accordance with the following steps:

Step E1, storing the initial values of the following variables which are respectively the number N which represents the sum of the electronic detonators in the initiating network, the variable E_2 which represents the number of the electronic detonators which contain errors in the process of delay-time-writing, and the cycle number W_2 into the cache of the control module; wherein the value of the variable E_2 is equal to the value of the number N;

Step E2, the control module judging whether the value of the cycle number W_2 and the value of the variable E_2 is 0: if the value of the cycle number W_2 or the value of the variable E_2 is 0, executing Step E5; if not, continuing with Step E3;

Step E3, executing an initiating device delay-time-writing process;

Step E4, subtracting 1 from the value of the cycle number W_2, and rendering the result to be a new value of the cycle number W_2, that is, $W_2=W_2-1$; then returning to Step E2;

Step E5, ending the present initiating device delay-time-writing flow.

9. The initiating device delay-time-setting flow according to claim 8, wherein:

Step E3 is carried out in accordance with the following steps:

Step F1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step F2, reading the identity code stored in the initiating device corresponding

to a certain electronic detonator in the initiating network;

Step F3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step F4, judging whether the present electronic detonator is in the calibrated state according to the state information of the detonator: if the judgement is negative, executing Step F8; if the judgement is positive, executing Step F5;

Step F5, reading the value D_0 of the delay time data stored in the initiating device corresponding to the present electronic detonator;

Step F6, transmitting a delay-time-writing instruction including the value D_0 of the delay time data to the present electronic detonator;

Step F7, the control module executing a signal receiving process:

if receiving the delay-time-writing-completed signal returned by the present electronic detonator, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator; and then subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator;

Step F8, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, $R=R-1$;

Step F9, judging whether the value of the variable R is 0: if the judgement is positive, executing Step F10; if not, returning to Step F2;

Step F10, ending the present initiating device delay-time-writing process.

10. The initiating device delay-time-setting flow according to claim 8, wherein:

Step E3 is carried out in accordance with the following steps,

Step H1, setting the value of the variable R which represents the number of electronic detonators that are to be written the delay time to be the same as the value of the variable E_2 which represents the number of electronic detonators that contain errors in the process of delay-time-writing, that is, $R=E_2$;

Step H2, reading the identity code stored in the initiating device corresponding to a certain electronic detonator in the initiating network;

Step H3, reading the state information stored in the initiating device corresponding to the present electronic detonator;

Step H4, judging whether the present electronic detonator is in the calibrated state according to the state information of the present detonator: if the judgement is negative, executing Step H9; if the judgement is positive, executing Step H5;

Step H5, reading the value D_0 of the delay time data stored in the initiating device corresponding to the present electronic detonator; and reading the value of the clock frequency f_B stored in the control module corresponding to the present electronic detonator;

Step H6, executing an initiating device delay-time-data-adjusting flow, to figure out a new value D_f of the delay time data according to the value of the clock frequency f_B;

Step H7, transmitting a delay-time-writing instruction including the variable D_f to the present electronic detonator;

Step H8, the control module executing the signal receiving process:

if receiving the delay-time-writing-completed signal returned by the present electronic detonator, the control module will set the delay-time-writing-succeeded indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator; and then subtracting 1 from the value of the variable E_2, and rendering the result to be a new value of the variable E_2, that is, $E_2=E_2-1$;

if not, the control module will set the delay-time-writing-error indication to the state information which is stored in the initiating device and is corresponding to the present electronic detonator;

Step H9, subtracting 1 from the value of the variable R, and rendering the result to be a new value of the variable R, that is, R=R-1;

Step H10, judging whether the value of the variable R is 0: if the judgement is positive, executing Step H11; if not, returning to Step H2;

Step H11, ending the present initiating device delay-time-writing process.

11. An initiating device delay-time-setting flow in an electronic detonator initiating system substantially as hereinbefore described with reference to the accompanying drawings.

DRAWINGS

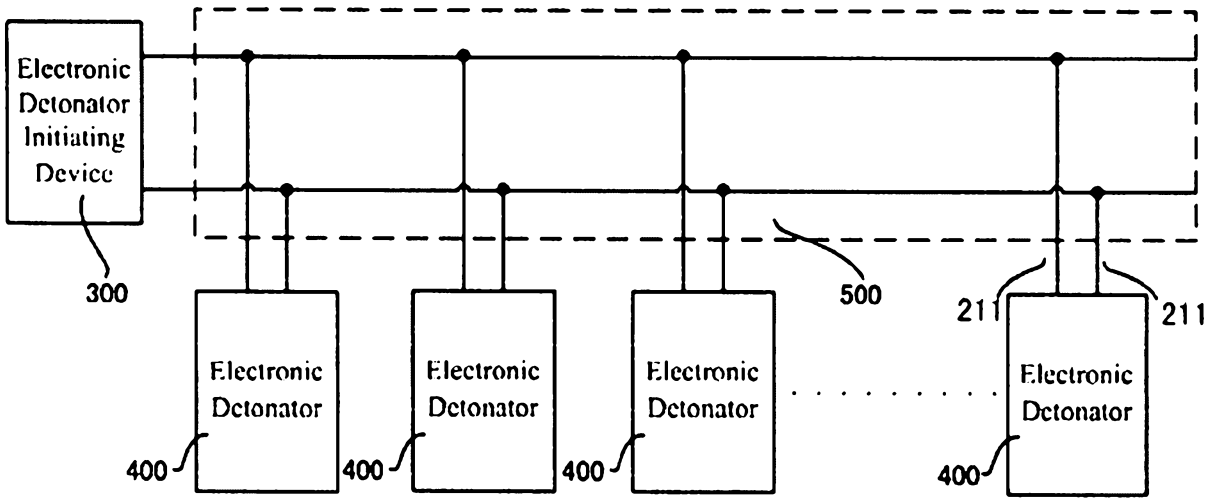

FIG.1

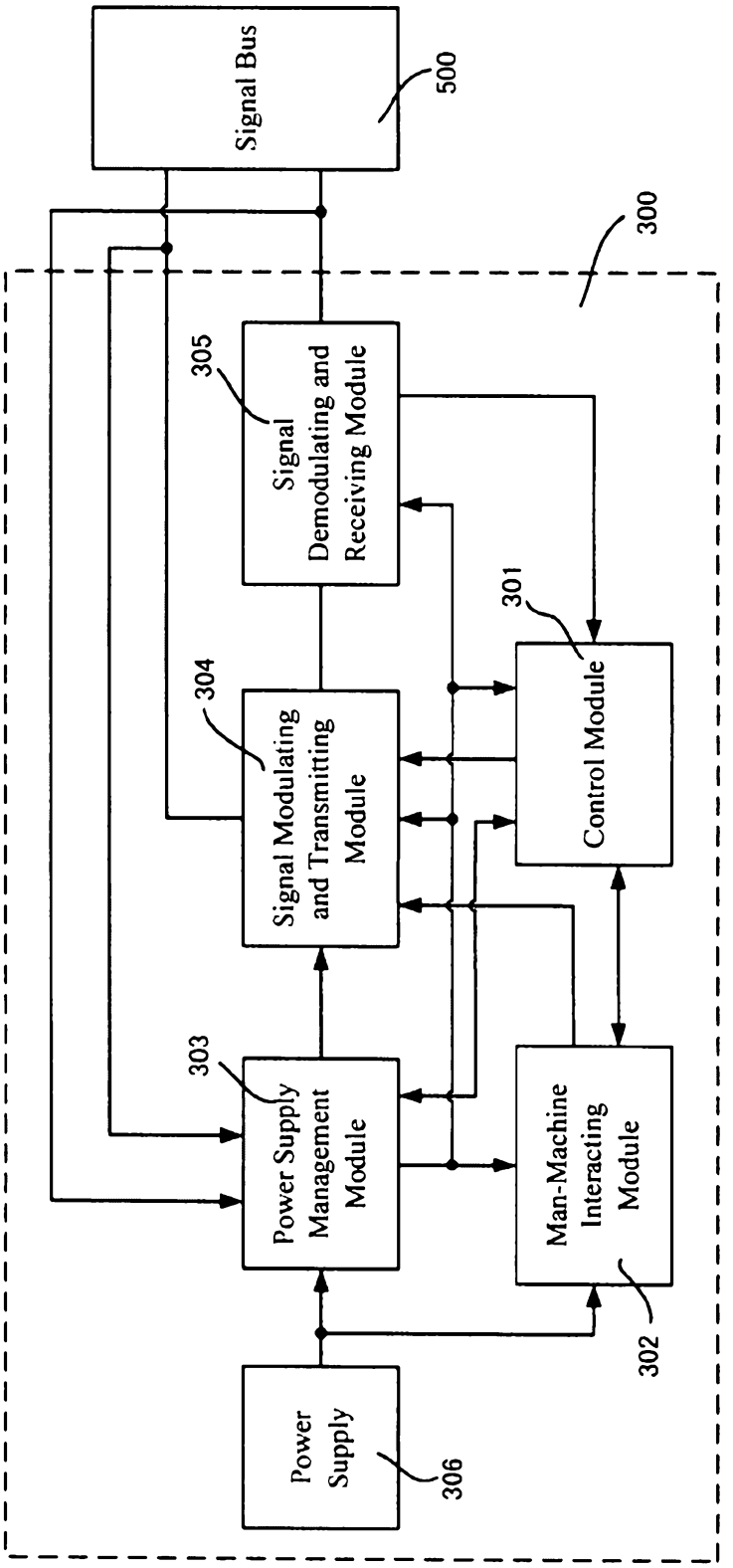
Signal Bus
500
300
305
Signal Demodulating and Receiving Module
301
Control Module
304
Signal Modulating and Transmitting Module
303
Power Supply Management Module
Man-Machine Interacting Module
302
Power Supply
306

FIG.2

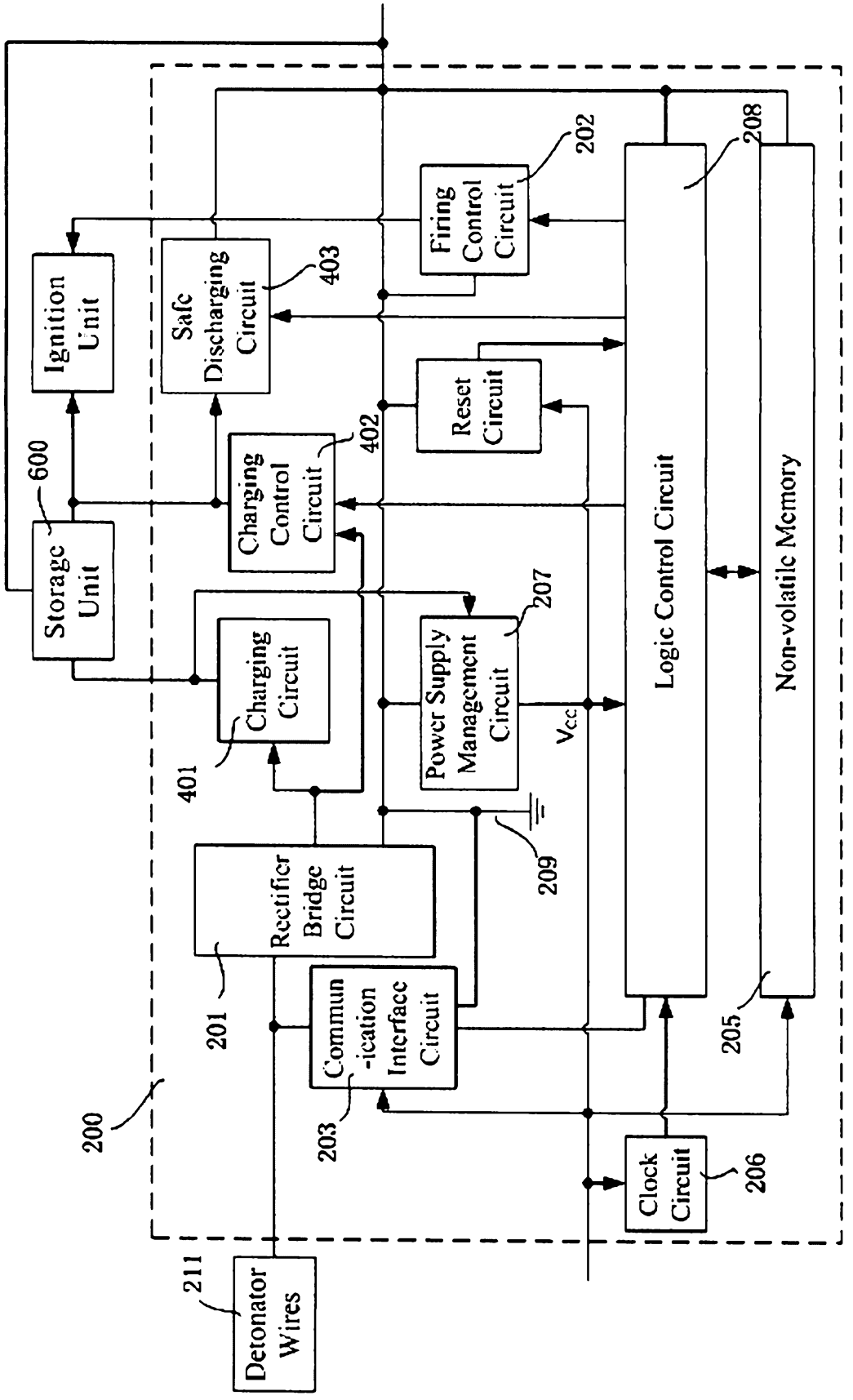
Ignition Unit
Safe Discharging Circuit
403
Firing Control Circuit
202
208
600
Storage Unit
Charging Control Circuit
402
Reset Circuit
Logic Control Circuit
Non-volatile Memory
Charging Circuit
401
Power Supply Management Circuit
207
Vcc
209
Rectifier Bridge Circuit
201
Commun-ication Interface Circuit
203
200
205
Clock Circuit
206
211
Detonator Wires

FIG.3

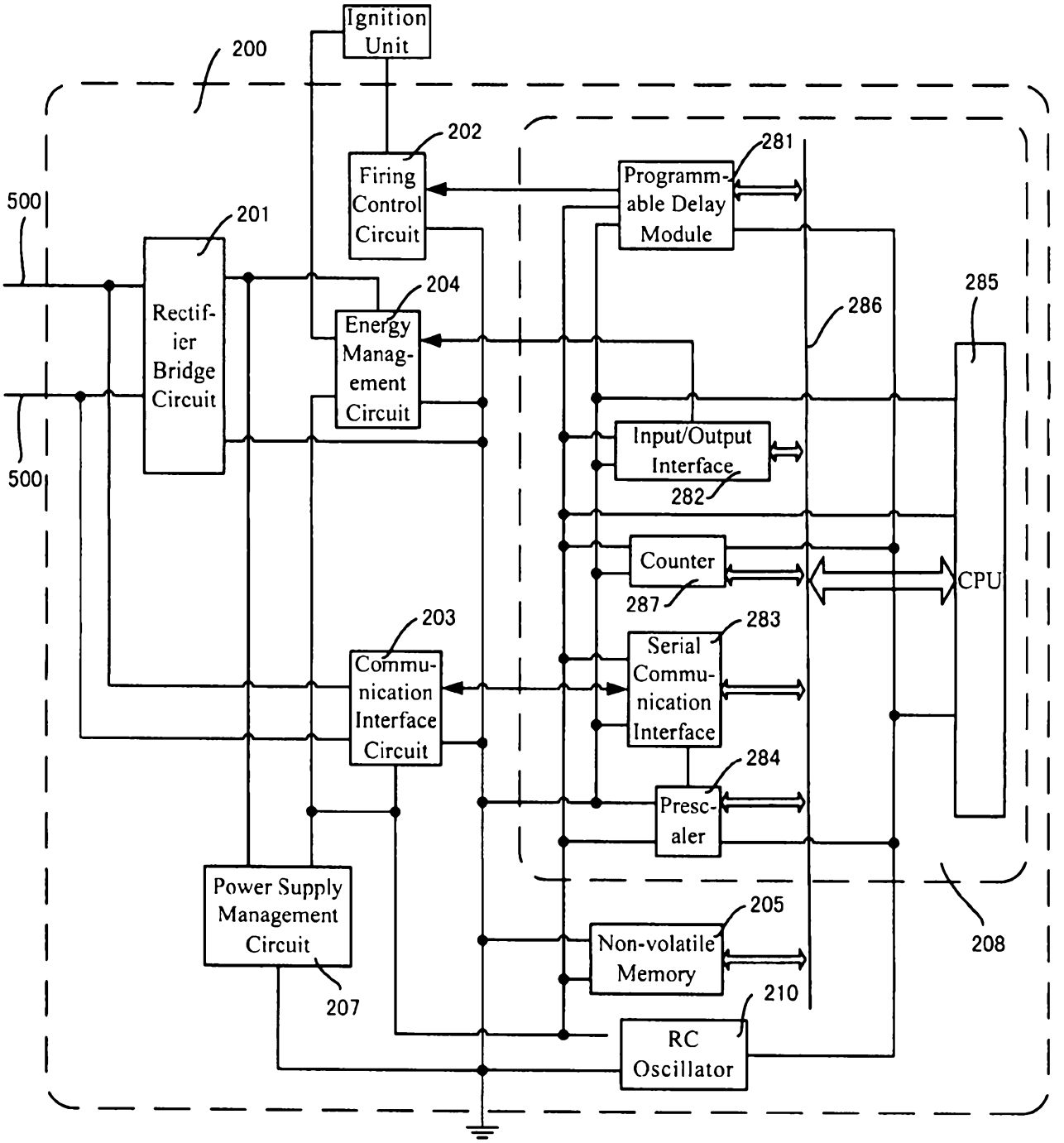
Ignition Unit
200
202
281
Firing Control Circuit
Programm-able Delay Module
500
201
Rectif-ier Bridge Circuit
204
Energy Manag-ement Circuit
285
286
Input/Output Interface
282
500
Counter
287
CPU
203
283
Commu-nication Interface Circuit
Serial Commu-nication Interface
284
Presc-aler
Power Supply Management Circuit
205
Non-volatile Memory
208
207
210
RC Oscillator

FIG.4

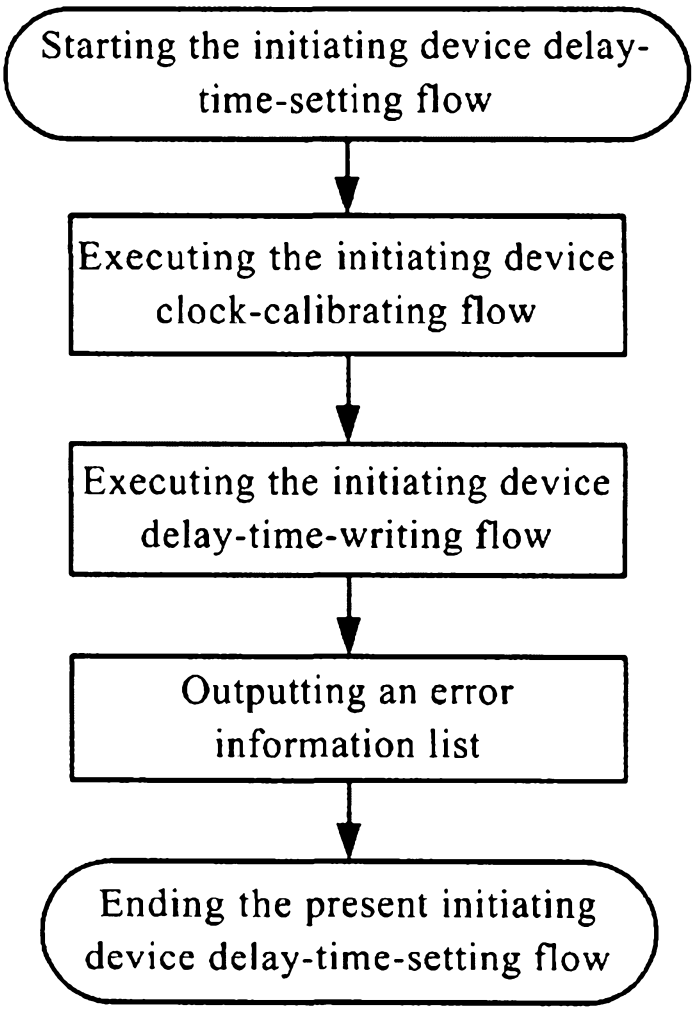
Starting the initiating device delay-time-setting flow
Executing the initiating device clock-calibrating flow
Executing the initiating device delay-time-writing flow
Outputting an error information list
Ending the present initiating device delay-time-setting flow

FIG.5

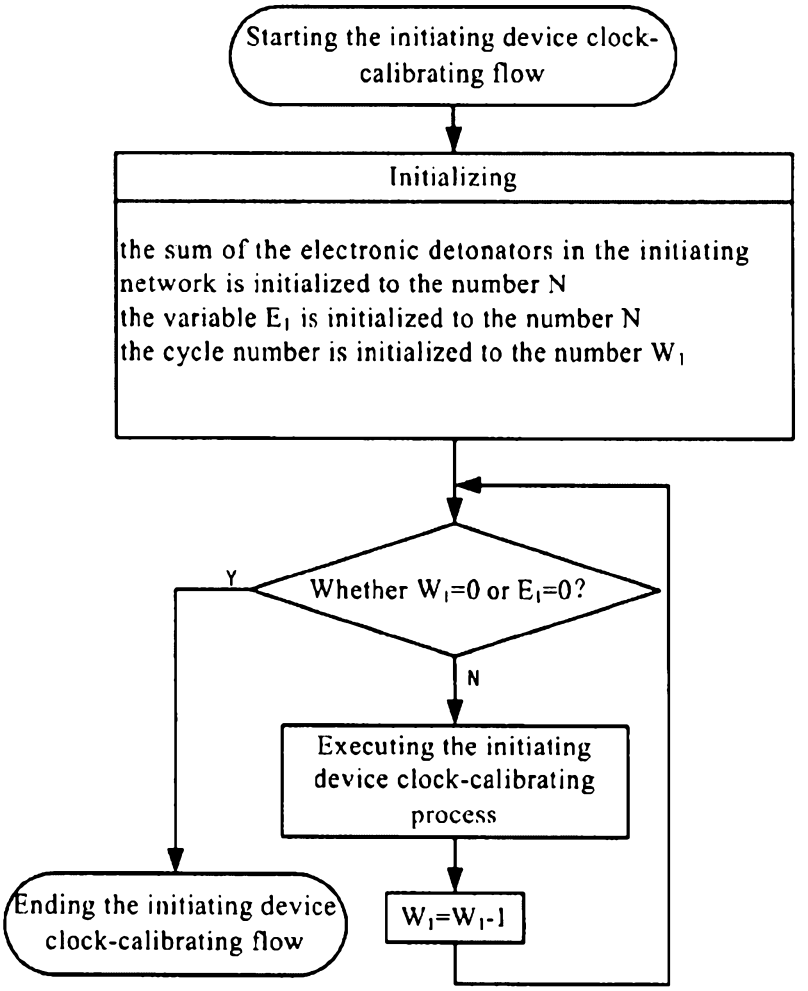
Starting the initiating device clock-calibrating flow
Initializing
the sum of the electronic detonators in the initiating network is initialized to the number N
the variable E_1 is initialized to the number N
the cycle number is initialized to the number W_1
Whether W_1=0 or E_1=0?
Y
N
Executing the initiating device clock-calibrating process
W_1=W_1-1
Ending the initiating device clock-calibrating flow

FIG.6

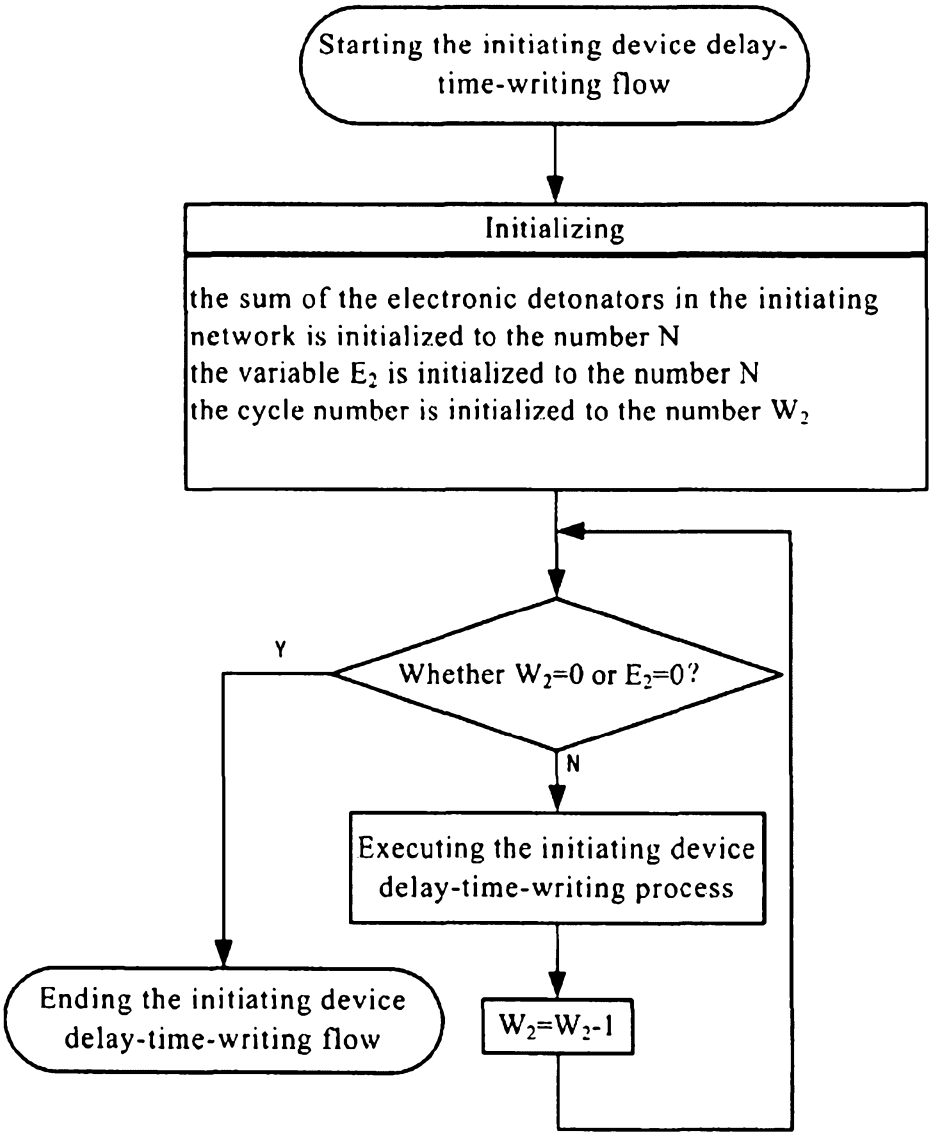
Starting the initiating device delay-time-writing flow
Initializing
the sum of the electronic detonators in the initiating network is initialized to the number N
the variable E_2 is initialized to the number N
the cycle number is initialized to the number W_2
Whether W_2=0 or E_2=0?
Y
N
Executing the initiating device delay-time-writing process
W_2=W_2-1
Ending the initiating device delay-time-writing flow

FIG.7

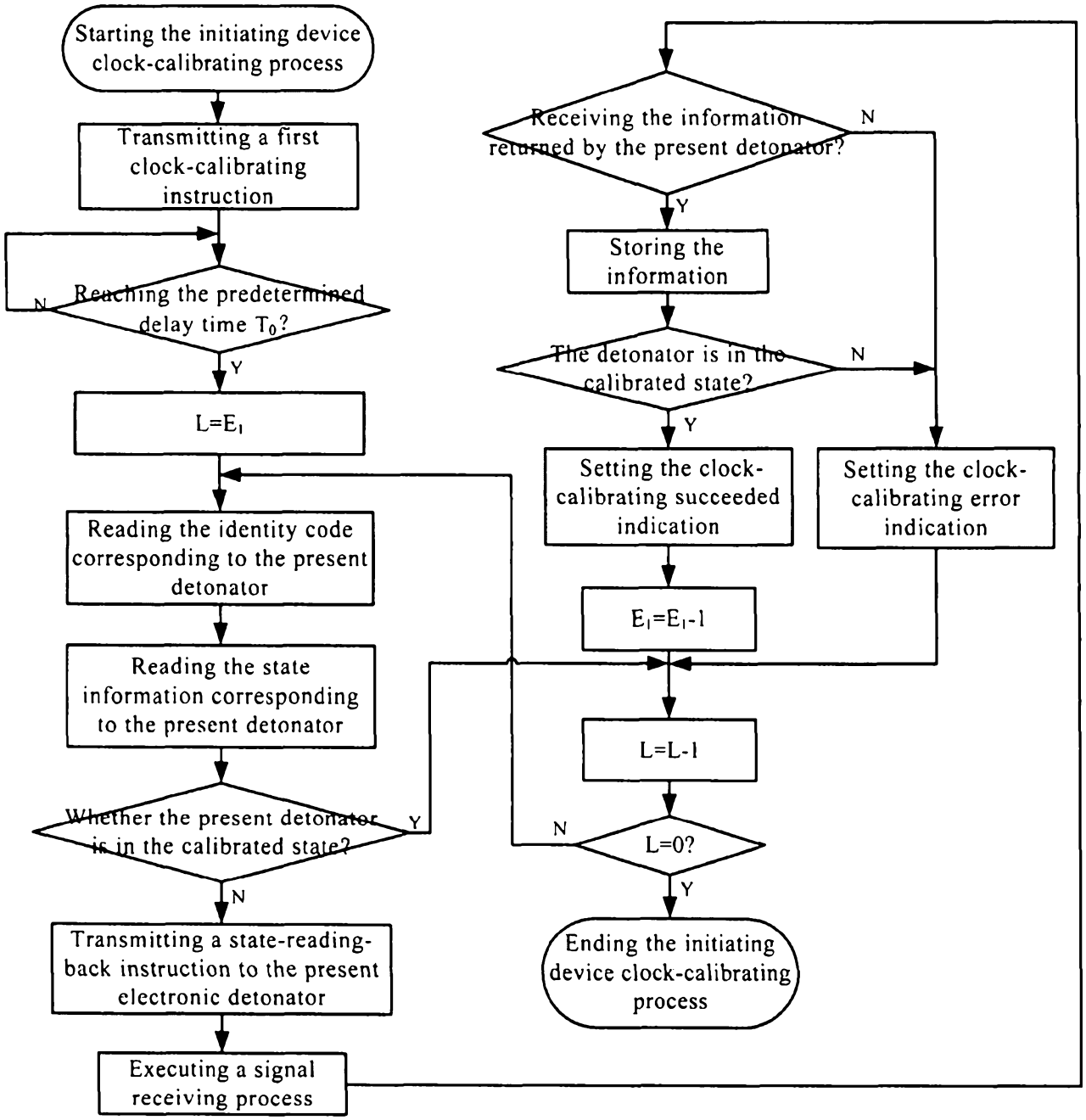
Starting the initiating device clock-calibrating process
Transmitting a first clock-calibrating instruction
Reaching the predetermined delay time T_0?
N
Y
$L=E_1$
Reading the identity code corresponding to the present detonator
Reading the state information corresponding to the present detonator
Whether the present detonator is in the calibrated state?
Y
N
Transmitting a state-reading-back instruction to the present electronic detonator
Executing a signal receiving process
Receiving the information returned by the present detonator?
N
Y
Storing the information
The detonator is in the calibrated state?
N
Y
Setting the clock-calibrating succeeded indication
Setting the clock-calibrating error indication
$E_1=E_1-1$
$L=L-1$
$L=0$?
N
Y
Ending the initiating device clock-calibrating process

FIG.8

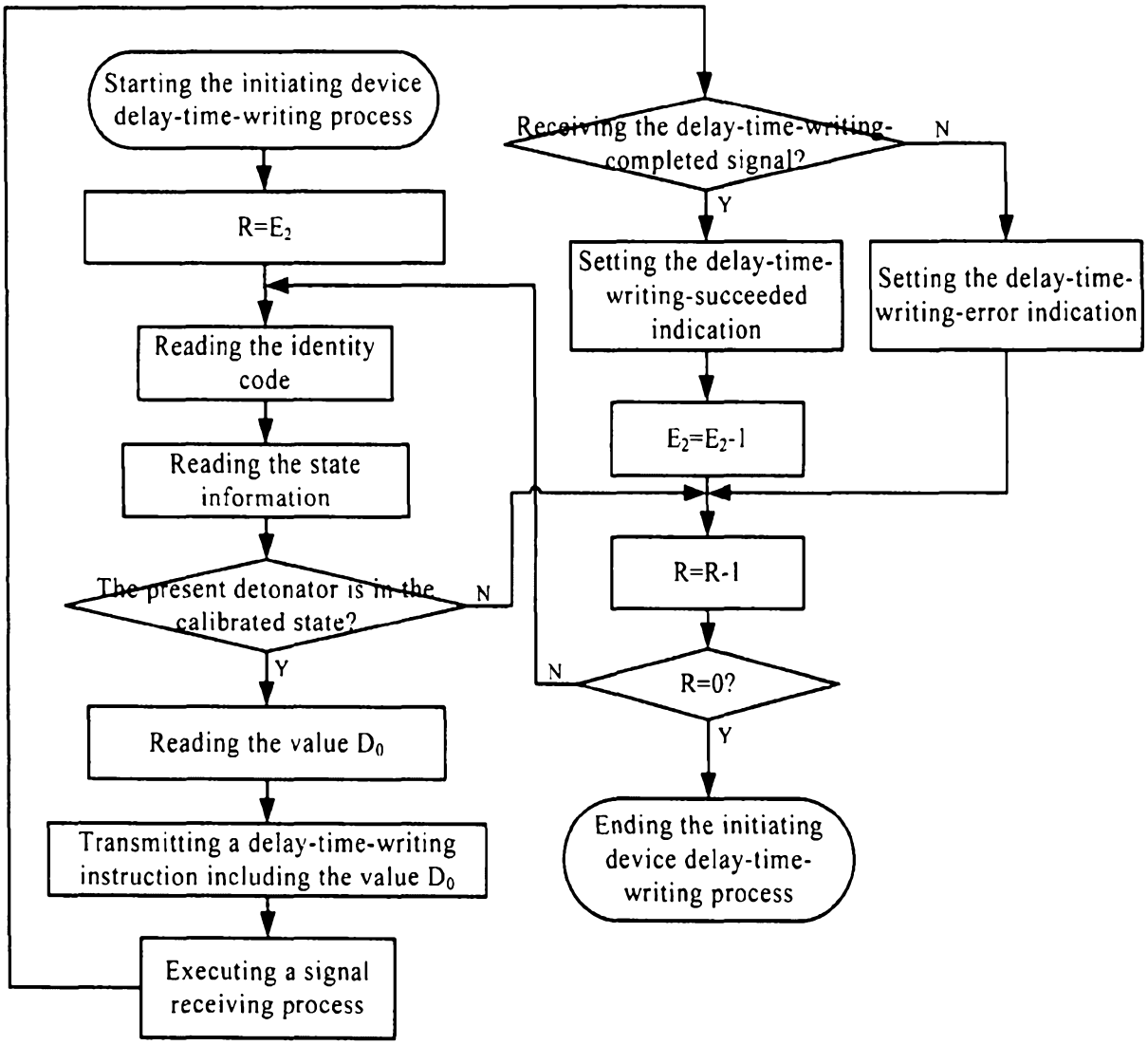
Starting the initiating device delay-time-writing process
R=E2
Reading the identity code
Reading the state information
The present detonator is in the calibrated state?
N
Y
Reading the value D0
Transmitting a delay-time-writing instruction including the value D0
Executing a signal receiving process
Receiving the delay-time-writing-completed signal?
N
Y
Setting the delay-time-writing-succeeded indication
Setting the delay-time-writing-error indication
E2=E2-1
R=R-1
N
R=0?
Y
Ending the initiating device delay-time-writing process

FIG.9

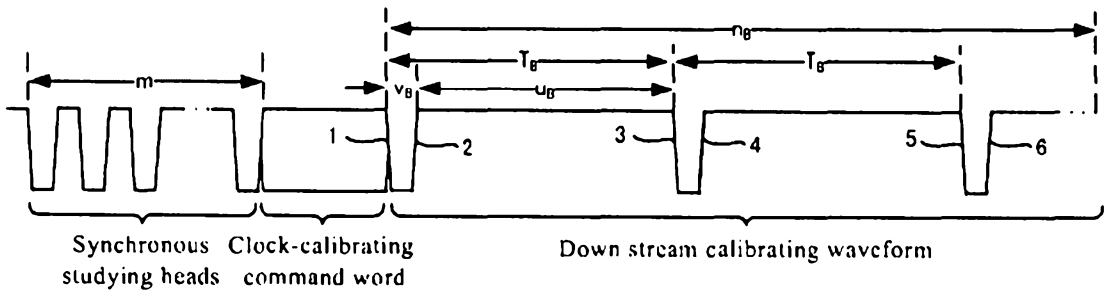
m
nB
TB
TB
vB
uB
1
2
3
4
5
6
Synchronous studying heads
Clock-calibrating command word
Down stream calibrating waveform

FIG.10

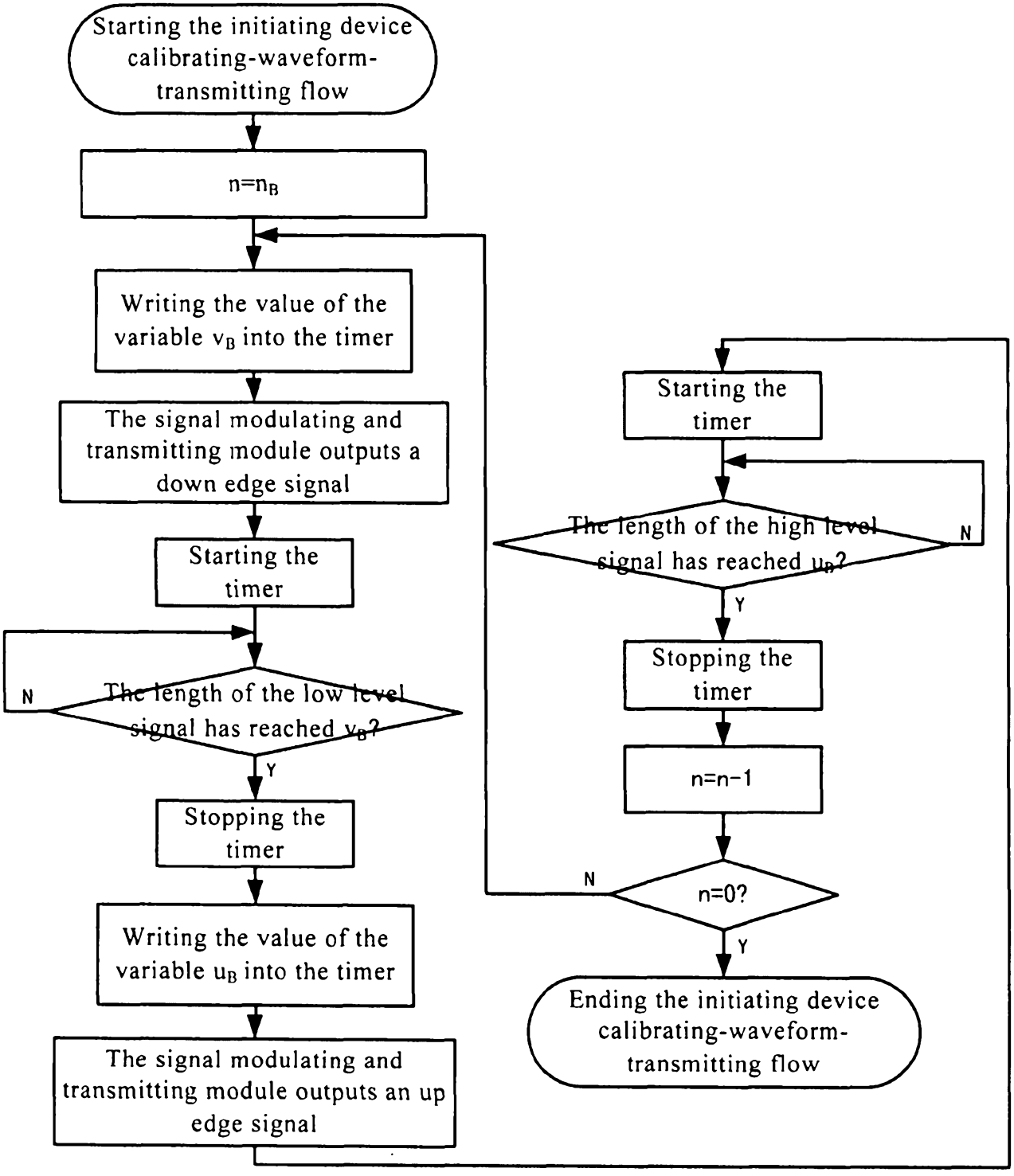
Starting the initiating device calibrating-waveform-transmitting flow
n=n_B
Writing the value of the variable v_B into the timer
The signal modulating and transmitting module outputs a down edge signal
Starting the timer
N
The length of the low level signal has reached v_B?
Y
Stopping the timer
Writing the value of the variable u_B into the timer
The signal modulating and transmitting module outputs an up edge signal
Starting the timer
The length of the high level signal has reached u_B?
N
Y
Stopping the timer
n=n-1
N
n=0?
Y
Ending the initiating device calibrating-waveform-transmitting flow

FIG.11

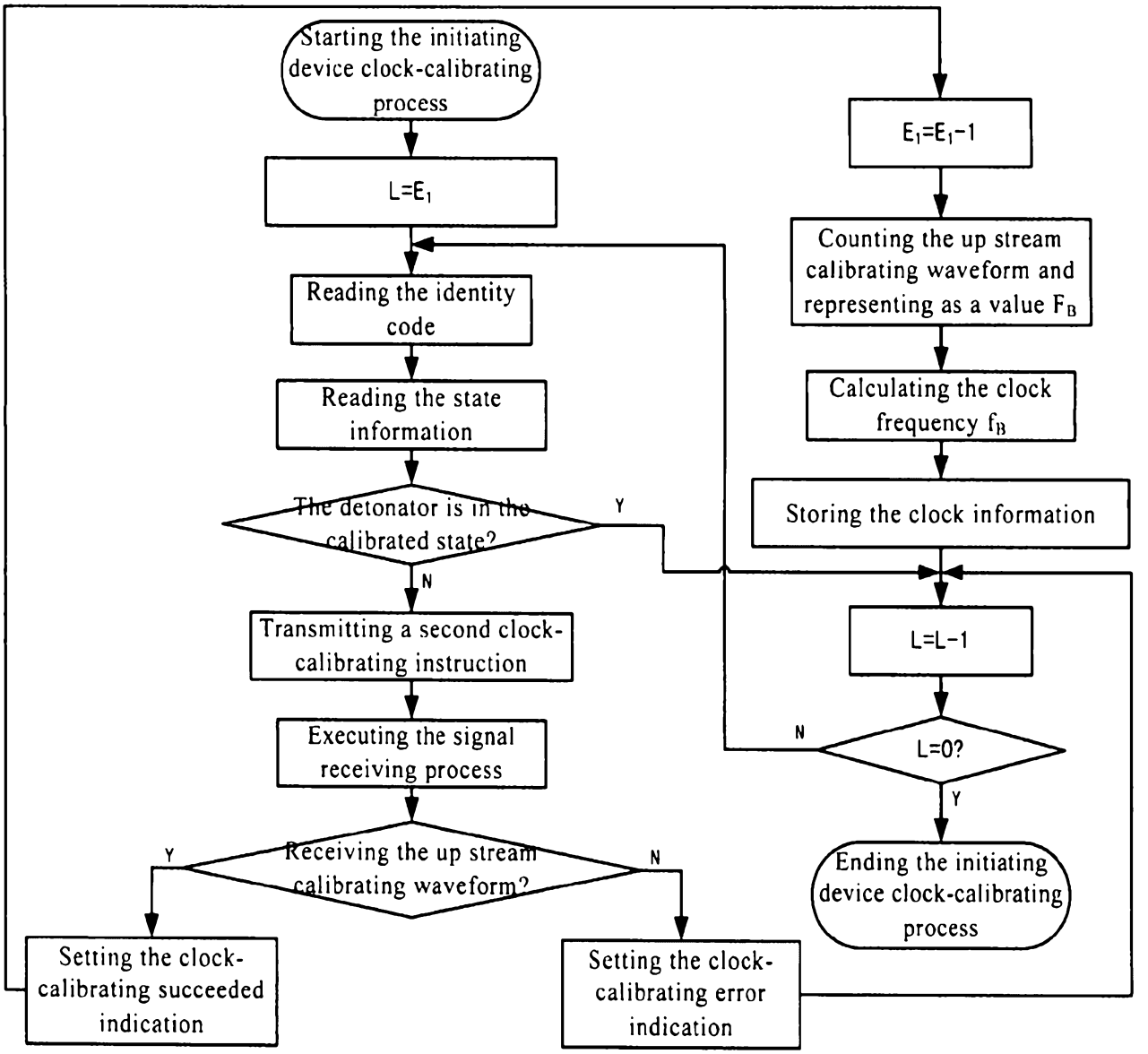
Starting the initiating device clock-calibrating process
L=E1
Reading the identity code
Reading the state information
The detonator is in the calibrated state?
Y
N
Transmitting a second clock-calibrating instruction
Executing the signal receiving process
Receiving the up stream calibrating waveform?
Y
N
Setting the clock-calibrating succeeded indication
Setting the clock-calibrating error indication
E1=E1-1
Counting the up stream calibrating waveform and representing as a value FB
Calculating the clock frequency fB
Storing the clock information
L=L-1
L=0?
N
Y
Ending the initiating device clock-calibrating process

FIG.12

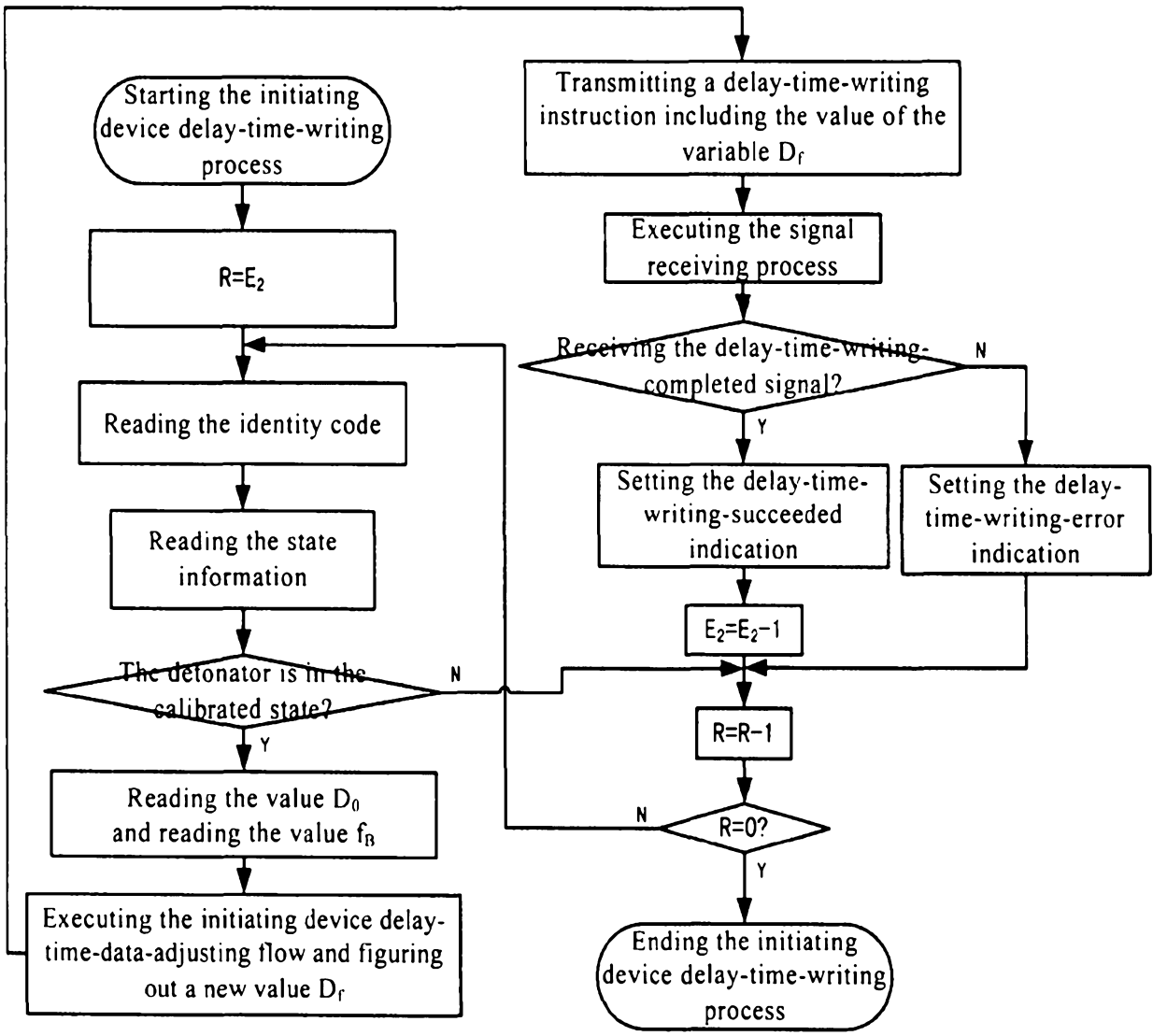
Starting the initiating device delay-time-writing process
R=E2
Reading the identity code
Reading the state information
The detonator is in the calibrated state?
N
Y
Reading the value D0 and reading the value fB
Executing the initiating device delay-time-data-adjusting flow and figuring out a new value Df
Transmitting a delay-time-writing instruction including the value of the variable Df
Executing the signal receiving process
Receiving the delay-time-writing-completed signal?
N
Y
Setting the delay-time-writing-succeeded indication
Setting the delay-time-writing-error indication
E2=E2-1
R=R-1
N
R=0?
Y
Ending the initiating device delay-time-writing process

FIG.13

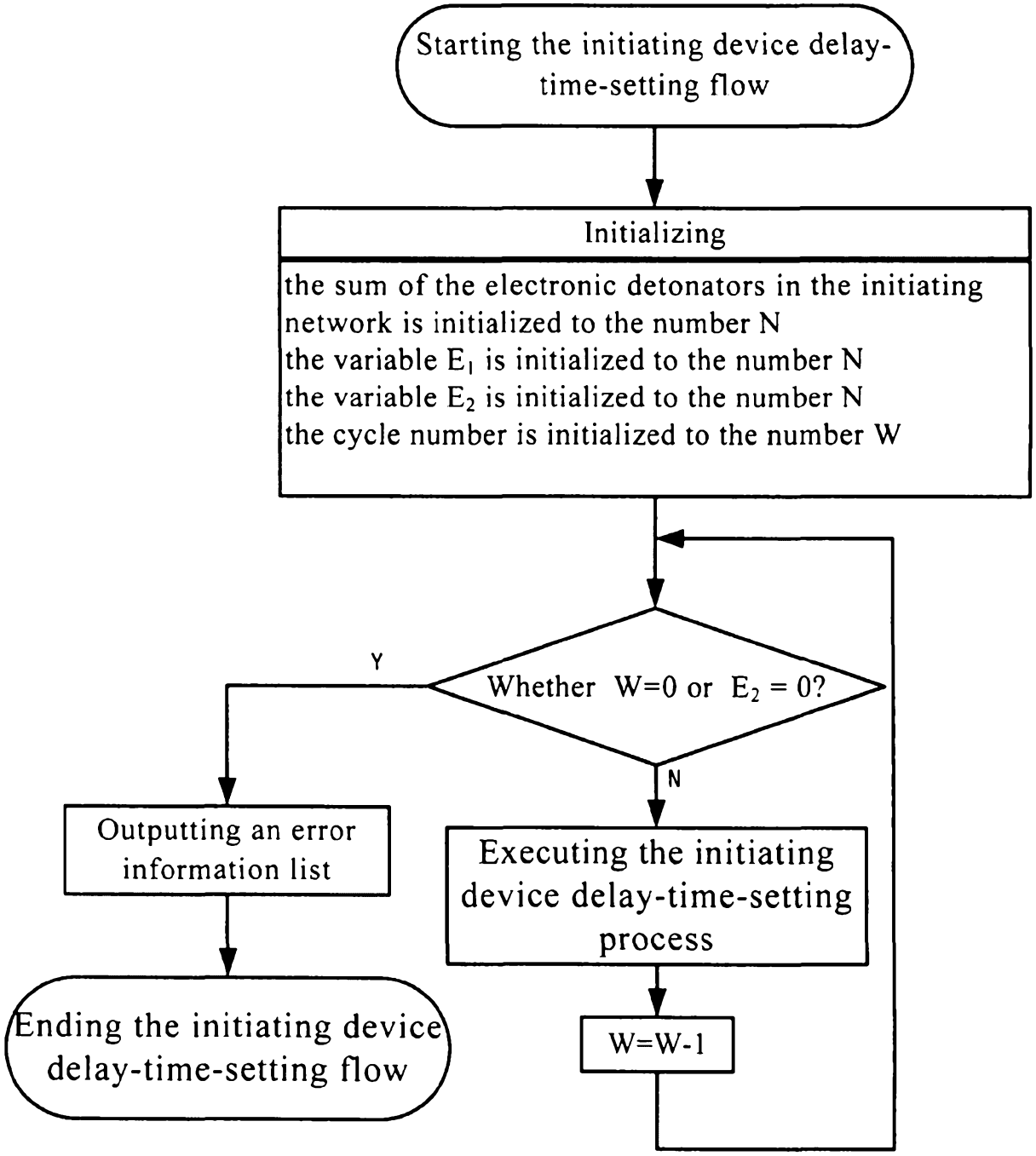
Starting the initiating device delay-time-setting flow
Initializing
the sum of the electronic detonators in the initiating network is initialized to the number N
the variable E_1 is initialized to the number N
the variable E_2 is initialized to the number N
the cycle number is initialized to the number W
Whether W=0 or E_2 = 0?
Y
N
Outputting an error information list
Executing the initiating device delay-time-setting process
Ending the initiating device delay-time-setting flow
W=W-1

FIG.14

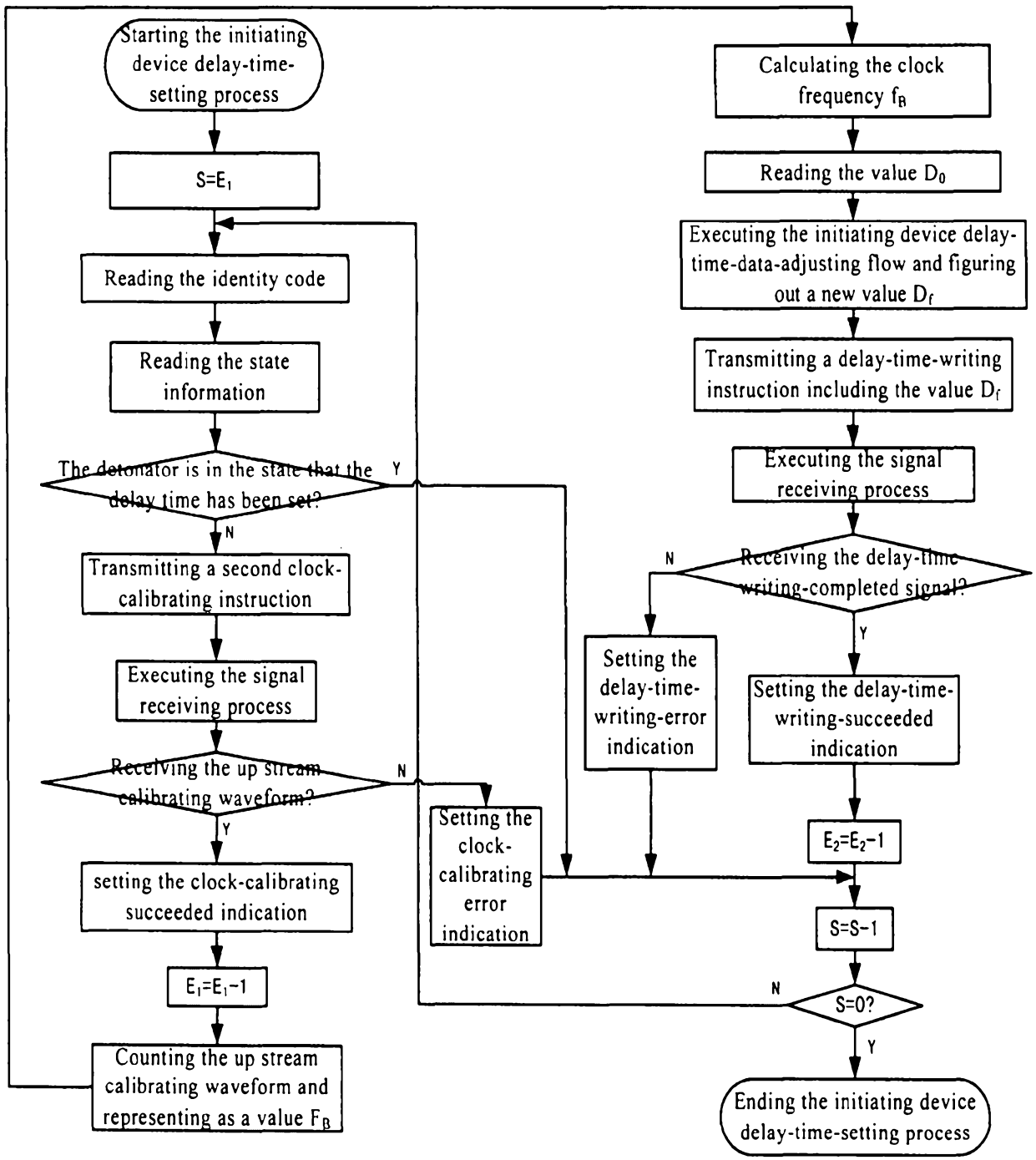
Starting the initiating device delay-time-setting process
S=E1
Reading the identity code
Reading the state information
The detonator is in the state that the delay time has been set?
Y
N
Transmitting a second clock-calibrating instruction
Executing the signal receiving process
Receiving the up stream calibrating waveform?
N
Y
setting the clock-calibrating succeeded indication
E1=E1-1
Counting the up stream calibrating waveform and representing as a value FB
Setting the clock-calibrating error indication
Calculating the clock frequency fB
Reading the value D0
Executing the initiating device delay-time-data-adjusting flow and figuring out a new value Df
Transmitting a delay-time-writing instruction including the value Df
Executing the signal receiving process
N
Receiving the delay-time writing-completed signal?
Y
Setting the delay-time-writing-error indication
Setting the delay-time-writing-succeeded indication
E2=E2-1
S=S-1
N
S=0?
Y
Ending the initiating device delay-time-setting process

FIG.15

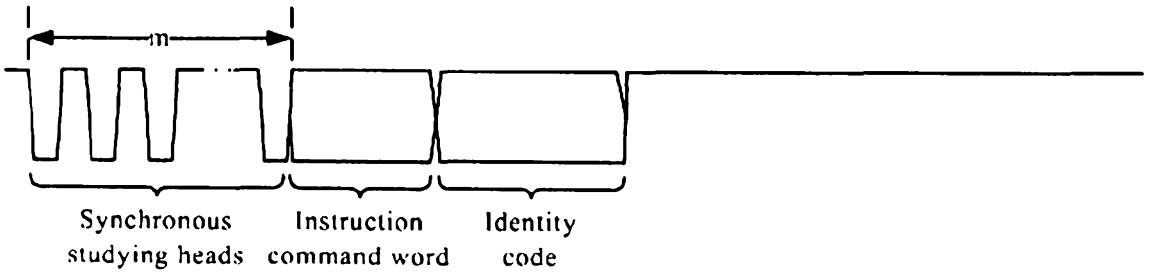
n
Synchronous studying heads
Instruction command word
Identity code

FIG.16

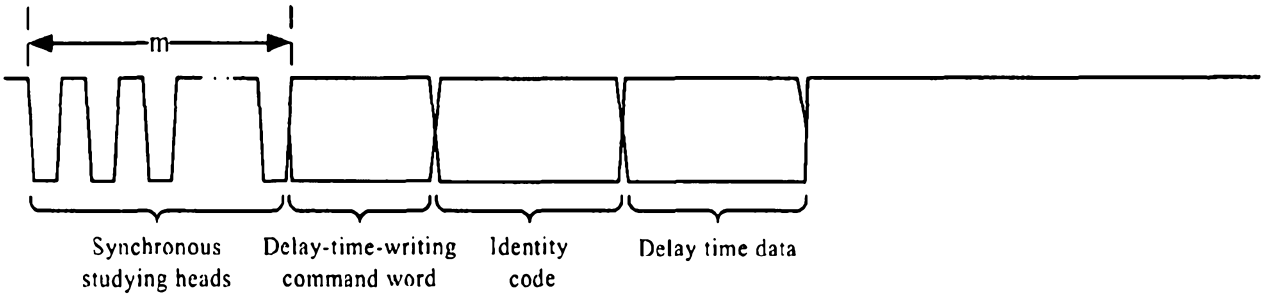

FIG.17

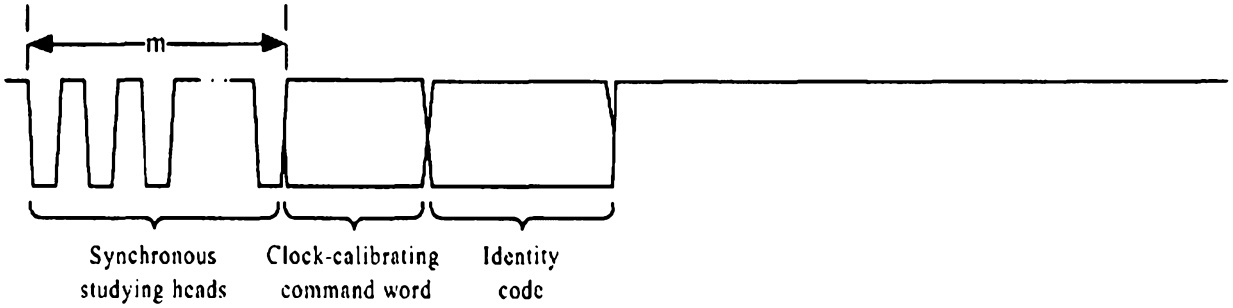

FIG.18

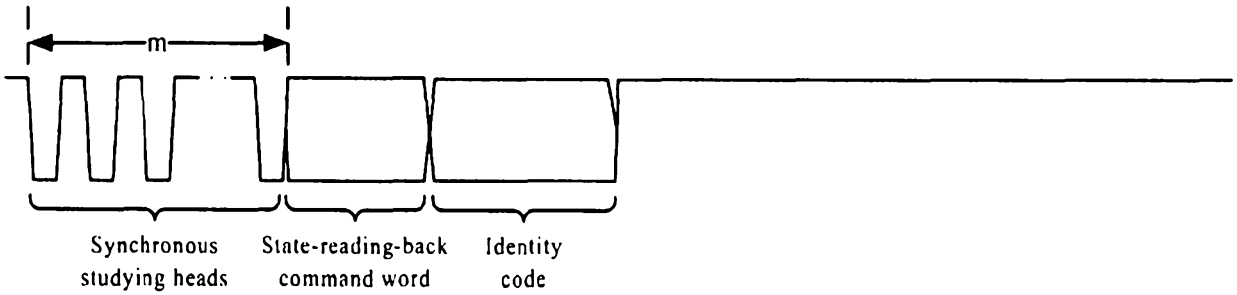

FIG.19

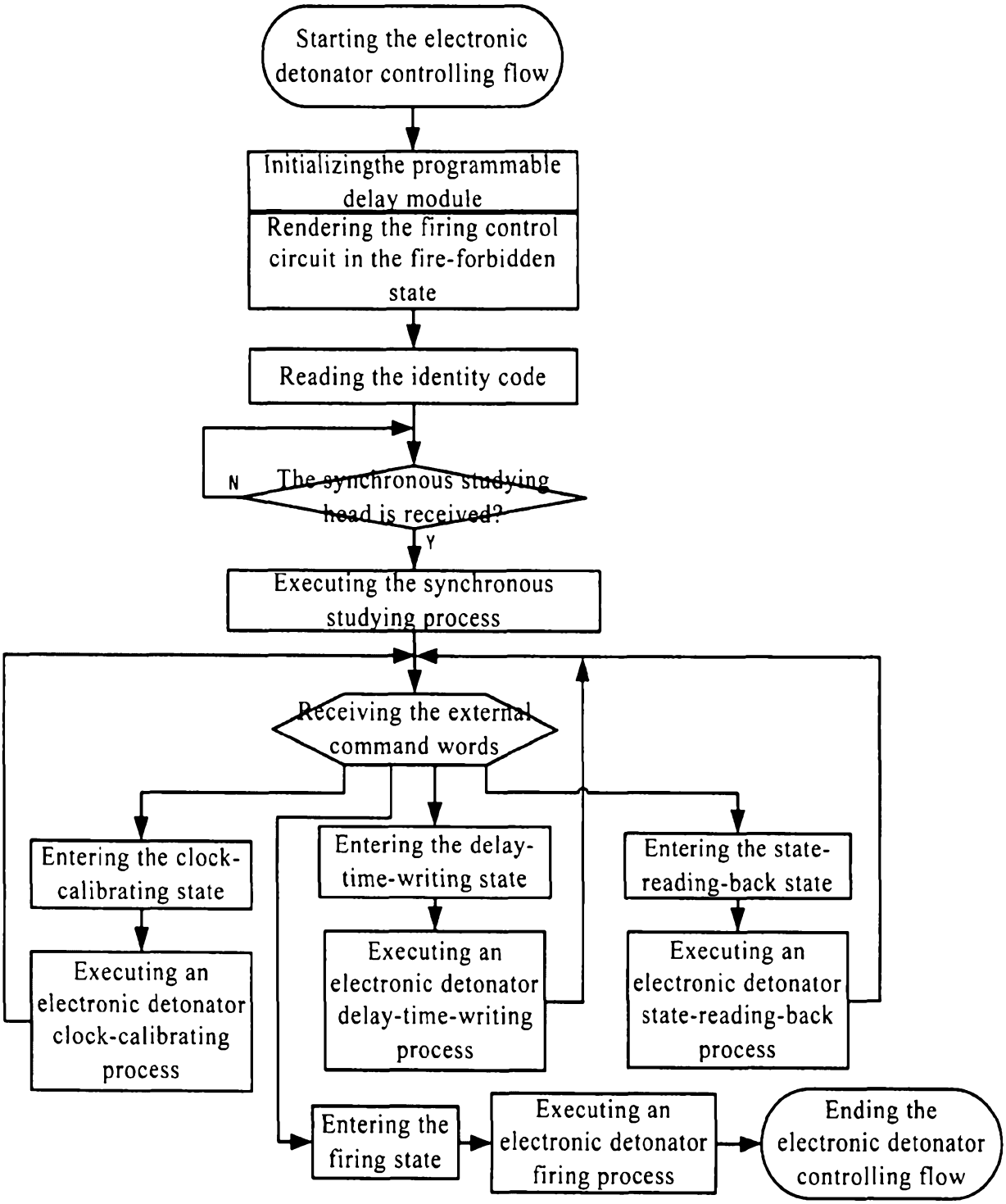
Starting the electronic detonator controlling flow
Initializingthe programmable delay module
Rendering the firing control circuit in the fire-forbidden state
Reading the identity code
N
The synchronous studying head is received?
Y
Executing the synchronous studying process
Receiving the external command words
Entering the clock-calibrating state
Executing an electronic detonator clock-calibrating process
Entering the delay-time-writing state
Executing an electronic detonator delay-time-writing process
Entering the state-reading-back state
Executing an electronic detonator state-reading-back process
Entering the firing state
Executing an electronic detonator firing process
Ending the electronic detonator controlling flow

FIG.20

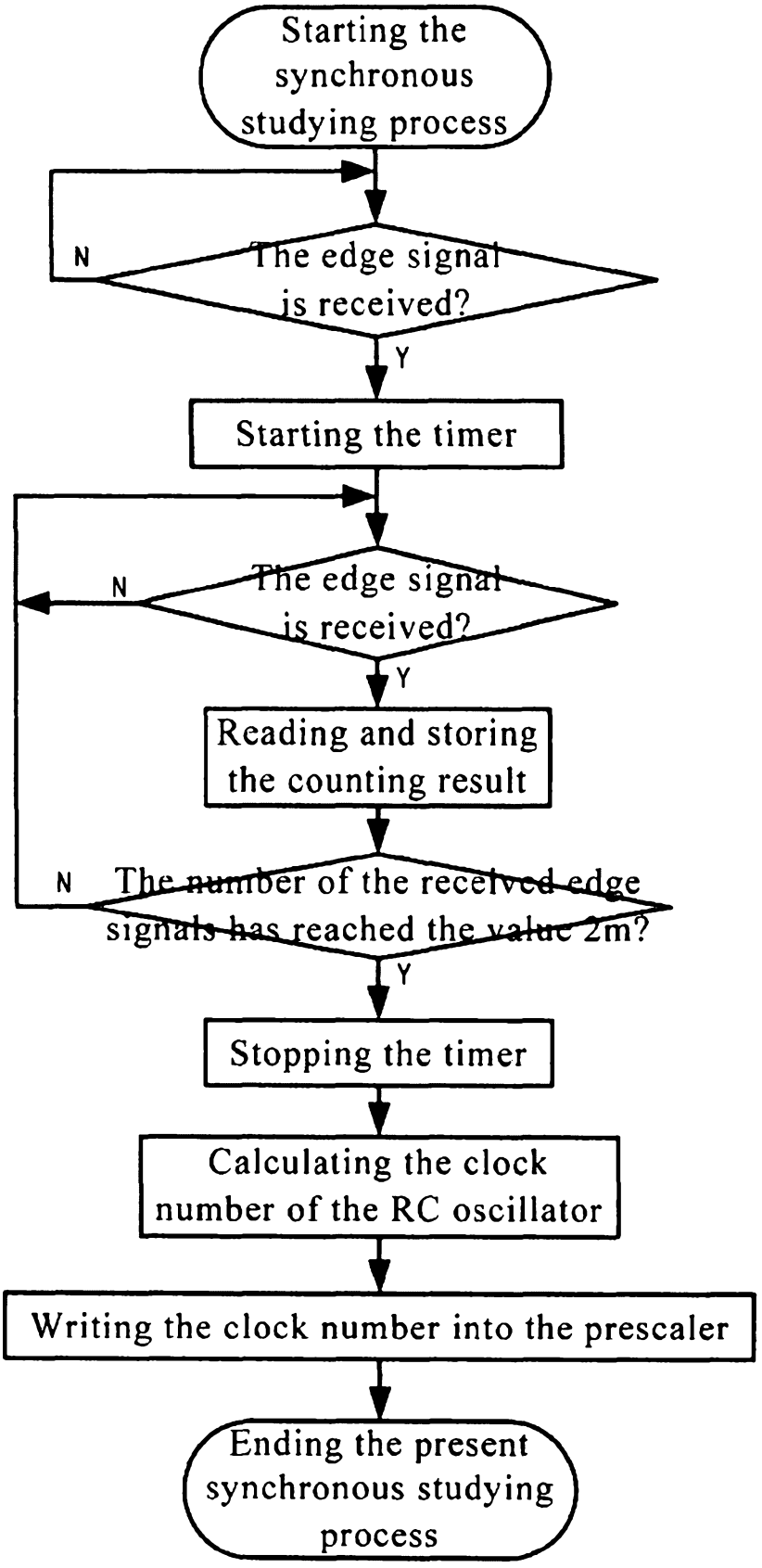
Starting the synchronous studying process
The edge signal is received?
N
Y
Starting the timer
The edge signal is received?
N
Y
Reading and storing the counting result
The number of the received edge signals has reached the value 2m?
N
Y
Stopping the timer
Calculating the clock number of the RC oscillator
Writing the clock number into the prescaler
Ending the present synchronous studying process

FIG.21

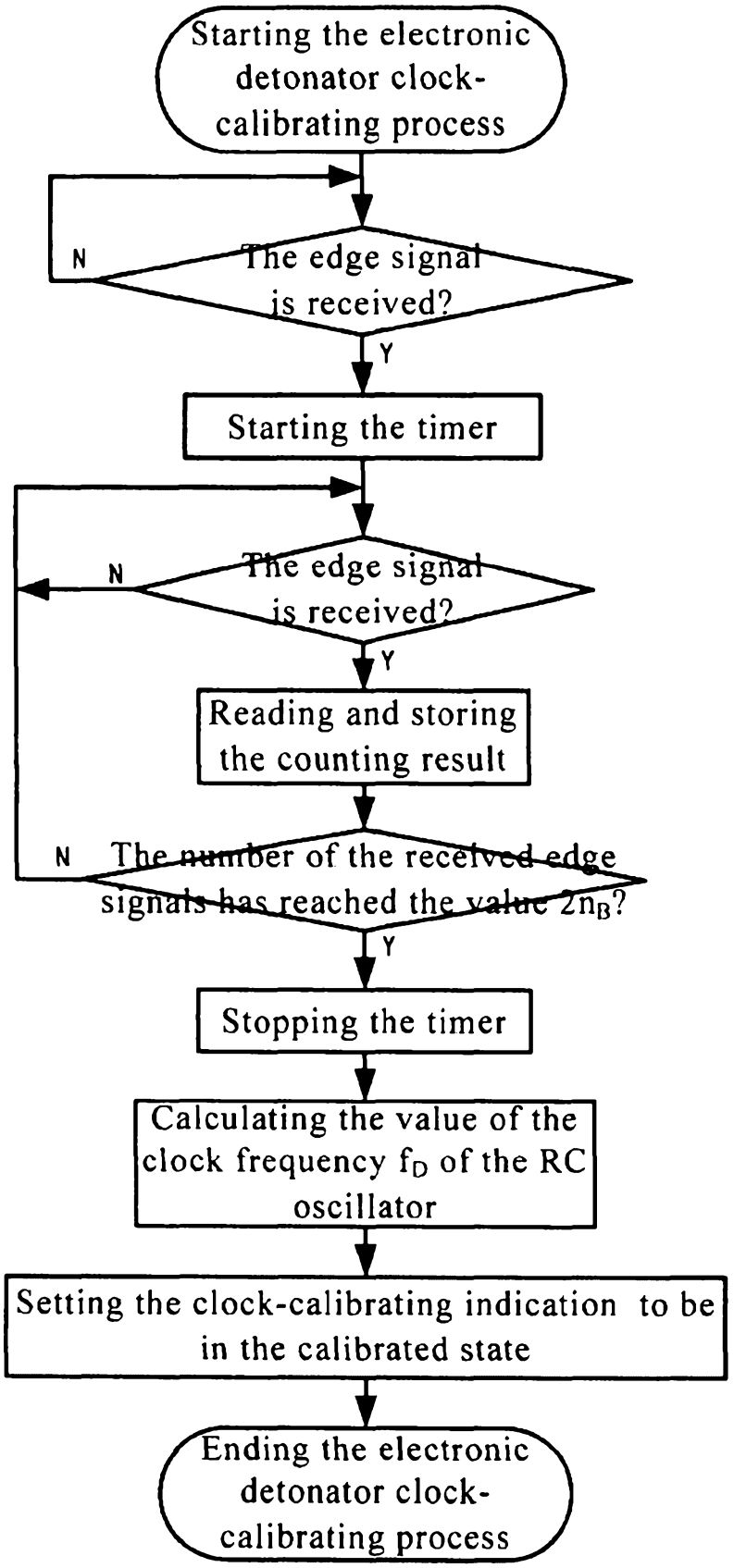
Starting the electronic detonator clock-calibrating process
The edge signal is received?
N
Y
Starting the timer
The edge signal is received?
N
Y
Reading and storing the counting result
The number of the received edge signals has reached the value $2n_B$?
N
Y
Stopping the timer
Calculating the value of the clock frequency f_D of the RC oscillator
Setting the clock-calibrating indication to be in the calibrated state
Ending the electronic detonator clock-calibrating process

FIG.22

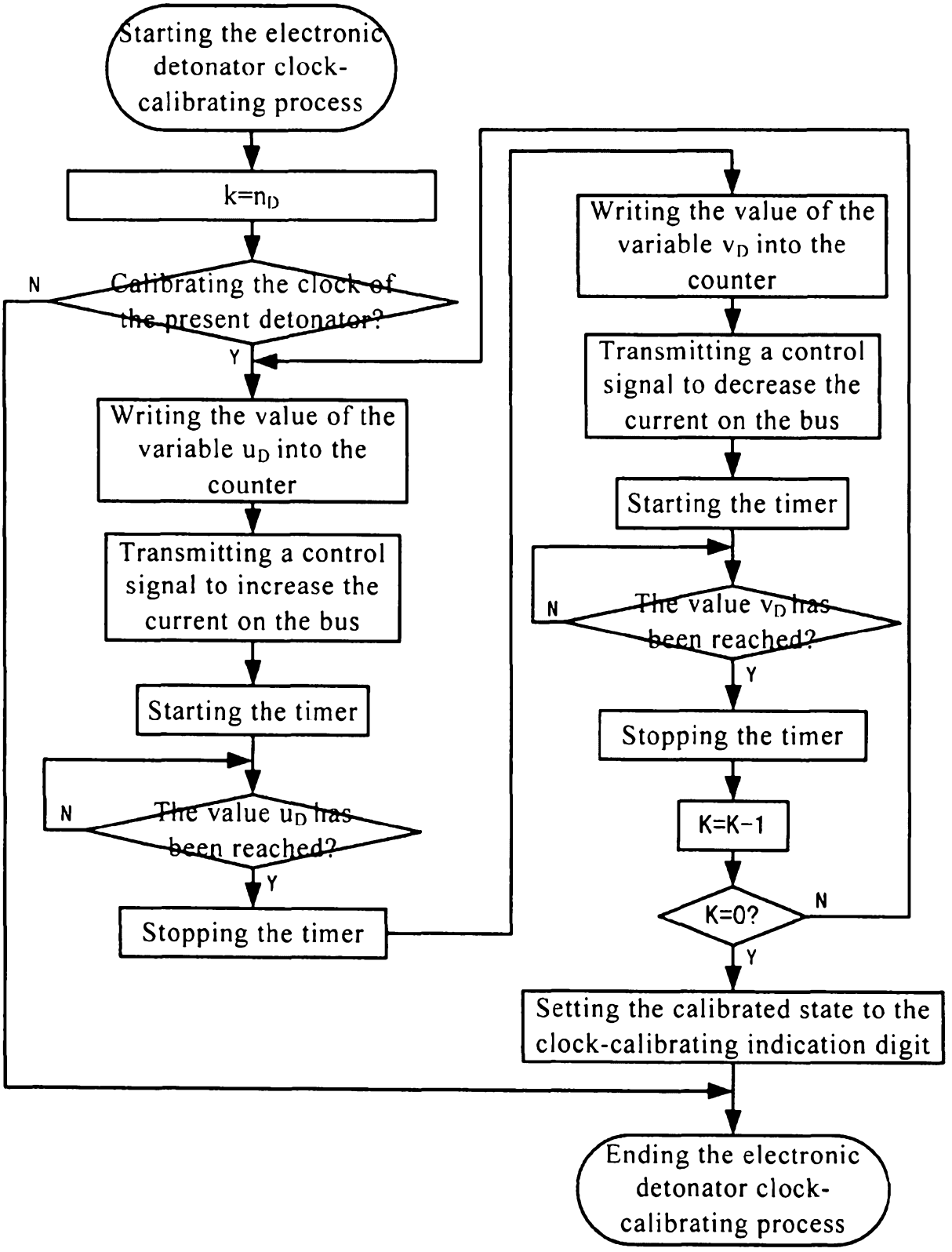
Starting the electronic detonator clock-calibrating process
k=nD
N
Calibrating the clock of the present detonator?
Y
Writing the value of the variable uD into the counter
Transmitting a control signal to increase the current on the bus
Starting the timer
N
The value uD has been reached?
Y
Stopping the timer
Writing the value of the variable vD into the counter
Transmitting a control signal to decrease the current on the bus
Starting the timer
N
The value vD has been reached?
Y
Stopping the timer
K=K-1
K=0?
N
Y
Setting the calibrated state to the clock-calibrating indication digit
Ending the electronic detonator clock-calibrating process

FIG.23

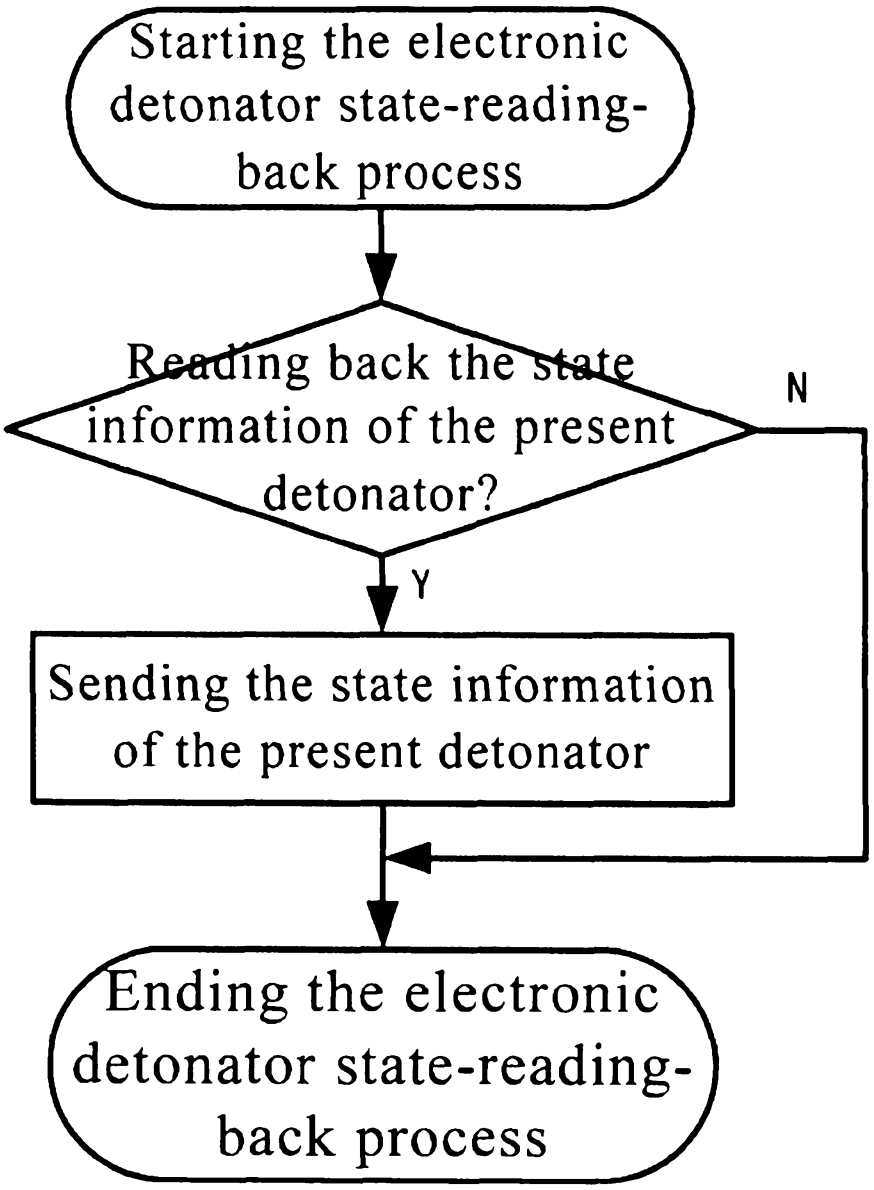
Starting the electronic detonator state-reading-back process
Reading back the state information of the present detonator?
N
Y
Sending the state information of the present detonator
Ending the electronic detonator state-reading-back process

FIG.24

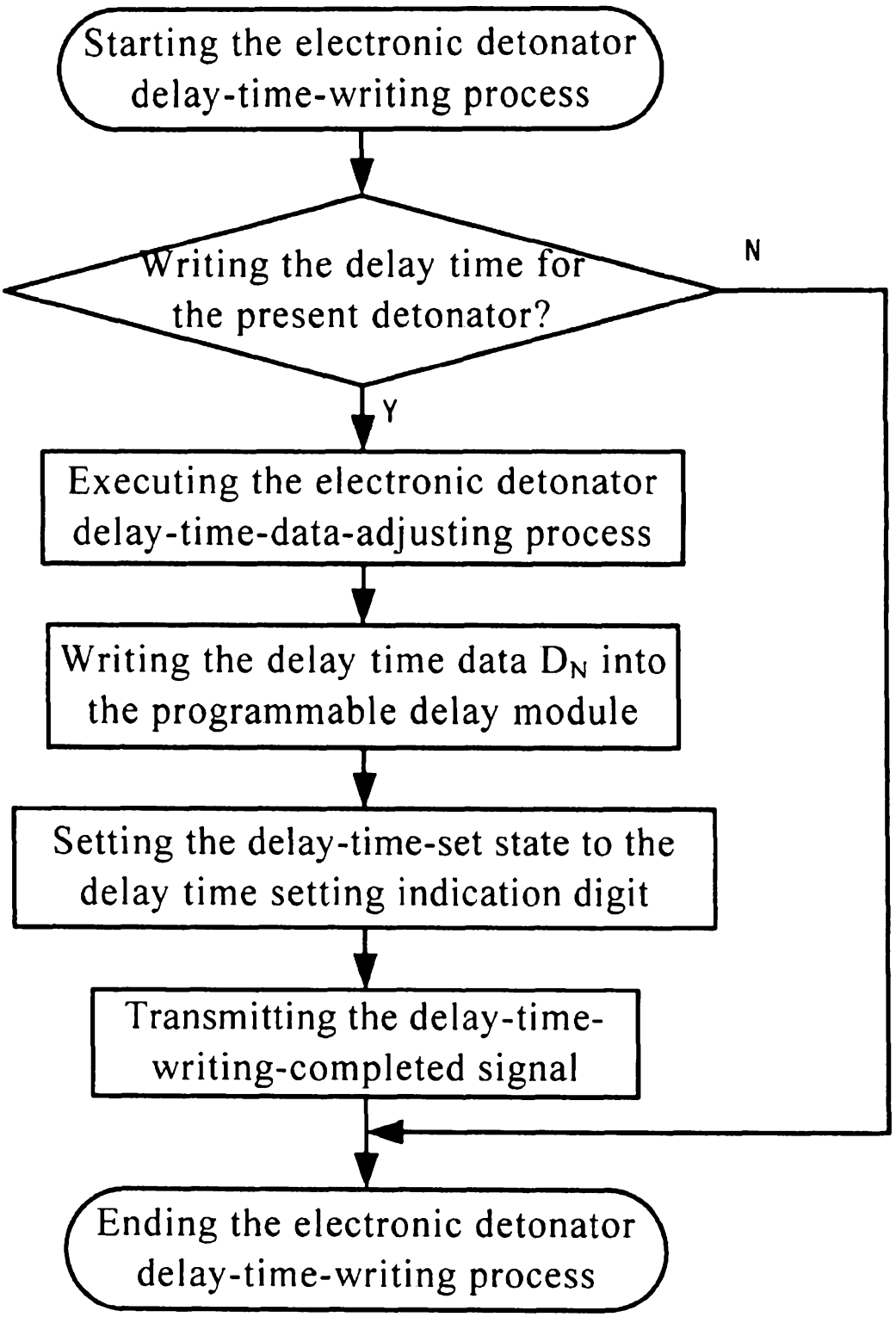
Starting the electronic detonator delay-time-writing process
Writing the delay time for the present detonator?
N
Y
Executing the electronic detonator delay-time-data-adjusting process
Writing the delay time data D_N into the programmable delay module
Setting the delay-time-set state to the delay time setting indication digit
Transmitting the delay-time-writing-completed signal
Ending the electronic detonator delay-time-writing process

FIG.25

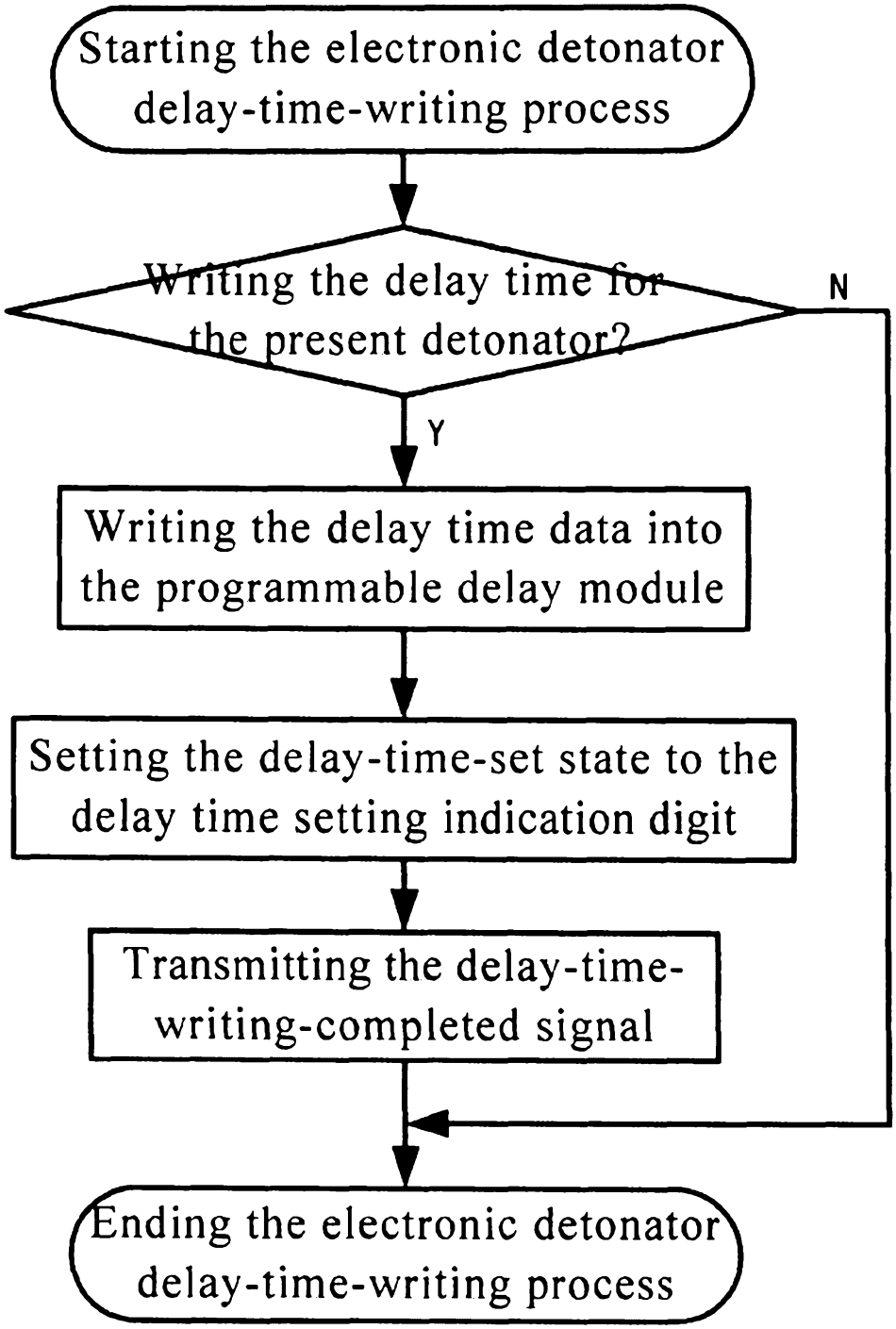
Starting the electronic detonator delay-time-writing process
Writing the delay time for the present detonator?
N
Y
Writing the delay time data into the programmable delay module
Setting the delay-time-set state to the delay time setting indication digit
Transmitting the delay-time-writing-completed signal
Ending the electronic detonator delay-time-writing process

FIG.26

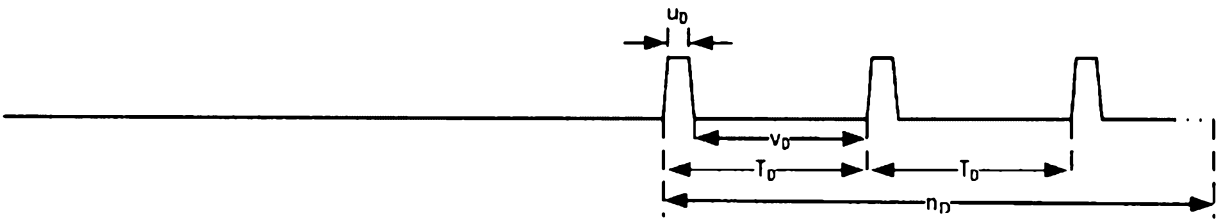

FIG.27

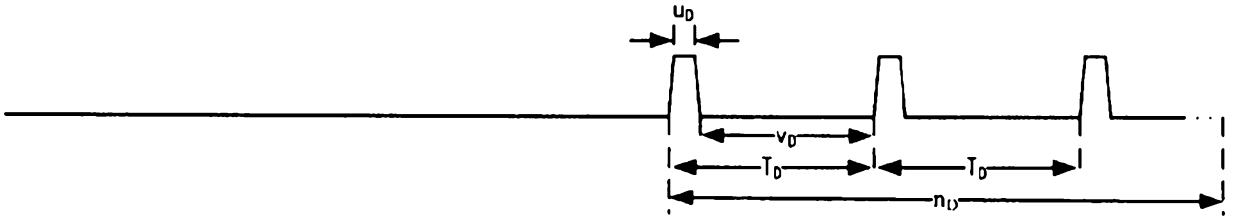

FIG.28

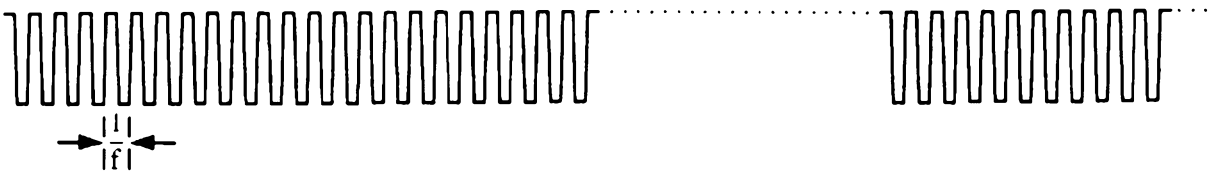

FIG.29

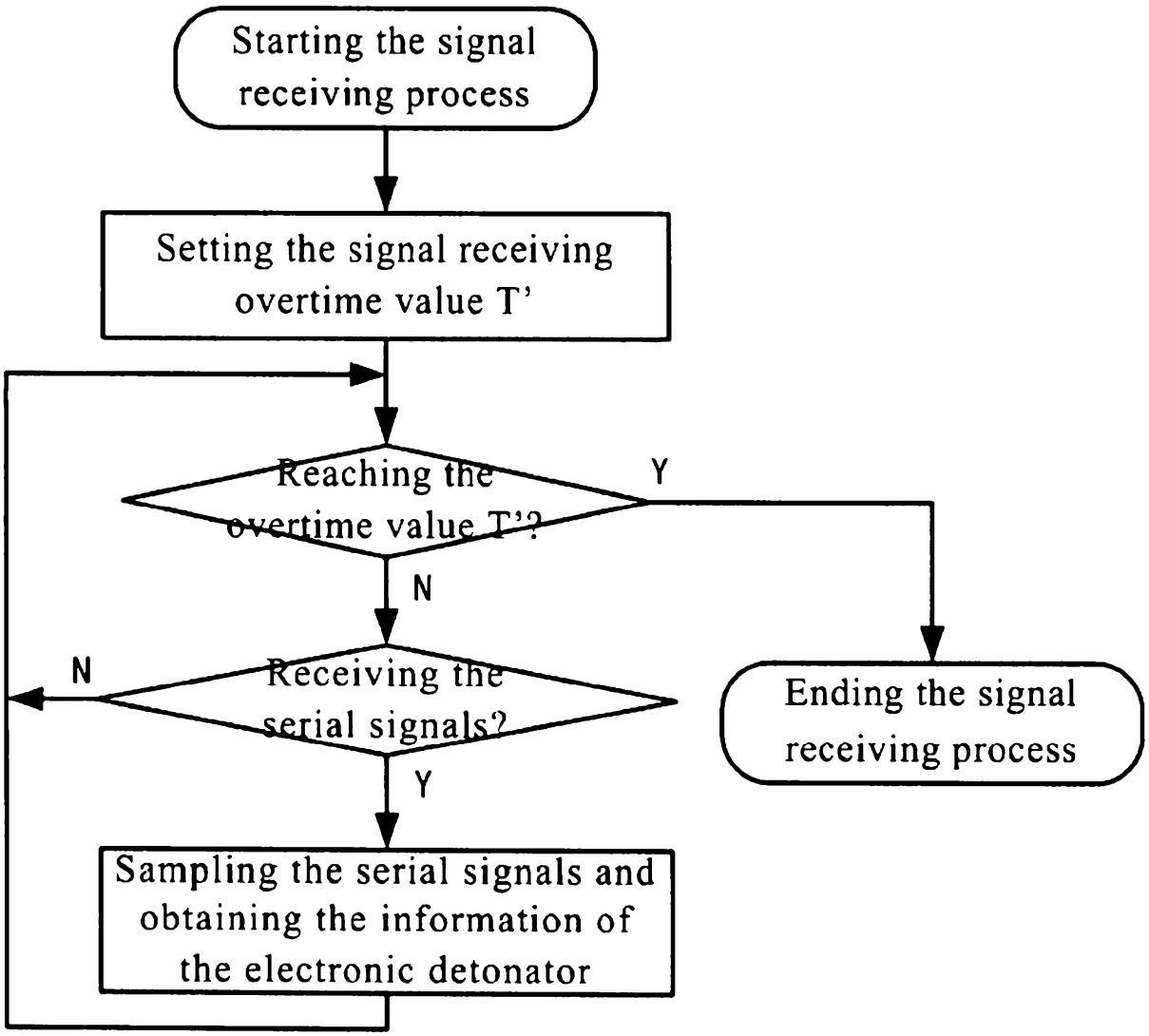
Starting the signal receiving process
Setting the signal receiving overtime value T'
Reaching the overtime value T'?
Y
N
Receiving the serial signals?
N
Y
Ending the signal receiving process
Sampling the serial signals and obtaining the information of the electronic detonator

FIG.30