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(54) **LOW INDUCTANCE BUSBAR SYSTEMS AND METHODS**

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,520,987 A * 7/1970 Ohlrich .... H02G 5/005 174/117 R
6,753,481 B2 * 6/2004 Novak H01L 23/50 174/255

(Continued)

FOREIGN PATENT DOCUMENTS

CN	201893455 U	7/2011
CN	102694356 A	9/2012
EP	1 311 045 A1	5/2003

OTHER PUBLICATIONS

Chen et al., "Investigation, Evaluation, and Optimization of Stray Inductance in Laminated Busbar", Power Electronics, IEEE Transactions on, vol. 29 , Issue 7, pp. 3679-3693, Sep. 18, 2013.

(Continued)

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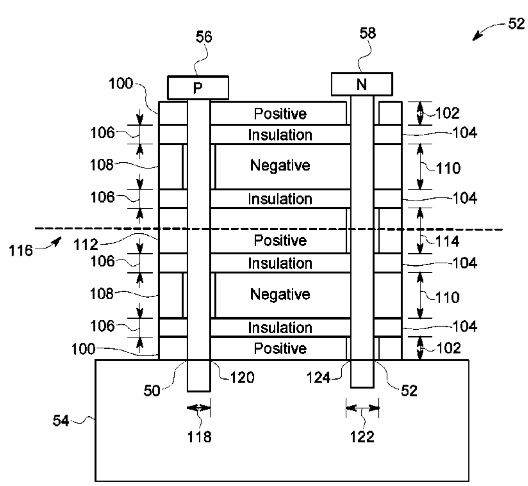
(57) **ABSTRACT**

An electrical system includes a power electronics system and a bus bar coupled to the power electronic system. The power electronics system includes a switching device configured to selectively connect and disconnect. The bus bar includes a first conductive layer and a second conductive layer. The first conductive layer is disposed directly adjacent a first insulation layer, wherein the first conductive layer is configured to conduct a first polarity of electrical power to, from, or both the power electronics system. The second conductive layer is disposed directly adjacent the first insulation layer, and is configured to conduct a second polarity of electrical power opposite the first polarity to, from, or both the power electronics system. The first conductive layer comprises a first thickness half a second thickness of the second conductive layer.

4 Claims, 5 Drawing Sheets



(51) **Int. Cl.**

H02B 1/20	(2006.01)
H02M 7/00	(2006.01)
H01G 2/02	(2006.01)

(52) **U.S. Cl.**

CPC ***H02M 7/003*** (2013.01); ***H05K 7/02*** (2013.01); *H01G 2/02* (2013.01); *H05K 999/99* (2013.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,798,833	B2	9/2010	Holbrook	
8,112,853	B2	2/2012	Yoshinaga et al.	
8,193,449	B2	6/2012	Esmaili et al.	
9,083,128	B2	7/2015	Pfeuffer et al.	
2007/0019352	A1*	1/2007	Anthony	H01C 7/123 361/118
2008/0013253	A1*	1/2008	Thrap	H01G 9/016 361/502
2010/0067173	A1*	3/2010	Guillet	H01G 9/016 361/502
2010/0302733	A1	12/2010	Woody et al.	
2011/0170232	A1*	7/2011	Weir	H01G 9/14 361/312
2013/0316200	A1*	11/2013	Ochi	H01M 2/1077 429/53
2014/0111959	A1	4/2014	Li et al.	
2014/0209344	A1*	7/2014	Kalayjian	H05K 7/1432 174/68.2
2015/0035496	A1*	2/2015	Kikuchi	B60L 11/1816 320/137

OTHER PUBLICATIONS

Extended European Search Report and Opinion issued in connection with corresponding EP Application No. 17197905.7 dated Feb. 26, 2018.

* cited by examiner

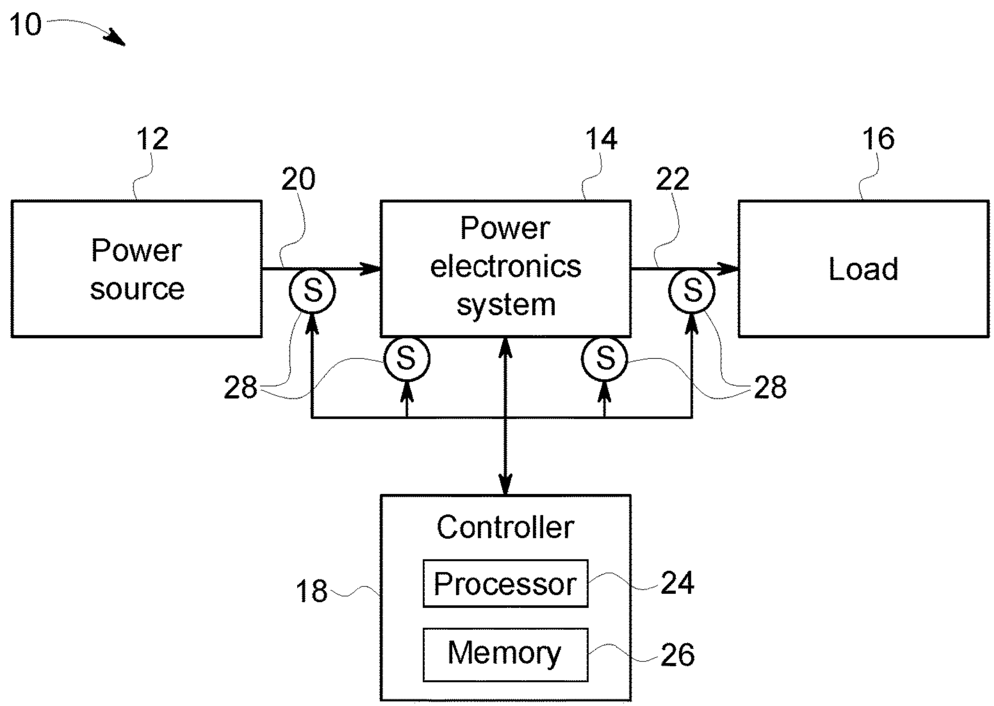

10
12
20
14
22
16
Power source
Power electronics system
Load
S
S
S
S
28
28
Controller
Processor
Memory
18
24
26

FIG. 1

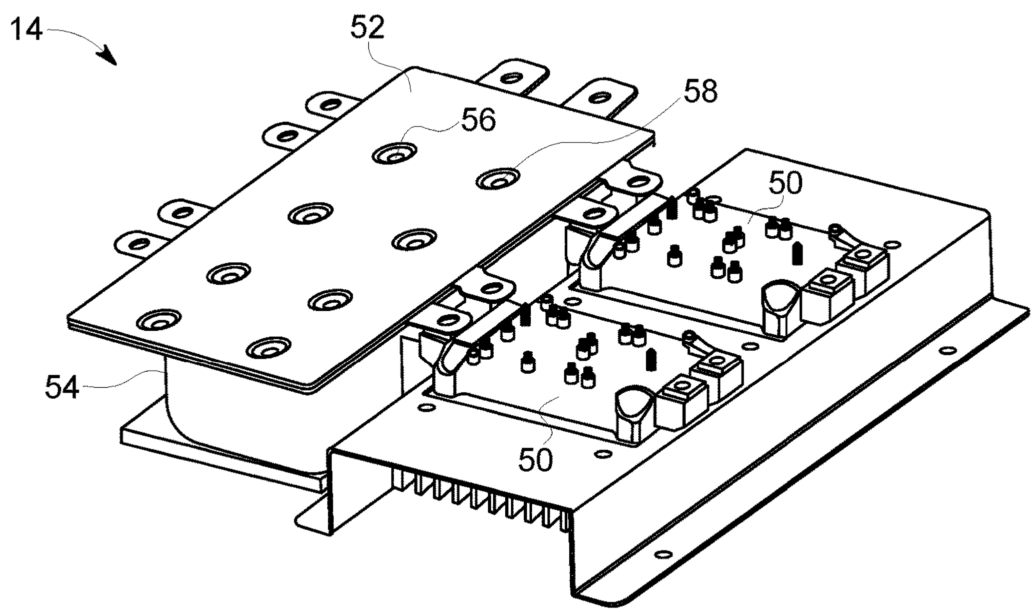


FIG. 2

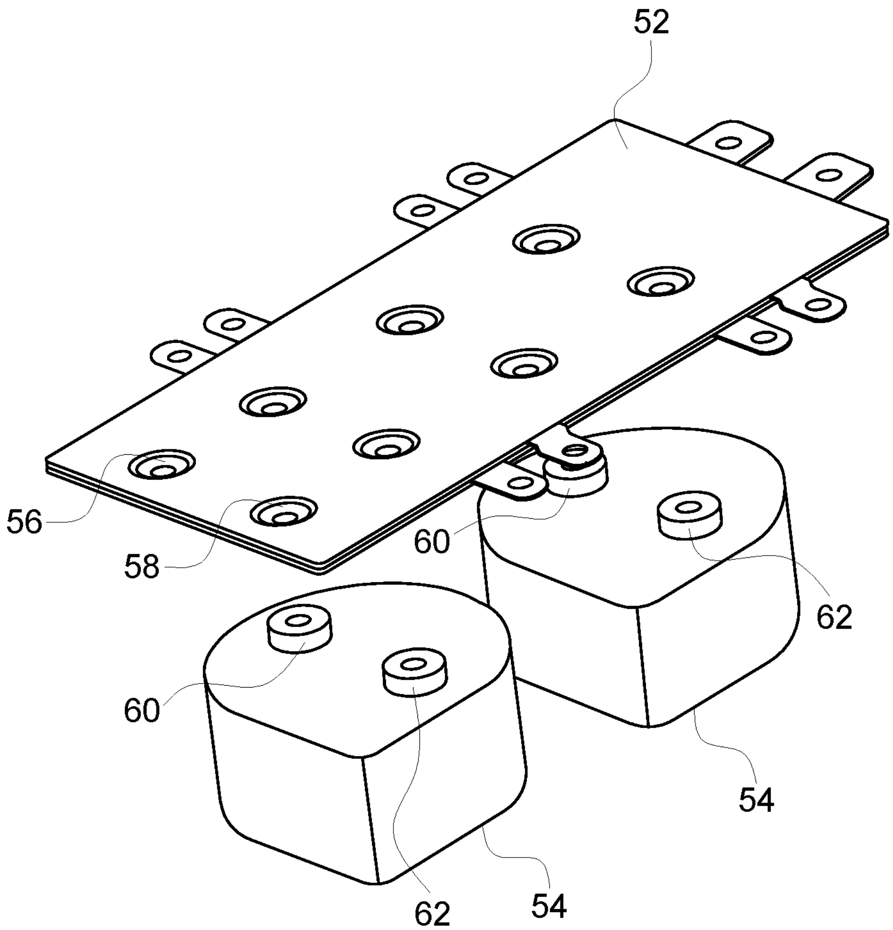


FIG. 3

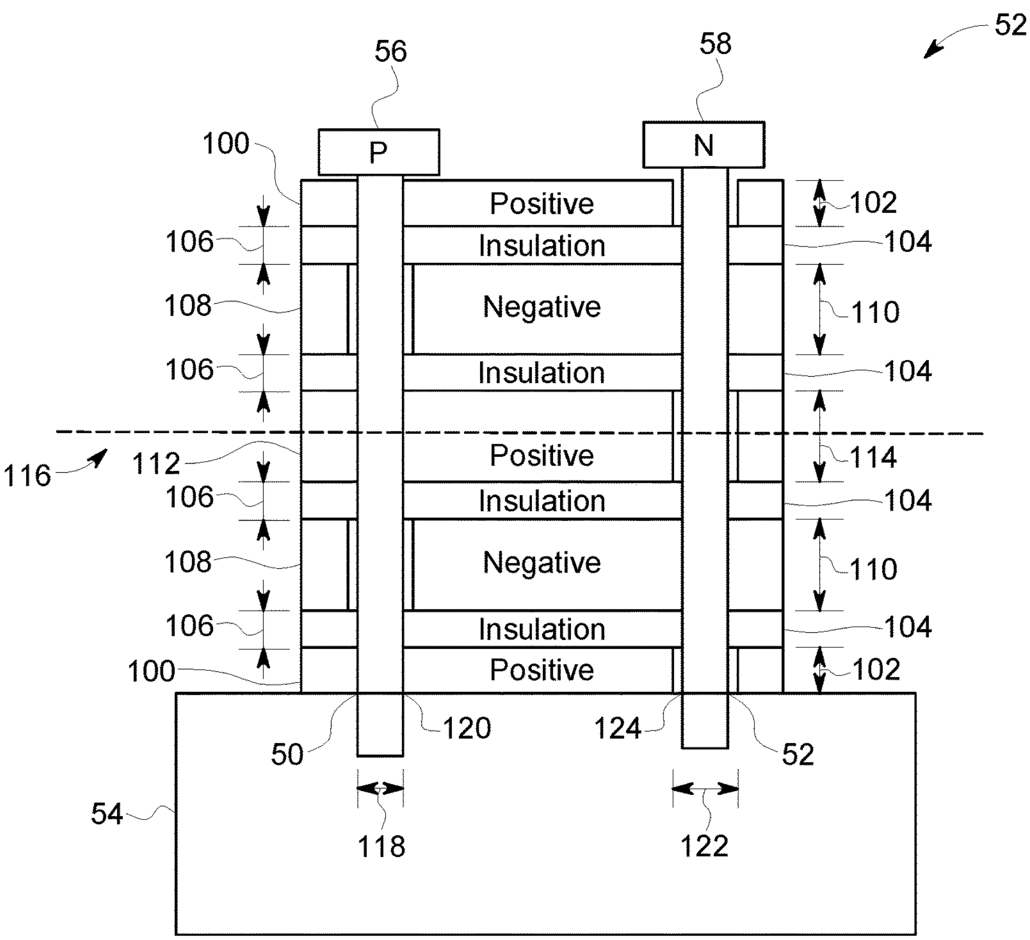

52
56
58
P
N
100
102
Positive
106
Insulation
104
108
Negative
110
106
Insulation
104
116
112
Positive
114
106
Insulation
104
108
Negative
110
106
Insulation
104
100
Positive
102
50
120
124
52
54
118
122

FIG. 4

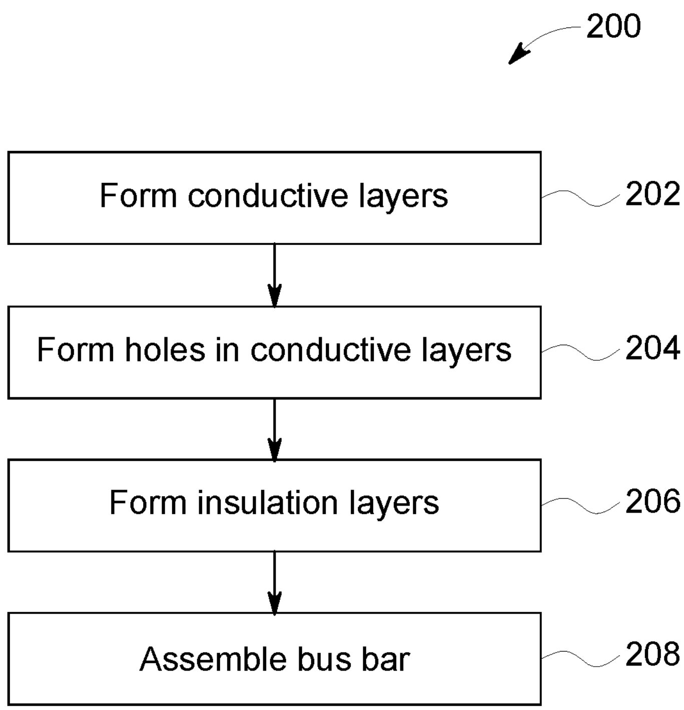

200
Form conductive layers
202
Form holes in conductive layers
204
Form insulation layers
206
Assemble bus bar
208

FIG. 5

LOW INDUCTANCE BUSBAR SYSTEMS AND METHODS

BACKGROUND

The subject matter disclosed herein relates to electrical systems and, more specifically, bus bars utilized in an electrical system.

Generally, an electrical system may include a bus bar to facilitate electrically connecting electrical devices. For example, a bus bar may be implemented to enable supplying DC electrical power from a power module that includes one or more switching devices (e.g., semiconductor switch, transistor, or power device) to an electrical load. In some instances, operation of switching devices may generate high levels of overvoltage in the bus bar structure due to the parasitic stray inductance. For example, when a switching device opens, the current in the bus bar changes, thereby resulting in a voltage spike, which may lead to voltage stress and/or affect operation of electrical devices (e.g., components).

BRIEF DESCRIPTION

Certain embodiments commensurate in scope with the original claims are summarized below. These embodiments are not intended to limit the scope of the claims, but rather these embodiments are intended only to provide a brief summary of possible forms of the claimed subject matter. Indeed, the claims may encompass a variety of forms that may be similar to or different from the embodiments set forth below.

In one embodiment, an electrical system includes a power electronics system and a bus bar coupled to the power electronic system. The power electronics system includes a switching device configured to selectively connect and disconnect. The bus bar includes a first conductive layer and a second conductive layer. The first conductive layer is disposed directly adjacent a first insulation layer, wherein the first conductive layer is configured to conduct a first polarity of electrical power to, from, or both the power electronics system. The second conductive layer is disposed directly adjacent the first insulation layer, and is configured to conduct a second polarity of electrical power opposite the first polarity to, from, or both the power electronics system. The first conductive layer comprises a first thickness half a second thickness of the second conductive layer.

In a second embodiment, a bus bar is configured to electrically connect to one or more electrical components. The bus bar includes an interior positive layer, first and second intermediate negative layers, and first and second exterior positive layers. The first intermediate negative layer and the second intermediate negative layer are electrically connected in parallel and disposed on opposite sides of the interior positive layer. The first exterior positive layer is electrically connected in parallel with the interior positive layer. The first exterior positive layer and the interior positive layer are disposed on opposite sides of the first intermediate negative layer. The second exterior positive layer is electrically connected in parallel with the interior positive layer and the first exterior positive layer. The second exterior positive layer and the interior positive layer are disposed on opposite sides of the second intermediate negative layer. The volume of the interior positive layer is different from volume of the first exterior positive layer and volume of the second exterior positive layer.

In a third embodiment, a method of manufacturing a bus bar used to electrically connect one or more electrical components includes coupling a first insulating layer to a first side of an interior positive layer, wherein the interior positive layer comprises a first thickness, coupling a second insulating layer to a second side of the interior positive layer, coupling a first intermediate negative layer to the first insulating layer, wherein the first intermediate negative layer comprises the first thickness, coupling a second intermediate negative layer to the second insulating layer, wherein the second intermediate negative layer comprises the first thickness, coupling a third insulating layer to the first intermediate negative layer, coupling a fourth insulating layer to the second intermediate negative layer, coupling a first external positive layer to the third insulating layer, wherein the first external positive layer comprises a second thickness different from the first thickness, and coupling a second external positive layer to the fourth insulating layer, wherein the second external positive layer comprises the second thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present disclosure will become better understood when the following detailed description is read with reference to the accompanying drawings in which like characters represent like parts throughout the drawings, wherein:

FIG. **1** is a perspective view of an electrical system, in accordance with an embodiment;

FIG. **2** is a perspective view of a power electronics system utilized in the electrical system of FIG. **1**, in accordance with an embodiment;

FIG. **3** is a perspective view of a bus bar utilized in the power electronics system shown of FIG. **2**, coupled to two capacitors, in accordance with an embodiment;

FIG. **4** is a side, section view of the bus bar having 9 layers, with the exterior conductive layers being half the thickness of the interior conductive layers, in accordance with an embodiment; and

FIG. **5** is a flow chart of a process for manufacturing the bus bar of FIG. **4**, in accordance with an embodiment.

DETAILED DESCRIPTION

One or more specific embodiments will be described below. In an effort to provide a concise description of these embodiments, all features of an actual implementation may not be described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

When introducing elements of various embodiments of the present disclosure, the articles "a," "an," "the," and "said" are intended to mean that there are one or more of the elements. The terms "comprising," "including," and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements. Furthermore, any numerical examples in the following discussion are intended to be non-limiting, and thus additional numerical values, ranges, and percentages are within the scope of the disclosed embodiments.

One embodiment of an electrical system **10** is shown in FIG. **1**. In some embodiments, the electrical system **10** may be included in an industrial system, a manufacturing system, an automation system, or the like, such as a factory or plant. Additionally, in some embodiments, the electrical system **10** may be included in a computing system, such as a computer, or an automotive system, such as an airplane, boat, or car.

In the depicted embodiment, the electrical system **10** includes a power source **12** (e.g., an AC power source), a power electronics system **14**, an electrical load **16** (e.g., a DC load), and a controller **18**. As depicted, the power source **12** is electrically connected to the power electronics system **14** via a first electrical connection **20** (e.g., one or more bus bars), which may enable the power source **12** to supply electrical power to the power electronics system **14**. Accordingly, in some embodiments, the power source **12** may be a power grid, an AC power generator, an alternator, or the like. In other embodiments, the power source may be a DC power source.

Additionally, in the depicted embodiment, the power electronics system **14** is electrically connected to the electrical load **16** via a second electrical connection **22** (e.g., a DC load), which may enable the power electronics system **14** to supply electrical power to the electrical load **16**. In some embodiments, the electrical load **16** may store the electrical power and/or use the electrical power to perform an operation. Accordingly, in some embodiments, the electrical load **16** may be a battery, a computer, an engine control unit, a display, a light bulb, a heating, ventilating, and air conditioning (HVAC) system, or the like. In other embodiments, the electrical load **16** may be an AC load.

Thus, in operation, the power electronics system **14** may convert input electrical power received from the power source **12** into output electrical power supplied to the electrical load **16**. In some embodiments, the power electronics system **14** may operate to convert input AC electrical power into output DC electrical power or vice versa. Additionally or alternatively, the power electronics system **14** may operate to convert input DC electrical power into output DC electrical power and/or to convert input AC electrical power into output AC electrical power, for example, to control (e.g., regulate) voltage and/or current supplied to the electrical load **16**.

To facilitate conversion, the controller **18** may control operation of the power electronics system **14**, for example, by instructing a switching device in the power electronics system **14** to open or close. Accordingly, the controller **18** may include a processor component **24** and a memory component **26**. In some embodiments, the memory component **26** may include a tangible, non-transitory, computer readable medium that stores instructions executable by the processor component **24**. Thus, in such embodiments, the memory component **26** may include random access memory (RAM), read only memory (ROM), rewritable non-volatile memory (e.g., flash memory), hard drives, optical discs, and/or the like. Additionally, the processor component **24** may include one or more general purpose microprocessors, one or more application specific processors (ASICs), one or more field programmable logic arrays (FPGAs), or any combination thereof. Additionally or alternatively, the controller **18** may utilize analog control based on op-amps, logic gates, and/or other control circuitry.

In some embodiments, the controller **18** may control operation of the power electronics system **14** based at least in part on measured operational parameters of the power electronics system **14**, such as current of input electrical power, voltage of input electrical power, current of output electrical power, and/or voltage of output electrical power. To facilitate determining the operational parameters, one or more sensors **28** may be disposed on or coupled to the power electronics system **14**, the first electrical connection **20**, and/or the second electrical connection **22**. In some embodiments, the sensors **28** may include temperature sensors, pressure sensors, voltage sensors, current sensors, power sensors, or any combination thereof. The sensors **28** may then communicate sensor data indicative of the measured operational parameters to the controller **18**.

Based at least in part on the measured operational parameters, the controller **18** may control operation of the power electronics system **14**, for example, to convert AC electrical power received from the power source **12** into voltage regulated DC electrical power to be supplied to the electrical load **16**. As described above, the controller **18** may control operation of the power electronics system **14**, for example, by instructing one or more switching devices in the power condition unit **14** to open or to close at specific times.

To help illustrate, an example embodiment of the power electronics system **14** is shown in FIG. **2**. As illustrated, the power electronics system **14** includes one or more switching devices **50**. In some embodiments, a switching device **50** may include a semiconductor (e.g., silicon, silicon carbide, gallium nitride, or any other) switch and/or transistor. Additionally or alternatively, the switching device **50** may include a mechanical switch.

As described above, the power electronics system **14** may be electrically coupled to other electrical devices via one or more electrical connections. For example, the power electronics system **14** may be electrically connected to an electrical load **16** via a second electrical connection **22**. Additionally or alternatively, the power electronics system **14** may be electrically connected to a power source **12** via a first electrical connection **20**.

In some embodiments, an electrical connection may be implemented using one or more bus bars **52**. For example, in the depicted embodiment, the bus bar **52** may electrically connect the switching device **50** to multiple capacitors **54** (e.g., electrical components or devices). In the illustrated embodiment, there are two capacitors **54** arranged in a 1×2 array. However, it should be noted that the depicted embodiment is merely intended to be illustrative. Thus, in other embodiments, any suitable number (e.g., 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, or more capacitors) of capacitors **54** may be arranged in any suitable configuration (e.g., 1×1, 1×2, 2×2, 2×3, etc.).

To facilitate electrically connecting electrical components, the bus bar **52** may include one or more conductive layers. For example, in the depicted embodiment, a positive terminal of each capacitor **54** is coupled to the bus bar via a positive fastener **56** (e.g., screw). Thus, the bus bar **52** may include one or more positive layers. Additionally, in some embodiments, a positive fastener **56** may extend through the bus bar **52** to electrically connect the positive terminal of a corresponding capacitor **54** to each of the positive layers of the bus bar **52**.

Additionally, in the depicted embodiment, a negative terminal of each capacitor **54** is coupled to the bus bar via a negative fastener **58** (e.g., screw). Thus, the bus bar **52** may include one or more negative layers. Additionally, in some embodiments, a negative fastener **58** may extend through the bus bar **52** to electrically connect the negative terminal of a corresponding capacitor **54** to each of the negative layers of the bus bar **52**.

As described above, other configurations of the capacitors **54** may be implemented. To help illustrate, another example embodiment of a bus bar **52** electrically coupled to the capacitors is shown in FIG. **3**. In particular, the bus bar **52** is electrically connected to two capacitors **54** arranged in a 1×2 array.

Additionally, as shown, each capacitor **54** has a positive terminal **60** and a negative terminal **62**. In some embodiments, the positive terminal **60** and/or the negative terminal **62** may include a threaded hole for receiving a fastener (e.g., a positive fastener **56** or a negative fastener **58**). In other embodiments, the positive terminal **60** and/or the negative terminal **62** may include a threaded rod, which may extend up through and receive a nut to secure a corresponding capacitor **54** to the bus bar **52**. In this manner, one or more capacitors **54** may be physically secured to and electrically connected to a bus bar **52**.

Returning to FIG. **2**, as described above, the switching devices **50** in the power electronics system **14** may operate (e.g., switch) to facilitate converting input electrical power into output electrical power. In particular, a switching device may selectively connect (e.g., close) and disconnect (e.g., open). In some embodiments, the switching devices **50** may switch at relatively high speeds, thereby resulting in larger changes in current over time (e.g., di/dt) and/or larger changes in voltage over time (e.g., dv/dt)

However, in some instances, change in voltage over time may generate electric fields that induce current in surrounding conductive components. Additionally, in some instances, change in current over time may generate magnetic fields that affect flow of electrical power. In other words, change in current over time in a bus bar **52** may result in voltage across the stray inductance in the bus bar **52**, such as voltage drops and/or voltage spikes. The overvoltage may affect operation and/or reliability (e.g., life span) of the bus bar **52** and/or other electrical components (e.g., capacitors **54** or power electronics system **14**).

In some embodiments, stray inductance may be reduced by implementing a laminated bus bar **52** to include a single positive layer and a single negative layer separated by an insulation layer. In this manner, magnetic field generated by flow of current through the positive layer may at least partially offset magnetic field generated by flow of current through the negative layer, thereby reducing stray inductance. However, magnetic fields offset distance between respective sources of the magnetic field. In the other words, magnetic fields generated with thinner insulation layer may offset to a larger degree than magnetic fields generated with thicker insulation layer.

To facilitate further reducing stray inductance, in some embodiments, a bus bar **52** may be implemented to include multiple parallel current paths. In particular, instead of a single positive layer and a single negative layer, the bus bar **52** may be implemented using multiple positive layers and multiple negative layers. To facilitate achieving relatively the same power rating, total volume (e.g., thickness, width, and/or height) of the multiple positive layers may be approximately equal to volume of the single positive layer. In this manner, bus bar **52** may conduct approximately the same magnitude of electrical power by dividing positive current between the multiple positive layer

Similarly, total volume (e.g., thickness, width, and/or height) of the multiple negative layers may be approximately equal to volume of the single negative layer. In this manner, bus bar **52** may conduct approximately the same magnitude of electrical power by dividing negative current between the negative layers. Additionally, to facilitate offsetting generated magnetic field, the positive layers may be staggered between the negative layers such that each pair of adjacent conductive (e.g., positive or negative) layers is separated by an insulation layer.

Additionally, in some embodiments, the bus bar **52** may be implemented using an equal number of positive layers and negative layers with the same thickness. For example, a bus bar **52** may include four positive layers staggered between four negative layers and seven insulation layers separating each adjacent positive layer and negative layer pair. In this manner, magnetic field generated by each conductive layer may be closer to an offsetting magnetic field generated by an opposite polarity conductive layer, thereby further reducing stray inductance in a bus bar **52**.

However, implementing equal number of positive layers and negative layers may increase implementation associated cost, such as component count and/or manufacturing complexity. For example, number of insulation layers utilized in a bus bar **52** may be increased (e.g., from one to seven). Additionally, total number of layer and, thus, total may be increased size of the bus bar **52** may be increased (e.g., from three to fifteen). Moreover, manufacturing complexity may increase to ensure that each fastener contacts the appropriate conductive layers (e.g., positive fastener **56** contacts each of the positive layers, but not the negative layers).

To facilitate reducing effect on implementation associated cost while maintaining improved stray inductance performance, other implementations of a bus bar **52** including multiple positive layers and/or multiple negative are considered. For example, in some embodiments, a bus bar **52** may be implemented such that number of positive layers differs from number of negative layers. Additionally or alternatively, a bus bar **52** may be implemented such that thickness of different conductive (e.g., positive or negative) layers differ.

To help illustrate, an example embodiment of a bus bar **52** implemented with multiple negative layers and multiple positive layers coupled to a capacitor **54** is shown in FIG. **4**. As depicted, the bus bar **52** includes external positive layers **100** each having a thickness **102** and an internal positive layer **112** have a thickness **114**. Additionally, as depicted, the bus bar **52** includes two internal negative layers **108** each have a thickness **110**. Thus, the bus bar **52** is implemented with different number of positive layers and negative layers.

To maintain electrical isolation, an insulation layer **104** having a thickness **106** is disposed between each adjacent pair of opposite polarity conductive layers. Thus, the bus bar **52** is implemented with four insulation layers **104** and nine total layers. In some embodiments, reducing number of insulation layers and/or reducing total number of layer may facilitate reducing implementation associated cost.

To facilitate reducing stray inductance, the thickness **114** of the internal positive layer **112** may approximately equal to the thickness **110** of each internal negative layer **108**. Additionally, the thickness **100** of each external positive layer **110** may be approximately half the thickness **114** of the internal positive layer **112** and, thus, approximately half the thickness **110** of each internal negative layer **108**. For illustrative purpose, the insulation layers **104** may have a thickness **106** of approximately 0.5 mm, the external positive layers **100** may each have a thickness **102** of approximately 1 mm, the internal negative layers **108** may each have a thickness **110** of approximately 2 mm, and the interior positive layer **112** may have a thickness **114** of approximately 2 mm.

It should be understood, however that other thicknesses **102**, **106**, **110**, **114** may be possible. Similarly, other thickness ratios between layers may also be possible. In particular, in the above-described embodiment, the ratio between the thickness of each external layers to thickness of each of the internal layers is 2:1. However, other ratios may be possible. For example, in other embodiments, the ratio may be 1.5:1, 1.7:1, 1.75:1, 1.8:1, 1.9:1, 2.1:1, 2.2:1, 2.3:1, 2.4:1, 2.5:1, or any other ratio. Similarly, the ratios of the thickness **106** of the insulation layers **104** to the thicknesses **102**, **110**, **114** of the exterior layers **100** and the interior layers **108**, **112** may vary.

It should be appreciated that in other embodiments a bus bar **116** may be implemented with the positive layers and the negative layers reversed. That is, the bus bar **52** may be implemented with three negative layers and two positive layers. Additionally, the external layers of the bus bar **52** may be negative layers, which are each half the thickness of an internal conductive layer. Further, though the bus bar **52** in FIG. **4** includes 5 conductive layers (e.g., one internal positive layer **112**, two negative layers **108**, and two external positive layers **100**), it should be understood that other embodiments of the bus bar **52** may include any off number of conductive layers. That is, the bus bar **52** may include 3, 5, 7, 9, 11, 13, 15, 17, 19, or more layers.

In the illustrated embodiment, the bus bar **52** is symmetrical about a plane **116** that extends through the middle of the internal positive layer **112**, parallel to the negative layers **108** and the external positive layers **100**. The symmetry of the bus bar **52** cancels magnetic flux to improve the performance of the bus bar **52**, however, embodiments of the bus bar **52** that are not symmetrical are also envisaged.

As illustrated, for each capacitor **54** connected to the bus bar **52**, each layer has a pair holes, including a smaller diameter **118** hole **120** and a larger diameter **122** hole **124**. The diameter difference between **118** and **122** depends on the insulation distance. As shown, the positive fastener **56** extends through the smaller diameter **118** holes **120** in the positive layers such that the positive fastener **56** is electrically connected to each of the external positive layers **100** and the internal positive layer **112**. In this manner, each of the positive layers and the positive terminal **60** of the capacitor **54** are electrically coupled via the positive fastener **56**. Additionally, the negative fastener **58** extends through the larger diameter **122** holes **124** in the internal negative layers **108**, such that the negative screw **58** electrically connected to each of the internal negative layers **108**. In this manner, each of the negative layers and the negative terminal **62** of the capacitor **54** are electrically coupled via the negative fastener **58**.

To facilitate maintaining electrical isolation between opposite polarity layers, as shown, the negative fastener **58** extends through the larger diameter **122** holes **124** of the positive layers, such that the negative fastener **58** is not electrically connected to any of the external positive layers **100** and the internal positive layer **112**. Correspondingly, the positive fastener **56** extends through the larger diameter **122** holes **124** of the internal negative layers **108** such that the positive fastener **56** is not electrically connected to any of the internal negative layers **108**. In this manner, the bus bar **52** may be implemented to create multiple parallel current paths.

In the illustrated embodiment, the positive layers **100**, **112** and the negative layers **108** are made of copper. However, the some or all of the conductive layers **100**, **108**, **112** may be made of copper alloys, or a different conductive material. Similarly, the insulation layers **104** may be made of mylar, epoxy, or any other any insulating, non-conductive material.

FIG. **5** illustrated a process **200** for manufacturing a bus bar **52**. In block **202**, the various conductive layers may be formed individually. In block **204**, the small diameter holes and large diameter holes may be formed (e.g., drilled) in each of the conductive layers as needed. For example, a small diameter hole and a large diameter hole may be drilled for each capacitor to which the bus bar is configured to couple. In block **206**, the insulation layers may be formed. Holes may or may not be formed in the insulation layers at this time. In block **208**, the bus bar may be assembled. In some embodiments, the bus bar may be assembled in a middle-out fashion such that insulation layers are coupled to either side of the internal positive layer. The negative layers may then be coupled to either of the insulation layers, followed by another pair of insulation layers, and then the external positive layers. In other embodiments, the bus bar may be assembled in a top-down or bottom-up fashion. For example, the various layers may be coupled to one another in the following order: external positive layer, insulation layer, negative layer, insulation layer, internal positive layer, insulation layer, negative layer, insulation layer, external positive layer. The various layers may be coupled to one another via laminating and plating processes.

Technical effects of the invention include by creating a number of parallel current paths through the bus bar, the stray inductance of the bus bar **52** may be reduced. The resultant bus bar, when paired with wide-band gap, high-speed switching devices, such as silicon carbide semiconductors, has a comparatively low stray inductance.

This written description uses examples to disclose the claimed subject matter, including the best mode, and also to enable any person skilled in the art to practice the disclosed subject matter, including making and using any devices or systems and performing any incorporated methods. The patentable scope of the disclosure is defined by the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal languages of the claims.

The invention claimed is:

1. A bus bar configured to electrically connect one or more electrical components, comprising:

an interior layer;

a first intermediate layer and a second intermediate layer electrically connected in parallel and disposed on opposite sides of the interior layer;

a first exterior layer electrically connected in parallel with the interior layer, wherein the first exterior layer and the interior layer are disposed on opposite sides of the first intermediate layer;

a second exterior layer electrically connected in parallel with the interior layer and the first exterior layer, wherein the second exterior layer and the interior layer are disposed on opposite sides of the second intermediate layer, wherein volume of the interior layer is different from volume of the first exterior layer and volume of the second exterior layer; and

a first terminal fastener extendinq through the bus bar and connecting to a first terminal of one of one or more capacitors, wherein the first terminal fastener contacts the interior layer and the exterior layers, connecting them in parallel, but does not contact the intermediate layers.

2. The bus bar of claim **1**, wherein the volume of the interior layer is, equal to a sum of the volume of the first exterior layer and the volume of the second exterior layer.

3. The bus bar of claim **1**, comprising a second terminal fastener extending through the bus bar and connecting to a second terminal of one of the one or more capacitors, wherein the second terminal fastener contacts the intermediate layers, connecting them in parallel, but does not contact the interior layer and the exterior layers.

4. The bus bar of claim **1**, wherein the bus bar is symmetrical about a plane extending through the interior layer and parallel to the first intermediate layer and the second intermediate layer.

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