(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 181 382 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
17.05.2023 Bulletin 2023/20

(21) Application number: **21207729.1**

(22) Date of filing: **11.11.2021**

(51) International Patent Classification (IPC):
H02M 7/217 *(2006.01)* *H02M 1/42* *(2007.01)*

(52) Cooperative Patent Classification (CPC):
H02M 1/4208; **H02M 7/2176**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(71) Applicant: **Infineon Technologies Austria AG**
9500 Villach (AT)

(72) Inventor: **FELDTKELLER, Martin**
81543 München (DE)

(74) Representative: **Sticht, Andreas**
Kraus & Weisert
Patentanwälte PartGmbB
Thomas-Wimmer-Ring 15
80539 München (DE)

(54) **POWER CONVERTER CONTROLLER, POWER CONVERTER AND METHOD**

(57) A controller for a power converter, a corresponding power converter and a corresponding method are provided. After reaching a first maximum voltage, power flowing is gradually reduced, and later the current provided to an output capacitor is gradually ramped up.

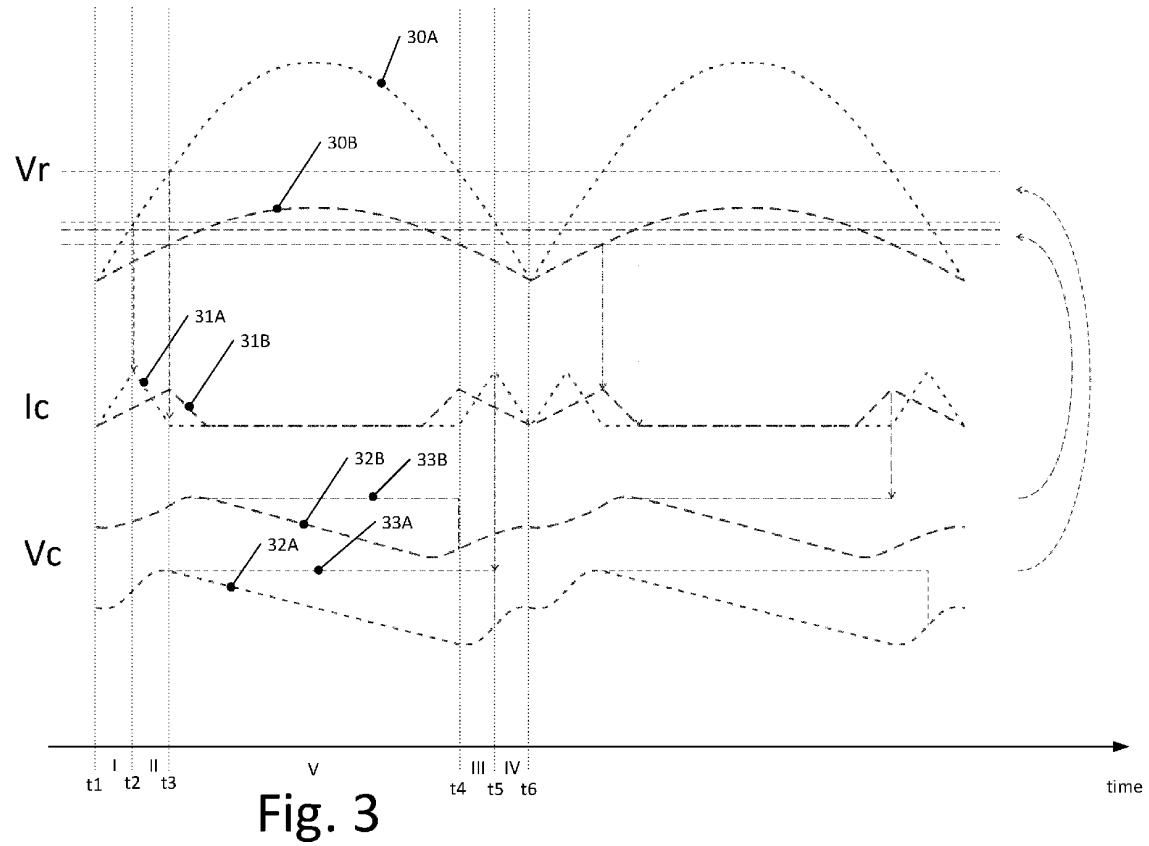

Fig. 3

EP 4 181 382 A1

Description

TECHNICAL FIELD

[0001] The present application relates to controllers for power converters, to power converters and to corresponding methods for operating such power converters.

BACKGROUND

[0002] Power converters are devices which convert an input electrical power (voltage and current) to an output electrical power (voltage and current), which may be required for a certain application. For example, to supply electrical appliances, power converters convert an AC (alternating current) input voltage like a mains voltage to a DC output voltage required for the corresponding appliance.

[0003] Depending on power consumption, various requirements regarding power factor correction (PFC), efficiency, galvanic isolation and the like may have to be met. The present application generally relates to power converters for low power, for example output power lower than 5 W, 2 W or lower than 1 W, where no galvanic isolation is required and efficiency is not the main issue. For those applications, typically costs and space requirement are major issues.

[0004] Various types of power converters are conventionally used for such applications. One type is referred to as non-isolated buck converter. In such a non-isolated buck converter, a control circuit is referenced to the source terminal of a buck switch used and has no direct access to the output terminals. Therefore, output voltage regulation may be quite inaccurate. This solution typically requires a high voltage input capacitor and a choke.

[0005] Another approach is sometimes referred to as "cap dropper" and uses a capacitor in series with input terminals receiving the input voltage. This capacitor takes most of the input voltage. A displacement current through the capacitor is rectified and used to generate an output voltage. The available current is limited and depends on the magnitude of the input voltage. A main disadvantage of this solution is that it requires a high voltage capacitor capable of operating under the input voltage, typically a comparatively high AC input voltage, over the lifetime of the power converter, including transients in the input voltage. This capacitor may be bulky and expensive.

[0006] A third solution is referred to as phase cut power supply. From a rectified sinusoidal input only portions are used where the input level voltage is below a threshold voltage. A low voltage output capacitor stores charge for times when the input voltage is higher and is not used.

[0007] Such phase cut power supplies require no inductive or high voltage component except the so-called phase cut switch, which separates the input voltage from the output capacitor when the input voltage is above the threshold, by switching off. Therefore, a required space is small and costs are comparatively low. The power efficiency is typically in the range of 10% to 40%, making it suitable for lower output powers, for example in a range from 300 mW to 500 mW. However, phase cut power supplies may have issues like generation of higher harmonics due to the switching off of the phase cut switch, control loop stability, efficiency and transient overvoltage robustness.

SUMMARY

[0008] A controller for a power converter as defined in claim 1, a power converter including such a controller as defined in claim 12 and a method as defined in claim 15 are provided. The dependent claims define further embodiments.

[0009] A controller for a power converter including a rectifier configured to receive an alternating current input signal and output rectified half waves, an output capacitor and a current control device coupled between the rectifier and the output capacitor is provided, wherein the controller is configured to control the current control device such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor up to a first maximum current value with a minimum on-resistance of the current control device;
(II) after reaching the first maximum current value, a current provided to the output capacitor via the current control device is gradually reduced;
(III) after the gradually reducing, the current provided to the output capacitor via the current control device is gradually ramped up to a second maximum current value, and
(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor with the minimum on-resistance of the current control device.

[0010] According to a further embodiment, a corresponding power converter including the rectifier, the output capacitor, the current control device and the above-mentioned controller is provided.

[0011] According to a further embodiment, a method for controlling a current control device of a power converter including a rectifier configured to receive an AC input signal and output rectified half waves, an output capacitor and the current control device coupled between the rectifier and the output capacitor is provided, wherein the method comprises controlling the current control device such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor up to a first maximum current value with a minimum on-resistance of the current

control device;

(II) after reaching the first maximum current value, a current provided to the output capacitor via the current control device is gradually reduced;

(III) after the gradually reducing, the current provided to the output capacitor via the current control device is gradually ramped up to a second maximum current value, and

(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor with the minimum on-resistance of the current control device.

[0012] The above summary is merely intended to give a brief overview of some embodiments is not to be construed as limiting in any way.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

Fig. 1 is a diagram illustrating a power converter according to an embodiment.

Fig. 2 is a flowchart illustrating a method according to an embodiment.

Fig. 3 is a diagram illustrating example voltages and currents for illustrating embodiments.

Fig. 4 is a diagram illustrating a control scheme according to some embodiments.

Figs. 5 to 8 are circuit diagrams illustrating power converters according to various embodiments.

DETAILED DESCRIPTION

[0014] In the following, various embodiments will be described in detail referring to the attached drawings. These embodiments are given by way of example only and are not to be construed as limiting. For example, while embodiments may be described as comprising a plurality of features (components, elements, method steps, devices, acts, events, etc.), in other embodiments some of these features may be omitted or may be replaced by alternative features. In addition to the features explicitly shown and described, other features, for example features used in conventional power converters like conventional phase cut power converters, may be used.

[0015] Features from different embodiments may be combined to form further embodiments. Modifications and variations described with respect to one of the embodiments are also applicable to other embodiments. For example, Figs. 6 to 8 describe different modifications of the embodiment of Fig. 5, and while these different modifications are described separately with respect to separate embodiments, two or more of these modifications may also be used in combination with each other.

[0016] Connections or couplings shown in the drawings or described herein refer to electrical connections or couplings unless noted otherwise. Such connections or couplings may be modified, for example by adding intervening elements or modifying elements, as long as the general purpose of the connection or coupling, for example to transmit a voltage or current or to transmit some information signal, is essentially maintained.

[0017] Turning now to the figures, Fig. 1 illustrates a power converter 10 according to an embodiment. Power converter 10, as will be described below in more detail, is a modification of a conventional phase cut converter.

[0018] Unlike conventional phase cut converters, in embodiments discussed herein a current from a rectifier to an output capacitor is not cut off abruptly, for example upon reaching a threshold input voltage, and then switched on abruptly again later, but is reduced or ramped up gradually. Gradually means that the absolute slope of the current is lower than a slope that would be present if a switching element like a transistor were switched off or on abruptly. For example, slopes of current over time when gradually decreasing or ramping up a current may be such that the duration of the gradually decreasing or ramping up is between 1% and 10% of the duration of a half wave of a rectified input voltage.

[0019] Power converter 10 receives an input voltage Vin and outputs an output voltage Vout. The input voltage Vin is provided to a rectifier 11, that provides a rectified voltage Vr. While a bridge rectifier using four diodes is illustrated in Fig. 1 as an example for rectifier 11, in other implementations other kinds of rectifiers, for example half wave rectifiers, may be used, for example for very low power applications, e.g. below 100mW output power. Input voltage Vin is an alternating current (AC) input voltage, for example a mains input voltage. Rectified voltage Vr then includes rectified half waves.

[0020] Power converter 10 of Fig. 1 furthermore includes a current control device 13 providing a current Ic to an output capacitor 14, at which the output voltage Vout can be tapped. The output voltage Vout corresponds to a voltage Vc at output capacitor 14. The current Ic generally depends on a resistance of current control device 13 and the voltage difference Vr-Vc according to Ohm's law. Current control device 13 may include a semiconductor device like a transistor. It should be noted that the resistance of current control device may have a non-linear behavior. For example, when a MOSFET transistor is used for implementation of current control device 13, the resistance may increase with current also in a fully switched on state according to a triode characteristic. In addition to a semiconductor device, current control device may include a passive ohmic resistor in series to such a semiconductor device, for example to protect the semiconductor device against overvoltages.

[0021] Current control device 13 is controlled by a phase cut controller 12. In contrast to conventional solu-

tions, where essentially a simple switch like a transistor switch which is only fully switched on or fully switched off is provided between a rectifier like rectifier 11 and an output capacitor like output capacitor 14, current control device 13 may be controlled to have a variable resistance, for example by operating a transistor above a threshold voltage, but below a voltage where the transistor is fully turned on (for example in a linear region) to provide gradually decreasing or rising currents, as will be explained further below.

[0022] As illustrated in Fig. 1, phase cut controller 12 may receive the rectified voltage Vr and the voltage at the output capacitor 14, Vc, and bases the control thereon. Examples for this control will now be explained further referring to Figs. 2 to 4.

[0023] Fig. 2 illustrates a method according to an embodiment, which may for example be implemented by phase cut controller 12 of Fig. 1 controlling current control device 13 accordingly. Fig. 3 shows example signals for illustrating the method of Fig. 3. Fig. 4 is a diagram for explaining the control further.

[0024] In Fig. 3, curves 30A and 30B illustrate two examples of the rectified input voltage Vr after rectifier 11 in the form of sinusoidal half waves. Curve 30A illustrates a higher input voltage, and curve 30B illustrates a lower input voltage.

[0025] Curves 31A and 31B illustrate corresponding examples of the current Ic provided via current control device 13, where curve 31A shows an example current of a rectified voltage Vr corresponding to curve 30A, and curve 31B shows a corresponding current Ic for curve 30B. Curves 32A and 32B show corresponding voltages Vc at output capacitor 14, where again curve 32A corresponds to curves 30A and 31A, and curve 32B corresponds to curves 30B and 31B.

[0026] It should be noted that the curves of Fig. 3 serve only as examples for illustration purposes, and depending on the implementation of phase cut controller 12, current control device 13 and on the magnitude of the input voltage Vin as well as depending on the implementation of rectifier 11 and output capacitor 14, curves may differ depending on implementation.

[0027] At 20, the method comprises providing a first part of each rectified half wave to the output capacitor up to a first maximum current value with a minimum on-resistance of the current control device. To illustrate, in Fig. 3, for curves 30A, 31A and 32A this corresponds to a phase I between times t1 and t2. Minimum on-resistance indicates that the current control device 13 is turned fully on. For example, a transistor is turned fully on, such that it has its (minimum) on-resistance Ron. Generally, each switch or similar device, even when switched on (i.e. conducting between its terminals), has some resistance left, which is referred to as the minimum on-resistance herein. This minimum on-resistance is not necessarily the theoretically obtainable minimum resistance, but the minimum resistance obtainable in practical use in a particular application. For example, the on-resistance of an n-channel depletion transistor, compared to an on-resistance at a gate source voltage Vgs=0, may be further reduced by applying a voltage Vgs>0. However, in many practical applications, Vgs=0 will be used, for example when no supply voltage above the source voltage is available. Therefore, the minimum on-resistance in this case corresponds to the on-resistance at Vgs=0. Further, the minimum on-resistance may also include an ohmic resistance of a resistor coupled in series to a semiconductor device, as mentioned above.

[0028] In this phase I, the current Ic therefore rises according to the rise in voltage difference Vr-Vc up to a first maximum current at time t2 for curve 31A. As in many cases a maximum of Vr is significantly larger than Vc, this may approximately correspond to a rise proportional to Vr. Similar considerations apply to curve 31B, where the current Ic also rises up to a first maximum current (different current than in case of curve 31A). It should be noted that phases I to V and times t1 to t6 are explicitly marked only for curves 30A, 31A, 32A and not curves 30B, 31B, 32B for clarity's sake.

[0029] Returning to Fig. 2, after reaching the first maximum current value, at 21 a current provided to the output capacitor is gradually reduced. This may be effected for example by gradually increasing a resistance of current control device 13. In some embodiments, this may be done until the current Ic reaches essentially zero or, in other words, the current control device 13 is completely switched off. An example for curve 31A is shown as a phase II between times t2 and t3, and is also shown in curve 31B, where after the maximum the current is gradually decreased to essentially zero, despite rising input voltage Vr. The control of the current control device 13 in this phase II may depend on the voltage Vc during phase II, and on the voltage Vr, both of which may be provided to phase cut controller 12 of Fig. 1 as already explained referring to Fig. 1.

[0030] After phase II of Fig. 3, in some embodiments after 21 a phase may follow where the current is essentially at zero. Essentially zero may mean smaller than currents through a resistive divider following rectifier 11, as will be explained with reference to Figs. 5 to 8, and may mean for example smaller than 100μA or smaller than 10μA. In Fig. 3, for curves 30A, 31A and 32A this phase is shown between times t3 and t4. In some other embodiments, phase III described next may immediately follow phase II at least in some situations, for example during startup, for a few half waves, and the current Ic may not go all the way down to zero, depending on the slopes of the current in phases II and III.

[0031] At 22 in Fig. 2, the current is gradually ramped up to a second maximum current value. As mentioned, for curves 30A, 31A and 33A this corresponds to a phase III between times t4 and t5. In particular, a resistance of current control device 13 during this phase may be gradually reduced until the minimum on-resistance Ron is reached at the second maximum threshold current. The control during this phase may be based on one or more

values of Vc during phase II, in particular a maximum value as indicated by lines 33A, 33B in Fig. 3, and on the voltage Vr. In some embodiments, the absolute value of the slope during phase II may be similar to the absolute value of the slope during phase III, for example within ± 5%, ± 10%, ± 15% or ± 20%.

[0032] Likewise, the first maximum current may be similar to the second maximum current, for example within ± 5%, ± 10%, ± 15% or ± 20%.

[0033] After reaching the second maximum current value, at 23 the method of Fig. 2 comprises providing a last part of each rectified half wave, i.e. a part until the end of the respective rectified half wave, to the output capacitor with the minimum on-resistance of the current control device. This corresponds, for curves 30A, 31A and 32A, to a phase IV in Fig. 3 between times t5 and t6, where the voltage Vr goes down to zero, and the current Ic essentially follows this Voltage and goes down to zero, linked by the minimum on-resistance Ron. After this, a next cycle starts, i.e. the method of Fig. 2 resumes at 20. However, Fig. 3 is a slight approximation as mentioned above. As the current Ic actually depends on Vr - Vc, There may be a slight "current gap" between the cycles, during a time when Vr drops below Vc. During this time, Ic is essentially at zero, a negative current Ic being prevented by rectifier 11.

[0034] The duration of phases II and III above may be between 1% and 10% of the duration of a half wave of Vr, but is not limited thereto.

[0035] Next, some details of the control of the current control device used in some embodiments will be discussed.

[0036] In some embodiments, the absolute value of the slope of the current Ic over time during phase II may be greater than the absolute value of the slope during phase I, and similarly the absolute value of the slope during phase III may be greater than the absolute value of the slope during phase IV. Furthermore, as mentioned the control during phase III may be based on a value of Vc during phase II. For example, a maximum value or also a plurality of values may be stored, and the stored value may be used to control the current control device during phase III, for example such that Vc follows a predefined control curve. In particular, the amount of current provided to the output capacitor inter alia during phase II determines the voltage at the output capacitor and its maximum, and therefore based on the maximum of Vc a similar, but mirrored current waveform may be provided during phase III. It should be noted that by storing a plurality of values of Vc, the "mirroring" may be more exact, but a stability of the corresponding control may be less. Therefore, in embodiments only the maximum value may be used, which still may give an approximately mirrored current waveform, but with higher loop stability in some embodiments. The way the current is reduced in phase II may for example be based on parametric modification of a stored control curve, which is selected based on the behavior of Vc in phase II and the input voltage Vr. The transition from phase I to phase II occurs when the current through the current control device 13 having a minimum on-resistance exceeds the current given by a control curve, which is generated also during phase I. During phase I the current is dominated by the minimum on-resistance, during phase II by the control curve.

[0037] A scheme for corresponding control curves will now further be explained referring to Fig. 4.

[0038] In the diagram of Fig. 4, various control curves are illustrated as current Ic depending on rectified input voltage Vr-Vc, where the control curve may be selected based on capacitor voltage Vc.

[0039] A curve 40 in Fig. 4 illustrates the behavior at the minimum on-resistance Ron of the current control device 13, corresponding to phases I and IV of Fig. 3. Here, the current Ic is determined by voltage Vr-Vc and the on-resistance Ron.

[0040] A family of curves 41 gives the current Ic over voltage Vr when the current is gradually reduced or ramped up, i.e. in phases II and III. A curve from family of curves 41 is selected based on the storage capacitor peak voltage, as indicated by lines 33B, 33A in Fig. 3, where for increasing storage capacitor peak voltage steeper curves are selected, as indicated by an arrow 42 in Fig. 4. A control of the current control device is then performed accordingly, for example by controlling a transistor accordingly to have a corresponding resistance. The current Ic actually provided is then the smaller one of a current given by curve 40 and a current given by the selected curve of the family of curves 41. This means that for example the maximum current (first maximum current or second maximum current above) may correspond to the current Ic at the crossing point between curve 40 and the selected one of family of curves 41.

[0041] Family of curves 41 may have a common crossing point on the y-axis (current axis), although this need not be the case. Furthermore, while the family of curves 41 is shown as linear functions in Fig. 4 and also in phases II and III of Fig. 3, this is not to be construed as limiting, and other continuous curves, for example continuous piecewise linear curves or other nonlinear continuous curves, may also be used. By the control thus implemented, a jump-like dependency of the current Ic from the applied voltage Vr may be avoided, in contrast to conventional phase cut controllers.

[0042] In some embodiments, phase cut controller 12 may be implemented as a microcontroller or similar processor device programmed accordingly to perform the respective control. Other implementations may use dedicated hardware components, in particular mostly analog hardware components, to implement phase cut controller 12. In this way, the power supply shown may be used to supply devices like devices including microcontrollers with power, without requiring a microcontroller for control itself. Example implementations will now be described referring to Figs. 5 to 8. Components and elements already discussed with respect to the previous figures will not be described again in detail.

[0043] In Fig. 5, a current control device is implemented by a depletion transistor 51. Depletion transistor 51 is dimensioned depending on a maximum expected voltage difference Vr-Vc across its source and drain terminals. For example, the input voltage Vin may be a mains voltage of 240 VAC, 220 VAC or 110 VAC, and thus Vr may also have peaks in that order, and Vc may be of the order of a few Volt, such that depletion transistor 51 may be a high voltage transistor capable of handling voltages of 500 V and more. In some embodiments (not shown) in Fig. 5, a series resistor may be coupled to transistor 51 to limit the current Ic. Such a series resistor then contributes to the overall minimum on-resistance of the current control device.

[0044] The voltage Vr is provided to the control circuit shown using a first resistive voltage divider including resistors 55, 56. Resistors 55, 56 are designed such that following elements like a differential amplifier 513 may be designed for lower voltages than Vr. Likewise, voltage Vc is provided via a second resistive divider including resistors 57, 58. Resistors 55 to 58 are high-ohmic resistors to reduce losses due to current flow via the dividers. For example, the overall series resistance of resistors 55, 56 or of resistors 57, 58 may be in the Megaohm range.

[0045] Transistor 51 is generally controlled by a control loop 50. In the control loop, a differential amplifier 54 receives a measure of the current Ic measured by a current detector 517 at a positive input and a reference voltage ref on a negative input and controls a current source 53, which applies a gate voltage to transistor 51. "Measure of the current Ic" refers to a signal which is at least approximately proportional to current Ic. Current detector 517 may for example be implemented using a shunt resistor, a current mirror, a magnetoresistive detector like a hall sensor or any other conventional current detector. Furthermore, current source 53 is connected to a source terminal of transistor 51 via a resistor 52, such that using current source 53 a gate source voltage is applied to transistor 51, to switch transistor 51 fully on (minimum on-resistance), off (essentially electrical isolation between source and drain) or operate transistor 51 in a regime inbetween to regulate the resistance and therefore current Ic.

[0046] Reference voltage ref is determined based on voltage Vr received by the controller via voltage divider 55, 56 and voltage Vc received by the controller via voltage divider 57, 58.

[0047] The divided voltage Vr from resistive voltage divider 55, 56 is provided to a positive input of a differential amplifier 513, and a reference voltage represented by a voltage source 514 is provided to a negative input of differential amplifier 513. This reference voltage generates an offset to differential amplifier 513. In an embodiment, the offset corresponds to a nominal voltage of output capacitor 14, divided by the divider ratio of resistive divider 55, 56. Instead of the reference voltage, another resistive divider with the same ratio may be used. For example, resistive dividers 55, 56 and 57, 58 may be implemented in the same manner (using the same resistance values or ratios), and in this case the node between resistors 57, 58 may be directly coupled to the negative input of differential amplifier instead of voltage source 514. The output of differential amplifier 513 is a signal which is approximately proportional to the voltage across transistor 51, i.e. Vr-Vc. This output is fed as numerator (N) to a divider 512.

[0048] The output of resistive divider 57, 58 is provided to a peak detector 59, which detects a peak in the divided voltage Vc, corresponding to the detection of the peak in Vc indicated by lines 33A, 33B of Fig. 3. Peak detector 59 is reset by a level detector 516. Level detector 516 receives the output signal of differential amplifier 54 and is configured to output a reset signal if the output of differential amplifier 54 corresponds to a control setting transistor 51 to a minimum on-resistance (i.e. phases I and IV of Fig. 3). As long as the peak detector 59 is reset, the output of peak detector 59 follows its input. The output of peak detector 59 is provided to a negative (inverting) input of a differential amplifier 510. A reference voltage represented by a voltage source 511 is provided to the positive input of differential amplifier 510. The output of differential amplifier 510 represents a difference between the voltage Vc and a maximum allowed output capacitor voltage which should not be exceeded, which may for example be a maximum operating voltage of a circuit receiving the voltage Vout. This maximum allowed voltage is represented by the reference voltage provided by voltage source 511. The output of differential amplifier 510 is fed as denominator (D) to divider 512. The output of divider 512 is provided to a function generator 515 which generates the reference voltage to provide a control function as by curve family 41. As mentioned, this function may for example be a piecewise linear function.

[0049] For example, for implementing function generator 513, the output signal of divider 512 may be a current signal. From this signal, a constant current may be subtracted, for example by adding a constant current with opposite polarity provided by a current source. From the thus resulting combined current only positive values are further used. This only positive current is subtracted from a reference current to obtain the output signal ref of function generator 515 that decreases with increasing input signal and is limited to a maximum value corresponding to the reference current. In case ref is a current signal, also current detector 517 is configured to provide a current signal, and differential amplifier 54 is configured to compare two current signals.

[0050] With respect to Figs. 6 to 8, now variations to the embodiment of Fig. 5 will be described. Components corresponding to components of Fig. 5 bear the same reference numerals and will not be described again. Instead, only the differences of the respective embodiments of Figs. 6 to 8 compared to the embodiment of Fig. 5 will be described. In Fig. 6, instead of providing an analog peak detector 59, a digital implementation is used.

In Fig. 6, the voltage Vc divided by resistive divider 57, 58 is provided to a negative (inverting) input of a differential amplifier 600, and a reference voltage generated by a voltage source 601 is provided to a positive input of differential amplifier 600. The function of differential amplifier 600 and voltage source 601 corresponds to the function of differential amplifier 510 and voltage source 511 in Fig. 5, with the difference that in Fig. 5 differential amplifier 510 is provided downstream of peak detector 59, whereas in Fig. 6 the peak detection occurs downstream of differential amplifier 600.

[0051] An output of differential amplifier 600 is provided to a logarithmic analog-to-digital converter 602, which generates a digital code that represents the logarithm of the input voltage. For example, depending on implementation of logarithmic analog-to-digital converter 602 and the encoding used, an inverter for each bit line may need to be provided, represented by inverter 603. Downstream of inverter 603 a digital peak detector 604 is provided. Alternatively to inverter 603 and (maximum) peak detector 604, in other implementations a digital minimum detector may be provided, and inverter 603 may be omitted. Peak detector 604, apart from being realized in the digital domain, has the same functionality as peak detector 59 of Fig. 5 and is reset based on the output signal of level detector 516. In contrast to analog implementations, a digital implementation of peak detector 604 (or a minimum detector) has no constraints regarding a hold time.

[0052] The output of peak detector 604 is then converted to an analog signal by an exponential multiplying digital-to-analog converter (DAC) 605. This DAC 605 multiplies the signal output by differential amplifier 513, which represents the voltage drop across transistor 51, with a factor that exponentially depends on the digital value output by peak detector 604. This may provide a similar function as divider 512. The output of DAC 605 is provided to function generator 515 already discussed with reference to Fig. 5.

[0053] Fig. 7 illustrates a further variation of the embodiment of Fig. 5. Generally, the efficiency of the power converters discussed herein decreases for lower output voltages, as a smaller part of the half waves of the voltage Vr may be used. In some cases, therefore, a two-stage conversion may be more efficient, where the power converter of Fig. 1, 5 or 6 generates a higher output voltage Vout than required by an application, and then an additional DC (direct current)/DC converter is used to downconvert this voltage. This is illustrated in Fig. 7, where the output voltage Vout is provided to a switched capacitor DC/DC converter. Switched capacitor DC/DC converter may be followed by a linear post regulator 71 to generate a required output voltage Vout2. As switched capacitor DC/DC converters and post regulators are conventional devices, they will not be described in further detail here.

[0054] To give a numerical example, when for example the components of the control loop are designed for voltages up to 30 V, an output voltage Vout close to 30 V may be generated. For example, the power converter may be designed to keep Vout in a range between 24 to 30 V including ripple. A 6:1 switched capacitor DC/DC converter may then be used to downconvert the voltage to a range between 4 V and 6 V, which could then be regulated to 3.3 V by linear post regulator 71. In this case, the average input current is only one sixth of a solution without the switched capacitor DC/DC converter 70 (i.e. directly providing Vout in the required range), which makes it easier to design the power converter for lower harmonic generation at better efficiencies.

[0055] Fig. 8 illustrates a further addition to the embodiment of Fig. 5. Generally, electronic power supplies as the power converters illustrated in Figs. 5 to 8 may be required to survive line surges in the input voltage Vin. For example, if Vin is a mains voltage, such line surges may be induced by lightning strikes into the power grid. In most cases discrete protection circuits are needed which use bulky components. These components remain bulky even if the total power of a connected electronic supply is only a few Watts or even less. Most technologies suitable to build a power converter as illustrated in Figs. 5 to 7 can handle voltages up to 600 V or 700 V. If such a supply could handle 1,200 V, protection against line surges would be easier.

[0056] The embodiment of Fig. 8 uses an additional depletion transistor 80 in series with transistor 51. To avoid having a voltage drop of 1,200 V on one chip, transistor 80 may be a discrete component separate from the remaining phase cut power supply, or may be provided on a separate chip die and integrated in a same package. During normal operation, transistor 80 is always on with its minimum on-resistance and therefore essentially does not influence operation of the power supply. In case of a surge in the input voltage, this is detected via resistive divider 55, 56, a differential amplifier 83, a transistor 82 controlled by differential amplifier 83 and a resistor 81 to keep depletion transistor 80 conducting when transistor 82 is off. To this end, differential amplifier 83 compares the divided voltage Vr to a reference voltage generated by a voltage source 84, and if the divided voltage Vr exceeds the reference voltage indicating a surge, a current flowing through transistor 82 causes a voltage drop across resistor 81 causing a negative gate source voltage at transistor 80, causing transistor 80 to be fully or partially switched off. Furthermore, at a high voltage (see Fig. 3) also transistor 51 is switched off. It should be noted that resistive divider 55, 56 in this case is used twice, once for controlling transistor 80 and once for the already described control loop controlling transistor 51. In other embodiments, separate dividers may be provided.

[0057] It should be noted that the arrangement of components 55, 56 and 80 to 84 is also capable of regulating the voltage Vr during an overvoltage input (surge of Vin) to a value that corresponds to the reference voltage generated by voltage source 84 multiplied by the inverse divider ratio of resistive divider 55, 56. This causes a

distribution of the overvoltage between transistors 51 and 80, such that a probability of damage by the overvoltage is reduced.

[0058] Furthermore, as already mentioned the modifications shown in Figs. 6 to 8 may be combined. For example, also in Figs. 6 and 8 switched capacitor DC/DC converter 70 and linear post regulator 71 may be provided, and the surge protection illustrated with respect to Fig. 8 may also be provided to the power converters of Figs. 6 and 7, etc.

[0059] Some embodiments are defined by the following examples:

Example 1. A controller for a power converter, the power converter including a rectifier configured to receive an alternating current input signal and output rectified half waves, an output capacitor, and a current control device coupled between the rectifier and the output capacitor, wherein the controller is configured to control the current control device such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor up to a first maximum current value with a minimum on resistance of the current control device ;

(II) after reaching the first maximum current value, a current provided to the output capacitor via the current control device is gradually reduced,

(III) after the gradually reducing, the current provided to the output capacitor via the current control device is gradually ramped up to a second maximum current value,
and

(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor with the minimum on resistance of the current control device.

Example 2. The controller of example 1, wherein the controller, in (II), is configured to control the current control device based on the output voltage of the rectifier and the capacitor voltage at the output capacitor during (II) .

Example 3. The controller of example 1 or 2, wherein the controller, in (III), is configured to control the current control device based on the output voltage of the rectifier and at least one value of the capacitor voltage of the output capacitor during (II).

Example 4. The controller of example 3, wherein the at least one value comprises a maximum value.

Example 5. The controller of any one of examples 1 to 4, wherein the first maximum current value is equal to the second maximum current value to within +/-20%.

Example 6. The controller of any one of examples 1 to 5, wherein the controller is configured to control the current control device to maintain the current at a minimum value between the gradually reducing and the gradually ramping up.

Example 7. The controller of example 6, wherein the minimum value is essentially zero.

Example 8. The controller of any one of examples 1 to 7, wherein an absolute value of a slope of the current when ramping up the current is equal to an absolute value of a slope when gradually decreasing the current to within +/-20%.

Example 9. The controller of any one of examples 1 to 8, wherein the controller is configured to increase an absolute value of a slope of the current when ramping up the current and a slope when gradually decreasing the current with increasing peak voltage across the output capacitor.

Example 10. The controller of any one of example 1 to 9, wherein the controller comprises:

a current source coupled to the control terminal of the current control device,
a differential amplifier, wherein a first input of the differential amplifier is configured to receive a signal corresponding to the current flowing from the current control device to the output capacitor, an output of the differential amplifier is configured to control the current source, and a second input of the differential amplifier is configured to receive a reference value from a reference value generating circuit.

Example 11. The controller of example 10, wherein the reference value generating circuit comprises:

a voltage divider coupled to the output capacitor to output a divided voltage,
a further differential amplifier configured to receive the divided voltage and a further reference voltage,
a logarithmic analog to digital converter coupled to the output of the further differential amplifier to provide a stream of digital values,
a peak detector configured to detect a peak value in the stream of digital values, and
circuitry configured to generate the reference value based on the peak value.

Example 12. The controller of example 11, wherein the circuitry configured to generate the reference value comprises:

an exponential multiplying digital to analog converter configured to receive the peak value and a multiplication reference based on an output voltage of the rectifier, and
a function generator configured to generate the reference value based on a falling transfer function and based on the output of the digital to analog converter.

Example 13. The controller of example 10, wherein the reference value generating circuit comprises:

a voltage divider coupled to the output capacitor to output a divided voltage,
a peak detector configured to detect a peak value in the divided voltage,
a further differential amplifier configured to receive the peak value and a further reference voltage,
circuitry configured to generate the reference value based on an output of the further differential amplifier.

Example 14. The controller of example 13, wherein the circuitry configured to generate the reference value comprises:

a divider configured to receive the output of the further differential amplifier as denominator and numerator based on an output voltage of the rectifier, and
a function generator configured to generate the reference value based on a falling transfer function and based on the output of the divider.

Example 15. The controller of any one of examples 1 to 14, wherein the current over time in (I) to (IV) is a continuous function.

Example 16. A power converter, comprising:

the controller of any one of examples 1 to 15,
the rectifier configured to receive an alternating current input signal and output rectified half waves,
the output capacitor, and
the current control device coupled between the rectifier and the output capacitor.

Example 17. The power converter of example 16, wherein the current control device comprises a transistor, wherein a first terminal of the transistor is coupled to the rectifier, a second terminal of the transistor is coupled to the output capacitor and a control terminal of the transistor is coupled to the controller.

Example 18. The power converter of example 16 or 17, comprising a further transistor coupled in series to the transistor to provide protection against line transients.

Example 19. The power converter of any one of examples 16 to 18, further comprising a direct current/direct current power converter coupled to the output capacitor to generate a further output voltage based on the output voltage.

Example 20. A method for controlling a current control device of a power converter including a rectifier configured to receive an alternating current input signal and output rectified half waves, an output capacitor and the current control device coupled between the rectifier and the output capacitor, wherein the method comprises controlling the current control device such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor up to a first maximum current value with a minimum on-resistance of the current control device ;
(II) after reaching the first maximum current value, a current provided to the output capacitor via the current control device is gradually reduced;
(III) after the gradually reducing, the current provided to the output capacitor via the current control device is gradually ramped up to a second maximum current value, and
(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor with the minimum on-resistance of the current control device.

Example 21. The method of example 20, comprising, in (II), controlling the current control device based on the output voltage of the rectifier and the capacitor voltage at the output capacitor during (II).

Example 22. The method of example 20 or 21, wherein the method, in (III), comprises controlling the current control device based on the output voltage of the rectifier and at least one value of the capacitor voltage of the output capacitor during (II).

Example 23. The method of example 22, wherein the at least one value comprises a maximum value.

Example 24. The method of any one of examples 20 to 23, wherein the first maximum current value is

equal to the second maximum current value to within +/-20%.

Example 25. The method of any one of examples 20 to 24, further comprising controlling the current control device to maintain the current at a minimum value between the gradually reducing and the gradually ramping up.

Example 26. The method of example 25, wherein the minimum value is essentially zero.

Example 27. The method of any one of examples 20 to 26, wherein an absolute value of a slope of the current when ramping up the current is equal to an absolute value of a slope when gradually decreasing the current to within +/-20%.

Example 28. The method of any one of examples 20 to 27, wherein the method comprises increasing an absolute value of a slope of the current when ramping up the current and a slope when gradually decreasing the current with increasing peak voltage across the output capacitor.

[0060] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

Claims

1. A controller (12) for a power converter (10), the power converter (10) including a rectifier (11) configured to receive an alternating current input signal (Vin) and output rectified half waves, an output capacitor (14), and a current control device (13, 51) coupled between the rectifier (11) and the output capacitor (14),
wherein the controller (12) is configured to control the current control device (13, 51) such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor (14) up to a first maximum current value with a minimum on resistance of the current control device (13, 51);
(II) after reaching the first maximum current value, a current (Ic) provided to the output capacitor (14) via the current control device (13, 51) is gradually reduced,
(III) after the gradually reducing, the current (Ic) provided to the output capacitor (14) via the current control device (13, 51) is gradually ramped up to a second maximum current value,
and
(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor (14) with the minimum on resistance of the current control device (13, 51).

2. The controller (12) of claim 1, wherein the controller (12), in (II), is configured to control the current control device (13, 51) based on the output voltage (Vr) of the rectifier (11) and the capacitor voltage (Vc) at the output capacitor (14) during (II).

3. The controller (12) of claim 1 or 2, wherein the controller (12), in (III), is configured to control the current control device (13, 51) based on the output voltage (Vr) of the rectifier (11) and at least one value of the capacitor voltage (Vc) of the output capacitor (14) during (II) .

4. The controller (12) of claim 3, wherein the at least one value comprises a maximum value.

5. The controller (12) of any one of claims 1 to 4, wherein the first maximum current value is equal to the second maximum current value to within +/-20%.

6. The controller (12) of any one of claims 1 to 5, wherein the controller (12) is configured to control the current control device (13, 51) to maintain the current at a minimum value between the gradually reducing and the gradually ramping up.

7. The controller (12) of claim 6, wherein the minimum value is essentially zero.

8. The controller (12) of any one of claims 1 to 7, wherein an absolute value of a slope of the current (Ic) when ramping up the current (Ic) is equal to an absolute value of a slope when gradually decreasing the current (Ic) to within +/- 20%.

9. The controller (12) of any one of claims 1 to 8, wherein the controller (12) is configured to increase an absolute value of a slope of the current (Ic) when ramping up the current and a slope when gradually decreasing the current (Ic) with increasing peak voltage across the output capacitor (14) .

10. The controller (12) of any one of claim 1 to 9, wherein the controller (12) comprises:

a current source (53) coupled to the control ter-

minal of the current control device (13, 51),
a differential amplifier (54), wherein a first input of the differential amplifier is configured to receive a signal corresponding to the current flowing from the current control device (13, 51) to the output capacitor (14), an output of the differential amplifier (54) is configured to control the current source (53), and a second input of the differential amplifier (54) is configured to receive a reference value (ref) from a reference value generating circuit (55 - 516).

11. The controller (12) of claim 10, wherein the reference value generating circuit (55 - 516) comprises:

a voltage divider (57, 58) coupled to the output capacitor (14) to output a divided voltage,
a further differential amplifier (600) configured to receive the divided voltage and a further reference voltage (601),
a logarithmic analog to digital converter (602) coupled to the output of the further differential amplifier (600) to provide a stream of digital values,
a peak detector (604) configured to detect a peak value in the stream of digital values, and
circuitry (513-515, 605) configured to generate the reference value based on the peak value.

12. A power converter (10), comprising:

the controller (12) of any one of claims 1 to 11,
the rectifier (11) configured to receive an alternating current input signal and output rectified half waves,
the output capacitor (14), and
the current control device (13, 51) coupled between the rectifier and the output capacitor.

13. The power converter (10) of claim 12, wherein the current control device (13, 51) comprises a transistor (51), wherein a first terminal of the transistor (51) is coupled to the rectifier (11), a second terminal of the transistor (51) is coupled to the output capacitor (14) and a control terminal of the transistor (51) is coupled to the controller (12) .

14. The power converter (10) of any one of claims 12 or 13, further comprising a direct current/direct current power converter (70) coupled to the output capacitor (14) to generate a further output voltage (Vout2) based on the output voltage (Vout).

15. A method for controlling a current control device (13, 51) of a power converter (10) including a rectifier (11) configured to receive an alternating current input signal (Vin) and output rectified half waves, an output capacitor (14) and the current control device (13, 51) coupled between the rectifier and the output capacitor,
wherein the method comprises controlling the current control device (13, 51) such that:

(I) a first part of each rectified half wave starting from the beginning of each rectified half wave is provided to the output capacitor (14) up to a first maximum current value with a minimum on-resistance of the current control device (13, 51);
(II) after reaching the first maximum current value, a current (Ic) provided to the output capacitor (14) via the current control device (13; 51) is gradually reduced;
(III) after the gradually reducing, the current (Ic) provided to the output capacitor (14) via the current control device (13, 51) is gradually ramped up to a second maximum current value, and
(IV) after a second maximum current value is reached, a last part of each rectified half wave ending with the end of each rectified half wave is provided to the output capacitor (14) with the minimum on-resistance of the current control device (13, 51).

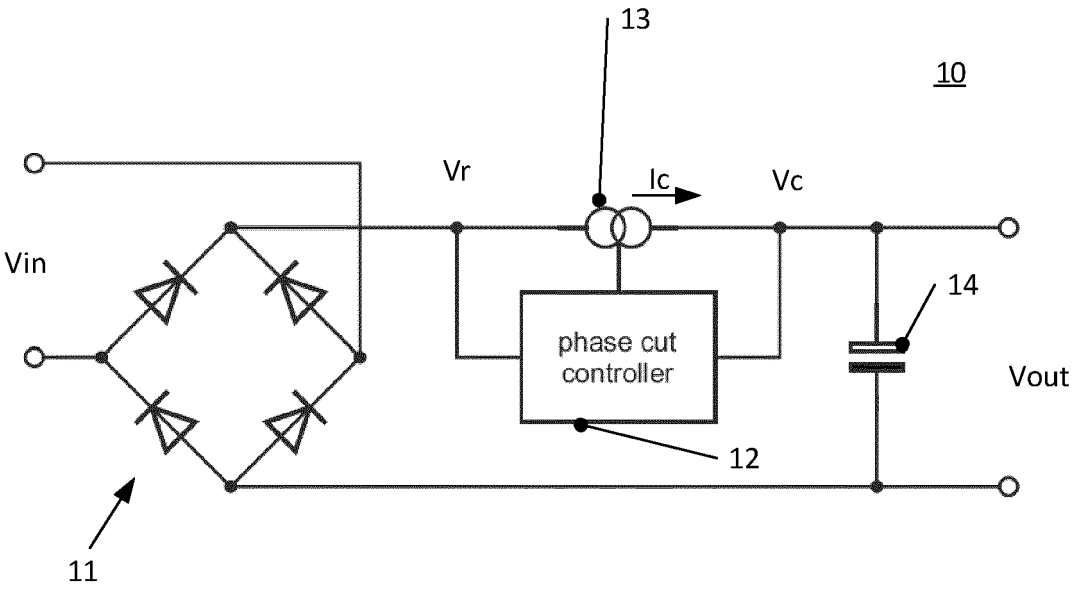
13
10
Vr
Ic
Vc
Vin
14
phase cut controller
Vout
12
11

Fig. 1

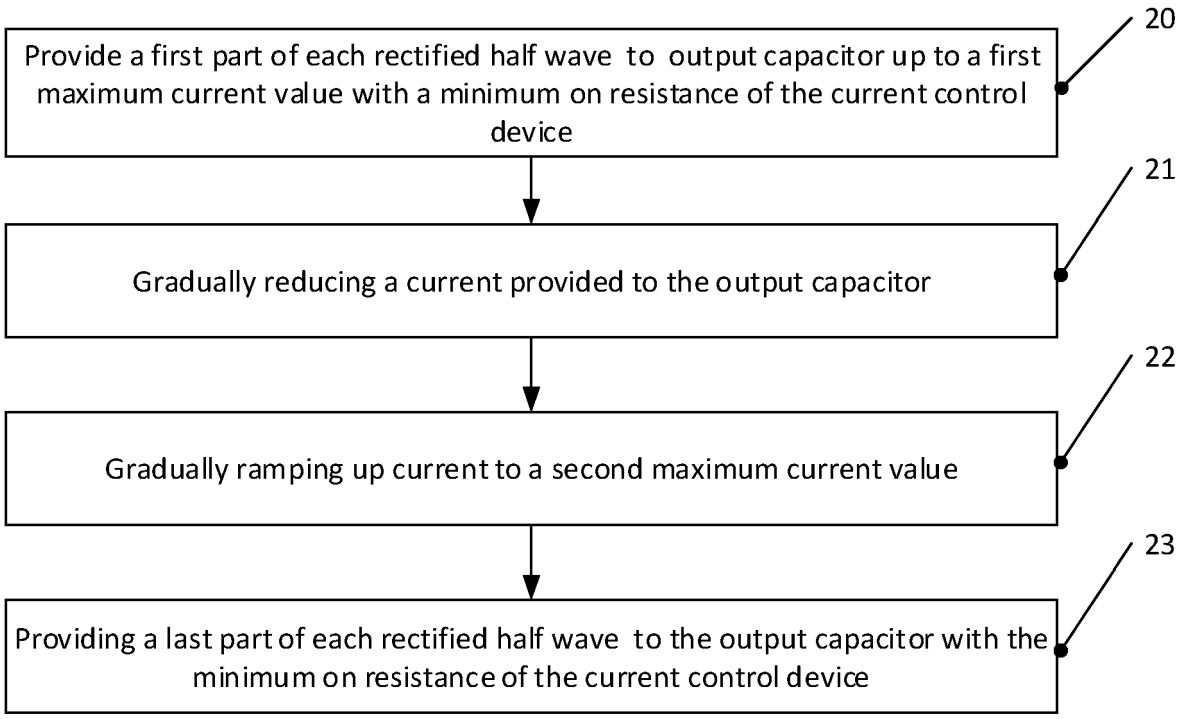
Provide a first part of each rectified half wave to output capacitor up to a first maximum current value with a minimum on resistance of the current control device
20
Gradually reducing a current provided to the output capacitor
21
Gradually ramping up current to a second maximum current value
22
Providing a last part of each rectified half wave to the output capacitor with the minimum on resistance of the current control device
23

Fig. 2

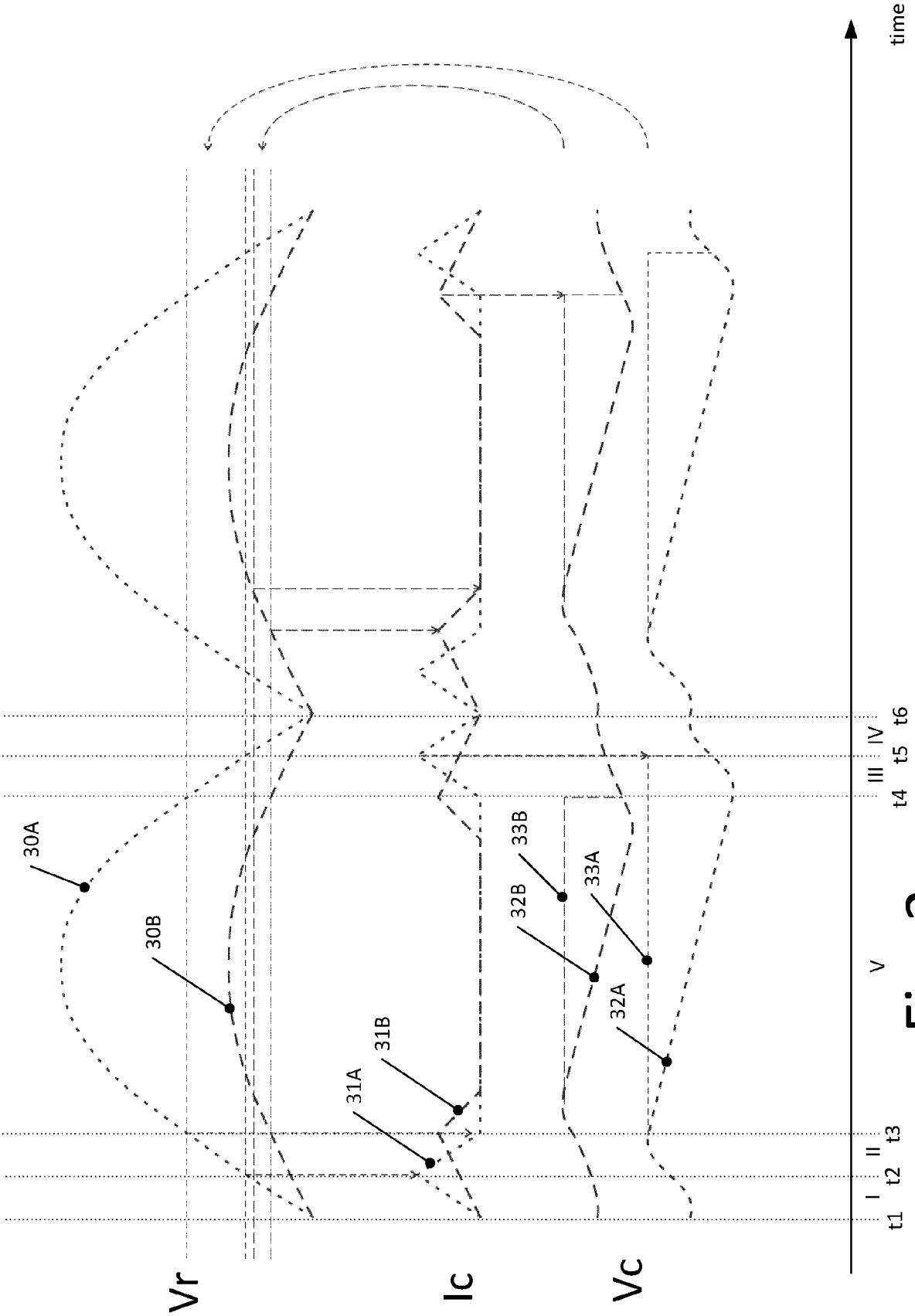
time
Vr
Ic
Vc
30A
30B
31A
31B
32A
32B
33A
33B
I
II
III
IV
V
t1
t2
t3
t4
t5
t6

Fig. 3

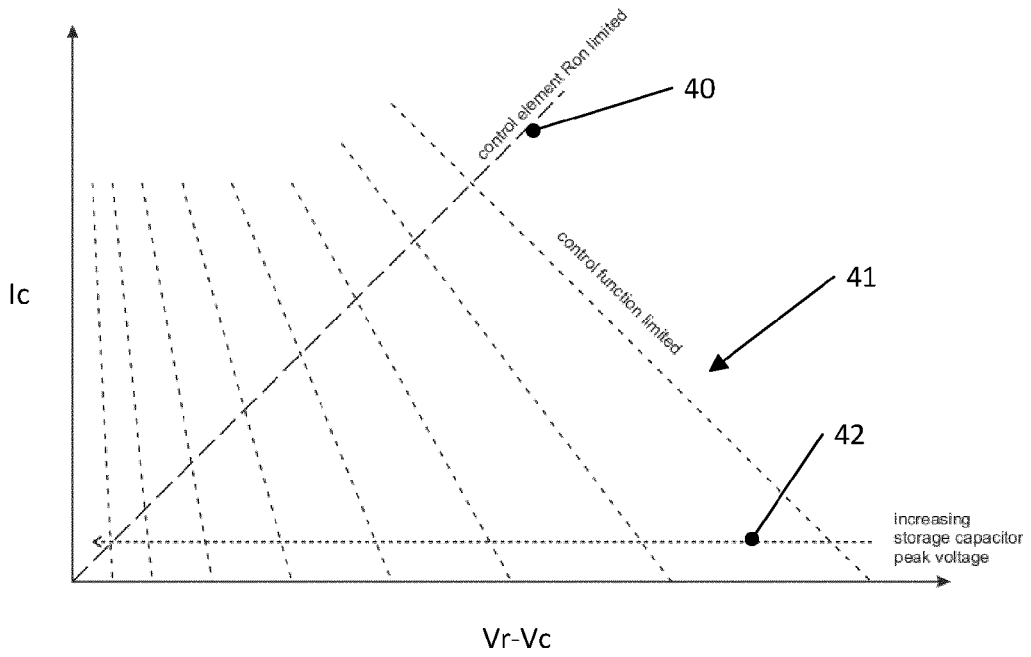
control element Ron limited
40
control function limited
41
42
Ic
increasing
storage capacitor
peak voltage
Vr-Vc

Fig. 4

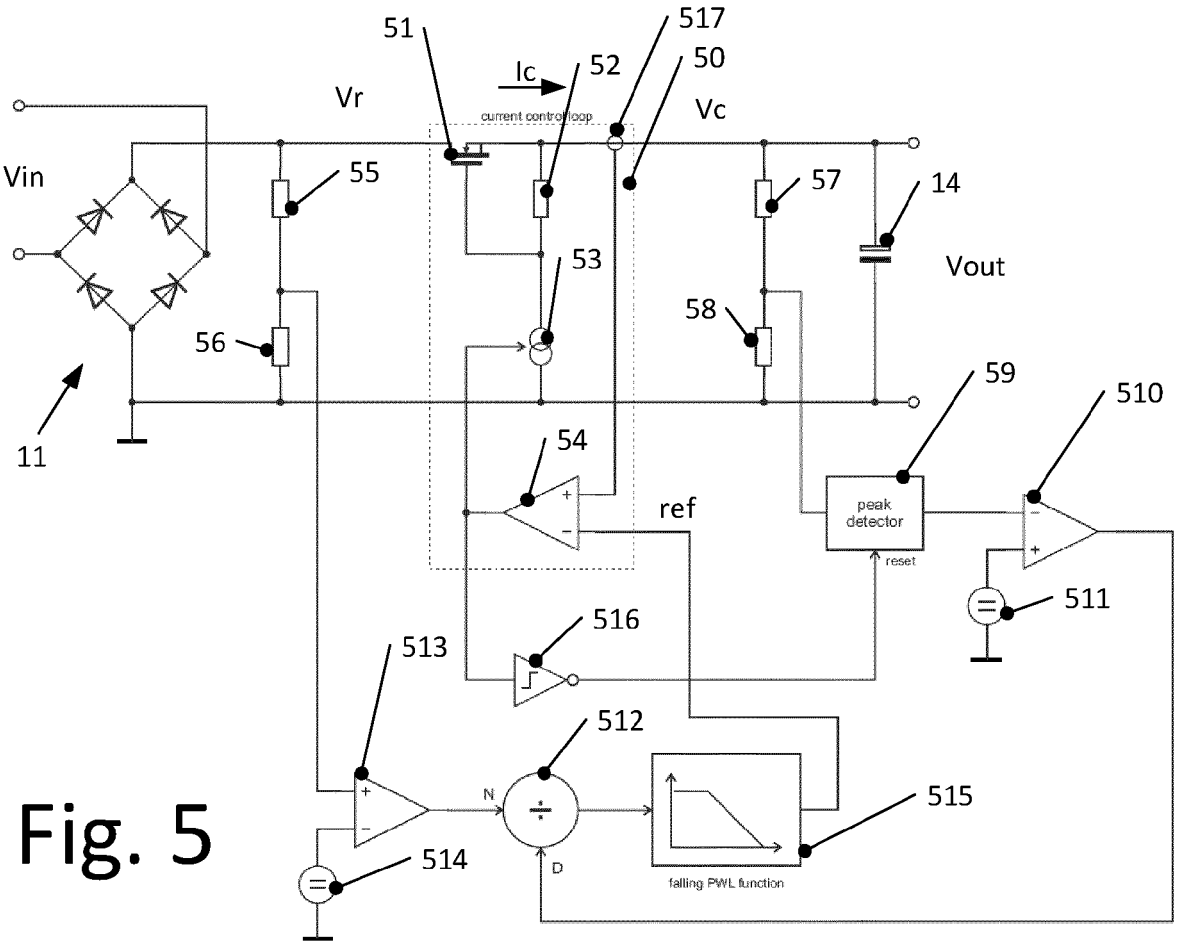
51
517
Ic
52
50
Vr
current control loop
Vc
Vin
55
57
14
Vout
53
58
56
59
510
54
ref
peak
detector
reset
511
516
513
512
N
515
514
D
falling PWL function
11

Fig. 5

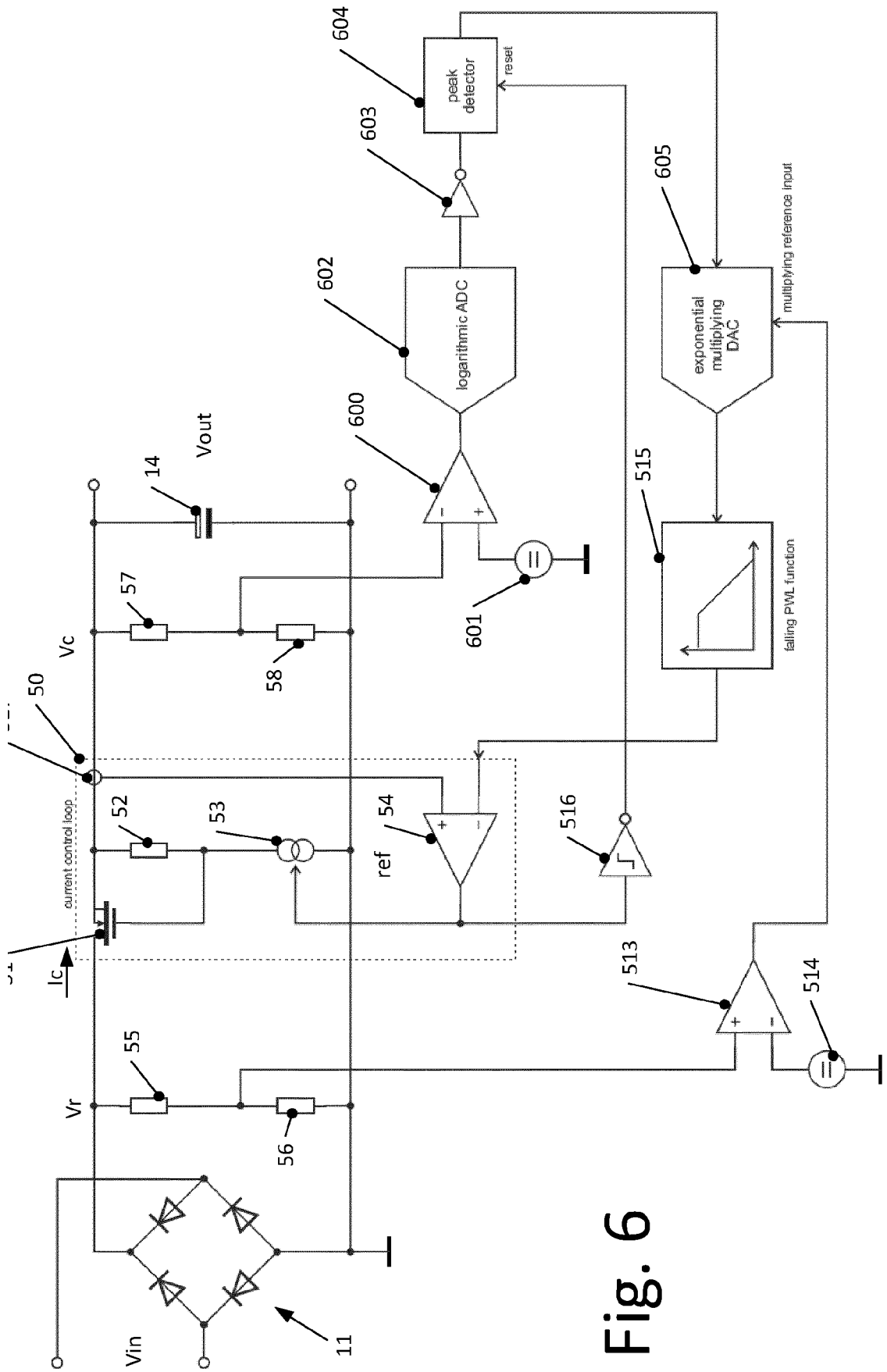
604
peak detector
reset
603
602
logarithmic ADC
605
exponential multiplying DAC
multiplying reference input
600
Vout
14
515
601
57
58
Vc
50
falling PWL function
current control loop
52
53
54
ref
516
Ic
513
514
55
Vr
56
Vin
11

Fig. 6

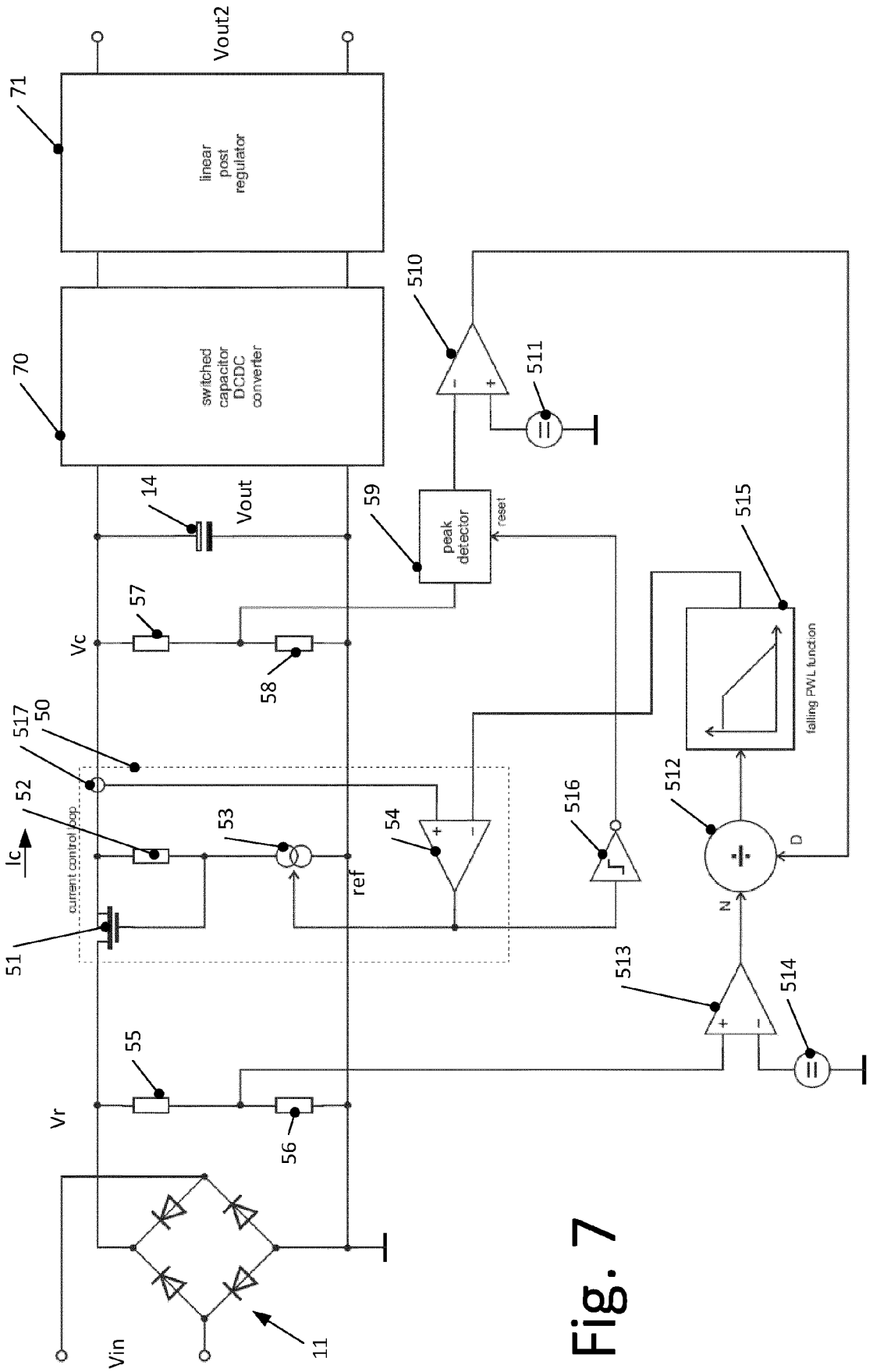
Vout2
71
linear post regulator
70
switched capacitor DCDC converter
14
Vout
59
peak detector
reset
510
511
515
57
Vc
58
517
50
52
Ic
current control loop
53
54
ref
516
512
falling PWL function
D
N
51
513
514
55
Vr
56
Vin
11

Fig. 7

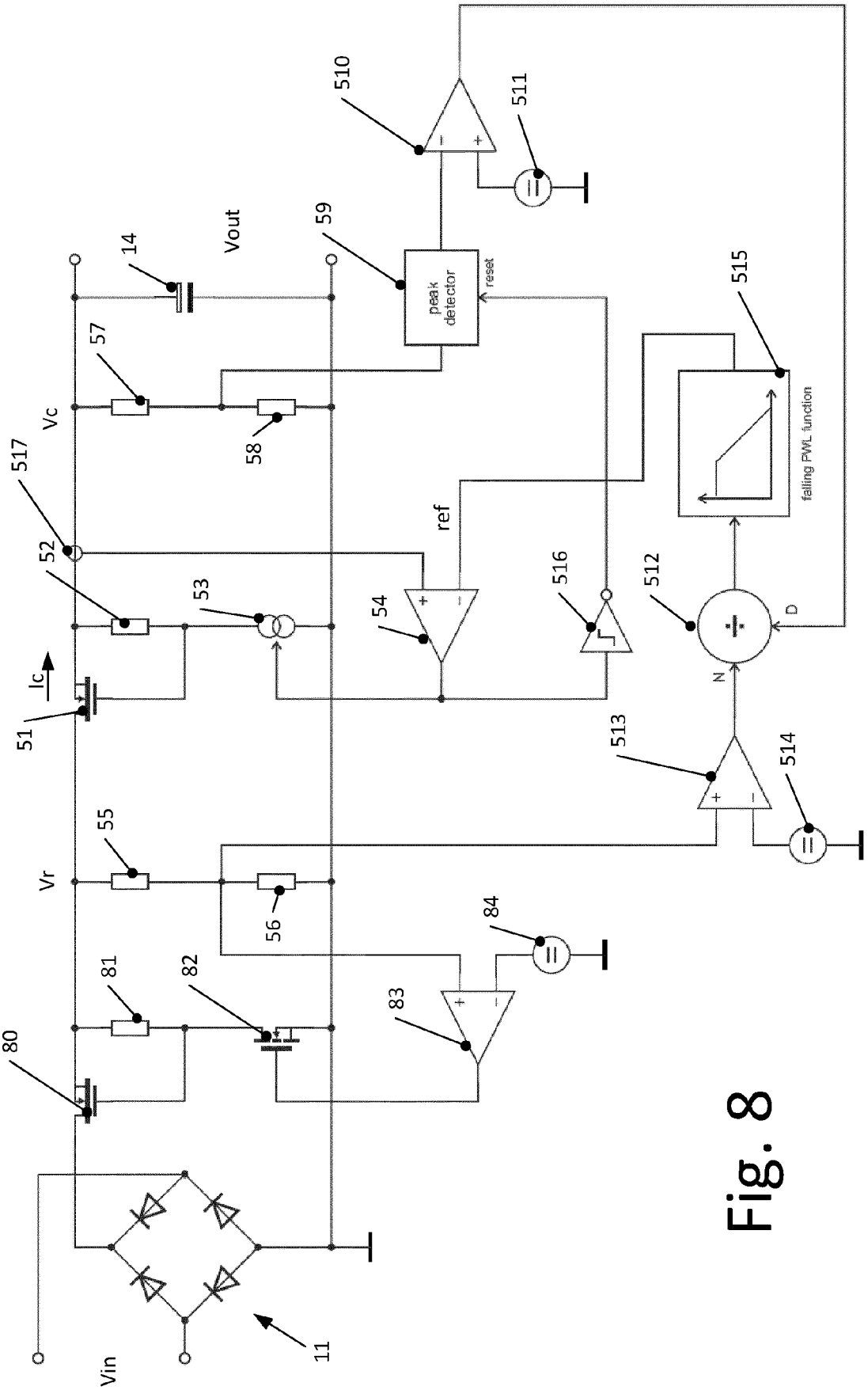
510
511
59
Vout
14
peak detector
reset
515
57
Vc
58
falling PWL function
517
ref
52
516
512
53
54
D
Ic
N
51
513
514
55
Vr
56
84
81
82
83
80
11
Vin

Fig. 8

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 21 20 7729

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	GB 2 458 699 A (DEEPSTREAM TECHNOLOGIES LTD [GB]) 30 September 2009 (2009-09-30) * page 9, line 6 - page 14, line 9 * * in particular page 12 * * figures 7,8,9b,9c *	1-15	INV. H02M7/217 ADD. H02M1/42
X	EP 2 560 063 A1 (NXP BV [NL]) 20 February 2013 (2013-02-20) * abstract * * * paragraphs [0059], [0060] * * figures 1,4,5 *	1-15	
A	EP 2 645 559 A2 (AIZO AG [DE]; AIZO GROUP AG [CH]) 2 October 2013 (2013-10-02) * paragraphs [0001] - [0005], [0073], [0098], [0099], [0126], [0139] - [0143] * * figures 2,3 *	1-15	
A	US 2017/196054 A1 (LENA DAVIDE [IT] ET AL) 6 July 2017 (2017-07-06) * paragraphs [0029] - [0035] * * figures 1,3 *	1-15	

TECHNICAL FIELDS SEARCHED (IPC)

H02M
H05B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	6 April 2022	Standaert, Frans

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 21 20 7729

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

06-04-2022

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2458699 A	30-09-2009	EP 2272160 A2	12-01-2011
		GB 2458699 A	30-09-2009
		WO 2009118535 A2	01-10-2009
EP 2560063 A1	20-02-2013	NONE	
EP 2645559 A2	02-10-2013	DE 202011002880 U1	02-05-2012
		EP 2645559 A2	02-10-2013
US 2017196054 A1	06-07-2017	US 2017196054 A1	06-07-2017
		US 2017265257 A1	14-09-2017

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82