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Wu et al.

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(54) **MECHANISMS FOR FORMING ULTRA SHALLOW JUNCTION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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(51) **Int. Cl.**

H01L 21/02	(2006.01)
H01L 27/088	(2006.01)
H01L 21/26	(2006.01)
H01L 21/425	(2006.01)

(52) **U.S. Cl.**
USPC **257/408**; 257/401; 438/513; 438/527

(58) **Field of Classification Search**
None
See application file for complete search history.

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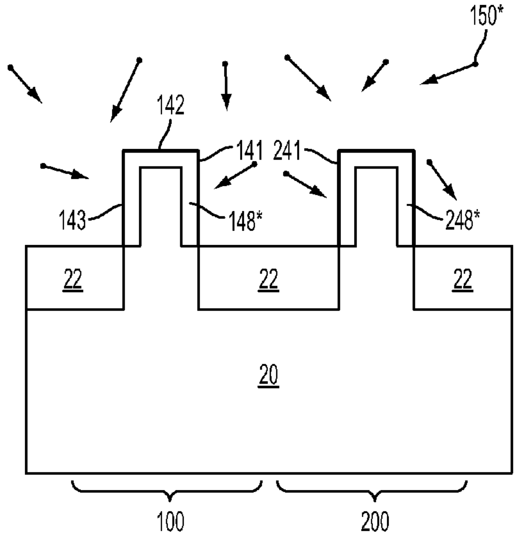
(57) **ABSTRACT**

The embodiments of methods and structures are for doping fin structures by plasma doping processes to enable formation of shallow lightly doped source and drain (LDD) regions. The methods involve a two-step plasma doping process. The first step plasma process uses a heavy carrier gas, such as a carrier gas with an atomic weight equal to or greater than about 20 amu, to make the surfaces of fin structures amorphous and to reduce the dependence of doping rate on crystalline orientation. The second step plasma process uses a lighter carrier gas, which is lighter than the carrier gas for the first step plasma process, to drive the dopants deeper into the fin structures. The two-step plasma doping process produces uniform dopant profile beneath the outer surfaces of the fin structures.

20 Claims, 9 Drawing Sheets



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2008/0124878	A1	5/2008	Cook et al.	
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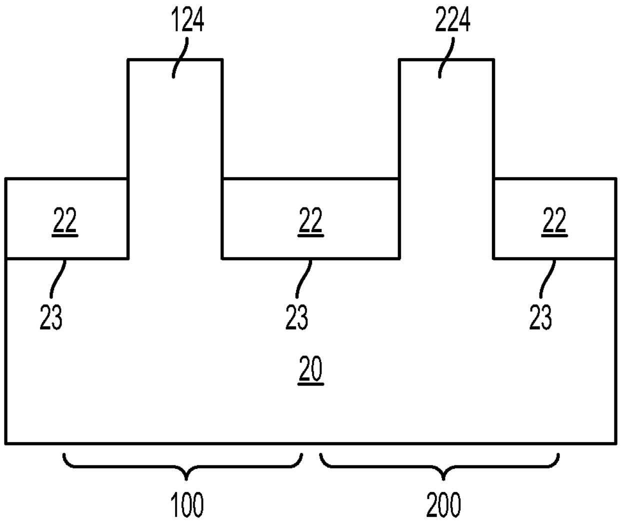
124
224
22
22
22
23
23
23
20
100
200

FIG. 1A

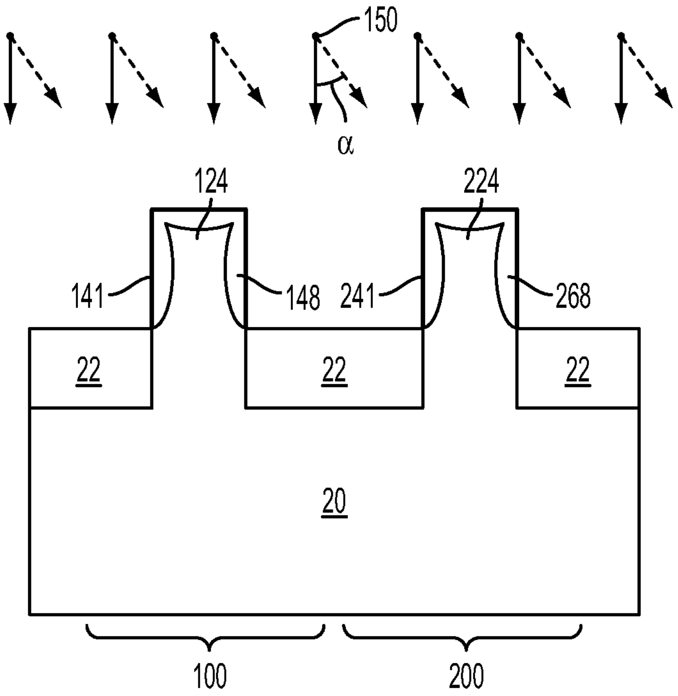
150
α
124
224
141
148
241
268
22
22
22
20
100
200

FIG. 1B

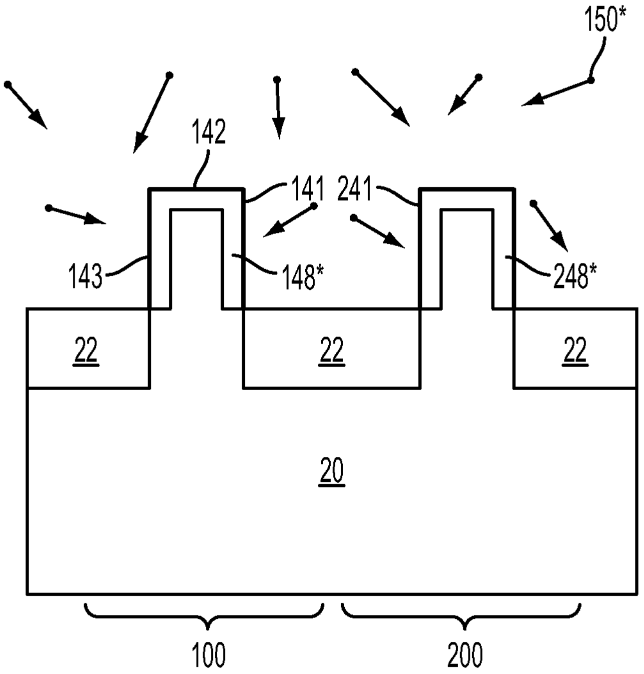

FIG. 1C

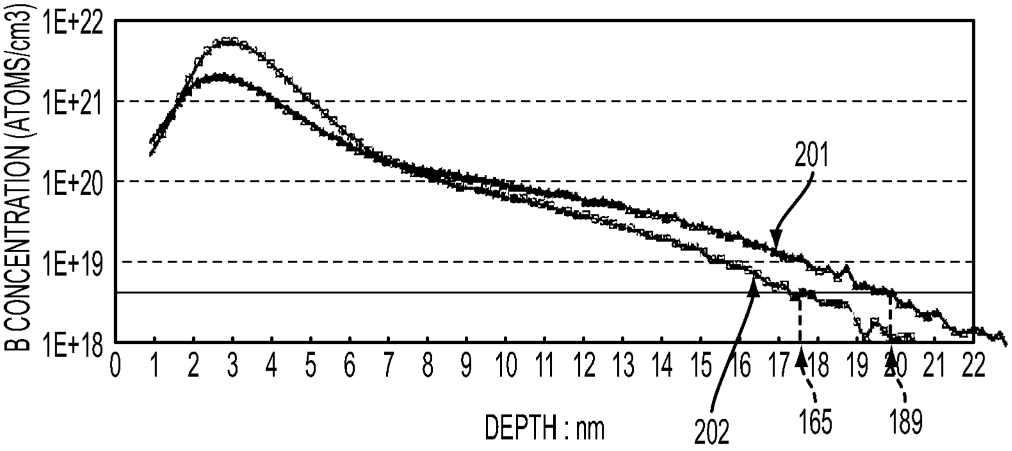
B CONCENTRATION (ATOMS/cm3)
1E+22
1E+21
1E+20
1E+19
1E+18
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
DEPTH : nm
201
202
165
189

FIG. 2A

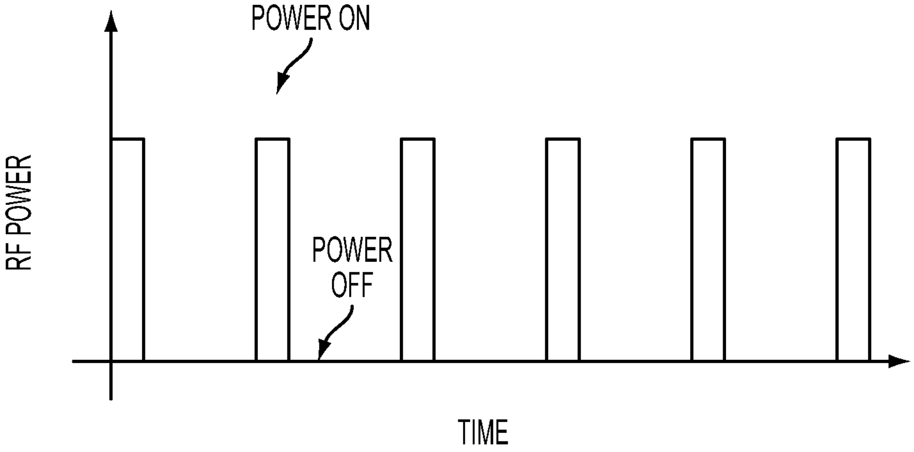
POWER ON
POWER OFF
RF POWER
TIME

FIG. 2B

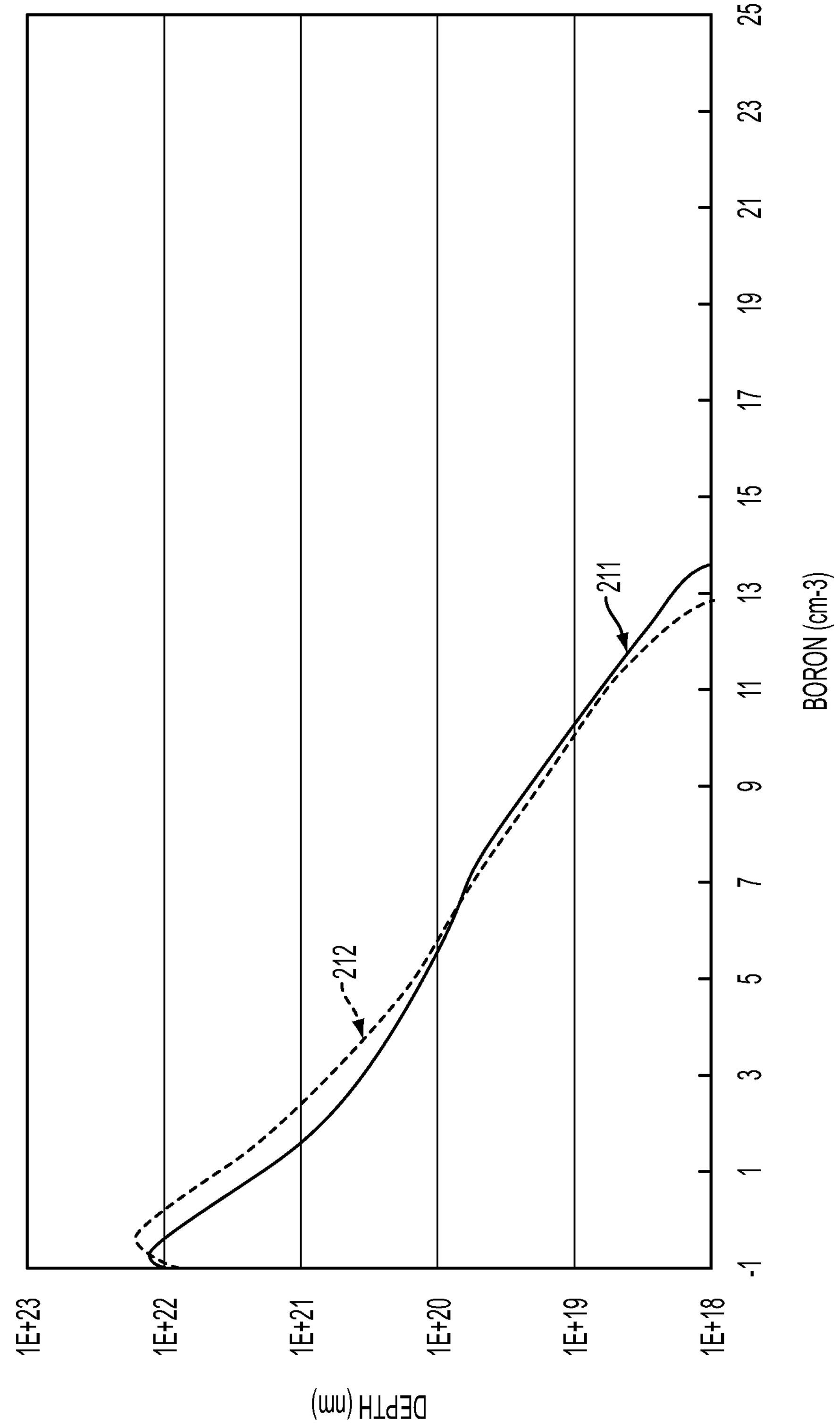
DEPTH (nm)
1E+23
1E+22
1E+21
1E+20
1E+19
1E+18
-1
1
3
5
7
9
11
13
15
17
19
21
23
25
BORON (cm-3)
211
212

FIG. 2C

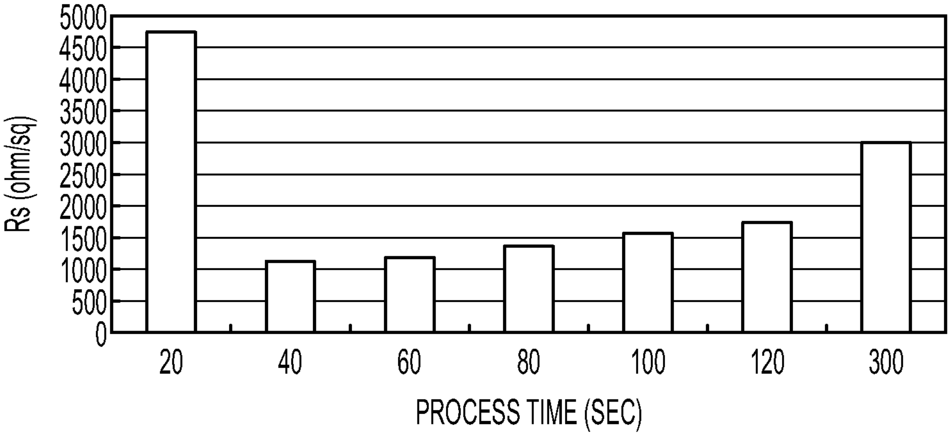
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
Rs (ohm/sq)
20
40
60
80
100
120
300
PROCESS TIME (SEC)

FIG. 2D

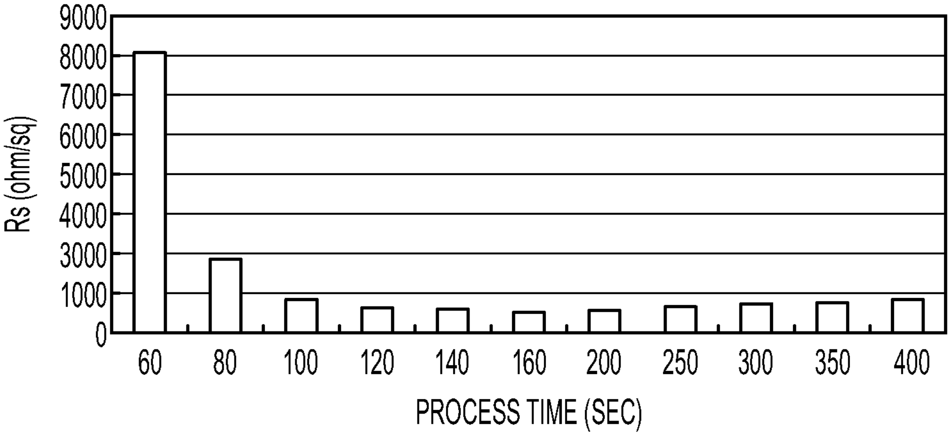
9000
8000
7000
6000
5000
4000
3000
1000
0
Rs (ohm/sq)
60
80
100
120
140
160
200
250
300
350
400
PROCESS TIME (SEC)

FIG. 2E

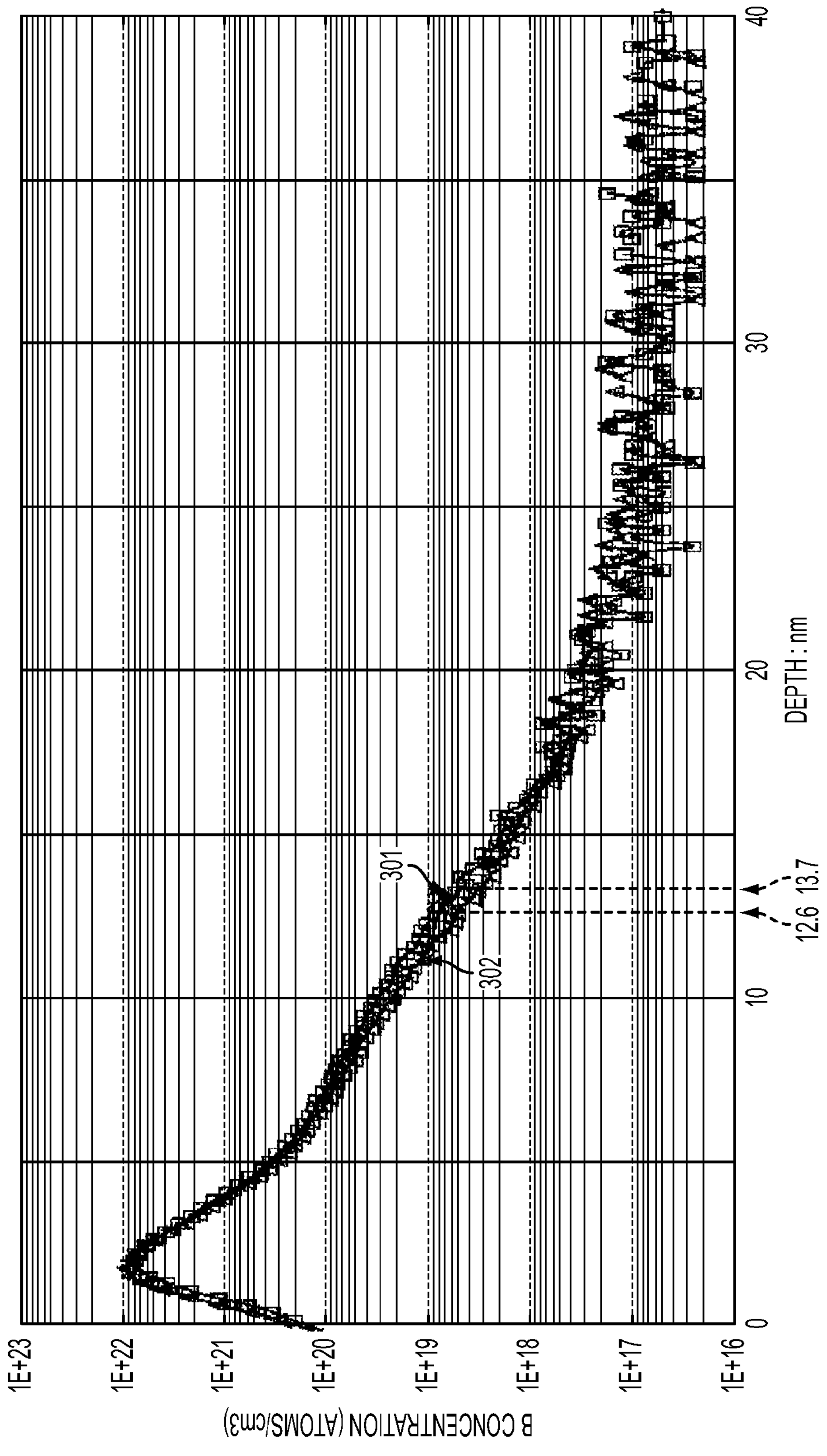
B CONCENTRATION (ATOMS/cm3)
1E+23
1E+22
1E+21
1E+20
1E+19
1E+18
1E+17
1E+16
0
10
20
30
40
DEPTH : nm
301
302
12.6
13.7

FIG. 3

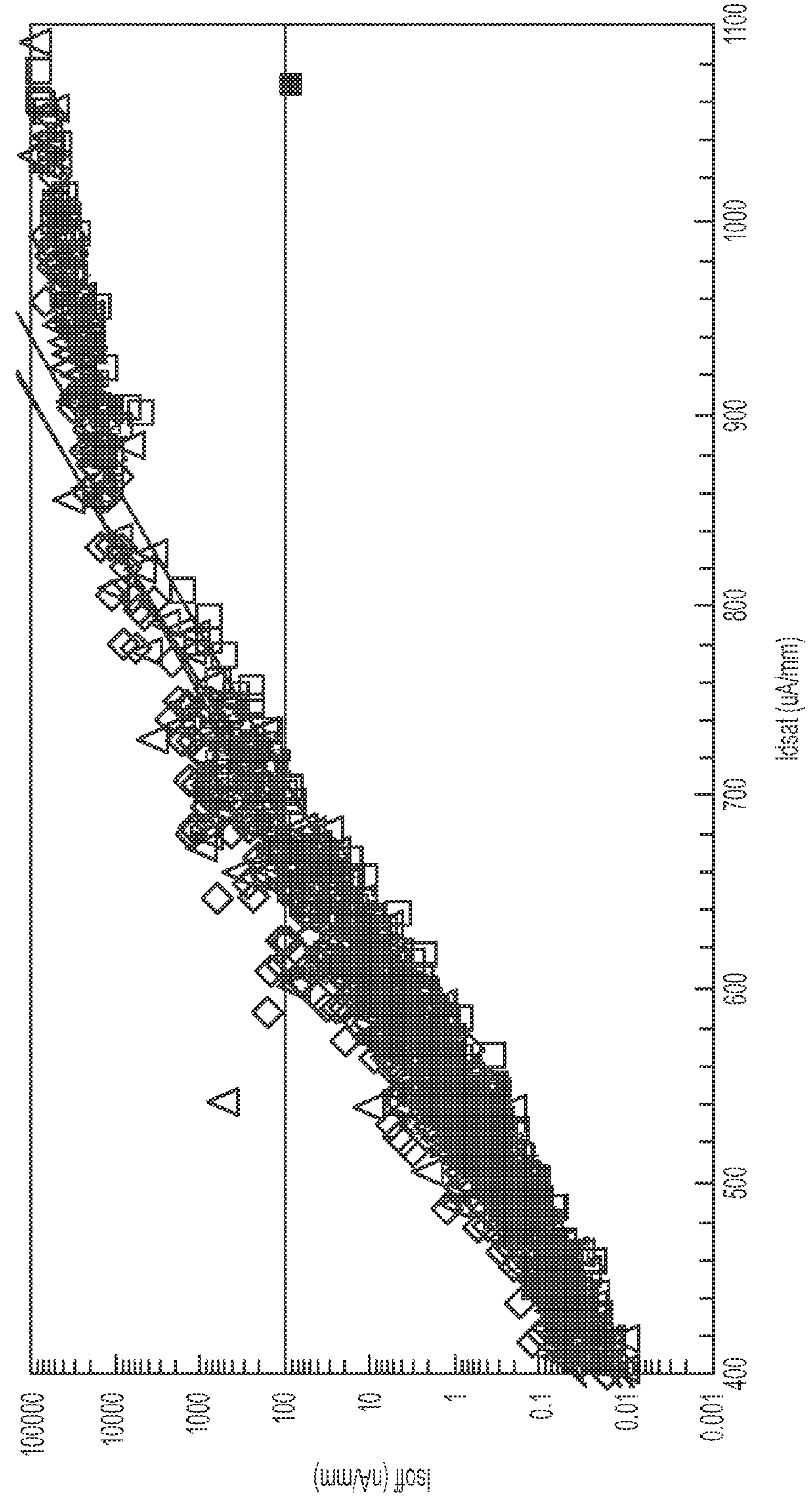
100000
10000
1000
100
10
1
0.1
0.01
0.001
Isoff (nA/mm)
400
500
600
700
800
900
1000
1100
Idsat (uA/mm)

FIG. 4A

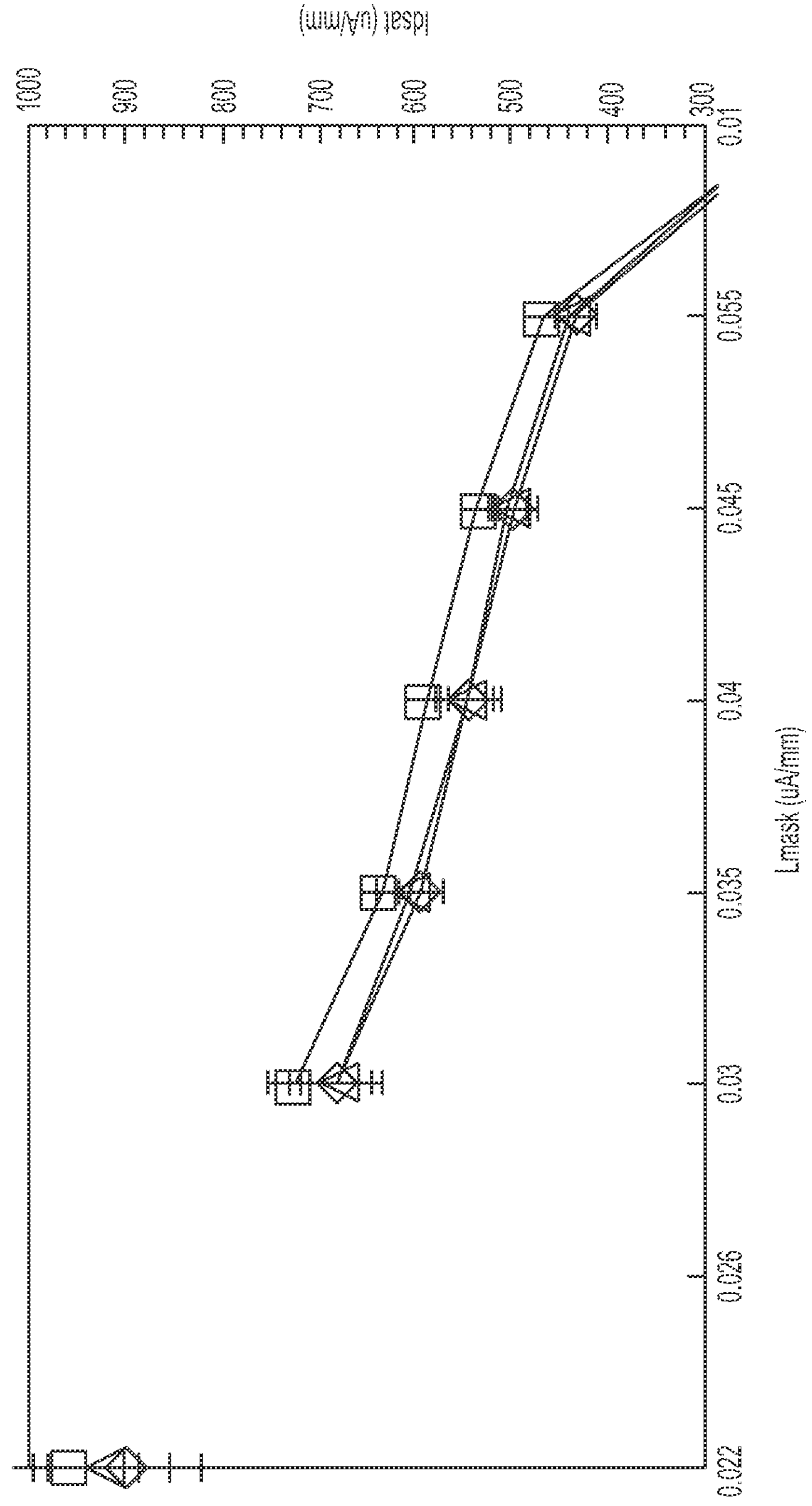
Idsat (uA/mm)
1000
900
800
700
600
500
400
300
0.01
0.055
0.045
0.04
0.035
0.03
0.026
0.022
Lmask (uA/mm)

FIG. 4B

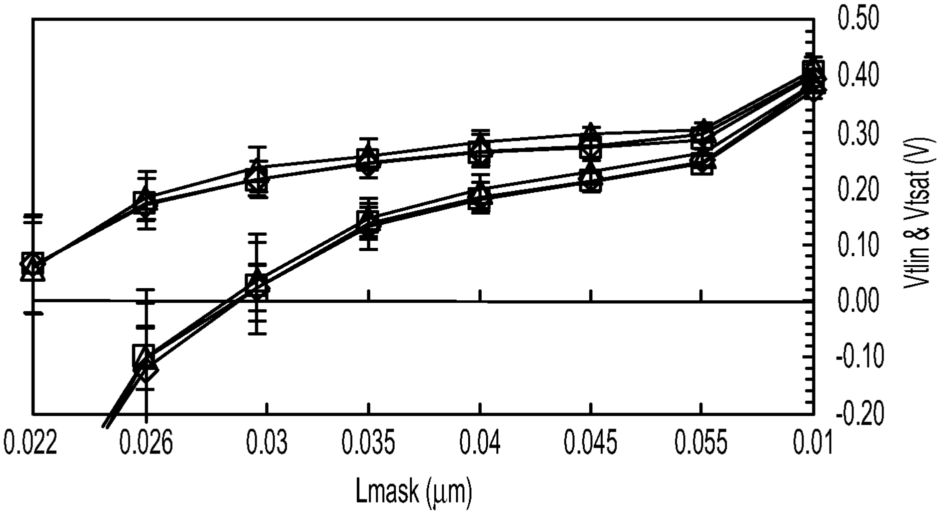
0.50
0.40
0.30
0.20
0.10
0.00
-0.10
-0.20
Vtlin & Vtsat (V)
0.022
0.026
0.03
0.035
0.04
0.045
0.055
0.01
Lmask (μm)

FIG. 4C

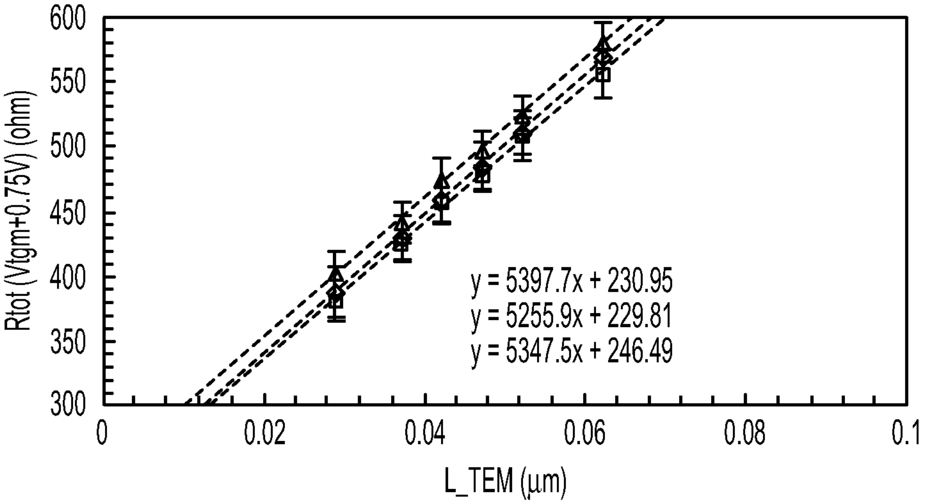
600
550
500
450
400
350
300
Rtot (Vtgm+0.75V) (ohm)
0
0.02
0.04
0.06
0.08
0.1
L_TEM (μm)
y = 5397.7x + 230.95
y = 5255.9x + 229.81
y = 5347.5x + 246.49

FIG. 4D

MECHANISMS FOR FORMING ULTRA SHALLOW JUNCTION

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation application of U.S. application Ser. No. 12/941,509, filed Nov. 8, 2010, which is incorporated herein by reference in its entirety.

The present application is related to U.S. patent application Ser. No. 12/707,788, filed on Feb. 18, 2010, titled MEMORY POWER GATING CIRCUIT AND METHODS; Ser. No. 12/758,426, filed on Apr. 12, 2010, titled FINFETS AND METHODS FOR FORMING THE SAME; Ser. No. 12/731,325, filed on Mar. 25, 2010, titled ELECTRICAL FUSE AND RELATED APPLICATIONS; Ser. No. 12/724,556, filed on Mar. 16, 2010, titled ELECTRICAL ANTI-FUSE AND RELATED APPLICATIONS; Ser. No. 12/757,203, filed on Apr. 9, 2010, titled STI STRUCTURE AND METHOD OF FORMING BOTTOM VOID IN SAME; Ser. No. 12/797,839, filed on Jun. 10, 2010, titled FIN STRUCTURE FOR HIGH MOBILITY MULTIPLE-GATE TRANSISTOR; Ser. No. 12/831,842, filed on Jul. 7, 2010, titled METHOD FOR FORMING HIGH GERMANIUM CONCENTRATION SiGe STRESSOR; Ser. No. 12/761,686, filed on Apr. 16, 2010, titled FINFETS AND METHODS FOR FORMING THE SAME; Ser. No. 12/766,233, filed on Apr. 23, 2010, titled FIN FIELD EFFECT TRANSISTOR; Ser. No. 12/757,271, filed on Apr. 9, 2010, titled ACCUMULATION TYPE FINFET, CIRCUITS AND FABRICATION METHOD THEREOF; Ser. No. 12/694,846, filed on Jan. 27, 2010, titled INTEGRATED CIRCUITS AND METHODS FOR FORMING THE SAME; Ser. No. 12/638,958, filed on Dec. 14, 2009, titled METHOD OF CONTROLLING GATE THICKNESS IN FORMING FINFET DEVICES; Ser. No. 12/768,884, filed on Apr. 28, 2010, titled METHODS FOR DOPING FIN FIELD-EFFECT TRANSISTORS; Ser. No. 12/731,411, filed on Mar. 25, 2010, titled INTEGRATED CIRCUIT INCLUDING FINFETS AND METHODS FOR FORMING THE SAME; Ser. No. 12/775,006, filed on May 6, 2010, titled METHOD FOR FABRICATING A STRAINED STRUCTURE; Ser. No. 12/886,713, filed Sep. 21, 2010, titled METHOD OF FORMING INTEGRATED CIRCUITS; Ser. No. 12/941,509, filed Nov. 8, 2010, titled MECHANISMS FOR FORMING ULTRA SHALLOW JUNCTION; Ser. No. 12/900,626, filed Oct. 8, 2010, titled TRANSISTOR HAVING NOTCHED FIN STRUCTURE AND METHOD OF MAKING THE SAME; Ser. No. 12/903,712, filed Oct. 13, 2010, titled FINFET AND METHOD OF FABRICATING THE SAME; 61/412,846, filed Nov. 12, 2010, filed Oct. 19, 2010, titled METHODS OF FORMING GATE DIELECTRIC MATERIAL and 61/405,858, filed Oct. 22, 2010, titled METHODS OF FORMING SEMICONDUCTOR DEVICES.

FIELD

This disclosure relates generally to integrated circuit devices and more particularly to processes of doping for field-effect transistors (FETs).

BACKGROUND

Semiconductor integrated circuit microelectronic fabrications are formed from semiconductor substrates within and upon which are formed semiconductor devices. Patterned conductor layers separated by dielectric layers are then formed over the semiconductor substrates to provide interconnect. Ubiquitous within the fabrication of semiconductor integrated circuit microelectronic fabrications is the use of field effect transistor (FET) devices as switching devices within both logic semiconductor integrated circuit microelectronic fabrications and memory semiconductor integrated circuit microelectronic fabrications. The accelerated shrinking of FET dimensions poses particular challenges for doping processes used in transistor fabrication. Dopant ion implantation by ion beams has widely been used to locally modify the electrical properties of silicon. However, ion implantation by ion beams has its limitations for meeting specifications of advanced devices.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

FIG. **1**A shows an integrated circuit structure, in accordance with some embodiments.

FIG. **1**B shows dopant ions being directed toward a substrate and implanted into fin structures to form implanted regions, in accordance with some embodiments.

FIG. **1**C shows dopant plasma ions directed toward a substrate and implanted into fin structures to form implanted regions, in accordance with some embodiments.

FIG. **2**A shows two dopant profiles for two substrates with two different orientations by using a plasma doping process, in accordance with some embodiments.

FIG. **2**B shows RF power for pulsed plasma as a function of time, in accordance with some embodiments.

FIG. **2**C shows two dopant profiles for two substrates with two different orientations by using another plasma doping process, in accordance with some embodiments.

FIG. **2**D shows resistivity of fin structures as a function of process time by using the plasma implantation process of FIG. **2**C, in accordance with some embodiments.

FIG. **2**E shows resistivity of fin structures as a function of process time by using the plasma implantation process of FIG. **2**A, in accordance with some embodiments.

FIG. **3** shows two dopant profiles for two substrates with two different orientations by using a two-step plasma implantation process, in accordance with some embodiments.

FIGS. **4**A-**4**D compare electrical results of fin structures for three different processes, in accordance with some embodiments.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

FIG. **1**A shows an integrated circuit structure **10**, in accordance with some embodiments. The illustrated integrated circuit structure **10** is formed on a portion of a substrate **20**. Substrate **20** may be a silicon substrate, a germanium substrate, or a substrate formed of other semiconductor materials. Substrate **20** may be doped with a p-type or an n-type impurity. Isolation regions, such as shallow trench isolation (STI) regions **22**, may be formed in or over substrate **20**. Semiconductor fins **124** and **224** are formed above surfaces **23** of STI regions **22**. In some embodiments, substrate **20** includes two PMOS (P-type metal-oxide-semiconductor) device regions **100** and **200**, and semiconductor fins **124** and **224** in the PMOS regions respectively, as shown in FIG. **1**A. In some other embodiments, device regions **100** and **200** are for NMOS (N-type MOS) devices. In yet some other embodiments, device region **100** is for an NMOS device and device region **200** is for a PMOS device, or vice versa.

In some embodiments, semiconductor fins **124** and **224** are formed by creating (or forming) shallow trench isolation (STI) regions **22**, and recessing the top surface of STI regions **22** to a level lower than the original top surface of substrate **20**. The remaining portions of substrate **20** between STI regions **22** thus become fins **124** and **224**. In some other embodiments, semiconductor fins **124** and **224** are formed of a material different from that of substrate **20**. They can be formed by recessing top portions of substrate **20** between neighboring STI regions **22** to form recesses, and re-growing a semiconductor material different from that of substrate **20** in the recesses. Top portions of STI regions **22** may then be removed, while bottom portions of STI regions **22** are not removed. As a result, the top portions of the re-grown semiconductor material between neighboring STI regions **22** become semiconductor fins **124**, **224**.

After fins **124** and **224** are formed, substrate **20** undergoes additional substrate processing to form FET devices. One operation in forming FET devices is doping the lightly doped source and drain (LDD) regions. Conventional LDD doping is performed by ion implantation with the assistance of ion beams. FIG. **1**B shows P-type dopant ions **150**, such as boron (B) ions, being directed toward substrate **20** and implanted into fins **124** and **224** to form implanted regions **148** and **248**, in accordance with some embodiments. The dopants, which are ions, may be directed toward substrate **20** vertically, or tilted toward the sidewalls of fins **124** ad **224** at an angle "α". Due to shadowing effect, the dopant profiles of implanted regions **148** and **248** are not uniform beneath the outer profiles **141**, **241** (denoted with bold lines) of fins **124** and **224** respectively. Such uneven dopant profiles of implanted regions **148**, **248** and other similar regions are more pronounced for advanced device technologies with high aspect ratios in the spaces between fins. The uneven dopant profiles would be maintained after dopant diffusion and would result in variation in device performance within a die (WID). Further, for advanced device technologies, such as technology nodes below 90 nanometers (nm), junction depth shallower than about 25 nm could be needed. For example, such shallow junction depth is used for FinFET (fin field effect transistor) structures with high aspect ratios, such as aspect ratios equal to or greater than about 1.3 for 22 nm technology nodes, in accordance with some embodiments. Doping by ion beams fails to achieve the requirement of shallow junction depth due to the relatively high energy of ion beams. As a result, new doping mechanisms are needed.

FIG. **1**C shows P-type dopant ions **150***, such as boron (B) ions, in the plasma sheath (whose boundary is not shown) right above the surface of substrate **20**, directed toward substrate **20** and implanted into fins **124** and **224** to form implanted regions **148*** and **248*** respectively, in accordance with some embodiments. The method of doping is called "Plasma doping" (PLAD). As shown in FIG. **1**C, the dopant plasma ions **150*** arrive at the substrate surface in a range of angles, instead of being at a certain angle as in the case of ion implantation by ion beams. Due to the range of arriving angles of the plasma ions, the dopant profiles **148*** and **248*** are more uniform beneath the outer profiles **141**, **241** of semiconductor fins **124**, **224**. Since the plasma ions have lower energy than the ions of ion beams, shallow junction depth (such as less than about 25 nm) can be achieved.

Semiconductor fins **124** and **224** are made of crystalline or epitaxial materials. In some embodiments, the top surfaces **142** and sidewall surfaces **143** have different crystalline orientation. For example, the top surfaces **142** could be in [100] orientation and the sidewall surfaces **143** could be in [110] orientation. Crystalline surfaces with different orientations could be doped at different rates.

FIG. **2**A shows a dopant profile **201** for a substrate with an [100] orientation on the substrate surface and a dopant profile **202** for another substrate with an [110] orientation on the substrate surface, in accordance with some embodiments. The measurement is taken by secondary ion mass spectroscopy (SIMS). Both substrates (N-type substrates) are doped by plasma doping (PLAD) with boron. The plasma doping was performed in a plasma doping system. An example of plasma doping systems is a PLAD system, made by Varian Semiconductor Equipment Associates Inc. of Gloucester, Mass. The doping gas is made by diluting a reactant gas mixture (15% B_2H_6 and 85% H_2), diluted by a carrier (or dilution) gas H_2. The ratio of the reactant gas to the carrier gas is about 49/80. The pressure of the plasma process is about 50 mTorr and RF (radio frequency) power is in a range from about 100 watts (W) to about 1000 W and at a radio frequency in a range from about 2 kilohertz (KHz) to about 13.6 megahertz (MHz). The substrate is not biased.

The radio frequency (RF) power for generating the plasma could be pulsed. FIG. **2**B shows a diagram of power cycle of a pulsed plasma, in accordance with some embodiments. FIG. **2**B shows that the RF power is turned on and off periodically. The duty ratio (power-on-time/total-time) of pulse could be in a range from about 5% to about 100% in accordance with some embodiments. The plasma doping was performed for equal to or less than about 5 minutes. The results are taken after plasma doping and also after a rapid thermal annealing (RTA) at 950° C. for less than about 5 seconds. The results show the junction depth, Xj, is about 16.5 nm for the substrate with [110] surface and about 18.9 nm for the substrate with [100] surface. Junction depth, Xj, is measured at dopant level of about 5E18 atoms/cm^3. Both junction depths, Xj, are less than the 25 nm, as required for advanced device technologies. The difference in junction depth, Xj, at [100] crystalline orientation (top surface) and at [110] crystalline orientation (sidewall surface) indicates a dependence of doping rate on the crystalline orientation.

FIG. **2**C shows a dopant profile **211** for a substrate with an [100] orientation on the substrate surface and a dopant profile **212** (dotted line) for another substrate with an [110] orientation on the substrate surface, in accordance with some embodiments. The dopants are also boron. The process gas used in collecting data in FIG. **2**C is similar with the exception that the carrier gas is Ar, instead of H_2. The results show that the junction depths, Xj, for both substrates are very close and both are at about 11 nm. By using Ar as a carrier gas, the dependence of the junction depth with substrate crystalline orientation disappears. The independence of junction depth from substrate crystalline orientation is more desirable for fin structures with different crystalline orientation of different surfaces of the fins.

In addition to the consideration of achieving shallow junction depth (less than about 25 nm) and independence of doping rate on crystalline orientation, a doping process also needs to be repeatable. FIG. **2**D shows the resistivity data taken from the substrates of FIG. **2**C (Ar as the carrier gas), in accordance with some embodiments. The resistivity data are taken from diffusion regions after the substrates are plasma doped with boron and are annealed. The data show that the resistivity varies significantly with the process time, which indicates very limited region(s) to produce repeatable results. In contrast, FIG. **2**E shows the resistivity data taken from the substrate of FIG. **2**A (H_2 as the carrier gas), in accordance with some embodiments. The data show that the resistivity is stable between about 120 seconds to about 250 seconds of process time, which is a fairly wide process window.

The data in FIGS. **2**A and **2**C-**2**E show that using Ar as a carrier gas removes the dependence of doping rate on crystalline orientation of the surface (i.e. [100] surface versus [110] surface). However, the resistivity data show that the process window of such process is too narrow to produce repeatable results. In contrast, the process window of the process using H_2 as a carrier (or dilution) gas is much wider and usable to produce repeatable results. However, the process of using H_2 as a carrier gas shows a dependence of doping rate on the crystalline orientation of the substrate.

FIG. **3** shows dopant profiles **301** (data with square symbol) and **302** (data with triangle symbol) for substrates with [100] surface orientation and [110] surface orientation respectively, in accordance with some embodiments. The plasma doping (PLAD) process used to generate the data in FIG. **3** uses a two-step process. The two-step process includes a first plasma doping process using Ar as a carrier gas to eliminate or reduce the dependence of doping rate on the crystalline orientation. The process condition and gas mixture for the first plasma doping process using Ar as a carrier gas has been described above for FIGS. **2**C and **2**D. The second plasma doping process uses H_2 as a carrier gas to achieve repeatable doping profiles from wafer to wafer, which has been described above for FIGS. **2**A and **2**E. The first plasma doping is performed for a duration in a range from about 10 seconds to about 100 seconds and the second plasma doping is performed for a duration in a range from about 10 seconds to about 300 seconds. In some embodiments, the duration for the second plasma is shorter than the duration of the first plasma. The data in FIG. **3** are taken after the 2-step plasma doping process and also a 950° C. thermal anneal. The thermal anneal is performed in a rapid thermal annealing system at peak temperature (950° C.) for equal to or less than about 5 seconds.

Dopant profiles **301** and **302** match pretty closely along the entire curves. The junction depth, Xj, for the substrate with [100] surface is measured to be about 12.6 nm, and the junction depth for the substrate with [110] surface is measured to be about 13.7 nm. The two junction depths are fairly close. The first-step doping plasma process using a relatively heavy carrier gas, such as Ar (atomic weight 40 amu) or Ne (atomic weight 20 amu), likely bombards the crystalline surface to make the substrate surface slightly amorphous, which eliminates or reduces the dependence of doping rate on crystalline orientation. The slightly amorphous surface allows the second-step doping process with a lighter carrier gas, such as H_2 or He, to deliver dopants deeper into the substrate repeatably. The slightly amorphous substrate surface can be re-crystallized again by the following annealing process(es) and does not impact the performance of the FETs.

FIG. **4**A shows data of Isoff (nA/μm) versus Idsat (nA/μm), in accordance with some embodiments. Isoff measures the current (off current) when the gate voltage (Vg) is set at zero, and Idsat measures the current (on current at saturation region) when the source voltage (Vs) is set at zero. The data are taken from finFET devices on substrates processed with three different processes. The 1^{st} process is a reference process using the conventional ion beams to drive dopants. The results of the 1^{st} process are marked by "diamond" symbol. The 2^{nd} process is a two-step plasma doping process described above with bias voltage set at 0 volt (no bias). The results of the 2^{nd} process are marked by "square" symbol. The 3^{rd} process is a two-step plasma doping process described above with bias voltage set at 0.3 KV (no bias). The results of the 3^{nd} process are marked by "triangle" symbol. The 3^{rd} process is similar to the 2^{nd} process with the exception that the bias voltage is 0.3 KV with the substrate being negatively biased. The Idsat is measured at Isoff equal to about 100 nA/μm. The results show that the Idsat is about 665.4 nA/μm for the 1^{st} process, about 702.4 for the 2^{nd} process and about 678.9 for the 3^{rd} process. The Idsat of the 1^{st} process is the lowest and the Idsat of the 2^{rd} process is the highest. The 2^{nd} process increases Idsat by about 5.6% over the reference process (1^{st} process). The 3^{rd} process increases Idsat by about 2.0% over the reference process. The results indicate an improvement in Idsat by using a plasma doping process, especially a plasma doping process without bias voltage.

FIG. **4**B shows the Idsat as a function of gate length (or gate width), in accordance with some embodiments. Lmask is the layout gate length, which could be different from actual gate lengths. However, the actual gate lengths increase with the layout gate lengths. The data in FIG. **4**B show that Idsat of the 2^{nd} process is consistently higher than the Idsat of the 1^{st} and 3^{rd} processes for different gate lengths between about 0.03 μm to about 0.055 μm.

FIG. **4**C shows Vtlin and Vtsat versus layout gate length (Lmask), in accordance with some embodiments. Vtlin is a measure of the gate voltage when the drain current is measurable and when the Vsource is set at zero and the Vdrain is set at 0.05V. Vtsat is a measure of the gate voltage when the drain voltage is measurable and when the Vsource is set at zero and the Vdrain is set at high value (such as greater than about 0.5 V, i.e. at saturation). The data show no significant difference of Vtlin and Vtsat between 3 different processes with gate widths between about 0.022 nm to about 0.1 nm.

FIG. **4**D shows the resistance of FinFET devices as a function of gate length (L_TEM) of the measured FinFET devices, in accordance with some embodiments. L_TEM is a gate length calibrated by a transmission electron microscope (TEM). The data in FIG. **4**D show resistivities for the 3 doping methods with data analyzed into linear lines and equations. The resistivity data for the 3 doping methods vary linearly with gate length.

$$Rs(1^{st}\ \text{Process})=5397.7\times L\_\text{TEM}+230.9 \tag{1}$$

$$Rs(2^{nd}\ \text{Process})=5255.9\times L\_\text{TEM}+229.8 \tag{2}$$

$$Rs(3^{rd}\ \text{Process})=5347.5\times L\_\text{TEM}+246.5 \tag{3}$$

The results show no abnormality of resistances and mobilities of dopants of FinFET devices for these 3 doping methods. The slopes of equations are inversely proportional to the mobility (1/μ) of dopants. The results show that dopants for the 2^{nd} process (plasma doping with zero bias) have the highest mobility in comparison to the other two processes. The results also indicate that the 2-step plasma doping process can be used as a doping process.

The plasma doping methods and results described above indicate that a 2-step plasma doping processes have good process windows and produce good device performance data. The plasma doping process with zero bias produces better

Idsat data than the process with a bias of about 0.3 KV. Both plasma doping processes, with zero bias and 0.3 KV bias, show better doping performance than the conventional ion beam doping process.

The annealing temperature used in the study above is about 950° C. Alternatively, the annealing temperature for LDD formation can be in a range from about 900° C. to about 1350° C. for a duration from milliseconds (ms) to minutes. As mentioned above, the plasma may be pulsed with duty ratio in a range from about 5% to about 100%. The RF power frequency may be in a range from about 2 KHz to about 13.6 MHz. In some embodiments, the RF power supply can have dual frequencies. The doping plasma may be generated in the processing chamber or remotely (remote plasma).

The annealing process used for collecting data in FIGS. **2**A and **2**C-**4**D is rapid thermal annealing (RTA). Alternatively, the annealing process can be laser anneal or flash anneal. The annealing time can be in a range from about 50 μs (micro seconds) to about 10 minutes. The doping gas in the example is a mixture of 15% H_2B_6 with 85% of H_2. Other ratios of gas mixtures may also be used. In addition, the boron containing gas does not need to be H_2B_6. Other types of boron-containing gas, such as BF_3, may also be used. The boron-containing gas does not need to be mixed with H_2. Other types of inert gas, such as He, Ar, Ne, Kr, Xe, may also be used. In some embodiments, N_2 may also be a carrier gas. However, heavier carrier gas, such as Ne, Ar, Kr, Xe, N_2, may be used to prepare the gas mixture for the first-step plasma doping process and lighter carrier gas, such as He or H_2, may be used for preparing the gas mixture for the second-step plasma doping process.

In some embodiments, the dopant-containing gas used in the first doping plasma, which makes the substrate surface slightly amorphous and doping process less sensitive to crystalline orientation of the substrate, is different from the dopant-containing gas used in the second doping plasma, which is used to drive the dopants deeper into the substrate. For example, if the dopant is boron, the dopant-containing gas used in the first doping plasma could be B_2H_6 and the dopant-containing gas used in the second doping plasma could be BF_3, or vice versa. The bias voltage applied on the substrate may also be turned on and off periodically to modify the doping characteristics in a manner similar to RF power being turned on and off to generate pulsed plasma, as shown in FIG. **2**B. The duty ratio (power-on-time/total-time) of bias pulse could also be in a range from about 5% to about 100%, in accordance with some embodiments.

The embodiments of methods described above for doping a substrate to form shallow LDD regions are described for PMOS. Similar methods also apply for NMOS, which uses N-type dopants, such as P and As. Phosphorous-containing or As-containing gas may be used for the doping LDD regions in manner described above for using boron-containing gas to dope P-type LDD.

The embodiments of methods and structures described above for doping fin structures by plasma doping process enable formation shallow lightly doped source and drain (LDD). The methods involve a two-step plasma doping process. The first step plasma process uses a heavy carrier gas, such as a carrier gas with an atomic weight equal to or greater than about 20 amu, to make the surfaces of fin structures amorphous and to reduce the dependence of doping rate on crystalline orientation. The second step plasma process uses a lighter carrier gas, which is lighter than the carrier gas for the first step plasma process, to drive the dopants deeper into the fin structures. The two-step plasma doping process produces uniform dopant profile beneath the outer surfaces of the fin structures.

In one embodiment, a method of doping a shallow lightly doped source and drain (LDD) regions of fin structures on a substrate is provided. The method includes applying a first doping plasma on the shallow LDD regions of the fin structures. The fin structures have surfaces with more than one crystalline orientation, and a first source gas of the first doping plasma includes a first dopant-containing gas and a first carrier gas, wherein the first dopant-containing gas includes the dopant. The doping rate of the first doping plasma is significantly the same on different surfaces of the fin structures with more than one crystalline orientation. The method also includes applying a second doping plasma on the shallow LDD regions of the fin structures after the first doping plasma is applied. A second source gas of the second doping plasma includes a second dopant-containing gas and a second carrier gas, and the second doping plasma delivers the dopant deeper below surfaces of the shallow LDD regions of the fin structures.

In another embodiment, a method of doping a shallow lightly doped source and drain (LDD) regions of fin structures on a substrate is provided. The method includes applying a first doping plasma on the shallow LDD regions of the fin structures, and the fin structures have surfaces with more than one crystalline orientation. A first source gas of the first doping plasma includes a first dopant-containing gas and a first carrier gas, and the first dopant-containing gas includes the dopant. The doping rate of the first doping plasma is significantly the same on different surfaces of the fin structures with more than one crystalline orientation. The method further includes applying a second doping plasma on the shallow LDD regions of the fin structures after the first doping plasma is applied. A second source gas of the second doping plasma includes a second dopant-containing gas and a second carrier gas. The second doping plasma delivers the dopant deeper below surfaces of the shallow LDD regions of the fin structures, and the dopant profiles of the shallow LDD regions are uniform beneath the outer profiles of the fin structures. In addition, the method includes performing a thermal annealing on the substrate after the second doping plasma is applied.

In yet another embodiment, a fin field-effect transistor (FinFET) having a fin structure with a shallow lightly doped source and drain (LDD) region is provided. The fin structure has a top surface with a first crystalline orientation. Two sidewall surfaces of the fin structure have a second crystalline orientation. The shallow LDD region is uniform beneath the top surface and the two sidewall surfaces of the fin structure, and dopants in the shallow LDD region are implanted in the fin structure by a two-step plasma doping process. A first step plasma doping process of the two-step plasma doping process uses a carrier gas with an atomic weight equal to or greater than 20 amu, and the first step plasma doping process makes the top surface and the two sidewall surfaces amorphous to reduce the difference in crystalline orientation of surfaces of the fin structure to enable dopants to be implanted uniformly beneath the surfaces of the fin structures by the second-step plasma doping process.

Various modifications, changes, and variations apparent to those of skill in the art may be made in the arrangement, operation, and details of the methods and systems disclosed. Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

1. A fin field-effect transistor (FinFET) comprising:

a substrate; and

a fin structure over the substrate, wherein the fin structure comprises a lightly doped source and drain (LDD) region uniformly formed beneath a top surface and sidewall surfaces of the fin structure, a first junction depth of the LDD region with respect to the top surface and a second junction depth of the LDD region with respect to the sidewall surfaces both being less than about 25 nm.

2. The FinFet of claim **1**, further comprising:

a shallow trench isolation (STI) structure disposed next to the fin structure.

3. The FinFet of claim **1**, wherein the fin structure has an aspect ratio equal to or greater than about 1.3.

4. The FinFET of claim **1**, wherein the top surface having a first crystalline orientation and the sidewall surfaces having a second crystalline orientation.

5. The FinFET of claim **4**, wherein the first crystalline orientation is and the second crystalline orientation is [110].

6. The FinFET of claim **1**, wherein the first and second junction depths are depths measured at a dopant level near 5E18 atoms/cm^3.

7. The FinFET of claim **1**, wherein the first junction depth is less than about 20 nm, and the second junction depth is less than the first junction depth.

8. The FinFET of claim **1**, wherein first junction depth and the second junction depth are both less than about 15 nm.

9. The FinFet of claim **1**, wherein the smallest dimension of the FinFET is equal to or less than about 90 nm.

10. A method of doping a lightly doped source and drain (LDD) region of a fin field-effect transistor (FinFET), comprising:

performing a first plasma doping on the LDD region of the fin structure, wherein the fin structure has surfaces with more than one crystalline orientation, wherein the doping rate of the first plasma doping is substantially the same on the surfaces of the fin structure.

11. The method of claim **10**, further comprising:

performing a second plasma doping on the LDD region of the fin structure after the first doping plasma is performed, wherein the second plasma doping delivers dopants deeper below surfaces of the LDD region of the fin structure than the first plasma doping.

12. The method of claim **11**, further comprising:

performing a thermal annealing on the substrate after the second plasma doping is performed.

13. The method of claim **12**, wherein the temperature of the thermal annealing ranges from about 900° C. to about 1350° C.

14. The method of claim **12**, wherein the thermal annealing is selected from one of rapid thermal annealing (RTA), laser anneal, and flash anneal.

15. The method of claim **12**, wherein an annealing time of the thermal annealing is in a range from about 50 ms to about 10 minutes.

16. The method of claim **11**, wherein the first plasma doping is performed using a dopant-containing gas mixed with a carrier gas selected from a group consisting of Ar, Ne, Kr, Xe, and N_2, and wherein the second plasma doping is performed using a dopant-containing gas mixed with a carrier gas selected from a group consisting of He and H_2.

17. The method of claim **11**, wherein the second plasma doping uses a second carrier gas lighter than a first carrier gas for the first plasma doping.

18. The method of claim **11**, wherein the first and second plasma dopings are performed without bias voltage.

19. The method of claim **11**, wherein plasma ions of the first and second plasma dopings have a lower energy than ions of ion beams.

20. A method of forming a fin field-effect transistor (FinFET) comprising:

forming a fin structure over a substrate, the fin structure having a top surface and sidewall surfaces;

performing a first plasma doping on the fin structure, wherein doping rates of the first plasma doping on the top and sidewall surfaces of the fin structures are substantially the same; and

performing a second plasma doping on the fin structure after the first doping plasma is performed, wherein the second plasma doping delivers dopants deeper below top and sidewall surfaces of the fin structure than the first plasma doping.

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