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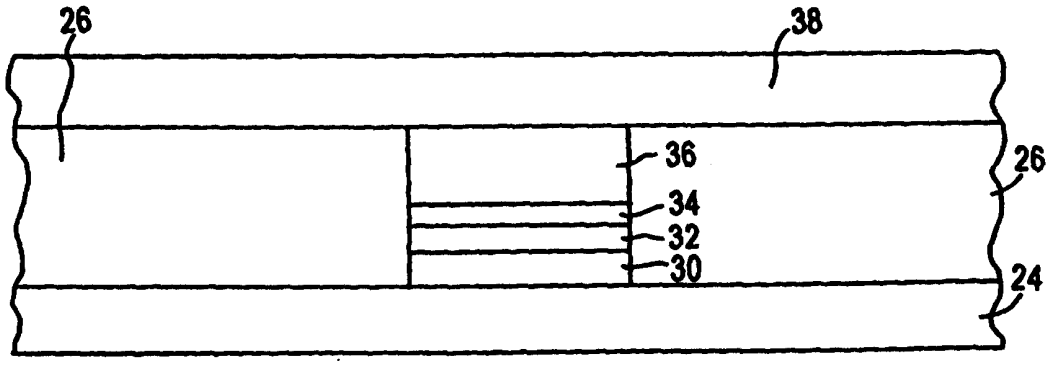
(54) Title: SILICIDE STOP LAYER IN A DAMASCENE GATE SEMICONDUCTOR STRUCTURE



(57) Abstract: A damascene gate semiconductor structure that is formed utilizing a silicide stop layer (34). Initially, a gate opening (28) is provided in an insulating layer (26) on a substrate (24). A first dielectric layer (30) is deposited in the gate opening (28) over the substrate (24). A silicide stop layer (34) is then deposited in the gate opening (28) over the first silicon layer (32). A second silicon layer (36) is then deposited in the gate opening (28) over the silicide stop layer (34). A metal or alloy layer (38) is then deposited over the insulating layer (26) and the second silicon layer (38). The damascene semiconductor structure is then temperature treated to react the metal or alloy layer (38) with the second silicon layer (36) to form a silicide layer (40). Any unreacted metal or alloy is then removed from the metal or alloy layer (38).

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SILICIDE STOP LAYER IN A DAMASCENE SEMICONDUCTOR STRUCTURE

TECHNICAL FIELD

The present invention relates to the formation of silicide in a damascene semiconductor structure. More particularly, the apparatus and method of the present invention allows for controlled silicidation of semiconductor material in a damascene semiconductor structure with the utilization of a silicide stop layer.

BACKGROUND ART

Semiconductor damascene structures are well known in the semiconductor device industry. Typically, to form a damascene structure, a dielectric layer is deposited on a silicon substrate and regions are etched in the dielectric layer in a controlled manner. The etched regions may be trenches, vias, or other etched formations well-known in the art. Subsequent to the step of etching the dielectric layer, specifically chosen materials are deposited in a calculated and controlled manner in the etched regions. The deposition and formation of material layers in the trench is part of damascene semiconductor processing. Through adequate design and processing of a semiconductor structure, the semiconductor structure can operate as a semiconductor device. Examples of semiconductor devices include transistors, memory units, LEDs, and other well-known semiconductor devices.

Often one of the material layers formed in a damascene semiconductor structure is a silicide layer. The material of the silicide layer typically comprises the product of a metal or alloy reacted with a silicon material. It is often advantageous for a silicide to be formed in a semiconductor structure in a self-aligned manner. A self-aligned silicide has the advantage of being formed in a semiconductor structure without the need to selectively etch any of the silicide layer away to define the silicide regions. Silicides are often formed in damascene semiconductor structures to provide low resistivity regions for various reasons. Such reasons include the provision of interconnect structures between semiconductor devices, lowering the resistivity of a region of a semiconductor structure to enhance the operability of a semiconductor device, or other reasons that are well-known in the art.

Figures 1-8 exemplify the formation of silicide regions in a semiconductor damascene structure. Figure 1 shows silicon substrate 10 with a gate 15 and spacers 11 formed thereon. The silicon substrate 10 may be N^+ doped to form source/drain regions 13. Figure 2 shows a dielectric layer 12 deposited on the silicon substrate 10 and surrounding the spacers 11. Figure 3 shows the gate 15 etched to form an opening 14 down to the silicon substrate 10. Figure 4 shows a dielectric layer 16 deposited in the opening 14 on the silicon substrate 10. Figure 5 shows a silicon layer 18 deposited on dielectric layer 16 in the opening 14. Figure 6 shows a metal layer 20 deposited on the dielectric layer 12 and on the silicon layer 18. Figure 7 shows silicide layer 22 formed from the semiconductor structure shown in Figure 6 by a heat treatment that reacts the silicon layer 18 with the metal layer 20 to form silicide layer 22 over dielectric layer 16. A layer of unreacted metal 21 from the metal layer 20 of Figure 6 remains over the dielectric layer 12 and silicide layer 22. The unreacted metal layer 21 is typically stripped away from the semiconductor structure using conventional stripping techniques. Figure 8 shows the semiconductor structure of Figure 7 after the unreacted metal layer 21 has been stripped away. Depending on the type of silicide formed, additional heat treatment may be preformed to produce the lowest resistivity phase of the silicide.

The exemplary semiconductor structure of Figure 8 is a characteristic structure of a metal-oxide semiconductor field-effect-transistor (MOSFET). The silicon substrate 10 may comprise a source and a drain. Further, dielectric layer 16 may serve as a gate dielectric and silicide region 20 may serve as a gate. Typically, during the silicidation of silicon layer 18, the entire silicon layer 18 is silicidized to form silicide layer 22. As a result, the silicide layer 22 is in contact with dielectric layer 16.

There are certain disadvantages to the prior art apparatus and method described above. Typically in semiconductor processing, silicon layer 18 is silicidized to form a silicide layer 22 and the entire silicon layer 18 is silicidized during a reaction with metal layer 20 during the heat treatment. This typically results in the direct contact of the silicide layer 22 with the dielectric layer 16. This has an undesirable effect on the work function. In an ideal MOSFET it is desirable for the gate, such as formed by silicide layer 22, and the semiconductor substrate with a source and drain, such as semiconductor substrate 10, to have the same work function.

The work function is the minimal energy needed to remove an electron from the fermi energy level (E_F) of a material to the vacuum energy level (E_0). The fermi energy level is the average energy of electrons in the material in the resting state. Figure 9 exemplifies a band diagram of an ideal MOSFET, wherein region 23 represents a gate, region 25 represents a gate dielectric, and region 27 represents a semiconductor substrate. Figure 9 is characterized as being an ideal MOSFET because the work function ($|_A$) 29 of region 23 and the work function ($|_B$) 31 of region 27 are substantially equivalent. This characteristic prevents the effect of a bias voltage between the gate and the semiconductor substrate. For a MOSFET to operate most efficiently and effectively, the work function of the gate and the work function of the semiconductor substrate should be approximately the same, preventing an effective bias voltage.

Figure 10 exemplifies the band diagram of a non-ideal MOSFET, wherein region 35 represents a gate and region 33 represents a semiconductor substrate that are separated by the gate dielectric represented by region 37. The work function ($|_C$) 39 of region 35 and the work function ($|_D$) 41 of region 33 are not equal. An exemplary MOSFET with a band diagram of Figure 10 has an effective bias voltage applied to the gate. Such a bias voltage can interfere with the operation of transistor having the general structure of Figure 8. Transistors are, therefore, normally engineered such that the work function of the gate region and the work function of the semiconductor region are the same.

One disadvantage of the MOSFETs exemplified in Figure 8 is that it is difficult to control the amount of silicidation of silicon layer 18 of Figure 6 and thereby control the work function of the gate region 22 to match the work function of the semiconductor substrate 10. These differences in work functions result in an effective bias voltage applied to the gate of the MOSFET, which is undesirable.

DISCLOSURE OF THE INVENTION

There is a need for a semiconductor damascene structure in which a semiconductor layer can be silicidized in a controlled manner, to allow for the work function of the gate and the work function of the silicon substrate to be substantially equal.

These and other needs are met by embodiments of the present invention which provide a damascene semiconductor structure with a silicide stop layer which enables improved control of the silicidation of semiconductor material in a damascene semiconductor structure. A gate and spacers are formed over a semiconductor substrate. A dielectric layer is formed over the semiconductor substrate and around the spacers. The gate is etched to form an opening down to the semiconductor substrate. A first silicon layer is deposited in

the opening over the semiconductor substrate. A silicide stop layer is then deposited in the opening over the first silicon layer. A second silicon layer is then deposited in the opening over the silicide stop layer. A metal layer or alloy layer is then deposited over the insulating layer and the second silicon layer and undergoes a temperature treatment. The temperature treatment causes the silicidation of the second silicon layer by reacting the metal layer or alloy with the second silicon layer. The unreacted metal or alloy layer of the metal layer or alloy layer is then stripped away and the semiconductor structure of the present invention is accomplished.

One of the advantages of the present invention is the controlled silicidation of semiconductor materials deposited in the trench by the utilization of a silicide stop layer. The silicide stop layer prevents silicidation of materials below the silicide stop layer by blocking the diffusion of metal from the metal layer. This feature allows, among other things, the tailoring of the work function of the gate and semiconductor substrate. This tailoring of the work function is a beneficial aspect to many types of semiconductor devices.

For example, a MOSFET can be in the form of a semiconductor damascene structure. An ideal MOSFET has a gate and semiconductor substrate with work functions that are substantially equal. Complete silicidation of the materials comprising the gate may inhibit the engineering of the work functions. The use of a silicide stop layer allows for the engineering of the work functions of a MOSFET to form an ideal MOSFET. This allows for such a MOSFET to operate most efficiently and effectively.

The foregoing and other features, aspects, and advantages of the present invention will become more apparent from the following detailed description of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-8 show the formation of a damascene gate in accordance with a prior art method.

Figure 9 is a prior art band diagram of an ideal MOSFET.

Figure 10 is a prior art band diagram of a non-ideal MOSFET.

Figures 11-20 depict the formation of a damascene gate in accordance with embodiments of the present invention.

MODES FOR CARRYING OUT THE INVENTION

The present invention addresses problems related to the use of damascene gates employing silicide or other metals as the gate electrode material. These problems, including change of work function, are solved in part by the provision of a silicide stop layer in the gate electrode that prevents the complete silicidation of the gate electrode. Since silicon remains in contact with the gate dielectric, even after silicidation of part of the gate electrode, the work function does not have to be re-engineered.

Figure 11 shows an exemplary semiconductor substrate with a gate 29 and spacers 27 formed thereon. The semiconductor substrate 24 may be N^+ doped to form source/drain regions 25. Figure 12, shows an insulating layer 26 deposited on the semiconductor substrate 24 and around the spacers 27. Figure 13 is the semiconductor structure of Figure 12 with an opening 28 etched in the gate 29 down to the semiconductor substrate 24. The opening 28 can define the semiconductor structure and is the characteristic that makes the semiconductor structure a damascene semiconductor structure.

Figure 14 shows a dielectric layer 30 deposited on semiconductor substrate 24 in the opening 28. This dielectric layer 30 forms a gate dielectric. A gate dielectric is a fundamental component of a MOSFET. The

dielectric layer 30 may comprise a high k dielectric, an oxide material, or any other material well known in the art that can be used as a gate dielectric. Figure 15 shows a semiconductor layer 32 deposited on the dielectric layer 30 and in the opening 28. Semiconductor layer 32 maybe between about 200 Å to about 500 Å thick. In certain embodiments, the semiconductor layer 32 is tailored such that the work functions of the gate and the work function of the semiconductor substrate are substantially equal, as required for an ideal MOSFET. Semiconductor layer 32 can be tailored by doping the material comprising semiconductor layer 32 such that the work function of layer 32 is substantially the same as the work function of the semiconductor substrate 24. In certain embodiments, semiconductor layer 32 is polycrystalline silicon.

In, Figure 16, a silicide stop layer 34 has been deposited on semiconductor layer 32 and in the opening 28. The silicide stop layer 34 may be comprised of SiN_x, TiN_x, WN_x, WC_x, or CrN_x and may be deposited by CVD, PVD, or other known techniques. In the above mentioned materials, subscript "x" represents all stoichometric variations of the listed materials. Other materials may be used for the silicon stop layer 34 that are conductive and act as a diffusion barrier to prevent diffusion of metal during silicidation. The silicide stop layer 34 may be between about 10 Å to about 200 Å thick in certain embodiments.

Semiconductor layer 36 is then deposited over silicide stop layer 34, as depicted in Figure 17. The semiconductor layer 36, in certain embodiments, comprises polycrystalline silicon. In Figure 18, a metal layer or alloy layer 38 is deposited over insulating layer 26 and semiconductor layer 36. The metal layer or alloy layer 38 may comprise nickel metal or nickel alloy, titanium metal or titanium alloy, cobalt metal or cobalt alloy, or other metals or alloys well known in the art that react with semiconductor materials to form silicides.

Figure 19 shows the semiconductor structure of Figure 18 after an appropriate temperature treatment or treatments, such as rapid thermal annealing steps. This causes the metal layer 38 to react with the semiconductor layer 36 to form silicide. The temperature selected and the number of rapid thermal anneal steps employed is dependent on the type of metal used to form the silicide. For example, when using titanium or cobalt, two rapid thermal annealing steps are typically used to form the lowest resistivity phase silicides. When nickel is used, a single, lower temperature rapid thermal annealing is normally employed to obtain the lowest resistivity phase silicide. When nickel is the metal, for example, annealing may be performed between the temperatures of about 250°C and about 750°C to react the metal layer or alloy layer 38 with semiconductor layer 36 to form a nickel silicide layer 40 above the silicide stop layer 34.

Figure 20 shows the semiconductor structure of Figure 19 after the removal of the unreacted metal from metal layer 38 using conventional stripping techniques. Such conventional stripping techniques include use of sulfuric peroxide, hydrochloric acid, nitric acid, phosphoric acid, or mixtures of these stripping agents. The semiconductor structure shown in Figure 20 is an exemplary embodiment that demonstrates an aspect of a MOSFET.

One of ordinary skill in the art would recognized that the illustrations of the deposition of dielectric layer 30, semiconductor layer 32, silicide stop layer 34, and semiconductor layer 36 in Figures 14-17 are ideal and simplified for the purpose of clearly disclosing the invention. It would be apparent to one of ordinary skill in the art that during the deposition of dielectric layer 30, semiconductor layer 32, silicide stop layer 34, and semiconductor layer 36 it is unavoidable that some of this material deposited will attach to spacers 27 and over insulating layer 26. Further, it would be obvious to one of ordinary skill in the art to selectively use a chemical vapor disposition (CVD) or a physical vapor deposition (PVD) technique to minimize material attached to the

spacers 27 in order to obtain a structure that most closely resembles that depicted in Figure 17. Further, one of ordinary skill in the art would realized that prior to achieving a semiconductor structures that resembles that depicted in Figure 17, excess material deposited over insulating layer 26 would be removed to achieve a semiconductor structure that illustrated in Figure 17.

The final product of the present invention is a damascene gate arrangement with unique advantages. In summary, the present invention is a damascene gate with a gate dielectric over a silicon substrate with a polysilicon crystalline layer on the gate dielectric. The polycrystalline silicon layer can be engineered to have the most compatible work function with the silicon substrate to prevent an effective bias voltage. By preventing such a bias voltage, the semiconductor device of the present invention can operate more effectively and efficiently. The silicide stop layer, which is formed over the polycrystalline silicon layer, protects the engineered polycrystalline silicon layer from being silicidized during the silicidation of semiconductor material formed over the silicide stop layer. In summary, the present invention offers the advantages of an effective damascene gate semiconductor device with the advantages of a silicide region formed on the gate. One such advantage is a silicide region with a relatively low sheet resistance.

The use of a silicide stop layer as provided in the present invention allows a silicidation process to occur within a damascene gate arrangement, without risking the altering of the work function. The silicide stop layer prevents complete silicidation of the gate electrode, preserving the silicon on the gate dielectric. This enables the effective engineering of the work function of the gate and the semiconductor substrate.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the pending claims.

CLAIMS

WHAT IS CLAIMED IS:

1. A method of forming a damascene semiconductor structure, comprising the steps of:

providing a gate opening (28) in an insulating layer (26) on a substrate (24);

depositing a first silicon layer (32) in the gate opening (28) over the substrate (24);

depositing a silicide stop layer (34) in the gate opening (28) over the first silicon layer (32);

depositing a second silicon layer (36) in the gate opening (28) over the silicide stop layer (34);

depositing a metal or alloy layer (38) over the insulating layer (26) and the second silicon layer (36);

temperature treating the damascene semiconductor structure to react the metal or alloy layer (38) with the second silicon layer (36) to form a silicide layer (40); and

removing unreacted metal or alloy in the metal or alloy layer (38), the silicide stop layer (34) preventing interaction of the first silicon layer (32) with the metal or alloy layer (38).

2. The method of claim 1, wherein the temperature treating is conducted between about 250^0C and about 750^0C.

3. The method of claim 1, wherein the silicide stop layer (34) is about 10 Å to about 200 Å thick.

4. The method of claim 1, wherein the silicide stop layer (34) is comprised of one of SiN_x, TiN_x, WN_x, WC_x, and CrN_x.

5. The method of claim 1, comprising the further step of depositing a high k dielectric layer (30) in the gate opening (28) over the substrate (24) before the step of depositing the first silicon layer (32).

6. A damascene semiconductor structure comprising:

a dielectric layer (26) on a substrate (24), the dielectric layer (26) having a gate opening (28);

a gate dielectric (30) in the gate opening (28) and on the substrate (24);

a silicon layer (32) on the gate dielectric (30);

a silicide stop layer (34) on the silicon layer (32); and

a silicided layer (40) on the silicide stop layer (34).

7. The semiconductor structure of claim 6, wherein the silicide stop layer (34) is about 10 Å to about 200 Å thick.

8. The semiconductor structure of claim 6, wherein the silicide stop layer (34) is comprised of one of SiN_x, TiN_z, WN_x, WC_x, and CrN_x.

9. The semiconductor structure of claim 6, wherein the gate dielectric is comprised of a high k dielectric material.

10. The semiconductor structure of claim 6, wherein the silicide layer (40) is comprised of one of NiSi, TiSi, and CoSi.

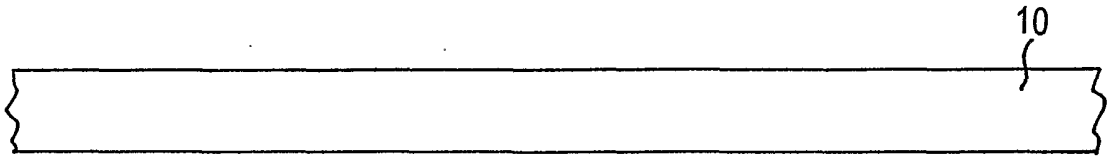

FIG. 1 (PRIOR ART)

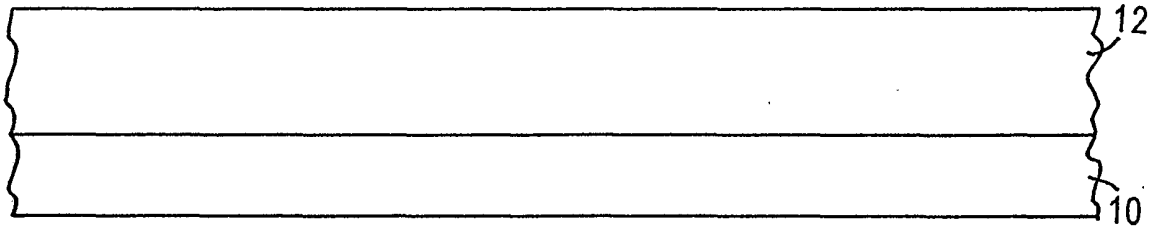

FIG. 2 (PRIOR ART)

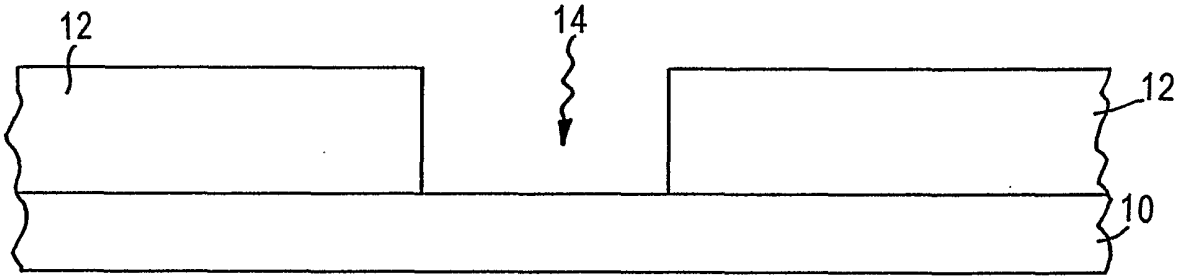

FIG. 3 (PRIOR ART)

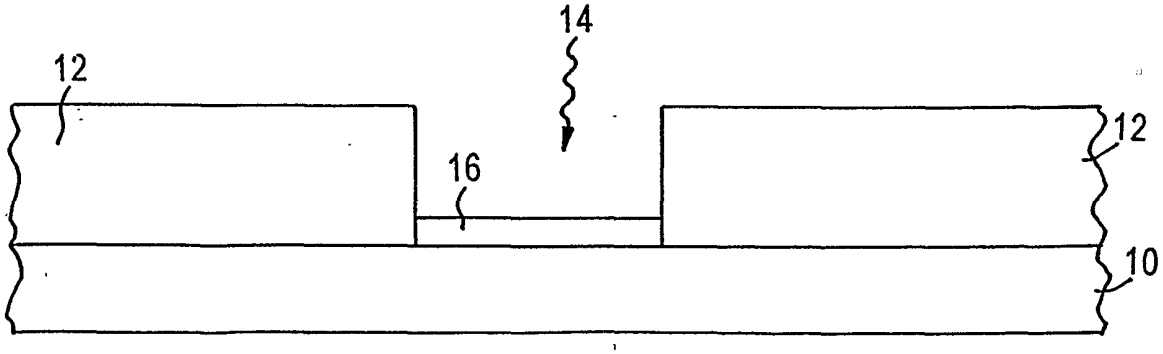

FIG. 4 (PRIOR ART)

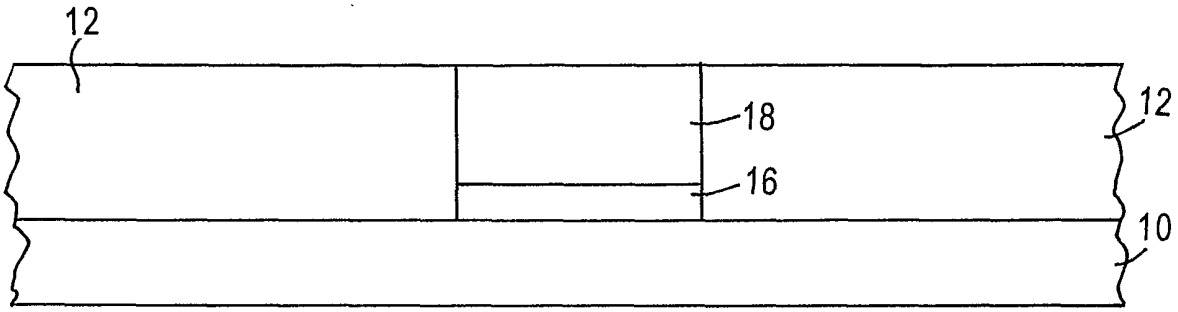

FIG. 5 (PRIOR ART)

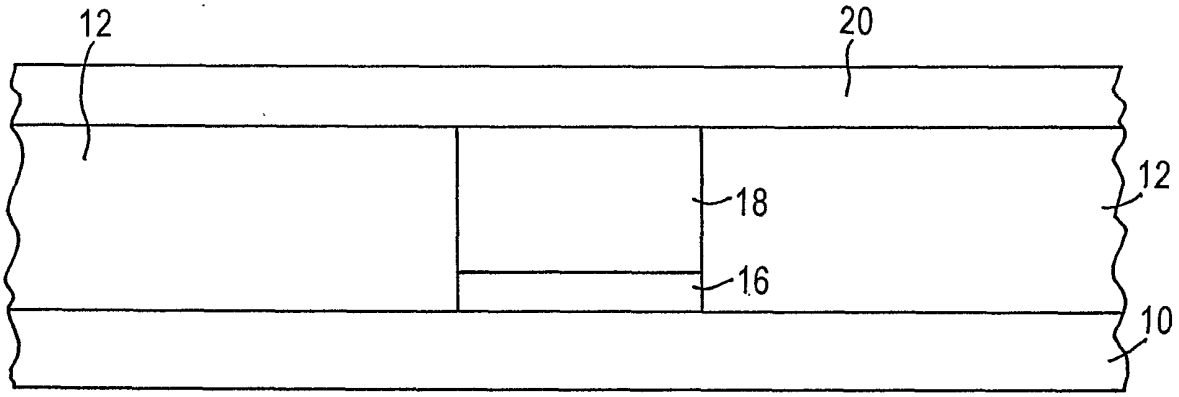

FIG. 6 (PRIOR ART)

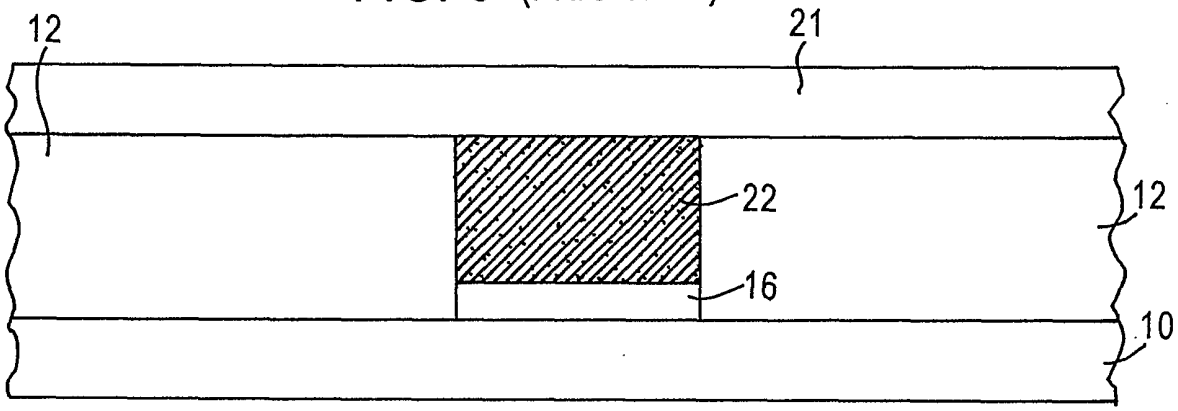

FIG. 7 (PRIOR ART)

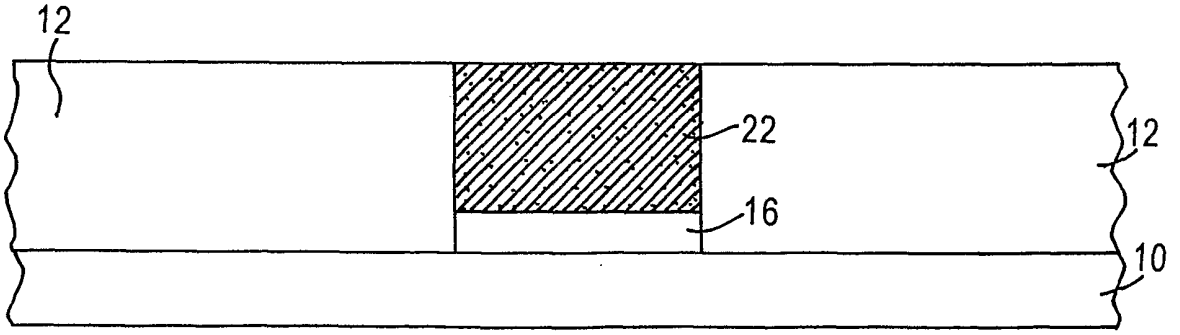

FIG. 8 (PRIOR ART)

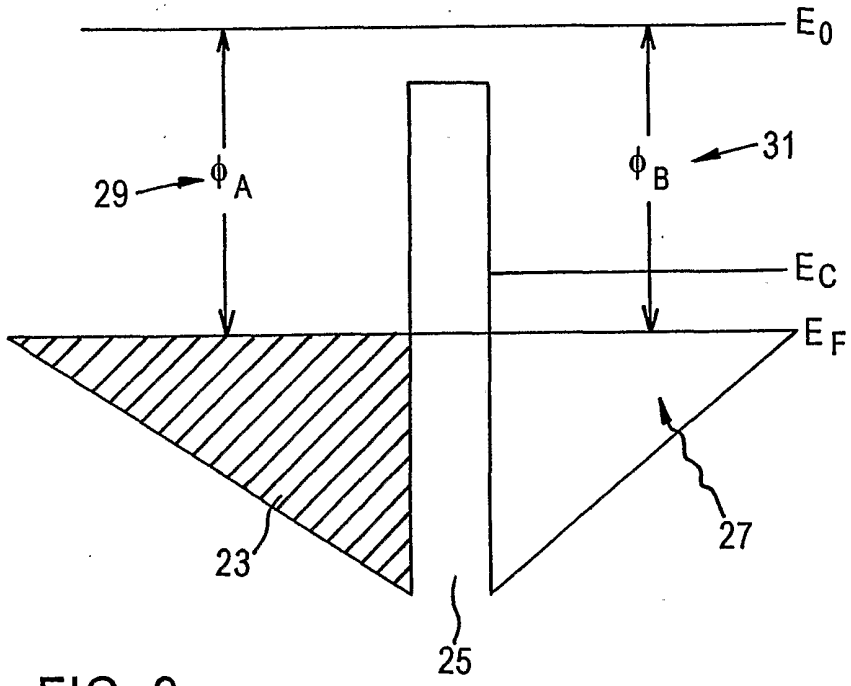

FIG. 9 (PRIOR ART)

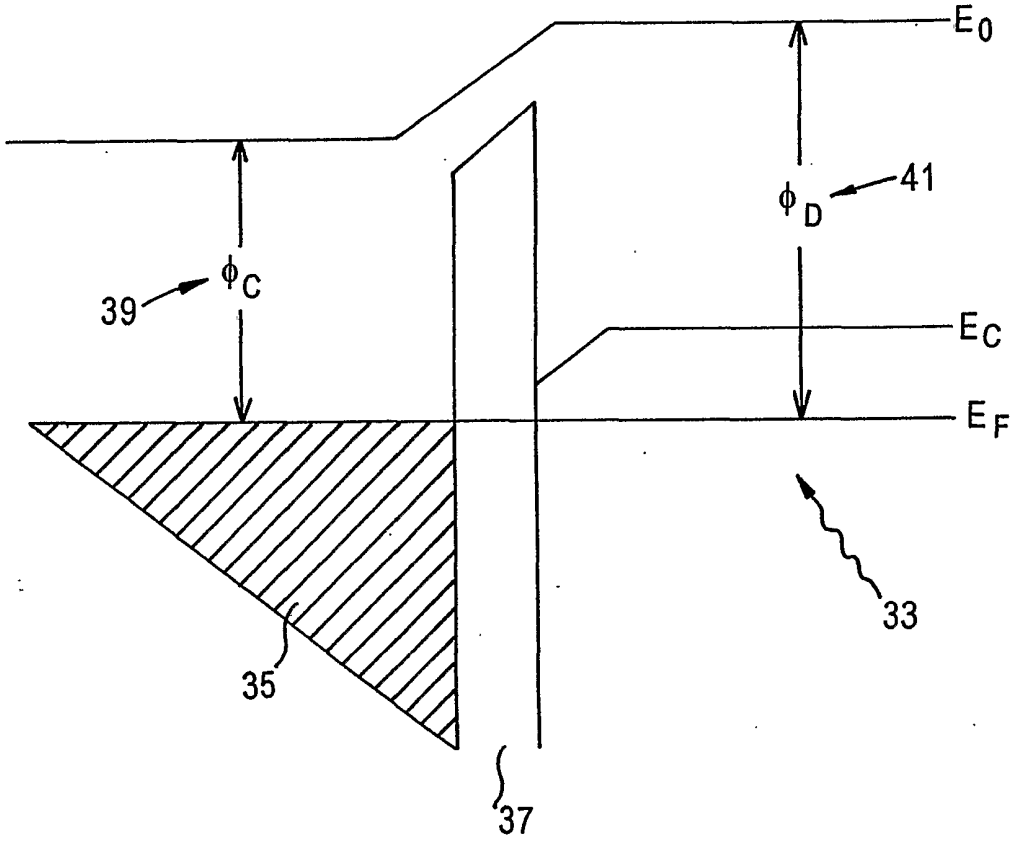

FIG. 10 (PRIOR ART)

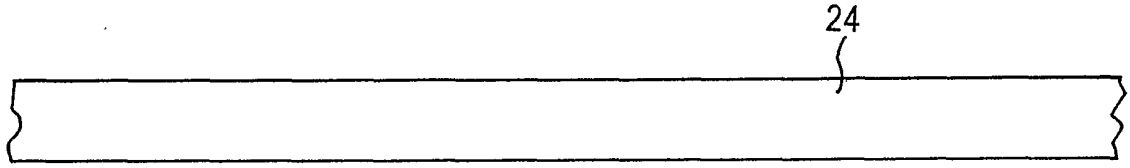

FIG. 11

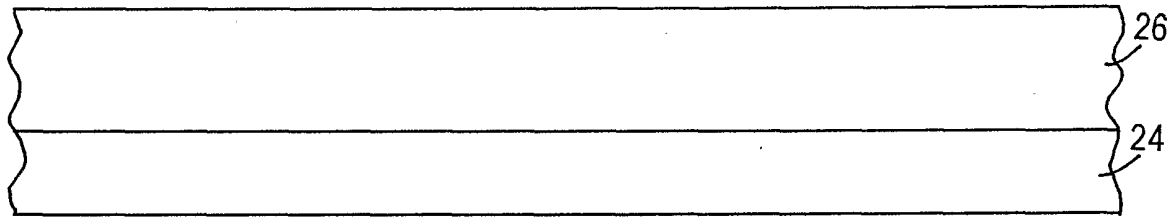

FIG. 12

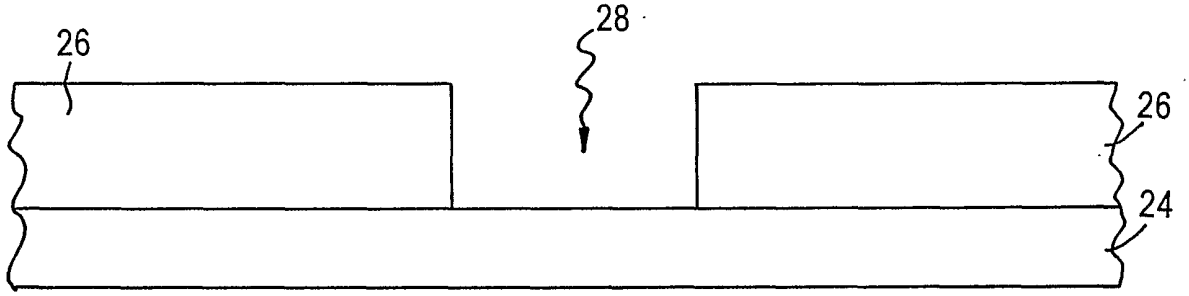

FIG. 13

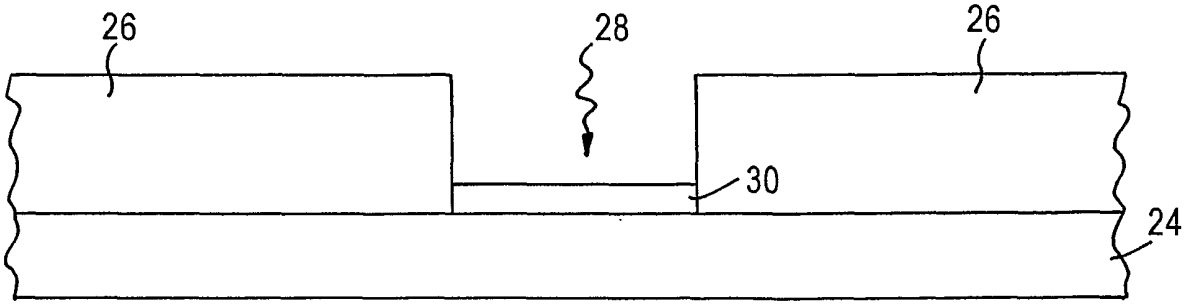

FIG. 14

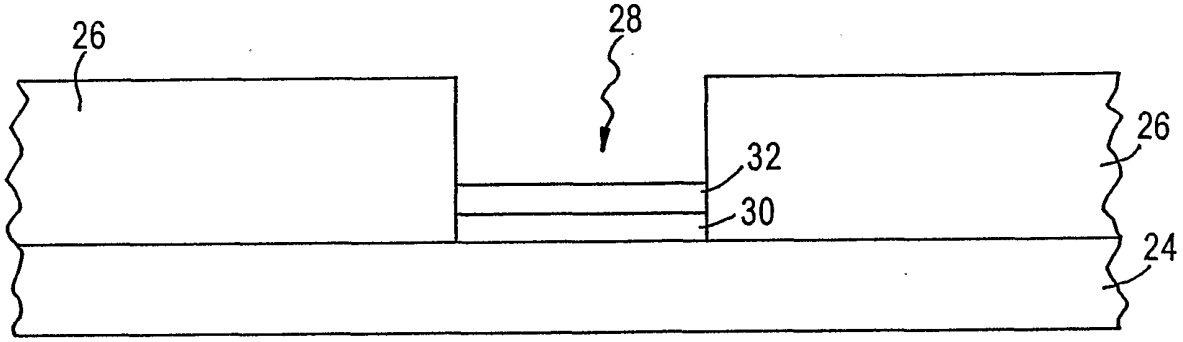

FIG. 15

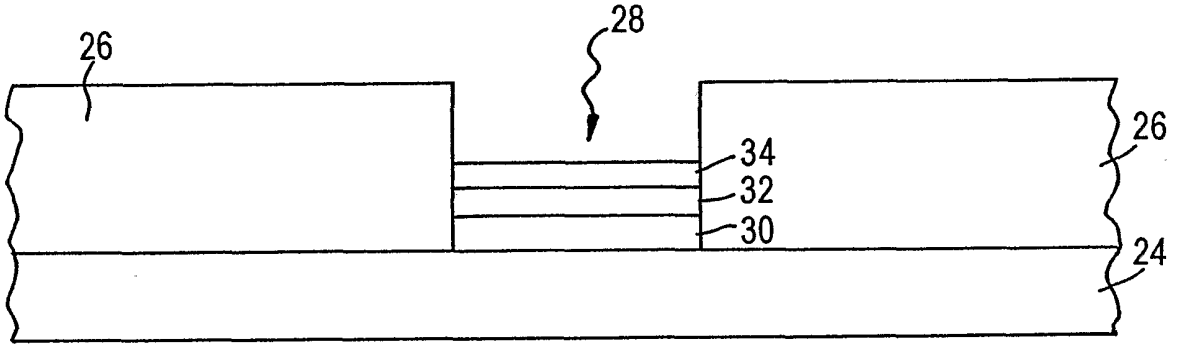

FIG. 16

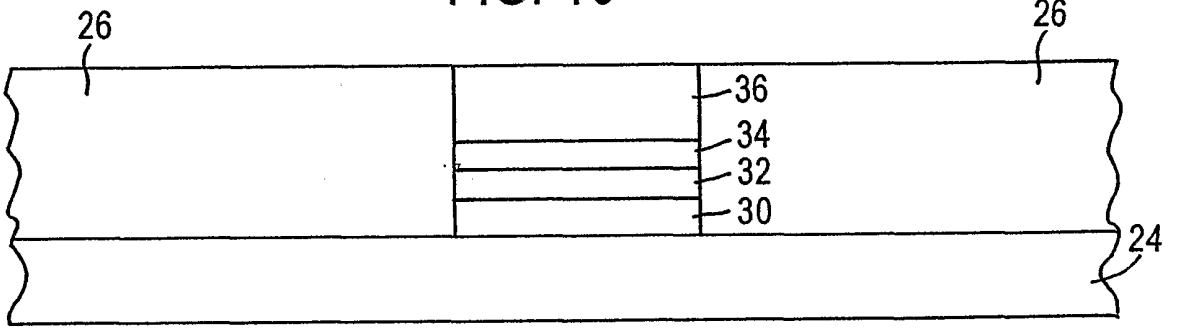

FIG. 17

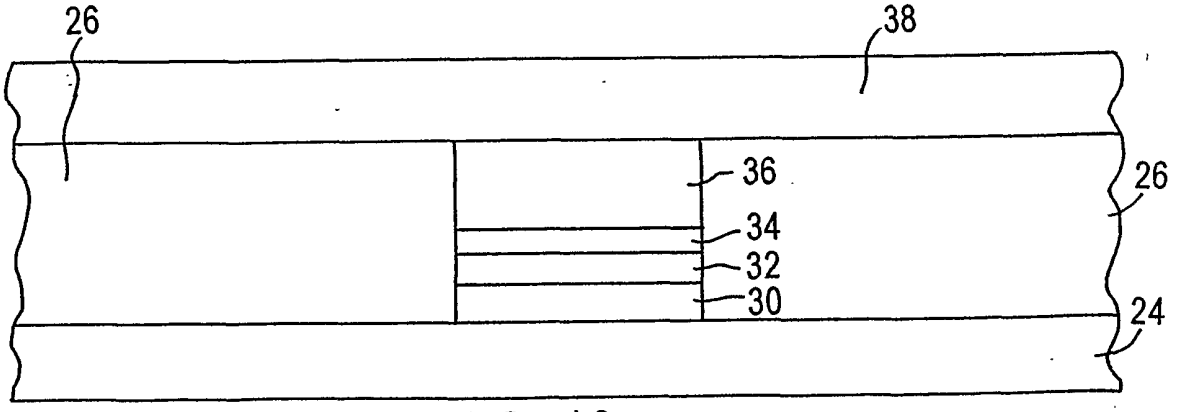

FIG. 18

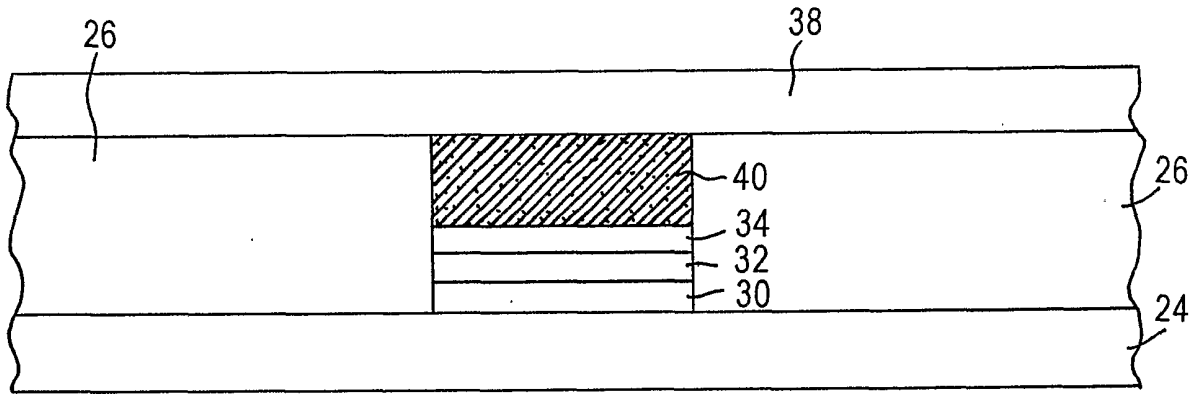

FIG. 19

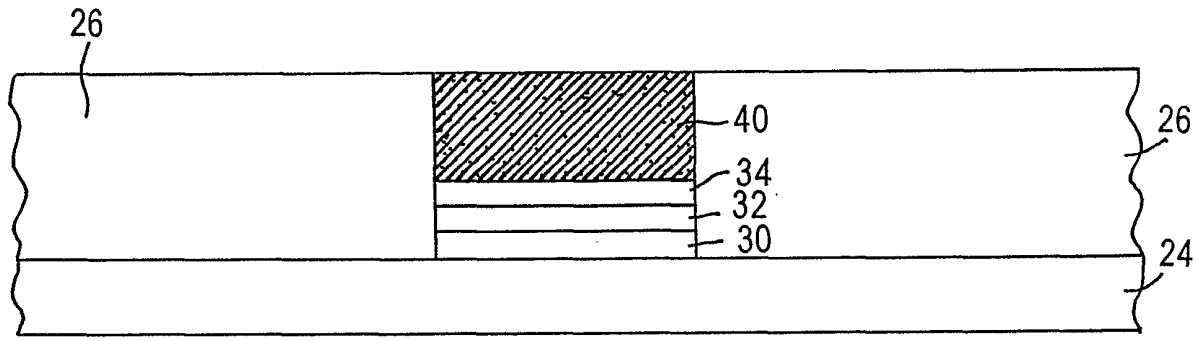

FIG. 20

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/43896

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 963 818 A (DOW DIANN M ET AL) 5 October 1999 (1999-10-05) column 7, line 64 -column 8, line 44; figures 14-17 ---	1-10
Y	US 5 861 340 A (BAI GANG ET AL) 19 January 1999 (1999-01-19) the whole document ---	1-10
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 449 (E-686), 25 November 1988 (1988-11-25) & JP 63 177538 A (FUJITSU LTD), 21 July 1988 (1988-07-21) abstract --- -/--	1-10

[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
30 July 2002	07/08/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boetticher, H

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 543 362 A (WU WEI E) 6 August 1996 (1996-08-06) the whole document ---	
A	US 5 889 331 A (BAI GANG) 30 March 1999 (1999-03-30) column 1, line 55-64 -----	

INTERNATIONAL SEARCH REPORT

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In ional Application No
PCT/US 01/43896

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5963818 A	05-10-1999	NONE	
US 5861340 A	19-01-1999	US 5818092 A	06-10-1998
JP 63177538 A	21-07-1988	NONE	
US 5543362 A	06-08-1996	NONE	
US 5889331 A	30-03-1999	NONE	