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(54) **METHODS OF COMMAND BASED AND CURRENT LIMIT CONTROLLED MEMORY DEVICE POWER UP**

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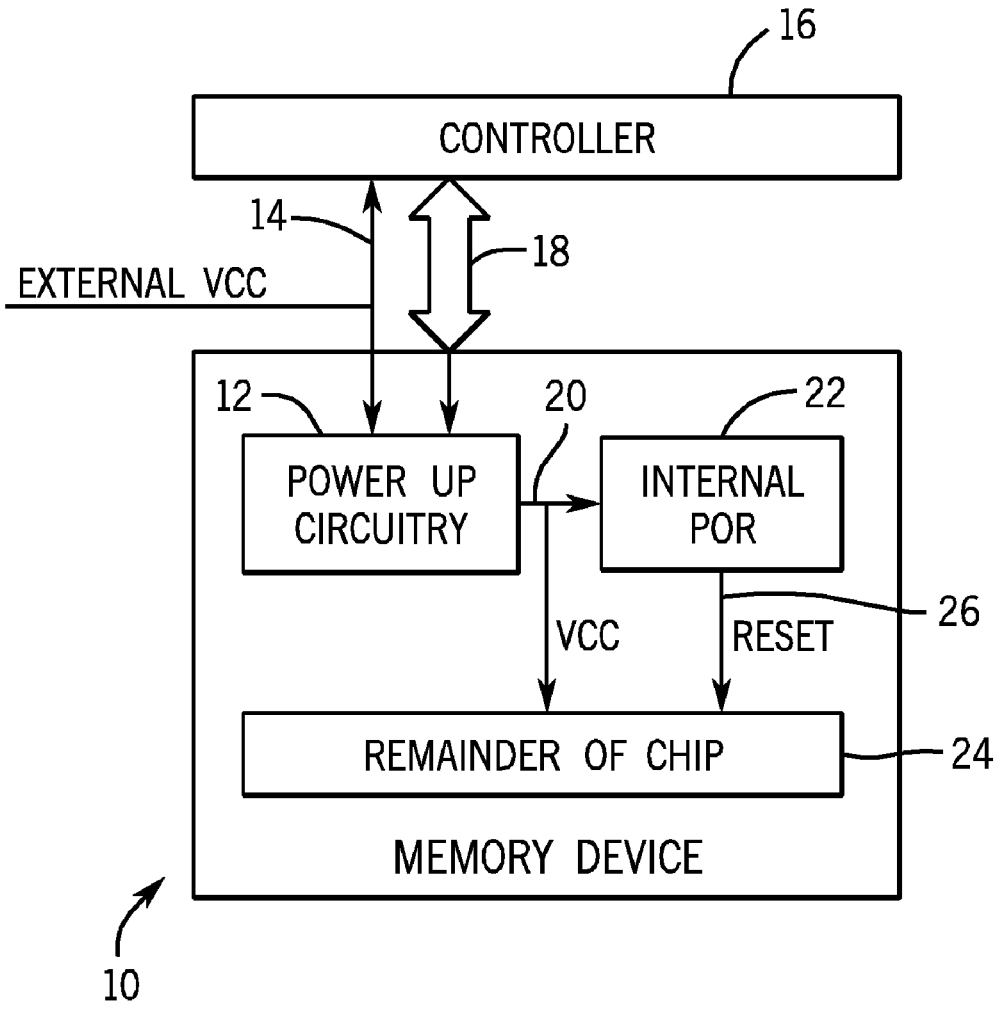
(57) **ABSTRACT**

Methods for powering up a memory device, for example, are disclosed. One such memory device includes power up circuitry configured to receive an external power supply and to provide an internal power supply to the memory device upon receipt of a command. The power up circuitry may be configured to provide the internal power supply limited to a peak current, or may be configured to provide the internal power supply not limited to a peak current. The memory device may be, for example, a synchronous dynamic random access memory (SDRAM) device or Flash memory.



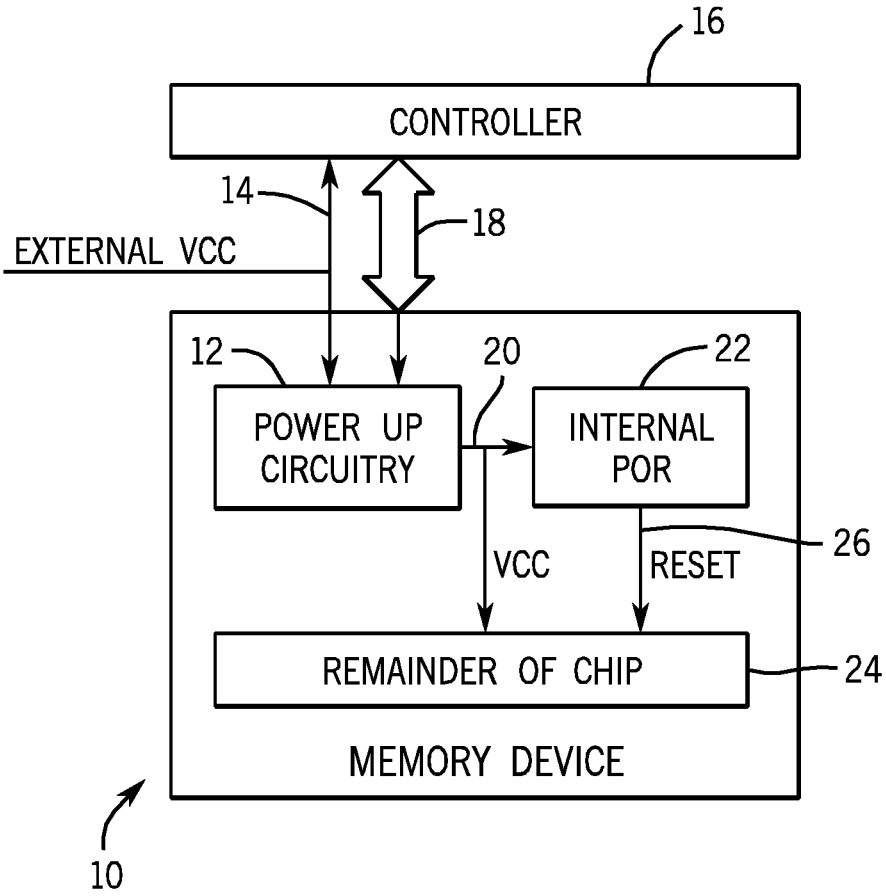

16
CONTROLLER
14
18
EXTERNAL VCC
12
20
22
POWER UP CIRCUITRY
INTERNAL POR
26
VCC
RESET
REMAINDER OF CHIP
24
MEMORY DEVICE
10

FIG. 1

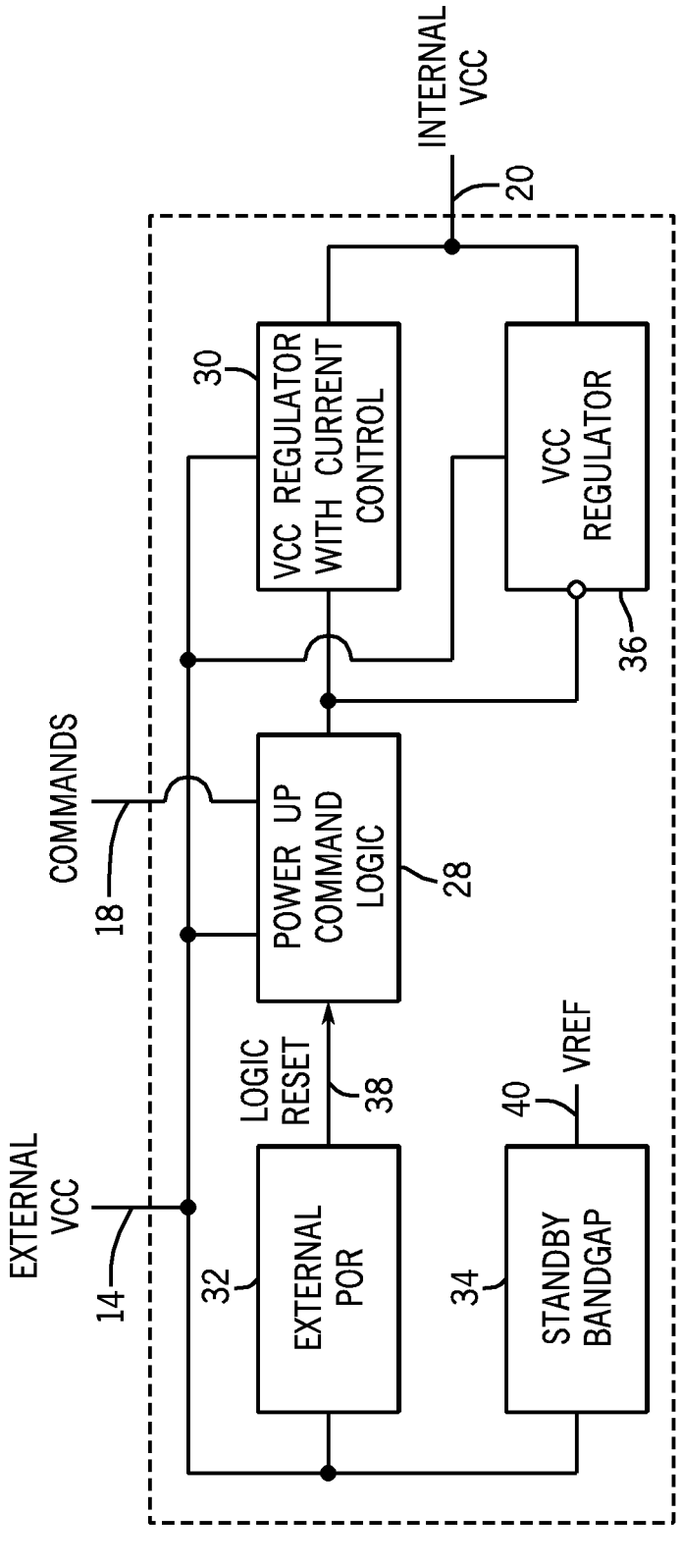

INTERNAL VCC
20
30
VCC REGULATOR WITH CURRENT CONTROL
VCC REGULATOR
36
COMMANDS
18
POWER UP COMMAND LOGIC
28
LOGIC RESET
38
40
VREF
EXTERNAL VCC
14
32
EXTERNAL POR
34
STANDBY BANDGAP
12

FIG. 2

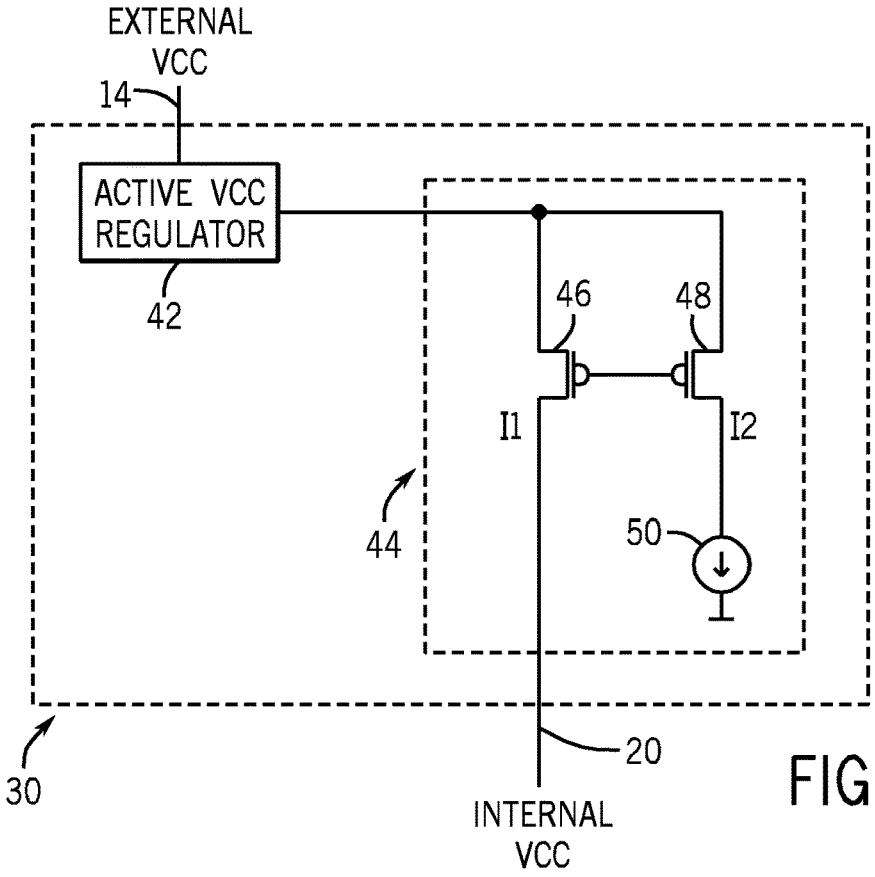

EXTERNAL
VCC
14
ACTIVE VCC
REGULATOR
42
46
48
I1
I2
44
50
30
20
INTERNAL
VCC

FIG. 3

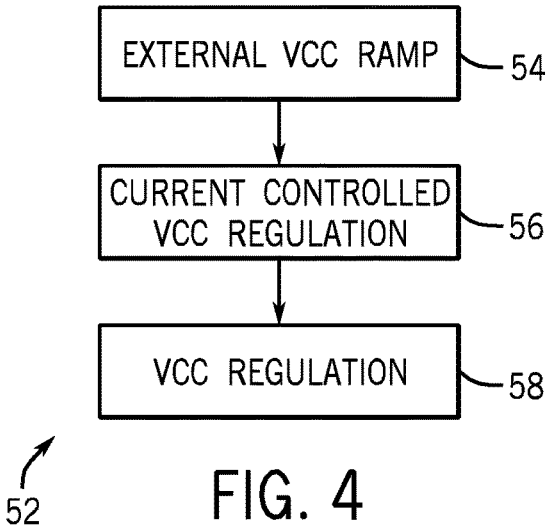

EXTERNAL VCC RAMP
54
CURRENT CONTROLLED
VCC REGULATION
56
VCC REGULATION
58
52

FIG. 4

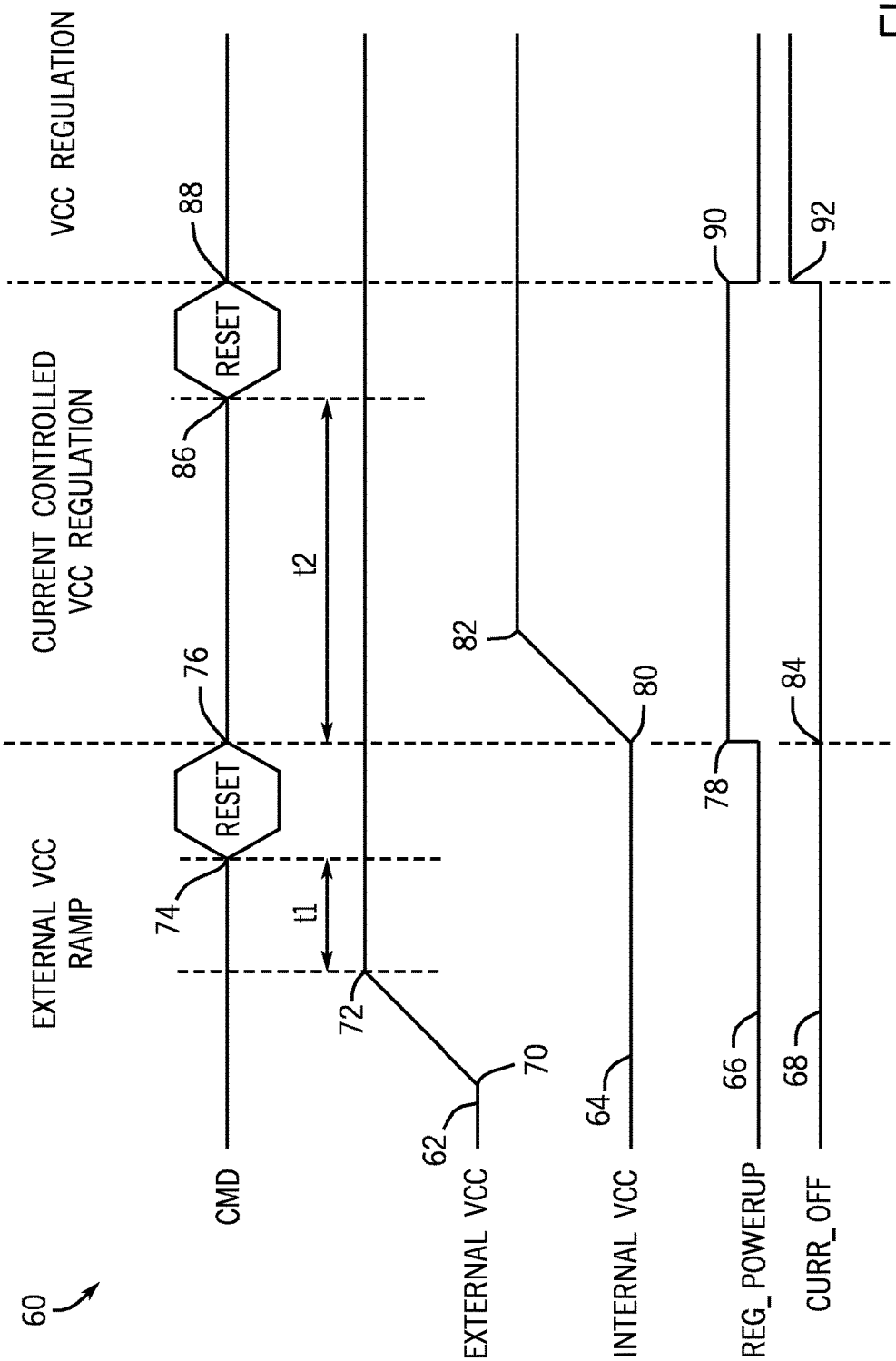
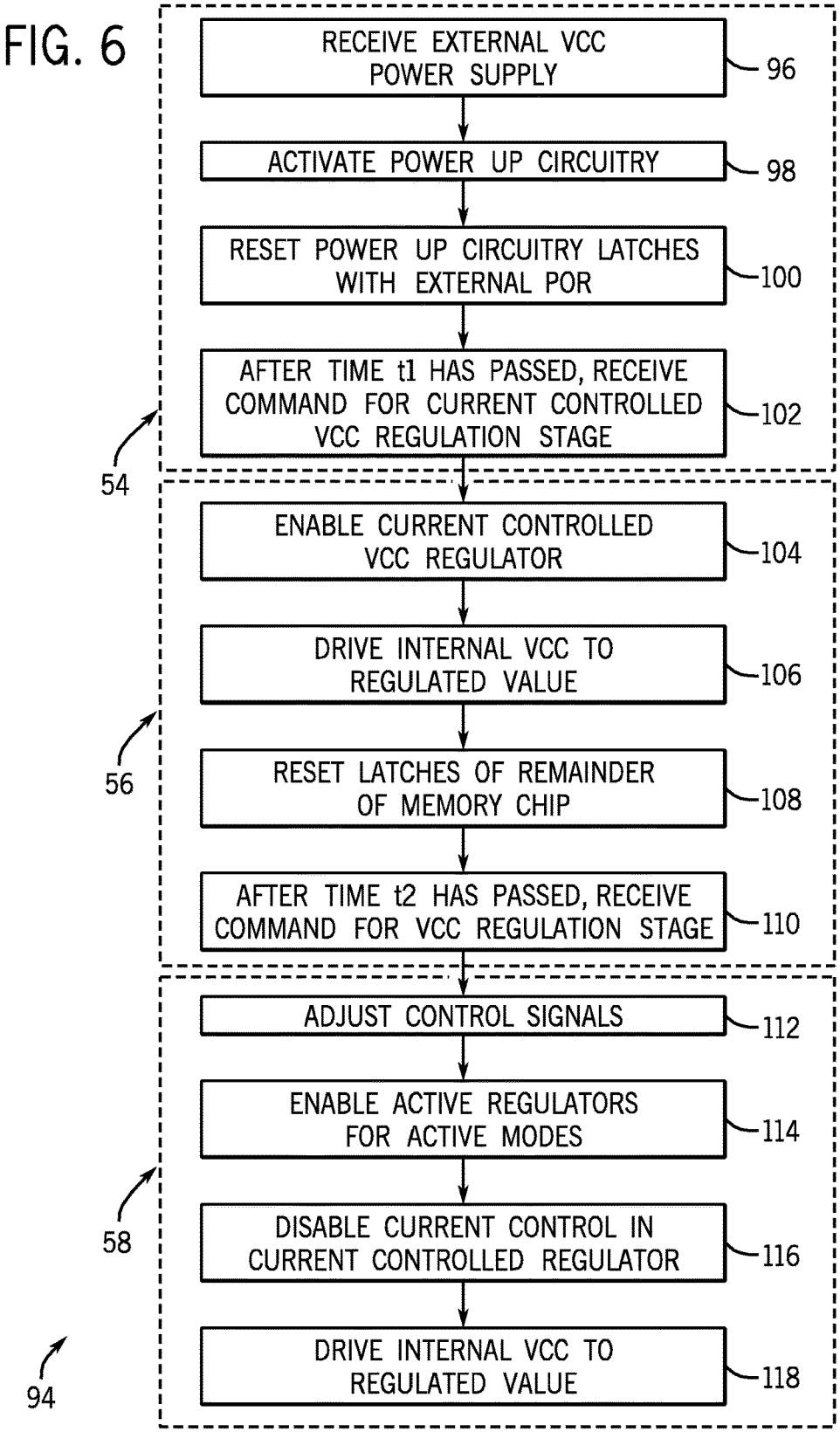

60
EXTERNAL VCC RAMP
CURRENT CONTROLLED VCC REGULATION
VCC REGULATION
CMD
EXTERNAL VCC
INTERNAL VCC
REG_POWERUP
CURR_OFF
RESET
RESET
t1
t2
62
64
66
68
70
72
74
76
78
80
82
84
86
88
90
92

FIG. 5

FIG. 6


RECEIVE EXTERNAL VCC POWER SUPPLY
96
ACTIVATE POWER UP CIRCUITRY
98
RESET POWER UP CIRCUITRY LATCHES WITH EXTERNAL POR
100
AFTER TIME t1 HAS PASSED, RECEIVE COMMAND FOR CURRENT CONTROLLED VCC REGULATION STAGE
102
54
ENABLE CURRENT CONTROLLED VCC REGULATOR
104
DRIVE INTERNAL VCC TO REGULATED VALUE
106
56
RESET LATCHES OF REMAINDER OF MEMORY CHIP
108
AFTER TIME t2 HAS PASSED, RECEIVE COMMAND FOR VCC REGULATION STAGE
110
ADJUST CONTROL SIGNALS
112
ENABLE ACTIVE REGULATORS FOR ACTIVE MODES
114
58
DISABLE CURRENT CONTROL IN CURRENT CONTROLLED REGULATOR
116
DRIVE INTERNAL VCC TO REGULATED VALUE
118
94

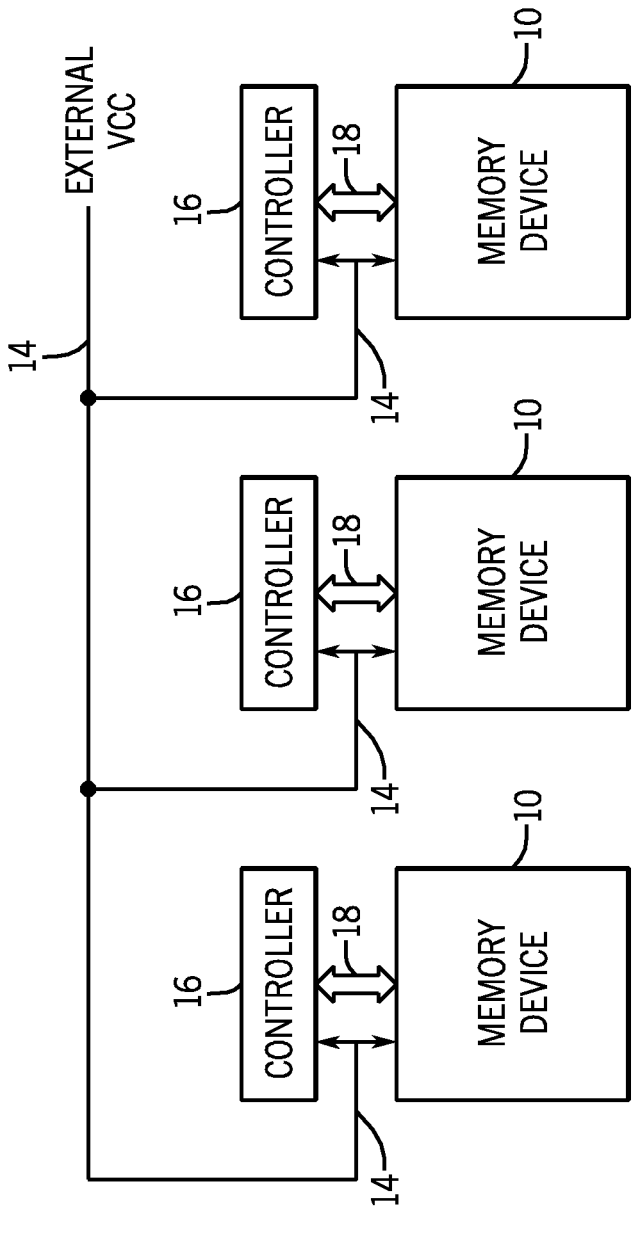



FIG. 7

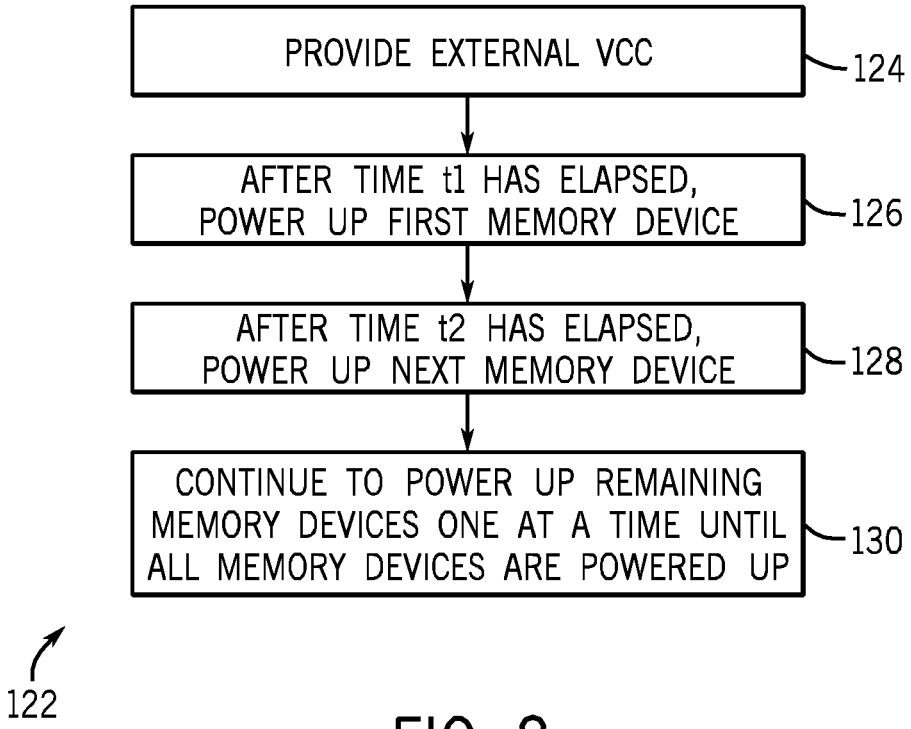

PROVIDE EXTERNAL VCC
124
AFTER TIME t1 HAS ELAPSED, POWER UP FIRST MEMORY DEVICE
126
AFTER TIME t2 HAS ELAPSED, POWER UP NEXT MEMORY DEVICE
128
CONTINUE TO POWER UP REMAINING MEMORY DEVICES ONE AT A TIME UNTIL ALL MEMORY DEVICES ARE POWERED UP
130
122

FIG. 8

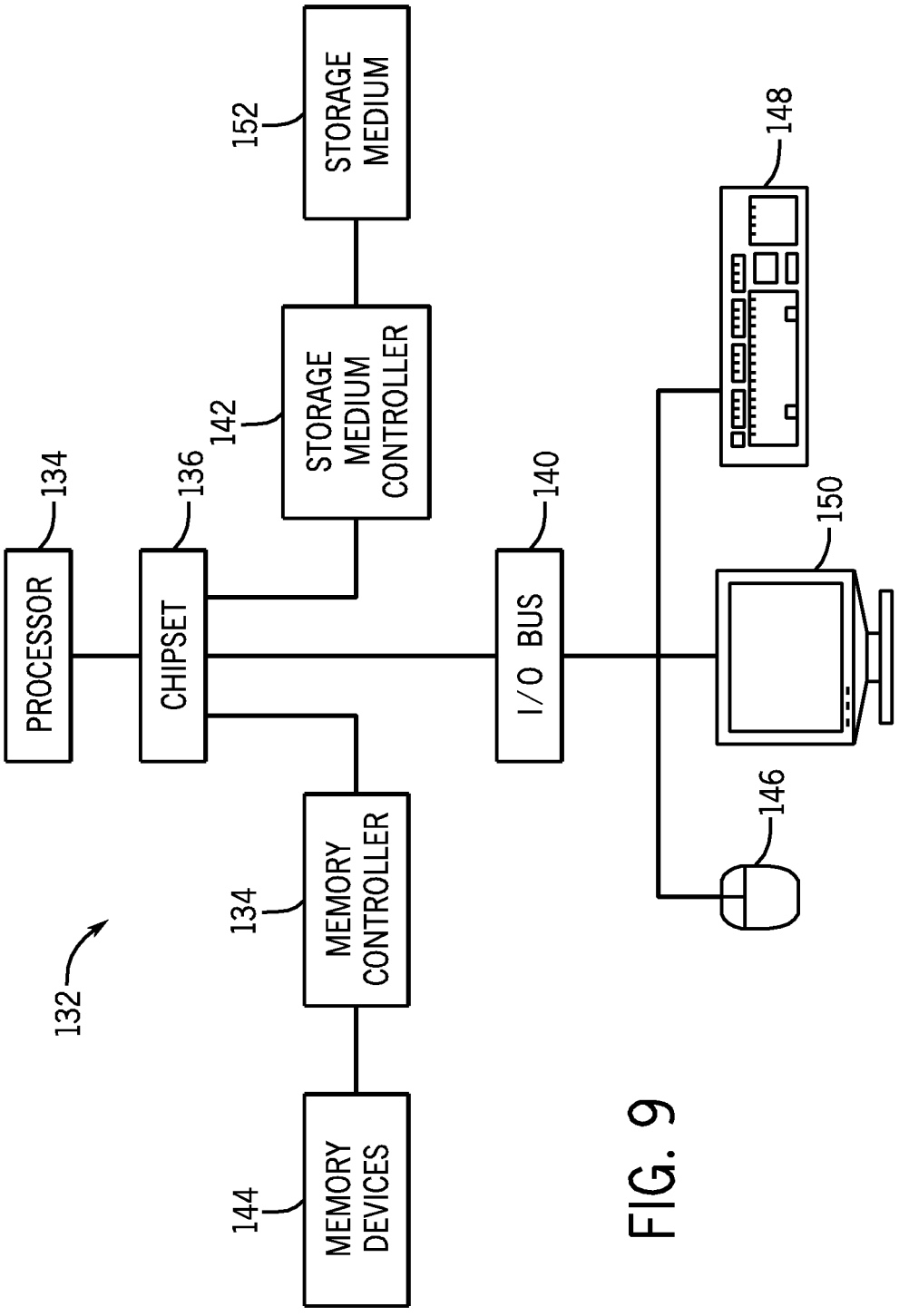

132
PROCESSOR
134
CHIPSET
136
STORAGE MEDIUM CONTROLLER
142
STORAGE MEDIUM
152
I/O BUS
140
MEMORY CONTROLLER
134
MEMORY DEVICES
144
148
150
146

FIG. 9

# METHODS OF COMMAND BASED AND CURRENT LIMIT CONTROLLED MEMORY DEVICE POWER UP

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a divisional of U.S. application Ser. No. 15/490,536, filed Apr. 18, 2017, which is a divisional of U.S. application Ser. No. 15/058,009, filed Mar. 1, 2016, now U.S. Pat. No. 9,640,227, which issued on May 2, 2017, which is a divisional of U.S. application Ser. No. 12/112,831, filed on Apr. 30, 2008, now U.S. Pat. No. 9,305,609, which issued on Apr. 5, 2016.

## BACKGROUND OF THE INVENTION

### Field of the Invention

**[0002]** The present invention relates generally to powering up memory devices and, more particularly, to powering up memory devices on command or in a current-controlled manner.

### Description of the Related Art

**[0003]** Electronic devices may employ one or more memory devices to store data for various purposes. For example, an electronic device may use a memory device to store data temporarily while the electronic device is active. Memory of this type may include random access memory (RAM). By way of example, synchronous dynamic random access memory (SDRAM) represents one form of RAM.

**[0004]** An electronic device may additionally or alternatively use a different memory device for long-term data storage when the electronic device is not active. Memory of this type may include non-volatile or Flash memory. By way of example, NAND Flash and NOR Flash represent common forms of Flash memory.

**[0005]** A memory controller may control a memory device using a variety of communication techniques; such techniques include standard parallel and serial peripheral interface (SPI). The memory controller may generally use commands to send data to be stored on a memory device, to access data stored on the memory device, or to adjust various settings regarding memory device operation.

**[0006]** When an electronic device powers up, the electronic device may provide a power supply voltage (VCC) to its electronic components, which may include one or more memory devices. When many electronic components of the electronic device power up in parallel, the electronic components may draw substantial power, which may place a constraint on the power supply of the electronic device. Moreover, many applications and standards may define peak current limits that should not be exceeded. A substantial draw of current on power up may not adhere to the standard.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** FIG. **1** is a block diagram representing a memory device having command based and current limit controlled power up circuitry in accordance with an embodiment;

**[0008]** FIG. **2** is a block diagram representing the command based and current limit controlled power up circuitry of FIG. **1**;

**[0009]** FIG. **3** is a block diagram representing a VCC regulator with current control in accordance with an embodiment;

**[0010]** FIG. **4** is a flowchart depicting a method of powering up the memory device of FIG. **1** in accordance with an embodiment;

**[0011]** FIG. **5** is a timing diagram associated with the method of FIG. **4**;

**[0012]** FIG. **6** is a flowchart describing the method of FIG. **4** in greater detail;

**[0013]** FIG. **7** is a block diagram representing a plurality of memory devices having command based and current limit controlled power up circuitry;

**[0014]** FIG. **8** is a flowchart describing a method of powering up the plurality of memory devices of FIG. **7** in accordance with an embodiment; and

**[0015]** FIG. **9** is a block diagram illustrating a system employing the memory device of FIG. **1** in accordance with an embodiment.

## DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

**[0016]** FIG. **1** illustrates a memory device **10** having command based and current limit controlled power up circuitry in accordance with an embodiment. The memory device **10** may be of any type of memory, such as synchronous dynamic random access memory (SDRAM), NAND Flash memory, or NOR Flash memory. The memory device **10** includes power up circuitry **12**, which may receive power from an external VCC **14** power supply. The external VCC **14** does not supply power directly to remaining circuitry of the memory device **10**, which could draw a substantial amount of current powering up. Instead, the external VCC **14** supplies power to the power up circuitry **12**, which includes circuitry for a controlled power up of the memory device **10**.

**[0017]** Once the power up circuitry **12** has powered up, a controller **16** may send a command **18** to the power up circuitry **12** to begin powering up the remaining circuitry of the memory device **10**. It should be noted that the controller **16** may communicate with the memory device **10** using any communication scheme. Thus, the controller **16** may issue the command **18** to the memory device **10** using a serial peripheral interface (SPI) protocol or a standard parallel protocol, for example.

**[0018]** When the controller **16** sends a first command **18** to the power up circuitry **12**, the power up circuitry **12** may enter a current controlled VCC regulation phase in powering up the memory device **10**. The power up circuitry **12** may supply an internal VCC **20** to an internal power on reset (POR) circuit **22** and to circuitry of a remainder of the chip **24**. To prevent the remainder of the chip **24** from drawing excessive current while powering up, the internal VCC **20** may be limited to a peak current limit. The peak current limit may be determined by a specification or a standard, or may vary by application. For example, the peak current limit may be between 4 milliamps (mA) and 20 mA to comport with certain memory device standards and to prevent current spikes while the remainder of the chip **24** is powered on.

**[0019]** When the internal POR circuit **22** receives the internal VCC **20** power, the internal POR circuit **22** may transmit a reset signal **26** to the remainder of the chip **24** to reset the latches therein. After the remainder of the chip **24** has powered on and the latches of the remainder of the chip

24 have been reset, the controller 16 may issue a second command 18 to the power up circuitry 12. When the power up circuitry 12 receives the second command 18, the power up circuitry 12 may subsequently enter a normal VCC regulation mode. In the normal VCC regulation mode, the internal VCC 20 is no longer limited to a peak current limit, but rather may supply additional current as needed to achieve a specified reference voltage.

[0020] FIG. 2 depicts the power up circuitry 12 of FIG. 1 in greater detail. As shown in FIG. 2, the external VCC 14 supplies power to a number of subcircuits which make up the power up circuitry 12. The subcircuits may include power up command logic 28, a VCC regulator with current control 30, an external power on reset (POR) circuit 32, a standby band gap circuit 34, and a VCC regulator 36 without current control. It should be appreciated that the number of regulators may vary based on design constraints and applications. For example, a greater number of regulators may be employed to reduce possible voltage drops due to internal resistance in the memory device 10.

[0021] Upon receiving power from the external VCC 14, the external POR circuit 32 may generate a reset signal 38. The reset signal 38 resets all of the latches in the power up command logic 28. The amount of time required for the external POR circuit 32 to reset the latches in the power up command logic 28 is referred to herein as a time t1, which may vary depending on the logic configuration and design and may last approximately 250 microseconds (μs). Once the time t1 has passed, the power up command logic 28 may receive a first command 18 from the controller 16.

[0022] Upon receipt of the first command 18 from the controller 16, the power up command logic 28 may begin to power up other circuitry in the memory device 10 by activating the VCC regulator with current control 30. For example, the power up command logic 28 may issue a signal both to the VCC regulator with current control 30 and to the VCC regulator 36. Based on logic within the VCC regulator with current control 30 and the VCC regulator 36, only the VCC regulator with current control 30 may be activated by the signal.

[0023] Once activated, the VCC regulator with current control 30 may output the internal VCC 20 power supply. As discussed above, the internal VCC 20 supplies power to the internal POR 22 and the remainder of the chip 24. It should be noted that the internal VCC 20 power supply from the VCC regulator with current control 30 may be limited to a peak current. For example, the VCC regulator with current control 30 may limit the peak current to between 4 mA and 20 mA, which may prevent the remainder of the chip 24 from drawing large spikes of current from the external VCC 14.

[0024] As noted in the discussion associated with FIG. 1 above, the reset signal 26 from the internal POR circuit 22 serves to reset the latches in the remainder of the chip 24. The amount of time required for the internal POR circuit 22 to reset the latches in the power up command logic 28 is referred to herein as a time t2, which may vary depending on the configuration and design of the remainder of the chip 24 and may last approximately 250 μs. Once the time t2 has elapsed from the activation of the VCC regulator with current control 30, the power up command logic 28 may receive a second command 18 from the controller 16. Upon receipt of the second command, the power up command logic 28 may activate the VCC regulator 36 and to deactivate the current control aspect of the VCC regulator with current control 30, which may subsequently operate in tandem to output the internal VCC 20 power supply.

[0025] The standby bandgap circuit 34 may supply a reference voltage 40 (also labeled Vref) to the VCC regulator 36 and the VCC regulator with current control 30 (with current control now deactivated). The VCC regulator 36 and the VCC regulator with current control 30 (with current control deactivated) may both thereafter output the internal VCC 20 at the reference voltage 40 without limiting the current drawn from the external VCC 14.

[0026] FIG. 3 represents a more detailed view of the VCC regulator with current control 30 of the power up circuitry 12 of FIG. 2. The VCC regulator with current control 30 may include an active VCC regulator 42 and a current limiter circuit 44. The active VCC regulator 42 receives power from the external VCC 14 and supplies power at the proper voltage to the remainder of the chip 24. The current limiter circuit 44 limits the amount of current output to the internal VCC 20 to a specified value.

[0027] The current limiter circuit 44 may include, for example, a current mirror formed by a transistor 46 with a gate terminal tied to a gate terminal of a transistor 48, as illustrated in FIG. 3. A current source 50 may supply a reference current I2 across the transistor 48, which may be mirrored across transistor 46 as a current I1 according to a relationship between the ratios of channel width to channel length (W/L) of each transistor 46 and 48,

$$I1 = \frac{(W/L)_{46}}{(W/L)_{48}} I2.$$

The (W/L) ratio of transistor 46 may be 85 times that of the transistor 48, and the current source 50 may supply a reference current I2 of 140-175 mA. Thus, the current I1 output to the internal VCC 20 by the VCC regulator with current control 30 may be approximately 18 mA. The current source 50 may represent any current source, such as the current source described in U.S. patent application Ser. No. 12/037,649, assigned to Micron Technology, Inc.

[0028] Turning to FIG. 4, a flowchart 52 depicts a method of powering up the memory device 10 using command based and current limit controlled power up circuitry, in accordance with an embodiment. Initially, an external VCC ramp phase 54 may begin when the external VCC 14 initially ramps up, supplying power to the power up circuitry 12 of the memory device 10 and to the controller 16. During the external VCC ramp phase 54, no additional circuitry of the memory device 10 draws power from the external VCC 14. Once a sufficient time t1 has elapsed to permit the logic of the power up circuitry 12 to reset, the controller 16 may send a first command 18 to the power up circuitry 12, causing the power up circuitry 12 to begin a current controlled VCC regulation phase 56.

[0029] In the current controlled VCC regulation phase 56, the power up circuitry 12 supplies the internal VCC 20 to the internal POR circuit 22 and to the remainder of the chip 24. However, for the duration of the current controlled VCC regulation phase 56, the current is limited to prevent current spikes drawn on the external VCC 14 while the remaining circuitry of the memory device 10 powers up. Once a sufficient time t2 has elapsed to permit the logic of the

remainder of the chip **24** to reset, the controller **16** may send a second command **18** to the power up circuitry **12** to initiate a VCC regulation phase **58**.

**[0030]** The VCC regulation phase **58** represents a final phase in powering up the memory device **10**. In the VCC regulation phase **58**, the power up circuitry **12** supplies the internal VCC **20** to the remainder of the chip **24** without limiting current. Thus, the VCC regulation phase **58** may represent normal memory device **10** operation once the device has powered up.

**[0031]** Turning to FIG. **5**, a timing diagram **60** corresponds to the flowchart **52** of FIG. **4**. The leftmost column of the timing diagram **60** indicates various voltage signals employed by the memory device **10**. Such voltage signals include CMD, representing commands **18** from the controller **16**; External VCC, representing the external VCC **14**; Internal VCC, representing the internal VCC **20**; reg_power up, representing a signal sent by the power up command logic **28** to activate the VCC regulator with current control **30**; and curr_off, representing a signal sent by the power up command logic **28** to deactivate current limiter circuitry **44**.

**[0032]** A first point **62** represents a point when the memory device **10** is off and no power is supplied at the start of the external VCC ramp phase **54**. Accordingly, the external VCC **14** is low at point **62**. Correspondingly, at point **64**, the internal VCC **20** is also low. Representing the initial states of the power up command logic **28**, at point **66**, the VCC regulator power up signal reg_power up is low, and at point **68**, the current control off signal curr_off is also low.

**[0033]** At point **70**, the external VCC **14** begins to ramp up rising until reaching a maximum at point **72**. Between points **70** and **72**, the power up circuitry **12** is powered up. As noted on the timing diagram **60**, the time t**1** begins once the external VCC **14** has ramped to its peak at point **72**. From the discussion above, the time t**1** represents the amount of time for the external POR circuit **32** to reset the latches in the power up command logic **28**. The time t**1** may vary depending on the logic configuration and design and may last approximately 250 μs.

**[0034]** After the time t**1** has elapsed, the controller **16** may send the first command **18** to the power up command logic **28** at point **74**. Terminating at point **76**, the command **18** may instruct the power up command logic **28** to initiate a subsequent power up phase. Although the command **18** illustrated in the timing diagram **60** is a reset command, any predetermined command may be chosen. As should be appreciated, the command **18** should be chosen such that the power up command logic **28** may initiate the current controlled VCC regulation phase **58** upon the receipt of the first command **18**.

**[0035]** With further reference to the timing diagram **60** of FIG. **5**, when the command **18** is received at point **76**, the current controlled VCC regulation phase **56** may begin. The power up command logic **28** subsequently sets the VCC regulator power up signal reg_power up to high at point **78**, which activates the VCC regulator with current control **30**. The VCC regulator with current control **30** may thereafter begin to output the internal VCC **20** at point **80**. The voltage of the internal VCC **20** may ramp until a reference voltage is reached at point **82**.

**[0036]** During the current controlled VCC regulation phase **56**, only the VCC regulator with current control **30** is activated. This result arises because the VCC regulator power up signal reg_power up is high while the current control off signal curr_off is low, as indicated by point **84**. It should be recalled that the time t**2**, which takes place from the start of the current controlled VCC regulation phase **56**, represents the amount of time for the internal POR circuit **22** to reset the latches in the remainder of the chip **24**. The time t**2** may vary depending on the configuration and design of the remainder of the chip **24** and may last approximately 250 μs.

**[0037]** After the time t**2** has elapsed, the controller **16** may send a second command **18** to the power up command logic **28** at point **86**. Terminating at point **88**, the second command **18** may instruct to the power up command logic **28** to initiate a subsequent power up phase. Although the second command **18** illustrated in the timing diagram **60** is a reset command, any predetermined command may be chosen. As should be appreciated, the second command **18** should be chosen such that the power up command logic **28** may initiate the VCC regulation phase **58** upon the receipt of the second command **18**.

**[0038]** Upon receipt of the second command **18**, the VCC regulation phase **58** may begin. As described above, the VCC regulation phase **58** represents the start of normal memory device **10** operation. Thus, the power up command logic **28** subsequently deactivates the current limiter circuit **44** in the VCC regulator with current control **30** and activates the VCC regulator **36**. This is reflected by points **90** and **92** in the timing diagram **60**, which indicate that the VCC regulator power up signal is set to low at point **90** and that the current control off signal is set to high at point **92**. Subsequently, the VCC regulator **36** and the VCC regulator with current control **30** (with current control now deactivated) may provide a constant voltage supply to the memory device **10**.

**[0039]** FIG. **6** illustrates a flowchart **94** depicting a more detailed description of the method outlined in the flowchart **52** of FIG. **4**. In the flowchart **94**, steps **96** through **102** take place during the external VCC ramp phase **54**. In step **96**, the external VCC **14** power supply ramps up. The power up circuitry **12** of the memory device **10** receives power from the external VCC **14** in step **98**, and the power up circuitry **12** begins to power up. At this point, the standby band gap circuit **34** may begin to output a reference voltage **40** (also labeled Vref), which may be used in subsequent power up phases by the VCC regulator with current control **30** and the VCC regulator **36**. In a next step **100**, the external POR circuit **32** supplies a reset signal **38** to the power up command logic **28**, resetting the latches of the power up command logic **28**. A final step **102** of the external VCC ramp phase **54** takes place after the time t**1** has elapsed, allowing sufficient time for the latches of the power up command logic **28** to reset. In step **102**, the first command **18** may be received by the power up command logic **28**, in advance of the current controlled VCC regulation phase **56**.

**[0040]** Steps **104-110** of the flowchart **94** take place during the current controlled VCC regulation phase **56**. In step **104**, the power up command logic **28** may provide a signal, such as the VCC regulator power up signal, reg_power up, indicated in the timing diagram **60** of FIG. **5**, to logic within the VCC regulator with current control **30** and the VCC regulator **36**. Based on the logic within the VCC regulator with current control **30** and the VCC regulator **36**, only the VCC regulator with current control **30** may be activated. In step **106**, the VCC regulator with current control **30** drives the internal VCC **20** to the regulated value without exceed-

ing a maximum peak current limit. For example, the peak current limit may be set to between 4 mA to 20 mA, preventing spikes in current drawn from the external VCC **14**. In a next step **108**, the internal POR circuit **22** supplies a reset signal **26** to the remainder of the chip **24**, resetting the latches of the remainder of the chip **24**. A final step **110** of the current controlled VCC regulation phase **56** takes place after the time t**2** has elapsed, allowing sufficient time for the latches of the remainder of the chip **24** to reset. In step **110**, the power up command logic **28** may receive the second command **18** in advance of the next phase in powering up, normal VCC regulation phase **58**.

**[0041]** Referring further to the flowchart **94** of FIG. **6**, steps **112**-**118** represent steps taking place during the normal VCC regulation phase **58**. In step **112**, after receiving the second command **18**, the power up command logic **28** may set the VCC regulator power up signal reg_power up to low and set the current control off signal curr_off is to high. In step **114**, the active regulators in the VCC regulator with current control **30** and the VCC regulator **36** may be enabled for active modes as the VCC regulator power up signal reg_power up is set low, and in step **116**, the current limiter circuit **44** in the VCC regulator with current control **30** may be disabled as the current control off signal curr_off is set high. Thus, by step **118**, the VCC regulator with current control **30** (with the current control disabled) and the VCC regulator **36** may operate in tandem to drive the internal VCC **20**. During step **118**, the internal VCC **20** may be driven to the reference voltage **40** without the active current limitation of the current controlled VCC regulation phase.

**[0042]** Turning next to FIG. **7**, a block diagram **120** depicts a plurality of memory devices **10** having command based and current limit controlled power up circuitry in accordance with an embodiment. As shown in the block diagram **120**, the external VCC **14** supplies power to the plurality of memory devices **10** and to a corresponding plurality of controllers **16**. Though the block diagram **120** depicts only three memory devices **10**, any number of memory devices **10** may be employed. Moreover, it should be appreciated that, alternatively, a single controller **16** may control all of the memory devices **10** in lieu of the plurality of controllers **16**. Because powering up numerous memory devices **10** in parallel may draw excessive current from the external VCC **14**, the command based and current limit controlled power up circuitry of the memory devices **10** may be employed to power each memory device **10** individually upon issuance by the controllers **16** of the commands **18**.

**[0043]** FIG. **8** is a flowchart **122** depicting a method of powering up the plurality of memory devices **10** of the block diagram **120** of FIG. **7**. In a first step **124**, the external VCC **14** is ramped up and supplied to the plurality of memory devices **10** and the plurality of controllers **16**. The first step **124** represents the external VCC ramp phase **54** of the flowchart **52** of FIG. **4**.

**[0044]** Step **126** takes place after a sufficient time t**1** has elapsed for the latches of the command based and current limit controlled power up circuitry of the memory devices **10** to reset. In step **126**, a first of the controllers **16** may issue a command **18** to a first of the memory devices **10** to initiate the current controlled VCC regulation phase **56** in the first of the memory devices **10**.

**[0045]** Step **128** takes place after a sufficient time t**2** has elapsed for the latches of the remainder of the circuitry of the first of the memory devices **10** to reset. In step **128**, the first of the controllers **16** may complete the power up of the first of the memory devices **10** by issuing a command **18** for the first of the memory devices **10** to initiate the VCC regulation phase **58**. At the same time, a second of the controllers **16** may issue a command **18** to a second of the memory devices **10** to initiate the current controlled VCC regulation phase **56** in the second of the memory devices **10**.

**[0046]** As indicated in step **130**, the above process may continue until all of the memory devices **10** have powered up. In this way, the current drawn by all of the memory devices **10** may be limited substantially from powering all of the memory devices **10** in parallel.

**[0047]** FIG. **9** illustrates a system **132** employing one or more memory devices **10** having command based and current limit controlled power up circuitry. The system **132** may form, for example, a desktop computer, a notebook computer, a server, a handheld computer, or a portable device, such as a portable phone or media player. The system **132** may include one or more processors, such as a central processing unit ("CPU") **134**. The CPU **134** may be used individually or in combination with other CPUs. In one embodiment of the invention, the CPU **134** may include one or more memory devices **10**.

**[0048]** A chipset **136** may be operably coupled to the CPU **134**. The chipset **136** operates as a communication pathway for signals between the CPU **134** and other components of the system **132**. Such other components include, for example, a memory controller **134**, which may, in some embodiments, represent the controller **16**; an input/output bus **140**; and a storage medium controller **142**, which may, in some embodiments, additionally or alternatively represent the controller **16**. As should be appreciated by those skilled in the art, the memory controller **134**, the input/output bus **140**, and the storage medium controller **142** may alternatively be incorporated into the chipset **136**.

**[0049]** One or more memory devices **144**, which may represent one or more memory devices **10** in some embodiments, may be operably coupled to the memory controller **134**. The memory devices **144** may represent volatile memory, such as synchronous dynamic random access memory (SDRAM), but may also represent non-volatile memory such as Flash memory. It should be noted that while the memory devices **144** may represent one or more memory devices **10**, in some embodiments the memory devices **144** may represent ordinary memory without command based and current limit controlled power up circuitry. The input/output bus **140** may permit the chipset **136** to communicate with a pointing input device **146**, such as a mouse; a keyboard input device **148**, such as a keyboard; and a display device **150**.

**[0050]** A non-volatile storage medium **152**, which may represent one or more memory devices **10** in some embodiments, may be operably coupled to the storage medium controller **142**. The non-volatile storage medium **152** may represent an internal disk drive or non-volatile memory, such as Flash memory. It should be noted that while the non-volatile storage medium **152** may represent one or more memory devices **10**, in some embodiments the non-volatile storage medium **152** may represent ordinary non-volatile memory without command based and current limit controlled power up circuitry.

**[0051]** While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and

have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

**1**. A method of powering one or more memory devices comprising:

receiving an external power supply;

powering a first portion of a memory device;

receiving a command; and

powering a second portion of the memory device.

**2**. The method of claim **1**, wherein powering the second portion of the memory device comprises supplying a current-limited internal power supply to the second portion of the memory.

**3**. The method of claim **2**, comprising regulating the external power supply in an internal vcc regulator with current control to limit the current-limited power supply to a peak current limit.

**4**. The method of claim **3**, wherein the peak current limit is between 4 milliamps (mA) and 20 mA.

**5**. The method of claim **2**, comprising receiving an additional command and supplying a non-current-limited internal power supply to the second portion of the memory.

**6**. The method of claim **5**, comprising resetting latches of the second portion of the memory before supplying the non-current-limited internal power supply to the second portion of the memory.

**7**. The method of claim **1**, wherein powering the second portion of the memory device comprises powering all remaining circuits of the memory device not of the first portion.

**8**. The method of claim **1**, comprising powering a first portion of another memory device while powering the first portion of the memory device and powering a second portion of the other memory device after powering the second portion of the memory device.

**9**. The method of claim **1**, wherein receiving the command comprises receiving the command from a serial peripheral interface bus (SPI).

**10**. A method of powering one or more memory devices comprising:

receiving an external power supply;

powering a first portion of a memory device;

receiving a command; and

powering a second portion of the memory device, wherein powering the second portion of the memory device, comprises supplying a current limit controlled power supply from power up circuitry on the memory device.

**11**. The method of claim **10**, comprising mirroring a reference current from a current source to supply the current limit controlled power supply from the power up circuitry to the second portion of the memory device.

**12**. The method of claim **10**, comprising regulating the external power supply in an internal vcc regulator with current control to limit the current limit controlled power supply to a peak current limit.

**13**. The method of claim **12**, wherein the peak current limit is between 4 milliamps (mA) and 20 mA.

**14**. The method of claim **10**, comprising receiving an additional command and supplying a non-current-limited controlled power supply to the second portion of the memory.

**15**. A method of powering one or more memory devices comprising:

receiving an external power supply at power up circuitry of a memory device;

supplying a current limit controlled power supply from the power up circuitry, utilizing the external power supply; and

powering the memory device with a current limit controlled power supply from the power up circuitry on the memory device.

**16**. The method of claim **15**, wherein the external power supply is a VCC power supply.

**17**. The method of claim **15**, wherein the current limit controlled power supply comprises a peak current limit between 4 milliamps (mA) and 20 mA.

**18**. The method of claim **15**, comprising mirroring a reference current from a current source to supply the current limit controlled power supply from the power up circuitry.

**19**. The method of claim **15**, comprising supplying a non-current-limited controlled power supply to the memory device after supplying the current limit controlled power supply for a predetermined amount of time.

**20**. The method of claim **19**, comprising resetting latches of at least a portion of the memory device before supplying the non-current-limited controlled power supply.

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