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(54) **THIN FILM TRANSISTOR, PIXEL STRUCTURE, DISPLAY DEVICE AND MANUFACTURING METHOD**

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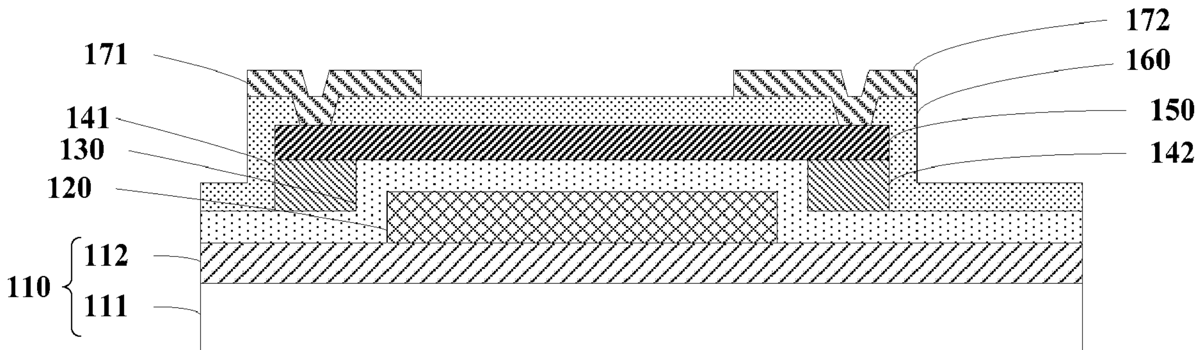
(57) **ABSTRACT**

The present disclosure provides a thin film transistor, a pixel structure, a display device, and a manufacturing method. The thin film transistor includes: a gate on the substrate; a gate insulating layer covering the gate and the substrate; a first support portion and a second support portion, which are provided on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion; a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate; and a source and a drain respectively connected to the semiconductor layer. The first support portion and the second support portion are respectively configured to support the semiconductor layer.



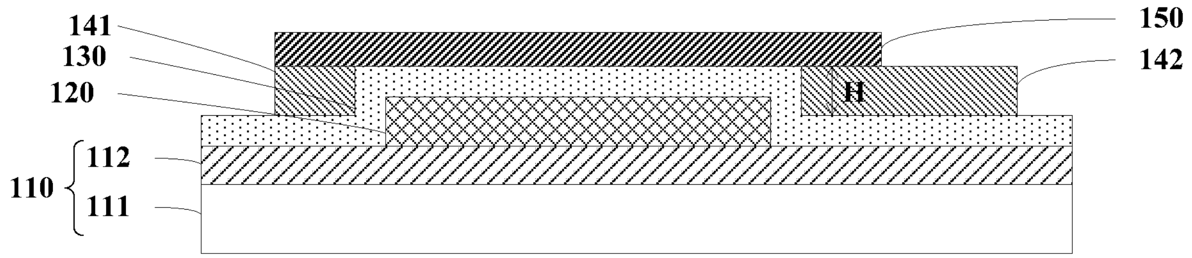


Fig. 1

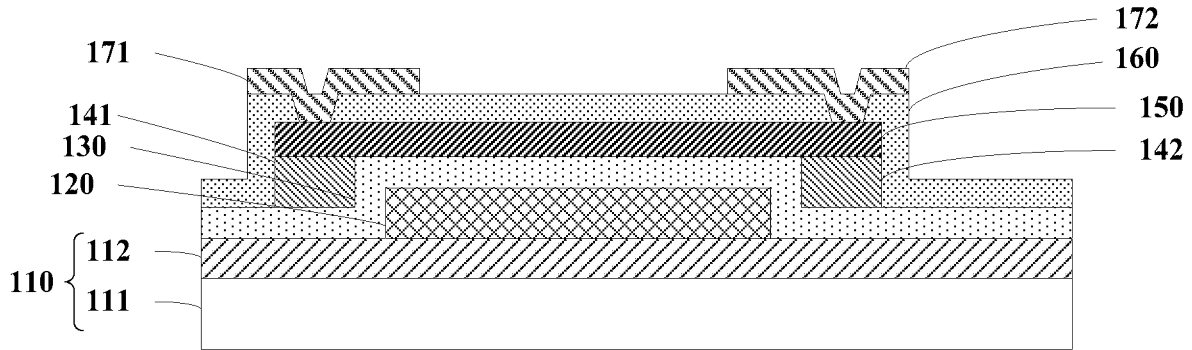


Fig. 2

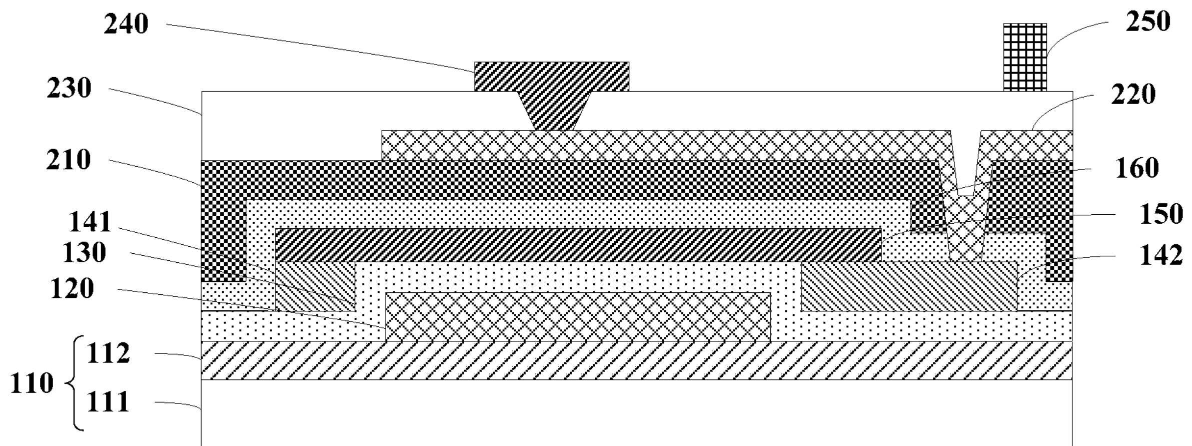


Fig. 3

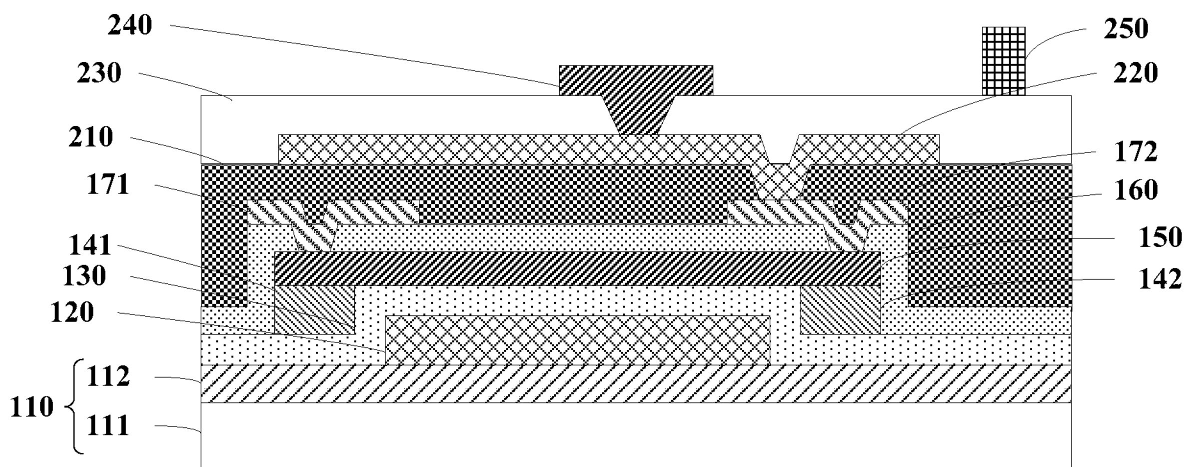


Fig. 4

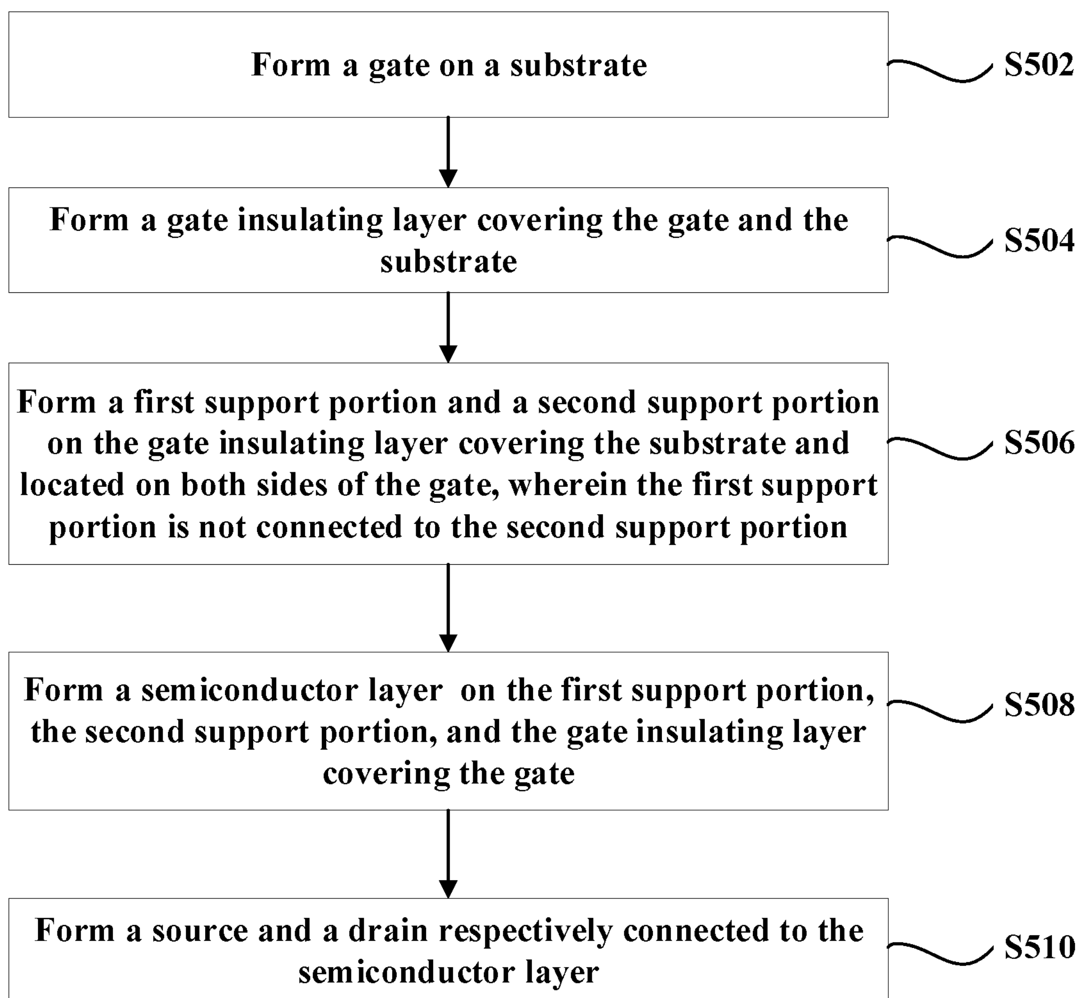


Fig. 5

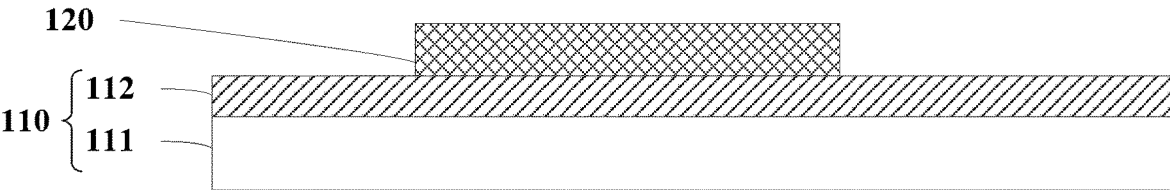


Fig. 6

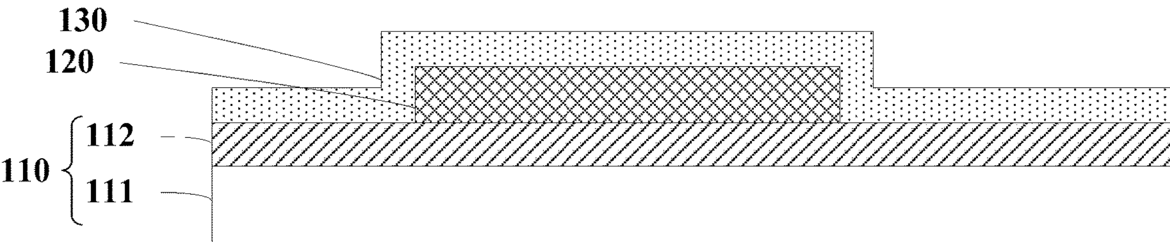


Fig. 7

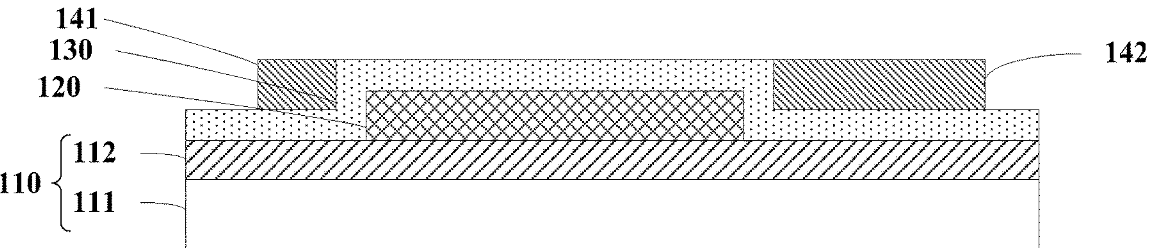


Fig. 8

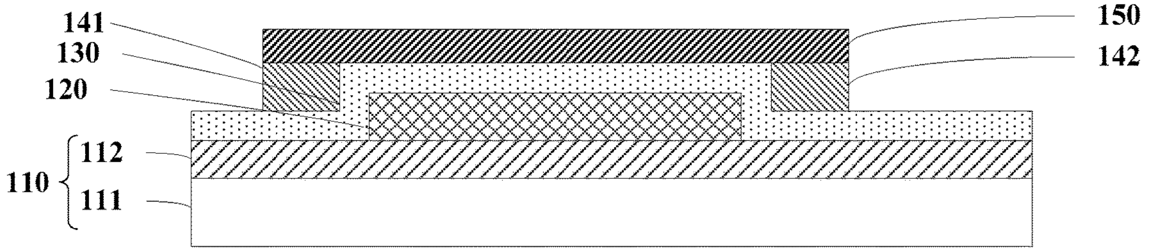


Fig. 9

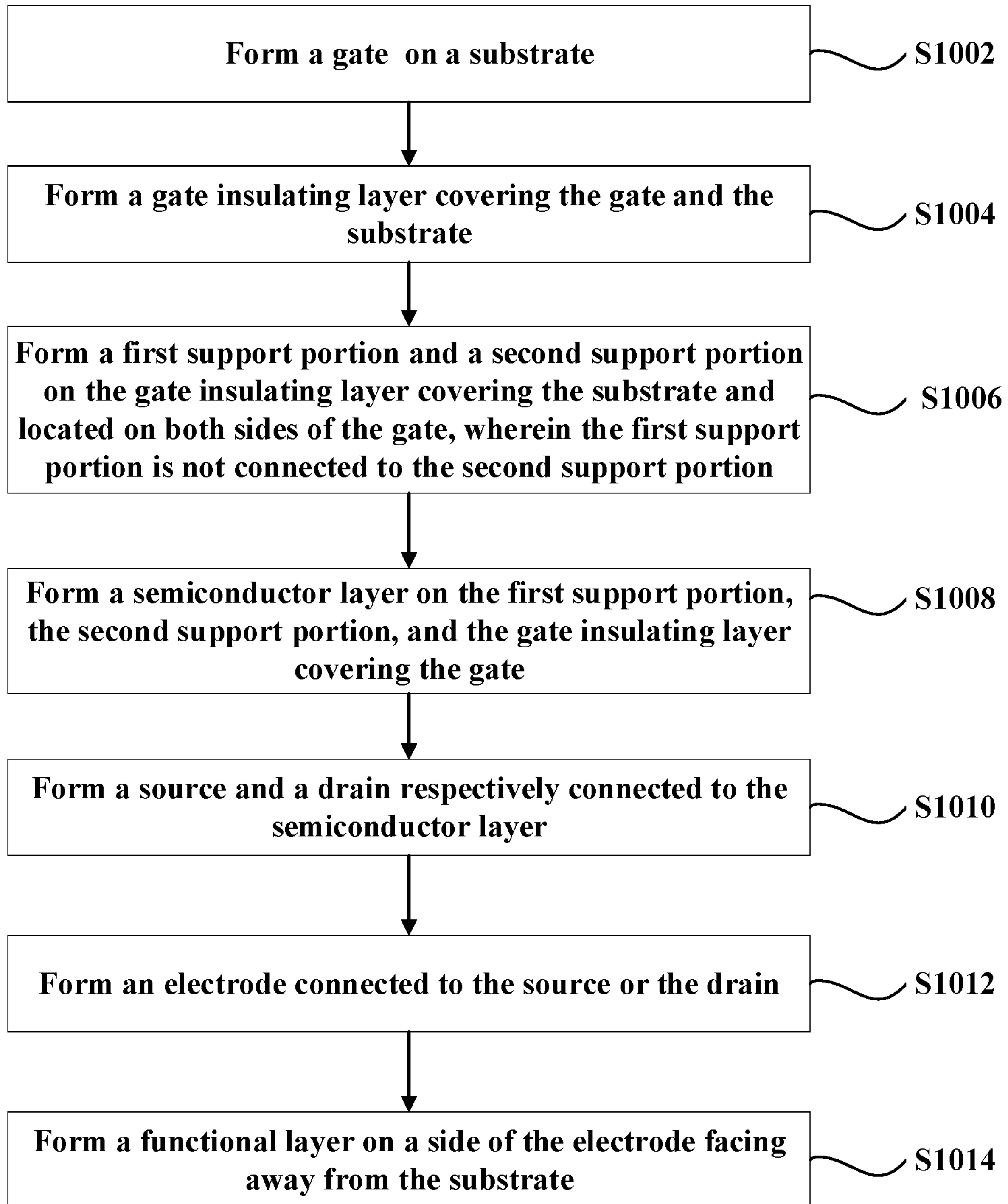


Fig. 10

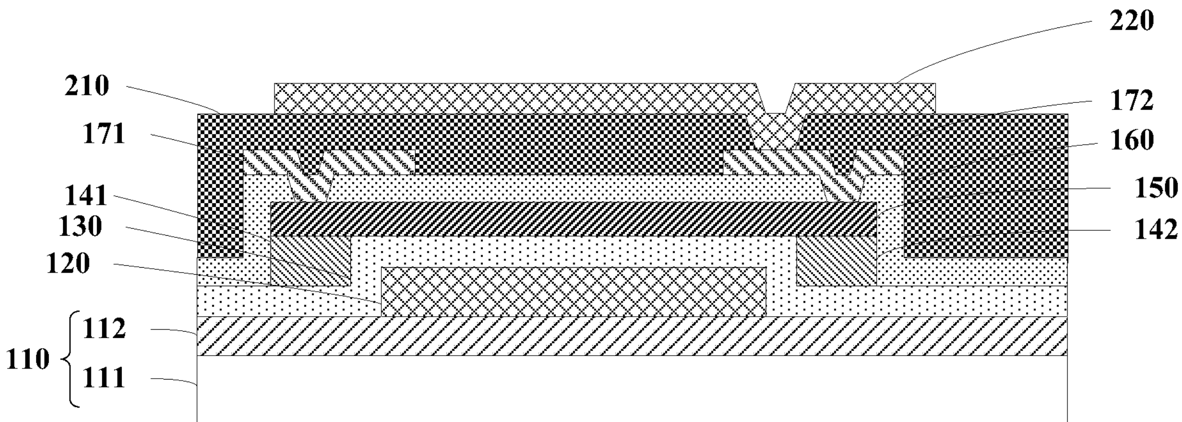


Fig. 11

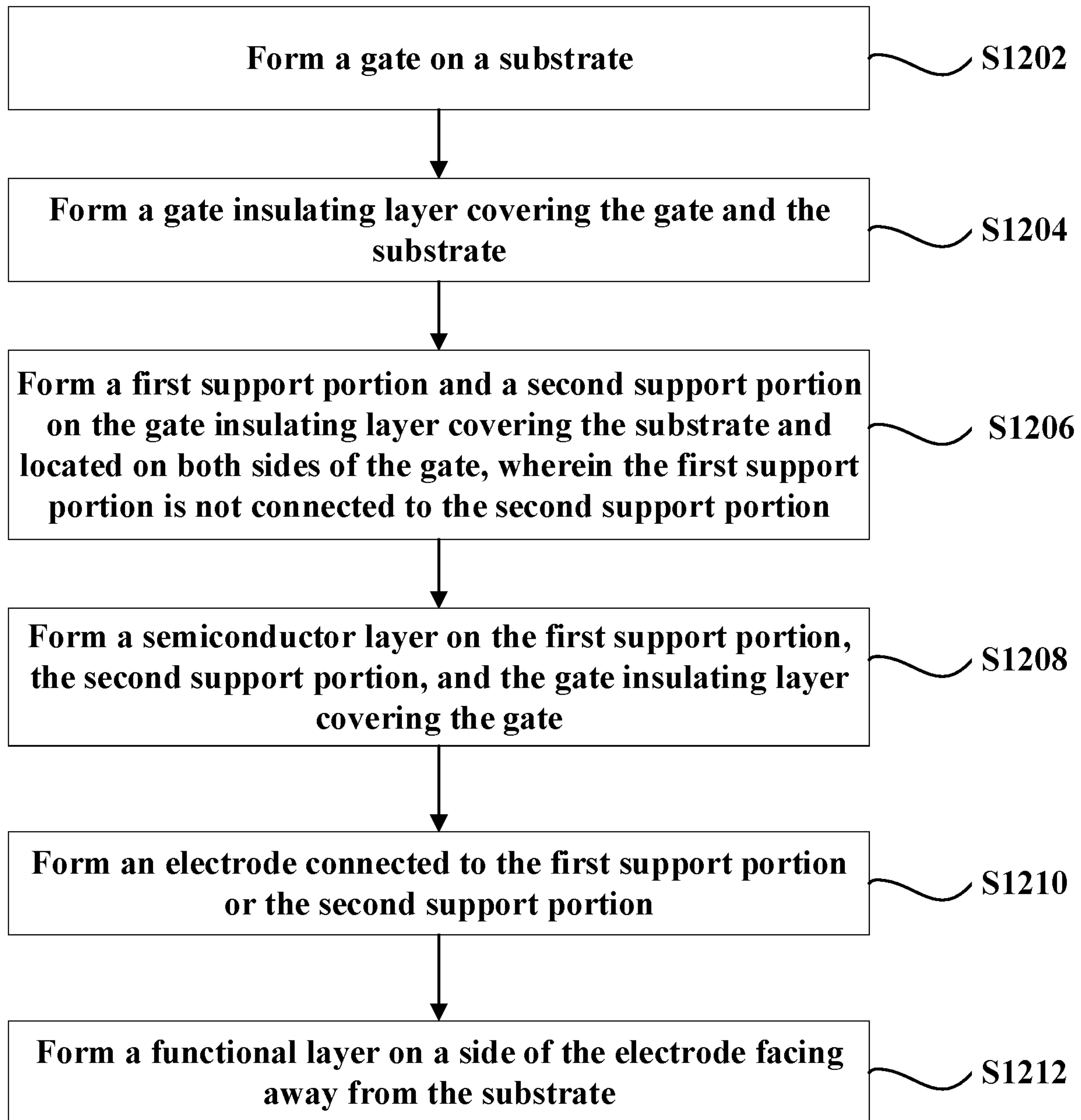


Fig. 12

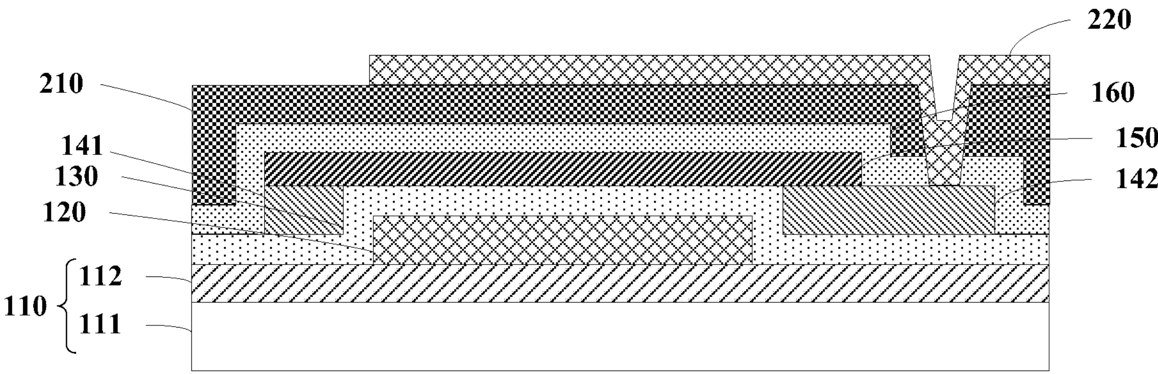


Fig. 13

THIN FILM TRANSISTOR, PIXEL STRUCTURE, DISPLAY DEVICE AND MANUFACTURING METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a U.S. National Stage Application under 35 U.S.C. § 371 of International Patent Application No. PCT/CN2019/075859, filed on Feb. 22, 2019, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to a thin film transistor, a pixel structure, a display device, and a manufacturing method.

BACKGROUND

[0003] In the field of display technology, it is often necessary to form a thin film transistor on a substrate. For example, the thin film transistor may be connected to a light emitting device as a driving transistor or the like for the light emitting device.

SUMMARY

[0004] According to an aspect of embodiments of the present disclosure, a thin film transistor is provided. The thin film transistor is provided on a substrate. The thin film transistor comprises: a gate on the substrate; a gate insulating layer covering the gate and the substrate; a first support portion and a second support portion, which are provided on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion; a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate; and a source and a drain each connected to the semiconductor layer; wherein the first support portion and the second support portion each are configured to support the semiconductor layer.

[0005] In some embodiments, surfaces on a side of the first support portion and the second support portion facing away from the substrate are flush with a surface on a side of a portion of the gate insulating layer on the gate facing away from the substrate; and the first support portion and the second support portion are provided at a step formed by the gate insulating layer on both sides of the gate, and extending directions of the first support portion and the second support portion are the same as that of the semiconductor layer.

[0006] In some embodiments, an orthographic projection of the semiconductor layer on the substrate is located inside an orthographic projection of the gate, the first support portion, and the second support portion on the substrate.

[0007] In some embodiments, the source is above the first support portion, and the drain is above the second support portion.

[0008] In some embodiments, materials of the first support portion and the second support portion comprise a conductive material, the first support portion serves as the source, and the second support portion serves as the drain.

[0009] In some embodiments, the conductive material comprises a metal material; and a solid solution of a metal and a semiconductor material is formed in areas where the first support portion and the second support portion are in contact with the semiconductor layer respectively.

[0010] In some embodiments, the metal material comprises aluminum; a material of the semiconductor layer comprises polysilicon; and the solid solution is a solid solution of silicon and aluminum.

[0011] In some embodiments, a material of the gate insulating layer comprises MgO.

[0012] According to another aspect of embodiments of the present disclosure, a pixel structure is provided. The pixel structure comprises the thin film transistor as described previously.

[0013] According to another aspect of embodiments of the present disclosure, an array substrate is provided. The array substrate comprises the thin film transistor as described previously.

[0014] According to another aspect of embodiments of the present disclosure, a display device is provided. The display device comprises: the array substrate as described previously.

[0015] According to another aspect of embodiments of the present disclosure, a manufacturing method for a thin film transistor is provided. The manufacturing method comprises: forming a gate on a substrate; forming a gate insulating layer covering the gate and the substrate; forming a first support portion and a second support portion on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion; forming a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate; and forming a source and a drain each connected to the semiconductor layer; wherein the first support portion and the second support portion each are configured to support the semiconductor layer.

[0016] In some embodiments, the manufacturing method further comprises: performing an annealing treatment on the semiconductor layer.

[0017] In some embodiments, after performing the annealing treatment, the manufacturing method further comprises: doping an area of the semiconductor layer on the first support portion and an area of the semiconductor layer on the second support portion; and forming the source and the drain respectively connected to the semiconductor layer in respective doped areas, wherein the source and the drain respectively form an ohmic contact with the respective doped areas.

[0018] In some embodiments, materials of the first support portion and the second support portion comprise a conductive material, the first support portion serves as the source, and the second support portion serves as the drain.

[0019] In some embodiments, the conductive material comprises a metal material; before performing the annealing treatment on the semiconductor layer, a material of the semiconductor layer comprises amorphous silicon; and the performing the annealing treatment on the semiconductor layer comprises: annealing the semiconductor layer by a laser annealing process to convert the amorphous silicon into polysilicon, wherein, by the laser annealing process, a solid solution of a metal and a semiconductor material is also formed in areas where the first support portion and the second support portion are in contact with the semiconductor layer respectively so as to form an ohmic contact.

[0020] In some embodiments, the metal material comprises aluminum; and the solid solution is a solid solution of silicon and aluminum.

[0021] Other features and advantages of the present disclosure will become apparent from the following detailed description of exemplary embodiments of the present disclosure with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The accompanying drawings, which constitute part of this specification, illustrate exemplary embodiments of the present disclosure and, together with this specification, serve to explain the principles of the present disclosure.

[0023] The present disclosure may be more clearly understood from the following detailed description with reference to the accompanying drawings, in which:

[0024] FIG. **1** is a schematic cross-sectional view showing a thin film transistor according to an embodiment of the present disclosure;

[0025] FIG. **2** is a schematic cross-sectional view showing a thin film transistor according to another embodiment of the present disclosure;

[0026] FIG. **3** is a schematic cross-sectional view showing a pixel structure according to an embodiment of the present disclosure;

[0027] FIG. **4** is a schematic cross-sectional view showing a pixel structure according to another embodiment of the present disclosure;

[0028] FIG. **5** is a flowchart showing a manufacturing method for a thin film transistor according to an embodiment of the present disclosure;

[0029] FIG. **6** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure;

[0030] FIG. **7** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure;

[0031] FIG. **8** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure;

[0032] FIG. **9** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a thin film transistor according to another embodiment of the present disclosure;

[0033] FIG. **10** is a flowchart showing a manufacturing method for a pixel structure according to an embodiment of the present disclosure;

[0034] FIG. **11** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a pixel structure according to an embodiment of the present disclosure;

[0035] FIG. **12** is a flowchart showing a manufacturing method for a pixel structure according to another embodiment of the present disclosure;

[0036] FIG. **13** is a schematic cross-sectional view showing a structure at a stage during a manufacturing process of a pixel structure according to another embodiment of the present disclosure.

[0037] It should be understood that the dimensions of the various parts shown in the accompanying drawings are not drawn according to the actual scale. In addition, the same or similar reference signs are used to denote the same or similar components.

DETAILED DESCRIPTION

[0038] Various exemplary embodiments of the present disclosure will now be described in detail with reference to the accompanying drawings. The description of the exemplary embodiments is merely illustrative and is in no way intended as a limitation to the present disclosure, its application or use. The present disclosure may be implemented in many different forms, which are not limited to the embodiments described herein. These embodiments are provided to make the present disclosure thorough and complete, and fully convey the scope of the present disclosure to those skilled in the art. It should be noticed that: relative arrangement of components and steps, material composition, numerical expressions, and numerical values set forth in these embodiments, unless specifically stated otherwise, should be explained as merely illustrative, and not as a limitation.

[0039] The use of the terms "first", "second" and similar words in the present disclosure do not denote any order, quantity or importance, but are merely used to distinguish between different parts. A word such as "comprise", "include" or variants thereof means that the element before the word covers the element(s) listed after the word without excluding the possibility of also covering other elements. The terms "up", "down", "left", "right", or the like are used only to represent a relative positional relationship, and the relative positional relationship may be changed correspondingly if the absolute position of the described object changes.

[0040] In the present disclosure, when it is described that a particular device is located between the first device and the second device, there may be an intermediate device between the particular device and the first device or the second device, and alternatively, there may be no intermediate device. When it is described that a particular device is connected to other devices, the particular device may be directly connected to said other devices without an intermediate device, and alternatively, may not be directly connected to said other devices but with an intermediate device.

[0041] All the terms (comprising technical and scientific terms) used in the present disclosure have the same meanings as understood by those skilled in the art of the present disclosure unless otherwise defined. It should also be understood that terms as defined in general dictionaries, unless explicitly defined herein, should be interpreted as having meanings that are consistent with their meanings in the context of the relevant art, and not to be interpreted in an idealized or extremely formalized sense.

[0042] Techniques, methods, and apparatus known to those of ordinary skill in the relevant art may not be discussed in detail, but where appropriate, these techniques, methods, and apparatuses should be considered as part of this specification.

[0043] The inventors of the present disclosure have found that, in the related art, during the process of forming a thin film transistor having a bottom gate structure, a patterned gate may cause a gate insulating layer to have a height difference. During the process of forming a semiconductor layer (e.g., an amorphous silicon layer) on the gate insulating layer, a portion of the semiconductor layer is at a

position of the height difference. This height difference does not facilitate crystallization of the semiconductor layer, thereby affecting the performance of the formed thin film transistor.

[0044] In view of this, the embodiments of the present disclosure provide a thin film transistor to improve the crystallization effect of a semiconductor layer. Hereinafter, a thin film transistor according to some embodiments of the present disclosure will be described in detail in conjunction with the accompanying drawings.

[0045] FIG. **1** is a schematic cross-sectional view showing a thin film transistor according to an embodiment of the present disclosure.

[0046] For example, as shown in FIG. **1**, the thin film transistor is provided on a substrate **110**. In some embodiments, the substrate **110** may comprise an initial substrate **111** and a buffer layer **112** on the initial substrate **111**. For example, the initial substrate **111** may comprise a glass substrate or the like. For example, the buffer layer **112** may comprise at least one of a silicon nitride layer or a silicon dioxide layer. For example, the thickness of the silicon nitride layer may range from 30 nm to 80 nm, and the thickness of the silicon dioxide layer may range from 300 nm to 800 nm. In other embodiments, the substrate **110** may comprise the initial substrate **111** without the buffer layer **112**.

[0047] As shown in FIG. **1**, the thin film transistor comprises a gate **120** on the substrate **110**. For example, a material of the gate **120** may comprise a metal material such as molybdenum (Mo). A thickness of the gate **120** may range from 2500 Å to 3500 Å.

[0048] As shown in FIG. **1**, the thin film transistor further comprises a gate insulating layer **130** covering the gate **120** and the substrate **110**. A portion of the gate insulating layer **130** on the substrate **110** is integral with a portion of the gate insulating layer **130** on the gate **120**. For example, a thickness of the gate insulating layer may range from 100 nm to 500 nm. As shown in FIG. **1**, the gate **120** causes the gate insulating layer **130** to have a height difference H.

[0049] As shown in FIG. **1**, the thin film transistor further comprises a first support portion **141** and a second support portion **142**, which are provided on the gate insulating layer **130** covering the substrate **110** and located on both sides of the gate **120**, wherein the first support portion **141** is not connected to the second support portion **142**. The first support portion **141** and the second support portion **142** are on the portion of the gate insulating layer **130** on the substrate **110**. The first support portion **141** and the second support portion **142** are respectively on both sides of the gate **120**. For example, the first support portion **141** and the gate **120** are separated by the gate insulating layer **130**, and the second support portion **142** and the gate **120** are separated by the gate insulating layer **130**. The first support portion **141** and the second support portion **142** may reduce the height difference H.

[0050] As shown in FIG. **1**, the thin film transistor further comprises a semiconductor layer **150** on the first support portion **141**, the second support portion **142**, and the gate insulating layer **130** covering the gate **120**. The semiconductor layer **150** is on a side of the first support portion **141**, the second support portion **142** and the gate insulating layer **130** facing away from the substrate **110**. For example, a material of the semiconductor layer **150** may comprise amorphous silicon, polysilicon, or the like. For example, the semiconductor layer **150** may be a low-temperature polysilicon material. The first support portion **141** and the second support portion **142** described above each are configured to support the semiconductor layer **150**.

[0051] The thin film transistor further comprises a source and a drain each connected to the semiconductor layer **150**. In some embodiments, materials of the first support portion **141** and the second support portion **142** may comprise a conductive material. For example, the conductive material comprises a metal material (e.g., aluminum (Al) or the like). For example, the first support portion **141** may serve as the source, and the second support portion **142** may serve as the drain. In this embodiment, the first support portion and the second support portion may serve as the source and the drain respectively, so that it is unnecessary to additionally form the source and the drain, and the device structure may be simplified.

[0052] So far, the above-described embodiments provide a thin film transistor. The thin film transistor comprises a gate on a substrate. The thin film transistor further comprises a gate insulating layer covering the gate and the substrate. The thin film transistor further comprises a first support portion and a second support portion, which are provided on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion. The thin film transistor further comprises a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate. The first support portion and the second support portion are respectively configured to support the semiconductor layer. The thin film transistor comprises a source and a drain respectively connected to the semiconductor layer. This embodiment may reduce the height difference of the gate insulating layer caused by the gate. In this way, during the manufacturing process, it is possible to improve the crystallization effect of the semiconductor layer on the first support portion, the second support portion and the gate insulating layer, thereby improving the performance of the thin film transistor.

[0053] In some embodiments, in a case where the materials of the first support portion **141** and the second support portion **142** comprise a metal material, a solid solution of a metal and a semiconductor material is formed in areas where the first support portion **141** and the second support portion **142** are in contact with the semiconductor layer **150** respectively. For example, the metal material comprises aluminum (i.e., the materials of the first support portion **141** and the second support portion **142** are aluminum), the material of the semiconductor layer comprises polysilicon, and the solid solution of the metal and the semiconductor material is a solid solution of silicon and aluminum. The solid solution of the metal and the semiconductor material may make the first support portion and the second support portion respectively form an ohmic contact with the semiconductor layer, which may reduce the contact resistance, thereby improving the response speed and performance of the device, and reducing the power consumption.

[0054] In some embodiments, as shown in FIG. **1**, surfaces on a side of the first support portion **141** and the second support portion **142** facing away from the substrate **110** (i.e. upper surfaces of the first support portion **141** and the second support portion **142** in FIG. **1**) are flush with a surface on a side of a portion of the gate insulating layer **130** on the gate **120** facing away from the substrate. In FIG. **1**, the above-

described surface of the portion of the gate insulating layer is a upper surface of the portion of the gate insulating layer **130** on the gate **120**. The upper surfaces of the two support portions are flush with the upper surface of the above-described portion of the gate insulating layer, thereby facilitating improving the crystallization effect of the semiconductor layer during the manufacturing process.

[0055] It should be noted that, the term "flush" here comprises, but is not limited to, absolute flush. For example, the upper surfaces of the two support portions may be higher or lower than the upper surface of the above-described portion of the gate insulating layer, as long as a height difference between these upper surfaces is within an allowable range. The allowed range may be determined according to actual conditions or actual needs.

[0056] It should also be noted that, in some cases, although the upper surfaces of the two support portions may be not flush with the upper surface of the above-described portion of the gate insulating layer, these two support portions may also reduce the height difference H of the gate insulating layer to a certain extent, and thus it is also possible to improve the crystallization effect of the semiconductor layer.

[0057] In some embodiments, the first support portion **141** and the second support portion **142** are provided at a step formed by the gate insulating layer **130** on both sides of the gate **120**. In other words, the first support portion **141** and the second support portion **142** are provided at a step formed by a portion of the gate insulating layer **130** on the substrate **110** and a portion of the gate insulating layer **130** on the gate **120**. Extending directions of the first support portion **141** and the second support portion **142** are the same as that of the semiconductor layer **150**. For example, the semiconductor layer **150** extends along a direction parallel to the substrate, and the first support portion **141** and the second support portion **142** also extend along the direction.

[0058] In some embodiments, a thickness of the first support portion **141** and a thickness of the second support portion **142** are 100 nm to 300 nm respectively. Of course, those skilled in the art should understand that, the thickness of the first support portion and the thickness of the second support portion described here are merely exemplary, and the scope of the embodiments of the present disclosure is not limited thereto.

[0059] In some embodiments, as shown in FIG. **1**, an orthographic projection (not shown) of the semiconductor layer **150** on the substrate **110** is located inside an orthographic projection (not shown) of the gate **120**, the first support portion **141**, and the second support portion **142** on the substrate **110**. In other words, the orthographic projection of the gate **120**, the first support portion **141**, and the second support portion **142** on the substrate **110** covers the orthographic projection of the semiconductor layer **150** on the substrate **110**.

[0060] In some embodiments, as shown in FIG. **1**, a portion of the second support portion **142** is not covered by the semiconductor layer **150**. The portion of the second support portion **142** that is not covered may be used to connect to another structure (e.g., an electrode of a light emitting device). In other embodiments, a portion of the first support portion **141** may not be covered by the semiconductor layer **150** (not shown).

[0061] In some embodiments, a material of the gate insulating layer **130** may comprise an insulating material having a dielectric constant greater than 3.9. In this embodiment, the gate insulating layer uses a material with a relatively large dielectric constant, which may increase the gate's ability to control the channel, and may change the gray scale under a small voltage change, thereby improving the response speed of the thin film transistor.

[0062] For example, the material of the gate insulating layer **130** may comprise MgO or the like. By using for example MgO or the like as the gate insulating layer, in addition to increasing the gate's ability to control the channel to improve the response speed of the thin film transistor, it may also make the gate insulating layer have a better heat insulation performance. In this way, in the process of laser annealing during the manufacturing process, heat radiation may be performed relatively slowly, thereby improving the crystallization effect of the semiconductor layer.

[0063] In other embodiments, the material of the gate insulating layer **130** may comprise silicon dioxide or the like.

[0064] FIG. **2** is a schematic cross-sectional view showing a thin film transistor according to another embodiment of the present disclosure. The thin film transistor is provided on the substrate **110**.

[0065] Similar to the thin film transistor shown in FIG. **1**, the thin film transistor shown in FIG. **2** comprises: the gate **120**, the gate insulating layer **130**, the first support portion **141**, the second support portion **142**, and the semiconductor layer **150**. As shown in FIG. **2**, the thin film transistor may further comprise a source **171** and a drain **172** respectively connected to the semiconductor layer **150**. The source **171** and the drain **172** are respectively on the semiconductor layer **150**. The source **171** is above the first support portion **141**, and the drain **172** is above the second support portion **142**.

[0066] In some embodiments, as shown in FIG. **2**, the thin film transistor may further comprise an interlevel dielectric layer (ILD) **160**. The interlayer dielectric layer **160** covers the gate insulating layer **130**, the first support portion **141**, the second support portion **142** and the semiconductor layer **150**. The source **171** and the drain **172** respectively pass through the interlayer dielectric layer **160** so as to be connected to the semiconductor layer **150**.

[0067] In the above-described embodiments, a thin film transistor according to other embodiments of the present disclosure is provided. In the thin film transistor, the source and the drain which are respectively connected to the semiconductor layer are provided. This eliminates the need to use the first support portion and the second support portion as the source and the drain respectively.

[0068] In the embodiment, since the first support portion and the second support portion may not serve as the source and the drain, the materials of the first support portion and the second support portion may not be limited to a conductive material. For example, the materials of the first support portion and the second support portion may comprise an insulating material such as silicon nitride, silicon dioxide, or the like.

[0069] In some embodiments, the above-described thin film transistor may be a PMOS (P-channel Metal Oxide Semiconductor) transistor or an NMOS (N-channel Metal Oxide Semiconductor) transistor.

[0070] In some embodiments of the present disclosure, a pixel structure is also provided. The pixel structure may comprise the thin film transistor as described above.

[0071] FIG. **3** is a schematic cross-sectional view showing a pixel structure according to an embodiment of the present disclosure.

[0072] As shown in FIG. **3**, the pixel structure may comprise the thin film transistor as shown in FIG. **1**. For example, the pixel structure may comprise the gate **120**, the gate insulating layer **130**, the first support portion **141**, the second support portion **142**, and the semiconductor layer **150**.

[0073] In some embodiments, the pixel structure may further comprise an electrode (e.g., an anode) **220** connected to the first support portion **141** or the second support portion **142**. For example, as shown in FIG. **3**, the electrode **220** is connected to the second support portion **142**.

[0074] In some embodiments, as shown in FIG. **3**, the pixel structure may further comprise a functional layer **240** on a side of the electrode **220** facing away from the thin film transistor. For example, the functional layer **240** is on a surface of the electrode **220**. For example, the functional layer **240** may comprise an electron transport layer, a hole transport layer, a light emitting layer, and the like. For another example, the functional layer **240** may further comprise an electron blocking layer and a hole blocking layer or the like.

[0075] So far, a pixel structure according to some embodiments of the present disclosure is provided. The pixel structure further comprises an electrode and a functional layer in addition to a thin film transistor. The electrode is connected to the first support portion or the second support portion.

[0076] In some embodiments, as shown in FIG. **3**, the pixel structure may further comprise an interlayer dielectric layer **160**. The interlayer dielectric layer **160** covers the gate insulating layer **130**, the first support portion **141**, the second support portion **142** and the semiconductor layer **150**. The pixel structure may further comprise a planarization layer (PLN) **210** on the interlayer dielectric layer **160**.

[0077] As shown in FIG. **3**, the electrode **220** passes through the planarization layer **210** and the interlayer dielectric layer **160** and is connected to the second support portion **142**. For example, a portion of the first support portion **141** or a portion of the second support portion **142** is not covered by the semiconductor layer **150**. The electrode **220** is connected to the portion of the first support portion **141** that is not covered or the portion of the second support portion **142** that is not covered. FIG. **3** shows that the electrode **220** is connected to the portion of the second support portion **142** that is not covered.

[0078] In some embodiments, as shown in FIG. **3**, the pixel structure may further comprise a pixel definition layer (PDL) **230** on the planarization layer **210** and the electrode **220**. The functional layer **240** passes through the pixel definition layer **230** and is in contact with the electrode **220**.

[0079] In some embodiments, as shown in FIG. **3**, the pixel structure may further comprise a photo spacer (PS) **250** on the pixel definition layer **230**.

[0080] FIG. **4** is a schematic cross-sectional view showing a pixel structure according to another embodiment of the present disclosure.

[0081] As shown in FIG. **4**, the pixel structure may comprise the thin film transistor as shown in FIG. **2**. For example, the pixel structure comprises the gate **120**, the gate insulating layer **130**, the first support portion **141**, the second support portion **142**, the semiconductor layer **150**, the interlayer dielectric layer **160**, the source **171**, and the drain **172**.

[0082] In some embodiments, the pixel structure may further comprise an electrode (e.g., an anode) **220** connected to the source **171** or the drain **172**. For example, as shown in FIG. **4**, the electrode **220** is connected to the drain **172**.

[0083] In some embodiments, as shown in FIG. **4**, the pixel structure may further comprise a functional layer **240** on a side of the electrode **220** facing away from the thin film transistor.

[0084] So far, a pixel structure according to other embodiments according to the present disclosure is provided. The pixel structure further comprises the electrode and the functional layer in addition to the thin film transistor. The electrode is connected to the source or the drain.

[0085] In some embodiments, as shown in FIG. **4**, the pixel structure may further comprise a planarization layer **210** covering the interlayer dielectric layer **160**, the source **171**, and the drain **172**. The electrode **220** passes through the planarization layer **210** and is connected to the drain **172**. In addition, similar to the pixel structure shown in FIG. **3**, the pixel structure shown in FIG. **4** may also comprise the pixel definition layer **230** and the photo spacer **250**.

[0086] In some embodiments, in the case where the materials of the first support portion **141** and the second support portion **142** are a conductive material, the first support portion **141** or the second support portion **142** respectively forms a capacitor with the gate. In this way, in the above-described pixel structure, a capacitor is also provided, so that it is unnecessary to additionally form a capacitor.

[0087] In the case where the gate insulating layer **130** uses an insulating material (e.g., MgO) having a relatively large dielectric constant (e.g., a dielectric constant greater than 3.9), an occupied area of the capacitor may be reduced. This may reduce the total area of the pixel structure, thereby raising the PPI (Pixels Per Inch) of the display panel.

[0088] In some embodiments of the present disclosure, an array substrate is also provided. The array substrate may comprise the thin film transistor as described above (e.g., the thin film transistor shown in FIG. **1** or **2**). For example, the array substrate may further comprise a substrate.

[0089] In some embodiments of the present disclosure, a display device is also provided. The display device comprises the array substrate as described above. For example, the display device may be a display panel, a display, a mobile phone, or a tablet computer and the like.

[0090] FIG. **5** is a flowchart showing a manufacturing method for a thin film transistor according to an embodiment of the present disclosure. FIGS. **6**, **7**, **8**, and FIG. **1** are schematic cross-sectional views showing structures of several stages during a manufacturing process of a thin film transistor according to some embodiments of the present disclosure. Hereinafter, a manufacturing process of a thin film transistor according to some embodiments of the present disclosure will be described in detail in conjunction with FIGS. **5**, **6**, **7**, **8**, and FIG. **1**. As shown in FIG. **5**, the manufacturing method may comprise steps **S502** to **S510**.

[0091] As shown in FIG. **5**, at step **S502**, a gate is formed on a substrate.

[0092] FIG. **6** is a schematic cross-sectional view showing a structure at step **S502** during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure. As shown in FIG. **6**, a buffer layer **112** is formed on an initial substrate (e.g., a high-temperature glass

substrate) **111** by a chemical vapor deposition process. For example, the buffer layer **112** may comprise at least one of a silicon nitride layer or a silicon dioxide layer. For example, a thickness of the silicon nitride layer may range from 30 nm to 80 nm, and a thickness of the silicon dioxide layer may range from 300 nm to 800 nm. Through the above-described process flow, a substrate **110** is formed. The substrate **110** may comprise the initial substrate **111** and the buffer layer **112**. Then, for example, a gate material layer (e.g., molybdenum) is formed on the substrate **110** by using a magnetron sputtering technique, and the gate material layer is patterned to form a gate **120**. For example, a thickness of the gate **120** may range from 2500 Å to 3500 Å.

[0093] Returning to FIG. **5**, at step S**504**, a gate insulating layer covering the gate and the substrate is formed.

[0094] FIG. **7** is a schematic cross-sectional view showing a structure at step **S504** during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure. As shown in FIG. **7**, for example, a gate insulating layer **130** covering the gate electrode **120** and the substrate **110** is formed by using an electron beam evaporation technique. A portion of the gate insulating layer **130** on the substrate **110** and a portion of the gate insulating layer **130** on the gate **120** are integrally formed. For example, a material of the gate insulating layer may comprise MgO or the like. For example, a thickness of the gate insulating layer may range from 100 nm to 500 nm.

[0095] Returning to FIG. **5**, at step S**506**, a first support portion and a second support portion are formed on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion.

[0096] FIG. **8** is a schematic cross-sectional view showing a structure at step **S506** during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure. As shown in FIG. **8**, a first support portion **141** and a second support portion **142** are formed on the gate insulating layer **130** covering the substrate **110** and located on both sides of the gate **120**, wherein the first support portion **141** is not connected to the second support portion **142**.

[0097] For example, a mask may be formed on the gate insulating layer **130**, wherein the mask exposes a portion of the gate insulating layer **130** (i.e., a portion on which the first support portion and the second support portion need to be formed). The first support portion **141** and the second support portion **142** are then formed on the exposed portion of the gate insulating layer **130** by a deposition process. The mask is then removed, thereby forming the structure shown in FIG. **8**.

[0098] For another example, a support portion material layer (e.g., Al) is formed on a side of the gate insulating layer **130** facing away from the substrate **110** by using a deposition process, and then the support portion material layer is patterned to form the first support portion **141** and the second support portion **142**.

[0099] Here, the first support portion and the second support portion that are patterned are in contact with the semiconductor layer respectively to define contact areas. A channel area is between the contact areas. That is, an actual channel area is defined.

[0100] As shown in FIG. **8**, the first support portion **141** and the second support portion **142** are respectively on both sides of the gate **120**. For example, the thickness of the first support portion **141** and the thickness of the second support portion **142** may range from 100 nm to 300 nm, respectively. For example, as shown in FIG. **8**, the first support portion **141** and the gate **120** are separated by the gate insulating layer **130**, and the second support portion **142** and the gate **120** are separated by the gate insulating layer **130**.

[0101] In some embodiments, materials of the first support portion **141** and the second support portion **142** comprise a conductive material. That is, a material of the support portion material layer may comprise a conductive material. For example, the conductive material comprises a metal material (e.g., aluminum). The first support portion **141** may serve as a source, and the second support portion **142** may serve as a drain.

[0102] Returning to FIG. **5**, at step S**508**, a semiconductor layer is formed on the first support portion, the second support portion, and the gate insulating layer covering the gate. The first support portion and the second support portion each are configured to support the semiconductor layer.

[0103] FIG. **1** is a schematic cross-sectional view showing a structure at step **S508** during a manufacturing process of a thin film transistor according to an embodiment of the present disclosure. For example, as shown in FIG. **1**, a semiconductor layer **150** (e.g., an amorphous silicon layer) **150** is formed on the first support portion **141**, the second support portion **142**, and the gate insulating layer **130** covering the gate **120** for example by a deposition process, and the semiconductor layer **150** is patterned.

[0104] In some embodiments, the manufacturing method may further comprise: performing an annealing treatment on the semiconductor layer **150**. For example, before the semiconductor layer is annealed, a material of the semiconductor layer may comprise amorphous silicon. For example, the semiconductor layer **150** is annealed by a laser annealing process (e.g., a laser-based microlens array local crystallization technology) to convert the amorphous silicon into polysilicon. Therefore, the annealing process may crystallize the semiconductor layer. In the embodiment, the first support portion and the second support portion described above are advantageous for the semiconductor layer to be in the same focal plane of laser, thereby improving the crystallization effect of the semiconductor layer and improving the performance of the thin film transistor.

[0105] In some embodiments, by the laser annealing process, a solid solution of a metal and a semiconductor material is also formed in areas where the first support portion **141** and the second support portion **142** are in contact with the semiconductor layer **150** respectively so as to form an ohmic contact. For example, the metal materials of the first support portion **141** and the second support portion **142** comprise aluminum, and the solid solution is a solid solution of silicon and aluminum.

[0106] Here, contacts area are laser annealed to form a solid solution of a metal and a semiconductor material (e.g., a solid solution of silicon and aluminum), so that an ohmic contact is formed in a self-aligned manner here. The process of forming the ohmic contact may solve the problems such as photoresist carbonization pollution resulting from forming an ohmic contact by heavy doping in the related art.

[0107] Returning to FIG. **5**, at step S**510**, a source and a drain each connected to the semiconductor layer are formed.

[0108] In some embodiments, the materials of the first support portion **141** and the second support portion **142**

comprise a conductive material. The first support portion **141** may serve as the source, and the second support portion **142** may serve as the drain. In this case, in the case where the first support portion and the second support portion are formed, the source and the drain are formed.

[0109] So far, a manufacturing method for a thin film transistor according to some embodiments of the present disclosure is provided. In the manufacturing method, a gate is formed on a substrate. A gate insulating layer covering the gate and the substrate is formed. A first support portion and a second support portion are formed on a gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion. A semiconductor layer is formed on the first support portion, the second support portion, and the gate insulating layer covering the gate. A source and a drain which are respectively connected to the semiconductor layer are formed. The first support portion and the second support portion are respectively configured to support the semiconductor layer. By forming the first support portion and the second support portion, the height difference of the gate insulating layer caused by the gate is reduced.

[0110] In addition, the use of, for example, MgO or the like as the gate insulating layer can make the gate insulating layer have a better heat insulation performance, so that during the laser annealing process, heat radiation may be performed relatively slowly, thereby improving the crystallization effect of the semiconductor layer.

[0111] In some embodiments, the first support portion and the second support portion may not serve as the source and the drain. In the case, after the annealing process, the manufacturing method may further comprise: forming a source and a drain respectively connected to the semiconductor layer.

[0112] Hereinafter, a manufacturing method for a thin film transistor according to other embodiments of the present disclosure will be described in detail in conjunction with FIG. **9** and FIG. **2**.

[0113] For example, a structure shown in FIG. **9** may be formed by the steps of the method shown in FIG. **5**. For example, the material of the semiconductor layer **150** is amorphous silicon. In the embodiment, the materials of the first support portion **141** and the second support portion **142** may comprise a conductive material or an insulating material. The semiconductor layer **150** is then annealed, for example, to convert amorphous silicon into polysilicon.

[0114] Next, as shown in FIG. **2**, a source **171** and a drain **172** connected to the semiconductor layer **150** are formed respectively. The process of forming the source and the drain will be described in detail below.

[0115] In some embodiments, after the annealing process, the manufacturing method may further comprise: doping an area of the semiconductor layer on the first support portion and an area of the semiconductor layer on the second support portion. For example, an interlayer dielectric layer **160** covering the structure shown in FIG. **9** may be formed. A material of the interlayer dielectric layer **160** may comprise at least one of silicon dioxide or silicon nitride. For example, a thickness of the interlayer dielectric layer ranges from 3000 Å to 5000 Å. The interlayer dielectric layer **160** is then etched to form two through holes exposing the semiconductor layer **150**. The two through holes respectively expose the area of the semiconductor layer on the first support portion and the area of the semiconductor layer on the second support portion. The semiconductor layer **150** is doped through the two through holes.

[0116] In some embodiments, the manufacturing method may further comprise: forming a source and a drain respectively connected to the semiconductor layer in doped areas. The source and the drain form an ohmic contact with the doped areas respectively. For example, a source **171** passing through one of the two through holes and a drain **172** passing through the other through hole of the two through holes are formed by processes such as deposition and patterning. This may form the thin film transistor as shown in FIG. **2**.

[0117] FIG. **10** is a flowchart showing a manufacturing method for a pixel structure according to an embodiment of the present disclosure. As shown in FIG. **10**, the manufacturing method comprises steps S**1002** to S**1014**.

[0118] At step S**1002**, a gate is formed on a substrate. For example, a gate **120** is formed on a substrate **110** by using processes such as deposition and patterning, so as to form a structure as shown in FIG. **6**.

[0119] At step S**1004**, a gate insulating layer covering the gate and the substrate is formed. For example, a gate insulating layer **130** covering the gate **120** and the substrate **110** is formed. A portion of the gate insulating layer **130** on the substrate **110** and a portion of the gate insulating layer **130** on the gate **120** are integrally formed. In this way, a structure shown in FIG. **7** is formed.

[0120] At step S**1006**, a first support portion and a second support portion are formed on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion. For example, as shown in FIG. **9**, a first support portion **141** and a second support portion **142** are formed on the gate insulating layer **130** covering the substrate **110** and located on both sides of the gate **120** by using processes such as deposition and patterning, wherein the first support portion **141** is not connected to the second support portion **142**.

[0121] At step S**1008**, a semiconductor layer is formed on the first support portion, the second support portion, and the gate insulating layer covering the gate. For example, as shown in FIG. **9**, a semiconductor layer **150** is formed on the first support portion **141**, the second support portion **142**, and the gate insulating layer **130** covering the gate electrode **120** by a deposition and patterning process. The first support portion **141** and the second support portion **142** each are configured to support the semiconductor layer **150**.

[0122] In some embodiments, an annealing process is performed on the semiconductor layer **150**.

[0123] At step S**1010**, a source and a drain each connected to the semiconductor layer are formed. For example, a source **171** and a drain **172** respectively connected to the semiconductor layer **150** may be formed by processes such as deposition and patterning, so as to form the structure shown in FIG. **2**. For example, it is possible to first form the interlayer dielectric layer **160** covering the structure shown in FIG. **9**, and then form the source **171** and the drain **172** passing through the interlayer dielectric layer **160** and connected to the semiconductor layer **150** respectively.

[0124] At step S**1012**, an electrode connected to the source or the drain is formed. For example, the electrode is an anode. For example, as shown in FIG. **11**, a planarization layer **210** may be formed on the structure shown in FIG. **2**, so that a planarization process is performed. The planarization layer **210** is then etched to form an opening exposing the

drain **172** (or the source **171**). An electrode **220** passing through the opening and connected to the drain **172** (or the source **171**) is formed by a process such as deposition.

[0125] At step S**1014**, a functional layer is formed on a side of the electrode facing away from the substrate. For example, a pixel definition layer **230** may be formed on the structure shown in FIG. **11** by using processes such as deposition and patterning, and a functional layer **240** passing through the pixel definition layer and in contact with the electrode **220** is then formed, so as to form the structure shown in FIG. **4**.

[0126] In some embodiments, as shown in FIG. **4**, a photo spacer **250** may be further formed on the pixel definition layer **230**.

[0127] So far, a manufacturing method for a pixel structure according to some embodiments of the present disclosure is provided. In the manufacturing method, since the first support portion and the second support portion are formed, the height difference of the gate insulating layer caused by the gate is reduced, which is advantageous for the semiconductor layer to be in the same focal plane of laser, so that it is possible to improve the crystallization quality of the semiconductor layer.

[0128] FIG. **12** is a flowchart showing a manufacturing method for a pixel structure according to another embodiment of the present disclosure. As shown in FIG. **12**, the manufacturing method may comprise steps S**1202** to S**1212**.

[0129] At step S**1202**, a gate is formed on a substrate. For example, a gate **120** may be formed on a substrate **110** by using processes such as deposition and patterning, so as to form the structure as shown in FIG. **6**.

[0130] In step S**1204**, a gate insulating layer covering the gate and the substrate is formed. For example, a gate insulating layer **130** covering the gate **120** and the substrate **110** is formed. A portion of the gate insulating layer **130** on the substrate **110** and a portion of the gate insulating layer **130** on the gate **120** are integrally formed. In this way, the structure shown in FIG. **7** is formed.

[0131] At step S**1206**, a first support portion and a second support portion are formed on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion. For example, a first support portion **141** and a second support portion **142** are formed on the gate insulating layer **130** covering the substrate **110** and located on both sides of the gate **120** by using processes such as deposition and patterning, so as to form the structure as shown in FIG. **8**, wherein the first support portion **141** is not connected to the second support portion **142**. The first support portion **141** and the second support portion **142** are respectively on both sides of the gate **120**. Materials of the first support portion **141** and the second support portion **142** may comprise a conductive material (e.g., a metal material). For example, the first support portion **141** may serve as a source, and the second support portion **142** may serve as a drain.

[0132] At step S**1208**, a semiconductor layer is formed on the first support portion, the second support portion, and the gate insulating layer covering the gate. For example, a semiconductor layer **150** is formed on the first support portion **141**, the second support portion **142**, and the gate insulating layer **130** covering the gate **120** by processes such as deposition and patterning, so as to form the structure as shown in FIG. **1**. The first support portion **141** and the second support portion **142** each are configured to support the semiconductor layer **150**.

[0133] In some embodiments, an annealing process is performed on the semiconductor layer **150**. For example, the annealing process may crystallize the semiconductor layer. For another example, during the annealing process, a solid solution of a metal and a semiconductor material is formed in an area where the first support portion **141** and the second support portion **142** are in contact with the semiconductor layer **150** respectively, thereby forming an ohmic contact.

[0134] At step S**1210**, an electrode connected to the first support portion or the second support portion is formed. For example, the electrode is an anode.

[0135] For example, as shown in FIG. **13**, an interlayer dielectric layer **160** may be formed on the structure shown in FIG. **1** by a process such as deposition. For example, a thickness of the interlayer dielectric layer **160** may range from 1000 Å to 3000 Å. The interlayer dielectric layer **160** is etched to form a first through hole exposing the second support portion **142** (or the first support portion **141**). Next, a planarization layer **210** is formed on the interlayer dielectric layer **160**. The planarization layer **210** is etched to form a second through hole, wherein the second through hole is aligned with the first through hole. Then, an electrode **220** that passes through the second through hole and the first through hole and is in contact with the second support portion **142** (or the first support portion **141**) is formed by a process such as deposition.

[0136] At step S**1212**, a functional layer is formed on a side of the electrode facing away from the substrate.

[0137] For example, a pixel definition layer **230** may be formed on the structure shown in FIG. **13** by using processes such as deposition and patterning, and a functional layer **240** passing through the pixel definition layer **230** and in contact with the electrode **220** is then formed, so as to form the structure as shown in FIG. **3**.

[0138] In some embodiments, as shown in FIG. **3**, a photo spacer **250** may be further formed on the pixel definition layer **230**.

[0139] So far, a manufacturing method for a pixel structure according to other embodiments of the present disclosure is provided. In the manufacturing method, since the first support portion and the second support portion are formed, the height difference of the gate insulating layer caused by the gate is reduced, which is advantageous for the semiconductor layer to be in the same focal plane of laser, thereby improving the crystallization quality of the semiconductor layer. Moreover, the first support portion may serve as a source, and the second support portion may serve as a drain, thereby simplifying the process flow.

[0140] Hereto, various embodiments of the present disclosure have been described in detail. Some details well known in the art are not described to avoid obscuring the concept of the present disclosure. According to the above description, those skilled in the art would fully know how to implement the technical solutions disclosed herein.

[0141] Although some specific embodiments of the present disclosure have been described in detail by way of examples, those skilled in the art should understand that the above examples are only for the purpose of illustration and are not intended to limit the scope of the present disclosure. It should be understood by those skilled in the art that modifications to the above embodiments and equivalently

substitution of part of the technical features may be made without departing from the scope and spirit of the present disclosure. The scope of the present disclosure is defined by the appended claims.

1. A thin film transistor provided on a substrate, comprising:
a gate on the substrate;
a gate insulating layer covering the gate and the substrate;
a first support portion and a second support portion, which are provided on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion;
a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate; and
a source and a drain each connected to the semiconductor layer;
wherein the first support portion and the second support portion each are configured to support the semiconductor layer.

2. The thin film transistor according to claim **1**, wherein:
surfaces on a side of the first support portion and the second support portion facing away from the substrate are flush with a surface on a side of a portion of the gate insulating layer on the gate facing away from the substrate; and
the first support portion and the second support portion are provided at a step formed by the gate insulating layer on both sides of the gate, and extending directions of the first support portion and the second support portion are the same as that of the semiconductor layer.

3. The thin film transistor according to claim **2**, wherein
an orthographic projection of the semiconductor layer on the substrate is located inside an orthographic projection of the gate, the first support portion, and the second support portion on the substrate.

4. The thin film transistor according to claim **1**, wherein
the source is above the first support portion, and the drain is above the second support portion.

5. The thin film transistor according to claim **1**, wherein
materials of the first support portion and the second support portion comprise a conductive material,
the first support portion serves as the source, and the second support portion serves as the drain.

6. The thin film transistor according to claim **5**, wherein
the conductive material comprises a metal material; and
a solid solution of a metal and a semiconductor material is formed in areas where the first support portion and the second support portion are in contact with the semiconductor layer respectively.

7. The thin film transistor according to claim **6**, wherein
the metal material comprises aluminum;
a material of the semiconductor layer comprises polysilicon; and
the solid solution is a solid solution of silicon and aluminum.

8. The thin film transistor according to claim **1**, wherein
a material of the gate insulating layer comprises MgO.

9. A pixel structure, comprising:
the thin film transistor according to claim **1**.

10. An array substrate, comprising the thin film transistor according to claim **1**.

11. A display device, comprising the array substrate according to claim **10**.

12. A manufacturing method for a thin film transistor, comprising:
forming a gate on a substrate;
forming a gate insulating layer covering the gate and the substrate;
forming a first support portion and a second support portion on the gate insulating layer covering the substrate and located on both sides of the gate, wherein the first support portion is not connected to the second support portion;
forming a semiconductor layer on the first support portion, the second support portion, and the gate insulating layer covering the gate; and
forming a source and a drain each connected to the semiconductor layer;
wherein the first support portion and the second support portion each are configured to support the semiconductor layer.

13. The manufacturing method according to claim **12**, further comprising:
performing an annealing treatment on the semiconductor layer.

14. The manufacturing method according to claim **13**, wherein after performing the annealing treatment, the manufacturing method further comprises:
doping an area of the semiconductor layer on the first support portion and an area of the semiconductor layer on the second support portion; and
forming the source and the drain respectively connected to the semiconductor layer in respective doped areas, wherein the source and the drain respectively form an ohmic contact with the respective doped areas.

15. The manufacturing method according to claim **13**, wherein
materials of the first support portion and the second support portion comprise a conductive material, the first support portion serves as the source, and the second support portion serves as the drain.

16. The manufacturing method according to claim **15**, wherein
the conductive material comprises a metal material;
before performing the annealing treatment on the semiconductor layer, a material of the semiconductor layer comprises amorphous silicon; and
the performing the annealing treatment on the semiconductor layer comprises: annealing the semiconductor layer by a laser annealing process to convert the amorphous silicon into polysilicon,
wherein, by the laser annealing process, a solid solution of a metal and a semiconductor material is also formed in areas where the first support portion and the second support portion are in contact with the semiconductor layer respectively so as to form an ohmic contact.

17. The manufacturing method according to claim **16**, wherein
the metal material comprises aluminum; and
the solid solution is a solid solution of silicon and aluminum.

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