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(54) **SYSTEMS AND METHODS FOR SHORT MEDIA DEFECT DETECTION USING MULTI-ITERATION SOFT DATA FEEDBACK**

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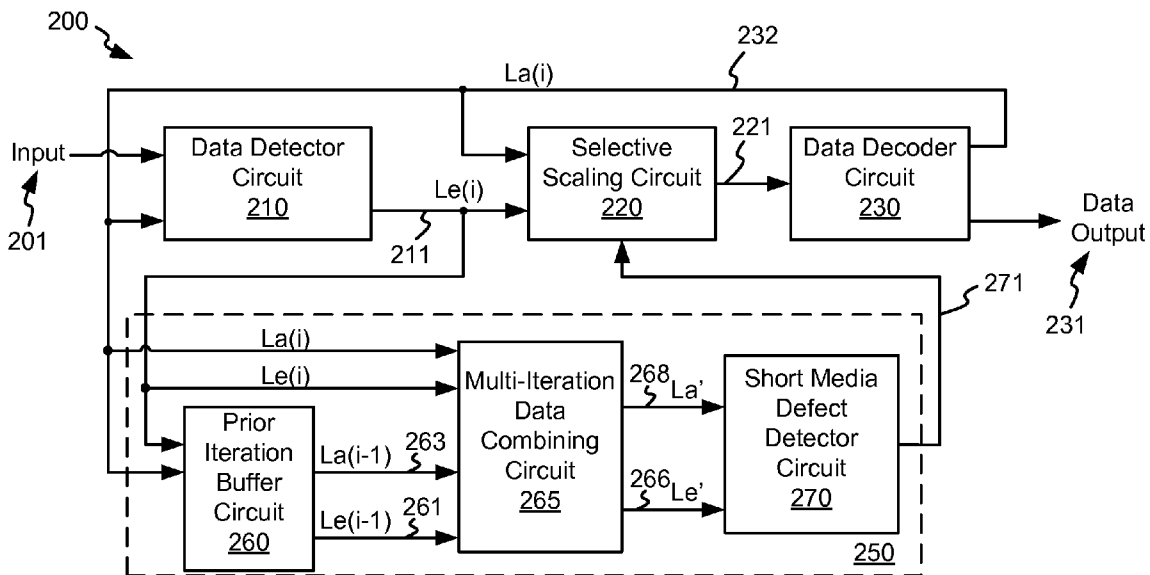
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(57) **ABSTRACT**
Various systems and methods for media defect detection.



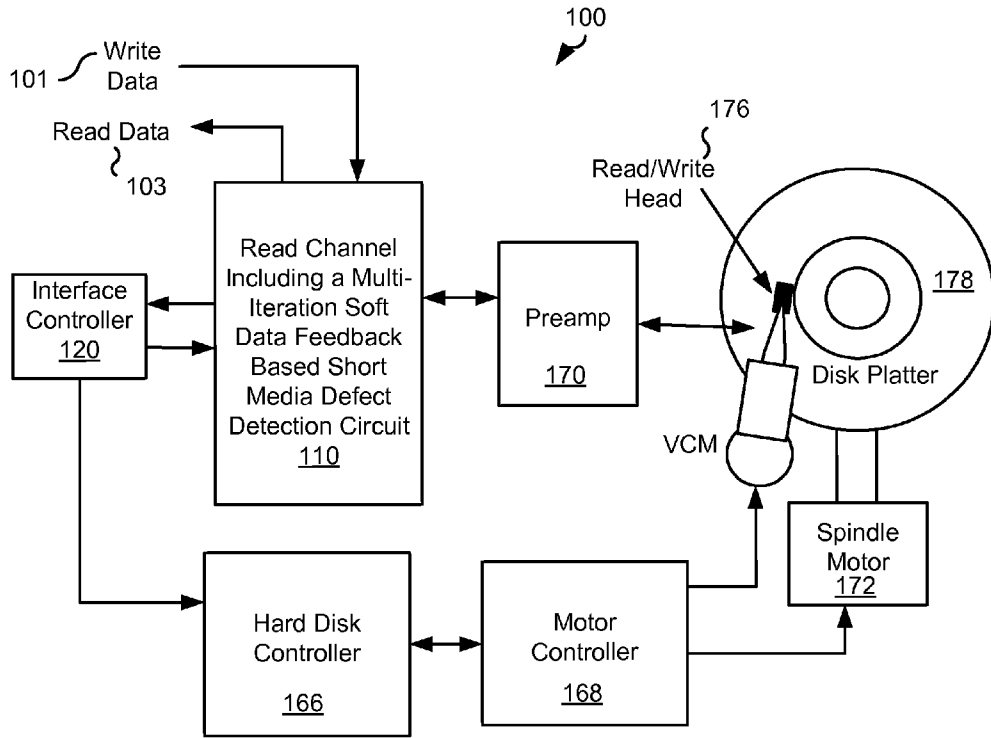


Fig. 1

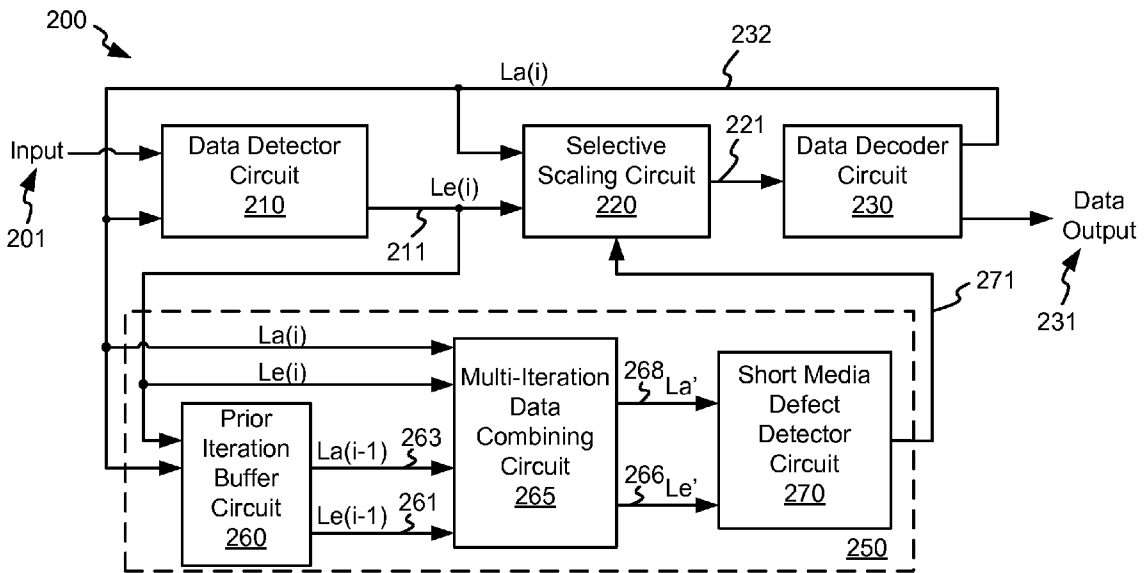


Fig. 2

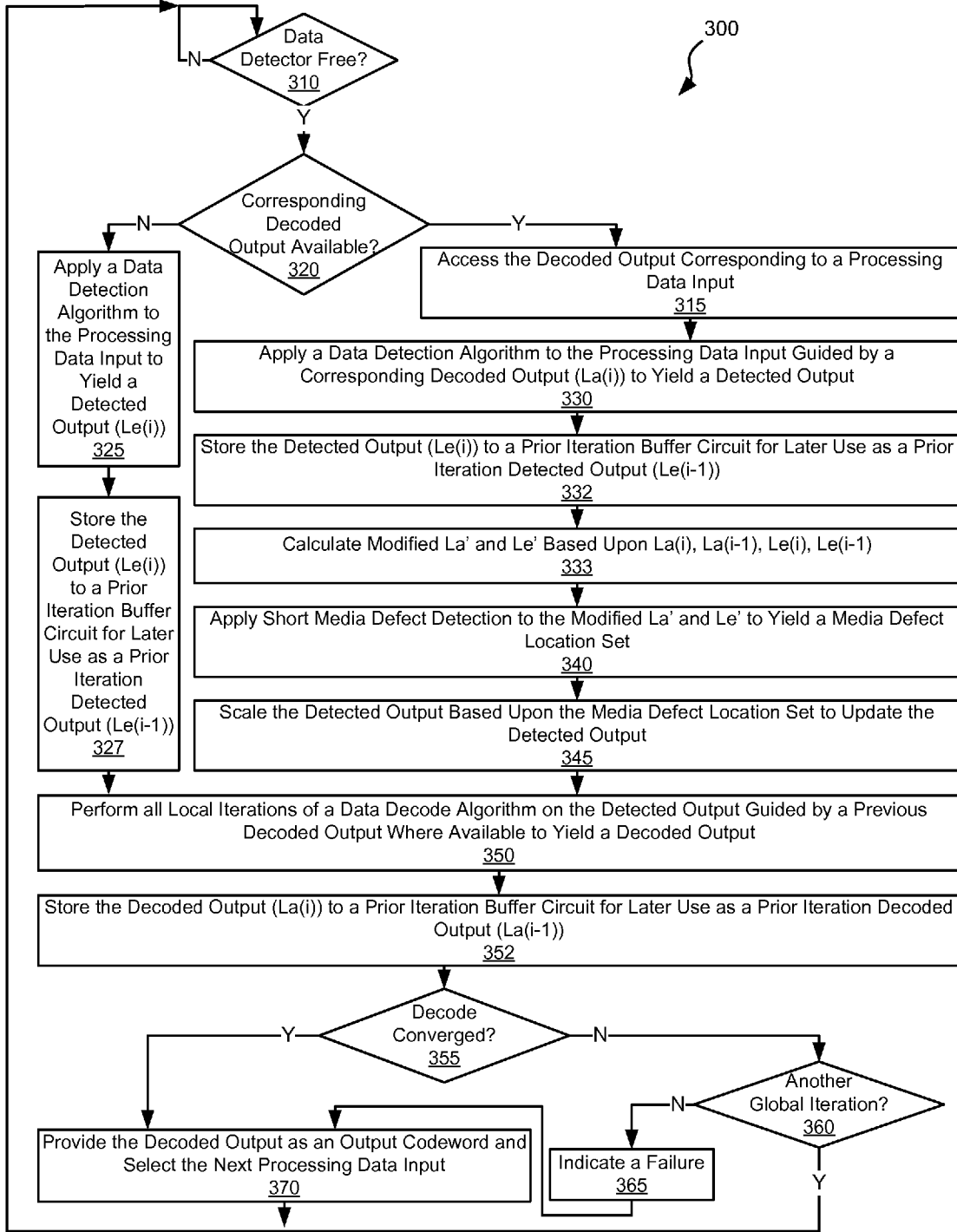


Fig. 3

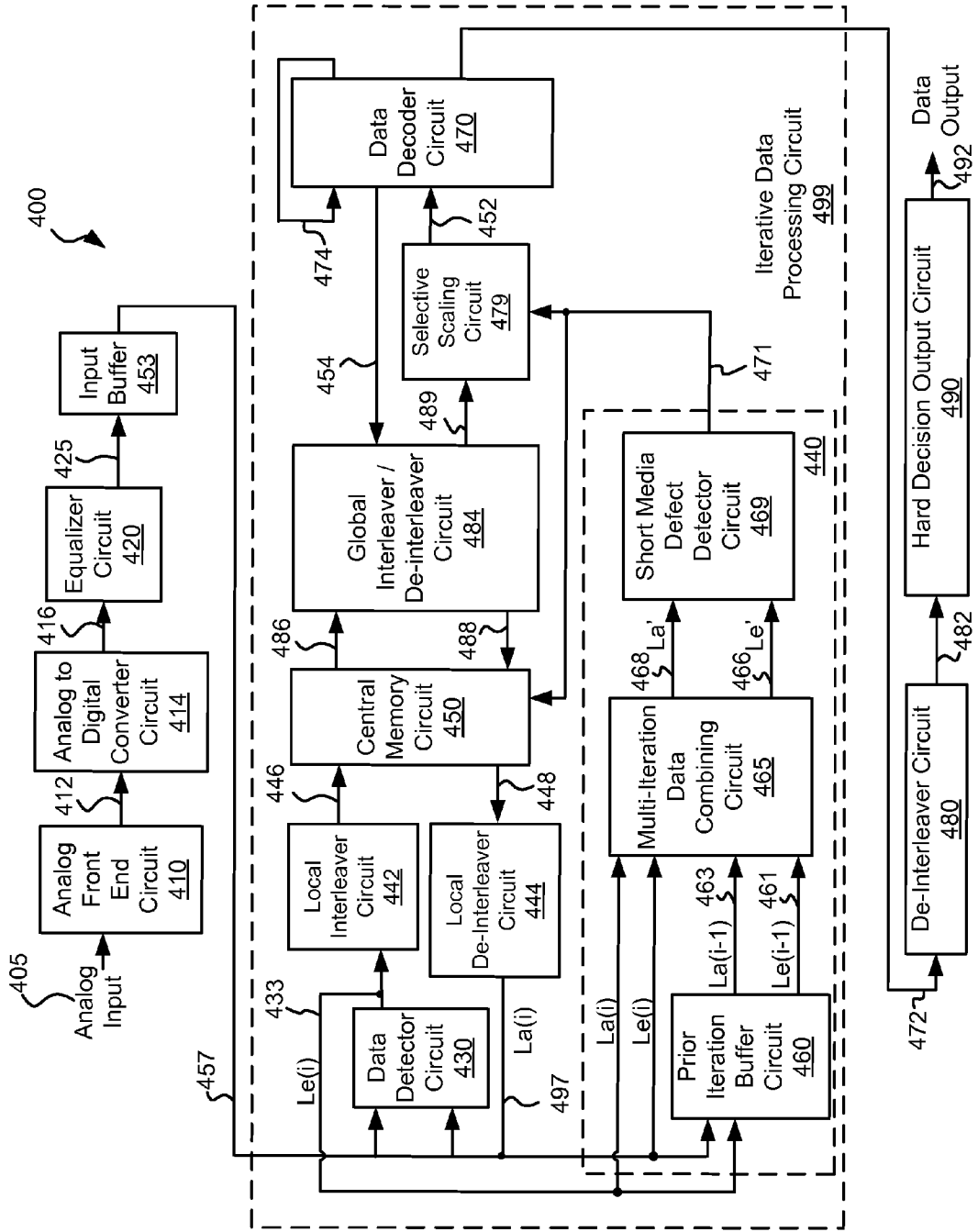


Fig. 4

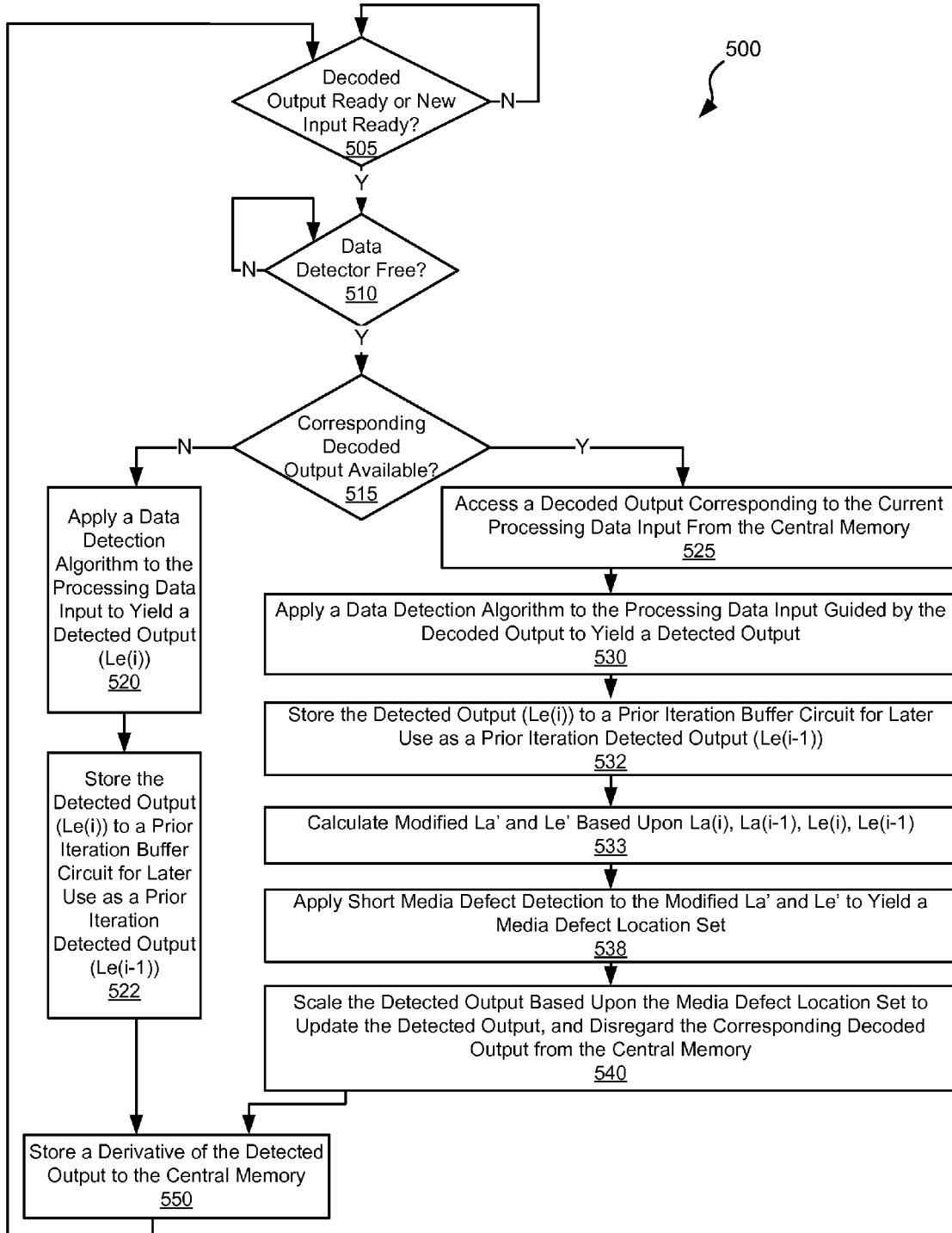


Fig. 5a

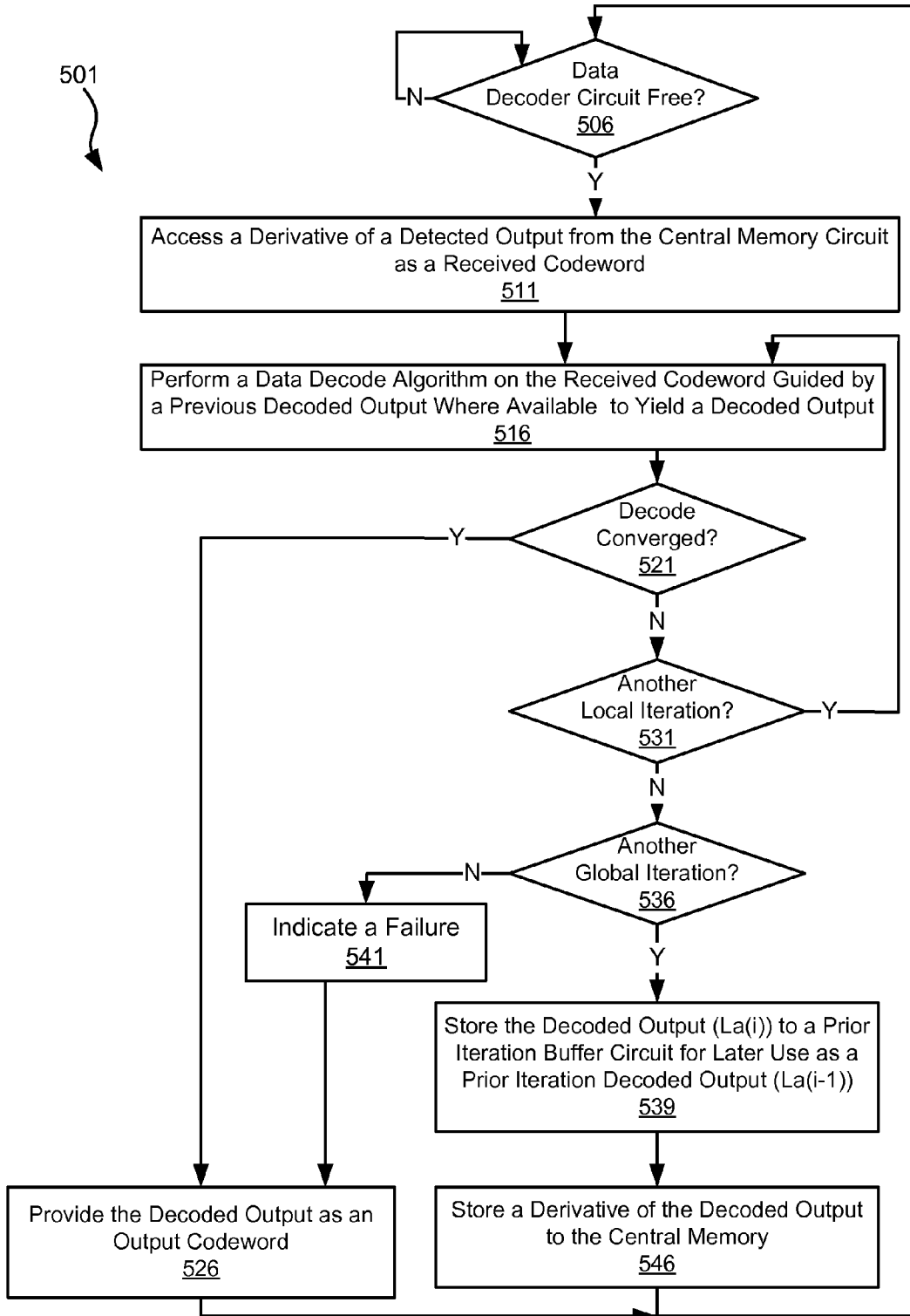


Fig. 5b

SYSTEMS AND METHODS FOR SHORT MEDIA DEFECT DETECTION USING MULTI-ITERATION SOFT DATA FEEDBACK

BACKGROUND

[0001] Embodiments are related to systems and methods for transferring information, and more particularly to systems and methods for determining problems related to a medium associated with a data transfer.

[0002] Various data transfer systems have been developed including storage systems, cellular telephone systems, radio transmission systems. In each of the systems data is transferred from a sender to a receiver via some medium. For example, in a storage system, data is sent from a sender (i.e., a write function) to a receiver (i.e., a read function) via a storage medium. The effectiveness of any transfer is impacted by any defects associated with the transfer medium. In some cases, data loss caused by defects in the transfer medium can make recovery of data from the transfer medium difficult even for data received from non-defective areas or times. Various approaches have been developed for identifying defects in the transfer medium. Such approaches provide a general ability to identify defects, but in many cases are inaccurate. In the best case, this inaccuracy limits the effectiveness of any defect identification. In the worst case, inaccurate defect detection may actually hamper the data recovery process.

[0003] Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for defect detection.

BRIEF SUMMARY

[0004] Embodiments are related to systems and methods for transferring information, and more particularly to systems and methods for determining problems related to a medium associated with a data transfer.

[0005] Various embodiments of the present inventions provide data processing systems. The data processing systems include: a data detector circuit, a defect identification circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to a detector input to yield a first detected output and a second detected output. The first detected output is derived from a first iteration applying the data detection algorithm, and the second detected output is derived from a second iteration applying the data detection algorithm. The defect detection circuit includes: a multi-iteration data combining circuit and a media defect detector circuit. The multi-iteration data combining circuit is operable to combine the first detected output with the second detected output to yield a modified detected output. The media defect detector circuit operable to apply a media defect detection algorithm to at least the modified detected output to yield a defect indicator. The data decoder circuit is operable to apply a data decode algorithm to a decoder input derived from the second detected output modified based on the defect indicator to yield a decoded output.

[0006] This summary provides only a general outline of some embodiments of the invention. The phrases “in one embodiment,” “according to one embodiment,” “in various embodiments”, “in one or more embodiments”, “in particular embodiments” and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the

present invention. Importantly, such phrases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

[0008] FIG. 1 shows a storage system including a read channel with a multi-iteration soft data feedback based short defect detector circuit in accordance with various embodiments of the present invention;

[0009] FIG. 2 depicts a data processing circuit including a multi-iteration soft data feedback based short defect detector circuit in accordance with various embodiments of the present invention;

[0010] FIG. 3 is a flow diagram showing a method in accordance with some embodiments of the present invention for data processing including multi-iteration soft data feedback based short media defect detection;

[0011] FIG. 4 shows another data processing circuit including a multi-iteration soft data feedback based short defect detector circuit in accordance with various embodiments of the present invention; and

[0012] FIGS. 5a-5b are flow diagrams showing a method in accordance with one or more embodiments of the present invention for data processing including multi-iteration soft data feedback based short media defect detection.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0013] Embodiments are related to systems and methods for transferring information, and more particularly to systems and methods for determining problems related to a medium associated with a data transfer.

[0014] Various embodiments of the present inventions provide data processing systems. The data processing systems include: a data detector circuit, a defect identification circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to a detector input to yield a first detected output and a second detected output. The first detected output is derived from a first iteration applying the data detection algorithm, and the second detected output is derived from a second iteration applying the data detection algorithm. The defect detection circuit includes: a multi-iteration data combining circuit and a media defect detector circuit. The multi-iteration data combining circuit is operable to combine the first detected output with the second detected output to yield a modified detected output. The media defect detector circuit operable to apply a media defect detection algorithm to at least the modified detected output to yield a defect indicator. The data decoder circuit is operable to apply a data decode algorithm to a first decoder input derived from the first detected output modified based on the defect indica-

tor to yield a first decoded output, and to apply the data decode algorithm to a second decoder input derived from the second detected output modified based on the defect indicator to yield a second decoded output.

[0015] In some instances of the aforementioned embodiments where the decoder input is a first decoder input and the decoder output is a first decoder output: the data detector circuit is further operable to apply the data detection algorithm to the detector input to yield a third detected output, where the third detected output is derived from a third iteration applying the data detection algorithm; the data decoder circuit is further operable to apply the data decode algorithm to a second decoder input derived from the third detected output modified based on the defect indicator to yield a second decoded output; the multi-iteration data combining circuit is further operable to combine a first decoded output and the second decoded output to yield a modified decoded output; and the media defect detector circuit is operable to apply the media defect detection algorithm to a combination of the modified detected output and the modified decoded output to yield the defect indicator. In some such instances, the modified decoded output is calculated in accordance with the following equation:

$$\text{modified decoded output} = \text{scalar} * \text{first decoded output} + \text{second decoded output},$$

where the scalar is a negative value. In some cases, the scalar is programmable.

[0016] In one or more instances of the aforementioned embodiments, the defect detection circuit further includes a memory operable to store the first detected output until the second detected output is available. In some instances of the aforementioned embodiments, the modified detected output is calculated in accordance with the following equation:

$$\text{modified detected output} = \text{scalar} * \text{first detected output} + \text{second detected output},$$

where the scalar is a negative value. In some cases, the scalar is programmable.

[0017] In various instances of the aforementioned embodiments, the system further includes a memory operable to pass a derivative of the first decoded output and a derivative of the second decoded output to the data detector circuit, and to pass a derivative of the first detected output and the derivative of the second detected output to the data decoder circuit. The media defect detector circuit is operable to disregard the second decoded output in the memory based at least in part upon assertion of the defect indicator. In one or more instances of the aforementioned embodiments, modifying the first detected output includes multiplying the first detected output by a scalar.

[0018] Other embodiments of the present invention provide methods for data processing that include receiving a first detected output and a second detected output. The first detected output is derived from a first iteration applying a data detection algorithm by a data detector circuit to a detector input, and the second detected output is derived from a second iteration applying the data detection algorithm to the detector input. The methods further include: calculating a modified detected output based on the first detected output and the second detected output; determining a defect on a medium from which the detector input is derived based at least in part on the modified detected output to yield a defect indicator; and applying a data decode algorithm by a data decoder circuit to a first decoder input derived from the first detected

output modified based on the defect indicator to yield a first decoded output, and applying the data decode algorithm to a second decoder input derived from the second detected output modified based on the defect indicator to yield a second decoded output.

[0019] In some instances of the aforementioned embodiments where the decoder input is a first decoder input and the decoder output is a first decoder output, the methods further include: applying the data detection algorithm to the detector input to yield a third detected output, where the third detected output is derived from a third iteration applying the data detection algorithm; applying the data decode algorithm by the data decoder circuit to a second decoder input derived from the third detected output modified based on the defect indicator to yield a second decoded output; and calculating a modified decoded output based on the first decoded output and the second decoded output. In such instances, determining the defect on the medium is based upon the modified detected output and the modified decoded output to yield the defect indicator. In some cases, the modified decoded output is calculated in accordance with the following equation:

$$\text{modified decoded output} = \text{scalar} * \text{first decoded output} + \text{second decoded output},$$

where the scalar is a negative value. In some cases, the scalar is programmable. In various cases, the modified detected output is calculated in accordance with the following equation:

$$\text{modified detected output} = \text{scalar} * \text{first detected output} + \text{second detected output},$$

where the scalar is a negative value. In some cases, the scalar is programmable. In some instances of the aforementioned embodiments, the methods further include storing the first detected output until the second detected output is available from the data detector circuit.

[0020] Turning to FIG. 1, a storage system 100 including a read channel circuit 110 having a multi-iteration soft data feedback based short defect detector circuit is shown in accordance with various embodiments of the present invention. Storage system 100 may be, for example, a hard disk drive. Storage system 100 also includes a preamplifier 170, an interface controller 120, a hard disk controller 166, a motor controller 168, a spindle motor 172, a disk platter 178, and a read/write head assembly 176. Interface controller 120 controls addressing and timing of data to/from disk platter 178. The data on disk platter 178 consists of groups of magnetic signals that may be detected by read/write head assembly 176 when the assembly is properly positioned over disk platter 178. In one embodiment, disk platter 178 includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

[0021] In operation, read/write head assembly 176 is accurately positioned by motor controller 168 over a desired data track on disk platter 178. Motor controller 168 both positions read/write head assembly 176 in relation to disk platter 178 and drives spindle motor 172 by moving read/write head assembly to the proper data track on disk platter 178 under the direction of hard disk controller 166. Spindle motor 172 spins disk platter 178 at a determined spin rate (RPMs). Once read/write head assembly 176 is positioned adjacent the proper data track, magnetic signals representing data on disk platter 178 are sensed by read/write head assembly 176 as disk platter 178 is rotated by spindle motor 172. The sensed magnetic signals are provided as a continuous, minute analog

signal representative of the magnetic data on disk platter **178**. This minute analog signal is transferred from read/write head assembly **176** to read channel circuit **110** via preamplifier **170**. Preamplifier **170** is operable to amplify the minute analog signals accessed from disk platter **178**. In turn, read channel circuit **110** decodes and digitizes the received analog signal to recreate the information originally written to disk platter **178**. This data is provided as read data **103**.

[0022] As part of processing data accessed from disk platter **178**, read channel circuit **110** performs a media defect detection process operable to determine whether received data is associated with a defective region of disk platter **178**. This media defect detection includes using multi-iteration soft data feedback to enhance the media defect detection. In some embodiments of the present invention, the data processing circuit including the multi-iteration soft data feedback based short media defect detector circuit may be implemented similar to that discussed below in relation to FIG. **2** or FIG. **4**, and/or may apply data processing similar to that discussed below in relation to FIG. **3** or FIGS. **5a-5b**.

[0023] It should be noted that storage system **100** may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system **100**, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

[0024] A data decoder circuit used in relation to read channel circuit **110** may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

[0025] In addition, it should be noted that storage system **100** may be modified to include solid state memory that is used to store data in addition to the storage offered by disk

platter **178**. This solid state memory may be used in parallel to disk platter **178** to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit **110**. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platter **178**. In such a case, the solid state memory may be disposed between interface controller **120** and read channel circuit **110** where it operates as a pass through to disk platter **178** when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter **178** and a solid state memory.

[0026] Turning to FIG. **2** depicts a data processing circuit **200** including a multi-iteration soft data feedback based short defect detector circuit **250** in accordance with various embodiments of the present invention. Multi-iteration soft data feedback based short defect detector circuit **250** includes a prior iteration buffer circuit **260**, a multi-iteration data combining circuit **265**, and a short media defect detector circuit **270**. Data processing circuit **200** includes a data detector circuit **210** that applies a data detection algorithm to a data input **201** guided by a soft decoded output **232**. Soft decoded output **232** is denoted $L_a(i)$, where 'i' represents the iteration number. In particular, 'i' indicates data derived from the most recent iteration, and 'i-1' indicates data derived from a preceding iteration.

[0027] In some embodiments of the present invention, data input **201** is derived from a storage medium. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources for data input **201**. Data detector circuit **210** may be, but is not limited to, a maximum a posteriori data detector circuit, or a Viterbi algorithm data detector circuit. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. Application of the data detection algorithm by data detector circuit **210** yields a detected output **211**. Detected output **211** is denoted $L_e(i)$, where 'i' represents the iteration number. In particular, 'i' indicates data derived from the most recent iteration, and 'i-1' indicates data derived from a preceding iteration. An iteration denoted by 'i' is a global iteration which is defined as processing a data set through both data detector circuit **210** and a data decoder circuit **230**.

[0028] Detected output **211** and soft decoded output **232** are provided to both a prior iteration buffer circuit **260** and a multi-iteration data combining circuit **265**. Prior iteration buffer circuit **260** stores detected output **211** and soft decoded

output **232** until it is aligned with the corresponding data from a subsequent iteration. In particular, prior iteration buffer circuit **260** provides detected output **261** ($Le(i-1)$) and soft decoded output **263** ($La(i-1)$) from a preceding iteration that are aligned with detected output **211** ($Le(i)$) and soft decoded output **232** ($La(i)$) from the most recent iteration. Detected output **261** ($Le(i-1)$) and soft decoded output **263** ($La(i-1)$) are provided to multi-iteration data combining circuit **265**.

[0029] In turn, multi-iteration data combining circuit **265** calculates a modified detected output **266** (Le') and a modified soft decoded output **268** (La') in accordance with the following equations after the first global iteration (i.e., $i=0$) has completed:

$$La' = \text{ScalarA} * La(i-1) + La(i), \text{ and}$$

$$Le' = \text{ScalarB} * Le(i-1) + Le(i).$$

ScalarA and ScalarB may be any values between zero to negative 0.99. In one particular embodiment of the present invention, ScalarA is -0.5 , and ScalarB is -0.5 . Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of scalar values that may be used for ScalarA and ScalarB in accordance with various embodiments of the present invention. For the first global iteration (i.e., $i=0$), modified detected output **266** (Le') and modified soft decoded output **268** (La') are calculated in accordance with the following equations:

$$La' = La(0), \text{ and}$$

$$Le' = Le(0).$$

[0030] Modified detected output **266** (Le') and Modified soft decoded output **268** (La') are provided to a short media defect detector circuit **270** that performs a short media defect detection. Short media defect detector circuit **270** may be any circuit operable to identify a potential media defect based upon a detected output and a decoded output. In one particular embodiment of the present invention, short media defect detector circuit **270** may be implemented similar to that disclosed in U.S. Pat. No. 8,201,051 entitled "Method for Detecting Short Burst Errors in LDPC System", issued Jun. 12, 2012 to Tan et al. The entirety of the aforementioned reference is incorporated herein by reference for all purposes. Where short media defect detector circuit **270** identifies a potential media defect, a defect indicator **271** is asserted. Otherwise, defect indicator **271** is not asserted.

[0031] Defect indicator **271** is provided to a selective scaling circuit **220**. Selective scaling circuit **220** delays detected output **211** to align it with defect indicator **271**. Where defect indicator **271** is asserted, selective scaling circuit **220** applies a symbol by symbol scaling to each symbol in soft decoded output **232** that corresponds to defect indicator **271**, and passes detected output **211** through on a symbol by symbol basis where defect indicator **271** is not asserted. This scaling operates to modify soft data associated with the effected symbols to reduce the probability that the symbol is considered properly found. By doing this, the likelihood that an effected symbol negatively impacts processing of the data set is reduced and the likelihood that the symbol will be modified by later processing is increased. Selective scaling circuit **220** provides a scaled output **221** to a data decoder circuit **230**. For the purposes of this document, a symbol may be either a non-binary symbol or a binary symbol depending upon the particular implementation.

[0032] Data decoder circuit **230** applies a data decode algorithm to scaled output **221** to yield a decoded output that includes soft decoded output **232**. In some embodiments of the present invention, data decoder circuit **230** is a low density parity check decoder circuit as are known in the art. Where the decoded output converges (i.e., yields the original data set as indicated by the lack of remaining errors), it is provided as a data output **231**.

[0033] Turning to FIG. 3, a flow diagram **300** shows a method in accordance with some embodiments of the present invention for data processing including multi-iteration soft data feedback based short media defect detection. Following flow diagram **300**, it is determined whether a data detector circuit is available to process a newly received data set or a data set that has already been subject to one or more prior global iterations (block **310**). As used herein, the phrase "global iteration" is used in its broadest sense to mean application of both a data detection algorithm and a data decode algorithm. Also, as used herein, the phrase "local iteration" is used in its broadest sense to mean an application of the data decode algorithm. In some instances of the present invention, one or more local iterations may be performed for each global iteration.

[0034] Where a data detector circuit is available (block **310**), a processing data input is accessed and it is determined whether a decoded output corresponding to the accessed processing data input exists (block **320**). Such a decoded output is available as a result from a preceding global iteration applied to the same processing data input. The processing data input may be, for example, derived from a storage medium. Where a corresponding decoded output is not available (block **320**), a data detection algorithm is applied to the processing data input to yield a detected output (block **325**). The data detection algorithm may be, but is not limited to, a Viterbi data detection algorithm or a maximum a posteriori data detection algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detection algorithms that may be used in relation to different embodiments of the present invention. The detected output ($Le(i)$) is stored to a prior iteration buffer circuit for later use as a prior iteration detected output ($Le(i-1)$) (block **327**).

[0035] Alternatively, where a corresponding decoded output ($La(i)$) is available (block **320**) it is accessed (block **315**) and a data detection algorithm is applied to the processing data input guided by the corresponding decoded output ($La(i)$) to yield a detected output ($Le(i)$) (block **330**). Such a corresponding decoded output is available for the second or later global iterations (i.e., $i \geq 1$) for a given processing data input. The detected output ($Le(i)$) is stored to a prior iteration buffer circuit for later use as a prior iteration detected output ($Le(i-1)$) (block **332**). A modified detected output (Le') and a modified decoded output (La') are calculated (block **333**) based upon decoded output from both the most recent global iteration ($La(i)$) and from the preceding global iteration ($La(i-1)$), and detected output from both the most recent global iteration ($Le(i)$) and from the preceding global iteration ($Le(i-1)$) in accordance with the following equations:

$$La' = \text{ScalarA} * La(i-1) + La(i), \text{ and}$$

$$Le' = \text{ScalarB} * Le(i-1) + Le(i).$$

ScalarA and ScalarB may be any values between zero to negative 0.99. In one particular embodiment of the present invention, ScalarA is -0.5 , and ScalarB is -0.5 . Based upon

the disclosure provided herein, one of ordinary skill in the art will recognize a variety of scalar values that may be used for ScalarA and ScalarB in accordance with various embodiments of the present invention.

[0036] A short media defect detection is applied to the suspect symbol indicator to determine whether a media defect is likely, and if so to provide a media defect location set (block 340). Such a media defect location set indicates which data in the processing data set corresponds to the likely media defect. The short media defect detection may be any media defect detection process known in the art. In one particular embodiment of the present invention, the binary media defect detection processed may be done similar to that disclosed in U.S. Pat. No. 8,201,051 entitled "Method for Detecting Short Burst Errors in LDPC System", issued Jun. 12, 2012 to Tan et al. The entirety of the aforementioned reference is incorporated herein by reference for all purposes.

[0037] Symbols of the detected output corresponding to the media defect location set are scaled to update the detected output (block 345). This scaling operates to modify soft data associated with the effected symbols to reduce the probability that the symbol is considered properly found. By doing this, the likelihood that an effected symbol negatively impacts processing of the data set is reduced and the likelihood that the symbol will be modified by later processing is increased.

[0038] All local iterations of a data decode algorithm are then applied to the detected output guided by a previous decoded output where available (block 350). This process generates an updated decoded output that may be used during subsequent global iterations where it does not converge (i.e., have no remaining unsatisfied checks). In some embodiments of the present invention, the data decode algorithm is a low density parity check algorithm as is known in the art. The decoded output (La(i)) is stored to the prior iteration buffer circuit for later use as a prior iteration decoded output (La(i-1)) (block 352).

[0039] It is determined whether the data decode algorithm converged (block 355). Where the data decode algorithm converged (block 355), the decoded output is provided as an output codeword, and the next processing data input is selected for processing (block 370). Alternatively, where the data decode algorithm failed to converge (block 355), it is determined whether another global iteration is allowed (block 360). Where another global iteration is not allowed (block 360), a failure is indicated (block 361) and the decoded output is provided as an output codeword, and the next processing data input is selected for processing (block 370). In contrast, where another global iteration is allowed (block 360), a subsequent location iteration is applied to the same processing data input guided by the results of the preceding global iteration.

[0040] Turning to FIG. 4, another data processing circuit 400 including a multi-iteration soft data feedback based short defect detector circuit 440 (shown in dashed lines) is shown in accordance with various embodiments of the present invention. Data processing circuit 400 includes an analog front end circuit 410 that receives an analog signal 405. Analog front end circuit 410 processes analog signal 405 and provides a processed analog signal 412 to an analog to digital converter circuit 414. Analog front end circuit 410 may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end

circuit 410. In some cases, analog signal 405 is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of media from which analog signal 405 may be derived.

[0041] Analog to digital converter circuit 414 converts processed analog signal 412 into a corresponding series of digital samples 416. Analog to digital converter circuit 414 may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples 416 are provided to an equalizer circuit 420. Equalizer circuit 420 applies an equalization algorithm to digital samples 416 to yield an equalized output 425. In some embodiments of the present invention, equalizer circuit 420 is a digital finite impulse response filter circuit as are known in the art. It may be possible that equalized output 425 may be received directly from a storage device in, for example, a solid state storage system. In such cases, analog front end circuit 410, analog to digital converter circuit 414 and equalizer circuit 420 may be eliminated where the data is received as a digital data input.

[0042] Equalized output 425 is stored to an input buffer 453 that includes sufficient memory to maintain one or more codewords until processing of that codeword is completed through an iterative data processing circuit 499 (outlined by dashed lines) including, where warranted, multiple global iterations (passes through both a data detector circuit 430 and a data decoder circuit 470) and/or local iterations (passes through data decoder circuit 470 during a given global iteration). An output 457 is provided to a data detector circuit 430

[0043] Data detector circuit 430 may be a single data detector circuit or may be two or more data detector circuits operating in parallel on different codewords (i.e., data sets). Whether it is a single data detector circuit or a number of data detector circuits operating in parallel, data detector circuit 430 is operable to apply a data detection algorithm to a received codeword or data set. In some embodiments of the present invention, data detector circuit 430 is a Viterbi algorithm data detector circuit as are known in the art. In other embodiments of the present invention, data detector circuit 430 is a maximum a posteriori data detector circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. In some cases, one data detector circuit included in data detector circuit 430 is used to apply the data detection algorithm to the received codeword for a first global iteration applied to the received codeword, and another data detector circuit included in data detector circuit 430 is operable to apply the data detection algorithm to the received codeword guided by a decoded output accessed from a central memory circuit 450 on subsequent global iterations.

[0044] Upon completion of application of the data detection algorithm to the received codeword (i.e., processing data input) on the first global iteration, data detector circuit 430 provides a detector output 433. Detector output 433 includes soft data (Le(i)). The 'i' represents the iteration number. In particular, 'i' indicates data derived from the most recent

iteration, and ‘i-1’ indicates data derived from a preceding iteration. As used herein, the phrase “soft data” is used in its broadest sense to mean reliability data with each instance of the reliability data indicating a likelihood that a corresponding bit position or symbol has been correctly detected. In some embodiments of the present invention, the soft data or reliability data is log likelihood ratio data as is known in the art. Detected output 433 is provided to a local interleaver circuit 442. Local interleaver circuit 442 is operable to shuffle sub-portions (i.e., local chunks) of the data set included as detected output and provides an interleaved codeword 446 that is stored to central memory circuit 450. Interleaver circuit 442 may be any circuit known in the art that is capable of shuffling data sets to yield a re-arranged data set. Interleaved codeword 446 is stored to central memory circuit 450.

[0045] Once data decoder circuit 470 is available, a previously stored interleaved codeword 446 is accessed from central memory circuit 450 as a stored codeword 486 and globally interleaved by a global interleaver/de-interleaver circuit 484. Global interleaver/De-interleaver circuit 484 may be any circuit known in the art that is capable of globally rearranging codewords. Global interleaver/De-interleaver circuit 484 provides a de-interleaved output 489 to a selective scaling circuit 479. As more fully described below, selective scaling circuit 479 selectively scales de-interleaved output 489 based upon a defect indicator 471 to yield a decoder input 452 into data decoder circuit 470. In some embodiments of the present invention, data decoder circuit 470 is a low density parity check decoder circuit as are known in the art. Application of the data decode algorithm by data decoder circuit 470 yield a decoded output 474. In cases where the decoded output 474 fails to converge (i.e., failed to yield the originally written data set) and another local iteration (i.e., another pass through data decoder circuit 470) is desired, data decoder circuit 470 re-applies the data decode algorithm to decoder input 452 guided by decoded output 474. This continues until either a maximum number of local iterations is exceeded or decoded output 474 converges.

[0046] Where decoded output 474 fails to converge and a number of local iterations through data decoder circuit 470 exceeds a threshold, the resulting decoded output is provided as a decoded output 454 back to central memory circuit 450 where it is stored awaiting another global iteration through a data detector circuit included in data detector circuit 430. Prior to storage of decoded output 454 to central memory circuit 450, decoded output 454 is globally de-interleaved to yield a globally de-interleaved output 488 that is stored to central memory circuit 450. The global de-interleaving reverses the global interleaving earlier applied to stored codeword 486 to yield decoder input 452. When a data detector circuit included in data detector circuit 430 becomes available, a previously stored de-interleaved output 488 accessed from central memory circuit 450 and locally de-interleaved by a de-interleaver circuit 444. De-interleaver circuit 444 re-arranges decoder output 448 to reverse the shuffling originally performed by interleaver circuit 442. A resulting de-interleaved output 497 (La(i)) is provided to data detector circuit 430 where it is used to guide subsequent detection of a corresponding data set previously received as equalized output 425. De-interleaved output 497 includes soft data (La(i)). The ‘i’ represents the iteration number. In particular, ‘i’ indicates data derived from the most recent iteration, and ‘i-1’ indicates data derived from a preceding iteration.

[0047] Alternatively, where the decoded output converges (i.e., yields the originally written data set), the resulting decoded output is provided as an output codeword 472 to a de-interleaver circuit 480. De-interleaver circuit 480 re-arranges the data to reverse both the global and local interleaving applied to the data to yield a de-interleaved output 482. De-interleaved output 482 is provided to a hard decision output circuit 490. Hard decision output circuit 490 is operable to re-order data sets that may complete out of order back into their original order. Ultimately, hard decision output circuit 490 provides the converged codeword as a data output to a recipient device (not shown).

[0048] Iterative data processing circuit 499 includes multi-iteration soft data feedback based short defect detector circuit 440 that is operable to identify one or more likely defective regions on a medium from which analog signal 405 is derived. Such defective regions are indicated by defect indicator 471 provided to selective scaling circuit 479. Multi-iteration soft data feedback based short defect detector circuit 440 includes a prior iteration buffer circuit 460, a multi-iteration data combining circuit 465, and a short media defect detector circuit 469.

[0049] Detector output 433 (Le(i)) and de-interleaved output 497 (La(i)) are provided to both a prior iteration buffer circuit 460 and a multi-iteration data combining circuit 465. Prior iteration buffer circuit 460 stores detector output 433 and de-interleaved output 497 until it is aligned with the corresponding data from a subsequent iteration. In particular, prior iteration buffer circuit 460 provides detector output 461 (Le(i-1)) and de-interleaved output 463 (La(i-1)) from a preceding iteration that are aligned with detector output 433 (Le(i)) and de-interleaved output 497 (La(i)) from the most recent iteration. Detector output 433 (Le(i-1)) and de-interleaved output 463 (La(i-1)) are provided to multi-iteration data combining circuit 465.

[0050] In turn, multi-iteration data combining circuit 465 calculates a modified detected output 466 (Le’) and a modified soft decoded output 468 (La’) in accordance with the following equations after the first global iteration (i.e., i=0) has completed:

$$La' = \text{ScalarA} * La(i-1) + La(i), \text{ and}$$

$$Le' = \text{ScalarB} * Le(i-1) + Le(i).$$

ScalarA and ScalarB may be any values between zero to negative 0.99. In one particular embodiment of the present invention, ScalarA is -0.5, and ScalarB is -0.5. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of scalar values that may be used for ScalarA and ScalarB in accordance with various embodiments of the present invention. For the first global iteration (i.e., i=0), modified detected output 466 (Le’) and modified soft decoded output 468 (La’) are calculated in accordance with the following equations:

$$La' = La(0), \text{ and}$$

$$Le' = Le(0).$$

[0051] Modified detected output 466 (Le’) and modified soft decoded output 468 (La’) are provided to a short media defect detector circuit 469 that performs a short media defect detection. Short media defect detector circuit 469 may be any circuit operable to identify a potential media defect based upon a detected output and a decoded output. In one particular embodiment of the present invention, short media defect

detector circuit 469 may be implemented similar to that disclosed in U.S. Pat. No. 8,201,051 entitled “Method for Detecting Short Burst Errors in LDPC System”, issued Jun. 12, 2012 to Tan et al. The entirety of the aforementioned reference is incorporated herein by reference for all purposes. Where short media defect detector circuit 469 identifies a potential media defect, a defect indicator 471 is asserted. Otherwise, defect indicator 471 is not asserted.

[0052] Defect indicator 471 is provided to selective scaling circuit 479. Selective scaling circuit 479 delays detector output 433 pulled from central memory circuit 450 and provided as de-interleaved output 489 to align it with defect indicator 471. Where defect indicator 471 is asserted, selective scaling circuit 479 applies a symbol by symbol scaling to each symbol in de-interleaved output 489 that corresponds to defect indicator 471. This scaling operates to modify soft data associated with the effected symbols to reduce the probability that the symbol is considered properly found. By doing this, the likelihood that an effected symbol negatively impacts processing of the data set is reduced and the likelihood that the symbol will be modified by later processing is increased. Selective scaling circuit 479 provides decoder input 452. For the purposes of this document, a symbol may be either a non-binary symbol or a binary symbol depending upon the particular implementation. In addition, when defect indicator 471 is asserted, the decoded output maintained in central memory circuit 450 corresponding to the location of defect indicator 471 is discarded from central memory circuit 450.

[0053] Turning to FIGS. 5a-5b, flow diagrams 500, 501 show a method in accordance with one or more embodiments of the present invention for data processing including multi-iteration soft data feedback based short defect detection. Following flow diagram 500 of FIG. 5a, it is determined whether a decoded output (La(i)) is ready in the central memory to guide re-application of a data detection algorithm to a data processing input, or if a new data processing input is ready for processing (block 505). The index ‘i’ represents the iteration number. In particular, ‘i’ indicates data derived from the most recent iteration, and ‘i-1’ indicates data derived from a preceding iteration. It is then determined whether a data detector circuit is available (block 510). Where a data detector circuit is available (block 510), the next processing data input is accessed and it is determined whether a decoded output corresponding to the detected output is available from the central memory (block 515). The decoded output is available for the second or later global iterations.

[0054] Where a corresponding decoded output (La(i)) is not available (block 515), a data detection algorithm is applied to the processing data input to yield a detected output (Le(i)) (block 520). Again, the index ‘i’ represents the iteration number, where ‘i’ indicates data derived from the most recent iteration, and ‘i-1’ indicates data derived from a preceding iteration. The data detection algorithm may be, but is not limited to, a Viterbi data detection algorithm or a maximum a posteriori data detection algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detection algorithms that may be used in relation to different embodiments of the present invention. The detected output (Le(i)) is stored to a prior iteration buffer circuit for later use as a prior iteration detected output (Le(i-1)) (block 522).

[0055] Alternatively, where a corresponding decoded output is available (block 515) it is accessed (block 525) and a data detection algorithm is applied to the processing data

input guided by the corresponding decoded output (La(i)) to yield a detected output (Le(i)) (block 530). Such a corresponding decoded output is available for the second or later global iterations (i.e., $i \geq 1$) for a given processing data input. The detected output (Le(i)) is stored to a prior iteration buffer circuit for later use as a prior iteration detected output (Le(i-1)) (block 532). A modified detected output (Le’) and a modified decoded output (La’) are calculated (block 533) based upon decoded output from both the most recent global iteration (La(i)) and from the preceding global iteration (La(i-1)), and detected output from both the most recent global iteration (Le(i)) and from the preceding global iteration (Le(i-1)) in accordance with the following equations:

$$La' = \text{ScalarA} * La(i-1) + La(i), \text{ and}$$

$$Le' = \text{ScalarB} * Le(i-1) + Le(i).$$

ScalarA and ScalarB may be any values between zero to negative 0.99. In one particular embodiment of the present invention, ScalarA is -0.5, and ScalarB is -0.5. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of scalar values that may be used for ScalarA and ScalarB in accordance with various embodiments of the present invention.

[0056] A short media defect detection is applied to the suspect symbol indicator to determine whether a media defect is likely, and if so to provide a media defect location set (block 538). Such a media defect location set indicates which data in the processing data set corresponds to the likely media defect. The short media defect detection may be any media defect detection process known in the art. In one particular embodiment of the present invention, the binary media defect detection processed may be done similar to that disclosed in U.S. Pat. No. 8,201,051 entitled “Method for Detecting Short Burst Errors in LDPC System”, issued Jun. 12, 2012 to Tan et al. The entirety of the aforementioned reference is incorporated herein by reference for all purposes.

[0057] Symbols of the detected output corresponding to the media defect location set are scaled to update the detected output (block 540). This scaling operates to modify soft data associated with the effected symbols to reduce the probability that the symbol is considered properly found. By doing this, the likelihood that an effected symbol negatively impacts processing of the data set is reduced and the likelihood that the symbol will be modified by later processing is increased. In addition, where a media defect is identified, the corresponding decoded output (La(i)) is disregarded from the central memory (block 540). This scaling operates to modify soft data associated with the effected symbols to reduce the probability that the symbol is considered properly found. By doing this, the likelihood that an effected symbol negatively impacts processing of the data set is reduced and the likelihood that the symbol will be modified by later processing is increased. A derivative of the detected output (Le(i)) is stored to the central memory (block 550). In some cases, the derivative of the detected output is an interleaved or shuffled version of the detected output.

[0058] Turning to FIG. 5b and following flow diagram 501, in parallel to the previously described data detection process, it is determined whether a data decoder circuit is available (block 506). The data decoder circuit may be, for example, a low density data decoder circuit as are known in the art. Where the data decoder circuit is available (block 506), a previously stored derivative of a detected output is accessed from the central memory and used as a received codeword

(block 511). A data decode algorithm is applied to the received codeword to yield a decoded output (block 516). It is then determined whether the decoded output converged (e.g., resulted in the originally written data as indicated by the lack of remaining unsatisfied checks) (block 521). Where the decoded output converged (block 521), the converged codeword is provided as a decoded output (block 526).

[0059] Alternatively, where the decoded output failed to converge (e.g., errors remain) (block 521), it is determined whether another local iteration is desired (block 531). In some cases, as a default seven local iterations are allowed per each global iteration. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize another default number of local iterations that may be used in relation to different embodiments of the present invention. Where another local iteration is desired (block 531), the data decode algorithm is re-applied using the current decoded output as a guide (block 516).

[0060] Alternatively, where another local iteration is not desired (block 531), it is determined whether another global iteration is allowed (block 536). As a default, another global iteration is allowed where there is sufficient available space in the central memory and an output memory reordering queue to allow another pass through processing the currently processing codeword. The amount of available space in the central memory and an output memory reordering queue is a function of how many iterations are being used by concurrently processing codewords to converge. For more detail on the output queue time limitation see, for example, U.S. patent application Ser. No. 12/114,462 entitled "Systems and Methods for Queue Based Data Detection and Decoding", and filed May 8, 2008 by Yang et al. The entirety of the aforementioned reference is incorporated herein by reference for all purposes. Thus, the amount of time that a codeword may continue processing through global iterations is a function of the availability of central memory and an output memory reordering queue. By limiting the number of global iterations that may be performed, the amount of time a codeword may continue processing through global iterations can be reduced.

[0061] Where another global iteration is allowed (block 536), the decoded output (La(i)) is stored to a prior iteration buffer circuit for later use as a prior iteration decoded output (La(i-1)) (block 539). In addition, a derivative of the decoded output is stored to the central memory (block 546). The derivative of the decoded output being stored to the central memory triggers the data set ready query of block 505 to begin the data detection process. Alternatively, where another global iteration is not allowed (block 536), a failure to converge is indicated (block 541), and the current decoded output is provided (block 526).

[0062] It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or only a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire

system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

[0063] In conclusion, the invention provides novel systems, devices, methods and arrangements for performing defect detection. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. For example, one or more embodiments of the present invention may be applied to various data storage systems and digital communication systems, such as, for example, tape recording systems, optical disk drives, wireless systems, and digital subscriber line systems. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A data processing system, the data processing system comprising:

a data detector circuit operable to apply a data detection algorithm to a detector input to yield a first detected output and a second detected output, wherein the first detected output is derived from a first iteration applying the data detection algorithm, and wherein the second detected output is derived from a second iteration applying the data detection algorithm;

a defect detection circuit including:

a multi-iteration data combining circuit operable to combine the first detected output with the second detected output to yield a modified detected output;

a media defect detector circuit operable to apply a media defect detection algorithm to at least the modified detected output to yield a defect indicator; and

a data decoder circuit operable to apply a data decode algorithm to a decoder input derived from the second detected output modified based on the defect indicator to yield a decoded output.

2. The data processing system of claim 1, wherein the decoder input is a first decoder input and the decoder output is a first decoder output, and wherein:

the data detector circuit is further operable to apply the data detection algorithm to the detector input to yield a third detected output, wherein the third detected output is derived from a third iteration applying the data detection algorithm;

the data decoder circuit is further operable to apply the data decode algorithm to a second decoder input derived from the third detected output modified based on the defect indicator to yield a second decoded output;

the multi-iteration data combining circuit is further operable to combine a first decoded output and the second decoded output to yield a modified decoded output; and

the media defect detector circuit is operable to apply the media defect detection algorithm to a combination of the modified detected output and the modified decoded output to yield the defect indicator.

3. The data processing system of claim 2, wherein the modified decoded output is calculated in accordance with the following equation:

$$\text{modified decoded output} = \text{scalar} * \text{first decoded output} + \text{second decoded output},$$

wherein the scalar is a negative value.

4. The data processing system of claim 3, wherein the scalar is programmable.

5. The data processing system of claim 1, wherein the defect detection circuit further comprises:

a memory operable to store the first detected output until the second detected output is available.

6. The data processing system of claim 1, wherein the modified detected output is calculated in accordance with the following equation:

$$\text{modified detected output} = \text{scalar} * \text{first detected output} + \text{second detected output},$$

wherein the scalar is a negative value.

7. The data processing system of claim 6, wherein the scalar is programmable.

8. The data processing system of claim 1, wherein the system further comprises a memory operable to pass a derivative of the first decoded output and a derivative of the second decoded output to the data detector circuit, and to pass a derivative of the first detected output and the derivative of the second detected output to the data decoder circuit, and wherein the media defect detector circuit is operable to disregard the second decoded output in the memory based at least in part upon assertion of the defect indicator.

9. The data processing system of claim 1, wherein modifying the first detected output includes multiplying the first detected output by a scalar.

10. The data processing system of claim 1, wherein the system is implemented as an integrated circuit.

11. The data processing system of claim 1, wherein the system is implemented as part of a storage device.

12. The data processing system of claim 1, wherein the data decoder circuit is a low density parity check decoder circuit.

13. The data processing system of claim 1, wherein the data detector circuit is selected from a group consisting of: a Viterbi algorithm data detector circuit, and a maximum a posteriori data detector circuit.

14. A method for data processing, the method comprising: receiving a first detected output and a second detected output, wherein the first detected output is derived from a first iteration applying a data detection algorithm by a data detector circuit to a detector input, and the second detected output is derived from a second iteration applying the data detection algorithm to the detector input; calculating a modified detected output based on the first detected output and the second detected output; determining a defect on a medium from which the detector input is derived based at least in part on the modified detected output to yield a defect indicator; applying a data decode algorithm by a data decoder circuit to a decoder input derived from the second detected output modified based on the defect indicator to yield a decoded output.

15. The method of claim 14, wherein the decoder input is a first decoder input and the decoder output is a first decoder output, and wherein the method further comprises:

applying the data detection algorithm to the detector input to yield a third detected output, wherein the third detected output is derived from a third iteration applying the data detection algorithm;

applying the data decode algorithm by the data decoder circuit to a second decoder input derived from the third detected output modified based on the defect indicator to yield a second decoded output

calculating a modified decoded output based on the first decoded output and the second decoded output; and wherein determining the defect on the medium is based upon the modified detected output and the modified decoded output to yield the defect indicator.

16. The method of claim 15, wherein the modified decoded output is calculated in accordance with the following equation:

$$\text{modified decoded output} = \text{scalar} * \text{first decoded output} + \text{second decoded output},$$

wherein the scalar is a negative value.

17. The method of claim 14, wherein the modified detected output is calculated in accordance with the following equation:

$$\text{modified detected output} = \text{scalar} * \text{first detected output} + \text{second detected output},$$

wherein the scalar is a negative value.

18. The method of claim 17, wherein the method further comprises: programming the scalar.

19. The method of claim 14, wherein the method further comprises:

storing the first detected output until the second detected output is available from the data detector circuit.

20. A storage device, the storage device comprising:

a storage medium; a read/write head assembly operable to sense information from the storage medium and to provide a corresponding continuous signal;

an analog to digital converter circuit operable to sample the continuous signal synchronous to a sampling clock to yield a set of digital samples;

an equalizer circuit operable to equalize the set of digital samples and to yield a detector input;

a data detector circuit operable to apply a data detection algorithm to the detector input to yield a first detected output and a second detected output, wherein the first detected output is derived from a first iteration applying the data detection algorithm, and wherein the second detected output is derived from a second iteration applying the data detection algorithm;

a defect detection circuit including: a multi-iteration data combining circuit operable to combine the first detected output with the second detected output to yield a modified detected output; a media defect detector circuit operable to apply a media defect detection algorithm to at least the modified detected output to yield a defect indicator; and

a data decoder circuit operable to apply a data decode algorithm to a decoder input derived from the second detected output modified based on the defect indicator to yield a decoded output.

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