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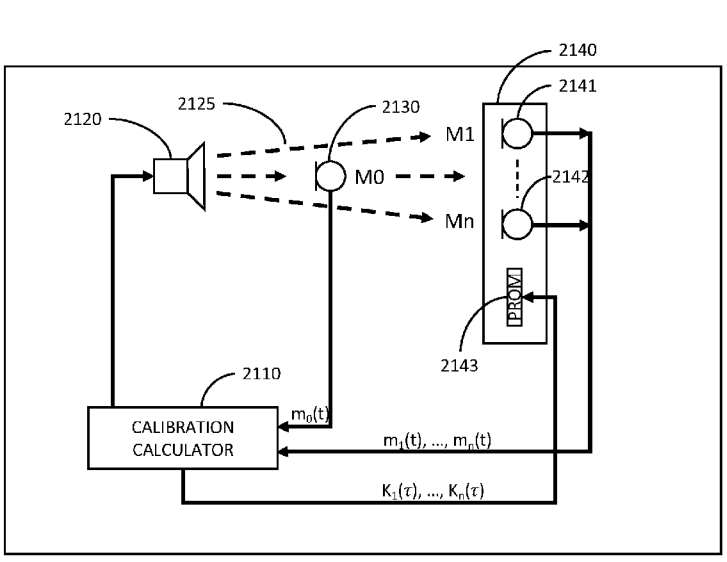

FIG. 14

(57) Abstract: Disclosed herein are systems and techniques for microphone array calibration, as well as communication systems in which calibrated microphones can be used. The systems and techniques disclosed herein may provide both phase and magnitude calibration for microphone arrays, resulting in improved performance for beamforming and other applications. Further, various systems and methods are disclosed herein for local storage of calibration coefficients in the microphone array (e.g., at the time of manufacture and calibration). Further, various systems and methods disclosed herein may include central application of the calibration of a microphone array (e.g., in an edge processor at operation time) to replace uncalibrated microphone signals with calibrated microphone signals further down in the signal chain.

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SYSTEMS AND TECHNIQUES FOR MICROPHONE ARRAY CALIBRATION

Cross-Reference to Related Applications

[0001] This application claims benefit of and priority to U.S. Provisional Application Serial No. 63/112,967, titled "Systems and Techniques for Microphone Array Calibration", which is hereby incorporated by reference in its entirety.

Field of the Disclosure

[0002] The present disclosure relates to systems and apparatuses in a daisy-chained network.

Background

[0003] As electronic components decrease in size, and as performance expectations increase, more components are included in previously un-instrumented or less-instrumented devices. In some settings, the communication infrastructure used to exchange signals between these components (e.g., in a vehicle) has required thick and heavy bundles of cables.

[0004] This disclosure is intended to provide an overview of subject matter of the present patent application. It is not intended to provide an exclusive or exhaustive explanation of the invention. Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with some aspects of the present invention as set forth in the remainder of the present application with reference to the drawings.

Summary of the Disclosure

[0005] Disclosed herein are systems and techniques for microphone array calibration, as well as communication systems in which calibrated microphones may be used. When an array of microphones is used for beamforming (e.g., for noise cancellation), production tolerances among the different microphones in the array can cause performance degradation of certain beamforming algorithms. Generally, once microphones are distributed and/or installed, no further calibration is possible. Systems and methods are disclosed for saving calibration coefficients on a microphone for application when the microphone is in use.

[0006] According to one aspect, a system for microphone array calibration comprises: a loudspeaker configured to play a test signal; a microphone array configured to receive the test signal and to generate a plurality of microphone array signals; a reference microphone positioned between the loudspeaker and the microphone array, wherein the reference microphone is configured to receive the test signal and to generate a reference signal; and a calibration calculator configured to process the plurality of microphone array signals and the reference signal, generate a set of filter coefficients, and transmit the set of filter coefficients to the microphone array.

[0007] According to some implementations, the system further comprises a memory associated with the microphone array configured to store the set of filter coefficients. In some implementations, the memory is positioned on a microphone array module with the microphone array. In some implementations, the memory is a cloud-based memory accessible by the microphone array. In some implementations, the memory is further configured to store microphone information, including at least one of vendor information, product information, version information, model information, capability information, serial number, make information, configuration information, routing information, and authentication information.

[0008] According to some implementations, the system further comprises a plurality of memory modules, wherein each of the plurality of memory modules is associated

with a respective microphone of the microphone array. In some implementations, the filter coefficients include phase calibration, frequency calibration, and magnitude calibration. In some implementations, the system further comprises a two-wire interface, wherein transmission of the filter coefficients to the microphone array occurs over the two-wire interface. In some implementations, each of the plurality of microphone array signals is unique and each respective microphone of the microphone array is associated with a respective subset of the set of filter coefficients.

[**0009**] According to another aspect, a method for microphone array calibration, comprises: playing a test signal at a loudspeaker; sampling the test signal at a microphone array; generating a plurality of microphone array signals at the microphone array; sampling the test signal at a reference microphone; generating a reference signal at the reference microphone; generating a set of filter coefficients based on the plurality of microphone array signals and the reference signal; and transmitting the set of filter coefficients to the microphone array.

[**0010**] According to some implementations, sampling the test signal at the microphone array comprises sampling the test signal at each respective microphone of the microphone array. In some implementations, generating a set of filter coefficients comprises generating a respective subset of filter coefficients for each respective microphone. According to some implementations, the method further comprises storing the respective subset of filter coefficients on each respective microphone. According to some implementations, the method further comprises storing the set of filter coefficients on the microphone array. In some implementations, transmitting the set of filter coefficients comprises transmitting the set of filter coefficients over a two-wire bus. According to some implementations, the method further comprises pre-calibrating the loudspeaker using the reference microphone.

[**0011**] According to another aspect, a self-calibrating microphone system comprises: a microphone module including: a microphone configured to receive an audio input signal and output a raw microphone output signal, wherein the microphone is pre-calibrated, and a non-volatile memory configured to store microphone

calibration coefficients for the microphone; a processor configured to receive the raw microphone signal and the microphone calibration coefficients, and generate a calibrated microphone signal; and a microphone signal sink configured to receive the calibrated microphone signal from the processor and output the calibrated microphone signal.

[**0012**] According to some implementations, the filter coefficients are configured to provide at least one of phase calibration, frequency calibration, and magnitude calibration. In some implementations, the system further comprises a two-wire bus wherein the processor and the microphone signal sink communicate over the two-wire bus. In some implementations, the processor is further configured to perform a convolution of the raw microphone signal and the microphone calibration coefficients to generate the calibrated microphone signal.

Brief Description of the Drawings

[**0013**] The present disclosure is best understood from the following detailed description in conjunction with the accompanying drawings. It is emphasized that, in accordance with the standard practice in the industry, various features are not necessarily drawn to scale, and are used for illustration purposes only. Where a scale is shown, explicitly or implicitly, it provides only one illustrative example. In other embodiments, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, not by way of limitation, in the figures of the accompanying drawings.

[**0014**] For a fuller understanding of the nature and advantages of the present invention, reference is made to the following detailed description of preferred embodiments and in connection with the accompanying drawings, in which:

[**0015**] FIG. 1 is a block diagram of an illustrative two-wire communication system, in accordance with various embodiments;

[**0016**] FIG. 2 is a block diagram of a node transceiver that may be included in a node of the system of FIG. 1, in accordance with various embodiments;

[**0017**] FIG. 3 is a diagram of a portion of a synchronization control frame used for communication in the system of FIG. 1, in accordance with various embodiments;

[**0018**] FIG. 4 is a diagram of a superframe used for communication in the system of FIG. 1, in accordance with various embodiments;

[**0019**] FIG. 5 illustrates example formats for a synchronization control frame in different modes of operation of the system of FIG. 1, in accordance with various embodiments;

[**0020**] FIG. 6 illustrates example formats for a synchronization response frame at different modes of operation of the system of FIG. 1, in accordance with various embodiments;

[**0021**] FIG. 7 is a block diagram of various components of the bus protocol circuitry of FIG. 2, in accordance with various embodiments;

[**0022**] FIGS. 8-11 illustrate examples of information exchange along a two-wire bus, in accordance with various embodiments of the bus protocols described herein;

[**0023**] FIG. 12 illustrates a ring topology for the two-wire bus and a unidirectional communication scheme thereon, in accordance with various embodiments;

[**0024**] FIG. 13 is a block diagram of a device that may serve as a node or host in the system of FIG. 1, in accordance with various embodiments;

[**0025**] FIG. 14 is a block diagram of a microphone array calibration system, in accordance with various embodiments;

[**0026**] FIGS. 15-17 are flow diagrams of methods for microphone array calibration, in accordance with various embodiments;

[**0027**] FIG. 18 is a block diagram of a microphone system in which the calibrations disclosed herein may be applied, in accordance with various embodiments;

[**0028**] FIG. 19 is a flow diagram of a method of applying a microphone array calibration, in accordance with various embodiments;

[**0029**] FIG. 20 is a block diagram of a two-wire communication system in which the microphone array calibrations disclosed herein may be applied, in accordance with various embodiments; and

[**0030**] FIGS. 21-22 are flow diagrams of methods of calibrating microphones and applying the microphone array calibrations, respectively, in accordance with various embodiments.

Detailed Description

[**0031**] Disclosed herein are systems and techniques for microphone array calibration, as well as communication systems in which calibrated microphones may be used. When an array of microphones is used for beamforming (e.g., as part of a road noise cancellation, other noise cancellation, or selective broadcast application), production tolerances among the different microphones in the array may cause performance degradation of certain beamforming algorithms. Some conventional calibration procedures attempt to address this degradation by generating filter coefficients for the microphones in order to equalize the differences in the magnitudes of the frequency responses of the microphones. However, conventional calibration procedures neglect to consider the impact of phase tolerances across the microphones in an array.

[**0032**] The systems and techniques disclosed herein may provide both phase and magnitude calibration for microphone arrays, resulting in improved performance for beamforming and other applications. Further, various systems and methods are

disclosed herein for local storage of calibration coefficients in the microphone array (e.g., at the time of manufacture and calibration). Further, various systems and methods disclosed herein may include central application of the calibration of a microphone array (e.g., in an edge processor at operation time) to replace uncalibrated microphone signals with calibrated microphone signals further down in the signal chain. Any of the microphone array calibration systems and methods disclosed herein may be implemented by the communication systems (e.g., the systems 100) disclosed herein.

[0033] In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments that may be practiced. It is to be understood that other embodiments may be utilized, and structural or logical changes may be made, without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0034] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

[0035] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C).

[0036] Various components may be referred to or illustrated herein in the singular (e.g., a "processor," a "peripheral device," etc.), but this is simply for ease of discussion,

and any element referred to in the singular may include multiple such elements in accordance with the teachings herein.

[**0037**] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. As used herein, the term "circuitry" may refer to, be part of, or include an application-specific integrated circuit (ASIC), an electronic circuit, and optical circuit, a processor (shared, dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware that provide the described functionality.

[**0038**] FIG. 1 is a block diagram of an illustrative half-duplex two-wire communication system 100, in accordance with various embodiments. The system 100 includes a host 110, a main node 102-1 and at least one sub node 102-2. In FIG. 1, three sub nodes (0, 1, and 2) are illustrated. The depiction of three sub nodes 102-2 in FIG. 1 is simply illustrative, and the system 100 may include one, two, or more sub nodes 102-2, as desired.

[**0039**] The main node 102-1 may communicate with the sub nodes 102-2 over a two-wire bus 106. The bus 106 may include different two-wire bus links between adjacent nodes along the bus 106 to connect the nodes along the bus 106 in a daisy-chain fashion. For example, as illustrated in FIG. 1, the bus 106 may include a link coupling the main node 102-1 to the sub node 0, a link coupling the sub node 0 to the sub node 1, and a link coupling the sub node 1 to the sub node 2. In some embodiments, the links of the bus 106 may each be formed of a single twisted-wire pair (e.g., an unshielded twisted pair). In some embodiments, the links of the bus 106 may each be formed of a coax cable (e.g., with the core providing the "positive" line and the shield providing the "negative" line, or vice versa). The two-wire bus links together provide a complete electrical path (e.g., a forward and a return current path) so that no additional ground or voltage source lines need be used.

[**0040**] The host 110 may include a processor that programs the main node 102-1, and acts as the originator and recipient of various payloads transmitted along the bus 106. In some embodiments, the host 110 may be or may include a microcontroller, for example. In particular, the host 110 may be the master of Inter-Integrated Circuit Sound (I2S) communications that happen along the bus 106. The host 110 may communicate with the main node 102-1 via an I2S/Time Division Multiplex (TDM) protocol, a Serial Peripheral Interface (SPI) protocol, and/or an Inter-Integrated Circuit (I2C) protocol. In some embodiments, the main node 102-1 may be a transceiver (e.g., the node transceiver 120 discussed below with reference to FIG. 2) located within a same housing as the host 110. The main node 102-1 may be programmable by the host 110 over the I2C bus for configuration and read-back, and may be configured to generate clock, synchronization, and framing for all of the sub nodes 102-2. In some embodiments, an extension of the I2C control bus between the host 110 and the main node 102-1 may be embedded in the data streams transmitted over the bus 106, allowing the host 110 direct access to registers and status information for the one or more sub nodes 102-2, as well as enabling I2C-to-I2C communication over distance to allow the host 110 to control the peripheral devices 108. In some embodiments, an extension of the SPI control bus between the host 110 and the main node 102-1 may be embedded in the data streams transmitted over the bus 106, allowing the host 110 direct access to registers and status information for the one or more sub nodes 102-2, as well as enabling SPI-to-SPI or SPI-to-I2C communication over distance to allow the host 110 to control the peripheral devices 108. In embodiments in which the system 100 is included in a vehicle, the host 110 and/or the main node 102-1 may be included in a headend of the vehicle.

[**0041**] The main node 102-1 may generate "downstream" signals (e.g., data signals, power signals, etc., transmitted away from the main node 102-1 along the bus 106) and receive "upstream" signals (e.g., transmitted toward the main node 102-1 along the bus 106). The main node 102-1 may provide a clock signal for synchronous data transmission over the bus 106. As used herein, "synchronous data" may include data streamed continuously (e.g., audio signals) with a fixed time interval

between two successive transmissions to/from the same node along the bus 106. In some embodiments, the clock signal provided by the main node 102-1 may be derived from an I2S input provided to the main node 102-1 by the host 110. A sub node 102-2 may be an addressable network connection point that represents a possible destination for data frames transmitted downstream on the bus 106 or upstream on the bus 106. A sub node 102-2 may also represent a possible source of downstream or upstream data frames. The system 100 may allow for control information and other data to be transmitted in both directions over the bus 106 from one node to the next. One or more of the sub nodes 102-2 may also be powered by signals transmitted over the bus 106.

[**0042**] In particular, each of the main node 102-1 and the sub nodes 102-2 may include a positive upstream terminal (denoted as "AP"), a negative upstream terminal (denoted as "AN"), a positive downstream terminal (denoted as "BP"), and a negative downstream terminal (denoted as "BN"). The positive and negative downstream terminals of a node may be coupled to the positive and negative upstream terminals of the adjacent downstream node, respectively. As shown in FIG. 1, the main node 102-1 may include positive and negative upstream terminals, but these terminals may not be used; in other embodiments, the main node 102-1 may not include positive and negative upstream terminals. The last sub node 102-2 along the bus 106 (the sub node 2 in FIG. 1) may include positive and negative downstream terminals, but these terminals may not be used; in other embodiments, the last sub node 102-2 along the bus may not include positive and negative downstream terminals.

[**0043**] As discussed in detail below, the main node 102-1 may periodically send a synchronization control frame downstream, optionally along with data intended for one or more of the sub nodes 102-2. For example, the main node 102-1 may transmit a synchronization control frame every 1024 bits (representing a superframe) at a frequency of 48 kHz, resulting in an effective bit rate on the bus 106 of 49.152 Mbps. Other rates may be supported, including, for example, 44.1 kHz. The synchronization control frame may allow the sub nodes 102-2 to identify the beginning of each

superframe and also, in combination with physical layer encoding/signaling, may allow each sub node 102-2 to derive its internal operational clock from the bus 106. The synchronization control frame may include a preamble for signaling the start of synchronization, as well as control fields that allow for various addressing modes (e.g., normal, broadcast, discovery), configuration information (e.g., writing to registers of the sub nodes 102-2), conveyance of I2C information, conveyance of SPI information, remote control of certain general-purpose input/output (GPIO) pins at the sub nodes 102-2, and other services. A portion of the synchronization control frame following the preamble and the payload data may be scrambled in order to reduce the likelihood that information in the synchronization control frame will be mistaken for a new preamble, and to flatten the spectrum of related electromagnetic emissions.

[**0044**] The synchronization control frame may get passed between sub node 102-2 (optionally along with other data, which may come from the main node 102-1 but additionally or alternatively may come from one or more upstream sub nodes 102-2 or from a sub node 102-2 itself) until it reaches the last sub node 102-2 (i.e., the sub node 2 in FIG. 1), which has been configured by the main node 102-1 as the last sub node 102-2 or has self-identified itself as the last sub node 102-2. Upon receiving the synchronization control frame, the last sub node 102-2 may transmit a synchronization response frame followed by any data that it is permitted to transmit (e.g., a 24-bit audio sample in a designated time slot). The synchronization response frame may be passed upstream between sub nodes 102-2 (optionally along with data from downstream sub nodes 102-2), and based on the synchronization response frame, each sub node 102-2 may be able to identify a time slot, if any, in which the sub node 102-2 is permitted to transmit.

[**0045**] In some embodiments, one or more of the sub nodes 102-2 in the system 100 may be coupled to and communicate with a peripheral device 108. For example, a sub node 102-2 may be configured to read data from and/or write data to the associated peripheral device 108 using I2S, pulse density modulation (PDM), TDM, SPI, and/or I2C protocols, as discussed below. Although the "peripheral

device 108" may be referred to in the singular herein, this is simply for ease of discussion, and a single sub node 102-2 may be coupled with zero, one, or more peripheral devices. Examples of peripheral devices that may be included in the peripheral device 108 may include a digital signal processor (DSP), a field programmable gate array (FPGA), an ASIC, an analog to digital converter (ADC), a digital to analog converter (DAC), a codec, a microphone, a microphone array, a speaker, an audio amplifier, a protocol analyzer, an accelerometer or other motion sensor, an environmental condition sensor (e.g., a temperature, humidity, and/or gas sensor), a wired or wireless communication transceiver, a display device (e.g., a touchscreen display), a user interface component (e.g., a button, a dial, or other control), a camera (e.g., a video camera), a memory device, or any other suitable device that transmits and/or receives data. A number of examples of different peripheral device configurations are discussed in detail herein.

[**0046**] In some embodiments, the peripheral device 108 may include any device configured for I2S communication; the peripheral device 108 may communicate with the associated sub node 102-2 via the I2S protocol. In some embodiments, the peripheral device 108 may include any device configured for I2C communication; the peripheral device 108 may communicate with the associated sub node 102-2 via the I2C protocol. In some embodiments, the peripheral device 108 may include any device configured for SPI communication; the peripheral device 108 may communicate with the associated sub node 102-2 via the SPI protocol. In some embodiments, a sub node 102-2 may not be coupled to any peripheral device 108.

[**0047**] A sub node 102-2 and its associated peripheral device 108 may be contained in separate housings and coupled through a wired or wireless communication connection or may be contained in a common housing. For example, a speaker connected as a peripheral device 108 may be packaged with the hardware for an associated sub node 102-2 (e.g., the node transceiver 120 discussed below with reference to FIG. 2), such that the hardware for the associated sub node 102-2 is

contained within a housing that includes other speaker components. The same may be true for any type of peripheral device 108.

[**0048**] As discussed above, the host 110 may communicate with and control the main node 102-1 using multi-channel I2S, SPI, and/or I2C communication protocols. For example, the host 110 may transmit data via I2S to a frame buffer (not illustrated) in the main node 102-1, and the main node 102-1 may read data from the frame buffer and transmit the data along the bus 106. Analogously, the main node 102-1 may store data received via the bus 106 in the frame buffer, and then may transmit the data to the host 110 via I2S.

[**0049**] Each sub node 102-2 may have internal control registers that may be configured by communications from the main node 102-1. A number of such registers are discussed in detail below. Each sub node 102-2 may receive downstream data and may retransmit the data further downstream. Each sub node 102-2 may receive and/or generate upstream data and/or retransmit data upstream and/or add data to and upstream transaction.

[**0050**] Communications along the bus 106 may occur in periodic superframes. Each superframe may begin with a downstream synchronization control frame; be divided into periods of downstream transmission (also called "downstream portions"), upstream transmission (also called "upstream portions"), and no transmission (where the bus 106 is not driven); and end just prior to transmission of another downstream synchronization control frame. The main node 102-1 may be programmed (by the host 110) with a number of downstream portions to transmit to one or more of the sub nodes 102-2 and a number of upstream portions to receive from one or more of the sub nodes 102-2. Each sub node 102-2 may be programmed (by the main node 102-1) with a number of downstream portions to retransmit down the bus 106, a number of downstream portions to consume, a number of upstream portions to retransmit up the bus 106, and a number of upstream portions in which the sub node 102-2 may transmit data received from the sub node 102-2 from the associated peripheral

device 108. Communication along the bus 106 is discussed in further detail below with reference to FIGS. 2-12.

[0051] Embodiments of the communication systems 100 disclosed herein are unique among conventional communication systems in that all sub nodes 102-2 may receive output data over the bus 106 within the same superframe (e.g., all sub nodes 102-2 may receive the same audio sample without sample delays between the nodes 102). In conventional communication systems, data is buffered and processed in each node before being passed downstream in the next frame to the next node. Consequently, in these conventional communication systems, the latency of data transmission depends on the number of nodes (with each node adding a delay of one audio sample). In the communication systems 100 disclosed herein, the bus 106 may only add one cycle of latency, no matter if the first or last sub node 102-2 receives the data. The same is true for upstream communication; data may be available at an upstream node 102 in the next superframe, no matter which sub node 102-2 provided the data.

[0052] Further, in embodiments of the communication systems 100 disclosed herein, downstream data (e.g., downstream audio data) may be put on the bus 106 by the main node 102-1 or by any of the sub nodes 102-2 that are upstream of the receiving sub node 102-2; similarly, upstream data (e.g., upstream audio data) may be put on the bus 106 by any of the sub nodes 102-2 that are downstream of the receiving node 102 (i.e., the main node 102-1 or a sub node 102-2). Such capability allows a sub node 102-2 to provide both upstream and downstream data at a specific time (e.g., a specific audio sample time). For audio data, this data can be received in the next audio sample at any downstream or upstream node 102 without further delays (besides minor processing delays that fall within the superframe boundary). As discussed further herein, control messages (e.g., in a synchronization control frame (SCF)) may travel to the last node 102 (addressing a specific node 102 or broadcast) and an upstream response (e.g., in a synchronization response frame (SRF)) may be created by the last downstream node 102 within the same superframe. Nodes 102 that have been addressed by the SCF change the content of the upstream

SRF with their own response. Consequently, within the same audio sample, a control and a response may be fully executed over multiple nodes 102. This is also in contrast to conventional communication systems, in which sample latencies would be incurred between nodes (for relaying messages from one node to the other).

[**0053**] Each of the main node 102-1 and the sub nodes 102-2 may include a transceiver to manage communication between components of the system 100. FIG. 2 is a block diagram of a node transceiver 120 that may be included in a node (e.g., the main node 102-1 or a sub node 102-2) of the system 100 of FIG. 1, in accordance with various embodiments. In some embodiments, a node transceiver 120 may be included in each of the nodes of the system 100, and a control signal may be provided to the node transceiver 120 via a main (MAIN) pin to indicate whether the node transceiver 120 is to act as a main node (e.g., when the MAIN pin is high) or a sub node (e.g., when the MAIN pin is low).

[**0054**] The node transceiver 120 may include an upstream differential signaling (DS) transceiver 122 and a downstream DS transceiver 124. The upstream DS transceiver 122 may be coupled to the positive and negative upstream terminals discussed above with reference to FIG. 1, and the downstream DS transceiver 124 may be coupled to the positive and negative downstream terminals discussed above with reference to FIG. 1. In some embodiments, the upstream DS transceiver 122 may be a low voltage DS (LVDS) transceiver, and the downstream DS transceiver 124 may be an LVDS transceiver. Each node in the system 100 may be AC-coupled to the bus 106, and data signals may be conveyed along the bus 106 (e.g., via the upstream DS transceiver 122 and/or the downstream DS transceiver 124) using a predetermined form of DS (e.g., LVDS or Multipoint LVDS (MLVDS) or similar signaling) with appropriate encoding to provide timing information over the bus 106 (e.g., differential Manchester coding, biphase mark coding, Manchester coding, Non-Return-to-Zero, Inverted (NRZI) coding with run-length limiting, or any other suitable encoding).

[**0055**] The upstream DS transceiver 122 and the downstream DS transceiver 124 may communicate with bus protocol circuitry 126, and the bus protocol circuitry 126

may communicate with a phased locked loop (PLL) 128 and voltage regulator circuitry 130, among other components. When the node transceiver 120 is powered up, the voltage regulator circuitry 130 may raise a "power good" signal that is used by the PLL 128 as a power-on reset.

[**0056**] As noted above, one or more of the sub nodes 102-2 in the system 100 may receive power transmitted over the bus 106 concurrently with data. For power distribution (which is optional, as some of the sub nodes 102-2 may be configured to have exclusively local power provided to them), the main node 102-1 may place a DC bias on the bus link between the main node 102-1 and the sub node 0 (e.g., by connecting, through a low-pass filter, one of the downstream terminals to a voltage source provided by a voltage regulator and the other downstream terminal to ground). The DC bias may be a predetermined voltage, such as 5 volts, 8 volts, the voltage of a car battery, or a higher voltage. Each successive sub node 102-2 can selectively tap its upstream bus link to recover power (e.g., using the voltage regulator circuitry 130). This power may be used to power the sub node 102-2 itself (and optionally one or more peripheral device 108 coupled to the sub node 102-2). A sub node 102-2 may also selectively bias the bus link downstream for the next-in-line sub node 102-2 with either the recovered power from the upstream bus link or from a local power supply. For example, the sub node 0 may use the DC bias on the upstream link of the bus 106 to recover power for the sub node 0 itself and/or for one or more associated peripheral device 108, and/or the sub node 0 may recover power from its upstream link of the bus 106 to bias its downstream link of the bus 106.

[**0057**] Thus, in some embodiments, each node in the system 100 may provide power to the following downstream node over a downstream bus link. The powering of nodes may be performed in a sequenced manner. For example, after discovering and configuring the sub node 0 via the bus 106, the main node 102-1 may instruct the sub node 0 to provide power to its downstream link of the bus 106 in order to provide power to the sub node 1; after the sub node 1 is discovered and configured, the main node 102-1 may instruct the sub node 1 to provide power to its downstream link of

the bus 106 in order to provide power to the sub node 2 (and so on for additional sub nodes 102-2 coupled to the bus 106). In some embodiments, one or more of the sub nodes 102-2 may be locally powered, instead of or in addition to being powered from its upstream bus link. In some such embodiments, the local power source for a given sub node 102-2 may be used to provide power to one or more downstream sub nodes.

[**0058**] In some embodiments, upstream bus interface circuitry 132 may be disposed between the upstream DS transceiver 122 and the voltage regulator circuitry 130, and downstream bus interface circuitry 131 may be disposed between the downstream DS transceiver 124 and the voltage regulator circuitry 130. Since each link of the bus 106 may carry AC (signal) and DC (power) components, the upstream bus interface circuitry 132 and the downstream bus interface circuitry 131 may separate the AC and DC components, providing the AC components to the upstream DS transceiver 122 and the downstream DS transceiver 124, and providing the DC components to the voltage regulator circuitry 130. AC couplings on the line side of the upstream DS transceiver 122 and downstream DS transceiver 124 substantially isolate the transceivers 122 and 124 from the DC component on the line to allow for high-speed bi-directional communications. As discussed above, the DC component may be tapped for power, and the upstream bus interface circuitry 132 and the downstream bus interface circuitry 131 may include a ferrite, a common mode choke, or an inductor, for example, to reduce the AC component provided to the voltage regulator circuitry 130. In some embodiments, the upstream bus interface circuitry 132 may be included in the upstream DS transceiver 122, and/or the downstream bus interface circuitry 131 may be included in the downstream DS transceiver 124; in other embodiments, the filtering circuitry may be external to the transceivers 122 and 124.

[**0059**] The node transceiver 120 may include a transceiver 127 for I2S, TDM, and PDM communication between the node transceiver 120 and an external device 155. Although the "external device 155" may be referred to in the singular herein, this is

simply for ease of illustration, and multiple external devices may communicate with the node transceiver 120 via the I2S/TDM/PDM transceiver 127. As known in the art, the I2S protocol is for carrying pulse code modulated (PCM) information (e.g., between audio chips on a printed circuit board (PCB)). As used herein, "I2S/TDM" may refer to an extension of the I2S stereo (2-channel) content to multiple channels using TDM. As known in the art, PDM may be used in sigma delta converters, and in particular, PDM format may represent an over-sampled 1-bit sigma delta ADC signal before decimation. PDM format is often used as the output format for digital microphones. The I2S/TDM/PDM transceiver 127 may be in communication with the bus protocol circuitry 126 and pins for communication with the external device 155. Six pins, BCLK, SYNC, DTX[1:0], and DRX[1:0], are illustrated in FIG. 2; the BCLK pin may be used for an I2S bit clock, the SYNC pin may be used for an I2S frame synchronization signal, and the DTX[1:0] and DRX[1:0] pins are used for transmit and receive data channels, respectively. Although two transmit pins (DTX[1:0]) and two receive pins (DRX[1:0]) are illustrated in FIG. 2, any desired number of receive and/or transmit pins may be used.

[**0060**] When the node transceiver 120 is included in the main node 102-1, the external device 155 may include the host 110, and the I2S/TDM/PDM transceiver 127 may provide an I2S slave (regarding BCLK and SYNC) that can receive data from the host 110 and send data to the host 110 synchronously with an I2S interface clock of the host 110. In particular, an I2S frame synchronization signal may be received at the SYNC pin as an input from the host 110, and the PLL 128 may use that signal to generate clocks. When the node transceiver 120 is included in a sub node 102-2, the external device 155 may include one or more peripheral devices 108, and the I2S/TDM/PDM transceiver 127 may provide an I2S clock master (for BCLK and SYNC) that can control I2S communication with the peripheral device 108. In particular, the I2S/TDM/PDM transceiver 127 may provide an I2S frame synchronization signal at the SYNC pin as an output. Registers in the node transceiver 120 may determine which and how many I2S/TDM channels are being transmitted as data slots over the bus 106. A TDM mode (TDMMODE) register in the

node transceiver 120 may store a value of how many TDM channels fit between consecutive SYNC pulses on a TDM transmit or receive pin. Together with knowledge of the channel size, the node transceiver 120 may automatically set the BCLK rate to match the number of bits within the sampling time (e.g., 48 kHz).

[**0061**] The node transceiver 120 may include a transceiver 129 for I2C communication between the node transceiver 120 and an external device 157. Although the "external device 157" may be referred to in the singular herein, this is simply for ease of illustration, and multiple external devices may communicate with the node transceiver 120 via the I2C transceiver 129. As known in the art, the I2C protocol uses clock (SCL) and data (SDA) lines to provide data transfer. The I2C transceiver 129 may be in communication with the bus protocol circuitry 126 and pins for communication with the external device 157. Four pins, ADR1, ADR2, SDA, and SCL are illustrated in FIG. 2; ADR1 and ADR2 may be used to modify the I2C addresses used by the node transceiver 120 when the node transceiver 120 acts as an I2C slave (e.g., when it is included in the main node 102-1), and SDA and SCL are used for the I2C serial data and serial clock signals, respectively. When the node transceiver 120 is included in the main node 102-1, the external device 157 may include the host 110, and the I2C transceiver 129 may provide an I2C slave that can receive programming instructions from the host 110. In particular, an I2C serial clock signal may be received at the SCL pin as an input from the host 110 for register accesses. When the node transceiver 120 is included in a sub node 102-2, the external device 157 may include a peripheral device 108 and the I2C transceiver 129 may provide an I2C master to allow the I2C transceiver to program one or more peripheral devices in accordance with instructions provided by the host 110 and transmitted to the node transceiver 120 via the bus 106. In particular, the I2C transceiver 129 may provide the I2C serial clock signal at the SCL pin as an output.

[**0062**] The node transceiver 120 may include a transceiver 136 for SPI communication between the node transceiver 120 and an external device 138.

Although the "external device 138" may be referred to in the singular herein, this is simply for ease of illustration, and multiple external devices may communicate with the node transceiver 120 via the SPI transceiver 136. As known in the art, the SPI protocol uses slave select (SS), clock (BCLK), master-out-slave-in (MOSI), and master-in-slave-out (MISO) data lines to provide data transfer, and pins corresponding to these four lines are illustrated in FIG. 2. The SPI transceiver 136 may be in communication with the bus protocol circuitry 126 and pins for communication with the external device 138. When the node transceiver 120 is included in the main node 102-1, the external device 138 may include the host 110 or another external device, and the SPI transceiver 136 may provide an SPI slave that can receive and respond to commands from the host 110 or other external device. When the node transceiver 120 is included in a sub node 102-2, the external device 138 may include a peripheral device 108 and the SPI transceiver 136 may provide an SPI host to allow the SPI transceiver 136 to send commands to one or more peripheral devices 108. The SPI transceiver 136 may include a read data first-in-first-out (FIFO) buffer and a write data FIFO buffer. The read data FIFO buffer may be used to collect data read from other nodes 102, and may be read by an external device 138 when the external device 138 transmits an appropriate read command. The write data FIFO buffer may be used to collect write data from the external device 138 before the write data is transmitted to another device.

[**0063**] The node transceiver 120 may include an interrupt request (IRQ) pin in communication with the bus protocol circuitry 126. When the node transceiver 120 is included in the main node 102-1, the bus protocol circuitry 126 may provide event-driven interrupt requests toward the host 110 via the IRQ pin. When the node transceiver 120 is included in a sub node 102-2 (e.g., when the MSTR pin is low), the IRQ pin may serve as a GPIO pin with interrupt request capability. The node transceiver 120 may include other pins in addition to those shown in FIG. 2 (e.g., as discussed below).

[**0064**] The system 100 may operate in any of a number of different operational modes. The nodes on the bus 106 may each have a register indicating which operational mode is currently enabled. Descriptions follow of examples of various operational modes that may be implemented. In a standby operational mode, bus activity is reduced to enable global power savings; the only traffic required is a minimal downstream preamble to keep the PLLs of each node (e.g., the PLL 128) synchronized. In standby operational mode, reads and writes across the bus 106 are not supported. In a discovery operational mode, the main node 102-1 may send predetermined signals out along the bus 106 and wait for suitable responses to map out the topology of sub nodes 102-2 distributed along the bus 106. In a normal operational mode, full register access may be available to and from the sub nodes 102-2 as well as access to and from peripheral devices 108 over the bus 106. Normal mode may be globally configured by the host 110 with or without synchronous upstream data and with or without synchronous downstream data.

[**0065**] FIG. 3 is a diagram of a portion of a synchronization control frame 180 used for communication in the system 100, in accordance with various embodiments. In particular, the synchronization control frame 180 may be used for data clock recovery and PLL synchronization, as discussed below. As noted above, because communications over the bus 106 may occur in both directions, communications may be time-multiplexed into downstream portions and upstream portions. In a downstream portion, a synchronization control frame and downstream data may be transmitted from the main node 102-1, while in an upstream portion, a synchronization response frame, and upstream data may be transmitted to the main node 102-1 from each of the sub nodes 102-2. The synchronization control frame 180 may include a preamble 182 and control data 184. Each sub node 102-2 may be configured to use the preamble 182 of the received synchronization control frame 180 as a time base for feeding the PLL 128. To facilitate this, a preamble 182 does not follow the "rules" of valid control data 184, and thus can be readily distinguished from the control data 184.

[**0066**] For example, in some embodiments, communication along the bus 106 may be encoded using a clock first, transition on zero differential Manchester coding scheme. According to such an encoding scheme, each bit time begins with a clock transition. If the data value is zero, the encoded signal transitions again in the middle of the bit time. If the data value is one, the encoded signal does not transition again. The preamble 182 illustrated in FIG. 5 may violate the encoding protocol (e.g., by having clock transitions that do not occur at the beginning of bit times 5, 7, and 8), which means that the preamble 182 may not match any legal (e.g., correctly encoded) pattern for the control data 184. In addition, the preamble 182 cannot be reproduced by taking a legal pattern for the control data 184 and forcing the bus 106 high or low for a single bit time or for a multiple bit time period. The preamble 182 illustrated in FIG. 5 is simply illustrative, and the synchronization control frame 180 may include different preambles 182 that may violate the encoding used by the control data 184 in any suitable manner.

[**0067**] The bus protocol circuitry 126 may include differential Manchester decoder circuitry that runs on a clock recovered from the bus 106 and that detects the synchronization control frame 180 to send a frame sync indicator to the PLL 128. In this manner, the synchronization control frame 180 may be detected without using a system clock or a higher-speed oversampling clock. Consequently, the sub nodes 102-2 can receive a PLL synchronization signal from the bus 106 without requiring a crystal clock source at the sub nodes 102-2.

[**0068**] As noted above, communications along the bus 106 may occur in periodic superframes. FIG. 4 is a diagram of a superframe 190, in accordance with various embodiments. As shown in FIG. 6, a superframe may begin with a synchronization control frame 180. When the synchronization control frame 180 is used as a timing source for the PLL 128, the frequency at which superframes are communicated ("the superframe frequency") may be the same as the synchronization signal frequency. In some embodiments in which audio data is transmitted along the bus 106, the superframe frequency may be the same as the audio sampling frequency used in the

system 100 (e.g., either 48 kHz or 44.1 kHz), but any suitable superframe frequency may be used. Each superframe 190 may be divided into periods of downstream transmission 192, periods of upstream transmission 194, and periods of no transmission 196 (e.g., when the bus 106 is not driven).

[**0069**] In FIG. 4, the superframe 190 is shown with an initial period of downstream transmission 192 and a later period of upstream transmission 194. The period of downstream transmission 192 may include a synchronization control frame 180 and X downstream data slots 198, where X can be zero. Substantially all signals on the bus 106 may be line-coded and a synchronization signal forwarded downstream from the main node 102-1 to the last sub node 102-2 (e.g., the sub node 102-2C) in the form of the synchronization preamble 182 in the synchronization control frame 180, as discussed above. Downstream, TDM, synchronous data may be included in the X downstream data slots 198 after the synchronization control frame 180. The downstream data slots 198 may have equal width. As discussed above, the PLL 128 may provide the clock that a node uses to time communications over the bus 106. In some embodiments in which the bus 106 is used to transmit audio data, the PLL 128 may operate at a multiple of the audio sampling frequency (e.g., 1024 times the audio sampling frequency, resulting in 1024-bit clocks in each superframe).

[**0070**] The period of upstream transmission 194 may include a synchronization response frame 197 and Y upstream data slots 199, where Y can be zero. In some embodiments, each sub node 102-2 may consume a portion of the downstream data slots 198. The last sub node (e.g., sub node 2 in FIG. 1) may respond (after a predetermined response time stored in a register of the last sub node) with a synchronization response frame 197. Upstream, TDM, synchronous data may be added by each sub node 102-2 in the upstream data slots 199 directly after the synchronization response frame 197. The upstream data slots 199 may have equal width. A sub node 102-2 that is not the last sub node (e.g., the sub nodes 0 and 1 in FIG. 1) may replace the received synchronization response frame 197 with its own upstream response if a read of one of its registers was requested in the synchronization

control frame 180 of the superframe 190 or if a remote I2C read was requested in the synchronization control frame 180 of the superframe 190.

[**0071**] As discussed above, the synchronization control frame 180 may begin each downstream transmission. In some embodiments, the synchronization control frame 180 may be 64 bits in length, but any other suitable length may be used. The synchronization control frame 180 may begin with the preamble 182, as noted above. In some embodiments, when the synchronization control frame 180 is retransmitted by a sub node 102-2 to a downstream sub node 102-2, the preamble 182 may be generated by the transmitting sub node 102-2, rather than being retransmitted.

[**0072**] The control data 184 of the synchronization control frame 180 may include fields that contain data used to control transactions over the bus 106. Examples of these fields are discussed below, and some embodiments are illustrated in FIG. 5. In particular, FIG. 5 illustrates example formats for the synchronization control frame 180 in normal mode, I2C mode, and discovery mode, in accordance with various embodiments. In some embodiments, a different preamble 182 or synchronization control frame 180 entirely may be used in standby mode so that the sub nodes 102-2 do not need to receive all of the synchronization control frame 180 until a transition to normal mode is sent.

[**0073**] In some embodiments, the synchronization control frame 180 may include a count (CNT) field. The CNT field may have any suitable length (e.g., 2 bits) and may be incremented (modulo the length of the field) from the value used in the previous superframe. A sub node 102-2 that receives a CNT value that is unexpected may be programmed to return an interrupt.

[**0074**] In some embodiments, the synchronization control frame 180 may include a node addressing mode (NAM) field. The NAM field may have any suitable length (e.g., 2 bits) and may be used to control access to registers of a sub node 102-2 over the bus 106. In normal mode, registers of a sub node 102-2 may be read from and/or written to based on the ID of the sub node 102-2 and the address of the register.

Broadcast transactions are writes which should be taken by every sub node 102-2. In some embodiments, the NAM field may provide for four node addressing modes, including "none" (e.g., data not addressed to any particular sub node 102-2), "normal" (e.g., data unicast to a specific sub node 102-2 specified in the address field discussed below), "broadcast" (e.g., addressed to all sub nodes 102-2), and "discovery."

[**0075**] In some embodiments, the synchronization control frame 180 may include an I2C field. The I2C field may have any suitable length (e.g., 1 bit) and may be used to indicate that the period of downstream transmission 192 includes an I2C transaction. The I2C field may indicate that the host 110 has provided instructions to remotely access a peripheral device 108 that acts as an I2C slave with respect to an associated sub node 102-2.

[**0076**] In some embodiments, the synchronization control frame 180 may include a node field. The node field may have any suitable length (e.g., 4 bits) and may be used to indicate which sub node is being addressed for normal and I2C accesses. In discovery mode, this field may be used to program an identifier for a newly discovered sub node 102-2 in a node ID register of the sub node 102-2. Each sub node 102-2 in the system 100 may be assigned a unique ID when the sub node 102-2 is discovered by the main node 102-1, as discussed below. In some embodiments, the main node 102-1 does not have a node ID, while in other embodiments, the main node 102-1 may have a node ID. In some embodiments, the sub node 102-2 attached to the main node 102-1 on the bus 106 (e.g., the sub node 0 in FIG. 1) will be sub node 0, and each successive sub node 102-2 will have a number that is 1 higher than the previous sub node. However, this is simply illustrative, and any suitable sub node identification system may be used.

[**0077**] In some embodiments, the synchronization control frame 180 may include a read/write (RW) field. The RW field may have any suitable length (e.g., 1 bit) and may be used to control whether normal accesses are reads (e.g., RW==1) or writes (e.g., RW==0).

[**0078**] In some embodiments, the synchronization control frame 180 may include an address field. The address field may have any suitable length (e.g., 8 bits) and may be used to address specific registers of a sub node 102-2 through the bus 106. For I2C transactions, the address field may be replaced with I2C control values, such as START/STOP, WAIT, RW, and DATA VLD. For discovery transactions, the address field may have a predetermined value (e.g., as illustrated in FIG. 5).

[**0079**] In some embodiments, the synchronization control frame 180 may include a data field. The data field may have any suitable length (e.g., 8 bits) and may be used for normal, I2C, and broadcast writes. The RESPCYCS value, multiplied by 4, may be used to determine how many cycles a newly discovered node should allow to elapse between the start of the synchronization control frame 180 being received and the start of the synchronization response frame 197 being transmitted. When the NAM field indicates discovery mode, the node address and data fields discussed below may be encoded as a RESPCYCS value that, when multiplied by a suitable optional multiplier (e.g., 4), indicates the time, in bits, from the end of the synchronization control frame 180 to the start of the synchronization response frame 197. This allows a newly discovered sub node 102-2 to determine the appropriate time slot for upstream transmission.

[**0080**] In some embodiments, the synchronization control frame 180 may include a cyclic redundancy check (CRC) field. The CRC field may have any suitable length (e.g., 16 bits) and may be used to transmit a CRC value for the control data 184 of the synchronization control frame 180 following the preamble 182. In some embodiments, the CRC may be calculated in accordance with the CCITT-CRC error detection scheme.

[**0081**] In some embodiments, at least a portion of the synchronization control frame 180 between the preamble 182 and the CRC field may be scrambled in order to reduce the likelihood that a sequence of bits in this interval will periodically match the preamble 182 (and thus may be misinterpreted by the sub node 102-2 as the start of a new superframe 190), as well as to reduce electromagnetic emissions as noted

above. In some such embodiments, the CNT field of the synchronization control frame 180 may be used by scrambling logic to ensure that the scrambled fields are scrambled differently from one superframe to the next. Various embodiments of the system 100 described herein may omit scrambling.

[**0082**] Other techniques may be used to ensure that the preamble 182 can be uniquely identified by the sub nodes 102-2 or to reduce the likelihood that the preamble 182 shows up elsewhere in the synchronization control frame 180, in addition to or in lieu of techniques such as scrambling and/or error encoding as discussed above. For example, a longer synchronization sequence may be used so as to reduce the likelihood that a particular encoding of the remainder of the synchronization control frame 180 will match it. Additionally or alternatively, the remainder of the synchronization control frame may be structured so that the synchronization sequence cannot occur, such as by placing fixed "0" or "1" values at appropriate bits.

[**0083**] The main node 102-1 may send read and write requests to the sub nodes 102-2, including both requests specific to communication on the bus 106 and I2C requests. For example, the main node 102-1 may send read and write requests (indicated using the RW field) to one or more designated sub nodes 102-2 (using the NAM and node fields) and can indicate whether the request is a request for the sub node 102-2 specific to the bus 106, an I2C request for the sub node 102-2, or an I2C request to be passed along to an I2C-compatible peripheral device 108 coupled to the sub node 102-2 at one or more I2C ports of the sub node 102-2.

[**0084**] Turning to upstream communication, the synchronization response frame 197 may begin each upstream transmission. In some embodiments, the synchronization response frame 197 may be 64 bits in length, but any other suitable length may be used. The synchronization response frame 197 may also include a preamble, as discussed above with reference to the preamble 182 of the synchronization control frame 180, followed by data portion. At the end of a downstream transmission, the last sub node 102-2 on the bus 106 may wait until the

RESPCYCS counter has expired and then begin transmitting a synchronization response frame 197 upstream. If an upstream sub node 102-2 has been targeted by a normal read or write transaction, a sub node 102-2 may generate its own synchronization response frame 197 and replace the one received from downstream. If any sub node 102-2 does not see a synchronization response frame 197 from a downstream sub node 102-2 at the expected time, the sub node 102-2 will generate its own synchronization response frame 197 and begin transmitting it upstream.

[**0085**] The data portion of the synchronization response frame 197 may include fields that contain data used to communicate response information back to the main node 102-1. Examples of these fields are discussed below, and some embodiments are illustrated in FIG. 6. In particular, FIG. 6 illustrates example formats for the synchronization response frame 197 in normal mode, I2C mode, and discovery mode, in accordance with various embodiments.

[**0086**] In some embodiments, the synchronization response frame 197 may include a count (CNT) field. The CNT field may have any suitable length (e.g., 2 bits) and may be used to transmit the value of the CNT field in the previously received synchronization control frame 180.

[**0087**] In some embodiments, the synchronization response frame 197 may include an acknowledge (ACK) field. The ACK field may have any suitable length (e.g., 2 bits), and may be inserted by a sub node 102-2 to acknowledge a command received in the previous synchronization control frame 180 when that sub node 102-2 generates the synchronization response frame 197. Example indicators that may be communicated in the ACK field include wait, acknowledge, not acknowledge (NACK), and retry. In some embodiments, the ACK field may be sized to transmit an acknowledgment by a sub node 102-2 that it has received and processed a broadcast message (e.g., by transmitting a broadcast acknowledgment to the main node 102-1). In some such embodiments, a sub node 102-2 also may indicate whether the sub node 102-2 has data to transmit (which could be used, for example, for demand-based upstream transmissions, such as non-TDM inputs from a keypad or touchscreen,

or for prioritized upstream transmission, such as when the sub node 102-2 wishes to report an error or emergency condition).

[0088] In some embodiments, the synchronization response frame 197 may include an I2C field. The I2C field may have any suitable length (e.g., 1 bit) and may be used to transmit the value of the I2C field in the previously received synchronization control frame 180.

[0089] In some embodiments, the synchronization response frame 197 may include a node field. The node field may have any suitable length (e.g., 4 bits) and may be used to transmit the ID of the sub node 102-2 that generates the synchronization response frame 197.

[0090] In some embodiments, the synchronization response frame 197 may include a data field. The data field may have any suitable length (e.g., 8 bits), and its value may depend on the type of transaction and the ACK response of the sub node 102-2 that generates the synchronization response frame 197. For discovery transactions, the data field may include the value of the RESPCYCS field in the previously received synchronization control frame 180. When the ACK field indicates a NACK, or when the synchronization response frame 197 is responding to a broadcast transaction, the data field may include a broadcast acknowledge (BA) indicator (in which the last sub node 102-2 may indicate if the broadcast write was received without error), a discovery error (DER) indicator (indicating whether a newly discovered sub node 102-2 in a discovery transaction matches an existing sub node 102-2), and a CRC error (CER) indicator (indicating whether a NACK was caused by a CRC error).

[0091] In some embodiments, the synchronization response frame 197 may include a CRC field. The CRC field may have any suitable length (e.g., 16 bits) and may be used to transmit a CRC value for the portion of the synchronization response frame 197 between the preamble and the CRC field.

[0092] In some embodiments, the synchronization response frame 197 may include an interrupt request (IRQ) field. The IRQ field may have any suitable length (e.g., 1

bit) and may be used to indicate that an interrupt has been signaled from a sub node 102-2.

[0093] In some embodiments, the synchronization response frame 197 may include an IRQ node (IRQNODE) field. The IRQNODE field may have any suitable length (e.g., 4 bits) and may be used to transmit the ID of the sub node 102-2 that has signaled the interrupt presented by the IRQ field. In some embodiments, the sub node 102-2 for generating the IRQ field will insert its own ID into the IRQNODE field.

[0094] In some embodiments, the synchronization response frame 197 may include a second CRC (CRC-4) field. The CRC-4 field may have any suitable length (e.g., 4 bits) and may be used to transmit a CRC value for the IRQ and IRQNODE fields.

[0095] In some embodiments, the synchronization response frame 197 may include an IRQ field, an IRQNODE field, and a CRC-4 field as the last bits of the synchronization response frame 197 (e.g., the last 10 bits). As discussed above, these interrupt-related fields may have their own CRC protection in the form of CRC-4 (and thus not protected by the preceding CRC field). Any sub node 102-2 that needs to signal an interrupt to the main node 102-1 will insert its interrupt information into these fields. In some embodiments, a sub node 102-2 with an interrupt pending may have higher priority than any sub node 102-2 further downstream that also has an interrupt pending. The last sub node 102-2 along the bus 106 (e.g., the sub node 2 in FIG. 1) may always populate these interrupt fields. If the last sub node 102-2 has no interrupt pending, the last sub node 102-2 may set the IRQ bit to 0, the IRQNODE field to its node ID, and provide the correct CRC-4 value. For convenience, a synchronization response frame 197 that conveys an interrupt may be referred to herein as an "interrupt frame."

[0096] In some embodiments, at least a portion of the synchronization response frame 197 between the preamble 182 and the CRC field may be scrambled in order to reduce emissions. In some such embodiments, the CNT field of the synchronization response frame 197 may be used by scrambling logic to ensure that the scrambled

fields are scrambled differently from one superframe to the next. Various embodiments of the system 100 described herein may omit scrambling.

[**0097**] Other techniques may be used to ensure that the preamble 182 can be uniquely identified by the sub nodes 102-2 or to reduce the likelihood that the preamble 182 shows up elsewhere in the synchronization response frame 197, in addition to or in lieu of techniques such as scrambling and/or error encoding as discussed above. For example, a longer synchronization sequence may be used so as to reduce the likelihood that a particular encoding of the remainder of the synchronization response frame 197 will match it. Additionally or alternatively, the remainder of the synchronization response frame may be structured so that the synchronization sequence cannot occur, such as by placing fixed "0" or "1" values at appropriate bits.

[**0098**] FIG. 7 is a block diagram of the bus protocol circuitry 126 of FIG. 2, in accordance with various embodiments. The bus protocol circuitry 126 may include control circuitry 154 to control the operation of the node transceiver 120 in accordance with the protocol for the bus 106 described herein. In particular, the control circuitry 154 may control the generation of synchronization frames for transmission (e.g., synchronization control frames or synchronization response frames, as discussed above), the processing of received synchronization frames, and the performance of control operations specified in received synchronization control frames. The control circuitry 154 may include programmable registers, as discussed below. The control circuitry 154 may create and receive synchronization control frames, react appropriately to received messages (e.g., associated with a synchronization control frame when the bus protocol circuitry 126 is included in a sub node 102-2 or from an I2C device when the bus protocol circuitry 126 is included in a main node 102-1), and adjust the framing to the different operational modes (e.g., normal, discovery, standby, etc.).

[**0099**] When the node transceiver 120 is preparing data for transmission along the bus 106, preamble circuitry 156 may be configured to generate preambles for

synchronization frames for transmission, and to receive preambles from received synchronization frames. In some embodiments, a downstream synchronization control frame preamble may be sent by the main node 102-1 every 1024 bits. As discussed above, one or more sub nodes 102-2 may synchronize to the downstream synchronization control frame preamble and generate local, phase-aligned main clocks from the preamble.

[**0100**] CRC insert circuitry 158 may be configured to generate one or more CRCs for synchronization frames for transmission. Frame/compress circuitry 160 may be configured to take incoming data from the I2S/TDM/PDM transceiver 127 (e.g., from a frame buffer associated with the transceiver 127), the I2C transceiver 129, and/or the SPI transceiver 136, optionally compress the data, and optionally generate parity check bits or error correction codes (ECC) for the data. A multiplexer (MUX) 162 may multiplex a preamble from the preamble circuitry 156, synchronization frames, and data into a stream for transmission. In some embodiments, the transmit stream may be scrambled by scrambling circuitry 164 before transmission.

[**0101**] For example, in some embodiments, the frame/compress circuitry 160 may apply a floating point compression scheme. In such an embodiment, the control circuitry 154 may transmit 3 bits to indicate how many repeated sign bits are in the number, followed by a sign bit and N-4 bits of data, where N is the size of the data to be transmitted over the bus 106. The use of data compression may be configured by the main node 102-1 when desired.

[**0102**] In some embodiments, the receive stream entering the node transceiver 120 may be descrambled by the descrambling circuitry 166. A demultiplexer (DEMUX) 168 may demultiplex the preamble, synchronization frames, and data from the receive stream. CRC check circuitry 159 on the receive side may check received synchronization frames for the correct CRC. When the CRC check circuitry 159 identifies a CRC failure in an incoming synchronization control frame 180, the control circuitry 154 may be notified of the failure and will not perform any control commands in the control data 184 of the synchronization control frame 180. When the CRC check

circuitry 159 identifies a CRC failure in an incoming synchronization response frame 197, the control circuitry 154 may be notified of the failure and may generate an interrupt for transmission to the host 110 in an interrupt frame. Deframe/decompress circuitry 170 may accept receive data, optionally check its parity, optionally perform error detection and correction (e.g., single error correction – double error detection (SECDED)), optionally decompress the data, and may write the receive data to the I2S/TDM/PDM transceiver 127 (e.g., a frame buffer associated with the transceiver 127), the I2C transceiver 129, and/or the SPI transceiver 136.

[**0103**] As discussed above, upstream and downstream data may be transmitted along the bus 106 in TDM data slots within a superframe 190. The control circuitry 154 may include registers dedicated to managing these data slots on the bus 106, a number of examples of which are discussed below. When the control circuitry 154 is included in a main node 102-1, the values in these registers may be programmed into the control circuitry 154 by the host 110. When the control circuitry 154 is included in a sub node 102-2, the values in these registers may be programmed into the control circuitry 154 by the main node 102-1.

[**0104**] In some embodiments, the control circuitry 154 may include a downstream slots (DNSLOTS) register. When the node transceiver 120 is included in the main node 102-1, this register may hold the value of the total number of downstream data slots. This register may also define the number of data slots that will be used for combined I2S/TDM/PDM receive by the I2S/TDM/PDM transceiver 127 in the main node 102-1. In a sub node 102-2, this register may define the number of data slots that are passed downstream to the next sub node 102-2 before or after the addition of locally generated downstream slots, as discussed in further detail below with reference to LDNSLOTS.

[**0105**] In some embodiments, the control circuitry 154 may include a local downstream slots (LDNSLOTS) register. This register may be unused in the main node 102-1. In a sub node 102-2, this register may define the number of data slots

that the sub node 102-2 will use and not retransmit. Alternatively, this register may define the number of slots that the sub node 102-2 may contribute to the downstream link of the bus 106.

[**0106**] In some embodiments, the control circuitry 154 may include an upstream slots (UPSLOTS) register. In the main node 102-1, this register may hold the value of the total number of upstream data slots. This register may also define the number of slots that will be used for I2S/TDM transmit by the I2S/TDM/PDM transceiver 127 in the main node 102-1. In a sub node 102-2, this register may define the number of data slots that are passed upstream before the sub node 102-2 begins to add its own data.

[**0107**] In some embodiments, the control circuitry 154 may include a local upstream slots (LUPSLOTS) register. This register may be unused in the main node 102-1. In a sub node 102-2, this register may define the number of data slots that the sub node 102-2 will add to the data received from downstream before it is sent upstream. This register may also define the number of data slots that will be used for combined I2S/TDM/PDM receive by the I2S/TDM/PDM transceiver 127 in the sub node 102-2.

[**0108**] In some embodiments, the control circuitry 154 may include a broadcast downstream slots (BCDNSLOTS) register. This register may be unused in the main node 102-1. In a sub node 102-2, this register may define the number of broadcast data slots. In some embodiments, broadcast data slots may always come at the beginning of the data field. The data in the broadcast data slots may be used by multiple sub nodes 102-2 and may be passed downstream by all sub nodes 102-2 whether or not they are used.

[**0109**] In some embodiments, the control circuitry 154 may include a slot format (SLOTFMT) register. This register may define the format of data for upstream and downstream transmissions. The data size for the I2S/TDM/PDM transceiver 127 may also be determined by this register. In some embodiments, valid data sizes include 8, 12, 16, 20, 24, 28, and 32 bits. This register may also include bits to

enable floating point compression for downstream and upstream traffic. When floating point compression is enabled, the I2S/TDM data size may be 4 bits larger than the data size over the bus 106. All nodes in the system 100 may have the same values for SLOTFMT when data slots are enabled, and the nodes may be programmed by a broadcast write so that all nodes will be updated with the same value.

[**0110**] FIGS. 8-11 illustrate examples of information exchange along the bus 106, in accordance with various embodiments of the bus protocols described herein. In particular, FIGS. 8-11 illustrate embodiments in which each sub node 102-2 is coupled to one or more speakers and/or one or more microphones as the peripheral device 108. This is simply illustrative, as any desired arrangement of peripheral device 108 may be coupled to any particular sub node 102-2 in accordance with the techniques described herein.

[**0111**] To begin, FIG. 8 illustrates signaling and timing considerations for bi-directional communication on the bus 106, in accordance with various embodiments. The sub nodes 102-2 depicted in FIG. 8 have various numbers of sensor/actuator elements, and so different amounts of data may be sent to, or received from, the various sub nodes 102-2. Specifically, sub node 1 has two elements, sub node 4 has four elements, and sub node 5 has three elements, so the data transmitted by the main node 102-1 includes two time slots for sub node 1, four time slots for sub node 4, and three time slots for sub node 5. Similarly, sub node 0 has three elements, sub node 2 has three elements, sub node 3 has three elements, sub node 6 has one element, and sub node 7 has four elements, so the data transmitted upstream by those sub nodes 102-2 includes the corresponding number of time slots. It should be noted that there need not have to be a one-to-one correlation between elements and time slots. For example, a microphone array, included in the peripheral device 108, having three microphones may include a DSP that combines signals from the three microphones (and possibly also information received from the main node 102-1 or from other sub nodes 102-2) to produce a single data sample, which, depending on the type of processing, could correspond to a single time slot or multiple time slots.

[0112] In FIG. 8, the main node 102-1 transmits an SCF followed by data for speakers coupled to specific sub nodes 102-2 (SD). Each successive sub node 102-2 forwards the SCF and also forwards at least any data destined for downstream sub nodes 102-2. A particular sub node 102-2 may forward all data or may remove data destined for that sub node 102-2. When the last sub node 102-2 receives the SCF, that sub node 102-2 transmits the SRF optionally followed by any data that the sub node 102-2 is permitted to transmit. Each successive sub node 102-2 forwards the SRF along with any data from downstream sub nodes 102-2 and optionally inserts data from one or more microphones coupled to the particular sub nodes 102-2 (MD). In the example of FIG. 8, the main node 102-1 sends data to sub nodes 1, 4, and 5 (depicted in FIG. 8 as active speakers) and receives data from sub nodes 7, 6, 3, 2, and 0 (depicted in FIG. 8 as microphone arrays).

[0113] FIG. 9 schematically illustrates the dynamic removal of data from a downstream transmission and insertion of data into an upstream transmission, from the perspective of the downstream DS transceiver 124, in accordance with various embodiments. In FIG. 9, as in FIG. 8, the main node 102-1 transmits a SCF followed by data for sub nodes 1, 4, and 5 (SD) in reverse order (e.g., data for sub node 5 is followed by data for sub node 4, which is followed by data for sub node 1, etc.) (see the row labeled MAIN). When sub node 1 receives this transmission, sub node 1 removes its own data and forwards to sub node 2 only the SCF followed by the data for sub nodes 5 and 4. Sub nodes 2 and 3 forward the data unchanged (see the row labeled SUB 2), such that the data forwarded by sub node 1 is received by sub node 4 (see the row labeled SUB 3). Sub node 4 removes its own data and forwards to sub node 5 only the SCF followed by the data for sub node 5, and, similarly, sub node 5 removes its own data and forwards to sub node 6 only the SCF. Sub node 6 forwards the SCF to sub node 7 (see the row labeled SUB 6).

[0114] At this point, sub node 7 transmits to sub node 6 the SRF followed by its data (see the row labeled SUB 6). Sub node 6 forwards to sub node 5 the SRF along with the data from sub node 7 and its own data, and sub node 5 in turn forwards to

sub node 4 the SRF along with the data from sub nodes 7 and 6. Sub node 4 has no data to add, so it simply forwards the data to sub node 3 (see the row labeled SUB 3), which forwards the data along with its own data to sub node 2 (see the row labeled SUB 2), which in turn forwards the data along with its own data to sub node 1. Sub node 1 has no data to add, so it forwards the data to sub node 0, which forwards the data along with its own data. As a result, the main node 102-1 receives the SRF followed by the data from sub nodes 7, 6, 3, 2, and 0 (see the row labeled MAIN).

[**0115**] FIG. 10 illustrates another example of the dynamic removal of data from a downstream transmission and insertion of data into an upstream transmission, from the perspective of the downstream DS transceiver 124, as in FIG. 9, although in FIG. 10, the sub nodes 102-2 are coupled with both sensors and actuators as the peripheral device 108 such that the main node 102-1 sends data downstream to all of the sub nodes 102-2 and receives data back from all of the sub nodes 102-2. Also, in FIG. 10, the data is ordered based on the node address to which it is destined or from which it originates. The data slot labeled "Y" may be used for a data integrity check or data correction.

[**0116**] FIG. 11 illustrates another example of the dynamic removal of data from a downstream transmission and insertion of data into an upstream transmission, from the perspective of the downstream DS transceiver 124, as in FIG. 9, although in FIG. 11, the data is conveyed downstream and upstream in sequential order rather than reverse order. Buffering at each sub node 102-2 allows for selectively adding, removing, and/or forwarding data.

[**0117**] As discussed above, each sub node 102-2 may remove data from downstream or upstream transmissions and/or may add data to downstream or upstream transmissions. Thus, for example, the main node 102-1 may transmit a separate sample of data to each of a number of sub nodes 102-2, and each such sub node 102-2 may remove its data sample and forward only data intended for downstream sub nodes 102-2. On the other hand, a sub node 102-2 may receive data from a downstream sub node 102-2 and forward the data along with additional

data. One advantage of transmitting as little information as needed is to reduce the amount of power consumed collectively by the system 100.

[**0118**] The system 100 may also support broadcast transmissions (and multicast transmissions) from the main node 102-1 to the sub nodes 102-2, specifically through configuration of the downstream slot usage of the sub nodes 102-2. Each sub node 102-2 may process the broadcast transmission and pass it along to the next sub node 102-2, although a particular sub node 102-2 may "consume" the broadcast message, (i.e., not pass the broadcast transmission along to the next sub node 102-2).

[**0119**] The system 100 may also support upstream transmissions (e.g., from a particular sub node 102-2 to one or more other sub nodes 102-2). Such upstream transmissions can include unicast, multicast, and/or broadcast upstream transmissions. With upstream addressing, as discussed above with reference to downstream transmissions, a sub node 102-2 may determine whether or not to remove data from an upstream transmission and/or whether or not to pass an upstream transmission along to the next upstream sub node 102-2 based on configuration of the upstream slot usage of the sub nodes 102-2. Thus, for example, data may be passed by a particular sub node 102-2 to one or more other sub nodes 102-2 in addition to, or in lieu of, passing the data to the main node 102-1. Such sub-sub relationships may be configured, for example, via the main node 102-1.

[**0120**] Thus, in various embodiments, the sub nodes 102-2 may operate as active/intelligent repeater nodes, with the ability to selectively forward, drop, and add information. The sub nodes 102-2 may generally perform such functions without necessarily decoding/examining all of the data, since each sub node 102-2 knows the relevant time slot(s) within which it will receive/transmit data, and hence can remove data from or add data into a time slot. Notwithstanding that the sub nodes 102-2 may not need to decode/examine all data, the sub nodes 102-2 may typically re-clock the data that it transmits/forwards. This may improve the robustness of the system 100.

[**0121**] In some embodiments, the bus 106 may be configured for unidirectional communications in a ring topology. For example, FIG. 12 illustrates an arrangement 1200 of the main node 102-1 and four sub nodes 102-2 in a ring topology, and illustrates signaling and timing considerations for unidirectional communication in the arrangement 1200, in accordance with various embodiments. In such embodiments, the node transceivers 120 in the nodes may include a receive-only transceiver (MAIN IN) and a transmit-only transceiver (MAIN OUT), rather than two bi-directional transceivers for upstream and downstream communication. In the link-layer synchronization scheme illustrated in FIG. 12, the main node 102-1 transmits a SCF 180, optionally followed by "downstream" data 1202 for the three speakers coupled to various sub nodes 102-2 (the data for the different speakers may be arranged in any suitable order, as discussed above with reference to FIGS. 8-11), and each successive sub node 102-2 forwards the synchronization control frame 180 along with any "upstream" data from prior sub nodes 102-2 and "upstream" data of its own to provide "upstream" data 1204 (e.g., the data from the eight different microphones may be arranged in any suitable order, as discussed above with reference to FIGS. 8-11).

[**0122**] As described herein, data may be communicated between elements of the system 100 in any of a number of ways. In some embodiments, data may be sent as part of a set of synchronous data slots upstream (e.g., using the data slots 199) by a sub node 102-2 or downstream (e.g., using the data slots 198) by a sub node 102-2 or a main node 102-1. The volume of such data may be adjusted by changing the number of bits in a data slot, or including extra data slots. Data may also be communicated in the system 100 by inclusion in a synchronization control frame 180 or a synchronization response frame 197. Data communicated this way may include I2C control data from the host 110 (with a response from a peripheral device 108 associated with a sub node 102-2); accesses to registers of the sub nodes 102-2 (e.g., for discovery and configuration of slots and interfaces) that may include write access from the host 110/main node 102-1 to a sub node 102-2 and read access from a sub node 102-2 to the host 110/main node 102-1; and event signaling via interrupts from

a peripheral device 108 to the host 110. In some embodiments, GPIO pins may be used to convey information from a sub node 102-2 to the main node 102-1 (e.g., by having the main node 102-1 poll the GPIO pins over I2C, or by having a node transceiver 120 of a sub node 102-2 generate an interrupt at an interrupt request pin). For example, in some such embodiments, a host 110 may send information to the main node 102-1 via I2C, and then the main node 102-1 may send that information to the sub node 102-2 via the GPIO pins. Any of the types of data discussed herein as transmitted over the bus 106 may be transmitted using any one or more of these communication pathways. Other types of data and data communication techniques within the system 100 may be disclosed herein.

[**0123**] Embodiments of the present disclosure may be implemented into a system using any suitable hardware and/or software to configure as desired. FIG. 13 schematically illustrates a device 1300 that may serve as a host or a node (e.g., a host 110, a main node 102-1, or a sub node 102-2) in the system 100, in accordance with various embodiments. A number of components are illustrated in FIG. 13 as included in the device 1300, but any one or more of these components may be omitted or duplicated, as suitable for the application.

[**0124**] Additionally, in various embodiments, the device 1300 may not include one or more of the components illustrated in FIG. 13, but the device 1300 may include interface circuitry for coupling to the one or more components. For example, the device 1300 may not include a display device 1306, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1306 may be coupled. In another set of examples, the device 1300 may not include an audio input device 1324 or an audio output device 1308, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1324 or audio output device 1308 may be coupled.

[**0125**] The device 1300 may include the node transceiver 120, in accordance with any of the embodiments disclosed herein, for managing communication along the

bus 106 when the device 1300 is coupled to the bus 106. The device 1300 may include a processing device 1302 (e.g., one or more processing devices), which may be included in the node transceiver 120 or separate from the node transceiver 120. As used herein, the term "processing device" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1302 may include one or more DSPs, ASICs, central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors, or any other suitable processing devices. The device 1300 may include a memory 1304, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), non-volatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive.

[**0126**] In some embodiments, the memory 1304 may be employed to store a working copy and a permanent copy of programming instructions to cause the device 1300 to perform any suitable ones of the techniques disclosed herein. In some embodiments, machine-accessible media (including non-transitory computer-readable storage media), methods, systems, and devices for performing the above-described techniques are illustrative examples of embodiments disclosed herein for communication over a two-wire bus. For example, a computer-readable media (e.g., the memory 1304) may have stored thereon instructions that, when executed by one or more of the processing devices included in the processing device 1302, cause the device 1300 to perform any of the techniques disclosed herein.

[**0127**] In some embodiments, the device 1300 may include another communication chip 1312 (e.g., one or more other communication chips). For example, the communication chip 1312 may be configured for managing wireless communications for the transfer of data to and from the device 1300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not

imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0128] The communication chip 1312 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The one or more communication chips 1312 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The one or more communication chips 1312 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The one or more communication chips 1312 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 1312 may operate in accordance with other wireless protocols in other embodiments. The device 1300 may include an antenna 1322 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0129] In some embodiments, the communication chip 1312 may manage wired communications using a protocol other than the protocol for the bus 106 described

herein. Wired communications may include electrical, optical, or any other suitable communication protocols. Examples of wired communication protocols that may be enabled by the communication chip 1312 include Ethernet, controller area network (CAN), I2C, media-oriented systems transport (MOST), or any other suitable wired communication protocol.

[**0130**] As noted above, the communication chip 1312 may include multiple communication chips. For instance, a first communication chip 1312 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1312 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1312 may be dedicated to wireless communications, and a second communication chip 1312 may be dedicated to wired communications.

[**0131**] The device 1300 may include battery/power circuitry 1314. The battery/power circuitry 1314 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the device 1300 to an energy source separate from the device 1300 (e.g., AC line power, voltage provided by a car battery, etc.). For example, the battery/power circuitry 1314 may include the upstream bus interface circuitry 132 and the downstream bus interface circuitry 131 discussed above with reference to FIG. 2 and could be charged by the bias on the bus 106.

[**0132**] The device 1300 may include a display device 1306 (or corresponding interface circuitry, as discussed above). The display device 1306 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[**0133**] The device 1300 may include an audio output device 1308 (or corresponding interface circuitry, as discussed above). The audio output device 1308

may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[**0134**] The device 1300 may include an audio input device 1324 (or corresponding interface circuitry, as discussed above). The audio input device 1324 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[**0135**] The device 1300 may include a GPS device 1318 (or corresponding interface circuitry, as discussed above). The GPS device 1318 may be in communication with a satellite-based system and may receive a location of the device 1300, as known in the art.

[**0136**] The device 1300 may include another output device 1310 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1310 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device. Additionally, any suitable ones of the peripheral devices 108 discussed herein may be included in the other output device 1310.

[**0137**] The device 1300 may include another input device 1320 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1320 may include an accelerometer, a gyroscope, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, or a radio frequency identification (RFID) reader. Additionally, any suitable ones of the sensors or peripheral devices 108 discussed herein may be included in the other input device 1320.

[**0138**] Any suitable ones of the display, input, output, communication, or memory devices described above with reference to the device 1300 may serve as the peripheral device 108 in the system 100. Alternatively or additionally, suitable ones of the display, input, output, communication, or memory devices described above with

reference to the device 1300 may be included in a host (e.g., the host 110) or a node (e.g., a main node 102-1 or a sub node 102-2).

[0139] The elements of a system 100 may be chosen and configured to provide audio and/or light control over the bus 106. In some embodiments, the system 100 may be configured to serve as a light control system in a vehicle or other environment, with lighting devices (e.g., strip-line light-emitting diodes (LEDs) or other LED arrangements) serving as peripheral devices 108 in communication with nodes 102 along the bus 106; data may be communicated over the bus 106 to control the color, intensity, duty cycle, and/or or other parameters of the lighting devices. In some embodiments, the system 100 may be configured to serve as an audio control system in a vehicle or other environment, with a microphone or other device including an accelerometer that may serve as a peripheral device 108 in communication with a node 102 along the bus 106; data from the accelerometer may be communicated over the bus 106 to control other peripheral devices 108 along the bus 106. For example, large spikes in the acceleration data or other predetermined acceleration data patterns may be used to trigger the generation of a sound effect, such as a cowbell or drum hit, by a processing device coupled to a node 102; that sound effect may be output by a speaker coupled to the processing device and/or by a speaker coupled to another node 102 along the bus 106. Some embodiments of the system 100 may combine any of the lighting control and/or audio control techniques disclosed herein.

[0140] Although various ones of the embodiments discussed above describe the system 100 in a vehicle setting, this is simply illustrative, and the system 100 may be implemented in any desired setting. For example, in some embodiments, a "suitcase" implementation of the system 100 may include a portable housing that includes the desired components of the system 100; such an implementation may be particularly suitable for portable applications, such as portable karaoke or entertainment systems.

[0141] As noted above, the calibration of microphones in an array (e.g., in embodiments of the system 100 in which one or more of the peripheral devices 108

include microphones) may be important for effective beamforming and other operations. FIGS. 14-22 illustrate example systems and techniques for calibration and the application of a calibration during runtime.

[**0142**] FIG. 14 illustrates a system for calibration of a microphone module during end-of-line test after production, in accordance with various embodiments. In the system of FIG. 14, a loudspeaker 2120 may play a test signal s(t) to a microphone module 2140 under calibration. The microphone module 2140 may include one microphone or it may include an array of *n* microphones $M_1...M_n$ 2141...2142. In some examples, $n=1$, and a microphone array is an array of one microphone. A reference microphone M_0 2130 may be placed between the loudspeaker 2120 and the microphone module 2140 or at any suitable known location relative to the loudspeaker 2120 and the microphone module 2140. The microphones $M_1...M_n$ may generate signals $m_1(t)...m_n(t)$, respectively, and these signals and the reference microphone signal $m_0(t)$ may be processed in a calibration calculator 2110. The calibration calculator 2110 may include any suitable processing devices, and may be, for example, a personal computer. The calibration calculator 2110 may generate a set of filter coefficients (also referred to herein as "calibration coefficients") $K_1...K_n$, and may transmit the filter coefficients to the microphone module 2140 under calibration. The coefficients may be stored in non-volatile memory 2143 (e.g., a programmable read-only memory (PROM)) associated with the microphone module2140.

[**0143**] Microphones modules are generally tested during or following production. In some examples, the speaker 2120 emits a tone, chirp, or a frequency range sweep, which is received at the reference microphone 2130 and at each of the microphones 2141, 2142 of the microphone module 2140. It is then determined whether each of the microphones 2141, 2142 passes a specification. A microphone 2141, 2142 response to the received tone includes frequency, magnitude, and phase measurements. Once it is determined what the received frequency, magnitude, and phase measurements are at a selected microphone 2141, 2142, calibration coefficients can be determined for the respective microphones or the microphone

module as a whole. In various examples, magnitude measurements are amplitude measurements. In some examples, some microphone modules do not pass the testing and are scrapped.

[**0144**] Microphone modules that pass the testing can be calibrated using test tone (or test chirp, test frequency sweep, etc.) response measurements, and a frequency and phase plot can be generated for each microphone 2141, 2142. The frequency and phase plots can be used for future microphone 2141, 2142 calibration. For example, calibration information can be generated for each microphone or for the microphone module as a whole and saved for future microphone calibration and/or compensation. In some examples, a transform is generated for each microphone 2141, 2142 which can be stored and used for later microphone compensation and/or calibration. In some examples, the calibration data is stored on a memory on the microphone module itself, such as in read only memory, programmable read only memory (PROM), erasable PROM (EPROM), and electrically erasable programmable read only memory (EEPROM). In some examples, the calibration data for the microphone is stored outside of the microphone. For example, the calibration data can be stored in a cloud storage and made accessible to a digital signal processor (DSP) for calibration before and during microphone use. In some examples, digital-bus networking features can be used to fetch specific microphone calibration data for each microphone.

[**0145**] In some examples, calibration of the microphones 2141, 2142 is accomplished using the reference microphone 2130. For instance, the reference microphone 2130 has a known response. Microphone calibration generates microphone calibration coefficients. The calibration coefficients can be stored on a microphone module, such that the calibration coefficients remain with the microphone regardless of where the microphone module is installed.

[**0146**] According to some implementations, calibration coefficients that are saved for each microphone include phase data, and in some examples, the calibration coefficients include phase tolerances. In some implementations, the calibration

coefficients include complex numbers. In some examples, the calibration coefficients include an impulse response. In some examples, the calibration coefficients include a transfer function.

[**0147**] According to various implementations, the reference microphone 2130 is the reference point in space, and the reference microphone 2130 calibrates the sound received from the speaker 2120, accounting for speaker 2120 uncertainties. In various examples, the reference microphone 2130 is pre-calibrated. In some examples, the frequency response of the reference microphone 2130 is pre-calibrated. In some examples, the frequency response of the reference microphone 2130 can be used for the microphone module 2140. In some implementations, phase information is included in the calibration, and saved to the microphone module, such as to a microphone memory 2143. In some examples, a computational device fetches calibration coefficient data stored on the microphone module 2140, and applies the data to the microphones 2141, 2142 to calibrate the microphones 2141, 2142.

[**0148**] In various implementations, the memory on the microphone module 2143 is an EPROM. In some examples, the memory module 2143 is an EEPROM. In some examples, the memory module 2143 is a one time programmable (OTP) EPROM. In some implementations, the memory module 2143 includes additional microphone information such as vendor information, product information, version information, serial number, device capabilities, as well as any other microphone information. In some implementations, the memory is integrated on an MCU or digital networking chip on the microphone module.

[**0149**] According to various implementations, calibration data that is stored on the microphone module itself includes frequency data, magnitude data, and phase data. In various examples, magnitude data includes amplitude data. In some examples, the calibration data is communicated over a 2-wire interface. In some examples, the calibration data is communicated over an audio communication network like a digital networking bus .

[**0150**] According to various implementations, calibration coefficients can be stored for a single microphone and calibration coefficients can be stored for a microphone array. In some examples, a single calibration is stored for the microphone array. For instance, if microphones are off center and the off-centered position of the microphones is discovered during calibration, the same calibration data can be used to calibrate for the off-centeredness of each of the microphone. Properties of the microphone array and microphone module 2140 can be calibrated together. In some examples, each microphone has individual calibration data.

[**0151**] In some examples, gain and phase correction can look like a shifted microphone. It can be known how a signal should appear at arrival, and adjustments can be made if the signal is misplaced. In various examples, a shift can be either a microphone mismatch or a microphone placement mismatch, as both are indistinguishable and can be taken care of simultaneously with the same end result.

[**0152**] In some implementations, microphones in the module 2140 are calibrated for a selected direction, and after a per sensor calibration, the microphones of the array in the microphone module 2140 are calibrated such that the microphones 2141, 2142 have identical frequency and phase responses. In general, once a microphone is calibrated, the calibration coefficients stay with the microphone and thus can be used wherever the microphone is eventually installed.

[**0153**] In some examples, the memory 2143 includes some calibration data that is specific for individual microphones and some calibration data that applies to the microphone module 2140. For example, physical characteristics of the microphone module 2140 such as the spacing between the microphones of a microphone array can be stored in the memory 2143. In some examples, coefficients are provided for a microphone array that is mounted in a vehicle head unit, such that beamforming can be applied to a driver. For example, a head unit may know which angle and/or direction to focus on, but the head unit may not know what kind of microphone array is installed. If the microphone array information is available to the head unit, the head unit can calculate beamforming characteristics. Information about a microphone

module that may be stored in the memory 2143 includes the number of microphones in the array, the gain range of the microphones, and physical characteristics of the microphones.

[0154] In some particular embodiments of the calibration method discussed above with reference to FIG. 14, short-time Fourier transforms may be used to calculate frequency domain representations S(f), M0(f), M1(f)...Mn(f) of the corresponding signals.

[0155] In some implementations, microphone data for multiple microphone modules in a system are stored on one memory device in a sub-node. In some implementations, microphone data for all microphone modules in a system are stored on one memory device in a sub-node. For example, calibration data can be stored at a sub node without onboard processing, but with data storage. In some examples, the data is stored after a post installation scenario test and stored in a network bus node having an available and open memory device.

[0156] FIG. 15 is a method 2200 illustrating operations that may be performed during calibration using a system like that of FIG. 14, according to various embodiments of the invention. At step 2202, a test signal s(t) is played back through a loudspeaker. For example, the test signal s(t) can be played back through the loudspeaker 2120. The test signal s(t) can be a test tone, a chirp, a frequency sweep, or any other type of signal. At step 2204, microphone audio signals $m_0(t)$, $m_1(t)$, ... $m_n(t)$ are sampled from the reference microphone and the microphones in the microphone array (e.g., the reference microphone audio signal $m_0(t)$ from the reference microphone 2130, and the microphone audio signals $m_1(t)$, ... $m_n(t)$ from the microphone array of the microphone module 2140.

[0157] At step 2206, frequency domain signals S(f), $M_0(f)$, $M_1(f)$, ..., $M_n(f)$ are determined based on frames of *N* audio samples of each time domain signal s(t), $m_0(t)$, $m_1(t)$, ..., $m_n(t)$. In some examples, a Fourier transform of the frames of the *N* audio samples of each time domain signal s(t), $m_0(t)$, $m_1(t)$, ..., $m_n(t)$ is used to calculate the

frequency domain signals S(f), $M_0(f)$, $M_1(f)$, ..., $M_n(f)$. At step 2208, calibration coefficients $K_1(t)$, ..., $K_n(t)$ are calculated for each microphone M1, ..., Mn (e.g., the microphones 2141, 2142 in the microphone array of the microphone module 2140). In some examples, spectral domain signals $M_1(f)$, ..., $M_n(f)$ and S(f) or $M_0(f)$ are used to calculate the calibration coefficients. In some examples, the frequency domain signals calculated at step 2206 are used to determine the calibration coefficients at step 2208. In some examples, the reference microphone audio signal $m_0(t)$ is used to determine the calibration coefficients for the microphones 2141, 2142 of the microphone array in the microphone module 2140. At step 2210, the calibration coefficients $K_1(t)$, ..., $K_n(t)$ are stored in a non-volatile memory associated with the microphone array (e.g., the calibration coefficients $K_1(\tau)$, ... $K_n(\tau)$ are stored in the memory 2143 of the microphone module 2140).

[0158] FIG. 16 is a method 2220 illustrating particular operations that may be performed in determining calibration coefficients, according to various embodiments of the invention. In particular, in some examples, the steps 2222 and 2224 of the method 2220 replace step 2208 of the method 2200 of FIG. 15. In some examples, the method 2220 begins after step 2206 of the method 2200 of FIG. 15. At step 2222, calibration transfer functions H_1... H_n are calculated for each microphone 2141, 2142 in the microphone module2140. In particular, the calibration transfer function Hx(f), x=1....n is calculated, where:

$$H_x(f) = \exp(i2\pi fd/c)\ \overline{M_0(f)M_0^*(f)}/\overline{M_x(f)M_0^*(f)}$$

[0159] In some examples, the calibration transfer functions are calculated using the sampled microphone audio signals $m_0(t)$, $m_1(t)$, ... $m_n(t)$. At step 2224, an inverse Fourier transform of $H_x(f)$ is used to calculate the calibration coefficients $K_1(\tau)$, ... $K_n(\tau)$ using the calibration transfer functions H_1... H_n. At step 2226, the calibration coefficients are stored in a non-volatile memory of the microphone module (e.g., the memory 2143 of the microphone module 2140).

[**0160**] In the embodiment of FIG. 16, the transfer function that maps M_0 to M_x, where x denotes any of the microphones 1...n, may be calculated as a quotient of: (1) a temporally averaged cross-correlation product of the microphone M_x and the reference microphone M_0 2130 (in the denominator), and (2) the auto-correlation product of M_0 (in the numerator). The calibration transfer function illustrated in FIG. 16 is the inverse of this transfer function, with the phase shift term $\exp(i2\pi fd/c)$ reflecting the time delay between M_0 and M_x, leading to shorter filters. Finite impulse response (FIR) filter coefficients K_x may be calculated by applying an inverse Fourier transform of the calibration transfer functions H_x 2312.

[**0161**] FIG. 17 is a method 2240 illustrating particular operations that may be performed in determining calibration coefficients, according to various embodiments of the invention. In particular, in some examples, the method 2240 begins after step 2204 of FIG. 15. As shown in FIG. 17, the method 2240 is a multi-step procedure. At step 2242, the test-signal loudspeaker is pre-calibrated. In particular, a transfer function $H_L(f)$ may be calculated to map the loudspeaker signal S(f) to the reference microphone signal $M_0(f)$. In one example:

$$H_L(f) = \overline{M_0(f)S^*(f)} / \overline{S^*(f)\,S(f)}$$

[**0162**] At step 2244, the calibration transfer functions $H_x(f)$, (x=1...n), are calculated. In particular:

$$x(f) = \exp(i2\pi fd/c)\ \overline{H_L(f)S(f)H_L{}^*(f)S^*(f)} / \overline{M_x(f)H_L{}^*(f)\,S^*(f)}$$

[**0163**] In some examples, the reference microphone M_0 is then not used for calculation of the calibration transfer functions H_x at step 2244. For instance, the reference microphone signal may be calculated as the product of $H_L(f)$ and S(f). The calculation of filter coefficients may then be performed as described above. In particular, at step 2246, the calibration coefficients $K_x(t)$, (x = 1 ...n) are determined by means of an inverse Fourier transform of $H_x(f)$, (x = 1...n). At step 2248, the calibration coefficients are stored in a microphone array memory. In yet another

embodiment, the first step of the calibration in the method 2240 may be omitted, and a loudspeaker may be utilized for outputting the test signal s(t) (e.g., a point-source with flat frequency response), and $H_L(f)$ may be set to 1 for all frequencies.

[**0164**] FIG. 18 illustrates a system 2400 including multiple microphone modules $A_1...A_m$ 2410...2420, according to various embodiments. The system 2400 illustrates the microphone modules $A_1...A_m$ 2410...2420 at the time of operation. In particular, the microphone modules $A_1...A_m$ 2410...2420 may be installed in a selected location for use. The microphone modules $A_1...A_m$ 2410...2420 may have been previously calibrated as described above with respect to FIGS. 14-17. During operation in the system 2400, the previously performed calibration may be used to filter the microphone signals for microphones in the modules $A_1...A_m$ 2410...2420. In particular, calibrations may have been previously performed for each of the microphone modules $A_1...A_m$ 2410...2420, and calibration coefficients may be stored in the memories 2413, 2423 on each microphone module $A_1...A_m$ 2410...2420. In the system of FIG. 18, a microphone signal processing unit 2430 may operate as an edge processor on the data interface 2450 (which may be, for example, any of the embodiments of the bus 106 disclosed herein) to the microphone signal sink 2440.

[**0165**] FIG. 19 is a diagram illustrating a method 2500 of applying the calibration coefficients during runtime, according to various embodiments. In some implementations, the method 2500 may be performed by the microphone signal processing unit 2430 of FIG. 18. At step 2502, calibration coefficients $K_{xy}(\tau)$, (x = 1…n, y=1…m), are retrieved by the microphone signal processing unit 2430 for the microphone modules $A_1...A_m$ 2410...2420 from the memories 2413, 2423 via the data interface 2510. At step 2504, a discrete convolution of the microphone signals $m_{xy}(t)$ with respective calibration coefficients $K_{xy}(\tau)$ is performed to yield calibrated microphone signals $n_{xy}(t)$.

$$n_{xy}(t) = \sum_{\tau} K_{xy}(\tau) m_{xy}(t - \tau)$$

[**0166**] where x = 1…n, y = 1…m

[**0167**] In some examples, the calibration coefficients K are applied as FIR filters. At step 2506, the original microphone signals $m_{xy}(t)$ are replaced with calibrated microphone signals $n_{xy}(t)$ in the microphone signal processing unit 2430. In some examples, the original microphone signals are replaced with calibrated microphone signals further down the data interface. At step 2508, calibrated microphone signals $n_{xy}(t)$ are forwarded to a microphone sink 2440 on the data interface 2450 in place of the original microphone signals $m_{xy}(t)$, x = 1…n, y = 1…m.

[**0168**] FIG. 20 is a diagram 2600 illustrating an example setting in which microphone modules calibrated in accordance with the techniques disclosed herein may be used, according to various embodiments of the disclosure. IN particular, FIG. 20 shows a vehicle including a main node 2602, a first sub-node 2604, a second sub-node 2606, and a third sub-node 2606. The main node 2602 is connected to the first sub-node 2604 via a bus 106; the first sub-node 2604 is connected to the second sub-node 2606 via the bus 106; and the second sub-node 2606 is connected to the third sub-node 2608 via the bus 106. Thus, the main node 2602, the first sub-node 2604, the second sub-node 2606, and the third sub-node 2608 are connected in a daisy-chain configuration, as described herein.

[**0169**] In some examples, the main node 2602 is a head unit. In some examples, digital audio signals from the second 2606 and third 2608 sub-nodes are sent to the first sub-node 2604. In various examples, any of the first 2604, second 2606, and third 2608 sub-nodes can include an audio-processing node. Similarly, the main node 2602 can include an audio-processing node. In various examples, an audio processing node can be a main node, a microphone node, an amplifier node, an emergency call node, or many other types of nodes. Although the setting of FIG. 20 is a vehicle, the systems and techniques disclosed herein may be used in any suitable setting. In some embodiments, the bus 106 may include a twisted wire pair (e.g., an unshielded twisted pair).

[**0170**] In some embodiments, the calibration of a microphone module may not take place in a factory at production time but may take place when the microphones are installed in their intended setting. For example, FIG. 21 is a diagram illustrating a method 2700 for microphone module calibration that may be performed by a system 100 to calibrate microphone modules in their operational setting, according to various embodiments of the disclosure. For example, the method 2700 can be performed in a vehicle, such as the vehicle illustrated in FIG. 20. However, the calibration procedure of FIG. 21 may be performed by a system 100 in a factory setting instead of an operational setting, as desired. Any appropriate ones of the techniques disclosed herein may be used to calculate the calibration coefficients of the procedure of FIG. 21.

[**0171**] At step 2702, the bus system is discovered and configured. The bus system can be any type of bus system, such as those described herein. At step 2704, a test signal is played from a reference speaker. In some examples, the test signal is a chirp. The reference speaker can be connected to the bus system. In some examples, the reference speaker is not connected to the bus system but is otherwise connected to the microphone system. At step 2706, while the test signal is applied, microphone nodes are sampled. Additionally, if there is a measurement microphone and/or reference microphone, at step 2706, the measurement microphone and/or reference microphone is sampled. At step 2708, calibration coefficients for each microphone node are calculated, along with any other calibration data. At step 2710, calibration information for each microphone node is stored in each microphone node.

[**0172**] FIG. 22 is a diagram illustrating a method 2750 for a microphone module operational procedure, according to various embodiments. The method 2750 may be performed by a system 100 to extract and use the calibration coefficients generated by any of the microphone module calibration techniques disclosed herein. At step 2752, the bus system is discovered and configured. The bus system can be any type of bus system, such as those described herein. At step 2754, pre-stored information from microphone nodes is read. In some examples, the pre-stored information is stored

on non-volatile memory at each microphone node, and the pre-stored information can include calibration information as well as general microphone information such as vendor, product, model number, serial number, version, etc. At step 2756, calibration information is forwarded to nodes that include an audio signal processor. At step 2758, the calibration information from the microphone is applied to audio signal processing nodes. At step 2760, audio output is played. The audio output can be analog or digital audio output, and can be output to a speaker, an amplifier, a phone, or any other audio output device.

[**0173**] Select Examples

[**0174**] Example 1 provides a system for microphone module calibration, comprising: a loudspeaker configured to play a test signal; a microphone module configured to receive the test signal and to generate a plurality of microphone array signals; a reference microphone positioned between the loudspeaker and the microphone module, wherein the reference microphone is configured to receive the test signal and to generate a reference signal; and a calibration calculator configured to process the plurality of microphone array signals and the reference signal, generate a set of filter coefficients, and transmit the set of filter coefficients to the microphone module.

[**0175**] Example 2 provides a system according to any of the preceding and/or following examples, further comprising a memory associated with the microphone array configured to store the set of filter coefficients.

[**0176**] Example 3 provides a system according to any of the preceding and/or following examples, wherein the memory is positioned on a microphone array module with the microphone array.

[**0177**] Example 4 provides a system according to any of the preceding and/or following examples, wherein the memory is a cloud-based memory accessible by the microphone array.

[**0178**] Example 5 provides a system according to any of the preceding and/or following examples, wherein the memory is further configured to store microphone information, including at least one of vendor information, product information, version information, model information, capability information, serial number, make information, configuration information, routing information, and authentication information.

[**0179**] Example 6 provides a system according to any of the preceding and/or following examples, further comprising a plurality of memory modules, wherein each of the plurality of memory modules is associated with a respective microphone of the microphone array.

[**0180**] Example 7 provides a system according to any of the preceding and/or following examples, wherein the filter coefficients include phase calibration, frequency calibration, and magnitude calibration.

[**0181**] Example 8 provides a system according to any of the preceding and/or following examples, further comprising a two-wire interface, wherein transmission of the filter coefficients to the microphone array occurs over the two-wire interface.

[**0182**] Example 9 provides a system according to any of the preceding and/or following examples, wherein each of the plurality of microphone array signals is unique and each respective microphone of the microphone array is associated with a respective subset of the set of filter coefficients.

[**0183**] Example 10 provides a method for microphone array calibration, comprising: playing a test signal at a loudspeaker; sampling the test signal at a microphone array; generating a plurality of microphone array signals at the microphone array; sampling the test signal at a reference microphone; generating a reference signal at the reference microphone; generating a set of filter coefficients based on the plurality of microphone array signals and the reference signal; and transmitting the set of filter coefficients to the microphone array.

[0184] Example 11 provides a method according to any of the preceding and/or following examples, wherein sampling the test signal at the microphone array comprises sampling the test signal at each respective microphone of the microphone array.

[0185] Example 12 provides a method according to any of the preceding and/or following examples, wherein generating a set of filter coefficients comprises generating a respective subset of filter coefficients for each respective microphone.

[0186] Example 13 provides a method according to any of the preceding and/or following examples, further comprising storing the respective subset of filter coefficients on each respective microphone.

[0187] Example 14 provides a method according to any of the preceding and/or following examples, further comprising storing the set of filter coefficients on the microphone array.

[0188] Example 15 provides a method according to any of the preceding and/or following examples, wherein transmitting the set of filter coefficients comprises transmitting the set of filter coefficients over a two-wire bus.

[0189] Example 16 provides a method according to any of the preceding and/or following examples, further comprising pre-calibrating the loudspeaker using the reference microphone.

[0190] Example 17 provides a self-calibrating microphone system, comprising: a microphone module including: a microphone configured to receive an audio input signal and output a raw microphone output signal, wherein the microphone is pre-calibrated, and a non-volatile memory configured to store microphone calibration coefficients for the microphone; a processor configured to receive the raw microphone signal and the microphone calibration coefficients, and generate a calibrated microphone signal; and a microphone signal sink configured to receive the calibrated microphone signal from the processor and output the calibrated microphone signal.

[**0191**] Example 18 provides a system according to any of the preceding and/or following examples, wherein the microphone calibration coefficients are configured for at least one of phase calibration, frequency calibration, and magnitude calibration.

[**0192**] Example 19 provides a system according to any of the preceding and/or following examples, wherein the processor is further configured to use the microphone calibration coefficients for phase calibration of the raw microphone signal.

[**0193**] Example 20 provides a system according to any of the preceding and/or following examples, further comprising a two-wire bus wherein the processor and the microphone signal sink communicate over the two-wire bus.

[**0194**] Example 21 provides a system according to any of the preceding and/or following examples, wherein the processor is further configured to perform a convolution of the raw microphone signal and the microphone calibration coefficients to generate the calibrated microphone signal.

[**0195**] Example 22 include any of the phase and frequency response calibration systems and techniques disclosed herein.

[**0196**] Example 23 includes the subject matter according to any of the preceding and/or following examples, and further includes storage of the calibration coefficients local to the microphone array.

[**0197**] Example 24 includes the subject matter according to any of the preceding and/or following examples, and further includes the central application of calibration coefficients to uncalibrated microphone data from multiple microphone arrays.

[**0198**] Example 25 includes the subject matter according to any of the preceding and/or following examples, and further includes the replacement of original microphone signals with calibrated microphone signals.

[**0199**] Example 26 includes the subject matter according to any of the preceding and/or following examples, and further specifies that a microphone array is a peripheral device in any of the two-wire communication systems disclosed herein.

[**0200**] Example 27 provides a method according to any of the preceding and/or following examples, wherein the microphone array includes a single microphone.

[**0201**] Example 28 provides a system according to any of the preceding and/or following examples, wherein the microphone array includes a single microphone.

[**0202**] Example 29 provides a system according to any of the preceding and/or following examples, further comprising a two-wire bus, wherein the memory is positioned on a network bus sub-node.

[**0203**] Variations and Implementations

[**0204**] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. For example, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the embodiments described herein.

[**0205**] Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described. In addition, any combination of two or more features, systems, articles, materials, kits, and/or methods described herein, if such features, systems,

articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present disclosure.

[**0206**] The foregoing outlines features of one or more embodiments of the subject matter disclosed herein. These embodiments are provided to enable a person having ordinary skill in the art (PHOSITA) to better understand various aspects of the present disclosure. Certain well-understood terms, as well as underlying technologies and/or standards may be referenced without being described in detail. It is anticipated that the PHOSITA will possess or have access to background knowledge or information in those technologies and standards sufficient to practice the teachings of the present disclosure.

[**0207**] The PHOSITA will appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes, structures, or variations for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. The PHOSITA will also recognize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

[**0208**] The above-described embodiments may be implemented in any of numerous ways. One or more aspects and embodiments of the present application involving the performance of processes or methods may utilize program instructions executable by a device (e.g., a computer, a processor, or other device) to perform, or control performance of, the processes or methods.

[**0209**] In this respect, various inventive concepts may be embodied as a computer readable storage medium (or multiple computer readable storage media) (e.g., a computer memory, one or more floppy discs, compact discs, optical discs, magnetic tapes, flash memories, circuit configurations in Field Programmable Gate Arrays or other semiconductor devices, or other tangible computer storage medium) encoded with one or more programs that, when executed on one or more computers or other

processors, perform methods that implement one or more of the various embodiments described above.

[0210] The computer readable medium or media may be transportable, such that the program or programs stored thereon may be loaded onto one or more different computers or other processors to implement various ones of the aspects described above. In some embodiments, computer readable media may be non-transitory media.

[0211] Note that the activities discussed above with reference to the **FIGURES** which are applicable to any integrated circuit that involves signal processing (for example, gesture signal processing, video signal processing, audio signal processing, analog-to-digital conversion, digital-to-analog conversion), particularly those that can execute specialized software programs or algorithms, some of which may be associated with processing digitized real-time data.

[0212] In some cases, the teachings of the present disclosure may be encoded into one or more tangible, non-transitory computer-readable mediums having stored thereon executable instructions that, when executed, instruct a programmable device (such as a processor or DSP) to perform the methods or functions disclosed herein. In cases where the teachings herein are embodied at least partly in a hardware device (such as an ASIC, IP block, or SoC), a non-transitory medium could include a hardware device hardware-programmed with logic to perform the methods or functions disclosed herein. The teachings could also be practiced in the form of Register Transfer Level (RTL) or other hardware description language such as VHDL or Verilog, which can be used to program a fabrication process to produce the hardware elements disclosed.

[0213] In example implementations, at least some portions of the processing activities outlined herein may also be implemented in software. In some embodiments, one or more of these features may be implemented in hardware provided external to the elements of the disclosed figures, or consolidated in any appropriate manner to achieve the intended functionality. The various components may include software (or reciprocating software) that can coordinate in order to achieve the operations as

outlined herein. In still other embodiments, these elements may include any suitable algorithms, hardware, software, components, modules, interfaces, or objects that facilitate the operations thereof.

[**0214**] Any suitably-configured processor component can execute any type of instructions associated with the data to achieve the operations detailed herein. Any processor disclosed herein could transform an element or an article (for example, data) from one state or thing to another state or thing. In another example, some activities outlined herein may be implemented with fixed logic or programmable logic (for example, software and/or computer instructions executed by a processor) and the elements identified herein could be some type of a programmable processor, programmable digital logic (for example, an FPGA, an erasable programmable read only memory (EPROM), an electrically erasable programmable read only memory (EEPROM)), an ASIC that includes digital logic, software, code, electronic instructions, flash memory, optical disks, CD-ROMs, DVD ROMs, magnetic or optical cards, other types of machine-readable mediums suitable for storing electronic instructions, or any suitable combination thereof.

[**0215**] In operation, processors may store information in any suitable type of non-transitory storage medium (for example, random access memory (RAM), read only memory (ROM), FPGA, EPROM, electrically erasable programmable ROM (EEPROM), etc.), software, hardware, or in any other suitable component, device, element, or object where appropriate and based on particular needs. Further, the information being tracked, sent, received, or stored in a processor could be provided in any database, register, table, cache, queue, control list, or storage structure, based on particular needs and implementations, all of which could be referenced in any suitable timeframe.

[**0216**] Any of the memory items discussed herein should be construed as being encompassed within the broad term 'memory.' Similarly, any of the potential processing elements, modules, and machines described herein should be construed as being encompassed within the broad term 'microprocessor' or 'processor.' Furthermore,

in various embodiments, the processors, memories, network cards, buses, storage devices, related peripherals, and other hardware elements described herein may be realized by a processor, memory, and other related devices configured by software or firmware to emulate or virtualize the functions of those hardware elements.

[**0217**] Further, it should be appreciated that a computer may be embodied in any of a number of forms, such as a rack-mounted computer, a desktop computer, a laptop computer, or a tablet computer, as non-limiting examples. Additionally, a computer may be embedded in a device not generally regarded as a computer but with suitable processing capabilities, including a personal digital assistant (PDA), a smart phone, a mobile phone, an iPad, or any other suitable portable or fixed electronic device.

[**0218**] Also, a computer may have one or more input and output devices. These devices can be used, among other things, to present a user interface. Examples of output devices that may be used to provide a user interface include printers or display screens for visual presentation of output and speakers or other sound generating devices for audible presentation of output. Examples of input devices that may be used for a user interface include keyboards, and pointing devices, such as mice, touch pads, and digitizing tablets. As another example, a computer may receive input information through speech recognition or in other audible formats.

[**0219**] Such computers may be interconnected by one or more networks in any suitable form, including a local area network or a wide area network, such as an enterprise network, and intelligent network (IN) or the Internet. Such networks may be based on any suitable technology and may operate according to any suitable protocol and may include wireless networks or wired networks.

[**0220**] Computer-executable instructions may be in many forms, such as program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that performs particular tasks or implement particular abstract data types. Typically, the

functionality of the program modules may be combined or distributed as desired in various embodiments.

[**0221**] The terms "program" or "software" are used herein in a generic sense to refer to any type of computer code or set of computer-executable instructions that may be employed to program a computer or other processor to implement various aspects as described above. Additionally, it should be appreciated that according to one aspect, one or more computer programs that when executed perform methods of the present application need not reside on a single computer or processor, but may be distributed in a modular fashion among a number of different computers or processors to implement various aspects of the present application.

[**0222**] Also, data structures may be stored in computer-readable media in any suitable form. For simplicity of illustration, data structures may be shown to have fields that are related through location in the data structure. Such relationships may likewise be achieved by assigning storage for the fields with locations in a computer-readable medium that convey relationship between the fields. However, any suitable mechanism may be used to establish a relationship between information in fields of a data structure, including through the use of pointers, tags or other mechanisms that establish relationship between data elements.

[**0223**] When implemented in software, the software code may be executed on any suitable processor or collection of processors, whether provided in a single computer or distributed among multiple computers.

[**0224**] Computer program logic implementing all or part of the functionality described herein is embodied in various forms, including, but in no way limited to, a source code form, a computer executable form, a hardware description form, and various intermediate forms (for example, mask works, or forms generated by an assembler, compiler, linker, or locator). In an example, source code includes a series of computer program instructions implemented in various programming languages, such as an object code, an assembly language, or a high-level language such as OpenCL,

RTL, Verilog, VHDL, Fortran, C, C++, JAVA, or HTML for use with various operating systems or operating environments. The source code may define and use various data structures and communication messages. The source code may be in a computer executable form (e.g., via an interpreter), or the source code may be converted (e.g., via a translator, assembler, or compiler) into a computer executable form.

[**0225**] In some embodiments, any number of electrical circuits of the FIGURES may be implemented on a board of an associated electronic device. The board can be a general circuit board that can hold various components of the internal electronic system of the electronic device and, further, provide connectors for other peripherals. More specifically, the board can provide the electrical connections by which the other components of the system can communicate electrically. Any suitable processors (inclusive of digital signal processors, microprocessors, supporting chipsets, etc.), memory elements, etc. can be suitably coupled to the board based on particular configuration needs, processing demands, computer designs, etc.

[**0226**] Other components such as external storage, additional sensors, controllers for audio/video display, and peripheral devices may be attached to the board as plug-in cards, via cables, or integrated into the board itself. In another example embodiment, the electrical circuits of the **FIGURES** may be implemented as standalone modules (e.g., a device with associated components and circuitry configured to perform a specific application or function) or implemented as plug-in modules into application-specific hardware of electronic devices.

[**0227**] Note that with the numerous examples provided herein, interaction may be described in terms of two, three, four, or more electrical components. However, this has been done for purposes of clarity and example only. It should be appreciated that the system can be consolidated in any suitable manner. Along similar design alternatives, any of the illustrated components, modules, and elements of the **FIGURES** may be combined in various possible configurations, all of which are clearly within the broad scope of this disclosure.

[**0228**] In certain cases, it may be easier to describe one or more of the functionalities of a given set of flows by only referencing a limited number of electrical elements. It should be appreciated that the electrical circuits of the **FIGURES** and its teachings are readily scalable and can accommodate a large number of components, as well as more complicated/sophisticated arrangements and configurations. Accordingly, the examples provided should not limit the scope or inhibit the broad teachings of the electrical circuits as potentially applied to a myriad of other architectures.

[**0229**] Also, as described, some aspects may be embodied as one or more methods. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[**0230**] Interpretation of Terms

[**0231**] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms. Unless the context clearly requires otherwise, throughout the description and the claims:

[**0232**] "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to".

[**0233**] "connected," "coupled," or any variant thereof, means any connection or coupling, either direct or indirect, between two or more elements; the coupling or connection between the elements can be physical, logical, or a combination thereof.

[**0234**] "herein," "above," "below," and words of similar import, when used to describe this specification shall refer to this specification as a whole and not to any particular portions of this specification.

[**0235**] "or," in reference to a list of two or more items, covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[**0236**] the singular forms "a", "an" and "the" also include the meaning of any appropriate plural forms.

[**0237**] Words that indicate directions such as "vertical", "transverse", "horizontal", "upward", "downward", "forward", "backward", "inward", "outward", "vertical", "transverse", "left", "right", "front", "back", "top", "bottom", "below", "above", "under", and the like, used in this description and any accompanying claims (where present) depend on the specific orientation of the apparatus described and illustrated. The subject matter described herein may assume various alternative orientations. Accordingly, these directional terms are not strictly defined and should not be interpreted narrowly.

[**0238**] The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

[**0239**] The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined.

[**0240**] Elements other than those specifically identified by the "and/or" clause may optionally be present, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" may refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[**0241**] As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified.

[**0242**] Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") may refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[**0243**] As used herein, the term "between" is to be inclusive unless indicated otherwise. For example, "between A and B" includes A and B unless indicated otherwise.

[**0244**] Also, the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. The use of "including," "comprising," or "having," "containing," "involving," and variations thereof herein, is meant to encompass the items listed thereafter and equivalents thereof as well as additional items.

[**0245**] In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e.,

to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively.

[**0246**] Numerous other changes, substitutions, variations, alterations, and modifications may be ascertained to one skilled in the art and it is intended that the present disclosure encompass all such changes, substitutions, variations, alterations, and modifications as falling within the scope of the appended claims.

[**0247**] In order to assist the United States Patent and Trademark Office (USPTO) and, additionally, any readers of any patent issued on this application in interpreting the claims appended hereto, Applicant wishes to note that the Applicant: (a) does not intend any of the appended claims to invoke 35 U.S.C. § 112(f) as it exists on the date of the filing hereof unless the words "means for" or "steps for" are specifically used in the particular claims; and (b) does not intend, by any statement in the disclosure, to limit this disclosure in any way that is not otherwise reflected in the appended claims.

[**0248**] The present invention should therefore not be considered limited to the particular embodiments described above. Various modifications, equivalent processes, as well as numerous structures to which the present invention may be applicable, will be readily apparent to those skilled in the art to which the present invention is directed upon review of the present disclosure.

CLAIMS

What is claimed is:

1. A system for microphone calibration, comprising:

a loudspeaker configured to play a test signal;

a microphone array configured to receive the test signal and to generate a plurality of microphone array signals;

a reference microphone positioned between the loudspeaker and the microphone array, wherein the reference microphone is configured to receive the test signal and to generate a reference signal; and

a calibration calculator configured to process the plurality of microphone array signals and the reference signal, generate a set of filter coefficients, and transmit the set of filter coefficients to the microphone array.

2. The system of claim 1, further comprising a memory associated with the microphone array configured to store the set of filter coefficients.

3. The system of claim 2, wherein the memory is positioned on a microphone array module with the microphone array.

4. The system of claim 2, wherein the memory is a cloud-based memory accessible by the microphone array.

5. The system of any one of claims 2 to 4, wherein the memory is further configured to store microphone information, including at least one of vendor information, product information, version information, model information, capability information, serial number, make information, configuration information, routing information, and authentication information.

6. The system of any one of the preceding claims, further comprising a plurality of memory modules, wherein each of the plurality of memory modules is associated with a respective microphone of the microphone array.

7. The system of any one of the preceding claims, wherein the filter coefficients provide phase calibration and magnitude calibration.

8. The system of any one of the preceding claims, further comprising a two-wire interface, wherein transmission of the filter coefficients to the microphone array occurs over the two-wire interface.

9. The system of any one of the preceding claims, wherein each of the plurality of microphone array signals is unique and each respective microphone of the microphone array is associated with a respective subset of the set of filter coefficients.

10. A method for microphone array calibration, comprising:

playing a test signal at a loudspeaker;

sampling the test signal at a microphone array;

generating a plurality of microphone array signals at the microphone array;

sampling the test signal at a reference microphone;

generating a reference signal at the reference microphone;

generating a set of filter coefficients based on the plurality of microphone array signals and the reference signal; and

transmitting the set of filter coefficients to the microphone array.

11. The method of claim 10, wherein sampling the test signal at the microphone array comprises sampling the test signal at each respective microphone of the microphone array.

12. The method of claim 10 or 11, wherein generating a set of filter coefficients comprises generating a respective subset of filter coefficients for each respective microphone.

13. The method of claim 12, further comprising storing the respective subset of filter coefficients on each respective microphone.

14. The method of any one of claims 10 to 13, further comprising storing the set of filter coefficients on the microphone array.

15. The method of claim any one of claims 10 to 14, wherein transmitting the set of filter coefficients comprises transmitting the set of filter coefficients over a two-wire bus.

16. The method of any one of claims 10 to 15, further comprising pre-calibrating the loudspeaker using the reference microphone.

17. A self-calibrating microphone system, comprising:
    a microphone module including:
        a microphone configured to receive an audio input signal and output a raw microphone output signal, wherein the microphone is pre-calibrated; and
        a non-volatile memory configured to store microphone calibration coefficients for the microphone;
    a processor configured to receive the raw microphone signal and the microphone calibration coefficients, and generate a calibrated microphone signal; and
    a microphone signal sink configured to receive the calibrated microphone signal from the processor and output the calibrated microphone signal.

18. The microphone system of claim 17, wherein the microphone calibration coefficients are configured for phase calibration and magnitude calibration.

19. The microphone system of claim 17 or 18, further comprising a two-wire bus, wherein the processor and the microphone signal sink communicate over the two-wire bus.

20. The microphone system of any one of claims 17 to 19, wherein the processor is further configured to perform a convolution of the raw microphone signal and the microphone calibration coefficients to generate the calibrated microphone signal.

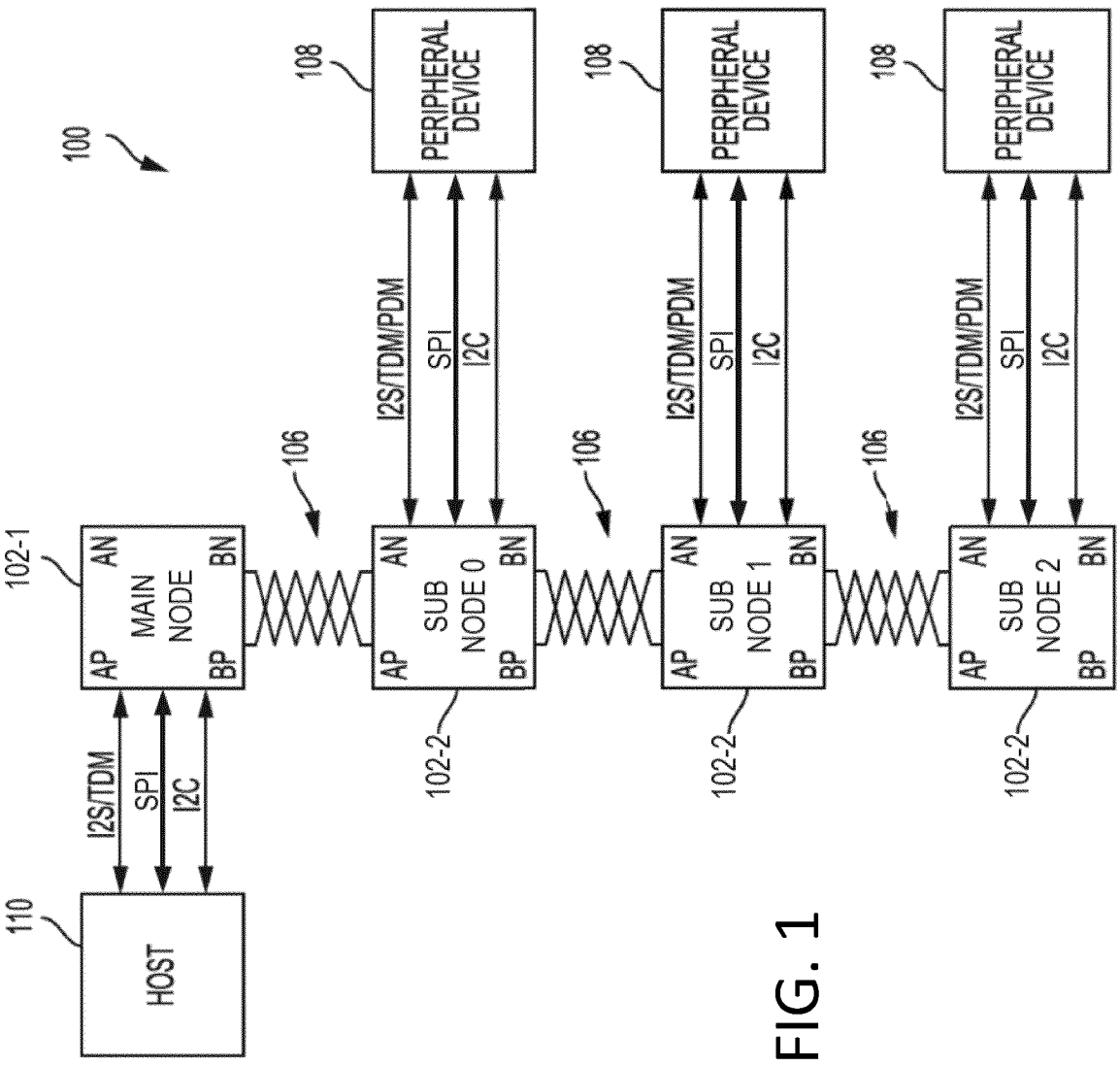
100
102-1
MAIN NODE
AN
BN
AP
BP
I2S/TDM
SPI
I2C
110
HOST
106
SUB NODE 0
102-2
I2S/TDM/PDM
108
PERIPHERAL DEVICE
SUB NODE 1
SUB NODE 2

FIG. 1

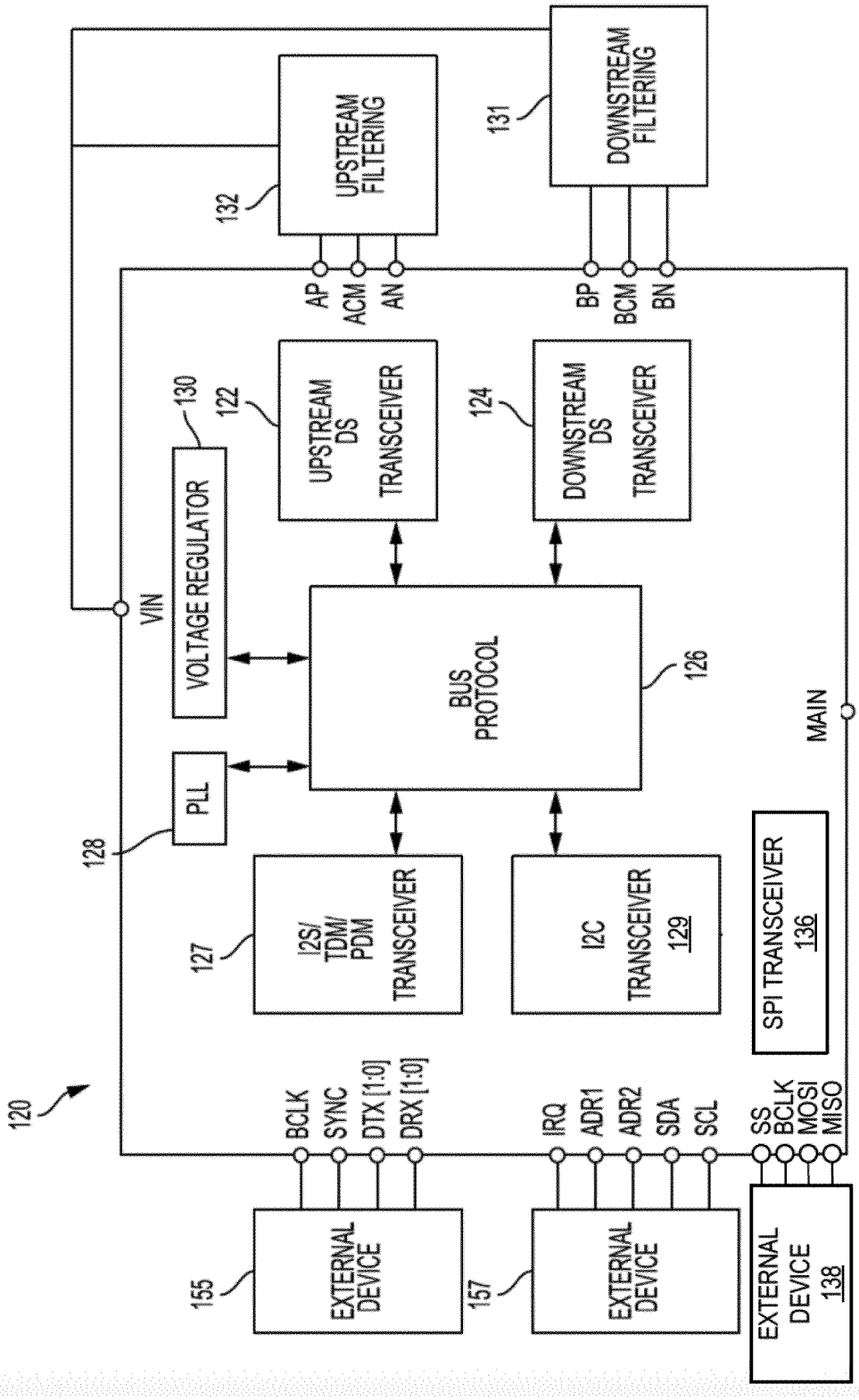
120
VIN
VOLTAGE REGULATOR
130
PLL
128
UPSTREAM DS TRANSCEIVER
122
DOWNSTREAM DS TRANSCEIVER
124
BUS PROTOCOL
126
I2S/ TDM/ PDM TRANSCEIVER
127
I2C TRANSCEIVER 129
SPI TRANSCEIVER 136
UPSTREAM FILTERING
132
DOWNSTREAM FILTERING
131
AP
ACM
AN
BP
BCM
BN
MAIN
BCLK
SYNC
DTX [1:0]
DRX [1:0]
IRQ
ADR1
ADR2
SDA
SCL
SS
BCLK
MOSI
MISO
EXTERNAL DEVICE
155
EXTERNAL DEVICE
157
EXTERNAL DEVICE 138

FIG. 2

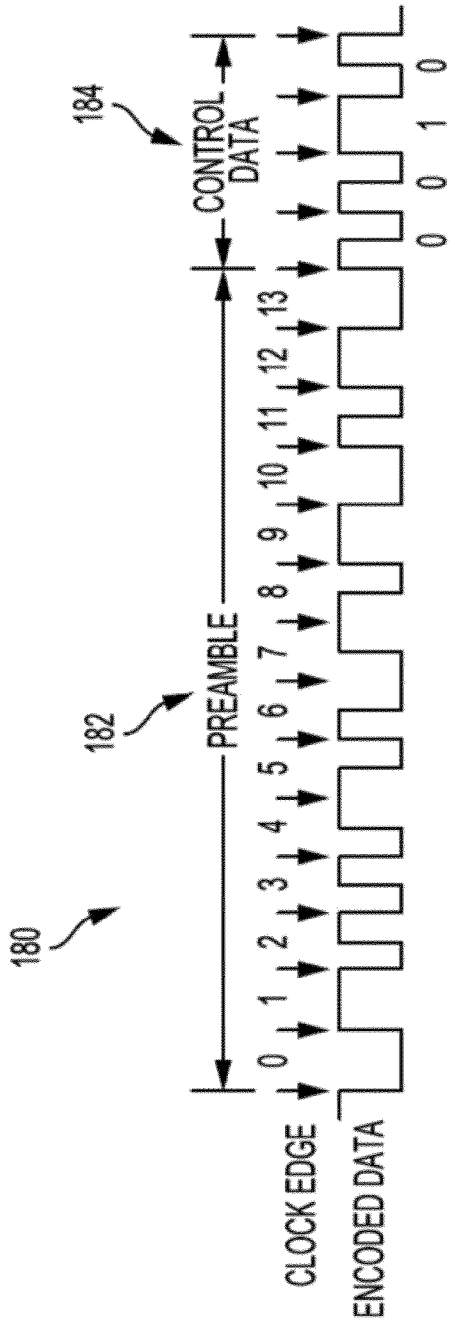
180
182
184
PREAMBLE
CONTROL DATA
CLOCK EDGE
ENCODED DATA
0 1 2 3 4 5 6 7 8 9 10 11 12 13
0 0 1 0

FIG. 3

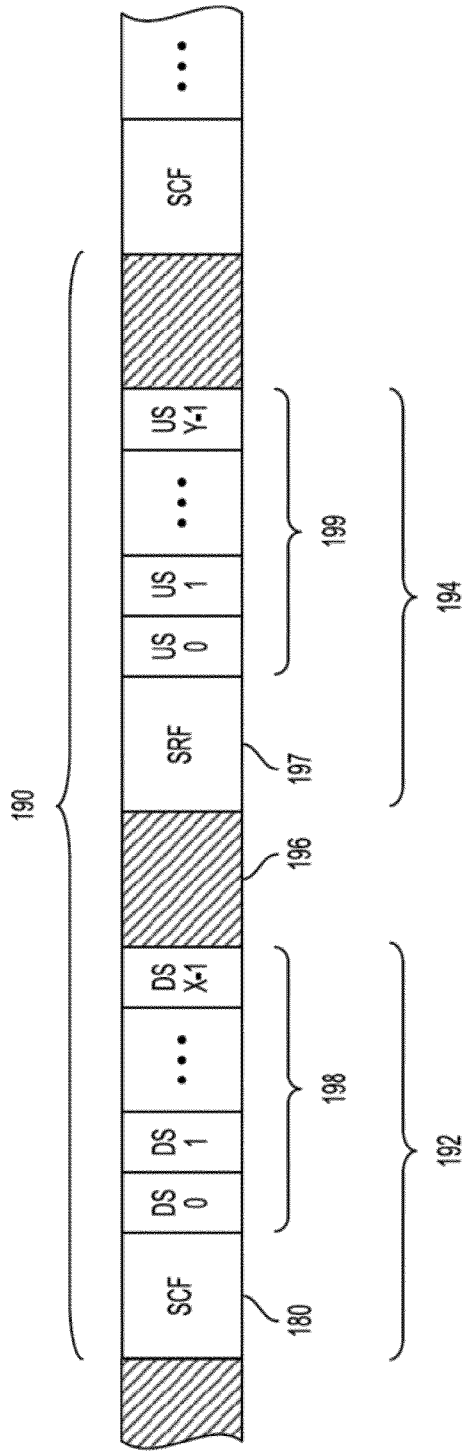
190
SCF
DS 0
DS 1
• • •
DS X-1
196
SRF
US 0
US 1
• • •
US Y-1
SCF
• • •
180
197
198
199
192
194

FIG. 4

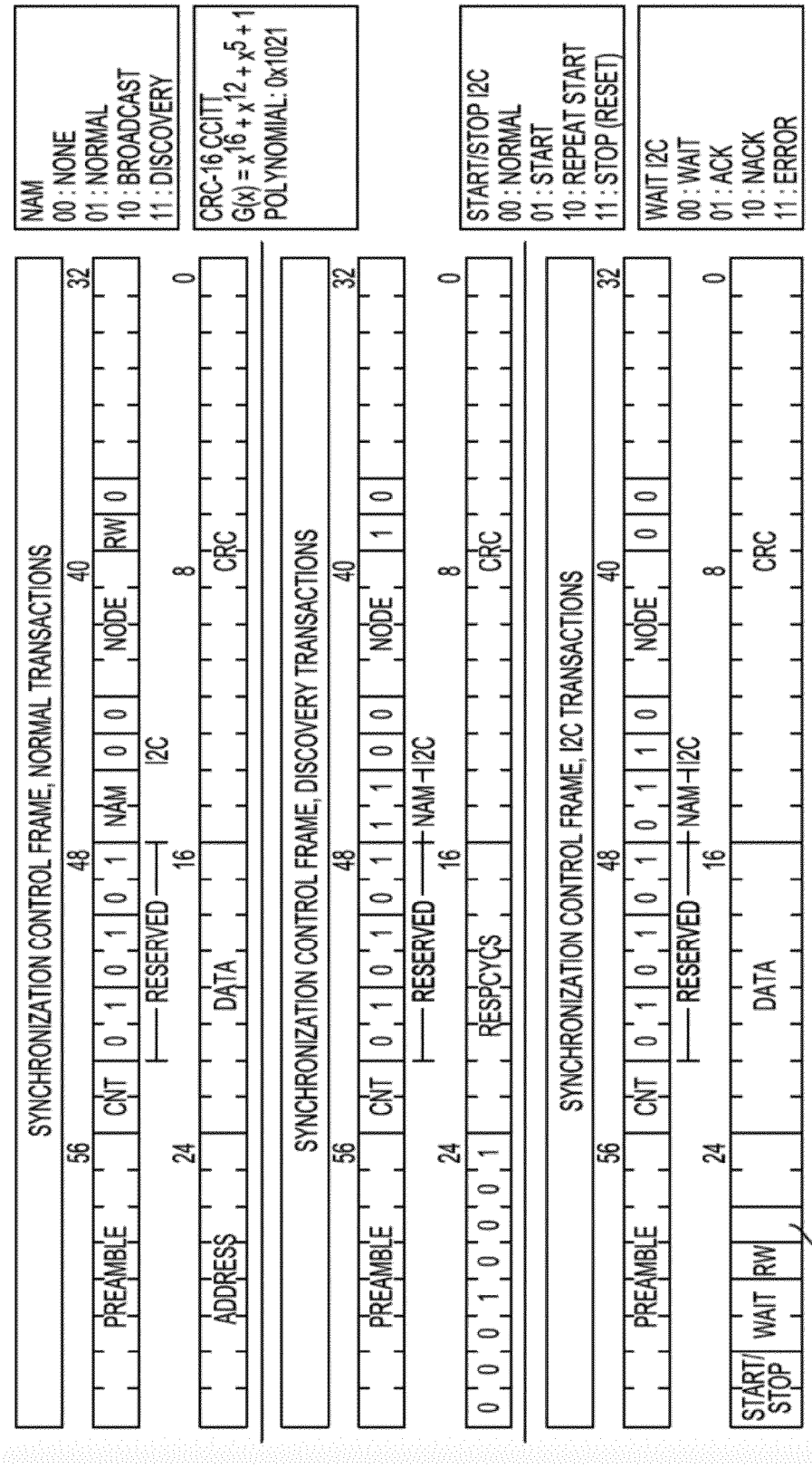
SYNCHRONIZATION CONTROL FRAME, NORMAL TRANSACTIONS
PREAMBLE
CNT
0 1 0 1 0 1
NAM
0 0
NODE
RW
0
RESERVED
I2C
ADDRESS
DATA
CRC
SYNCHRONIZATION CONTROL FRAME, DISCOVERY TRANSACTIONS
PREAMBLE
CNT
0 1 0 1 0 1
1 1 0 0
NODE
1 0
RESERVED
NAM-I2C
0 0 1 0 0 0 1
RESPCYCS
CRC
SYNCHRONIZATION CONTROL FRAME, I2C TRANSACTIONS
PREAMBLE
CNT
0 1 0 1 0 1
0 1 1 0
NODE
0 0
RESERVED
NAM-I2C
START/ STOP
WAIT
RW
DATA
CRC
DATA VID
56
48
40
32
24
16
8
0
NAM
00 : NONE
01 : NORMAL
10 : BROADCAST
11 : DISCOVERY
CRC-16 CCITT
G(x) = x16 + x12 + x5 + 1
POLYNOMIAL: 0x1021
START/STOP I2C
00 : NORMAL
01 : START
10 : REPEAT START
11 : STOP (RESET)
WAIT I2C
00 : WAIT
01 : ACK
10 : NACK
11 : ERROR

FIG. 5

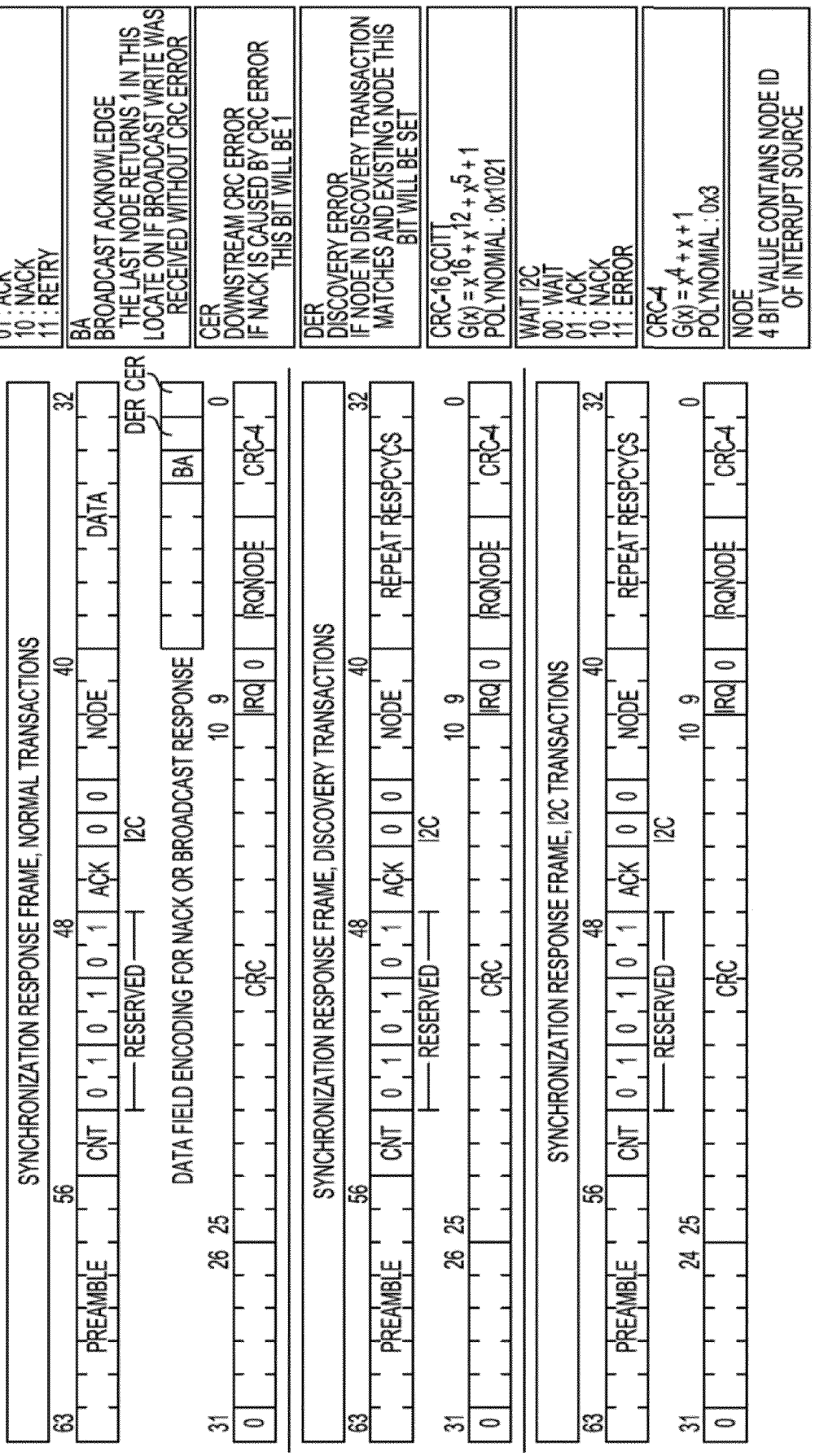
SYNCHRONIZATION RESPONSE FRAME, NORMAL TRANSACTIONS
PREAMBLE
CNT
RESERVED
I2C
ACK
NODE
DATA
DER CER
DATA FIELD ENCODING FOR NACK OR BROADCAST RESPONSE
BA
CRC
IRQ
IRQNODE
CRC-4
SYNCHRONIZATION RESPONSE FRAME, DISCOVERY TRANSACTIONS
REPEAT RESPCYCS
SYNCHRONIZATION RESPONSE FRAME, I2C TRANSACTIONS
ACK
00 : WAIT
01 : ACK
10 : NACK
11 : RETRY
BA
BROADCAST ACKNOWLEDGE
THE LAST NODE RETURNS 1 IN THIS
LOCATE ON IF BROADCAST WRITE WAS
RECEIVED WITHOUT CRC ERROR
CER
DOWNSTREAM CRC ERROR
IF NACK IS CAUSED BY CRC ERROR
THIS BIT WILL BE 1
DER
DISCOVERY ERROR
IF NODE IN DISCOVERY TRANSACTION
MATCHES AND EXISTING NODE THIS
BIT WILL BE SET
CRC-16 CCITT
G(x) = x16 + x12 + x5 + 1
POLYNOMIAL : 0x1021
WAIT I2C
00 : WAIT
01 : ACK
10 : NACK
11 : ERROR
CRC-4
G(x) = x4 + x + 1
POLYNOMIAL : 0x3
NODE
4 BIT VALUE CONTAINS NODE ID
OF INTERRUPT SOURCE

FIG. 6

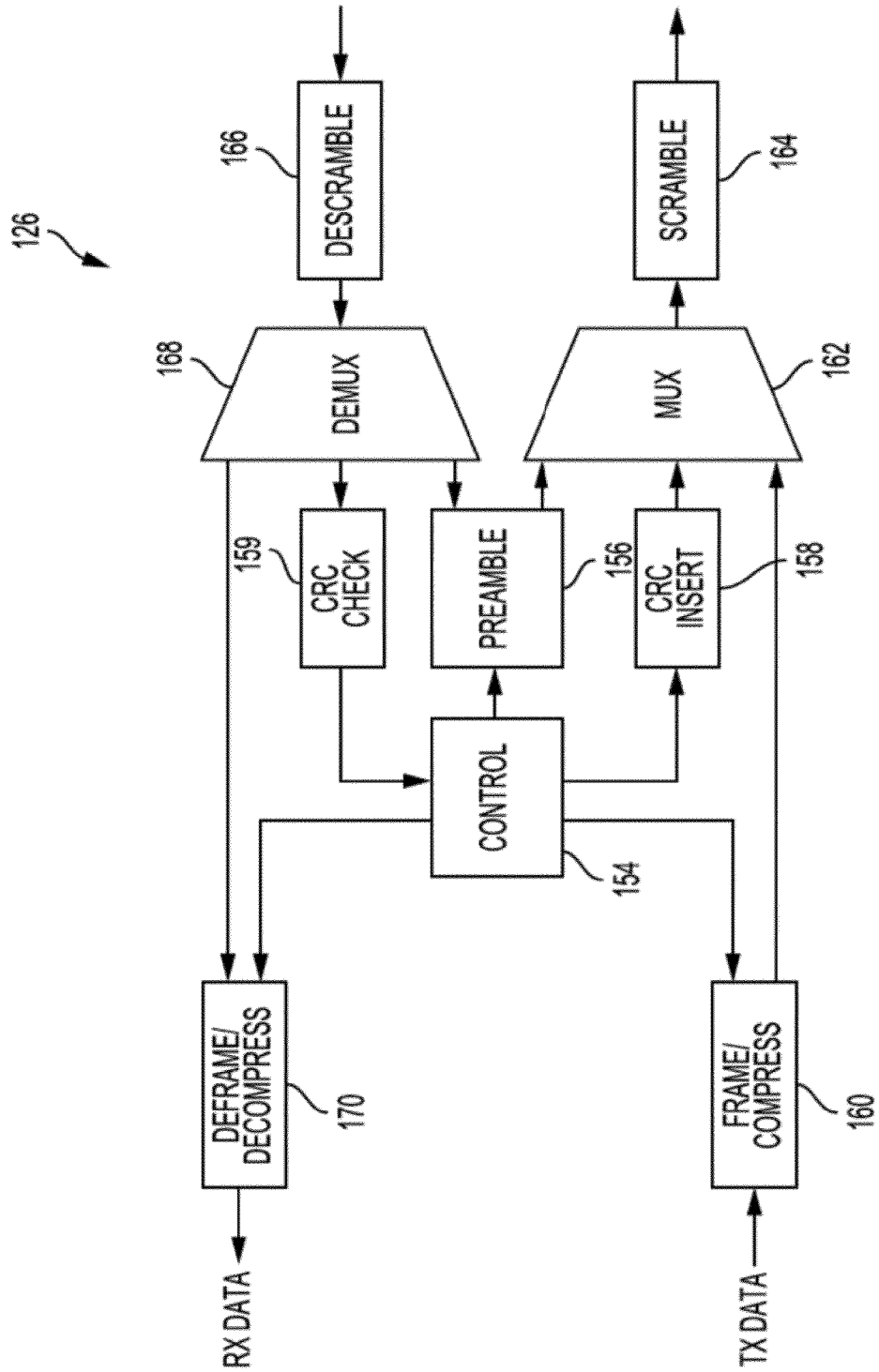
126
166
DESCRAMBLE
164
SCRAMBLE
168
DEMUX
MUX
162
159
CRC CHECK
PREAMBLE
156
CRC INSERT
158
CONTROL
154
DEFRAME/ DECOMPRESS
170
FRAME/ COMPRESS
160
RX DATA
TX DATA

FIG. 7

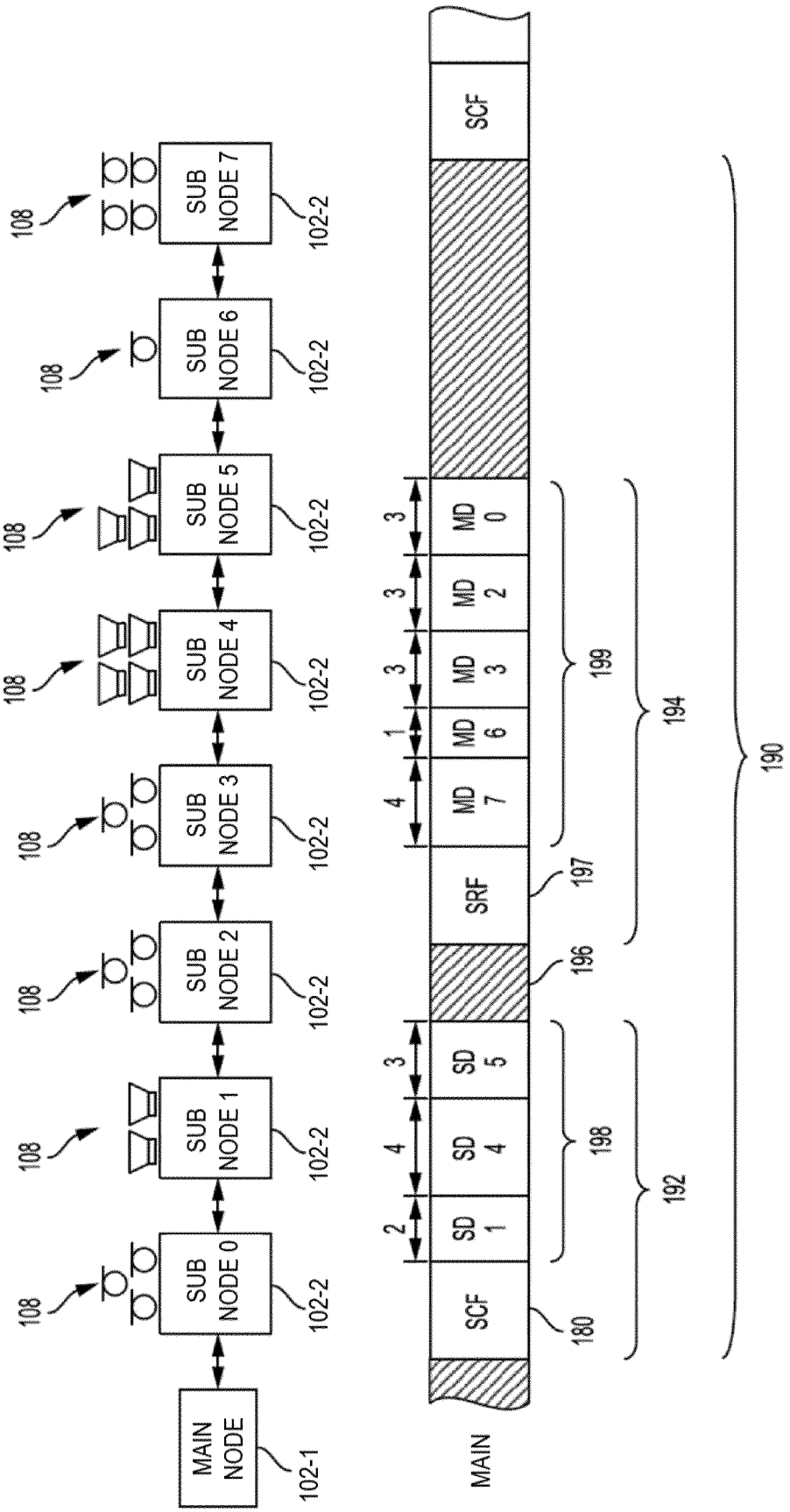
MAIN NODE
102-1
SUB NODE 0
SUB NODE 1
SUB NODE 2
SUB NODE 3
SUB NODE 4
SUB NODE 5
SUB NODE 6
SUB NODE 7
102-2
108
MAIN
SCF
SD 1
SD 4
SD 5
SRF
MD 7
MD 6
MD 3
MD 2
MD 0
2
4
3
1
180
196
197
198
199
192
194
190

FIG. 8

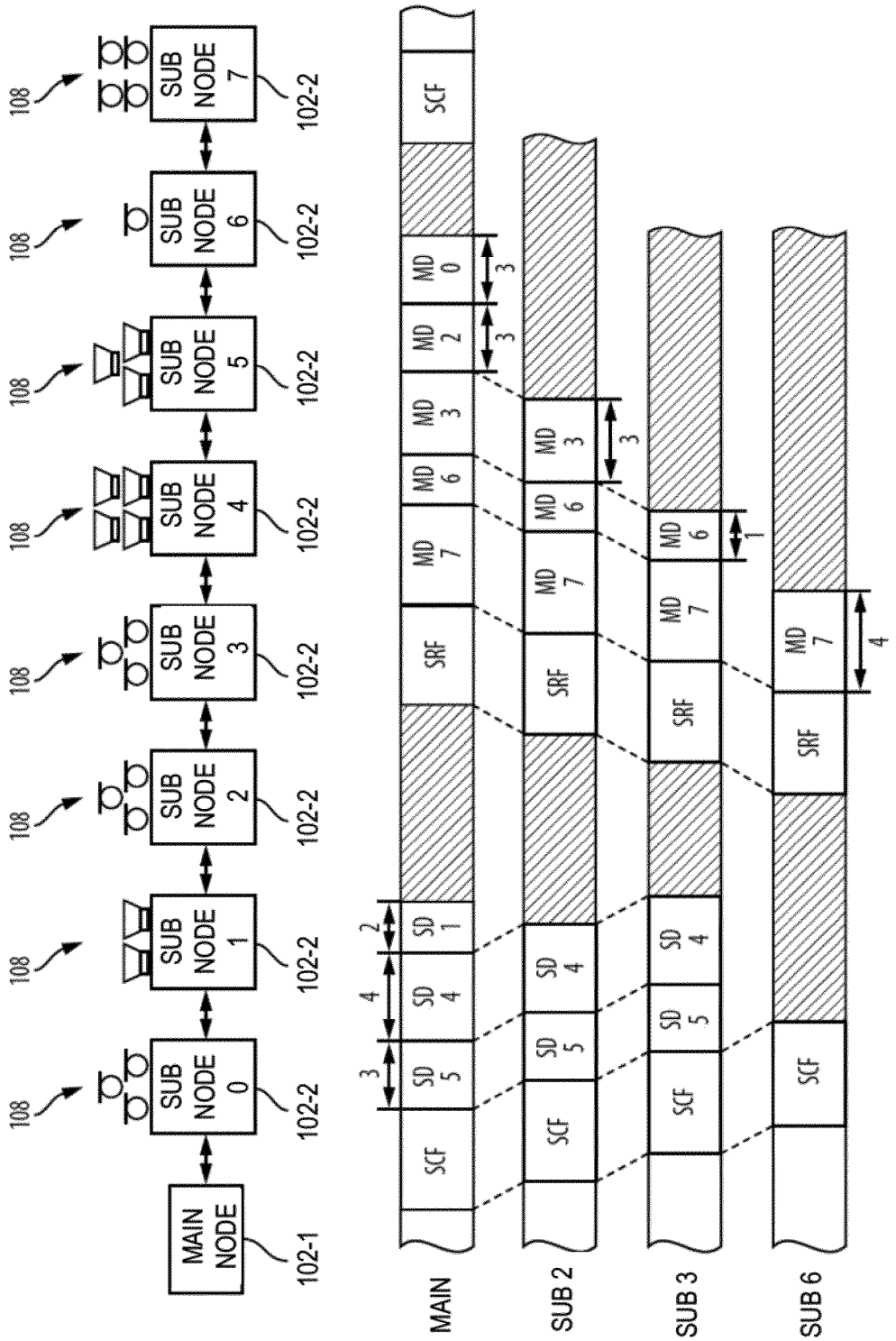
MAIN NODE
102-1
SUB NODE 0
SUB NODE 1
SUB NODE 2
SUB NODE 3
SUB NODE 4
SUB NODE 5
SUB NODE 6
SUB NODE 7
102-2
108
SCF
SD 5
SD 4
SD 1
SRF
MD 7
MD 6
MD 3
MD 2
MD 0
MAIN
SUB 2
SUB 3
SUB 6

FIG. 9

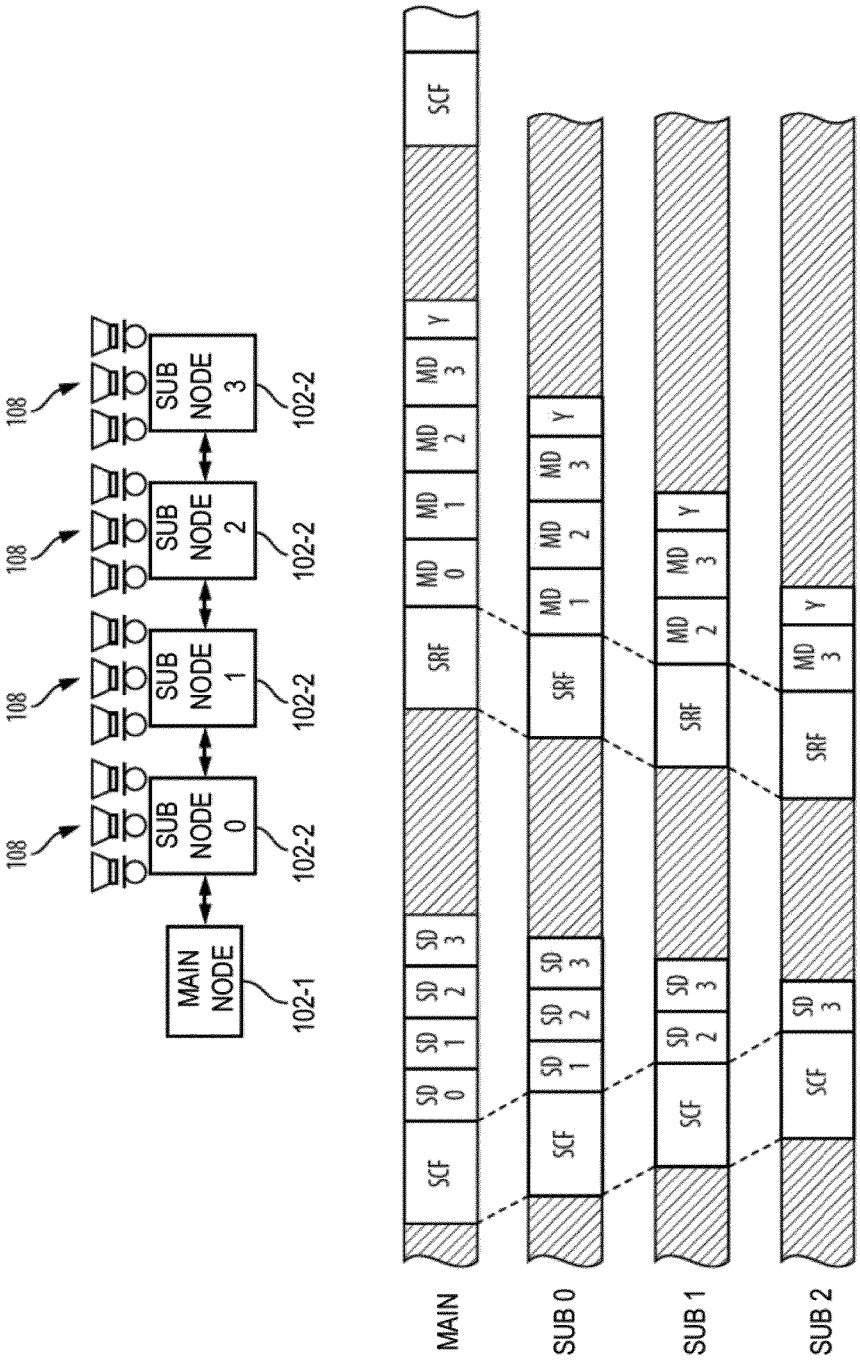
MAIN NODE
102-1
SUB NODE 0
SUB NODE 1
SUB NODE 2
SUB NODE 3
102-2
108
SCF
SD 0
SD 1
SD 2
SD 3
SRF
MD 0
MD 1
MD 2
MD 3
Y
MAIN
SUB 0
SUB 1
SUB 2

FIG. 10

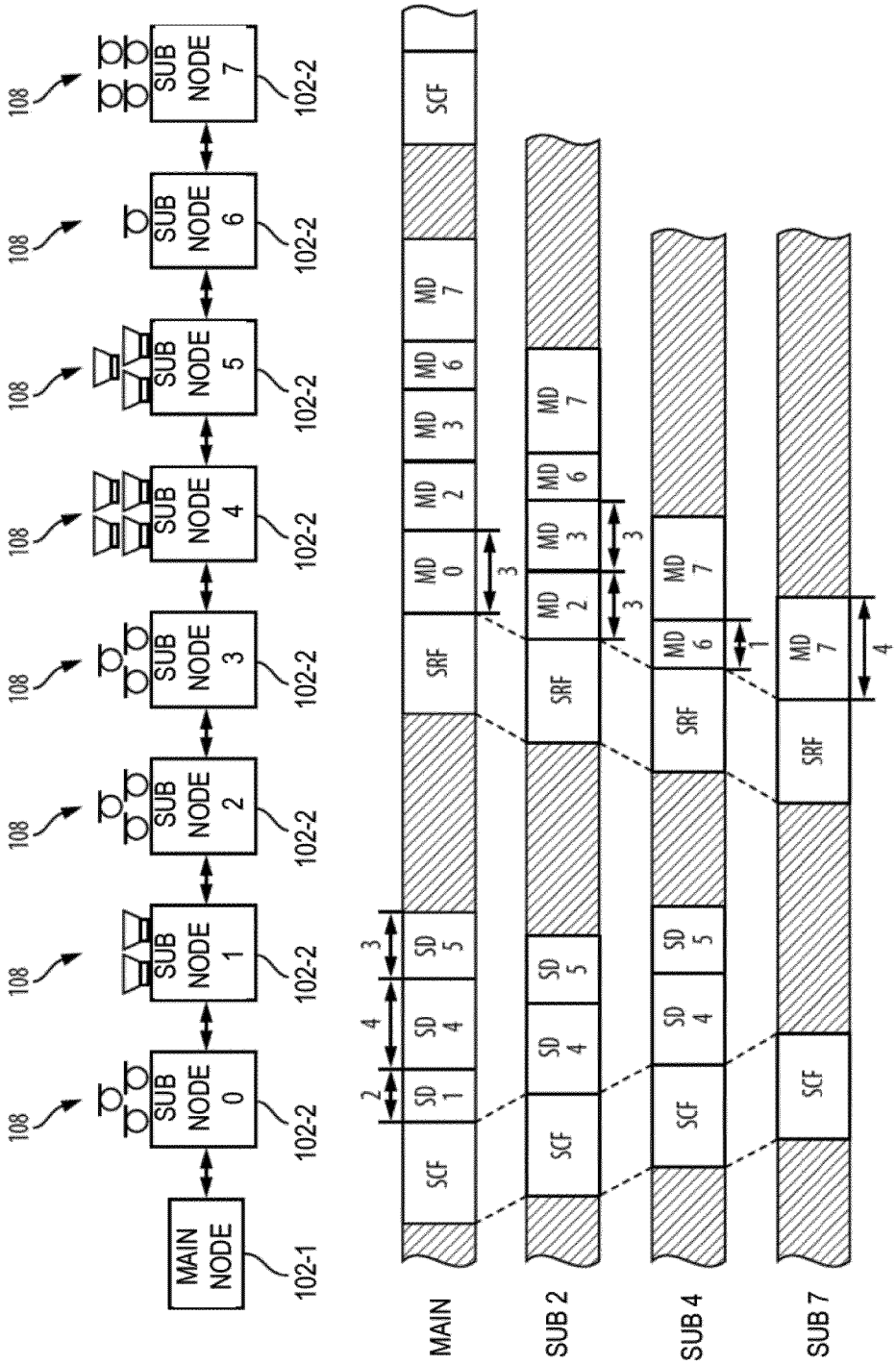
MAIN NODE
102-1
SUB NODE 0
SUB NODE 1
SUB NODE 2
SUB NODE 3
SUB NODE 4
SUB NODE 5
SUB NODE 6
SUB NODE 7
102-2
108
SCF
SD 1
SD 4
SD 5
SRF
MD 0
MD 2
MD 3
MD 6
MD 7
2
4
3
1
MAIN
SUB 2
SUB 4
SUB 7

FIG. 11

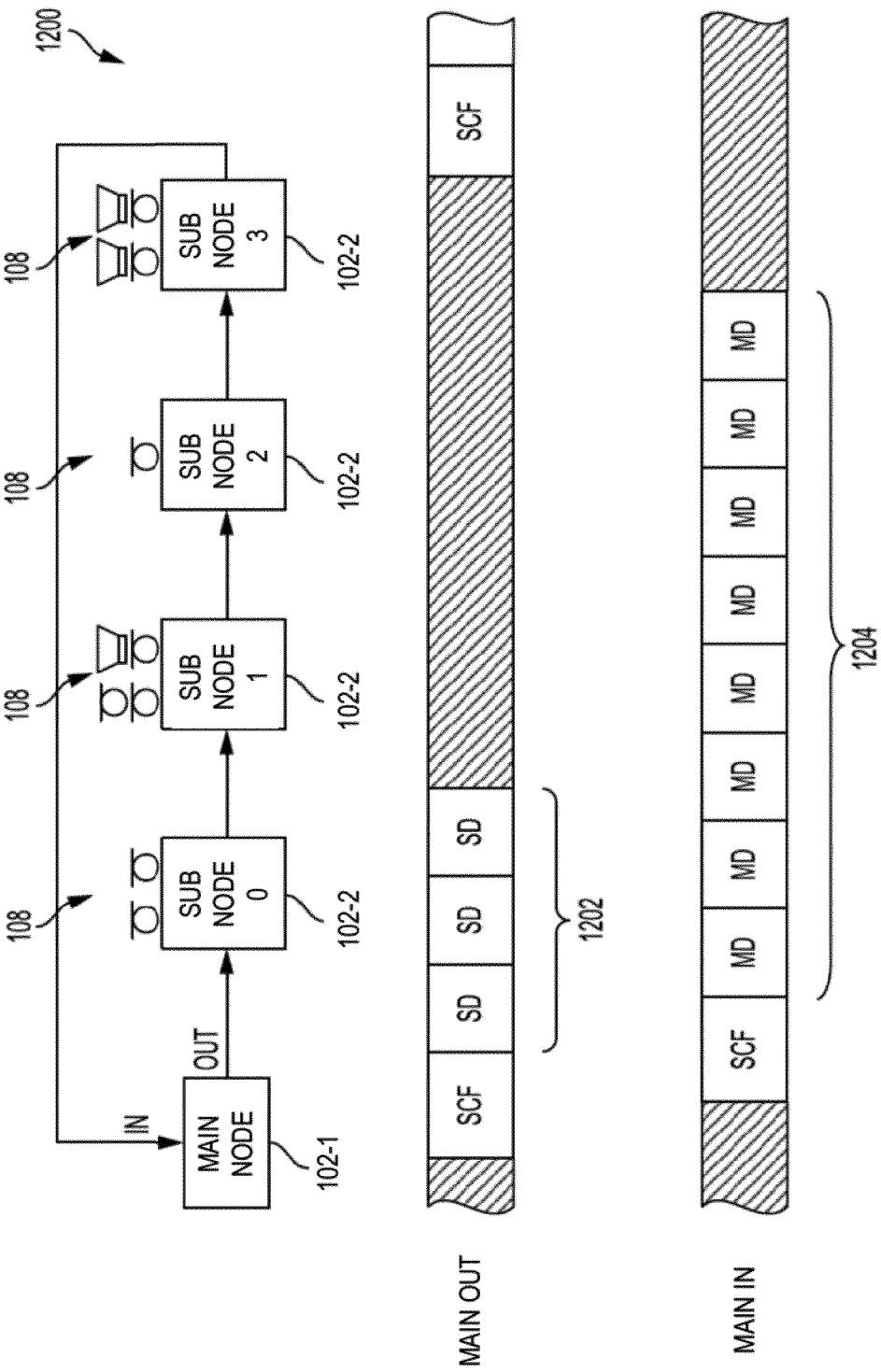
1200
MAIN NODE
102-1
IN
OUT
SUB NODE 0
SUB NODE 1
SUB NODE 2
SUB NODE 3
102-2
108
SCF
SD
1202
MAIN OUT
MD
1204
MAIN IN

FIG. 12

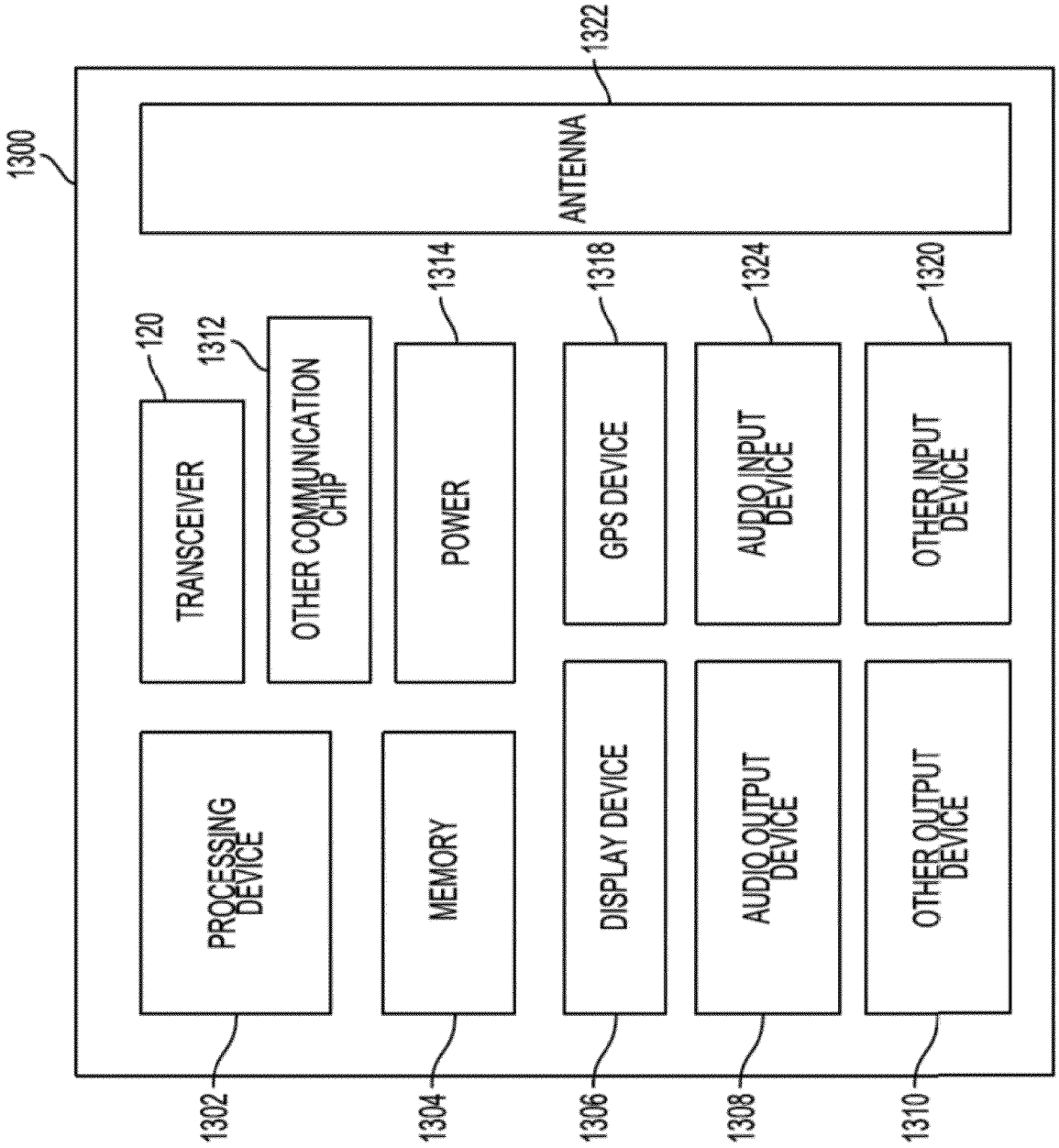
1300
1322
ANTENNA
1314
1318
1324
1320
120
1312
TRANSCEIVER
OTHER COMMUNICATION CHIP
POWER
GPS DEVICE
AUDIO INPUT DEVICE
OTHER INPUT DEVICE
PROCESSING DEVICE
MEMORY
DISPLAY DEVICE
AUDIO OUTPUT DEVICE
OTHER OUTPUT DEVICE
1302
1304
1306
1308
1310

FIG. 13

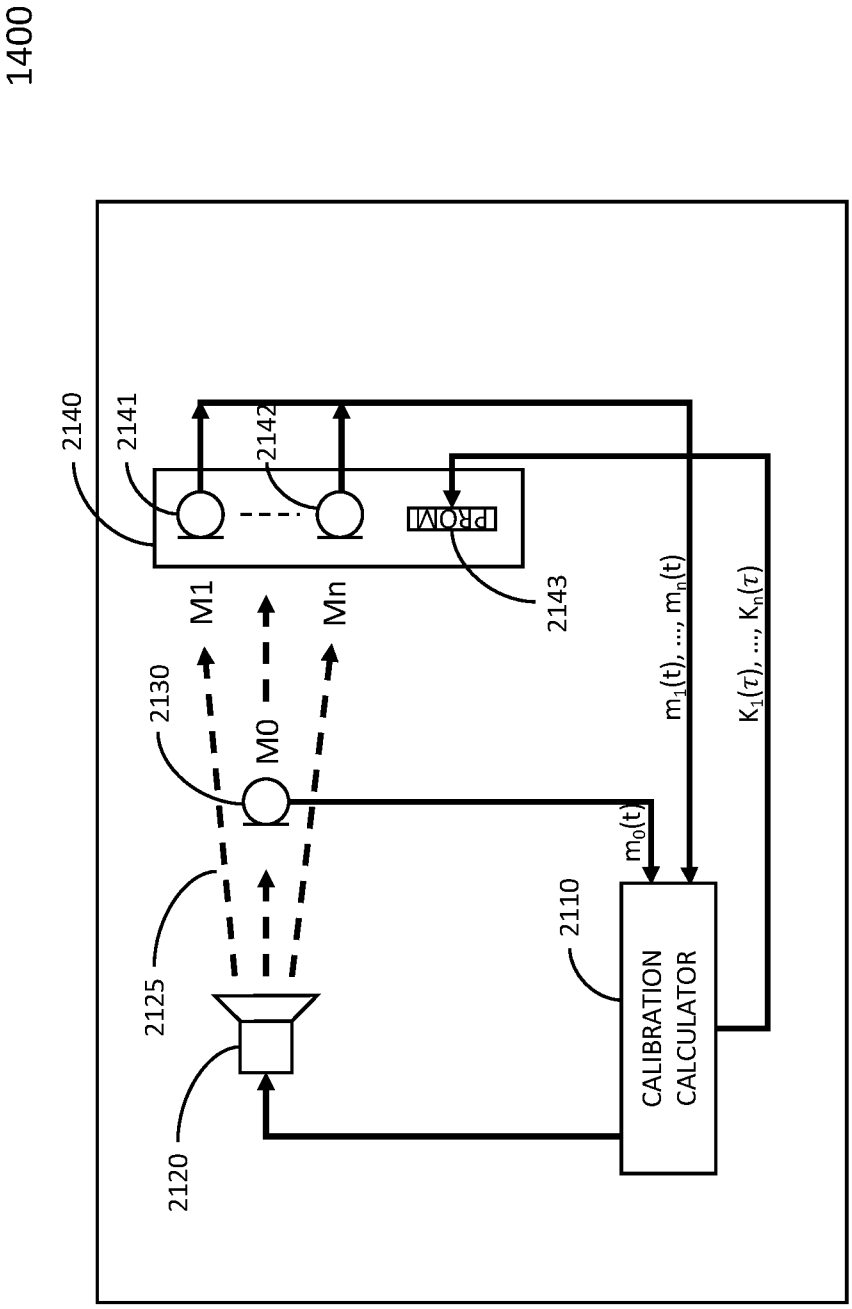
1400
2140
2141
2142
PROM
2143
M1
Mn
M0
2130
2125
2120
2110
CALIBRATION CALCULATOR
$m_0(t)$
$m_1(t), ..., m_n(t)$
$K_1(\tau), ..., K_n(\tau)$

FIG. 14

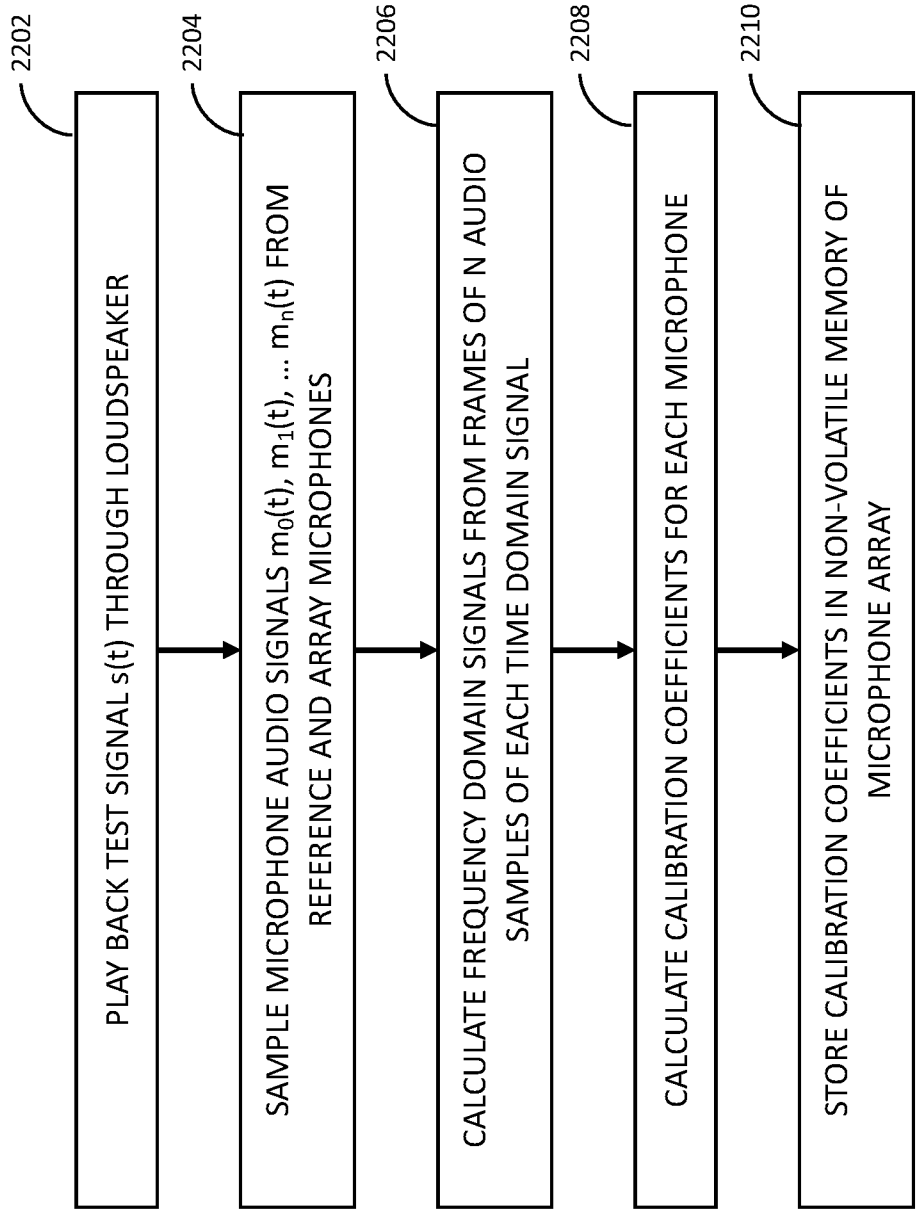
2200
2202
PLAY BACK TEST SIGNAL s(t) THROUGH LOUDSPEAKER
2204
SAMPLE MICROPHONE AUDIO SIGNALS $m_0(t)$, $m_1(t)$, ... $m_n(t)$ FROM REFERENCE AND ARRAY MICROPHONES
2206
CALCULATE FREQUENCY DOMAIN SIGNALS FROM FRAMES OF N AUDIO SAMPLES OF EACH TIME DOMAIN SIGNAL
2208
CALCULATE CALIBRATION COEFFICIENTS FOR EACH MICROPHONE
2210
STORE CALIBRATION COEFFICIENTS IN NON-VOLATILE MEMORY OF MICROPHONE ARRAY

FIG. 15

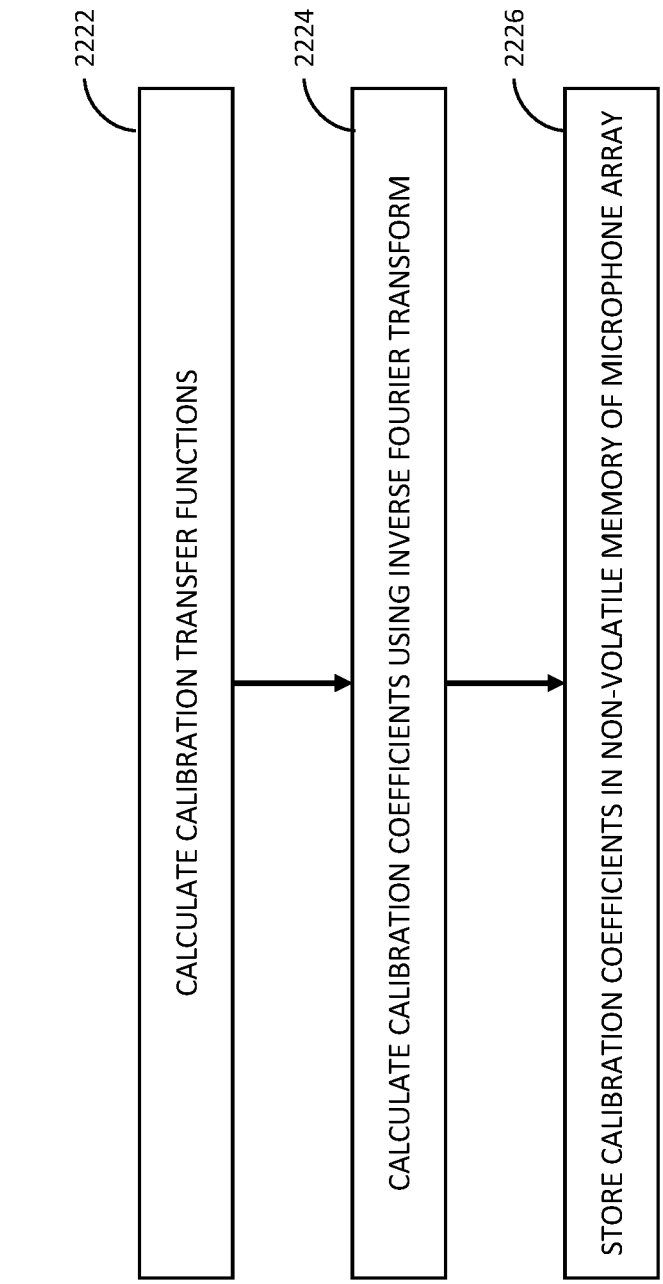
2222
2224
2226
CALCULATE CALIBRATION TRANSFER FUNCTIONS
CALCULATE CALIBRATION COEFFICIENTS USING INVERSE FOURIER TRANSFORM
STORE CALIBRATION COEFFICIENTS IN NON-VOLATILE MEMORY OF MICROPHONE ARRAY
2220

FIG. 16

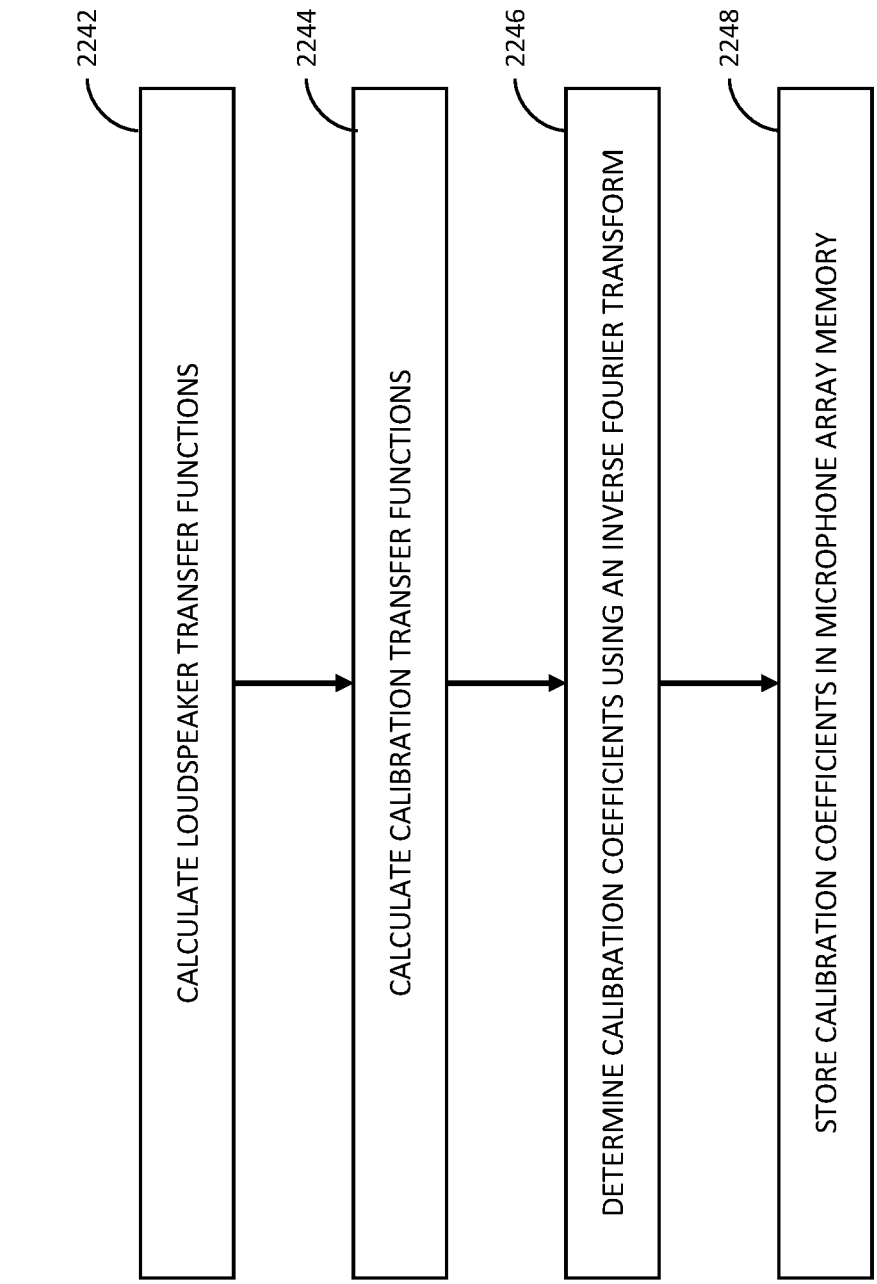
2240
2242
CALCULATE LOUDSPEAKER TRANSFER FUNCTIONS
2244
CALCULATE CALIBRATION TRANSFER FUNCTIONS
2246
DETERMINE CALIBRATION COEFFICIENTS USING AN INVERSE FOURIER TRANSFORM
2248
STORE CALIBRATION COEFFICIENTS IN MICROPHONE ARRAY MEMORY

FIG. 17

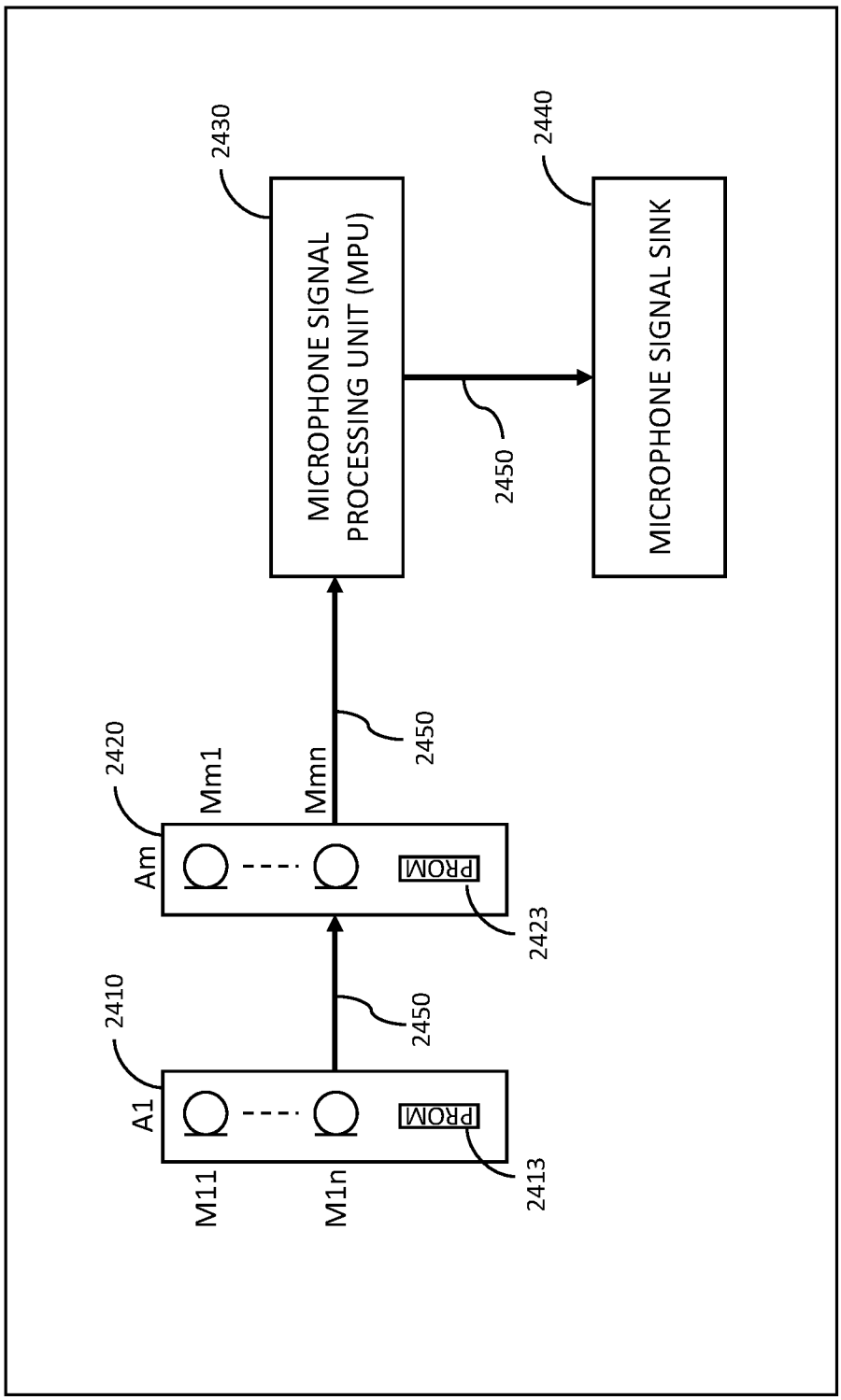
2400
2410
A1
M11
M1n
2413
PROM
2450
2420
Am
Mm1
Mmn
2423
2430
MICROPHONE SIGNAL PROCESSING UNIT (MPU)
2440
MICROPHONE SIGNAL SINK

FIG. 18

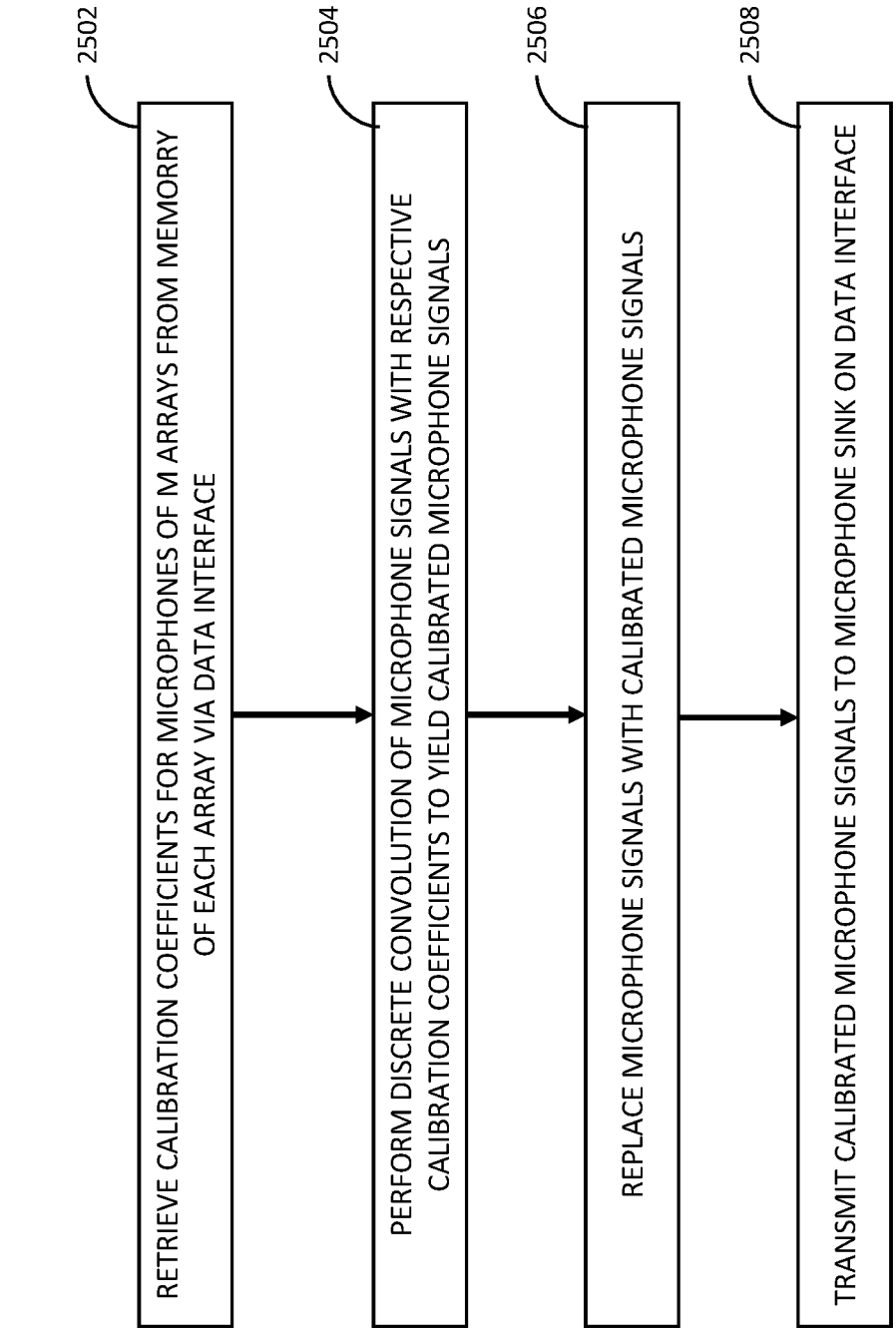
2500
2502
RETRIEVE CALIBRATION COEFFICIENTS FOR MICROPHONES OF M ARRAYS FROM MEMORY OF EACH ARRAY VIA DATA INTERFACE
2504
PERFORM DISCRETE CONVOLUTION OF MICROPHONE SIGNALS WITH RESPECTIVE CALIBRATION COEFFICIENTS TO YIELD CALIBRATED MICROPHONE SIGNALS
2506
REPLACE MICROPHONE SIGNALS WITH CALIBRATED MICROPHONE SIGNALS
2508
TRANSMIT CALIBRATED MICROPHONE SIGNALS TO MICROPHONE SINK ON DATA INTERFACE

FIG. 19

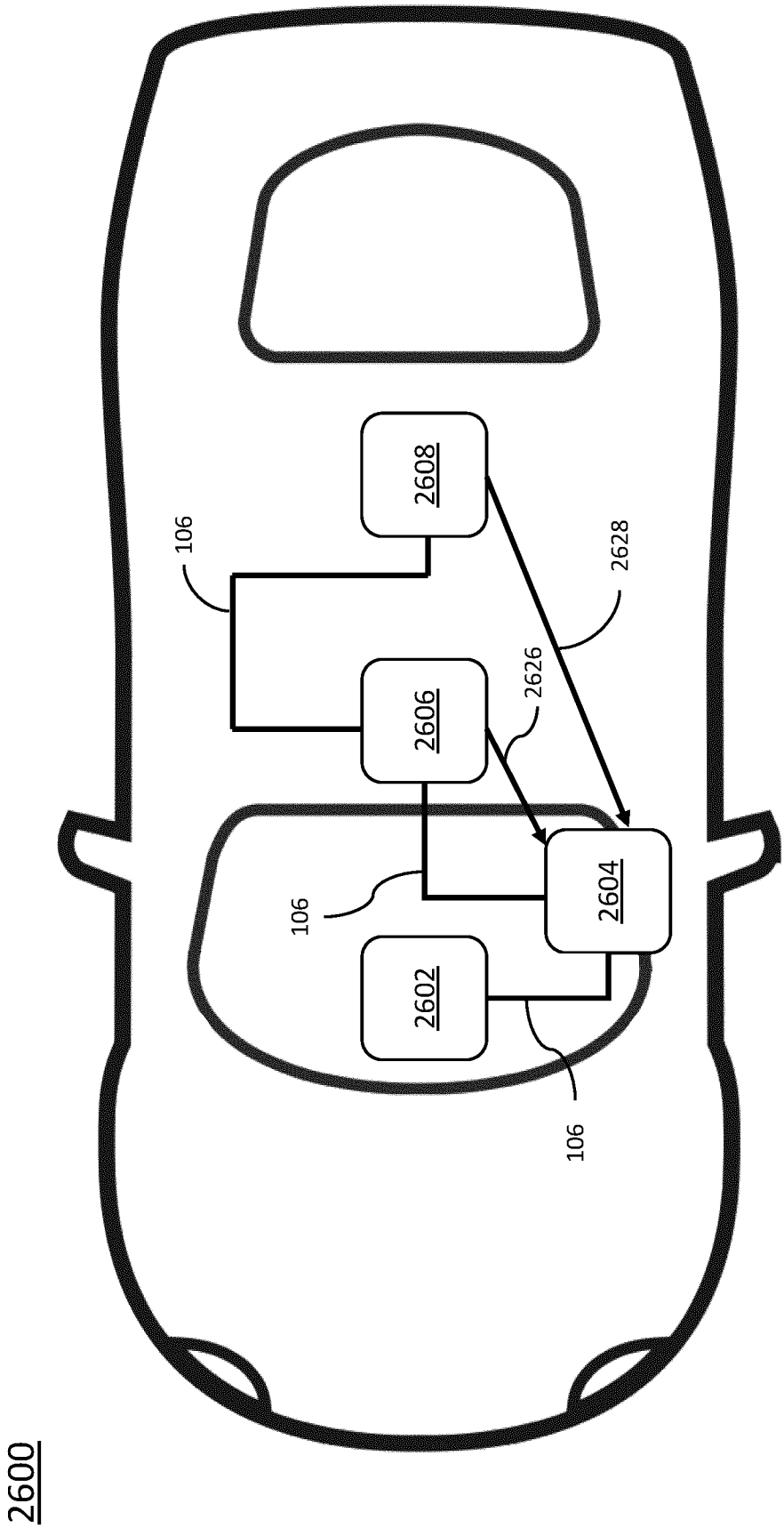

FIG. 20

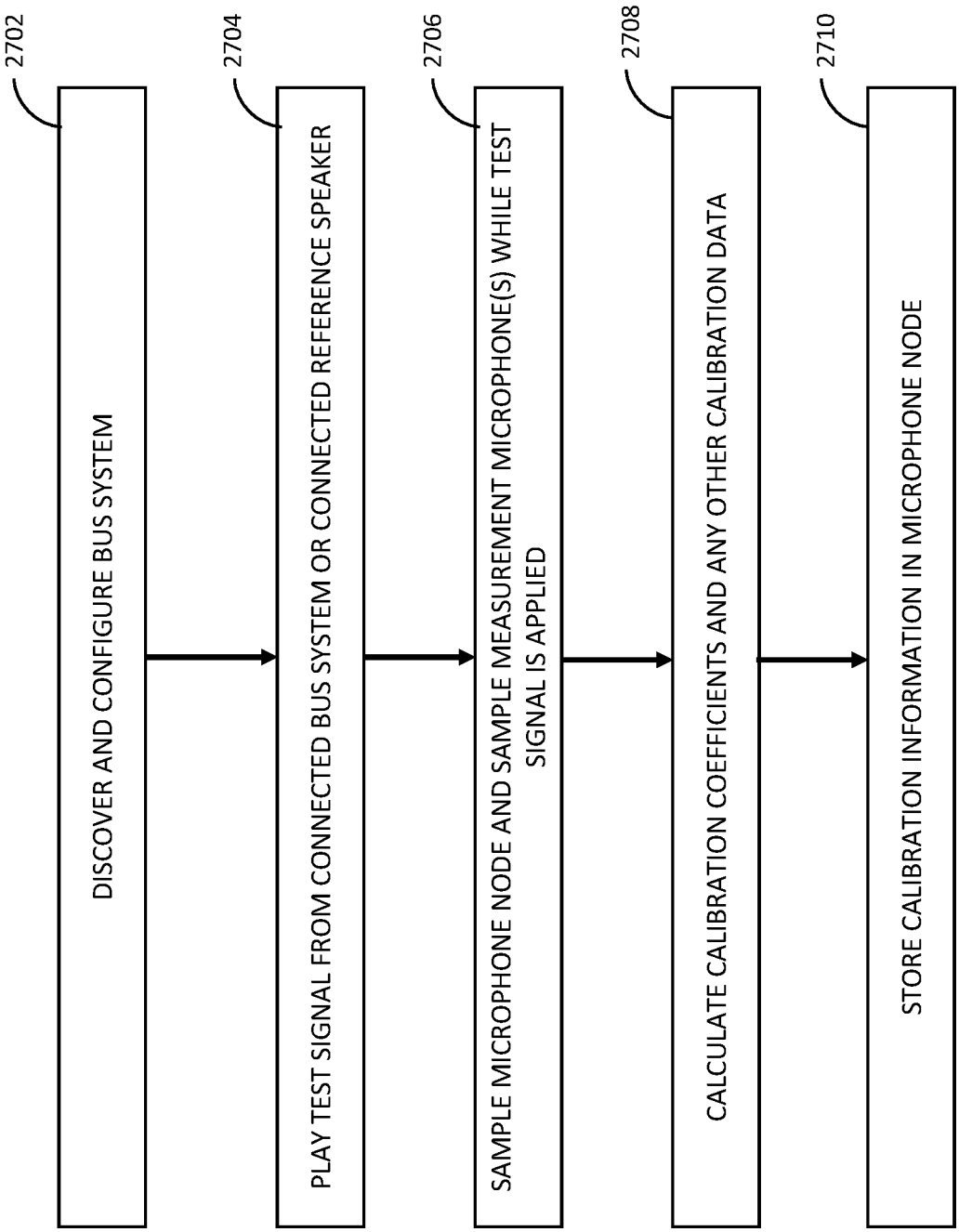
2700
2702
DISCOVER AND CONFIGURE BUS SYSTEM
2704
PLAY TEST SIGNAL FROM CONNECTED BUS SYSTEM OR CONNECTED REFERENCE SPEAKER
2706
SAMPLE MICROPHONE NODE AND SAMPLE MEASUREMENT MICROPHONE(S) WHILE TEST SIGNAL IS APPLIED
2708
CALCULATE CALIBRATION COEFFICIENTS AND ANY OTHER CALIBRATION DATA
2710
STORE CALIBRATION INFORMATION IN MICROPHONE NODE

FIG. 21

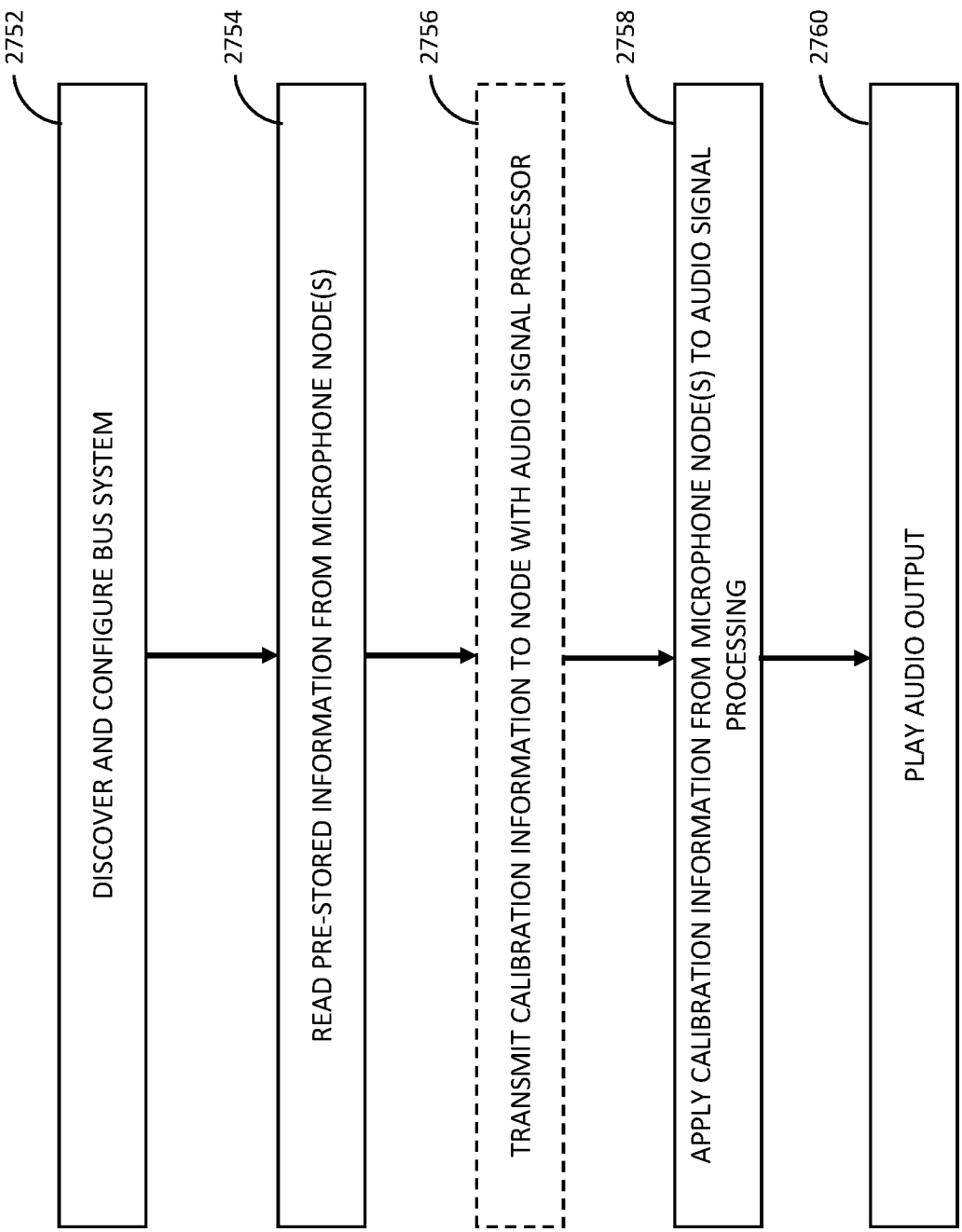
2750
2752
DISCOVER AND CONFIGURE BUS SYSTEM
2754
READ PRE-STORED INFORMATION FROM MICROPHONE NODE(S)
2756
TRANSMIT CALIBRATION INFORMATION TO NODE WITH AUDIO SIGNAL PROCESSOR
2758
APPLY CALIBRATION INFORMATION FROM MICROPHONE NODE(S) TO AUDIO SIGNAL PROCESSING
2760
PLAY AUDIO OUTPUT

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2021/081514

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04R3/00 H04R29/00 H04S7/00 H04R1/00 H04R1/32
H04R1/40 G06F13/00 H03K3/00 H04B3/00 H04J3/00
H04L7/00 H04L12/00 H04W4/00 H05B45/00 H04W36/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04R H04S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/260340 A1 (MAO XIADONG [US]) 8 November 2007 (2007-11-08) paragraphs [0025], [0055], [0056]; figures 1A, 1B, 3	1-20
X	US 2013/170666 A1 (NG SAMUEL SAMSUDIN [SG] ET AL) 4 July 2013 (2013-07-04) paragraphs [0008] - [0010], [0012], [0013], [0028] - [0031], [0036] - [0039], [0044], [0045]; figures 3, 4A, 4B	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 February 2022	18/02/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Radomirescu, B-M

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2021/081514

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007260340 A1	08-11-2007	CN 101484221 A	15-07-2009
		CN 101484933 A	15-07-2009
		CN 107638689 A	30-01-2018
		US 2007260340 A1	08-11-2007
US 2013170666 A1	04-07-2013	NONE	