(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 099 150 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
04.08.2004 Bulletin 2004/32

(21) Application number: **00927180.0**

(22) Date of filing: **01.05.2000**

(51) Int Cl.[7]: **G06F 1/24**

(86) International application number:
PCT/EP2000/004188

(87) International publication number:
WO 2000/072122 (30.11.2000 Gazette 2000/48)

(54) **RESET SYSTEM FOR MULTIPLE COMPONENT SYSTEM**

RÜCKSETZSYSTEM FÜR MEHRKOMPONENTENSYSTEM

SYSTEME DE REINITIALISATION POUR SYSTEME A PLUSIEURS CONSTITUANTS

(84) Designated Contracting States:
DE DK FR GB NL

(30) Priority: **21.05.1999 US 316783**

(43) Date of publication of application:
16.05.2001 Bulletin 2001/20

(73) Proprietor: **Koninklijke Philips Electronics N.V.**
5621 BA Eindhoven (NL)

(72) Inventors:
- **JENSEN, Rune, H.**
  NI-5656 AA Eindhoven (NL)
- **GARTLAN, Michael**
  NL-5656 AA Eindhoven (NL)

(74) Representative: **de Jong, Durk Jan et al**
Philips
Intellectual Property & Standards
P.O. Box 220
5600 AE Eindhoven (NL)

(56) References cited:
DE-A- 4 021 859
US-A- 5 086 505
US-A- 5 703 498

EP 1 099 150 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to the field of electronic systems, and in particular to systems comprising components having potentially different reset strategies.

2. Description of Related Art

[0002] To contain and potentially shorten the design and development cycle time for large scale systems, previously designed components, or modules, are commonly used. Such modules, having been designed for systems having differing requirements, often have differing clock and timing constraints. Some modules, for example, may employ a positive-edge-triggered clocking scheme, others may employ a negative-edge-triggered clocking scheme, while others may be level sensitive, multi-phased, and so on. In like manner, the convention used for resetting each module may differ. Asynchronous or synchronous reset strategies may be employed, and often a combination of both is common. For each module, the reset strategy employed introduces timing constraints relative to the particular clocking scheme employed. Examples of such timing constraints include: a synchronous reset must arrive at the module a specified duration before the active edge of the clock and/or be held at its active state for a specified duration after the clock edge; an asynchronous reset should not be released in close proximity to a change of clock state in a level sensitive clocking design; a reset signal should not be asserted, or de-asserted, in close proximity to an assertion or desertion of a set signal; and so on. From a systems viewpoint, the varying reset and clocking strategies produce a combinatorially complex set of design constraints.

[0003] To accommodate the varying clocking strategies among modules, conventional systems include a module-clock-generator that generates the various clocking signals, at appropriate frequency and phase relative to each other for proper system operation. Accommodation of the varying reset strategies is commonly somewhat less structured. Typically, because of the combinatorial nature of the problem, specific reset circuitry is designed for each module, or for each set of modules having a similar combination of reset and clock configurations. While the design of each reset circuit may not be unduly burdensome, the system level design task of properly defining, configuring, and testing each of these circuits can be significant.

[0004] US 5 703 498 A (FURTEK FREDERICK CURTIS ET AL) 30 December 1997 (1997-12-30), for example, shows a signal distribution architecture for clock and reset signal distribution in a programmable array including separate networks for distributing clock and reset signals to logic cells of an array.

[0005] The testing task for reset circuits is particularly burdensome because of the difficulties associated with timing related anomalies. In a well structured system design, the system designer strives to use synchronous functions and operations to minimize timing related problems. Because of the lack of standardization for reset strategies, and the variety of alternatives available, including asynchronous operation, the likelihood of a timing related error is high, and the cost of isolating and preventing the particular circumstances that produce the problematic timing sequences is high.

[0006] The use of specific, time-dependent, reset circuits also minimizes the likelihood that systems designed with such circuits will "scale" as technologies change, or as other features are added to the system. Similarly, the use of such a system as a future module in a larger system will only serve to exacerbate the problems associated with modules having differing reset strategies and timing constraints.

BRIEF SUMMARY OF THE INVENTION

[0007] It is an object of this invention to provide a reset architecture that provides for a reliable and robust system reset capability that is independent of the reset configurations used in the modules that comprise the system. It is another object of this invention to provide a reset architecture that is modular. It is another object of this invention to provide a reset architecture that is scalable. It is another object of this invention to provide a reset architecture that is easy to test. It is another object of this invention to provide a reset architecture that reduces the complexity associated with system tests.

[0008] These objects, and others, are achieved by providing a reset module that operates in conjunction with the system clock module to provide a combination of reset and clock assertions that can be relied upon to reset conventional processing modules having a variety of reset architectures. In a preferred embodiment, a reset command initiates an assertion of the reset signal and an activation of all clocks at the system level. After a predetermined number of clock cycles, the system level clocks are deactivated, and then the reset signal is de-asserted. By providing multiple clock cycles with the reset signal asserted, processing modules having either asynchronous and synchronous reset will be reset. By disabling the clocks before de-asserting the reset signal, the likelihood of a timing hazard caused by an interaction of the reset signal and a clocking signal is reduced or eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention is explained in further detail, and by way of example, with reference to the accompanying drawings wherein:

FIG. 1 illustrates an example block diagram of a processing system having a reset module in accordance with this invention.

FIG. 2 illustrates an example flow diagram of a controller and reset module for a processing system in accordance with this invention.

FIG. 3 illustrates an example timing diagram of a processing system in accordance with this invention.

DETAILED DESCRIPTION OF THE INVENTION

[0010] FIG. 1 illustrates an example block diagram of a processing system 100 having a reset module 150 in accordance with this invention. In addition to the reset module 150, the processing system 100 comprises a controller 110, a clock module 120, and one or more processing modules 131-133.

[0011] The processing modules 131-133 are used herein as paradigms for devices that perform some function in dependence upon a clocking signal 121-123, respectively, and which are responsive to a reset signal 151 that place the module into a known, or knowable, initial state. The processing device, for example, may be a state machine that is resettable to a predefined state, or to a state corresponding to an external parameter; it may be a printer controller that initiates a sequence of commands to place the print head of a printer into a known state, at a known physical location; a CD player controller that reads the contents of the currently loaded disk and present a menu for selection by a user; and so on.

[0012] The clock module 120 provides the necessary module-clock signals 121-123 for each of the processing modules 131-133. Conventionally, the clock module 120 provides these module-clock signals 121-123 based upon a common master clock signal 101, to facilitate synchronization and other time related operations. In accordance with this invention, the generation of the module-clock signals 121-123 is also dependent upon a clock enable signal 111 that is provided by the controller 110.

[0013] The controller 110 operates in conjunction with the reset module 150 and clock module 120 as follows. Upon receipt of a reset command 105, the reset module 150 asserts the reset signal 151, and the controller 110 asserts the clock enable signal 111. Once asserted, the reset module 150 is configured, in accordance with this invention, to keep the reset signal 151 asserted until the clock enable signal 111 is de-asserted, using, for example a set-reset bistable device (SR-flip-flop). The controller 110 is configured, in accordance with this invention, to assert the clock enable signal 111 for a predetermined number of cycles of the master clock 101. This predetermined number of cycles is at least as great as the largest of the minimum number of master clock cycles required to initialize each processing module 131-133. That is, for example, if the minimum number of clock cycles required to initialize modules 131, 132, and 133 is three, zero, and two clock cycles, the controller 110 asserts the clock enable signal 111 for at least three clock cycles. In accordance with a preferred embodiment of this invention, recognizing that the speed of a reset operation is not typically a significant performance parameter, the predetermined number of cycles for asserting the clock enable signal is chosen to be a number that is greater than the minimum requirement. In accordance with another aspect of this invention, the predetermined number of cycles for asserting the clock enable signal is chosen to be a number that is substantially greater than an expected minimum requirement, thereby allowing for a large margin for the addition of other, as yet unknown, processing module, or allowing for the use of the controller 110 and reset module 150 for other processing systems. In a common embodiment of this invention, the predetermined number of cycles for asserting the clock enable signal 111 is chosen to be 256.

[0014] The controller 110 de-asserts the clock enable signal 111 after the predetermined number of master clock 101 cycles. As noted above, the reset module 150 is configured to de-assert the reset signal 151 after receiving this de-assertion of the clock enable signal 111. In a preferred embodiment of this invention, the reset signal 151 is de-asserted after a minimum time duration from the de-assertion of the clock enable signal 111, to allow for reset hold time durations, if any, of the processing modules 131-133.

[0015] FIG. 2 illustrates an example flow diagram for a processing system having a reset module in accordance with this invention. This flow diagram is effected upon receipt of a reset command, which may be explicit or implicit; an explicit reset is, for example, a reset that is initiated by a user, while an implicit reset is, for example, one that is initiated when power is first applied to the system. In response to the reset command, the reset signal is asserted and communicated to each of the processing modules, at 210. This signal remains asserted until explicitly de-asserted, at 250. At 220, the clock-enable signal is asserted and communicated to the clock module, in response to which the clock module provides the individual clock signals to each processing module. At 230, the controller waits for a predetermined number of clock cycles, as discussed above. Thereafter, the clock-enable signal is de-asserted, at 240, in response to which the clock module ceases the individual clock signals to each processing module. After the clocks are ceased, the reset signal is de-asserted, at 250, and the normal system operations are resumed, at 260.

[0016] FIG. 3 illustrates an example timing diagram of a processing system in accordance with this invention, using the same reference numerals as the corresponding signals in FIG. 1. Line 3A illustrates an example reset command 105, which as mentioned above, may be explicit or implicitly generated. Line 3B illustrates an ex-

ample master clock signal 101, which is typically generated by a free running crystal oscillator or other source using techniques common in the art. In accordance with this invention, in response to the asserted reset command at 301, the reset signal 151 is asserted, at 305. In the example timing diagram of FIG. 3, the assertion 305 of the reset signal 151 is synchronous with the master clock 101, but the assertion 305 may occur asynchronously as well. Also in response to the assertion of the reset command at 301, the clock-enable signal 111 is asserted, at 306. Because the clock-enable signal 111 is related to clock generation based on the master clock 101, the clock-enable signal 111 in a preferred embodiment is synchronous with the master clock 101. Following conventional hazard-avoidance design practice, the clock-enable signal 111 preferably occurs during an inactive period of the master clock 101. Illustrated at 3D, the clock-enable signal 111 occurs a short time duration after a rising edge 303 of the master clock 101 and before the next falling edge 304. Thereafter, the clock module 120 of FIG. 1 generates the appropriate module-clock signals 121, 122, and any others. The particular frequency and phase of each module-clock signal is determined by the requirements of the individual processing modules in the system and the overall system timing constraints, using common system design techniques.

[0017] After N 315 cycles of the master clock 101, the clock-enable signal 111 is de-asserted, terminating the generation of module-clock signals 121, 122, and any others. As above, the de-assertion 307 of the clock-enable signal 111 is preferably synchronous with the master clock 101 and occurs during an inactive period of the master clock 101. In response to the de-assertion 307 of the clock-enable signal 111, the reset signal 151 is de-asserted, at 308. As noted above, the de-assertion of the reset signal 151 in a preferred embodiment occurs after some minimum time duration after the de-assertion of the clock-enable signal 111, to avoid any potential hazards caused by a race between the clock-enable signal 111, the reset signal 151, and the master clock 101.

[0018] Illustrated in FIG. 3, at 320, the clock-enable signal 111 is re-asserted some time after the reset signal 151 is de-asserted, thereby allowing the system 100 of FIG. 1 to resume normal operation after the above described reset process. In a preferred embodiment, the time duration between the de-assertion 308 of the reset signal 151 and the resumption 320 of normal operations is at least one cycle of the master clock 101, but can be more, depending upon an anticipated delay time required for the processing modules 131-133 to properly complete their reset processes.

[0019] The foregoing merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention. For example, the signals of FIG. 3 are illustrated as being active-high. Some systems 100 or modules 131-133 may employ active-low signaling; the addition of inverters to effect the appropriate operations within each system or module would be evident to one of ordinary skill in the art. In an alternative embodiment, for example, the reset module 150 may be configured to provide both an active high and an active low reset signal 151, and the appropriately phased reset signal provided to each processing module 131-133. The particular configurations and structures are provided in FIG. 1 for illustration only. Alternative configurations, such as the incorporation of the clock module 120 within the controller 110, would be evident to one of ordinary skill in the art. The functional blocks may be implemented in hardware, software, or a combination of both. For example, the functions of the controller 110 may be embodied in programming code that is executed in an embedded processor, or programming code that effects the creation of a programmed logic array that operates as a state machine to effect the required functions. These and other system implementation and optimization techniques will be evident to one of ordinary skill in the art in view of this invention, and within the intended scope of the following claims.

Claims

1. A processing system (100) comprising:

at least one processing module (131) that is responsive to a module-clock signal (121) and a reset signal (151), wherein the processing module (131) is initialized to an initial state in response to an assertion of the reset signal (151), and performs a processing function in dependence upon a de-assertion of the reset signal (151),
a clock module (120) that provides the module-clock signal (121) in dependence upon a master-clock signal (101) and an assertion of a clock-enable signal (111),
a controller (110) that provides the assertion of the clock-enable signal (111) in dependence upon a reset command (105), and
a reset module (150) that provides the assertion of the reset signal (151) in response to the reset command (105) and provides the de-assertion of the reset signal (151) in response to a de-assertion of the clock-enable signal (111),

wherein

the controller (110) provides the de-assertion of the clock-enable signal (111) after a number of cycles of the master-clock signal (101).

2. The processing system (100) of claim 1, wherein

the number of cycles of the master-clock signal (101) is dependent upon a time required to effect the initial state of the at least one processing mod-

ule (131).

3. The processing system (100) of claim 1, wherein the number of cycles of the master-clock signal (101) is a predetermined number that is substantially larger than an expected number of cycles of the master-clock signal (101) to effect the initial state of the at least one processing module (131).

4. The processing system (100) of claim 1, wherein the de-assertion of the reset signal (151) occurs a time duration after the de-assertion of the clock-enable signal that is greater than a hold time duration associated with the at least one processing module (131).

5. A method of resetting a plurality of processing modules, the method comprising:

asserting (210) a reset signal in response to a reset command,
enabling (220) one or more clocks used by the plurality of processing modules for a predetermined number of cycles of a master clock, and thereafter
disabling (240) the one or more clocks, and
de-asserting (250) the reset signal.

6. The method of claim 5, wherein the predetermined number of cycles of the master clock is dependent upon a reset characteristic of at least one of the plurality of processing modules.

7. The method of claim 5, wherein the predetermined number of cycles of the master clock is independent of a reset characteristic of the plurality of processing modules.

Patentansprüche

1. Verarbeitungssystem (110) mit:

mindestens einem Verarbeitungsmodul (131), das auf ein Modultaktsignal (121) und ein Reset-Signal (151) reagiert, wobei das Verarbeitungsmodul (131) in Reaktion auf die Aktivierung des Reset-Signals (151) in einen Anfangszustand versetzt wird und in Abhängigkeit von einer Deaktivierung des Reset-Signals (151) eine Verarbeitung vornimmt,
einem Taktmodul (120), das das Modultaktsignal (121) in Abhängigkeit von einem Mastertaktsignal (101) und einer Aktivierung eines Taktfreigabesignals (111) liefert,
einem Controller (110), der die Aktivierung des Taktfreigabesignals (111) in Abhängigkeit von einem Reset-Befehl (105) liefert, und
einem Reset-Modul, das die Aktivierung des Reset-Signals (151) in Reaktion auf den Reset-Befehl (105) liefert und die Deaktivierung des Reset-Signals (151) in Reaktion auf eine Deaktivierung des Taktfreigabesignals (111) schafft,

wobei
der Controller (110) nach einer Anzahl von Zyklen des Mastertaktsignals (101) für die Deaktivierung des Taktfreigabesignals (111) sorgt.

2. Verarbeitungssystem (100) nach Anspruch 1, wobei
die Anzahl von Zyklen des Mastertaktsignals (101) von der Zeit abhängig ist, die benötigt wird, um mindestens ein Verarbeitungsmodul (131) in den Anfangszustand zu bringen.

3. Verarbeitungssystem (100) nach Anspruch 1, wobei
die Anzahl von Zyklen des Mastertaktsignals (101) eine vorgegebene Zahl ist, die wesentlich größer als die erwartete Anzahl von Zyklen des Mastertaktsignals (101) ist, um mindestens ein Verarbeitungsmodul (131) in den Anfangszustand zu bringen.

4. Verarbeitungssystem (100) nach Anspruch 1, wobei
die Deaktivierung des Reset-Signals (151) eine Zeitspanne nach der Deaktivierung des Taktfreigabesignals auftritt, die größer ist als die zu dem mindestens einen Verarbeitungsmodul (131) gehörende Haltedauer.

5. Verfahren zum Rücksetzen einer Vielzahl von Verarbeitungsmodulen, wobei das Verfahren Folgendes umfasst:

Aktivierung (210) eines Reset-Signals in Reaktion auf einen Reset-Befehl,
Freigabe (220) einer oder mehrerer Takte, die von der Vielzahl von Verarbeitungsmodulen für eine vorgegebene Anzahl von Zyklen eines Mastertaktes verwendet werden, und
anschließend
Sperrung (240) des einen Takts oder der mehreren Takte, und
Deaktivierung (250) des Reset-Signals.

6. Verfahren nach Anspruch 5, wobei die vorgegebene Anzahl von Zyklen des Mastertaktes von einer Reset-Eigenschaft von mindestens einem der Vielzahl von Verarbeitungsmodulen abhängt.

7. Verfahren nach Anspruch 5, wobei die vorgegebene Anzahl von Zyklen des Mastertaktes nicht von

einer Reset-Eigenschaft der Vielzahl von Verarbeitungsmodulen abhängt.

Revendications

1. Système de traitement (100) comprenant:

au moins un module de traitement (131) qui réagit à un signal d'horloge de module (121) et à un signal de réinitialisation (151) où le module de traitement (131) est initialisé à un état initial en réaction à une affirmation du signal de réinitialisation (151) et qui exécute une fonction de traitement dépendamment d'une non-affirmation du signal de réinitialisation (151),
un module d'horloge (120) qui fournit le signal d'horloge de module (121) dépendamment d'un signal d'horloge principale (101) et d'une affirmation d'un signal de validation d'horloge (111),
un contrôleur (110) qui fournit l'affirmation du signal de validation d'horloge (111) dépendamment d'une commande de réinitialisation (105), et
un module de réinitialisation (150) qui fournit l'affirmation du signal de réinitialisation (151) en réaction à la commande de réinitialisation (105) et qui fournit la non-affirmation du signal de réinitialisation (151) en réaction à la non-affirmation du signal de validation d'horloge (111),

où

le contrôleur (110) fournit la non-affirmation du signal de validation d'horloge (111) après un certain nombre de cycles du signal d'horloge principale (101).

2. Système de traitement (100) selon la revendication 1, où

le nombre de cycles du signal d'horloge principale (101) est dépendant d'un temps qui est nécessaire à effectuer l'état initial du au moins un module de traitement (131).

3. Système de traitement (100) selon la revendication 1, où

le nombre de cycles du signal d'horloge principale (101) est un nombre prédéterminé qui est sensiblement plus grand qu'un nombre attendu de cycles du signal d'horloge principale (101) pour effectuer l'état initial du au moins un module de traitement (131).

4. Système de traitement (100) selon la revendication 1, où

la non-affirmation du signal de réinitialisation (151) se présente pendant une durée après la non-affirmation du signal de validation d'horloge qui est supérieure à une durée de maintien de temps étant connexe à le au moins un module de traitement (131).

5. Procédé de réinitialisation d'une pluralité de modules de traitement, le procédé comprenant:

l'affirmation (210) d'un signal de réinitialisation en réaction à une commande de réinitialisation,
la validation (220) d'une ou de plusieurs horloges qui sont utilisées par la pluralité de modules de traitement pendant un nombre prédéterminé de cycles d'une horloge principale, et
après cela
la désactivation (240) d'une ou de plusieurs horloges, et
la non-affirmation (250) du signal de réinitialisation.

6. Procédé selon la revendication 5, où le nombre prédéterminé de cycles de l'horloge principale est dépendant d'une caractéristique de réinitialisation d'au moins une pluralité de modules de traitement.

7. Procédé selon la revendication 5, où le nombre prédéterminé de cycles de l'horloge principale est indépendant d'une caractéristique de réinitialisation de la pluralité de modules de traitement.

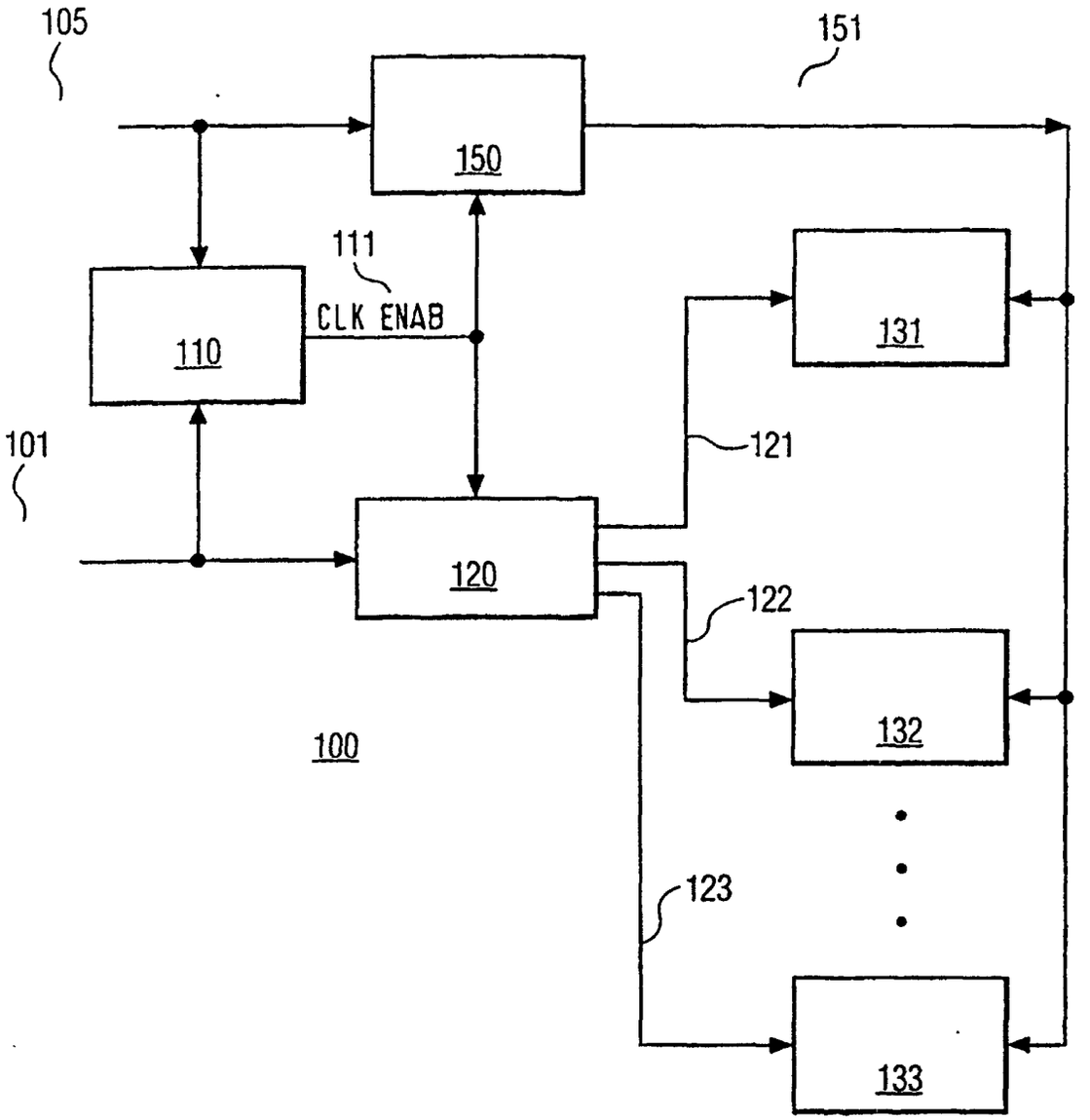

FIG. 1

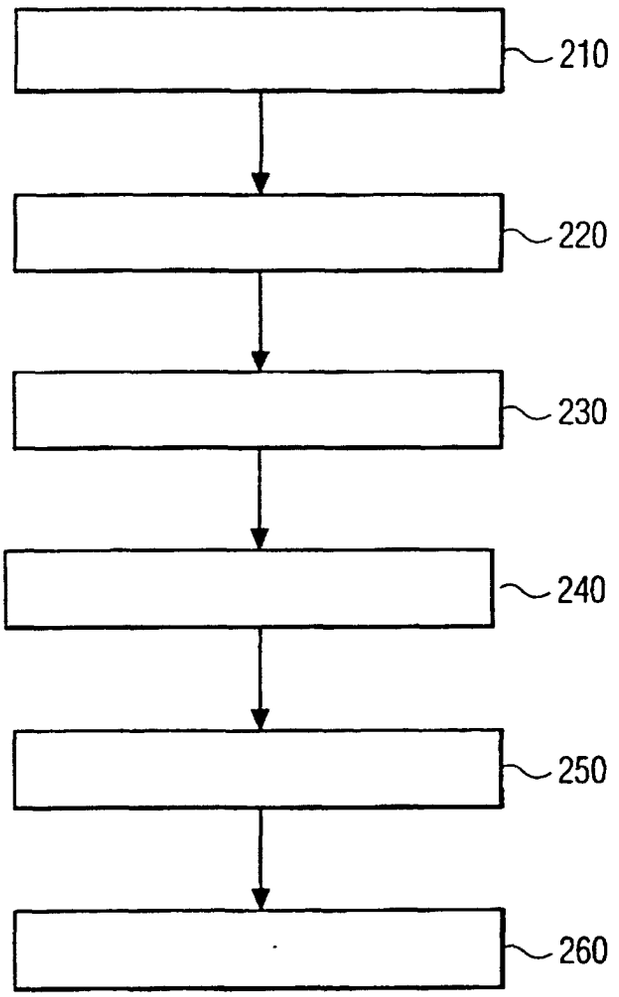

FIG. 2

FIG. 3A

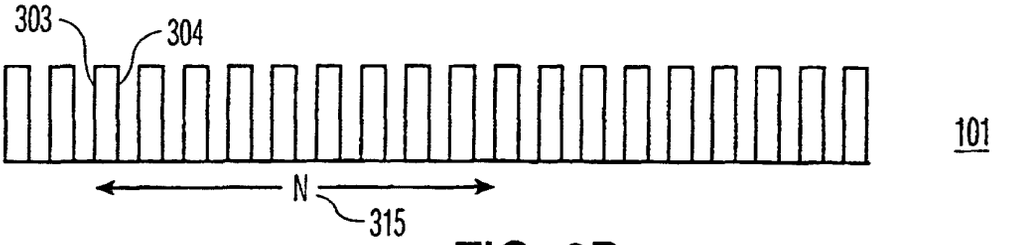

FIG. 3B

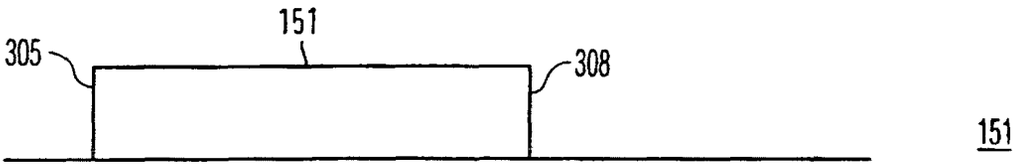

FIG. 3C

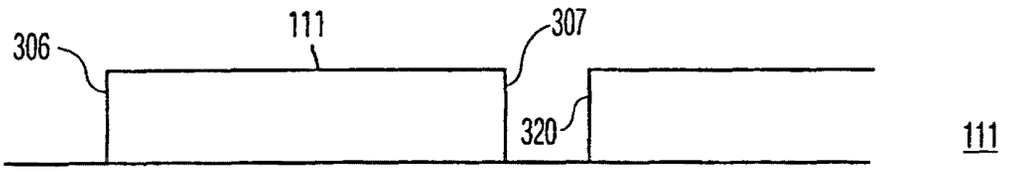

FIG. 3D

FIG. 3E

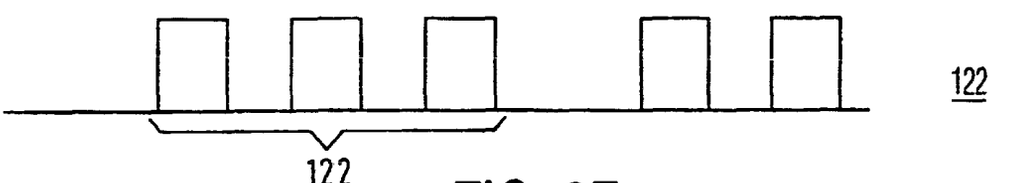

FIG. 3F