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(54) TRANSMITTING CIRCUIT, TRANSCEIVER, COMMUNICATION SYSTEM AND METHOD FOR TRANSMITTING DATA

SENDESCHALTUNG, SENDER/EMPFÄNGER, KOMMUNIKATIONSSYSTEME UND DATENÜBERTRAGUNGSVERFAHREN

CIRCUIT D'ÉMISSION, ÉMETTEUR-RÉCEPTEUR, SYSTÈME DE COMMUNICATION ET PROCÉDÉ DE TRANSMISSION DE DONNÉES

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(56) References cited:
EP-A1- 2 019 486
CN-A- 101 924 729
CN-A- 102 130 697
US-A1- 2011 122 972
WO-A2-2006/103585
CN-A- 102 098 255
CN-A- 102 148 789

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Description

TECHNICAL FIELD

[0001] The present invention relates to the field of communications, and in particular, to a transmitting circuit, a transceiver, a communication system, and a method for transmitting data.

BACKGROUND

[0002] A radio communication system has an increasingly higher requirement on bandwidth. An E-Band microwave technology has won popularity from a medium-and-long distance high-speed wireless point-to-point system because it has a bandwidth of 10 GHz (71-76 GHz and 81-86 GHz) and is in an atmospheric fading decline. With the upgrading of the technology and processing capabilities of chip, technologies such as a high-performance signal processing technology, and a high-spectral-efficiency modulation and coding technology all have come true, which all require the system to have a highly efficient analog to digital converter (ADC) and digital to analog converter (DAC).

[0003] Generally, an ADC/DAC bottleneck caused by a high bandwidth and high speed may be solved by using a time domain interleaved sampling method or a frequency domain multichannel sampling method. However, these two methods need complex post-processing on an output signal of the ADC/DAC, which degrades system performance.

[0004] In addition, the DAC tends to have a higher speed and a higher precision than the ADC. Therefore, a case where capabilities of the DAC and ADC are asymmetric generally occurs in a communication system. For example, an E-band with the bandwidth of 5 GHz imposes a minimum requirement of as a high as 10 Gsps on the ADC and the DAC, but the DAC is easier to meet such a high requirement because the processing speed of the DAC is higher than that of the ADC.

[0005] US 2011/122972 A1 discloses awireless communication system including a receiver 300 and a transmitter 400. The function of the transmitter 400 is similar to that of the receiver 300, but in reverse. Within digital section 401 of the transmitter 400, a summer 416 sums the N unconverted sample streams. The summed signal is then passed to a digital-to-analog converter (DAC) 420, which converts the sample stream to analog and provided an analog baseband signal comprising the N signals. Within the receiver 300, the combined signal sent from the transmitter 400 is converted to the digital domain by a single ADC. The DAC 420 of the transmitter 400 corresponds to only one ADC 350 of the receiver 300.

[0006] WO 2006/103585 A2 discloses a signal transmitter comprising a DSP block 10 for dividing the 4GHz baseband signal into N sub-bands, and N complex digital-to-analog converters (DAC) 12 are provided to convert the N sub-bands to the analogue domain. WO 2006/103585 A2 only disclose signal transmitters, does not discloses relationship of the DAC of the transmitter and the ADC of the receiver.

[0007] CN 102130697 A discloses downlink/uplink RF channel devices. The downlink RF channel device includes DAC, modulators, amplifiers, power amplifiers, etc., to support the multi-band bandwidth plus the bandwidth to meet the needs of a plurality of frequency bands digital pre-distortion required bandwidth. The uplink RF channel device includes ADC, a demodulator, amplifier, etc., to support the bandwidth to meet the needs of a plurality of multi-band digital band bandwidth plus the bandwidth required pre-distortion. However, in CN 102130697 A, each of the DAC of the transmitter corresponds to only one ADC of the receiver.

[0008] CN 101924729 A discloses a modulation method and apparatus. The modulation apparatus includes filters, DACs, multiplexers, and amplifiers. CN 101924729 A does not disclose relationship of the DAC of the transmitter and the ADC of the receiver.

[0009] CN 102 148 789 A discloses a method and device for receiving a multicarrier modulation signal. It discloses a multi-channel receiving method for reducing requirements on ADC sampling rate.

SUMMARY

[0010] Embodiments of the present invention provide a transmitting circuit, a transceiver, a communication system, and a method for transmitting data, which can reduce the processing complexity of the transceiver, thereby improving system performance.

[0011] In one aspect, a transceiver is provided, including a receiving circuit and a transmitting circuit, where the transmitting circuit includes: a digital interface circuit, configured to obtain, in a predetermined bandwidth, first data to be sent, and decompose the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer; a digital modulation circuit, configured to receive the N first sub digital signal flows, and modulate the N first sub digital signal flows to obtain N first modulated signals; a first frequency relocation circuit, configured to receive the N first modulated signals, and perform frequency relocation on the N first modulated signals, where there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation; a first synthesizer, configured to synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer smaller than or equal to N; a first digital to analog converter, configured to receive the first bandwidth signal, and perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal; and a first up-conversion circuit, configured to receive the first analog signal, and convert

the first analog signal into a radio frequency signal, so that the radio frequency signal is sent to a receiving circuit by an antenna.

[0012] The receiver circuit includes: a down-conversion circuit, configured to convert a radio frequency signal received on a receiving antenna into an analog signal; an intermediate frequency power divider, configured to decompose the analog signal into N parallel sub analog signal flows; a second frequency relocation circuit, configured to perform frequency relocation on the N parallel sub analog signal flows; N analog to digital converters, configured to perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows; a digital demodulation circuit, configured to perform demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals; and a digital interface circuit, configured to synthesize the N parallel demodulated signals into second data.

[0013] In another aspect, a method for communication is provided, including a method for receiving data and a method for transmitting data, the method for transmitting data includes: obtaining, in a predetermined bandwidth, first data to be sent, and decomposing the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer; modulating the N first sub digital signal flows to obtain N first modulated signals; performing frequency relocation on the N first modulated signals, where there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation; synthesizing M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer smaller than or equal to N; performing, by a first digital to analog converter, digital to analog conversion on the first bandwidth signal to obtain a first analog signal; and converting the first analog signal into a radio frequency signal, so that the radio frequency signal is sent to a receiving circuit by an antenna.

[0014] The method for receiving data includes: converting a radio frequency signal received on a receiving antenna into an analog signal; decomposing the analog signal into N parallel sub analog signal flows; performing frequency relocation on the N parallel sub analog signal flows; performing analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows; performing demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals; and synthesizing the N parallel demodulated signals into second data.

[0015] The transmitting circuit in the technical solution can decompose data into multiple parallel sub digital signal flows, perform modulation and frequency relocation on the multiple sub digital signal flows respectively, and then synthesize the multiple sub digital signal flows into a large bandwidth signal; further, the transmitting circuit converts the large bandwidth signal into an analog signal by using a digital to analog converter, and finally converts the analog signal into a radio frequency signal through up-conversion. Because the embodiments of the present invention can divide a large bandwidth into multiple sub-bands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the processing complexity, thereby improving system performance.

BRIEF DESCRIPTION OF DRAWINGS

[0016] To illustrate the technical solutions in the embodiments of the present invention more clearly, the following briefly introduces the accompanying drawings required for describing the embodiments of the present invention. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a schematic circuit diagram of a transmitting circuit according to a first embodiment of the present invention;

FIG. 2 is a schematic circuit diagram of a transmitting circuit according to a second embodiment of the present invention;

FIG. 3 is a schematic circuit diagram of a transmitting circuit according to a third embodiment of the present invention;

FIG. 4 is a schematic circuit diagram of a transmitting circuit according to a fourth embodiment of the present invention;

FIG. 5 is a schematic circuit diagram of a transceiver according to a fifth embodiment of the present invention;

FIG. 6 is a schematic circuit diagram of a communication system according to a sixth embodiment of the present invention;

FIG. 7A and FIG. 7B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to a seventh embodiment of the present invention;

FIG. 8A and FIG. 8B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to an eighth embodiment of the present invention;

FIG. 9A and FIG. 9B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to a ninth embodiment of the present invention;

FIG. 10 is a schematic circuit diagram of a transceiver according to a tenth embodiment of the present invention;

FIG. 11 is a schematic circuit diagram of a transceiver according to an eleventh embodiment of the present invention;

FIG. 12 is a schematic circuit diagram of a synthesizer according to an embodiment of the present invention;

FIG. 13 is a schematic flowchart of a method for transmitting data according to a twelfth embodiment of the present invention;

FIG. 14 is a schematic flowchart of a method for transmitting data according to a thirteenth embodiment of the present invention; and

FIG. 15 is a schematic flowchart of a communication method according to a fourteenth embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0017] The following clearly and completely describes the technical solutions in the embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are merely a part rather than all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0018] It should be understood that the technical solution of the present invention may be applied to various communication systems, for example, a GSM (Global System of Mobile communication, Global System of Mobile communication) system, a CDMA (Code Division Multiple Access, Code Division Multiple Access) system, a WCDMA (Wideband Code Division Multiple Access, Wideband Code Division Multiple Access) system, a GPRS (General Packet Radio Service, General Packet Radio Service), an LTE (Long Term Evolution, Long Term Evolution) system, an LTE-A (Advanced long term evolution, Long Term Evolution-Advanced) system, a UMTS (Universal Mobile Telecommunication System, Universal Mobile Telecommunication System), and the like.

[0019] The embodiments of the present invention may be applied to wireless networks of different standards. A radio access network may include different network elements in different systems. For example, network elements of the radio access network on LTE and LTE-A include an eNB (eNodeB, evolved base station), network elements of the radio access network on WCDMA include an RNC (Radio Network Controller, radio network controller) and a NodeB. Similarly, other wireless networks such as WiMAX (Worldwide Interoperability for Microwave Access, Worldwide Interoperability for Microwave Access) may also use a solution similar to that provided in the embodiments of the present invention, with only a slight difference in related modules of the base station system, which is not limited in the embodiments of the present invention.

[0020] The embodiments of the present invention provide an implementation solution of a high-speed millimetric wave (an E-Band in particular) system, which may be applied to a backhaul (backhaul) technology of microwave communication. The application scope of this implementation solution is not limited thereto according to the embodiments of the present invention, and the implementation solution may also be applied to other microwave or radio communication systems, for example, a wireless point-to-point system and the like.

[0021] When a time domain interleaved sampling method or a frequency domain multichannel sampling method is used to solve an ADC/DAC bottleneck caused by a high bandwidth and high speed, complex post-processing needs to be performed on an output signal of the ADC/DAC, and a transmitted signal is easily distorted, making it difficult to ensure system performance. The foregoing two methods have a very high requirement for DAC/ADC synchronization, which makes it more difficult to perform joint control on multiple DACs/ADCs.

[0022] FIG. 1 is a schematic circuit diagram of a transmitting circuit 100 according to a first embodiment of the present invention. The transmitting circuit 100 includes a digital interface circuit 110, a digital modulation circuit 120, a first frequency relocation circuit 130, a first synthesizer 140, a first digital to analog converter 150, and an up-conversion circuit 160.

[0023] The digital interface circuit 110 obtains, in a predetermined bandwidth, first data to be sent, and decomposes the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer. The digital modulation circuit 120 receives the N first sub digital signal flows, and modulates the N first sub digital signal flows to obtain N first modulated signals. The first frequency relocation circuit 130 receives the N first modulated signals, and performs frequency relocation on the N first modulated signals, where there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation. The first synthesizer 140 is configured to synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer. The first digital to analog converter 150 is configured to receive the first bandwidth signal, and perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal. The first up-conversion circuit 160 receives the first analog signal, and converts the first analog signal into a radio frequency signal, so that the radio frequency signal is sent by an antenna.

[0024] According to the embodiment of the present invention, a predetermined bandwidth can be divided into N subbands, and each subband is processed independently, that is, each subband is sent and received inde-

pendently. That is, N sub digital signal flows can be processed independently in a transmission channel of the transmitting circuit, and at least some sub digital signal flows of the N sub digital signal flows whose frequency bands are continuous are synthesized into one data flow. In addition, digital to analog conversion is performed on the data flow to obtain an analog signal; after the analog signal obtained by conversion is processed by using an analog circuit, the analog signal is sent through a transmitting antenna.

[0025] Specifically, at a transmitting end, the digital interface unit decomposes a single data flow or multiple data flows into multiple parallel data flows (that is, multiple sub digital signal flows). For example, the digital interface unit may decompose one piece of 4-bit data of a user into four 1-bit sub digital signal flows, or decompose two pieces of 2-bit data of a user into four 1-bit sub digital signal flows. Then, a digital modulator performs digital modulation on the N sub digital signal flows to obtain N first modulated signals with the same frequency. For example, the digital modulation circuit may perform modulation on the N sub digital signal flows respectively by using N FPGAs (Field Programmable Gate Arrays). The first frequency relocation circuit may perform frequency relocation on the N first modulated signals respectively by using N frequencies to obtain N modulated signals with continuous frequencies without a frequency band gap. For example, the first frequency relocation circuit may perform frequency relocation on the N first modulated signals by using N frequency mixers and corresponding N local oscillators. The first synthesizer synthesizes at least some modulated signals of the N modulated signals into a large bandwidth signal. A high-speed DAC performs digital to analog conversion on the large bandwidth signal, and sends the converted signal through the up-conversion circuit. Because each subband is processed independently at the transmitting end, each subband can be split at the receiving end by using a band-pass filter, and subbands are sampled by a low-speed ADC to obtain the sub digital signal flows; finally, digital modulation is performed on the sub digital signal of each subband independently.

[0026] It should be understood that bandwidths occupied by the first sub digital signal flows may be equal or unequal and M may be smaller than or equal to N. For example, when M is smaller than N, some sub digital signal flows are synthesized into a large bandwidth signal; when M is equal to N, all the sub digital signal flows are synthesized into a large bandwidth signal.

[0027] The transmitting circuit according to the embodiment of the present invention can decompose data into multiple parallel sub digital signal flows, perform modulation and frequency relocation on the multiple sub digital signal flows respectively, and then synthesize the multiple sub digital signal flows into a large bandwidth signal; further, the transmitting circuit converts the large bandwidth signal into an analog signal by using a digital to analog converter, and finally converts the analog signal into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0028] Because there is no frequency band gap between the multiple modulated signals that have undergone frequency relocation, spectral utilization is increased.

[0029] In addition, at the transmitting end, multiple subchannels use only one high-speed DAC and one analog intermediate frequency circuit, thereby saving devices and costs of the transmitting circuit.

[0030] According to the embodiment of the present invention, the first synthesizer 480 may include an adder, where the adder is configured to add the N first modulated signals that have undergone frequency relocation, to synthesize the modulated signals into a first bandwidth signal.

[0031] According to the embodiment of the present invention, N may be at least 4. The value of N is not limited thereto according to the embodiment of the present invention, and N may also be smaller than 4. In addition, the first data may be at least one binary digital signal flow.

[0032] FIG. 2 is a schematic circuit diagram of a transmitting circuit 200 according to a second embodiment of the present invention. The transmitting circuit provided in the embodiment in FIG. 2 may use more than two synthesizers and digital to analog converters.

[0033] The transmitting circuit in FIG. 2 includes a digital interface circuit 210, a digital modulation circuit 220, a first frequency relocation circuit 230, a first synthesizer 240, a first digital to analog converter 250, and an up-conversion circuit 260, which are similar to the digital interface circuit 110, the digital modulation circuit 120, the first frequency relocation circuit 130, the first synthesizer 140, the first digital to analog converter 150, and the up-conversion circuit 160 in FIG. 1 and are not further described herein.

[0034] The transmitting circuit 200 in FIG. 2 further includes a second synthesizer 270 and a second digital to analog converter 280.

[0035] The second synthesizer 270 synthesizes L first modulated signals of the N first modulated signals that have undergone frequency relocation into a second bandwidth signal, where the L first modulated signals are different from the M first modulated signals, that is, the L first modulated signals are signals other than the M first modulated signals of the N first modulated signals and L is a positive integer. The second digital to analog converter 280 receives the second bandwidth signal, and performs digital to analog conversion on the second bandwidth signal to obtain a second analog signal; the up-conversion circuit 260 is configured to receive the first

analog signal and the second analog signal, and synthesize the first analog signal and the second analog signal into a radio frequency signal.

[0036] For example, the first frequency relocation circuit may perform frequency relocation on the N first modulated signals respectively by using N frequencies with the same gap, so that bandwidths of the N first modulated signals that have undergone frequency relocation are continuous, that is, bandwidths of the N first modulated signals are adjacent. The first frequency relocation circuit may also perform frequency relocation on the L first modulated signals respectively by using L frequencies with the same gap, while perform frequency relocation on the M first modulated signals respectively by using M frequencies with the same gap. In this case, the first analog signal and the second analog signal may have bandwidth overlapping or a frequency gap.

[0037] Optionally, as another embodiment, the up-conversion circuit 160 may also perform frequency relocation on the first analog signal and the second analog signal respectively before synthesizing the first analog signal and the second analog signal into the radio frequency signal.

[0038] For example, in a case where the first analog signal and the second analog signal have bandwidth overlapping or a frequency band gap, frequency relocation may be further performed on the first analog signal and the second analog signal, so that the bandwidths of the first analog signal and the second analog signals that have undergone frequency relocation are continuous and do not have a frequency gap or overlapping.

[0039] FIG. 3 is a schematic circuit diagram of a transmitting circuit 300 according to a third embodiment of the present invention. The transmitting circuit provided in the embodiment in FIG. 3 includes a transmitting circuit corresponding to each antenna of multiple antennas (for example, a first antenna and a second antenna), so that a multi-antenna system can be supported. Each unit of a transmitting circuit corresponding to the first antenna has the same function as each unit of a transmitting circuit corresponding to the second antenna.

[0040] Corresponding to the first antenna, the transmitting circuit 300 in FIG. 3 includes a digital interface circuit 310, a digital modulation circuit 320, a first frequency relocation circuit 330, a first synthesizer 340, a first digital to analog converter 350, and a first up-conversion circuit 360, which are similar to the digital interface circuit 110, the digital modulation circuit 120, the first frequency relocation circuit 130, the first synthesizer 140, the first digital to analog converter 150, and the up-conversion circuit 160 in FIG. 1 and are not further described herein.

[0041] According to the embodiment of the present invention, corresponding to the second antenna, the digital interface circuit 310 further obtains, in the predetermined bandwidth, second data to be sent, and decomposes the second data into N parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the N second sub digital signal flows is smaller than the predetermined bandwidth. As an embodiment, M may be equal to N; the digital modulation circuit 320 further receives the N second sub digital signal flows, and modulates the N second sub digital signal flows to obtain N second modulated signals. Corresponding to the second antenna, the transmitting circuit 300 in FIG. 3 further includes a second frequency relocation circuit 370, a second synthesizer 380, a second digital to analog converter 390, and a second up-conversion circuit 395.

[0042] The second frequency relocation circuit 370 receives the N second modulated signals, and performs frequency relocation on the N second modulated signals, where there is no frequency band gap between adjacent second modulated signals of the N second modulated signals that have undergone frequency relocation. The second synthesizer 380 synthesizes the N second modulated signals that have undergone frequency relocation into a second bandwidth signal. The second digital to analog converter 390 receives the second bandwidth signal, and performs digital to analog conversion on the second bandwidth signal to obtain a second analog signal. The first up-conversion circuit 360 receives a first analog signal, and converts the first analog signal into a first radio frequency signal, so that the first radio frequency signal is sent by the first antenna. The second up-conversion circuit 395 receives the second analog signal, and converts the second analog signal into a second radio frequency signal, so that the second radio frequency signal is sent by the second antenna.

[0043] According to the embodiment of the present invention, the digital modulation circuit 320 includes N modulators, where the N modulators modulate the N first sub digital signal flows respectively and modulate the N second sub digital signal flows respectively.

[0044] For example, the modulators may be implemented by using an FGPA, and digital modulation is performed, by using the same FPGA, on the first sub digital signal flows corresponding to the first antenna and the second sub digital signal flows corresponding to the second antenna. That is, a first modulated signal and a second modulated signal output from the same FPGA can be output to a frequency mixer that performs frequency relocation by using the same frequency. Due to independence of each frequency domain subchannel, highly complex digital processing devices and FPGAs may be distributed in multiple different DSP/FPGA chips/boards, thereby making the implementation easier and more flexible.

[0045] When M=N, sub digital signal flows of the first data corresponding to the first antenna or sub digital signal flows of the second data corresponding to the second antenna are synthesized into a large bandwidth signal, and digital to analog conversion is performed on the large bandwidth signal by using a DAC. That is, at the transmitting end, all subchannels corresponding to each antenna use only one high speed DAC and one analog in-

termediate frequency circuit, thereby saving devices and costs of the transmitting circuit.

[0046] FIG. 4 is a schematic circuit diagram of a transmitting circuit 400 according to a fourth embodiment of the present invention. The transmitting circuit provided in the embodiment in FIG. 4 includes transmitting circuits corresponding to multi-polarized antennas (for example, an H-polarized antenna and a V-polarized antenna), so that a multi-polarized antenna system can be supported.

[0047] The transmitting circuit 400 in FIG. 4 includes a digital interface circuit 410, a digital modulation circuit 420, a first frequency relocation circuit 430, a first synthesizer 440, a first digital to analog converter 450, and a first up-conversion circuit 460, which are similar to the digital interface circuit 110, the digital modulation circuit 120, the first frequency relocation circuit 130, the first synthesizer 140, the first digital to analog converter 150, and the up-conversion circuit 160 in FIG. 1 and are not further described herein.

[0048] A transmitting antenna of the transmitting circuit 400 is a dual-polarized antenna; the digital modulation circuit 420 modulates the N first sub digital signal flows on the H-polarized antenna, and preferably M=N.

[0049] The digital interface circuit 410 further obtains, in the predetermined bandwidth, second data to be sent, and decomposes the second data into K parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the K second sub digital signal flows is smaller than the predetermined bandwidth and K is a positive integer.

[0050] The digital modulation circuit 420 further receives the K second sub digital signal flows, and modulates the K second sub digital signal flows on a V-polarized antenna to obtain K second modulated signals.

[0051] The transmitting circuit 400 further includes a second digital modulation circuit 425, a second frequency relocation circuit 470, a second synthesizer 480, a second digital to analog converter 490, a second up-conversion circuit 495, and a coupler 465.

[0052] The second digital modulation circuit 425 receives the K second sub digital signal flows, and modulates the K second sub digital signal flows on the V-polarized antenna to obtain K second modulated signals; the second frequency relocation circuit 470 receives the K second modulated signals, and performs frequency relocation on the K second modulated signals, where there is no frequency band gap between adjacent second modulated signals of the K second modulated signals that have undergone frequency relocation; the second synthesizer synthesizes the K second modulated signals that have undergone frequency relocation into a second bandwidth signal; the second digital to analog converter 490 receives the second bandwidth signal, and performs digital to analog conversion on the second bandwidth signal to obtain a second analog signal, where the first up-conversion circuit 460 receives the first analog signal, and converts the first analog signal into a first radio frequency signal. The second up-conversion circuit 495 receives the second analog signal, and converts the second analog signal into a second radio frequency signal. The coupler 465 couples the first radio frequency signal and the second radio frequency signal, so that the first radio frequency signal and the second radio frequency signal are sent by the dual-polarized antenna respectively.

[0053] According to the embodiment of the present invention, the digital modulation circuit 420 includes N+K modulators, where the N modulators modulate the N first sub digital signal flows respectively and the K modulators modulate the K second sub digital signal flows respectively and N may be equal to K.

[0054] FIG. 5 is a schematic circuit diagram of a transceiver 500 according to a fifth embodiment of the present invention. The transceiver 500 includes a receiving circuit and a transmitting circuit. The transmitting circuit in FIG. 5 may include a digital interface circuit 510, a digital modulation circuit 520, a first frequency relocation circuit 530, a first synthesizer 540, a first digital to analog converter 550, and an up-conversion circuit 560, which are similar to the digital interface circuit 110, the digital modulation circuit 120, the first frequency relocation circuit 130, the first synthesizer 140, the first digital to analog converter 150, and the up-conversion circuit 160 in FIG. 1 and are not further described herein.

[0055] The receiver circuit may include a down-conversion circuit 595, an intermediate frequency power divider 590, a second frequency relocation circuit 580, and N analog to digital converters 570.

[0056] The down-conversion circuit 595 converts a radio frequency signal received on a receiving antenna into an analog signal. The intermediate frequency power divider 590 decomposes the analog signal into N parallel sub analog signal flows. The second frequency relocation circuit 580 performs frequency relocation on the N parallel sub analog signal flows. The N analog to digital converters 570 perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows. The digital demodulation circuit 525 performs demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals. The digital interface circuit 510 synthesizes the N parallel demodulated signals into second data.

[0057] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing

needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0058] According to the embodiment of the present invention, a requirement for an ADC may be reduced in a frequency domain subchannel sampling manner at a receiving end; and subchannels in a digital domain are divided at a transmitting end, so that the receiving end can process each independent frequency domain subchannel. On one hand, each frequency domain subchannel can transmit data independently, thereby increasing a system flexibility. On the other hand, due to independence of each frequency domain subchannel, highly complex digital processing devices and FPGAs may be distributed in multiple different DSP/FPGA chips/boards. Meanwhile, only one high speed DAC and one analog transmission intermediate frequency circuit are used, thereby saving related devices and costs.

[0059] FIG. 6 is a schematic circuit diagram of a communication system 600 according to a sixth embodiment of the present invention. The communication system 600 includes a transmitter and a receiver.

[0060] The transmitter in FIG. 6 includes the transmitting circuit in FIG. 1, FIG. 2, FIG. 3, or FIG. 4. The transmitting circuit includes a digital interface circuit 610, a digital modulation circuit 620, a first frequency relocation circuit 630, a first synthesizer 540, a first digital to analog converter 650, and an up-conversion circuit 660, which are similar to the digital interface circuit 110, the digital modulation circuit 120, the first frequency relocation circuit 130, the first synthesizer 140, the first digital to analog converter 150, and the up-conversion circuit 160 in FIG. 1 and are not further described herein.

[0061] The receiver includes a down-conversion circuit 665, an intermediate frequency power divider 655, a second frequency relocation circuit 645, Q analog to digital converters 635, a digital demodulation circuit 625, and a digital interface circuit 615.

[0062] The down-conversion circuit 665 converts a radio frequency signal received on a receiving antenna into an analog signal. The intermediate frequency power divider 655 decomposes the analog signal into Q parallel sub analog signal flows. The second frequency relocation circuit 645 performs frequency relocation on the Q parallel sub analog signal flows. The Q analog to digital converters 635 perform analog to digital conversion on the Q parallel sub analog signal flows respectively to obtain Q parallel digital signal flows. The digital demodulation circuit 625 performs demodulation processing on the Q parallel digital signal flows to obtain Q parallel demodulated signals. The digital interface circuit 615 synthesizes the Q parallel demodulated signals into first data, where Q may be equal to N in applications.

[0063] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0064] According to the embodiment of the present invention, a requirement for an ADC may be reduced in a frequency domain subchannel sampling manner at a receiving end; and subchannels in a digital domain are divided at a transmitting end, so that the receiving end can process each independent frequency domain subchannel. On one hand, each frequency domain subchannel can transmit data independently, thereby increasing a system flexibility. On the other hand, due to independence of each frequency domain subchannel, highly complex digital processing devices and FPGAs may be distributed in multiple different DSP/FPGA chips/boards. Meanwhile, only one high speed DAC and one analog transmission intermediate frequency circuit are used, thereby saving related devices and costs.

[0065] The embodiments of the present invention are described in more detail with reference to specific examples.

[0066] FIG. 10 is a schematic circuit diagram of a transceiver according to a tenth embodiment of the present invention. FIG. 12 is a schematic circuit diagram of a synthesizer according to an embodiment of the present invention. The transceiver in FIG. 10 is an example of the transceiver in FIG. 5.

[0067] Referring to FIG. 10, a transmitting circuit of the transceiver includes one DAC, while a receiving circuit of the transceiver includes N ADCs, that is, the number of ADCs is N times the number of DACs. The transceiver may be divided into three parts: a digital modulation and demodulation part, an analog intermediate frequency part, and an analog radio frequency part. The following describes a working principle of the transceiver in detail by using the analog intermediate frequency part and the analog radio frequency part as an example.

[0068] Referring to FIG. 10, at a transmitting end, a digital interface circuit 1001 obtains data in a predetermined bandwidth (for example, 5 GHz), and decomposes the data into N parallel sub digital signal flows, where a bandwidth occupied by each sub digital signal flow is smaller than the predetermined bandwidth. For example, if data with a total bandwidth of 5 GHz is decomposed into four digital signal flows (that is, four subchannels), the bandwidth of each sub digital signal flow is 1.25 GHz. For example, a piece of 4-bit data may be divided into

four pieces of 1-bit sub digital signal flows, or two pieces of 2-bit data may be divided into four pieces of 1-bit sub digital signal flows, where the four pieces of 1-bit sub digital signal flows are transmitted in four subchannels respectively.

[0069] A digital modulation circuit formed by N (for example, four) field programmable gate arrays (FPGAs) 1002 to 1005 receives the N sub digital signal flows, and modulates the N sub digital signal flows to obtain N modulated signals, where the N FPGAs 1002 to 1005 correspond to the N sub digital signal flows one by one. According to the embodiment of the present invention, the digital modulation circuit may also be implemented by using an application specific integrated circuit (Application Specific Integrated Circuit, ASIC) and the like.

[0070] The working principle of the digital modulation circuit is as follows: N sub digital signal flows are processed independently by using the N FPGAs 1002 to 1005. Each FPGA has the same function, and the FPGA processing (in a single carrier or multicarrier modulation manner) on the subchannels mainly implement modulation on digital signals. The modulation on the digital signal flows includes but is not limited to channel coding, symbol mapping modulation, OFDM modulation, pulse shaping, sampling rate conversion, pre-emphasis, pre-equalization, peak-to-average ratio suppression, and the like. Each FPGA may include: an encoding module, configured to encode input digital signal flows, for example, configured to perform low-density parity-check (Low-density Parity-check, LDPC) coding; a constellation point mapping module, configured to map the input sub digital signal flows to corresponding constellation points, for example, 64 phase quadrature amplitude modulation (Quadrature Amplitude Modulation, QAM); an inverse fast Fourier transform (Inverse Fast Fourier Transform, IFFT) module, configured to perform inverse fast Fourier transform on the input sub digital signal flows to convert frequency domain signals into time domain signals; a window adding module, configured to add a time domain window and a frequency domain window to the input time domain signals simultaneously or separately; a framing module, configured to insert a preamble sequence into signals to implement a framing function; and a sampling rate converting module, configured to convert a sampling rate into a sampling rate of the DAC. Through digital modulation by the FPGAs, the center frequency of a modulated signal output by each FPGA is 1.2 GHz, and a bandwidth occupied by useful signals is 0.5750 GHz to 1.8250 GHz.

[0071] A frequency relocation circuit formed by N frequency mixers 1006 to 1009 and N local oscillators f_1 to f_N receives the N modulated signals, and performs frequency mixing and frequency relocation on the N modulated signals. For example, assuming that N=4, if the center frequency of the modulated signal output by each FPGA is 1.2 GHz and the local oscillators choose frequencies f_1=0 GHz, f_2=1.25 GHz, f_3=2.5 GHz, and f_4=3.75 GHz, after the frequency relocation is performed, the center frequencies of modulated signals output by the frequency mixers 1006 to 1009 are changed to 1.2 GHz, 1.45 GHz, 3.6 GHz, and 4.95 GHz respectively, with the total occupied frequency band of 0.5750 GHz to 5.5750 GHz, and there is no frequency band gap between adjacent modulated signals.

[0072] The synthesizer 1010 synthesizes the N second modulated signals that have undergone frequency relocation into a large bandwidth signal. Referring to FIG. 12, the synthesizer 1010 may include an adder 1210 and an SINC function 1220. The synthesizer 1010 adds data flow 1 to data flow N (the N modulated signals that have undergone frequency relocation). For example, assuming that N=4, and f_1=0GHz, f_2=1.25GHz, f_3=2.5GHz, and f_4=3.75GHz, the four subbands are synthesized into a large bandwidth signal of 5 GHz, that is, 0.5750 GHz to 5.5750 GHz. The SINC function 1220 is configured to compensate the synthesized large bandwidth signal, and output the compensated signal to a DAC 1011.

[0073] The DAC 1011 receives the large bandwidth signal from the synthesizer 1010, performs digital to analog conversion on the large bandwidth signal, and outputs the output analog signal to an up-conversion circuit.

[0074] The up-conversion circuit receives the analog signal output by the DAC 1011, and converts the analog signal into a radio frequency signal, so that the radio frequency signal is sent by an antenna. The up-conversion circuit may include an up-conversion of the intermediate frequency part and an up-conversion of the analog radio frequency part. Specifically, in the analog intermediate frequency part, the analog signal output by the DAC 1011 undergoes an analog intermediate frequency modulation (that is, a first up-conversion) by a frequency mixer 1012 and a local oscillator f_{IF}, and then is filtered by a band pass filter (Band Pass Filter, BPF) 1013, and is further amplified by an amplifier 1014; finally, the amplified analog signal is output to the analog radio frequency part. In the analog radio frequency part, the analog signal output by the analog intermediate frequency part undergoes an up-conversion (that is, a second up-conversion) by a frequency mixer 1015 and a local oscillator f_{RF}, and then is amplified by an amplifier 1016, and is further filtered by a BPF 1017; after the analog signal is amplified by an amplifier 1018, the amplified analog signal is transferred by a duplexer 1019 to an antenna 1020 for transmission.

[0075] At the receiving end, the antenna 1020 receives a radio frequency signal from a peer transceiver, where the radio frequency signal enters, through the duplexer 1019, a receiving circuit of the transceiver, and then is filtered by a BPF 1049; the radio frequency signal is further amplified by an amplifier 1048, and finally undergoes a down-conversion by a frequency mixer 1047 and the local oscillator f_{RF} to obtain an analog intermediate frequency signal.

[0076] The analog intermediate frequency signal is divided by an intermediate frequency power divider 1046 to obtain N parallel sub analog signal flows with N same frequencies and transmitted in N subchannels respec-

tively. The sub analog signal flows are respectively amplified by amplifiers 1042 to 1045, filtered by BPFs 1038 to 1041, then relocated, through frequency relocation (intermediate frequency down-conversion) by frequency mixers 1034 to 1037 and local oscillators f_1' to f_N', to a desired frequency, and finally, filtered by BPFs 1030 to 1033. Sub analog signals that have undergone intermediate frequency processing have the same frequency, which means that the frequency of each sub analog signal is the same as that of each signal output by the FPGAs of the transmitting end.

[0077] Multiple parallel sub data flows that have undergone intermediate frequency processing are sampled by their respective ADCs to obtain sub digital signal flows (that is, discrete sampling signals) of the subchannels, and the sub digital signal flows are output to a digital demodulation circuit formed by N FPGAs for demodulation.

[0078] The working principle of the digital demodulation circuit is as follows: Sub digital signal flows of the subchannels are processed by their respective FPGAs to obtain a sending bit decision signal corresponding to each sub digital signal flow. The FPGA processing of the subchannels mainly implement demodulation on digital signals, including a single carrier or multicarrier modulation manner. The demodulation on the digital signals includes but is not limited to channel estimation, coding demodulation, sampling rate conversion, synchronization, equalization, and the like. Each FPGA may include: a sampling rate converting module, configured to convert an ADC sampling rate into a sampling rate of a symbol rate; an automatic gain controlling module, configured to estimate an input signal power, and adjust a gain of an analog device; a frame synchronizing module, configured to implement a frame synchronization function; a frequency deviation estimating and compensating module, configured to estimate and compensate a carrier frequency deviation and a sampling frequency deviation; an FFT module, configured to convert a time domain signal into a frequency domain signal; a channel estimating module, configured to perform channel estimation to implement correlation detection on signals; a residual frequency deviation estimating and compensating module, configured to estimate and compensate a residual carrier frequency deviation and a sampling frequency deviation; a phase noise eliminating module, configured to eliminate phase noise caused by radio frequency devices; and a decoding module, configured to implement data decoding.

[0079] The sending bit decision signals of multiple subchannels that have been processed by the FPGA are synthesized by a digital interface circuit 1001 to obtain a high speed receiving decision signal.

[0080] According to the embodiment of the present invention, a requirement for an ADC may be reduced in a frequency domain subchannel sampling manner at a receiving end; and subchannels in a digital domain are divided at a transmitting end, so that the receiving end can process each independent frequency domain subchannel. On one hand, each frequency domain subchannel can transmit data independently, thereby increasing a system flexibility. On the other hand, due to independence of each frequency domain subchannel, highly complex digital processing devices and FPGAs may be distributed in multiple different DSP/FPGA chips/boards. Meanwhile, only one high speed DAC and one analog transmission intermediate frequency circuit are used, thereby saving related devices and costs.

[0081] FIG. 11 is a schematic circuit diagram of a transceiver according to an eleventh embodiment of the present invention. A transmitting circuit in the transceiver in FIG. 11 is an example of the embodiment in FIG. 2.

[0082] Different from the embodiment in FIG. 10, the transmitting circuit of the transceiver in FIG. 11 may include M DACs, while a receiving circuit of the transceiver in FIG. 11 includes NxM ADCs, that is, the number of ADCs is N times the number of DACs.

[0083] Referring to FIG. 11, at a transmitting end, a digital interface circuit 1101 obtains data in a predetermined bandwidth (for example, 5 GHz), and decomposes the data into MxN parallel sub digital signal flows, where a bandwidth occupied by each sub digital signal flow is smaller than the predetermined bandwidth. For example, if data with a total bandwidth of 5 GHz is decomposed into 2xN sub digital signal flows (that is, 2xN subchannels), the bandwidth of each sub digital signal flow is 5/(2xN) GHz.

[0084] A digital modulation circuit formed by 2xN FPGAs 1102 to 1105 receives the 2xN sub digital signal flows, and modulates the 2xN sub digital signal flows to obtain 2xN modulated signals, where the 2xN FPGAs 1102 to 1105 correspond to the 2xN sub digital signal flows one by one. The center frequency of a modulated signal output by each FPGA is 1.2 GHz (assuming that N=2), and the bandwidth occupied by useful signals is 0.5750 GHz to 1.8250 GHz.

[0085] A frequency relocation circuit formed by N frequency mixers 1106 to 1107 and N local oscillators f_1 to f_N receives N modulated signals output by the N FPGAs 1102 to 1103, and performs frequency mixing and frequency relocation on the N modulated signals. A frequency relocation circuit formed by another N frequency mixers 1108 to 1109 and N local oscillators whose frequencies are f_1 to f_N receives N modulated signals output by the N FPGAs 1104 to 1105, and performs frequency mixing and frequency relocation on the N modulated signals. For example, assuming that N=2, if the center frequency of the modulated signal output by each FPGA is 1.2 GHz and the local oscillators choose frequencies f_1=0 GHz and f_2=1.25 GHz, after the frequency relocation is performed, center frequencies of modulated signals output by the frequency mixers 1106 to 1109 are changed to 1.2 GHz, 2.45 GHz, 1.2 GHz, and 2.45 GHz respectively.

[0086] A synthesizer 1110 synthesizes the N modulated signals that have undergone frequency relocation by the N frequency mixers 1006 to 1007 into a large band-

width signal. A synthesizer 1111 synthesizes the N modulated signals that have undergone frequency relocation by the N frequency mixers 1008 to 1009 into a large bandwidth signal. For example, assuming that N=2, and f_1=0 GHz and f_2=1.25 GHz, the synthesizer 1110 and the synthesizer 1111 synthesize their two subbands into a large bandwidth signal of 2.5 GHz respectively, that is, 0.5750 GHz to 3.0750 GHz, and there is no frequency band gap between adjacent modulated signals.

[0087] A DAC 1111 and a DAC 1112 receive the two large bandwidth signals from the synthesizer 1110 and the synthesizer 1111 respectively, perform digital to analog conversion on the two large bandwidth signals to obtain analog signals, and output the analog signals to an up-conversion circuit.

[0088] The up-conversion circuit receives the analog signals output by the DAC 1111 and the DAC 1112, and converts the analog signals into radio frequency signals, so that the radio frequency signals are sent by an antenna. Specifically, in the analog intermediate frequency part, the analog signals output by the DAC 1111 the DAC 1112 respectively are filtered by a BPF 1113 and a BPF 1114, and undergo intermediate frequency up-conversion and frequency relocation by a frequency mixer 1115 and a local oscillator g_1 and a frequency mixer 1116 and a local oscillator g_m; then the analog signals are filtered by a BPF 1117 and a BPF 1118, and are further amplified by an amplifier 1119 and an amplifier 1120; finally, after the two analog signals output and amplified by the amplifier 119 and the amplifier 1120 are synthesized by an intermediate frequency power synthesizer 1116, the two analog signals are output to the analog radio frequency part, where a difference between g_1 and g_m is 2.5 GHz, so that the intermediate frequency power synthesizer 1116 synthesizes the two analog signals into a large bandwidth signal of 5 GHz, that is, 0.5750 GHz to 5.5750 GHz. The analog radio frequency part in FIG. 11 includes a frequency mixer 1121, a local oscillator f_c, an amplifier 1122, a BPF 1123, and an amplifier 1124, which are similar to the units of the analog radio frequency part in FIG. 10 and are not further described herein. Finally, the analog signals output by the analog radio frequency part are transferred through a duplexer 1125 to an antenna 1126 for transmission.

[0089] An amplifier 1127, a frequency mixer 1128 and a local oscillator f_c, an intermediate frequency power divider 1129, amplifiers 1130 to 1133, BPFs 1134 to 1137, BPFs 1142 to 1145, ADCs 1146 to 1149 and FPGAs 1150 to 1153 of the receiving circuit in the transceiver in FIG. 11 have functions similar to those of the units of the receiving circuit in FIG. 10, which are not further described herein. The receiving circuit in FIG. 11 is different from the receiving circuit in FIG. 10 in that: Frequency mixers 1138 to 1139 and a local oscillators whose frequency is f_1+g_1 perform frequency relocation on analog signals output by the BPFs 1134 to 1135, while frequency mixers 1140 to 1141 and a local oscillator whose frequency is f_m+g_m perform frequency relocation on analog signals output by the BPFs 1136 to 1137.

[0090] FIG. 7A and FIG. 7B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to a seventh embodiment of the present invention. The transmitting circuit and the receiving circuit in FIG. 7A and FIG. 7B are an example of the embodiment in FIG. 4.

[0091] The transmitting circuit of the embodiment in FIG. 7A modulates a large bandwidth signal on an H-polarized antenna and a V-polarized antenna respectively to obtain an H-polarized signal and a V-polarized signal, and then sends the H-polarized signal and the V-polarized signal through a dual-polarized antenna. The receiving circuit in FIG. 7B receives the H-polarized signal and the V-polarized signal from the dual-polarized antenna and demodulates the H-polarized signal and the V-polarized signal.

[0092] An antenna 720 of the transmitting circuit and an antenna 770 of the receiving circuit are dual-polarized antennas. A digital modulation circuit modulates N sub digital signal flows on the H-polarized antenna and the V-polarized antenna respectively. The embodiment in FIG. 7A includes a DAC 711 and a DAC 731 that correspond to the H-polarized antenna and the V-polarized antenna respectively.

[0093] Referring to FIG. 7A, at a transmitting end, corresponding to the H-polarized antenna, a digital interface circuit 701 obtains data in a predetermined bandwidth (for example, 5 GHz), and decomposes the data into N parallel sub digital signal flows. Similarly, corresponding to the DAC 731, the digital interface circuit 701 can obtain N sub digital signal flows.

[0094] A transmitting circuit corresponding to the H-polarized antenna includes N FPGAs 702 to 705, N frequency mixers 706 to 709, local oscillators whose frequencies are f_1 to f_N, a synthesizer 710, the DAC 711, a BPF 713, an amplifier 714, a frequency mixer 715, a local oscillator whose frequency is f_{RF}, an amplifier 716, a BPF 717, and an amplifier 718. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 10, which are not further described herein. A transmitting circuit corresponding to the V-polarized antenna includes N FPGAs 722 to 725, N frequency mixers 726 to 729, local oscillators whose frequencies are f_1 to f_N, a synthesizer 730, the DAC 731, a BPF 733, an amplifier 734, a frequency mixer 735, a local oscillator whose frequency is f_{RF}, an amplifier 736, a BPF 737, and an amplifier 738. Similarly, functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 10, which are not further described herein. The transmitting circuit in FIG. 7A is different from the transmitting circuit in FIG. 10 in that: The amplifier 718 and the amplifier 738 send the H-polarized signal and the V-polarized signal to an coupler (OMT) 719 respectively, and the coupler 719 converts the H-polarized signal and the V-polarized signal into a dual-polarized signal, and outputs the dual-polarized signal to a dual-polarized antenna 720.

[0095] Referring to FIG. 7B, at a receiving end, a coupler 769 converts a dual-polarized signal received from a dual-polarized antenna 770 into an H-polarized signal and a V-polarized signal.

[0096] A receiving circuit corresponding to the H-polarized antenna includes a BPF 768, an amplifier 767, a frequency mixer 766, and a local oscillator f_{RF}, an intermediate frequency power divider 765, amplifiers 761 to 764, BPFs 757 to 760, frequency mixers 753 to 756, local oscillators whose frequencies are f_1' to f_N', BPFs 749 to 752, ADCs 745 to 748, and FPGAs 741 to 744. These units are similar to the units of the receiving circuit in FIG. 10, which are not further described herein. A receiving circuit corresponding to the V-polarized antenna includes a BPF 798, an amplifier 797, a frequency mixer 796, and a local oscillator f_{RF}, an intermediate frequency power divider 785, amplifiers 791 to 794, BPFs 787 to 790, frequency mixers 783 to 786, local oscillators whose frequencies are f_1' to f_N', BPFs 779 to 782, ADCs 775 to 778, and FPGAs 771 to 774. These units are similar to the units of the receiving circuit in FIG. 10, which are not further described herein. The receiving circuit in FIG. 7B is different from the receiving circuit in FIG. 10 in that: The coupler 769 receives a dual-polarized signal from the dual-polarized antenna 770, converts the dual-polarized signal into an H-polarized signal and a V-polarized signal, and outputs the H-polarized signal and the V-polarized signal to a BPF 768 and BPF 798 respectively.

[0097] FIG. 8A and FIG. 8B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to an eighth embodiment of the present invention. The transmitting circuit and the receiving circuit in FIG. 8A and FIG. 8B are an example of the embodiment in FIG. 3.

[0098] The transmitting circuit in the embodiment in FIG. 8A corresponds to multiple antennas antenna 1 to antenna M, and the receiving circuit in FIG. 8B corresponds to multiple antennas antenna 1 to antenna N.

[0099] At a transmitting end, a large bandwidth signal is modulated on each antenna, and then the modulated signal is sent through each antenna. At a receiving end, multiple signals are received and demodulated on each antenna.

[0100] Referring to FIG. 8A, at a transmitting end, corresponding to each antenna, a digital interface circuit 701 obtains data in a predetermined bandwidth (for example, 5 GHz), and decomposes the data into N parallel sub digital signal flows.

[0101] Corresponding to antenna 1, a transmitting circuit includes N FPGAs 802 to 805, N frequency mixers 806 to 809, local oscillators whose frequencies are f_1 to f_N, a synthesizer 810, a DAC 811, a frequency mixer 812, a local oscillator whose frequency is f_{IF}, a BPF 813, an amplifier 814, a frequency mixer 815, a local oscillator whose frequency is f_{RF}, an amplifier 816, a BPF 817, and an amplifier 818. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 10, which are not further described herein. Corresponding to antenna M, a transmitting circuit includes N FPGAs 802 to 805, N frequency mixers 826 to 829, local oscillators whose frequencies are f_1 to f_N, a synthesizer 830, a DAC 831, a frequency mixer 832, a local oscillator whose frequency is f_{IF}, a BPF 833, an amplifier 834, a frequency mixer 835, a local oscillator whose frequency is f_{RF}, an amplifier 836, a BPF 837, and an amplifier 838. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 10, which are not further described herein. The transmitting circuit in FIG. 8A is different from the transmitting circuit in FIG. 10 in that: The amplifier 818 and the amplifier 838 output a radio frequency signal to antenna 1 and antenna M respectively.

[0102] As can be seen from the above, sub digital signal flows of the transmitting circuit corresponding to antenna 1 and sub digital signal flows of the transmitting circuit corresponding to antenna M undergo digital modulation by using the same FPGAs. For example, two modulated signals output by the FPGA 802 are output to the frequency mixer 806 and the frequency mixer 826 respectively, and two modulated signals output by the FPGA 803 are output to the frequency mixer 807 and the frequency mixer 827 respectively, and the like.

[0103] Referring to FIG. 8B, at a receiving end, a receiving circuit corresponding to antenna 1 includes a BPF 868, an amplifier 867, a frequency mixer 866, and a local oscillator f_{RF}, an intermediate frequency power divider 865, amplifiers 861 to 864, BPFs 857 to 860, frequency mixers 853 to 856, local oscillators whose frequencies are f_1' to f_N', BPFs 849 to 852, ADCs 845 to 848, and FPGAs 841 to 844. These units are similar to the units of the receiving circuit in FIG. 10, which are not further described herein. A receiving circuit corresponding to antenna N includes a BPF 898, an amplifier 897, a frequency mixer 896, and a local oscillator f_{RF}, an intermediate frequency power divider 895, amplifiers 891 to 894, BPFs 897 to 890, frequency mixers 883 to 886, local oscillators whose frequencies are f_1' to f_N', BPFs 879 to 882, ADCs 875 to 878, and FPGAs 841 to 844. These units are similar to the units of the receiving circuit in FIG. 10, which are not further described herein. The receiving circuit in FIG. 8B is different from the transmitting circuit in FIG. 10 in that: The BPF 868 and the BPF 898 receive a radio frequency signal from antenna 1 and antenna N respectively.

[0104] As can be seen from the above, sub digital signal flows of the receiving circuit corresponding to antenna 1 and sub digital signal flows of the receiving circuit corresponding to antenna N undergo digital demodulation by using the same FPGAs. For example, the ADC 845 and the ADC 875 each output a digital signal to the FPGA 841 for digital demodulation, and the ADC 846 and the ADC 876 each output a digital signal to the FPGA 842 for digital demodulation, and the like.

[0105] FIG. 9A and FIG. 9B are respectively schematic circuit diagrams of a transmitting circuit and a receiving circuit according to a ninth embodiment of the present

invention. The transmitting circuit and the receiving circuit in FIG. 9A are an example of a combination of FIG. 3 and FIG. 4.

[0106] The embodiment in FIG. 9A includes transmitting circuits corresponding to multiple dual-polarized antennas dual-polarized antenna 1 to dual-polarized antenna M, and the embodiment in FIG. 9B includes receiving circuits corresponding to multiple dual-polarized antennas dual-polarized antenna 1 to dual-polarized antenna N. In addition, the transmitting circuit corresponding to each dual-polarized antenna modulates a large bandwidth signal on an H-polarized antenna and a V-polarized antenna respectively to obtain an H-polarized signal and a V-polarized signal, and sends the H-polarized signal and the V-polarized signal through the dual-polarized antenna, and the receiving circuit corresponding to each dual-polarized antenna receives the H-polarized signal and the V-polarized signal from the dual-polarized antenna and demodulates the H-polarized signal and the V-polarized signal.

[0107] At a transmitting end, a transmitting circuit corresponding to dual-polarized antenna 1 includes a transmitting circuit corresponding to the H-polarized antenna and a transmitting circuit corresponding to the V-polarized antenna. The transmitting circuit corresponding to the H-polarized antenna includes N FPGAs 902 to 905, N frequency mixers 906 to 909, local oscillators whose frequencies are f_1 to f_N, a synthesizer 910, a DAC 911, a frequency mixer 912, a local oscillator whose frequency is f_{IF}, a BPF 913, an amplifier 914, a frequency mixer 915, a local oscillator whose frequency is f_{RF}, an amplifier 916, a BPF 917, and an amplifier 918. The amplifier 918 is connected to a coupler 919, and the coupler 919 is connected to an antenna 920. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 7A, which are not further described herein. The transmitting circuit corresponding to the V-polarized antenna includes N FPGAs 902' to 905', N frequency mixers 926 to 929, local oscillators whose frequencies are f_1 to f_N, a synthesizer 930, a DAC 931, a frequency mixer 932, a local oscillator f_{IF}, a BPF 933, an amplifier 934, a frequency mixer 935, a local oscillator whose frequency is f_{RF}, an amplifier 936, a BPF 937, and an amplifier 938. The amplifier 938 is connected to the coupler 919, and the coupler 919 is connected to the antenna 920. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 7B, which are not further described herein.

[0108] At the transmitting end, the transmitting circuit corresponding to dual-polarized antenna M includes a transmitting circuit corresponding to the H-polarized antenna and a transmitting circuit corresponding to the V-polarized antenna. The transmitting circuit corresponding to the H-polarized antenna includes N FPGAs 902 to 905, N frequency mixers 906' to 909', local oscillators whose frequencies are f_1 to f_N, a synthesizer 910', a DAC 911', a frequency mixer 912', a local oscillator f_{IF}, a BPF 913', an amplifier 914', a frequency mixer 915', a local oscillator whose frequency is f_{RF}, an amplifier 916', a BPF 917', and an amplifier 918'. The amplifier 918' is connected to a coupler 919', and the coupler 919' is connected to an antenna 920'. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 7A, which are not further described herein. The transmitting circuit corresponding to the V-polarized antenna includes N FPGAs 902' to 905', N frequency mixers 926' to 929', local oscillators whose frequencies are f_1 to f_N, a synthesizer 930, a DAC 931, a frequency mixer 932', a local oscillator f_{1F}, a BPF 933', an amplifier 934', a frequency mixer 935', a local oscillator whose frequency is f_{RF}, an amplifier 936', a BPF 937', and an amplifier 938'. The amplifier 938' is connected to the coupler 919', and the coupler 919' is connected to the antenna 920'. Functions of these units are similar to those of the corresponding units of the transmitting circuit in FIG. 7B, which are not further described herein.

[0109] At a receiving end, the receiving circuit corresponding to dual-polarized antenna 1 includes a receiving circuit corresponding to the H-polarized antenna and a receiving circuit corresponding to the V-polarized antenna. The receiving circuit corresponding to the H-polarized antenna includes a BPF 968, an amplifier 967, a frequency mixer 966, and a local oscillator f_{RF}, an intermediate frequency power divider 965, amplifiers 961 to 964, BPFs 957 to 960, frequency mixers 953 to 956, local oscillators whose frequencies are f_1' to f_N', BPFs 949 to 952, ADCs 945 to 948, and FPGAs 941 to 944. These units are similar to the units of the receiving circuit in FIG. 7A, which are not further described herein. The receiving circuit corresponding to the V-polarized antenna includes a BPF 998, an amplifier 997, a frequency mixer 996, and a local oscillator f_{RF}, an intermediate frequency power divider 995, amplifiers 991 to 994, BPFs 987 to 990, frequency mixers 983 to 986, local oscillators whose frequencies are f_1' to f_N', BPFs 979 to 982, ADCs 975 to 978, and FPGAs 941' to 944'. These units are similar to the units of the receiving circuit in FIG. 7B, which are not further described herein.

[0110] At the receiving end, the receiving circuit corresponding to dual-polarized antenna N includes a receiving circuit corresponding to the H-polarized antenna and a receiving circuit corresponding to the V-polarized antenna. The receiving circuit corresponding to the H-polarized antenna includes a BPF 968', an amplifier 967', a frequency mixer 966', and a local oscillator f_{RF}, an intermediate frequency power divider 965', amplifiers 961' to 964', BPFs 957' to 960', frequency mixers 953' to 956', local oscillators whose frequencies are f_1' to f_N', BPFs 949' to 952', ADCs 945' to 948', and FPGAs 941' to 944'. These units are similar to the units of the receiving circuit in FIG. 7B, which are not further described herein. The receiving circuit corresponding to the V-polarized antenna includes a BPF 998', an amplifier 997', a frequency mixer 996', and a local oscillator f_{RF}, an intermediate frequency power divider 995', amplifiers 991' to 994', BPFs 987' to 990', frequency mixers 983' to 986', local oscilla-

tors whose frequencies are f_1' to f_N', BPFs 979' to 982', ADCs 975' to 978', and FPGAs 941' to 944'. These units are similar to the units of the receiving circuit in FIG. 7B, which are not further described herein.

[0111] The transmitting circuit, the transceiver, and the communication system according to the embodiments of the present invention have been described above. The following describes a method for transmitting data and a method for transmitting data according to the embodiments of the present invention with reference to FIG. 13 to FIG. 15.

[0112] FIG. 13 is a schematic flowchart of a method for transmitting data according to a twelfth embodiment of the present invention. The method for transmitting data includes the following content:

1310. Obtain, in a predetermined bandwidth, first data to be sent, and decompose the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer.

1320. Modulate the N first sub digital signal flows to obtain N first modulated signals.

1330. Perform frequency relocation on the N first modulated signals, so that there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation.

1340. Synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer.

1350. Perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal.

1360. Convert the first analog signal into a radio frequency signal, so that the radio frequency signal is sent by an antenna.

[0113] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0114] Optionally, as another embodiment, the method in FIG. 13 further includes: synthesizing L first modulated signals of the N first modulated signals that have undergone frequency relocation into a second bandwidth signal, where the L first modulated signals are different from the M first modulated signals; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1306, the first analog signal and the second analog signal may be synthesized into the radio frequency signal.

[0115] Optionally, as another embodiment, the method in FIG. 13 further includes: performing frequency relocation on the first analog signal and the second analog signal respectively before synthesizing the first analog signal and the second analog signal into the radio frequency signal.

[0116] Optionally, as another embodiment, the method in FIG. 13 further includes: obtaining, in the predetermined bandwidth, second data to be sent, and decomposing the second data into N parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the N second sub digital signal flows is smaller than the predetermined bandwidth and M=N; modulating the N second sub digital signal flows to obtain N second modulated signals, performing frequency relocation on the N second modulated signals, where there is no frequency band gap between adjacent second modulated signals of the N second modulated signals that have undergone frequency relocation; synthesizing the N second modulated signals that have undergone frequency relocation into a second bandwidth signal; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1360, the first analog signal is converted into a first radio frequency signal, so that the first radio frequency signal is sent by a first antenna, and the second analog signal is converted in a second radio frequency signal, so that the second radio frequency signal is sent by a second antenna.

[0117] In 1320, the N first sub digital signal flows may be modulated by using N modulators, and the N second sub digital signal flows may be modulated by using the N modulators.

[0118] According to the embodiment of the present invention, the antenna is a dual-polarized antenna, in 1320, the N first sub digital signal flows may be modulated on an H-polarized antenna, where M=N. The method in FIG. 13 further includes: obtaining, in the predetermined bandwidth, second data to be sent, and decomposing the second data into K parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the K second sub digital signal flows is smaller than the predetermined bandwidth and K is a positive integer; modulating the K second sub digital signal flows on a V-polarized antenna to obtain K second modulated signals; performing frequency relocation on the K second modulated signals, where there is no frequency band gap between adjacent second modulated

signals of the K second modulated signals that have undergone frequency relocation; synthesizing the K second modulated signals that have undergone frequency relocation into a second bandwidth signal; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1360, the first analog signal may be converted into a first radio frequency signal and the second analog signal is received, and the second analog signal is converted into a second radio frequency signal; and the first radio frequency signal and the second radio frequency signal are coupled, so that the first radio frequency signal and the second radio frequency signal are sent by the dual-polarized antenna.

[0119] In 1320, the N first sub digital signal flows may be modulated by using N modulators, and the K second sub digital signal flows may be modulated by using K modulators.

[0120] In 1340, the N first modulated signals that have undergone frequency relocation may be added by using an adder to synthesize the modulated signals into a first bandwidth signal.

[0121] According to the embodiment of the present invention, N is at least 4, and the first data is at least one binary digital signal flow.

[0122] FIG. 14 is a schematic flowchart of a method for transmitting data according to a thirteenth embodiment of the present invention.

[0123] The method for transmitting data in FIG. 14 includes a method for receiving data and the method for transmitting data in FIG. 13, where the method for receiving data includes the following content:

1410. Convert a radio frequency signal received on a receiving antenna into an analog signal.
1420. Decompose the analog signal into Q parallel sub analog signal flows.
1430. Perform frequency relocation on the Q parallel sub analog signal flows.
1440. Perform analog to digital conversion on the Q parallel sub analog signal flows respectively to obtain Q parallel digital signal flows.
1450. Perform demodulation processing on the Q parallel digital signal flows to obtain Q parallel demodulated signals.
1460. Synthesize the Q parallel demodulated signals into second data, where Q may be equal to N in applications.

[0124] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance. FIG. 15 is a schematic flowchart of a communication method according to a fourteenth embodiment of the present invention.

[0125] The communication method in FIG. 15 includes a method for receiving data and the method for transmitting data in FIG. 13, where the method for receiving data includes the following content:

1510. Convert a radio frequency signal received on a receiving antenna into an analog signal.
1520. Decompose the analog signal into N parallel sub analog signal flows.
1530. Perform frequency relocation on the N parallel sub analog signal flows.
1540. Perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows.
1550. Perform demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals.
1560. Synthesize the N parallel demodulated signals into first data.

[0126] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0127] Compared with the technical solution in the prior art where a processing speed of a DAC/ADC is increased by using a frequency domain method or a time domain method, the embodiments of the present invention have a lower complexity during signal processing, signals are not easily distorted, and no joint control on multiple DACs/ADCs exists. Compared with the technical solution where a signal bandwidth is reduced in the prior art, the present invention reduces the number of DACs and requirements for analog intermediate frequency process-

ing devices of a transmitting end. Compared with the existing frequency domain multichannel technology, the present invention does not need to reserve a guard space between each channel. In addition, frequency bands can be divided freely without restriction, and the system features powerful scalability. Furthermore, the embodiments of the present invention provide a complete one-to-one sending and receiving solution, and support a system with multi-polarized antennas and/or multiple antennas.

[0128] A person of ordinary skill in the art may be aware that, in combination with the examples described in the embodiments disclosed in this specification, units and algorithm steps may be implemented by electronic hardware, or a combination of computer software and electronic hardware. Whether the functions are performed by hardware or software depends on particular applications and design constraint conditions of the technical solutions. A person skilled in the art may use different methods to implement the described functions for each particular application, but it should not be considered that the implementation goes beyond the scope of the present invention.

[0129] It may be clearly understood by a person skilled in the art that, for the purpose of convenient and brief description, for a detailed working process of the foregoing system, apparatus, and unit, reference may be made to the corresponding process in the foregoing method embodiments, and the details will not be described herein again.

[0130] In the several embodiments provided in the present application, it should be understood that the disclosed system, apparatus, and method may be implemented in other manners. For example, the described apparatus embodiments are merely exemplary. For example, the unit division is merely logical function division and may be other division in actual implementation. For example, a plurality of units or components may be combined or integrated into another system, or some features may be ignored or not performed. In addition, the displayed or discussed mutual couplings or direct couplings or communication connections may be implemented through some interfaces. The indirect couplings or communication connections between the apparatuses or units may be implemented in electronic, mechanical, or other forms.

[0131] The units described as separate parts may or may not be physically separate, and parts displayed as units may or may not be physical units, may be located in one position, or may be distributed on a plurality of network units. A part or all of the units may be selected according to actual needs to achieve the objectives of the solutions of the embodiments.

[0132] In addition, functional units in the embodiments of the present invention may be integrated into one processing unit, or each of the units may exist alone physically, or two or more units are integrated into one unit.

[0133] When the functions are implemented in a form of a software functional unit and sold or used as an independent product, the functions may be stored in a computer-readable storage medium. Based on such an understanding, the technical solutions of the present invention essentially, or the part contributing to the prior art, or a part of the technical solutions may be implemented in a form of a software product. The computer software product is stored in a storage medium, and includes several instructions for instructing a computer device (which may be a personal computer, a server, or a network device) to perform all or a part of the steps of the methods described in the embodiments of the present invention. The foregoing storage medium includes: any medium that can store program code, such as a USB flash drive, a removable hard disk, a read-only memory (Read-Only Memory, ROM), a random access memory (Random Access Memory, RAM), a magnetic disk, or an optical disc.

[0134] The foregoing descriptions are merely specific embodiments of the present invention, but are not intended to limit the protection scope of the present invention. Any variation or replacement readily figured out by a person skilled in the art within the technical scope disclosed in the present invention shall fall within the protection scope of the present invention. Therefore, the protection scope of the present invention shall be subject to the protection scope of the claims.

[0135] FIG. 13 is a schematic flowchart of a method for transmitting data according to a twelfth embodiment of the present invention. The method for transmitting data includes the following content:

1310. Obtain, in a predetermined bandwidth, first data to be sent, and decompose the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer.

1320. Modulate the N first sub digital signal flows to obtain N first modulated signals.

1330. Perform frequency relocation on the N first modulated signals, so that there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation.

1340. Synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer.

1350. Perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal.

1360. Convert the first analog signal into a radio frequency signal, so that the radio frequency signal is sent by an antenna.

[0136] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relo-

cation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0137] Optionally, as another embodiment, the method in FIG. 13 further includes: synthesizing L first modulated signals of the N first modulated signals that have undergone frequency relocation into a second bandwidth signal, where the L first modulated signals are different from the M first modulated signals; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1306, the first analog signal and the second analog signal may be synthesized into the radio frequency signal.

[0138] Optionally, as another embodiment, the method in FIG. 13 further includes: performing frequency relocation on the first analog signal and the second analog signal respectively before synthesizing the first analog signal and the second analog signal into the radio frequency signal.

[0139] Optionally, as another embodiment, the method in FIG. 13 further includes: obtaining, in the predetermined bandwidth, second data to be sent, and decomposing the second data into N parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the N second sub digital signal flows is smaller than the predetermined bandwidth and M=N; modulating the N second sub digital signal flows to obtain N second modulated signals, performing frequency relocation on the N second modulated signals, where there is no frequency band gap between adjacent second modulated signals of the N second modulated signals that have undergone frequency relocation; synthesizing the N second modulated signals that have undergone frequency relocation into a second bandwidth signal; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1360, the first analog signal is converted into a first radio frequency signal, so that the first radio frequency signal is sent by a first antenna, and the second analog signal is converted in a second radio frequency signal, so that the second radio frequency signal is sent by a second antenna.

[0140] In 1320, the N first sub digital signal flows may be modulated by using N modulators, and the N second sub digital signal flows may be modulated by using the N modulators.

[0141] According to the embodiment of the present invention, the antenna is a dual-polarized antenna, in 1320, the N first sub digital signal flows may be modulated on an H-polarized antenna, where M=N. The method in FIG. 13 further includes: obtaining, in the predetermined bandwidth, second data to be sent, and decomposing the second data into K parallel second sub digital signal flows, where a bandwidth occupied by each second sub digital signal flow of the K second sub digital signal flows is smaller than the predetermined bandwidth and K is a positive integer; modulating the K second sub digital signal flows on a V-polarized antenna to obtain K second modulated signals; performing frequency relocation on the K second modulated signals, where there is no frequency band gap between adjacent second modulated signals of the K second modulated signals that have undergone frequency relocation; synthesizing the K second modulated signals that have undergone frequency relocation into a second bandwidth signal; and performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; in 1360, the first analog signal may be converted into a first radio frequency signal and the second analog signal is received, and the second analog signal is converted into a second radio frequency signal; and the first radio frequency signal and the second radio frequency signal are coupled, so that the first radio frequency signal and the second radio frequency signal are sent by the dual-polarized antenna.

[0142] In 1320, the N first sub digital signal flows may be modulated by using N modulators, and the K second sub digital signal flows may be modulated by using K modulators.

[0143] In 1340, the N first modulated signals that have undergone frequency relocation may be added by using an adder to synthesize the modulated signals into a first bandwidth signal.

[0144] According to the embodiment of the present invention, N is at least 4, and the first data is at least one binary digital signal flow.

[0145] FIG. 14 is a schematic flowchart of a method for transmitting data according to a thirteenth embodiment of the present invention.

[0146] The method for transmitting data in FIG. 14 includes a method for receiving data and the method for transmitting data in FIG. 13, where the method for receiving data includes the following content:

1410. Convert a radio frequency signal received on a receiving antenna into an analog signal.

1420. Decompose the analog signal into Q parallel sub analog signal flows.

1430. Perform frequency relocation on the Q parallel sub analog signal flows.

1440. Perform analog to digital conversion on the Q parallel sub analog signal flows respectively to obtain Q parallel digital signal flows.

1450. Perform demodulation processing on the Q parallel digital signal flows to obtain Q parallel de-

modulated signals.

1460. Synthesize the Q parallel demodulated signals into second data, where Q may be equal to N in applications.

[0147] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0148] FIG. 15 is a schematic flowchart of a communication method according to a fourteenth embodiment of the present invention.

[0149] The communication method in FIG. 15 includes a method for receiving data and the method for transmitting data in FIG. 13, where the method for receiving data includes the following content:

1510. Convert a radio frequency signal received on a receiving antenna into an analog signal.

1520. Decompose the analog signal into N parallel sub analog signal flows.

1530. Perform frequency relocation on the N parallel sub analog signal flows.

1540. Perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows.

1550. Perform demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals.

1560. Synthesize the N parallel demodulated signals into first data.

[0150] According to the embodiment of the present invention, data can be decomposed into multiple parallel sub digital signal flows; modulation and frequency relocation are performed on the multiple sub digital signal flows respectively, and then the multiple sub digital signal flows are synthesized into a large bandwidth signal; further, the large bandwidth signal is converted into an analog signal by using a digital to analog converter, and finally the analog signal is converted into a radio frequency signal through up-conversion. Because the embodiment of the present invention can divide a large bandwidth into multiple subbands and can process multiple sub digital signal flows at a transmitting end and a receiving end independently, no complex post-processing needs to be performed on the analog signal after the digital to analog conversion is performed, which can reduce the signal processing complexity of a transceiver, thereby improving system performance.

[0151] Compared with the technical solution in the prior art where a processing speed of a DAC/ADC is increased by using a frequency domain method or a time domain method, the embodiments of the present invention have a lower complexity during signal processing, signals are not easily distorted, and no joint control on multiple DACs/ADCs exists. Compared with the technical solution where a signal bandwidth is reduced in the prior art, the present invention reduces the number of DACs and requirements for analog intermediate frequency processing devices of a transmitting end. Compared with the existing frequency domain multichannel technology, the present invention does not need to reserve a guard space between each channel. In addition, frequency bands can be divided freely without restriction, and the system features powerful scalability. Furthermore, the embodiments of the present invention provide a complete one-to-one sending and receiving solution, and support a system with multi-polarized antennas and/or multiple antennas.

[0152] A person of ordinary skill in the art may be aware that, in combination with the examples described in the embodiments disclosed in this specification, units and algorithm steps may be implemented by electronic hardware, or a combination of computer software and electronic hardware. Whether the functions are performed by hardware or software depends on particular applications and design constraint conditions of the technical solutions. A person skilled in the art may use different methods to implement the described functions for each particular application, but it should not be considered that the implementation goes beyond the scope of the present invention.

[0153] It may be clearly understood by a person skilled in the art that, for the purpose of convenient and brief description, for a detailed working process of the foregoing system, apparatus, and unit, reference may be made to the corresponding process in the foregoing method embodiments, and the details will not be described herein again.

[0154] In the several embodiments provided in the present application, it should be understood that the disclosed system, apparatus, and method may be implemented in other manners. For example, the described apparatus embodiments are merely exemplary. For example, the unit division is merely logical function division and may be other division in actual implementation. For example, a plurality of units or components may be combined or integrated into another system, or some features may be ignored or not performed. In addition, the displayed or discussed mutual couplings or direct couplings or communication connections may be implemented

through some interfaces. The indirect couplings or communication connections between the apparatuses or units may be implemented in electronic, mechanical, or other forms.

[0155] The units described as separate parts may or may not be physically separate, and parts displayed as units may or may not be physical units, may be located in one position, or may be distributed on a plurality of network units. A part or all of the units may be selected according to actual needs to achieve the objectives of the solutions of the embodiments.

[0156] In addition, functional units in the embodiments of the present invention may be integrated into one processing unit, or each of the units may exist alone physically, or two or more units are integrated into one unit.

[0157] When the functions are implemented in a form of a software functional unit and sold or used as an independent product, the functions may be stored in a computer-readable storage medium. Based on such an understanding, the technical solutions of the present invention essentially, or the part contributing to the prior art, or a part of the technical solutions may be implemented in a form of a software product. The computer software product is stored in a storage medium, and includes several instructions for instructing a computer device (which may be a personal computer, a server, or a network device) to perform all or a part of the steps of the methods described in the embodiments of the present invention. The foregoing storage medium includes: any medium that can store program code, such as a USB flash drive, a removable hard disk, a read-only memory (Read-Only Memory, ROM), a random access memory (Random Access Memory, RAM), a magnetic disk, or an optical disc.

[0158] The foregoing descriptions are merely specific embodiments of the present invention, but are not intended to limit the protection scope of the present invention. Any variation or replacement readily figured out by a person skilled in the art within the technical scope disclosed in the present invention shall fall within the protection scope of the present invention. Therefore, the protection scope of the present invention shall be subject to the protection scope of the claims.

Claims

1. A transceiver, comprising a receiving circuit and a transmitting circuit;
   wherein the transmitting circuit comprises:

   a first digital interface circuit (110, 210, 310, 410, 510, 610, 701, 801, 901, 1001, 1101), configured to obtain, in a predetermined bandwidth, first data to be sent, and decompose the first data into N parallel first sub digital signal flows, wherein a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer greater than 1;
   a first digital modulation circuit (120, 220, 320, 420, 520, 620), configured to receive the N first sub digital signal flows, and modulate the N first sub digital signal flows to obtain N first modulated signals;
   a first frequency relocation circuit (130, 230, 330, 430, 530, 630), configured to receive the N first modulated signals, and perform frequency relocation on the N first modulated signals, so that there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation;
   a first synthesizer (140, 240, 340, 440, 540, 640), configured to synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, wherein M is a positive integer smaller than or equal to N;
   a first digital to analog converter (150, 250, 350, 450, 550, 650), configured to receive the first bandwidth signal, and perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal; and
   a first up-conversion circuit (160, 260, 360, 460, 560, 660), configured to receive the first analog signal, and convert the first analog signal into a first frequency signal, so that the radio frequency signal is sent to the receiving circuit by a first antenna;

   wherein the receiving circuit comprises:

   a down-conversion circuit (665), configured to convert a radio frequency signal received on a receiving antenna into an analog signal;
   an intermediate frequency power divider (655), configured to decompose the analog signal into N parallel sub analog signal flows;
   a second frequency relocation circuit (645), configured to perform frequency relocation on the N parallel sub analog signal flows;
   N analog to digital converters (635), configured to perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows;
   a digital demodulation circuit (625), configured to perform demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals; and
   a second digital interface circuit (615), configured to synthesize the N parallel demodulated signals into second data.

2. The transceiver according to claim 1, the transmitting circuit further comprising:

a second synthesizer (270, 380, 480), configured to synthesize L first modulated signals of the N first modulated signals that have undergone frequency relocation into a second bandwidth signal, wherein the L first modulated signals are different from the M first modulated signals, L is a positive integer, and a sum of L and M is smaller than or equal to N; and

a second digital to analog converter (280, 390, 490), configured to receive the second bandwidth signal, and perform digital to analog conversion on the second bandwidth signal to obtain a second analog signal;

wherein the first up-conversion circuit is configured to receive the first analog signal and the second analog signal, and synthesize the first analog signal and the second analog signal into the radio frequency signal.

3. The transceiver according to claim 2, wherein the first up-conversion circuit is further configured to perform frequency relocation on the first analog signal and the second analog signal respectively before synthesizing the first analog signal and the second analog signal into the radio frequency signal.

4. The transceiver according to claim 1, wherein:

the first digital interface circuit is further configured to obtain, in the predetermined bandwidth, second data to be sent, and decompose the second data into N parallel second sub digital signal flows, wherein a bandwidth occupied by each second sub digital signal flow of the N second sub digital signal flows is smaller than the predetermined bandwidth; and

the first digital modulation circuit is further configured to receive the N second sub digital signal flows, and modulate the N second sub digital signal flows to obtain N second modulated signals;

the transmitting circuit further comprising:

a third frequency relocation circuit (370, 470), configured to receive the N second modulated signals, and perform frequency relocation on the N second modulated signals, wherein there is no frequency band gap between adjacent second modulated signals of the N second modulated signals that have undergone frequency relocation;

a second synthesizer (380, 480), configured to synthesize P signals of the N second modulated signals that have undergone frequency relocation into a second bandwidth signal, wherein P is a positive integer smaller than or equal to N; and

a second digital to analog converter (390, 490), configured to receive the second bandwidth signal, and perform digital to analog conversion on the second bandwidth signal to obtain a second analog signal;

wherein the first up-conversion circuit is specifically configured to receive the first analog signal, and convert the first analog signal into the first radio frequency signal, so that the first radio frequency signal is sent by the first antenna; and

the transmitting circuit further comprising a second up-conversion circuit (395, 495), wherein the second up-conversion circuit is specifically configured to receive the second analog signal, and convert the second analog signal into a second radio frequency signal, so that the second radio frequency signal is sent by a second antenna.

5. The transceiver according to claim 4, wherein the first digital modulation circuit comprises N modulators, wherein the N modulators modulate the N first sub digital signal flows respectively, and the N modulators are further configured to modulate the N second sub digital signal flows.

6. The transceiver according to claim 1, wherein the first antenna is a dual-polarized antenna,

wherein the dual-polarized antenna comprises an H-polarized antenna and a V-polarized antenna; and

the first digital interface circuit is further configured to obtain, in the predetermined bandwidth, second data to be sent, and decompose the second data into K parallel second sub digital signal flows, wherein a bandwidth occupied by each second sub digital signal flow of the K second sub digital signal flows is smaller than the predetermined bandwidth and K is a positive integer;

the transmitting circuit further comprising:

a second digital modulation circuit (425), configured to receive the K second sub digital signal flows, and modulate the K second sub digital signal flows on the V-polarized antenna to obtain K second modulated signals, wherein K is a positive integer greater than 1;

a third frequency relocation circuit (470), configured to receive the K second modulated signals, and perform frequency relocation on the K second modulated signals, wherein there is no frequency band gap between adjacent second modulated signals of the K second modulated signals that have undergone frequency relocation;

a second synthesizer (480), configured to synthesize at least two signals of the K second modulated signals that have undergone frequency relocation into a second bandwidth signal; and

a second digital to analog converter (490), configured to receive the second bandwidth signal, and perform digital to analog conversion on the second bandwidth signal to obtain a second analog signal; and
the transmitting circuit further comprising:

a second up-conversion circuit (495), configured to receive the second analog signal, and convert the second analog signal into a second radio frequency signal; and
a coupler (465), configured to couple the first radio frequency signal and the second radio frequency signal, so that the first radio frequency signal and the second radio frequency signal are sent by the dual-polarized antenna respectively, wherein the first radio frequency signal is sent by the H-polarized antenna and the second radio frequency signal is sent by the V-polarized antenna.

7. The transceiver according to claim 1, wherein the first antenna is a dual-polarized antenna, wherein the dual-polarized antenna comprises an H-polarized antenna and a V-polarized antenna;
the first digital interface circuit is further configured to obtain, in the predetermined bandwidth, second data to be sent, and decompose the second data into K parallel second sub digital signal flows, wherein a bandwidth occupied by each second sub digital signal flow of the K second sub digital signal flows is smaller than the predetermined bandwidth and K is a positive integer; and the first modulation circuit comprises N+K modulators, wherein the N modulators modulate the N first sub digital signal flows respectively and the K modulators modulate the K second sub digital signal flows respectively;
the transmitting circuit further comprising:

a second frequency relocation circuit, configured to receive the K second modulated signals, and perform frequency relocation on the K second modulated signals, wherein there is no frequency band gap between adjacent second modulated signals of the K second modulated signals that have undergone frequency relocation;
a second synthesizer, configured to synthesize at least two signals of the K second modulated signals that have undergone frequency relocation into a second bandwidth signal; and
a second digital to analog converter, configured to receive the second bandwidth signal, and perform digital to analog conversion on the second bandwidth signal to obtain a second analog signal; and
the transmitting circuit further comprising: a second up-conversion circuit, configured to receive the second analog signal, and convert the second analog signal into a second radio frequency signal; and a coupler, configured to couple the first radio frequency signal and the second radio frequency signal, so that the first radio frequency signal and the second radio frequency signal are sent by the dual-polarized antenna respectively, wherein the first radio frequency signal is sent by the H-polarized antenna and the second radio frequency signal is sent by the V-polarized antenna.

8. The transceiver according to any one of claims 1 to 7, wherein the first synthesizer comprises an adder (1210), wherein the adder is configured to add the N first modulated signals that have undergone frequency relocation to synthesize the N first modulated signals into a first bandwidth signal.

9. The transceiver according to any one of claims 1 to 8, wherein N is at least 4 and the first data is at least one binary digital signal flow.

10. A method for communication, comprising a method for transmitting data and a method for receiving data; wherein the method for transmitting data comprises:

obtaining (1310), in a predetermined bandwidth, first data to be sent, and decomposing the first data into N parallel first sub digital signal flows, wherein a bandwidth occupied by each first sub digital signal flow of the N first sub digital signal flows is smaller than the predetermined bandwidth and N is a positive integer greater than 1;
modulating (1320) the N first sub digital signal flows to obtain N first modulated signals;
performing (1330) frequency relocation on the N first modulated signals, so that there is no frequency band gap between adjacent first modulated signals of the N first modulated signals that have undergone frequency relocation;
synthesizing (1340) M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, wherein M is a positive integer smaller than or equal to N;
performing (1350), by a first digital to analog converter, digital to analog conversion on the first bandwidth signal to obtain a first analog signal; and
converting (1360) the first analog signal into a radio frequency signal, so that the radio frequency signal is sent to the receiving circuit by a first antenna;

wherein the method for receiving data comprises:

converting a second radio frequency signal re-

ceived on a receiving antenna into a second analog signal;
decomposing the second analog signal into N parallel sub analog signal flows;
performing frequency relocation on the N parallel sub analog signal flows;
performing analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows;
performing demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals; and
synthesizing the N parallel demodulated signals into the first data.

11. The method according to claim 10, the method for transmitting data further comprising:

synthesizing L first modulated signals of the N first modulated signals that have undergone frequency relocation into a second bandwidth signal, wherein the L first modulated signals are different from the M first modulated signals, L is a positive integer, and a sum of L and M is smaller than or equal to N;
performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; and
synthesizing the first analog signal and the second analog signal into the radio frequency signal.

12. The method according to claim 11, the method for transmitting data further comprising:
performing frequency relocation on the first analog signal and the second analog signal respectively before synthesizing the first analog signal and the second analog signal into the radio frequency signal.

13. The method according to claim 10, the method for transmitting data further comprising:

obtaining, in the predetermined bandwidth, second data to be sent, and decomposing the second data into N parallel second sub digital signal flows, wherein a bandwidth occupied by each second sub digital signal flow of the N second sub digital signal flows is smaller than the predetermined bandwidth;
modulating the N second sub digital signal flows to obtain N second modulated signals;
performing frequency relocation on the N second modulated signals, so that there is no frequency band gap between adjacent second modulated signals of the N second modulated signals that have undergone frequency relocation;
synthesizing P signals of the N second modulated signals that have undergone frequency relocation into a second bandwidth signal, wherein P is a positive integer smaller than or equal to N;
performing digital to analog conversion on the second bandwidth signal to obtain a second analog signal; and
converting the second analog signal into a second radio frequency signal, so that the second radio frequency signal is sent by a second antenna.

Patentansprüche

1. Sende-/Empfangsvorrichtung, umfassend eine Empfangsschaltung und eine Sendeschaltung; wobei die Sendeschaltung Folgendes umfasst:

eine erste digitale Schnittstellenschaltung (110, 210, 310, 410, 510, 610, 701, 801, 901, 1001,1101), ausgelegt zum Erhalten, in einer vorbestimmten Bandbreite, von ersten zu sendenden Daten, und Zerlegen der ersten Daten in N parallele erste digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem ersten digitalen Signalteilfluss der N ersten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist und wobei N eine positive ganze Zahl größer als 1 ist;
eine erste digitale Modulationsschaltung (120, 220, 320, 420, 520, 620), ausgelegt zum Empfangen der N ersten digitalen Signalteilflüsse und Modulieren der N ersten digitalen Signalteilflüsse, um N erste modulierte Signale zu erhalten;
eine erste Frequenzverschiebungsschaltung (130, 230, 330, 430, 530, 630), ausgelegt zum Empfangen der N ersten modulierten Signale und Durchführen von Frequenzverschiebung auf den N ersten modulierten Signalen, sodass es keine Frequenzbandlücke zwischen angrenzenden ersten modulierten Signalen der N ersten modulierten Signale gibt, die Frequenzverschiebung durchlaufen haben;
einen ersten Synthetisator (140, 240, 340, 440, 540, 640), ausgelegt zum Synthetisieren von M ersten modulierten Signalen der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein erstes Bandbreitensignal, wobei M eine positive ganze Zahl kleiner oder gleich N ist;
einen ersten Digital-Analog-Wandler (150, 250, 350, 450, 550, 650), ausgelegt zum Empfangen des ersten Bandbreitensignals und Durchführen von Digital-zu-Analog-Umwandlung auf dem ersten Bandbreitensignal, um ein erstes analoges Signal zu erhalten; und
eine erste Aufwärtswandlungsschaltung (160,

260, 360, 460, 560, 660), ausgelegt zum Empfangen des ersten analogen Signals und Umwandeln des ersten analogen Signals in ein erstes Frequenzsignal, sodass das Funkfrequenzsignal durch eine erste Antenne zur Empfangsschaltung gesendet wird;
wobei die Empfangsschaltung Folgendes umfasst:

eine Abwärtswandlungsschaltung (665), ausgelegt zum Umwandeln eines an einer Empfangsantenne empfangenen Funkfrequenzsignals in ein analoges Signal;
einen Zwischenfrequenzleistungsteiler (655), ausgelegt zum Zerlegen des analogen Signals in N parallele analoge Signalteilflüsse;
eine zweite Frequenzverschiebungsschaltung (645), ausgelegt zum Durchführen von Frequenzverschiebung auf den N parallelen analogen Signalteilflüssen;
N Analog-Digital-Wandler (635), ausgelegt zum Durchführen von Analog-zu-Digital-Umwandlung auf den N parallelen analogen Signalteilflüssen, um entsprechend N parallele digitale Signalteilflüsse zu erhalten;
eine digitale Demodulationsschaltung (625), ausgelegt zum Durchführen von Demodulationsverarbeitung auf den N parallelen digitalen Signalteilflüssen, um N parallele demodulierte Signale zu erhalten; und
eine zweite digitale Schnittstellenschaltung (615), ausgelegt zum Synthetisieren der N parallelen demodulierten Signale in zweite Daten.

2. Sende-/Empfangsvorrichtung nach Anspruch 1, wobei die Sendeschaltung ferner Folgendes umfasst:

einen zweiten Synthetisator (270, 380, 480), ausgelegt zum Synthetisieren von L ersten modulierten Signalen der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal, wobei die L ersten modulierten Signale von den M ersten modulierten Signalen verschieden sind, L eine positive ganze Zahl ist und eine Summe von L und M kleiner oder gleich N ist; und
einen zweiten Digital-Analog-Wandler (280, 390, 490), ausgelegt zum Empfangen des zweiten Bandbreitensignals und Durchführen von Digital-zu-Analog-Umwandlung auf dem zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten;
wobei die erste Aufwärtswandlungsschaltung ausgelegt ist zum Empfangen des ersten analogen Signals und des zweiten analogen Signals und Synthetisieren des ersten analogen Signals und des zweiten analogen Signals in das Funkfrequenzsignal.

3. Sende-/Empfangsvorrichtung nach Anspruch 2, wobei die erste Aufwärtswandlungsschaltung ferner ausgelegt ist zum Durchführen von Frequenzverschiebung auf dem ersten analogen Signal bzw. dem zweiten analogen Signal vor dem Synthetisieren des ersten analogen Signals und des zweiten analogen Signals in das Funkfrequenzsignal.

4. Sende-/Empfangsvorrichtung nach Anspruch 1, wobei
die erste digitale Schnittstellenschaltung ferner ausgelegt ist zum Erhalten, in der vorbestimmten Bandbreite, von zweiten zu sendenden Daten, und Zerlegen der zweiten Daten in N parallele zweite digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem zweiten digitalen Signalteilfluss der N zweiten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist; und
die erste digitale Modulationsschaltung ferner ausgelegt ist zum Empfangen der N zweiten digitalen Signalteilflüsse und Modulieren der N zweiten digitalen Signalteilflüsse, um N zweite modulierte Signale zu erhalten;
wobei die Sendeschaltung ferner Folgendes umfasst:

eine dritte Frequenzverschiebungsschaltung (370, 470), ausgelegt zum Empfangen der N zweiten modulierten Signale und Durchführen von Frequenzverschiebung auf den N zweiten modulierten Signalen, wobei es keine Frequenzbandlücke zwischen angrenzenden zweiten modulierten Signalen der N zweiten modulierten Signale gibt, die Frequenzverschiebung durchlaufen haben;
einen zweiten Synthetisator (380, 480), ausgelegt zum Synthetisieren von P Signalen der N zweiten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal, wobei P eine positive ganze Zahl kleiner oder gleich N ist; und
einen zweiten Digital-Analog-Wandler (390, 490), ausgelegt zum Empfangen des zweiten Bandbreitensignals und Durchführen von Digital-zu-Analog-Umwandlung auf dem zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten;
wobei die erste Aufwärtswandlungsschaltung spezifisch ausgelegt ist zum Empfangen des ersten analogen Signals und Umwandeln des ersten analogen Signals in das erste Funkfrequenzsignal, sodass das erste Funkfrequenzsignal durch die erste Antenne gesendet wird; und
wobei die Sendeschaltung ferner eine zweite Aufwärtswandlungsschaltung (395, 495) um-

fasst, wobei die zweite Aufwärtswandlungsschaltung spezifisch ausgelegt ist zum Empfangen des zweiten analogen Signals und zum Umwandeln des zweiten analogen Signals in ein zweites Funkfrequenzsignal, sodass das zweite Funkfrequenzsignal durch eine zweite Antenne gesendet wird.

5. Sende-/Empfangsvorrichtung nach Anspruch 4, wobei die erste digitale Modulationsschaltung N Modulatoren umfasst, wobei die N Modulatoren entsprechend die N ersten digitalen Signalteilflüsse modulieren und wobei die N Modulatoren ferner ausgelegt sind zum Modulieren der N zweiten digitalen Signalteilflüsse.

6. Sende-/Empfangsvorrichtung nach Anspruch 1, wobei die erste Antenne eine dual polarisierte Antenne ist, wobei die dual polarisierte Antenne eine H-polarisierte Antenne und eine V-polarisierte Antenne umfasst; und
wobei die erste digitale Schnittstellenschaltung ferner ausgelegt ist zum Erhalten, in der vorbestimmten Bandbreite, von zweiten zu sendenden Daten, und Zerlegen der zweiten Daten in K parallele zweite digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem zweiten digitalen Signalteilfluss der K zweiten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist, und wobei K eine positive ganze Zahl ist;
wobei die Sendeschaltung ferner Folgendes umfasst:

eine zweite digitale Modulationsschaltung (425), ausgelegt zum Empfangen der K zweiten digitalen Signalteilflüsse und Modulieren der K zweiten digitalen Signalteilflüsse auf der V-polarisierten Antenne, um K zweite modulierte Signale zu erhalten, wobei K eine positive ganze Zahl größer als 1 ist;
eine dritte Frequenzverschiebungsschaltung (470), ausgelegt zum Empfangen der K zweiten modulierten Signale und Durchführen von Frequenzverschiebung auf den K zweiten modulierten Signalen, wobei es keine Frequenzbandlücke zwischen angrenzenden zweiten modulierten Signalen der K zweiten modulierten Signale gibt, die Frequenzverschiebung durchlaufen haben;
einen zweiten Synthetisator (480), ausgelegt zum Synthetisieren von mindestens zwei Signalen der K zweiten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal; und
einen zweiten Digital-Analog-Wandler (490), ausgelegt zum Empfangen des zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten; und
wobei die Sendeschaltung ferner Folgendes umfasst:

eine zweite Aufwärtswandlungsschaltung (495), ausgelegt zum Empfangen des zweiten analogen Signals und Umwandeln des zweiten analogen Signals in ein zweites Funkfrequenzsignal; und
einen Koppler (465), ausgelegt zum Koppeln des ersten Funkfrequenzsignals und des zweiten Funkfrequenzsignals, sodass das erste Funkfrequenzsignal und das zweite Funkfrequenzsignal entsprechend durch die dual-polarisierte Antenne gesendet werden, wobei das erste Funkfrequenzsignal durch die H-polarisierte Antenne gesendet wird und das zweite Funkfrequenzsignal durch die V-polarisierte Antenne gesendet wird.

7. Sende-/Empfangsvorrichtung nach Anspruch 1, wobei die erste Antenne eine dual polarisierte Antenne ist, wobei die dual polarisierte Antenne eine H-polarisierte Antenne und eine V-polarisierte Antenne umfasst;
wobei die erste digitale Schnittstellenschaltung ferner ausgelegt ist zum Erhalten, in der vorbestimmten Bandbreite, von zweiten zu sendenden Daten, und Zerlegen der zweiten Daten in K parallele zweite digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem zweiten digitalen Signalteilfluss der K zweiten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist, und wobei K eine positive ganze Zahl ist; und
wobei die erste digitale Modulationsschaltung N+K Modulatoren umfasst, wobei die N Modulatoren entsprechend die N ersten digitalen Signalteilflüsse modulieren und die K Modulatoren entsprechend die K zweiten digitalen Signalteilflüsse modulieren. wobei die Sendeschaltung ferner Folgendes umfasst:

eine zweite Frequenzverschiebungsschaltung, ausgelegt zum Empfangen der K zweiten modulierten Signale und Durchführen von Frequenzverschiebung auf den K zweiten modulierten Signalen, wobei es keine Frequenzbandlücke zwischen angrenzenden zweiten modulierten Signalen der K zweiten modulierten Signale gibt, die Frequenzverschiebung durchlaufen haben;
einen zweiten Synthetisator, ausgelegt zum Synthetisieren von mindestens zwei Signalen der K zweiten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal; und
einen zweiten Digital-Analog-Wandler, ausge-

legt zum Empfangen des zweiten Bandbreitensignals und Durchführen von Digital-zu-Analog-Umwandlung auf dem zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten; und
wobei die Sendeschaltung ferner Folgendes umfasst:

eine zweite Aufwärtswandlungsschaltung, ausgelegt zum Empfangen des zweiten analogen Signals und Umwandeln des zweiten analogen Signals in ein zweites Funkfrequenzsignal; und
einen Koppler, ausgelegt zum Koppeln des ersten Funkfrequenzsignals und des zweiten Funkfrequenzsignals, sodass das erste Funkfrequenzsignal und das zweite Funkfrequenzsignal entsprechend durch die dual-polarisierte Antenne gesendet werden, wobei das erste Funkfrequenzsignal durch die H-polarisierte Antenne gesendet wird und das zweite Funkfrequenzsignal durch die V-polarisierte Antenne gesendet wird.

8. Sende-/Empfangsvorrichtung nach einem der Ansprüche 1 bis 7, wobei der erste Synthetisator einen Addierer (1210) umfasst, wobei der Addierer ausgelegt ist zum Addieren der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, um die N ersten modulierten Signale in ein erstes Bandbreitensignal zu synthetisieren.

9. Sende-/Empfangsvorrichtung nach einem der Ansprüche 1 bis 8, wobei N mindestens 4 ist und die ersten Daten mindestens ein binärer digitaler Signalstrom sind.

10. Verfahren zur Kommunikation, ein Verfahren zum Senden von Daten und ein Verfahren zum Empfangen von Daten umfassend;
wobei das Verfahren zum Senden von Daten Folgendes umfasst:

Erhalten (1310), in einer vorbestimmten Bandbreite, von ersten zu sendenden Daten, und Zerlegen der ersten Daten in N parallele erste digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem ersten digitalen Signalteilfluss der N ersten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist und wobei N eine positive ganze Zahl größer als 1 ist;
Modulieren (1320) der N ersten digitalen Signalteilflüsse, um N erste modulierte Signale zu erhalten;
Durchführen (1330) von Frequenzverschiebung auf den N ersten modulierten Signalen, sodass es keine Frequenzbandlücke zwischen angrenzenden ersten modulierten Signalen der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, gibt;
Synthetisieren (1340) von M ersten modulierten Signalen der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein erstes Bandbreitensignal, wobei M eine positive ganze Zahl kleiner oder gleich N ist;
Durchführen (1350), durch einen ersten Digital-Analog-Wandler, einer Digital-zu-Analog-Umwandlung auf dem ersten Bandbreitensignal, um ein erstes analoges Signal zu erhalten; und
Umwandeln (1360) des ersten analogen Signals in ein Funkfrequenzsignal, sodass das Funkfrequenzsignal durch eine erste Antenne an die Empfangsschaltung gesendet wird;
wobei das Verfahren zum Empfangen von Daten Folgendes umfasst:

Umwandeln eines an einer Empfangsantenne empfangenen zweiten Funkfrequenzsignals in ein zweites analoges Signal;
Zerlegen des zweiten analogen Signals in N parallele analoge Signalteilströme;
Durchführen von Frequenzverschiebung auf den N parallelen analogen Signalteilströmen;
Durchführen von Analog-zu-Digital-Umwandlung auf den N parallelen analogen Signalteilflüssen, um entsprechend N parallele digitale Signalteilflüsse zu erhalten;
Durchführen von Demodulationsverarbeitung auf den N parallelen digitalen Signalteilflüssen, um N parallele demodulierte Signale zu erhalten; und
Synthetisieren der N parallelen demodulierten Signale in die ersten Daten.

11. Verfahren nach Anspruch 10, wobei das Verfahren zum Senden von Daten ferner Folgendes umfasst:

Synthetisieren von L ersten modulierten Signalen der N ersten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal, wobei die L ersten modulierten Signale von den M ersten modulierten Signalen verschieden sind, L eine positive ganze Zahl ist und eine Summe von L und M kleiner oder gleich N ist;
Durchführen einer Digital-zu-Analog-Umwandlung auf dem zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten; und
Synthetisieren des ersten analogen Signals und des zweiten analogen Signal in das Funkfrequenzsignal.

12. Verfahren nach Anspruch 11, wobei das Verfahren zum Senden von Daten ferner Folgendes umfasst:

Durchführen von Frequenzverschiebung auf dem ersten analogen Signal bzw. dem zweiten analogen Signal vor dem Synthetisieren des ersten analogen Signals und des zweiten analogen Signals in das Funkfrequenzsignal.

13. Verfahren nach Anspruch 10, wobei das Verfahren zum Senden von Daten ferner Folgendes umfasst:

Erhalten, in der vorbestimmten Bandbreite, von zweiten zu sendenden Daten, und Zerlegen der zweiten Daten in N parallele zweite digitale Signalteilflüsse, wobei eine Bandbreite, die von jedem zweiten digitalen Signalteilfluss der N zweiten digitalen Signalteilflüsse belegt wird, kleiner als die vorbestimmte Bandbreite ist;
Modulieren der N zweiten digitalen Siignalteilflüsse, um N zweite modulierte Signale zu erhalten;
Durchführen von Frequenzverschiebung auf den N zweiten modulierten Signalen, sodass es keine Frequenzbandlücke zwischen angrenzenden zweiten modulierten Signalen der N zweiten modulierten Signale, die Frequenzverschiebung durchlaufen haben, gibt;
Synthetisieren von P Signalen der N zweiten modulierten Signale, die Frequenzverschiebung durchlaufen haben, in ein zweites Bandbreitensignal, wobei P eine positive ganze Zahl kleiner oder gleich N ist;
Durchführen einer Digital-zu-Analog-Umwandlung auf dem zweiten Bandbreitensignal, um ein zweites analoges Signal zu erhalten; und
Umwandeln des zweiten analogen Signals in ein zweites Funkfrequenzsignal, sodass das zweite Funkfrequenzsignal durch eine zweite Antenne gesendet wird;

Revendications

1. Émetteur-récepteur, comprenant un circuit de réception et un circuit d'émission ;
le circuit d'émission comprenant :

un premier circuit d'interface numérique (110, 210, 310, 410, 510, 610, 701, 801, 901, 1001, 1101) configuré pour obtenir, dans une largeur de bande prédéterminée, des premières données à envoyer, et décomposer les premières données en N premiers sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque premier sous-flux de signaux numériques des N premiers sous-flux de signaux numériques étant inférieure à la largeur de bande prédéterminée et N étant un nombre entier positif supérieur à 1 ;
un premier circuit de modulation numérique (120, 220, 320, 420, 520, 620) configuré pour recevoir les N premiers sous-flux de signaux numériques, et moduler les N premiers sous-flux de signaux numériques pour obtenir N premiers signaux modulés ;
un premier circuit de translation de fréquence (130, 230, 330, 430, 530, 630) configuré pour recevoir les N premiers signaux modulés, et réaliser une translation de fréquence sur les N premiers signaux modulés, de telle sorte qu'il n'y a pas d'espace de bande de fréquence entre des premiers signaux modulés adjacents des N premiers signaux modulés qui ont subi une translation de fréquence ;
un premier synthétiseur (140, 240, 340, 440, 540, 640), configuré pour synthétiser M premiers signaux modulés des N premiers signaux modulés qui ont subi une translation de fréquence, en un premier signal de largeur de bande, M étant un nombre entier positif inférieur ou égal à N ;
un premier convertisseur numérique-analogique (150, 250, 350, 450, 550, 650) configuré pour recevoir le premier signal de largeur de bande, et réaliser une conversion numérique-analogique sur le premier signal de largeur de bande pour obtenir un premier signal analogique ; et
un premier circuit de conversion ascendante (160, 260, 360, 460, 560, 660) configuré pour recevoir le premier signal analogique, et convertir le premier signal analogique en un premier signal de fréquence, de telle sorte que le signal radiofréquence est envoyé au circuit de réception par une première antenne ;
le circuit de réception comprenant :

un circuit de conversion descendante (665), configuré pour convertir un signal radiofréquence reçu sur une antenne de réception en un signal analogique ;
un diviseur de puissance à fréquence intermédiaire (655), configuré pour décomposer le signal analogique en N sous-flux de signaux analogiques parallèles ;
un deuxième circuit de translation de fréquence (645), configuré pour réaliser une translation de fréquence sur les N sous-flux de signaux analogiques parallèles ;
N convertisseurs analogiques-numériques (635), configurés pour réaliser une conversion analogique-numérique sur les N sous-flux de signaux analogiques parallèles respectivement pour obtenir N flux de signaux numériques parallèles ;
un circuit de démodulation numérique (625), configuré pour réaliser un traitement de démodulation sur les N flux de signaux

numériques parallèles pour obtenir N signaux démodulés parallèles ; et
un second circuit d'interface numérique (615), configuré pour synthétiser les N signaux démodulés parallèles en secondes données.

2. Émetteur-récepteur selon la revendication 1, le circuit d'émission comprenant en outre :

un second synthétiseur (270, 380, 480) configuré pour synthétiser L premiers signaux modulés des N premiers signaux modulés qui ont subi une translation de fréquence en un second signal de largeur de bande, les L premiers signaux modulés étant différents des M premiers signaux modulés, L étant un nombre entier positif, et une somme de L et M étant inférieure ou égale à N ; et
un second convertisseur numérique-analogique (280, 390, 490), configuré pour recevoir le second signal de largeur de bande, et réaliser une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ;
le premier circuit de conversion ascendante étant configuré pour recevoir le premier signal analogique et le second signal analogique, et synthétiser le premier signal analogique et le second signal analogique dans le signal radiofréquence.

3. Émetteur-récepteur selon la revendication 2, le premier circuit de conversion ascendante étant en outre configuré pour réaliser une translation de fréquence sur le premier signal analogique et le second signal analogique respectivement avant la synthétisation du premier signal analogique et du second signal analogique dans le signal radiofréquence.

4. Émetteur-récepteur selon la revendication 1,
le premier circuit d'interface numérique étant en outre configuré pour obtenir, dans la largeur de bande prédéterminée, des secondes données à envoyer, et décomposer les secondes données en N seconds sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque second sous-flux de signal numérique des N seconds sous-flux de signaux numériques étant inférieure à la largeur de bande prédéterminée ; et
le premier circuit de modulation numérique étant en outre configuré pour recevoir les N seconds sous-flux de signaux numériques, et moduler les N second sous-flux de signaux numériques pour obtenir N seconds signaux modulés ;
le circuit d'émission comprenant en outre :

un troisième circuit de translation de fréquence (370, 470) configuré pour recevoir les N seconds signaux modulés, et réaliser une translation de fréquence sur les N seconds signaux modulés, dans lequel il n'y a pas d'espace de bande de fréquence entre des seconds signaux modulés adjacents des N seconds signaux modulés qui ont subi une translation de fréquence ;
un second synthétiseur (380, 480), configuré pour synthétiser P signaux des N seconds signaux modulés qui ont subi une translation de fréquence en un second signal de largeur de bande, P étant un nombre entier positif inférieur ou égal à N ; et
un second convertisseur numérique-analogique (390, 490), configuré pour recevoir le second signal de largeur de bande, et réaliser une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ;
le premier circuit de conversion ascendante étant spécifiquement configuré pour recevoir le premier signal analogique, et convertir le premier signal analogique en le premier signal radiofréquence, de telle sorte que le premier signal radiofréquence est envoyé par la première antenne ; et
le circuit d'émission comprenant en outre un second circuit de conversion ascendante (395, 495), le second circuit de conversion ascendante étant spécifiquement configuré pour recevoir le second signal analogique, et convertir le second signal analogique en un second signal radiofréquence, de telle sorte que le second signal radiofréquence est envoyé par une seconde antenne.

5. Émetteur-récepteur selon la revendication 4, le premier circuit de modulation numérique comprenant N modulateurs, les N modulateurs modulant respectivement les N premiers sous-flux de signaux numériques, et les N modulateurs étant en outre configurés pour moduler les N seconds sous-flux de signaux numériques.

6. Émetteur-récepteur selon la revendication 1, la première antenne étant une antenne à double polarisation,
l'antenne à double polarisation comprenant une antenne à polarisation H et une antenne à polarisation V ; et
le premier circuit d'interface numérique étant en outre configuré pour obtenir, dans la largeur de bande prédéterminée, des secondes données à envoyer, et décomposer les secondes données en K seconds sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque second sous-flux de signal numérique des K seconds sous-flux de signaux numériques étant inférieure à

la largeur de bande prédéterminée et K étant un nombre entier positif ;
le circuit d'émission comprenant en outre :

un second circuit de modulation numérique (425), configuré pour recevoir les K seconds sous-flux de signaux numériques, et moduler les K seconds sous-flux de signaux numériques sur l'antenne à polarisation V pour obtenir K seconds signaux modulés, K étant un nombre entier positif supérieur à 1 ;
un troisième circuit de translation de fréquence (470), configuré pour recevoir les K seconds signaux modulés, et réaliser une translation de fréquence sur les K seconds signaux modulés, dans lequel il n'y a pas d'espace de bande de fréquence entre des seconds signaux modulés adjacents des K seconds signaux modulés qui ont subi une translation de fréquence ;
un second synthétiseur (480), configuré pour synthétiser au moins deux signaux des K seconds signaux modulés qui ont subi une translation de fréquence en un second signal de largeur de bande ; et
un second convertisseur numérique-analogique (490), configuré pour recevoir le second signal de largeur de bande, et réaliser une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ; et
le circuit d'émission comprenant en outre :

un second circuit de conversion ascendante (495), configuré pour recevoir le second signal analogique, et convertir le second signal analogique en un second signal radiofréquence ; et
un coupleur (465), configuré pour coupler le premier signal radiofréquence et le second signal radiofréquence, de telle sorte que le premier signal radiofréquence et le second signal radiofréquence sont envoyés par l'antenne à double polarisation respectivement, le premier signal radiofréquence étant envoyé par l'antenne à polarisation H et le second signal radiofréquence étant envoyé par l'antenne à polarisation V.

7. Émetteur-récepteur selon la revendication 1, la première antenne étant une antenne à double polarisation, l'antenne à double polarisation comprenant une antenne à polarisation H et une antenne à polarisation V ;
le premier circuit d'interface numérique étant en outre configuré pour obtenir, dans la largeur de bande prédéterminée, les secondes données à envoyer, et décomposer les secondes données en K seconds sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque second sous-flux de signal numérique des K seconds sous-flux de signaux numériques étant inférieure à la largeur de bande prédéterminée et K étant un nombre entier positif ; et
le premier circuit de modulation comprenant N+K modulateurs, les N modulateurs modulant respectivement les N premiers sous-flux de signaux numériques et les K modulateurs modulant respectivement les K seconds sous-flux de signaux numériques ;
le circuit d'émission comprenant en outre :

un deuxième circuit de translation de fréquence, configuré pour recevoir les K seconds signaux modulés, et réaliser une translation de fréquence sur les K seconds signaux modulés, dans lequel il n'y a pas d'intervalle de bande de fréquence entre des seconds signaux modulés adjacents des K seconds signaux modulés qui ont subi une translation de fréquence ;
un second synthétiseur, configuré pour synthétiser au moins deux signaux des K seconds signaux modulés qui ont subi une translation de fréquence en un second signal de largeur de bande ; et
un second convertisseur numérique-analogique, configuré pour recevoir le second signal de largeur de bande, et réaliser une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ; et
le circuit d'émission comprenant en outre :

un second circuit de conversion ascendante, configuré pour recevoir le second signal analogique, et convertir le second signal analogique en un second signal radiofréquence ; et
un coupleur, configuré pour coupler le premier signal radiofréquence et le second signal radiofréquence, de telle sorte que le premier signal radiofréquence et le second signal radiofréquence sont envoyés par l'antenne à double polarisation respectivement, le premier signal radiofréquence étant envoyé par l'antenne à polarisation H et le second signal radiofréquence étant envoyé par l'antenne à polarisation V.

8. Émetteur-récepteur selon l'une quelconque des revendications 1 à 7, le premier synthétiseur comprenant un additionneur (1210), l'additionneur étant configuré pour ajouter les N premiers signaux modulés qui ont subi une translation de fréquence pour synthétiser les N premiers signaux modulés en un premier signal de largeur de bande.

9. Émetteur-récepteur selon l'une quelconque des revendications 1 à 8, N étant au moins 4 et les premières données étant au moins un flux de signal numérique binaire.

10. Procédé de communication, comprenant un procédé d'émission de données et un procédé de réception de données ;
le procédé d'émission de données comprenant :

l'obtention (1310), dans une largeur de bande prédéterminée, de premières données à envoyer, et la décomposition des premières données en N premiers sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque premier sous-flux de signaux numériques des N premiers sous-flux de signaux numériques étant inférieure à la largeur de bande prédéterminée et N étant un nombre entier positif supérieur à 1 ;
la modulation (1320) des N premiers sous-flux de signaux numériques pour obtenir N premiers signaux modulés ;
la réalisation (1330) d'une translation de fréquence sur les N premiers signaux modulés, de telle sorte qu'il n'y a pas d'espace de bande de fréquence entre des premiers signaux modulés adjacents des N premiers signaux modulés qui ont subi une translation de fréquence ;
la synthèse (1340) de M premiers signaux modulés des N premiers signaux modulés qui ont subi une translation de fréquence en un premier signal de largeur de bande, M étant un nombre entier positif inférieur ou égal à N ;
la réalisation (1350), par un premier convertisseur numérique-analogique, d'une conversion numérique-analogique sur le premier signal de largeur de bande pour obtenir un premier signal analogique ;

et

la conversion (1360) du premier signal analogique en un signal radiofréquence, de telle sorte que le signal radiofréquence est envoyé au circuit de réception par une première antenne ;
le procédé de réception de données comprenant :

la conversion d'un second signal radiofréquence reçu sur une antenne de réception en un second signal analogique ;
la décomposition du second signal analogique en N sous-flux de signaux analogiques parallèles ;
la réalisation d'une translation de fréquence sur les N sous-flux de signaux analogiques parallèles ;
la réalisation d'une conversion analogique-numérique sur les N sous-flux de signaux analogiques parallèles respectivement pour obtenir N flux de signaux numériques parallèles ;
la réalisation d'un traitement de démodulation sur les N flux de signaux numériques parallèles pour obtenir N signaux démodulés parallèles ; et
la synthèse des N signaux démodulés parallèles dans les premières données.

11. Procédé selon la revendication 10, le procédé d'émission de données comprenant en outre :

la synthèse de L premiers signaux modulés des N premiers signaux modulés qui ont subi une translation de fréquence en un second signal de largeur de bande, les L premiers signaux modulés étant différents des M premiers signaux modulés, L étant un nombre entier positif, et une somme de L et M étant inférieure ou égale à N ;
la réalisation d'une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ; et
la synthèse du premier signal analogique et du second signal analogique dans le signal radiofréquence.

12. Procédé selon la revendication 11, le procédé d'émission de données comprenant en outre :
la réalisation d'une translation de fréquence sur le premier signal analogique et le second signal analogique respectivement avant la synthèse du premier signal analogique et du second signal analogique dans le signal radiofréquence.

13. Procédé selon la revendication 10, le procédé d'émission de données comprenant en outre :

l'obtention, dans la largeur de bande prédéterminée, de secondes données à envoyer, et la décomposition des secondes données en N seconds sous-flux de signaux numériques parallèles, une largeur de bande occupée par chaque second sous-flux de signal numérique des N seconds sous-flux de signaux numériques étant inférieure à la largeur de bande prédéterminée ;
la modulation des N second sous-flux de signaux numériques pour obtenir N seconds signaux modulés ;
la réalisation d'une translation de fréquence sur les N seconds signaux modulés, de telle sorte qu'il n'y a pas d'espace de bande de fréquence entre des seconds signaux modulés adjacents des N seconds signaux modulés qui ont subi une translation de fréquence ;
la synthèse de P signaux des N seconds signaux

modulés qui ont subi une translation de fréquence en un second signal de largeur de bande, P étant un nombre entier positif inférieur ou égal à N ;

la réalisation d'une conversion numérique-analogique sur le second signal de largeur de bande pour obtenir un second signal analogique ; et

la conversion du second signal analogique en un second signal radiofréquence, de sorte que le second signal radiofréquence est envoyé par une seconde antenne.

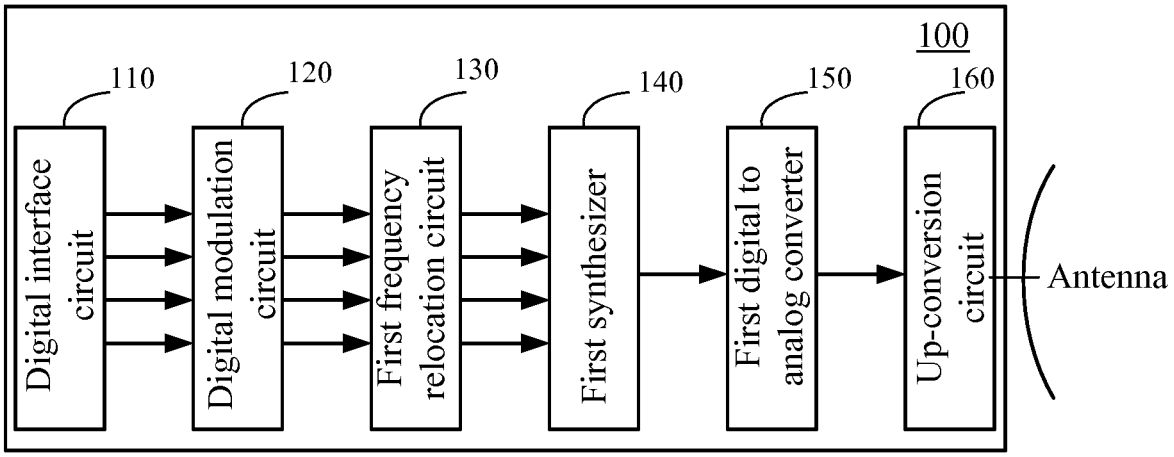
100
110
120
130
140
150
160
Digital interface circuit
Digital modulation circuit
First frequency relocation circuit
First synthesizer
First digital to analog converter
Up-conversion circuit
Antenna

FIG. 1

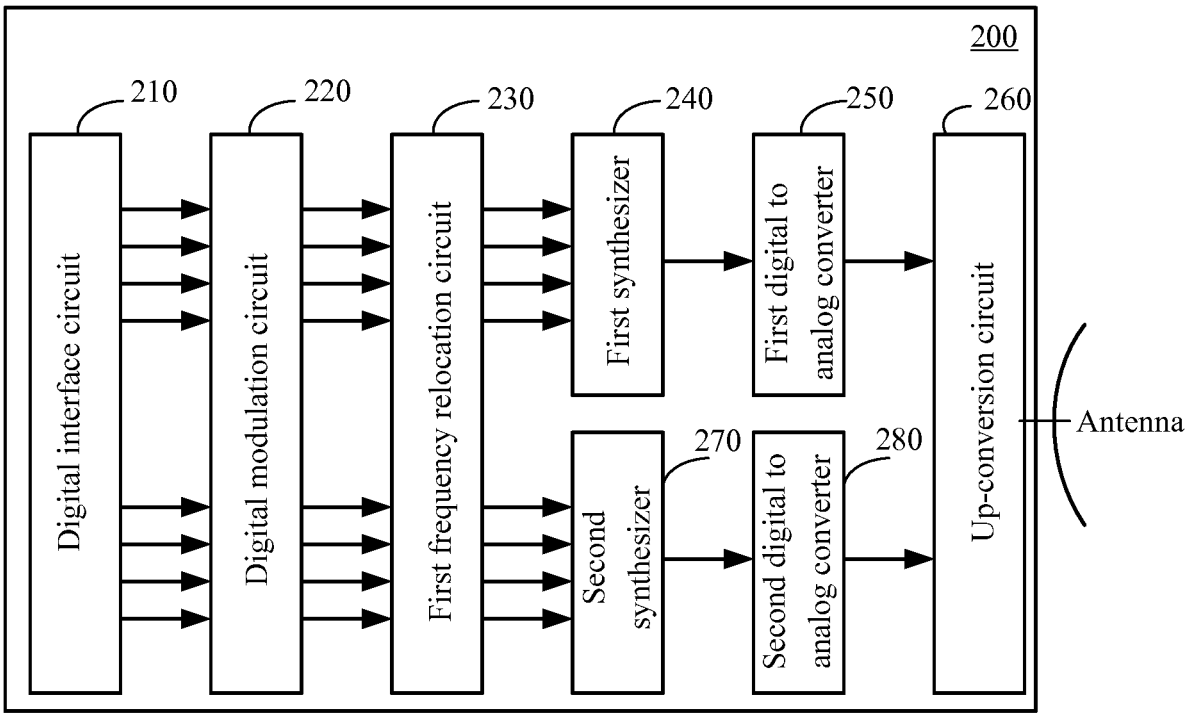
200
210
220
230
240
250
260
270
280
Digital interface circuit
Digital modulation circuit
First frequency relocation circuit
First synthesizer
First digital to analog converter
Second synthesizer
Second digital to analog converter
Up-conversion circuit
Antenna

FIG. 2

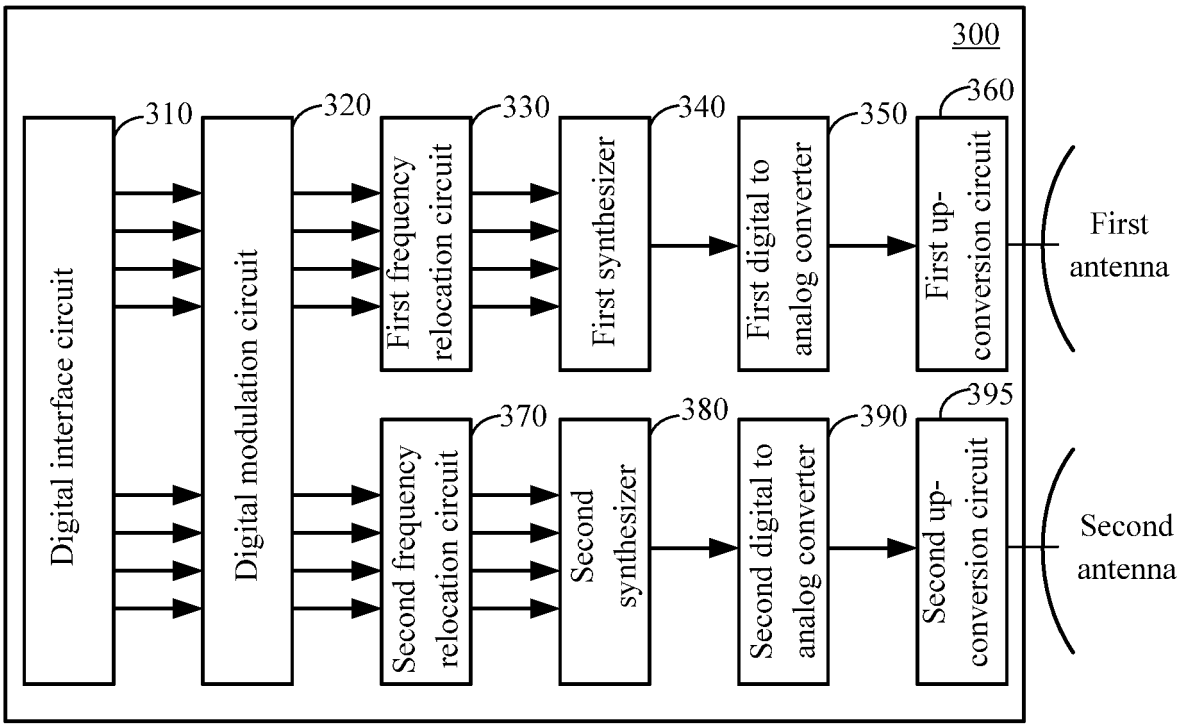
300
Digital interface circuit
310
Digital modulation circuit
320
First frequency relocation circuit
330
First synthesizer
340
First digital to analog converter
350
First up-conversion circuit
360
First antenna
Second frequency relocation circuit
370
Second synthesizer
380
Second digital to analog converter
390
Second up-conversion circuit
395
Second antenna

FIG. 3

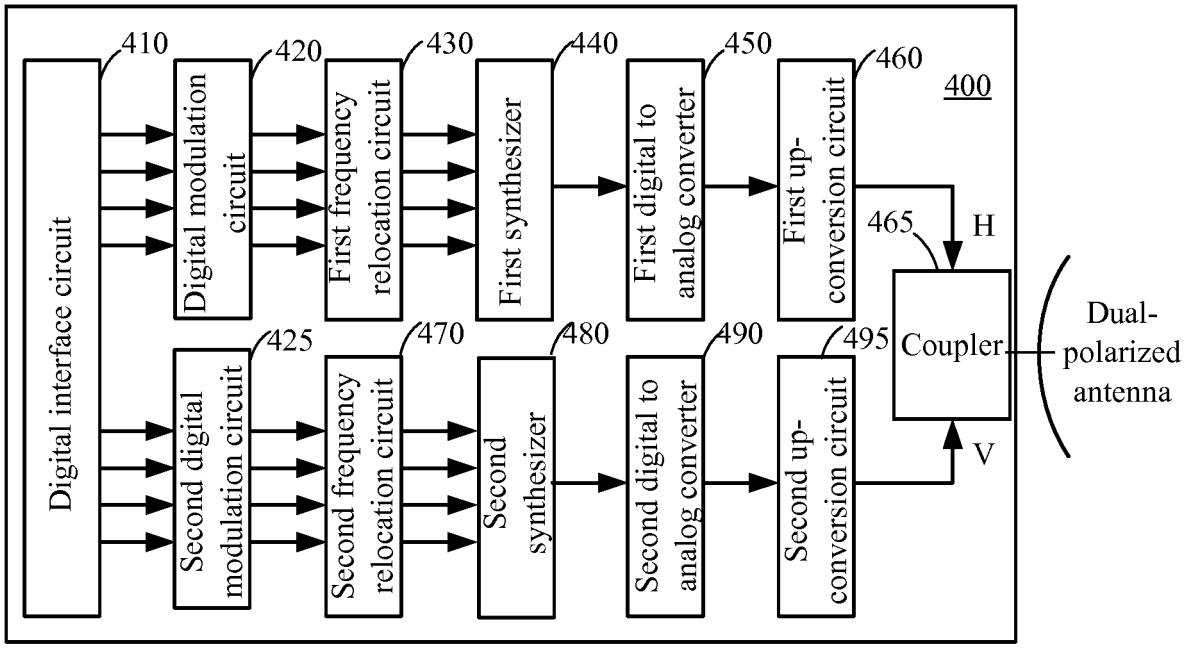
Digital interface circuit
410
Digital modulation circuit
420
First frequency relocation circuit
430
First synthesizer
440
First digital to analog converter
450
First up-conversion circuit
460
400
465
H
Coupler
Dual-polarized antenna
V
Second digital modulation circuit
425
Second frequency relocation circuit
470
Second synthesizer
480
Second digital to analog converter
490
Second up-conversion circuit
495

FIG. 4

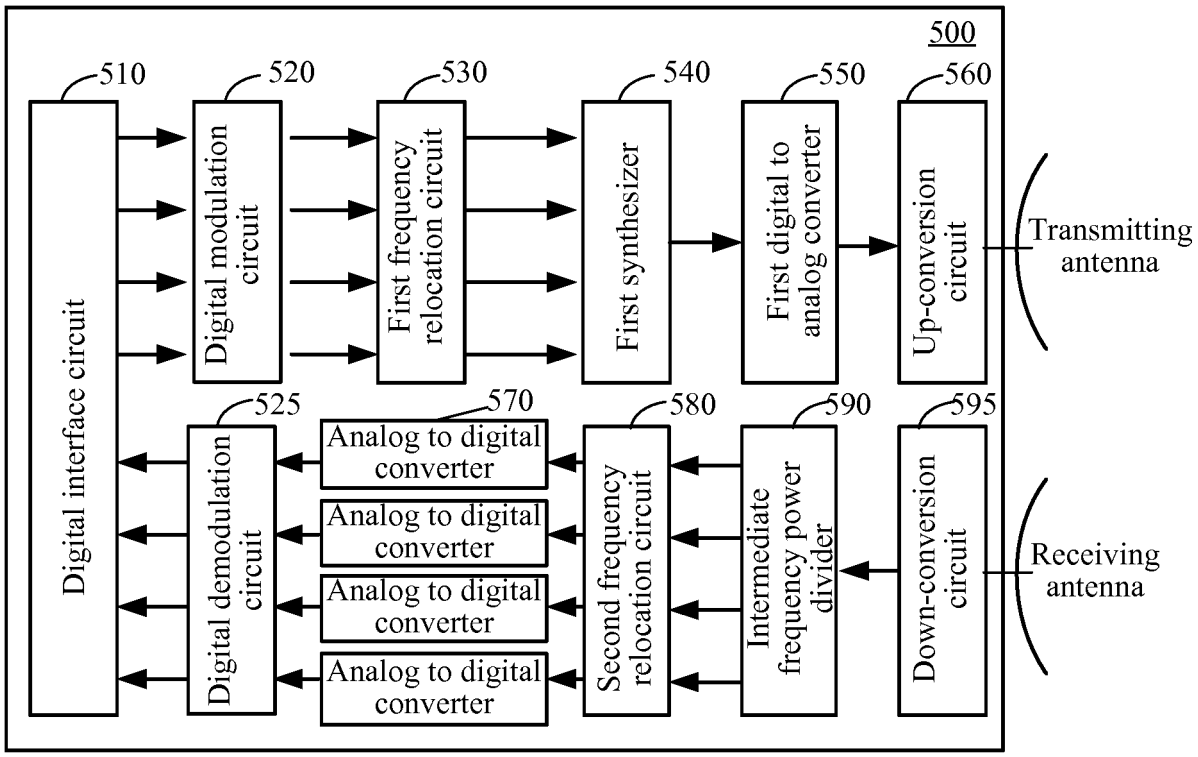
500
510
Digital interface circuit
520
Digital modulation circuit
530
First frequency relocation circuit
540
First synthesizer
550
First digital to analog converter
560
Up-conversion circuit
Transmitting antenna
525
Digital demodulation circuit
570
Analog to digital converter
Analog to digital converter
Analog to digital converter
Analog to digital converter
580
Second frequency relocation circuit
590
Intermediate frequency power divider
595
Down-conversion circuit
Receiving antenna

FIG. 5

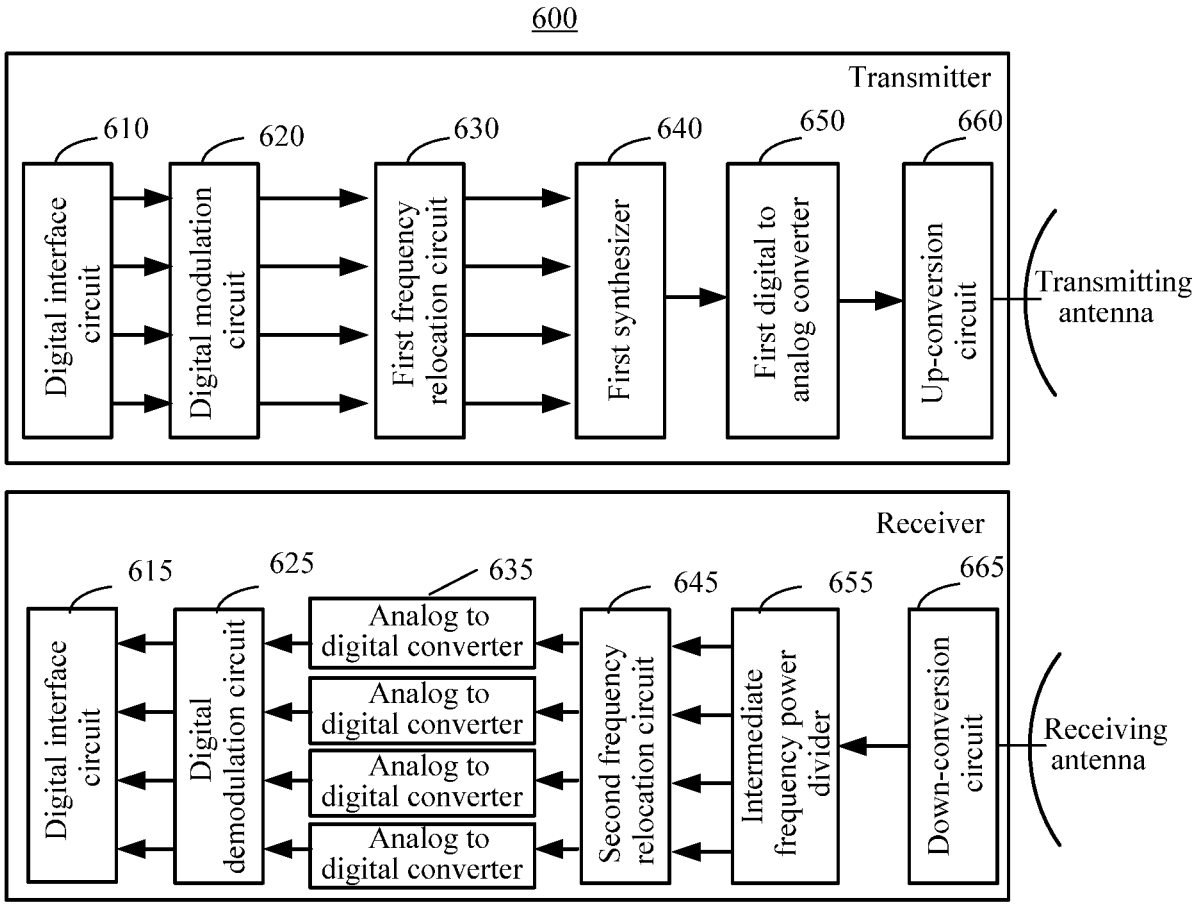
600
Transmitter
610
620
630
640
650
660
Digital interface circuit
Digital modulation circuit
First frequency relocation circuit
First synthesizer
First digital to analog converter
Up-conversion circuit
Transmitting antenna
Receiver
615
625
635
645
655
665
Digital interface circuit
Digital demodulation circuit
Analog to digital converter
Analog to digital converter
Analog to digital converter
Analog to digital converter
Second frequency relocation circuit
Intermediate frequency power divider
Down-conversion circuit
Receiving antenna

FIG. 6

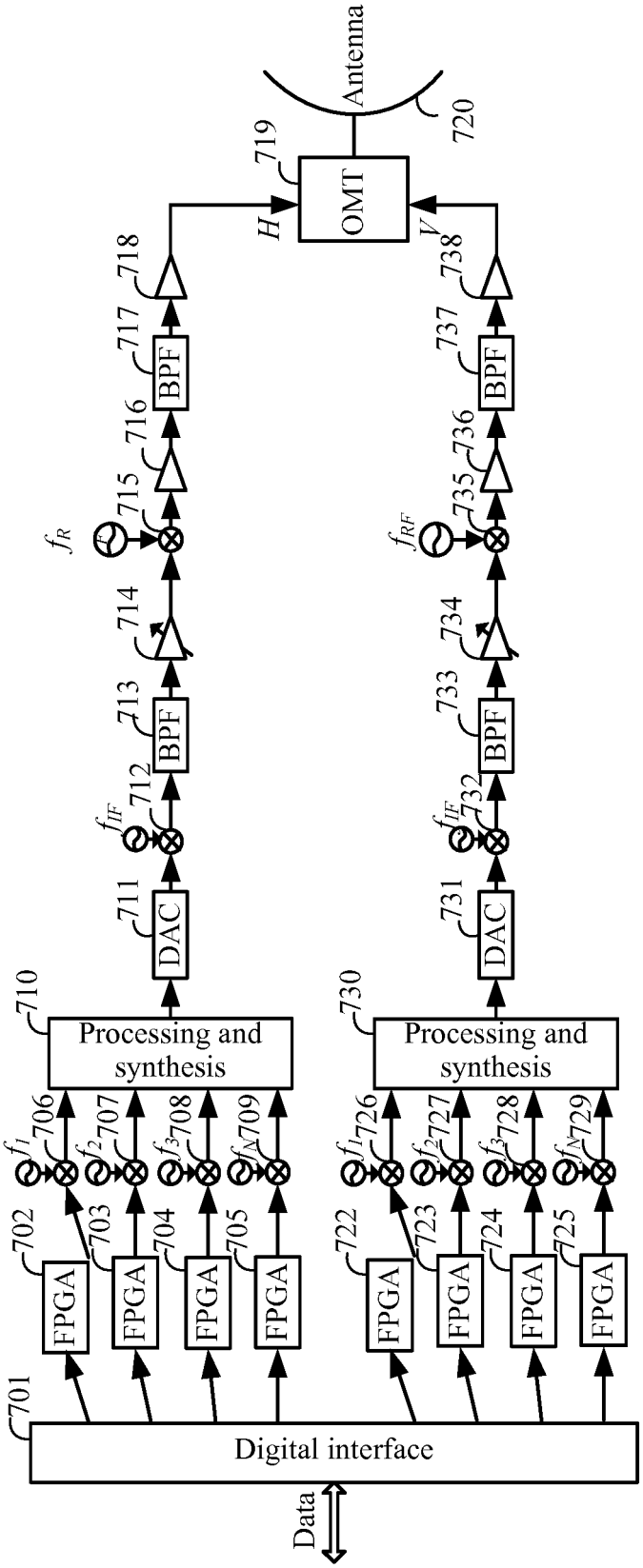
Antenna
720
719
OMT
H
V
718
738
717
737
BPF
716
736
715
735
f_R
f_{RF}
714
734
713
733
BPF
712
732
f_{IF}
711
731
DAC
710
730
Processing and synthesis
706
726
707
727
708
728
709
729
f_1
f_2
f_3
f_N
702
722
703
723
704
724
705
725
FPGA
701
Digital interface
Data

FIG. 7A

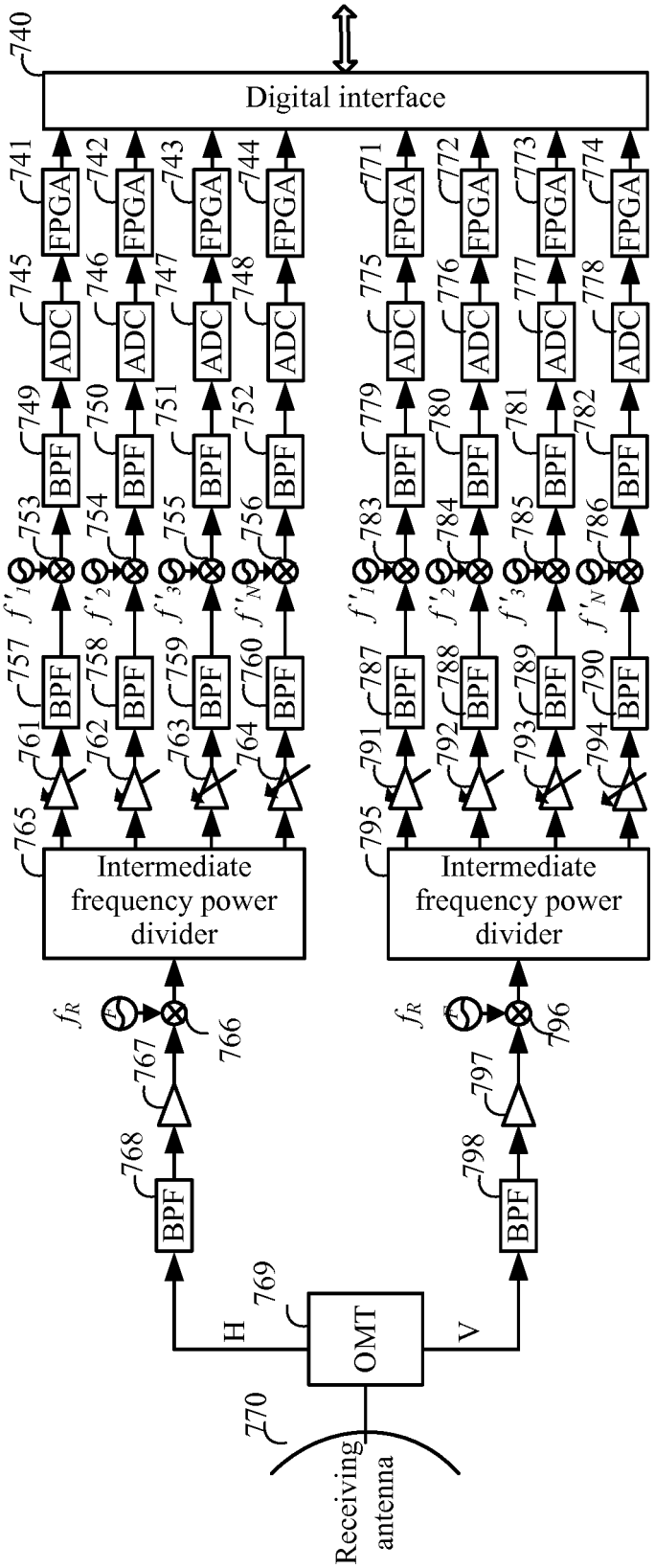
740
Digital interface
741
742
743
744
771
772
773
774
FPGA
745
746
747
748
775
776
777
778
ADC
749
750
751
752
779
780
781
782
BPF
753
754
755
756
783
784
785
786
f'_1
f'_2
f'_3
f'_N
757
758
759
760
787
788
789
790
761
762
763
764
791
792
793
794
765
795
Intermediate frequency power divider
f_R
766
767
768
796
797
798
H
769
OMT
V
770
Receiving antenna

FIG. 7B

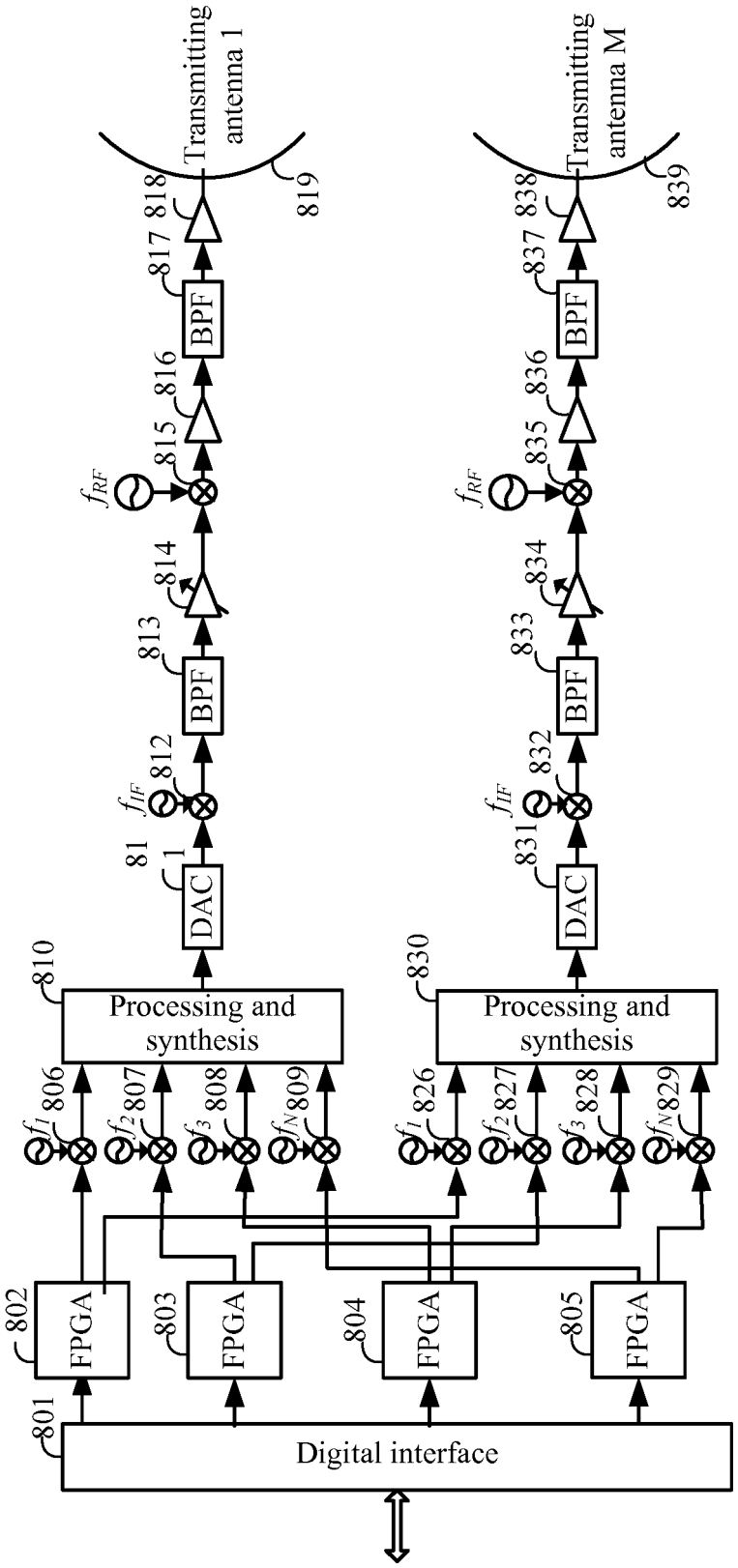
Transmitting antenna 1
819
818
817
BPF
816
815
f_{RF}
814
813
BPF
812
f_{IF}
81 1
DAC
810
Processing and synthesis
806
807
808
809
f_1
f_2
f_3
f_N
802
FPGA
803
FPGA
801
Digital interface
Transmitting antenna M
839
838
837
BPF
836
835
f_{RF}
834
833
BPF
832
f_{IF}
831
DAC
830
Processing and synthesis
826
827
828
829
f_1
f_2
f_3
f_N
804
FPGA
805
FPGA

FIG. 8A

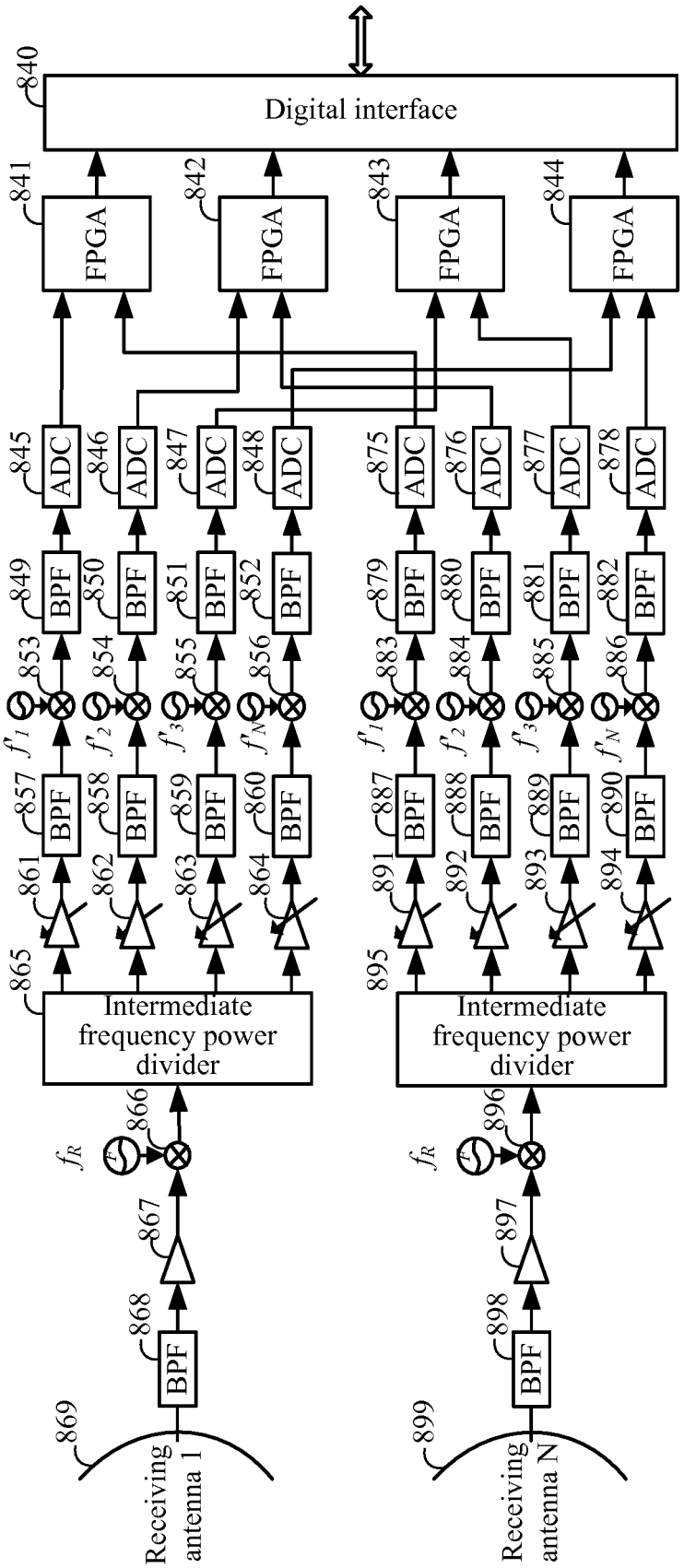
840
Digital interface
841
842
843
844
FPGA
845
846
847
848
875
876
877
878
ADC
849
850
851
852
879
880
881
882
BPF
853
854
855
856
883
884
885
886
f'_1
f'_2
f'_3
f'_N
857
858
859
860
887
888
889
890
861
862
863
864
891
892
893
894
865
895
Intermediate frequency power divider
f_R
866
896
867
897
868
898
869
899
Receiving antenna 1
Receiving antenna N

FIG. 8B

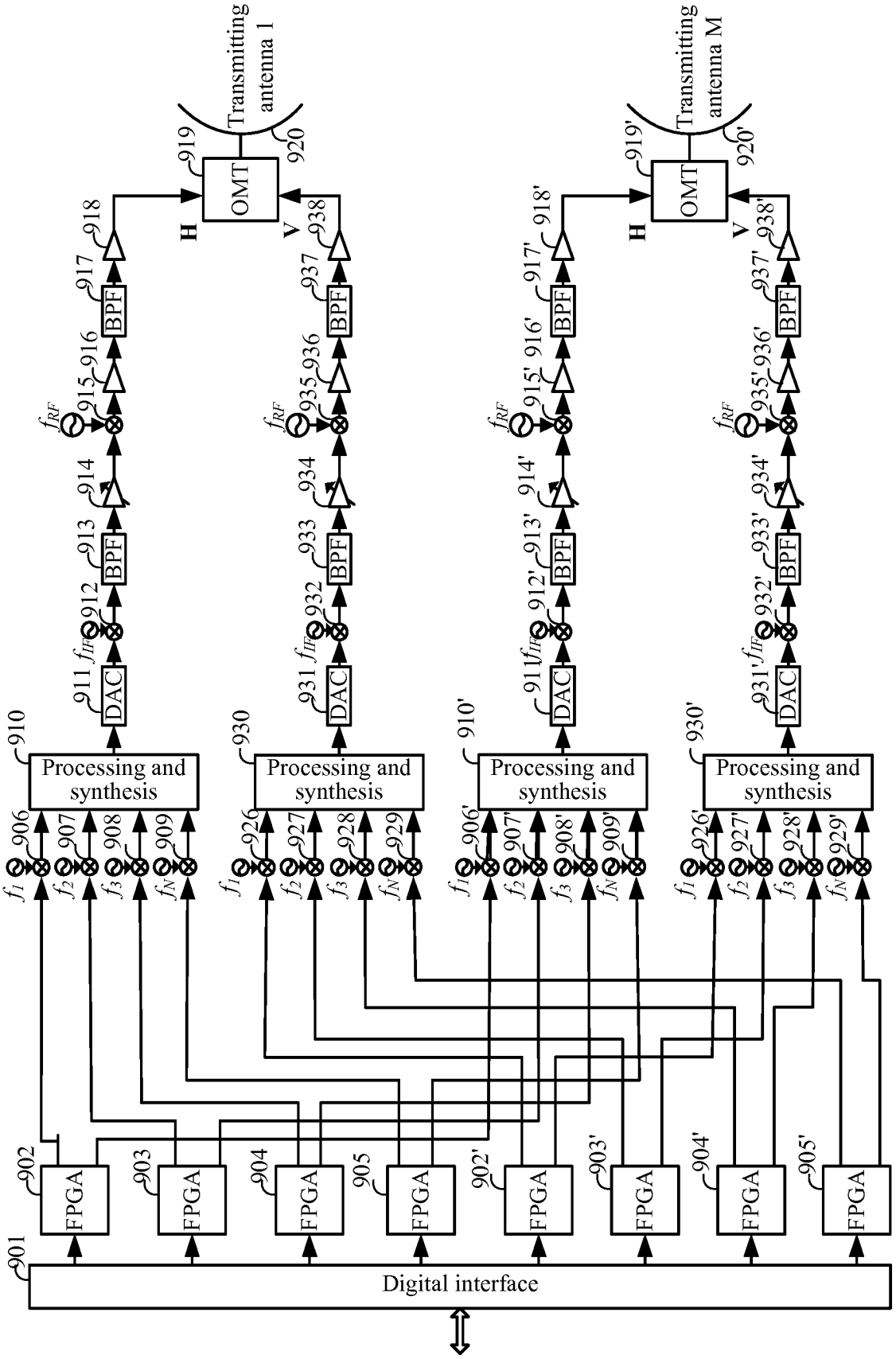
Digital interface
FPGA
Processing and synthesis
DAC
BPF
OMT
H
V
Transmitting antenna 1
Transmitting antenna M
f_{RF}
f_{IF}
f_1
f_2
f_3
f_N

FIG. 9A

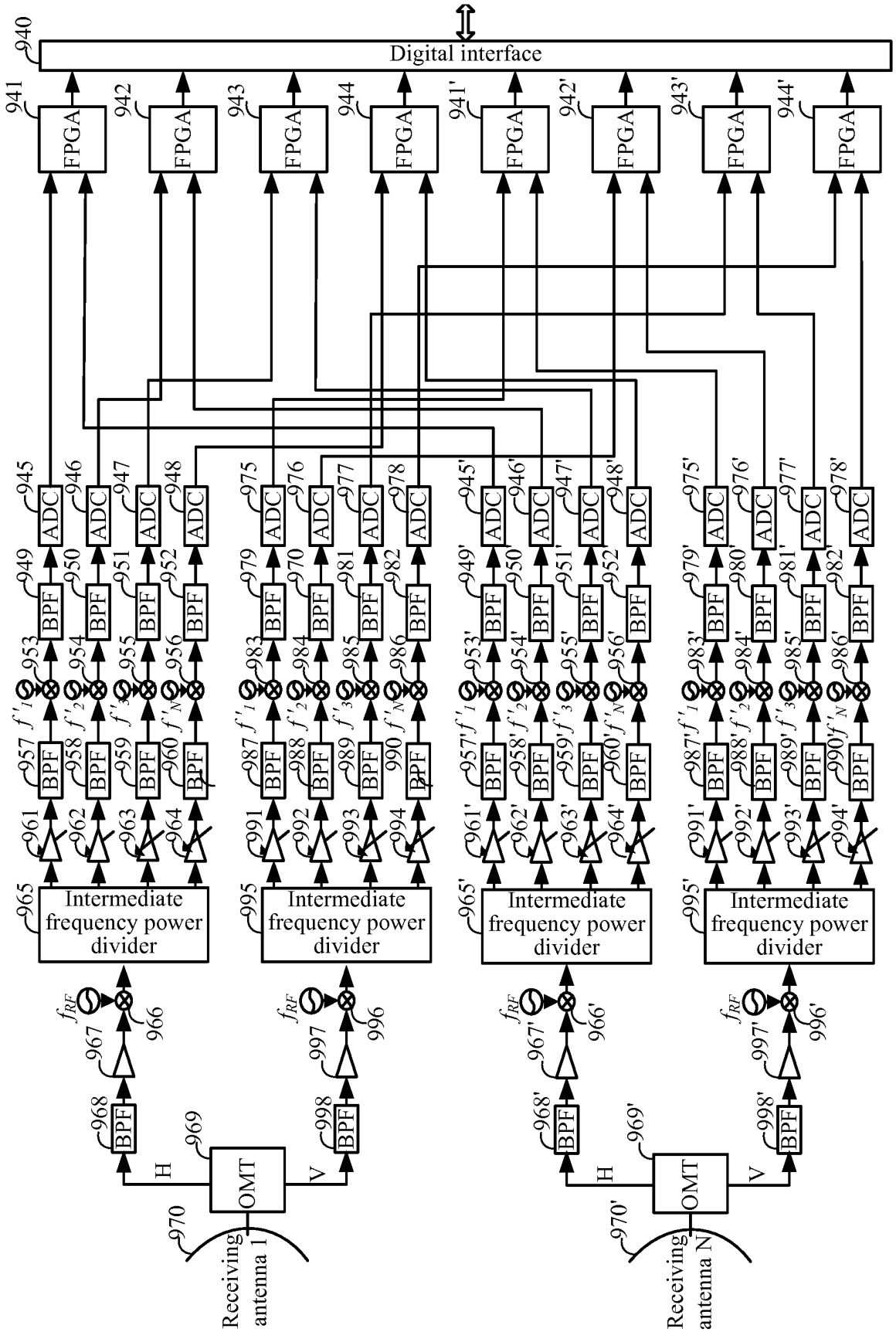
940
Digital interface
941
942
943
944
941'
942'
943'
944'
FPGA
945
946
947
948
975
976
977
978
945'
946'
947'
948'
975'
976'
977'
978'
ADC
949
950
951
952
979
970
981
982
949'
950'
951'
952'
979'
980'
981'
982'
BPF
953
954
955
956
983
984
985
986
953'
954'
955'
956'
983'
984'
985'
986'
957
958
959
960
987
988
989
990
957'
958'
959'
960'
987'
988'
989'
990'
961
962
963
964
991
992
993
994
961'
962'
963'
964'
991'
992'
993'
994'
965
Intermediate frequency power divider
995
965'
995'
f_{RF}
967
966
997
996
967'
966'
997'
996'
968
998
968'
998'
H
V
969
OMT
970
Receiving antenna 1
969'
970'
Receiving antenna N

FIG. 9B

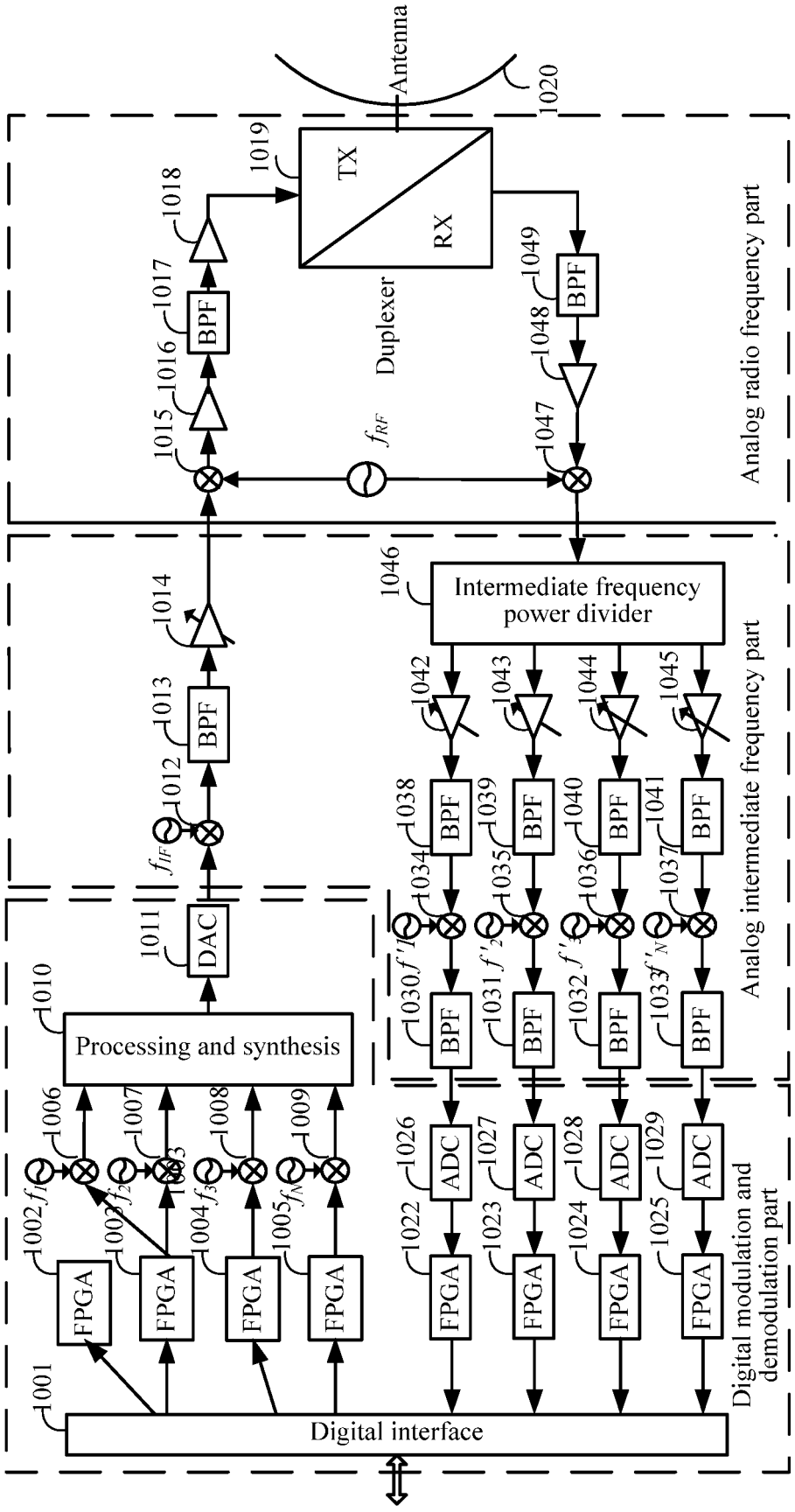
Antenna
1020
1019
TX
RX
Duplexer
1018
1017
BPF
1016
1015
f_{RF}
1049
BPF
1048
1047
Analog radio frequency part
1046
Intermediate frequency power divider
1014
1013
BPF
1012
f_{IF}
1042
1043
1044
1045
1038
1039
1040
1041
BPF
1034
1035
1036
1037
1011
DAC
1010
Processing and synthesis
1030 f'_1
1031 f'_2
1032 f'_3
1033 f'_N
Analog intermediate frequency part
1006
1007
1008
1009
1002 f_1
1003 f_2
1004 f_3
1005 f_N
1026
1027
1028
1029
ADC
1022
1023
1024
1025
FPGA
1001
Digital interface
Digital modulation and demodulation part

FIG. 10

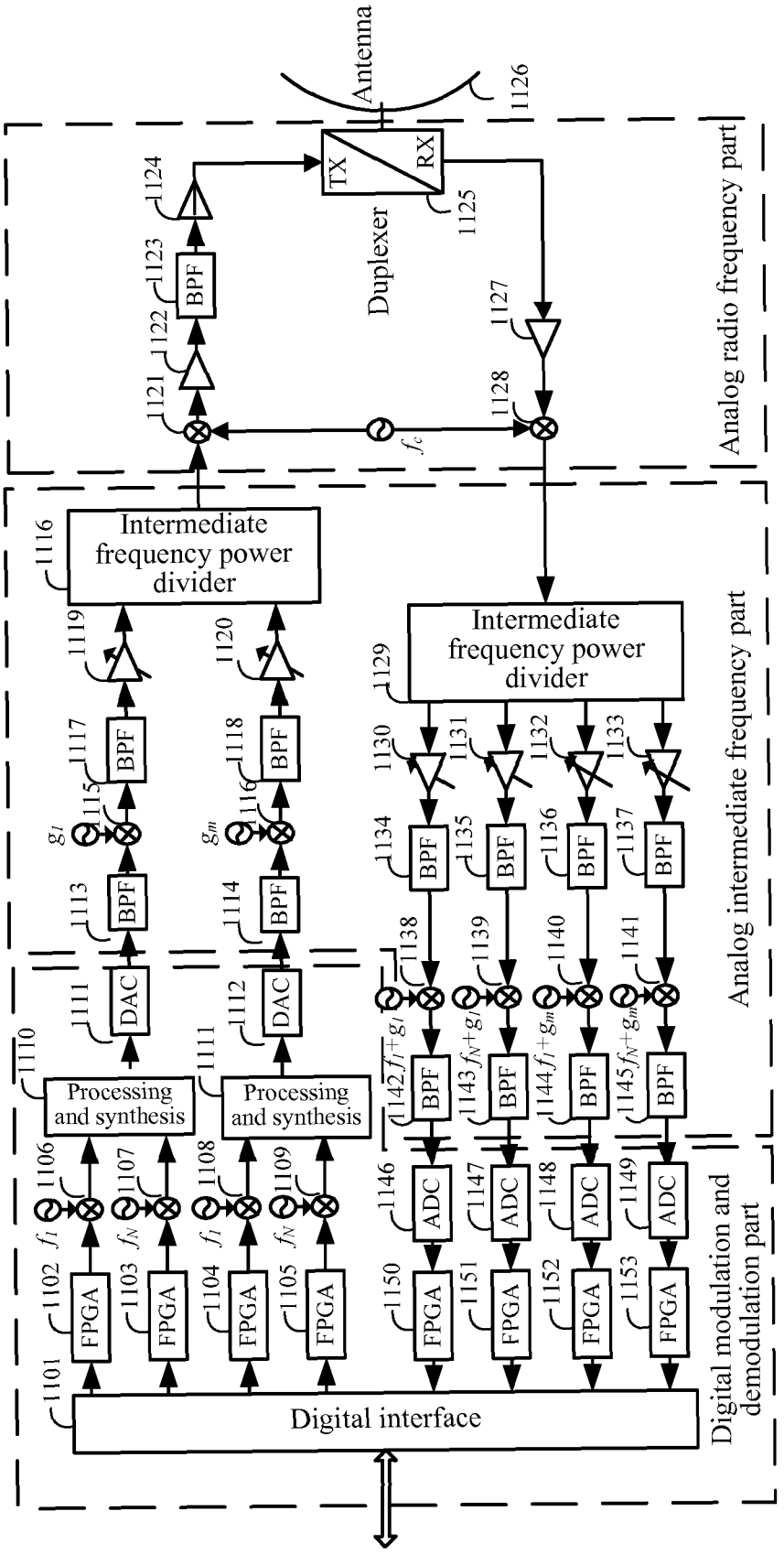
Antenna
1126
TX
RX
Duplexer
1125
1124
1123
BPF
1122
1121
1127
1128
f_c
Analog radio frequency part
1116
Intermediate frequency power divider
1119
1120
1129
Intermediate frequency power divider
1130
1131
1132
1133
1117
1118
1134
1135
1136
1137
g_l
g_m
1115
1116
1113
1114
1138
1139
1140
1141
DAC
1111
1112
f_l+g_l
f_N+g_l
f_l+g_m
f_N+g_m
1142
1143
1144
1145
1110
1111
Processing and synthesis
Processing and synthesis
1106
1107
1108
1109
f_l
f_N
f_l
f_N
1146
1147
1148
1149
ADC
1102
1103
1104
1105
1150
1151
1152
1153
FPGA
1101
Digital interface
Analog intermediate frequency part
Digital modulation and demodulation part

FIG. 11

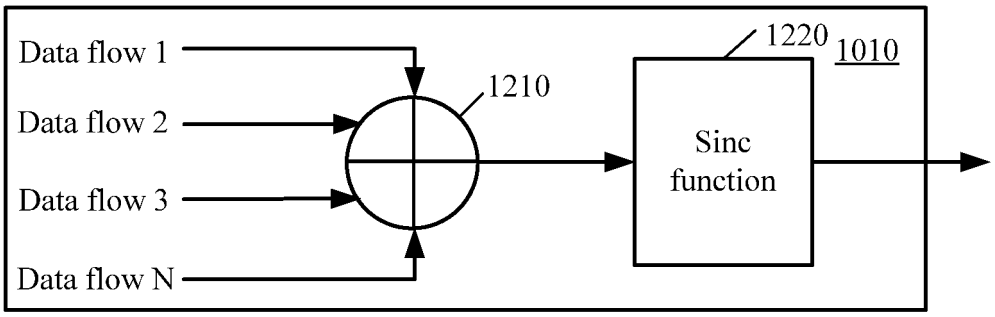
Data flow 1
Data flow 2
Data flow 3
Data flow N
1210
1220
1010
Sinc function

FIG. 12

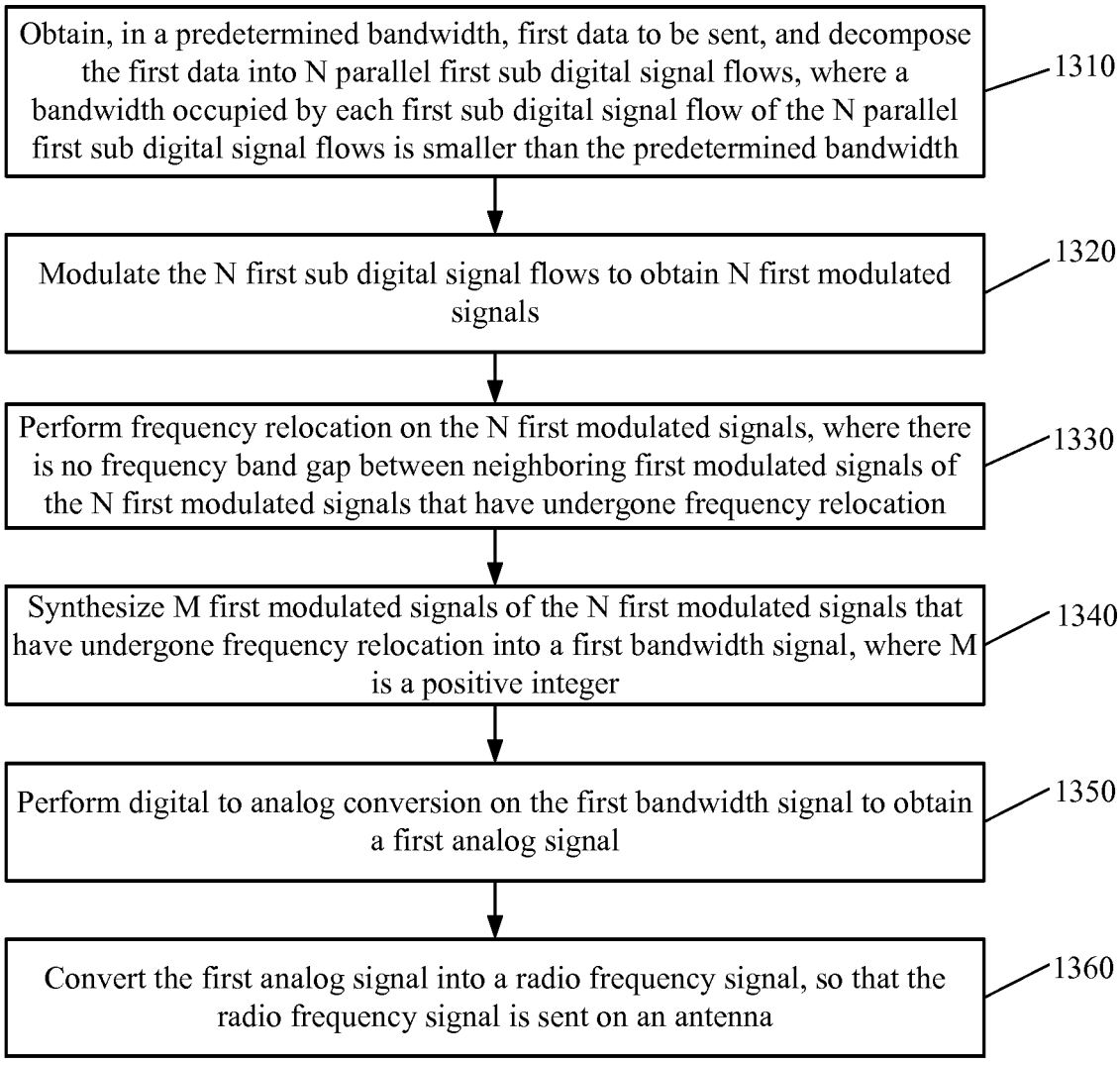
Obtain, in a predetermined bandwidth, first data to be sent, and decompose the first data into N parallel first sub digital signal flows, where a bandwidth occupied by each first sub digital signal flow of the N parallel first sub digital signal flows is smaller than the predetermined bandwidth
1310
Modulate the N first sub digital signal flows to obtain N first modulated signals
1320
Perform frequency relocation on the N first modulated signals, where there is no frequency band gap between neighboring first modulated signals of the N first modulated signals that have undergone frequency relocation
1330
Synthesize M first modulated signals of the N first modulated signals that have undergone frequency relocation into a first bandwidth signal, where M is a positive integer
1340
Perform digital to analog conversion on the first bandwidth signal to obtain a first analog signal
1350
Convert the first analog signal into a radio frequency signal, so that the radio frequency signal is sent on an antenna
1360

FIG. 13

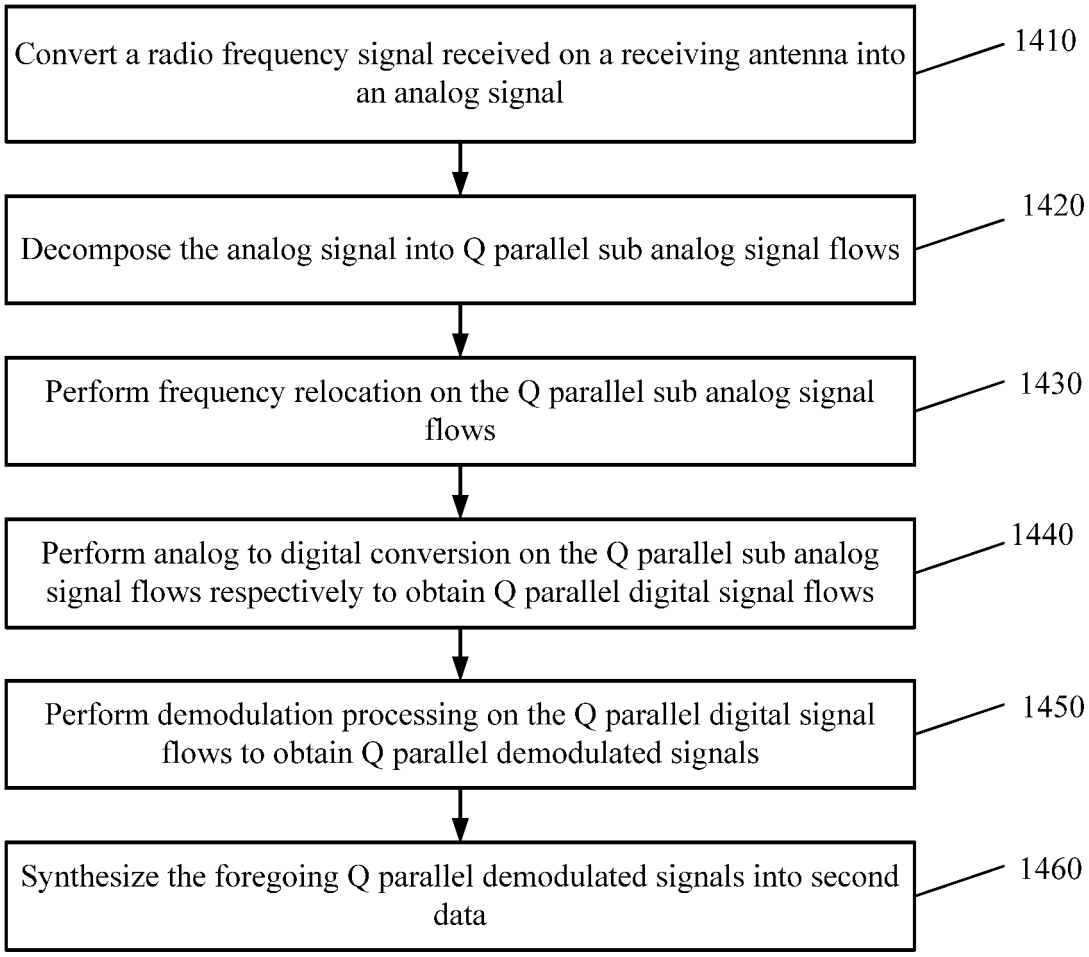
Convert a radio frequency signal received on a receiving antenna into an analog signal
1410
Decompose the analog signal into Q parallel sub analog signal flows
1420
Perform frequency relocation on the Q parallel sub analog signal flows
1430
Perform analog to digital conversion on the Q parallel sub analog signal flows respectively to obtain Q parallel digital signal flows
1440
Perform demodulation processing on the Q parallel digital signal flows to obtain Q parallel demodulated signals
1450
Synthesize the foregoing Q parallel demodulated signals into second data
1460

FIG. 14

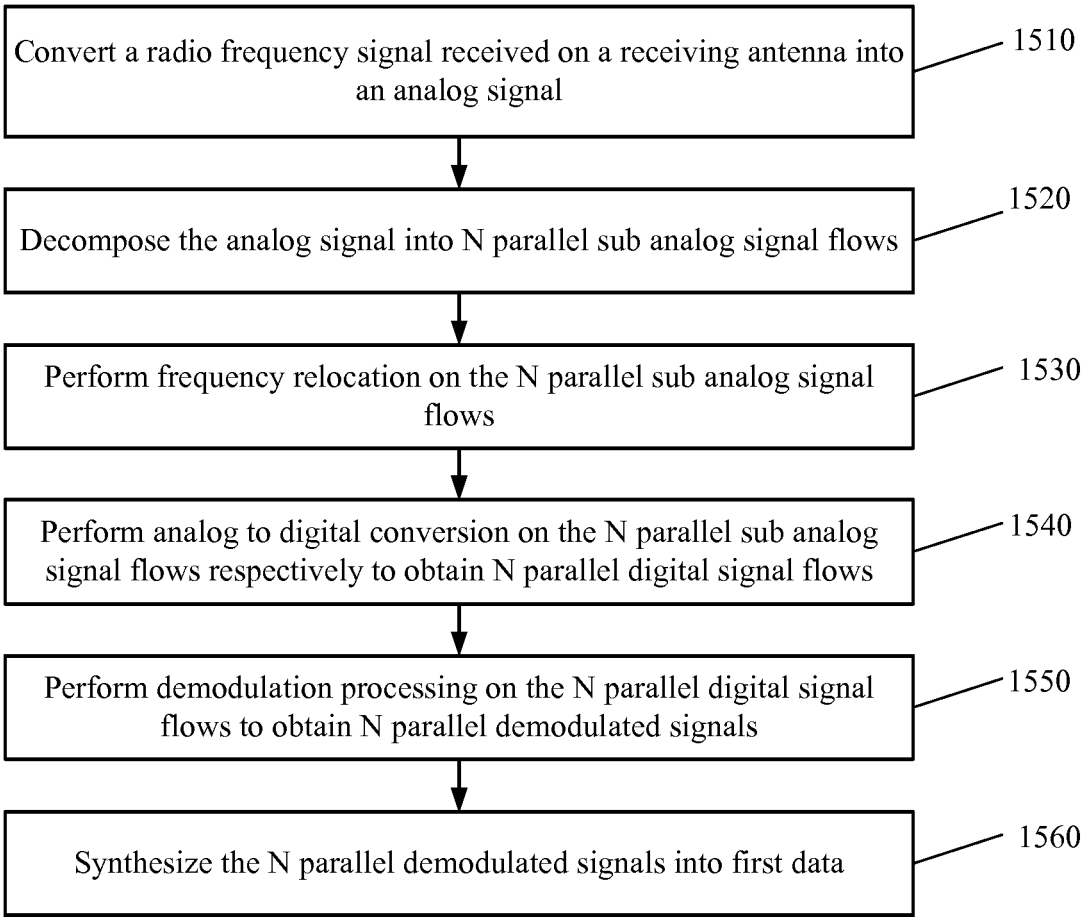
Convert a radio frequency signal received on a receiving antenna into an analog signal
1510
Decompose the analog signal into N parallel sub analog signal flows
1520
Perform frequency relocation on the N parallel sub analog signal flows
1530
Perform analog to digital conversion on the N parallel sub analog signal flows respectively to obtain N parallel digital signal flows
1540
Perform demodulation processing on the N parallel digital signal flows to obtain N parallel demodulated signals
1550
Synthesize the N parallel demodulated signals into first data
1560

FIG. 15

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2011122972 A1 **[0005]**
- WO 2006103585 A2 **[0006]**
- CN 102130697 A **[0007]**
- CN 101924729 A **[0008]**
- CN 102148789 A **[0009]**