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(54) **Clocked pulse frequency modulation buck DC-to-DC converter**

Gleichstromabwärtswandler mit Taktimpulsfrequenzmodulation

Convertisseur-abaisseur CC-CC à modulation en fréquence d'impulsions

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(56) References cited:
US-A1- 2005 111 149 **US-A1- 2009 040 791**

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Description

Technical Field

[0001] This disclosure relates generally to circuits and methods for controlling operation of switching power converters. More particularly, the present disclosure relates to circuits and methods for controlling operation of a pulse frequency modulated buck DC-to-DC converter to decrease noise coupling and permit a variable current to accommodate large output currents.

Background Art

[0002] As is known in the art, a buck DC-to-DC converter is a voltage step down and current step up converter. A buck DC-to-DC converter has a power switching section and a low pass filter section. The power switching section reduces the DC component of the power supply voltage source and the filter section removes the high frequency harmonics created by the power switching section to generate the desired DC output voltage level.

[0003] The power switching section has a first switch with a first terminal connected to one terminal of a power supply voltage source. The power supply voltage source may be a battery or the rectified AC power mains. The second terminal of the first switch is connected to a filter section of the buck DC-to-DC converter. A second switch in the power switching section has a first terminal connected to a ground reference voltage terminal. The second terminal of the second switch is connected to the second terminal of the first switch and the filter section of the buck DC-to-DC converter. The first and second switches each have a control terminal that is connected to control circuitry that determines the switching frequency and duration of the activations of the first and second switches based on a feedback signal from an output of the buck DC-to-DC converter.

[0004] The input of the filter section is a first terminal of an inductor and the second terminal of the inductor is connected to a first terminal of a filter capacitor. The second terminal of the filter capacitor is connected to the ground reference voltage terminal. The output of the buck DC-to-DC converter is the common connection of the second terminal of the inductor and the first terminal of the filter capacitor. A sense circuit is commonly applied to the output terminal of the buck DC-to-DC converter to provide the feedback signal for the control circuitry.

[0005] The buck DC-to-DC converter operates in a continuous, synchronous, or pulse width modulated mode for higher current or heavily loaded operation. The first and second switches are activated and deactivated at a fixed frequency and the period between each activation and deactivation is determined by comparing the feedback signal with a desired reference signal to create the desired output voltage. When the buck DC-to-DC converter operates in a discontinuous, asynchronous or pulse frequency modulated mode for low current or lightly loaded operation, the switches do not supply the current from the power supply voltage source on each cycle and the current then supplied during the commutation mode where current is provided from the collapsing field of the inductor. Often the discontinuous mode is used in portable electronics such as smart cellular telephones, tablet computers, digital readers, etc. as a "sleep mode". The only current required by the system in these applications is monitoring current for system maintenance (i.e. system clocking and timers, cellular network monitoring, wireless network monitoring).

[0006] In the pulse frequency modulation mode, the buck DC-to-DC converter turns on the first switch to apply the power supply voltage source to the inductor when the output voltage falls below a reference voltage. The first switch is then turned off when the current in the coil reaches a threshold value (sleep current limit). The second switch is turned on when the first switch is turned off. The second switch is then turned off when the current in the coil is fully discharged. The pulse frequency modulation mode is not typically used for large currents as the current limit is normally set low to maximize efficiency.

[0007] Buck DC-to-DC converter converters operate in the pulse frequency modulation mode have serious problems with noise coupling when operating a high current levels. Further, when the second switch is open, there is no path from the filter section for negative currents resulting from overvoltage situations at the output of the buck DC-to-DC converter.

[0008] U. S. Patent Application Publication 2009/0040791 (Qahouq et al.) provides a switching mode power converter that includes a modulation circuit to dynamically control a variable switching frequency of the power converter based on an error voltage of the power converter. The power converter further include a control circuit connected to the modulation circuit and is arranged to dynamically limit an inductor current in the power converter while the switching frequency of the power converter changes. A variable limit on the inductor current may be based on the error voltage of the power converter, a load current of the power converter, or information from a power manager of a system in which the power converter resides. In some implementations, the power converter includes a disabling circuit to control the modulation circuit to disable the variable switching frequency when a sufficiently large load transient is detected.

[0009] U. S. Patent Application Publication 2005/0111149 (Motomori) describes a switching regulator that comprises a main switch, a rectifier switch, an RS-flipflop, a judging unit, an edge pulse generator, a second prohibiting unit, a reference voltage source. When a voltage drop caused due to an on-resistance of the main switch exceeds a predetermined value, the judging unit sets a set signal of the RS-flipflop at a high level to cut off an overcurrent. The edge pulse generator monitors a gate voltage of the rectifier switch, and sets a prohibition signal at a high level for a predetermined time period from the trailing edge. Then, the second pro-

hibiting unit sets the set signal at a low level for prohibiting cutting off the overcurrent for reducing the likelihood that the main switch will be destroyed by the overcurrent.

Summary of the invention

[0010] An object of this disclosure is to provide circuits and methods for operating a buck DC-to-DC converter in a pulse frequency mode with variable current limits to provide the ability to manage large output currents.

[0011] Another object of this disclosure is to provide circuits and methods for operating a buck DC-to-DC converter in hysteretic mode where switching of the power supply voltage source is governed by output current and voltage thresholds.

[0012] To accomplish at least one of these objects, a hysteretic mode control circuit within a DC-to-DC converter. The hysteretic mode control circuit is configured for varying the current limit that controls the switching interval and duration of a power switching section of the DC-to-DC converter to permit the DC-to-DC converter to manage large changes in its output current load.

[0013] The hysteretic mode control circuit has a positive current limit circuit and a negative current limit circuit. The positive current limit circuit is configured for determining a first reference voltage that is used for controlling activation a first switching device of a switching section of the DC-to-DC converter for transferring current to a load device placed at the output of the DC-to-DC converter. In some embodiments, the positive current limit circuit has a first matching switching device having geometry and impurity implantations matching the first switching device. The matching switching device is connected to a first reference current source configured to develop a first reference limit signal for turning on and turning off the first switching device. The first reference limit signal is compared to an output voltage of the power switching section to determine if the first switching device is to be turned on or turned off.

[0014] In some embodiments, the negative current limit circuit is configured for determining a second reference voltage that is used for controlling activation a second switching device of a switching section of the DC-to-DC converter for accepting current from the DC-to-DC converter. In some embodiments, the negative current limit circuit has a second matching switching device having geometry and impurity implantations matching the first switching device. The matching switching device is connected to a second reference current source configured to develop a second reference limit signal for turning on and turning off the second switching device. The second reference limit signal is compared to the output voltage of the power switching section to determine if the second switching device is to be turned on or turned off.

[0015] In other embodiments, the positive current section has a dynamic current limit circuit that has a first reference current source providing a maximum reference current to a reference leg of a first current mirror. A mirror leg of the first current mirror is connected to provide a reference limit voltage for an output of the positive current section to determine the switching interval and duration of the first switching device of the power switching section to provide current to the filter section of the DC-to-DC converter. A feedback signal from the output of the DC-to-DC converter and a first reference voltage are inputs to a comparator for determining if the feedback signal is greater than or less than the first reference voltage. An output of the comparator is an input to a switching device that is activated or deactivated to divert current from the reference leg of the current mirror and thus modify the current in mirror leg of the current mirror and thus adjust the voltage level of the reference limit voltage.

[0016] A load device is connected to the mirror leg of the current mirror for developing the reference limit voltage. In various embodiments, the dynamic current limit circuit has a second current source connected in parallel with the mirror leg of the current mirror to provide an optional minimum reference current.

[0017] In various embodiments, hysteretic mode control circuit has a variable current limit circuit. A driver control circuit receives a first control signal developed by a comparison of a feedback signal from the output of the DC-to-DC converter with a reference voltage and a second control signal developed by the variable current limit circuit for controlling activation the first switching device of a switching section of the DC-to-DC converter for transferring current to a load device placed at the output of the DC-to-DC converter.

[0018] The variable current limit circuit is configured for determining the second control signal by sensing a voltage level present at the input to the low pass filter of the DC-to-DC converter. The voltage level sensing signal is applied to a first terminal of a adjustable differential current source. A control terminal of the differential current source is controlled by the comparison of the feedback signal from the output of the DC-to-DC converter with the reference voltage. The second control signal developed across the adjustable differential current source is applied to the driver control circuit to permit activation of the first and second switching devices according to the level of the necessary voltage across or current through the low pass filter.

[0019] In various embodiments, a compensation current source is connected in parallel with the differential current source. The compensation current source provides a fixed ramp current that is summed with the differential current source for providing compensation to prevent sub-harmonic oscillation.

[0020] In various embodiments that accomplish at least one of these objects, a DC-to-DC converter includes a hysteretic mode control circuit configured for varying the current limit that controls the switching interval and duration of a power switching section of the DC-to-DC converter to permit the DC-to-DC converter to manage large changes in output current load of the DC-to-DC converter.

[0021] In various embodiments that accomplish at least one of these objects, a method for providing hysteretic mode control within a DC-to-DC converter. The method provides the mode control through a hysteretic mode control circuit that varies the current limit that controls the switching interval and duration of a power switching section of the DC-to-DC converter to permit the DC-to-DC converter to manage large changes in output current load of the DC-to-DC converter.

[0022] The method begins by determining a limit signal proportional to a positive limit current and a negative limit current for the current flowing in the low pass filter of the DC-to-DC converter. In various embodiments, the limit signal is a voltage that is compared to a voltage that is developed at the input of the low pass filter of the DC-to-DC converter. If a positive voltage that is developed at the input of the low pass filter of the DC-to-DC converter is greater than a positive limit signal voltage, a first latching circuit is reset and a positive switching device is disabled to prevent current from flowing into the low pass filter. Alternately, if the positive voltage that is developed at the input of the low pass filter of the DC-to-DC converter is less than the positive limit signal voltage, the first latching circuit is not reset and the positive switching device is enabled to allow current to flow into the low pass filter.

[0023] If a negative voltage that is developed at the input of the low pass filter of the DC-to-DC converter is greater than a negative limit signal voltage, a second latching circuit is reset and a negative switching device is disabled to prevent current from flowing from the low pass filter. Alternately, if the negative voltage that is developed at the input of the low pass filter of the DC-to-DC converter is less than the negative limit signal voltage, second first latching circuit is not reset and the negative switching device is enabled to allow current to flow from the low pass filter.

[0024] In some embodiments, first setting a maximum reference current and a minimum reference current develop the positive and negative limit signals. A difference between a reference voltage of the DC-to-DC converter and a feedback voltage of the DC-to-DC converter is determined as difference voltage. The difference voltage is converted to a difference current. The difference current is subtracted from the maximum reference current to form a variable limit current. A positive variable limit current is mirrored and converted to the positive limit signal and a negative variable limit current is mirrored and converted to the negative limit signal.

Description of the Drawings

[0025]

Fig. 1 is a schematic of a DC-to-DC converter operating with a pulse width modulation mode and pulse frequency modulation mode.

Fig. 2 is a schematic of DC-to-DC converter operating with a pulse width modulation mode and pulse frequency modulation mode embodying the principals of the present disclosure.

Fig. 3 is a schematic of a positive and negative current limit circuit incorporated within a DC-to-DC converter embodying the principals of the present disclosure.

Fig. 4 is a schematic of an embodiment of a positive dynamic current limit circuit and a negative dynamic current limit circuit incorporated within a DC-to-DC converter of Fig. 2.

Fig. 5 is a schematic of a DC-to-DC converter with a dynamic sleep mode embodying the principals of the present disclosure.

Fig. 6 is a plot of the waveforms of the signals the DC-to-DC converter of Fig. 5 with a dynamic sleep mode with a continuous loading.

Fig. 7 is a plot of the waveforms of the signals the DC-to-DC converter of Fig. 5 in dynamic sleep mode operation illustrating a change in load current.

Figs. 8 and 9 are flowcharts of a method for providing hysteretic mode control within a DC-to-DC converter embodying the principals of the present disclosure.

Description of the preferred embodiments

[0026] Fig. 1 is a schematic of a DC-to-DC converter operating with a pulse width modulation mode and pulse frequency modulation mode. The power switching section **120** has a switching control circuit **125** that generates control signals that are applied to a positive input of a driver circuit **130a** and a negative input of a driver circuit **130b**. The output of the driver circuit **130a** is applied to the gate of the PMOS transistor **MP1** and the output of the driver circuit **130b** is applied to the gate of the NMOS transistor **MN1**. The source of the PMOS transistor **MP1** is connected to the power supply voltage source **VDD** and the source of the NMOS transistor **MN1** is connected to the substrate supply voltage source **VSS**. The substrate supply voltage source **VSS** is often the ground reference voltage source, but in some applications is a negative voltage level. The commonly connected drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** are connected to an input terminal of the filter section **135**. The input terminal is a first terminal of an inductor **L1**. The control circuit **125** determines that during the continuous mode or pulse width modulation mode the control signals **116** and **118** are applied to the driver circuit **130a** and the driver circuit **130b** such that the PMOS transistor **MP1** is turned on and the NMOS transistor **MN1** is turned off, a current from the power supply voltage source **VDD** from the first terminal of the inductor **L1** out

the second terminal of the inductor **L1** into the first terminal of the output capacitor C_{OUT} and to the substrate supply voltage source **VSS**. The output voltage V_{OUT} is present at the junction of the second terminal of the inductor **L1** and the output capacitor C_{OUT}.

[0027] It is known in the art, that the voltage (V_{L1}) across the inductor **L1** is determined by the formula:

$$V_{L1} = L \frac{di_L}{dt}$$

The output voltage V_{OUT} is equal to the difference of the power supply voltage source **VDD** and the voltage V_{L1} across the inductor **L1** in the on state and equal to the negative of the voltage $-V_{L1}$ across the inductor **L1** in the off state. The duty cycle of the buck DC-to-DC converter determines the on state time and the off state time. It can be shown that the output voltage V_{OUT} is equal to the duty cycle of the buck DC-to-DC converter multiplied by the voltage level of the power supply voltage source VDD.

[0028] The feedback stage **140** has three inputs. The first input **107** is the feedback voltage V_{FB} that is developed from the output voltage V_{OUT} at common connection of the second terminal of the inductor **L1** and the first terminal of the output capacitor C_{OUT}. The second and third inputs are the first and second reference voltages V_{REF1} and V_{REF2} generated by the switch control circuit **105**. The switch control circuit **105** has a digital-to-analog converter **110** that receives a reference control word **112** and an offset control word **114**. The digital-to-analog converter **110** converts the reference control word **112** to the first reference voltage V_{REF1} and the offset control word **114** to the second reference voltage V_{REF2}. The first reference voltage V_{REF1} and the second reference voltage V_{REF2} are the second and third inputs to the feedback stage **115**. The feedback control stage **115** has a first comparator **117** for providing a first control signal **116** and a second comparator **119** for providing a second control signal **118**. The first control signal **116** is applied to a data input **D** of a first data flip-flop **127** of the switching control circuit **125**. The second control signal **118** is applied to a data input **D** of a second data flip-flop **129** of the switching control circuit **125**. An oscillator **150** generates the clock pulse signal **152** that is applied to the clock **CK** input of the first data flip-flop **127** and the second data flip-flop **129**. The output of the first data flip-flop **127** is applied to the input of the positive driver circuit **130a** and the output of the second data flip-flop **129** is applied to the input of the negative driver circuit **130b**. The output of the first driver circuit **130a** is applied to the gate of the PMOS transistor **MP1** and the output of the second driver circuit **130b** is applied to the gate of the NMOS transistor **MN1**.

[0029] A current/voltage sense circuit **140** is placed at the junction of the second terminal of the inductor **L1** and the output capacitor C_{OUT}. The current/voltage sense circuit **140** determines the feedback voltage V_{FB} and the feedback current I_{FB}. The feedback voltage V_{FB} is fed back as the first input to the first comparator **117** and the second comparator **118**. The feedback current I_{FB} is fed back to a pulse width modulation/pulse frequency modulation control circuit **145**. Based on the feedback current I_{FB} as determined by the load current I_{OUT}, the pulse width modulation/pulse frequency modulation control circuit **145** resets the first data flip-flop **127** and the second data flip-flop **129**. If the DC-to-DC converter is operating in the pulse width modulation mode, the first data flip-flop **127** and the second data flip-flop **129** are not reset and the data outputs of the first data flip-flop **127** and the second data flip-flop **129** are controlled by the feedback voltage V_{FB} to determine the pulse width of the control signals driving the first driver circuit **130a** and the second driver circuit **130b** and thus the PMOS transistor **MP1** and the NMOS transistor **MN1.**

[0030] When the load current I_{OUT} decreases to a predetermined level, the DC-to-DC converter is set to the pulse frequency modulation mode. The feedback current I_{FB} is interpreted by the pulse width modulation/pulse frequency modulation control circuit **145** such that the second data flip-flop **129** is reset. This turns off the NMOS transistor **MN1.** The pulse width modulation/pulse frequency modulation control circuit **145** resets the first data flip-flop **127** and the PMOS transistor **MP1** is turned off. If the output voltage V_{OUT} decreases below a threshold, the output current I_{OUT} is increasing and the pulse width modulation/pulse frequency modulation control circuit **145** releases the reset of the first data flip-flop **127** to activate the PMOS transistor **MP1** to allow current to flow into the filter section **135**.

[0031] Since the NMOS transistor **MN1** is turned off, the DC-to-DC converter can not accept current from the load, therefore any overvoltage of the output voltage V_{OUT} is not discharged. Further, the PMOS transistor **MP1** is turned on asynchronously at high load creating serious implications for noise being coupled to the system that is load being powered.

[0032] Fig. 2 is a schematic of a DC-to-DC converter operating with pulse width modulation mode and pulse frequency modulation mode embodying the principals of the present disclosure. A switch control circuit **205** has a digital-to-analog converter **210** that receives a reference control word **212** and an offset control word **214**. The digital-to-analog converter **210** converts the reference control word **112** to the first reference voltage V_{REF1} and converts the offset control word **114** to the second reference voltage V_{REF2}. The first reference voltage V_{REF1} and the second reference voltage V_{REF2} are two of the three inputs to the feedback stage **215**. The feedback stage **215** has a first comparator **217** that receives the first reference voltage V_{REF1} and a second comparator **219** that receives the second reference voltage V_{REF2}. The third **207** of the three inputs to the feedback stage **215** receives the feedback voltage V_{FB} that is compared to the first reference voltage V_{REF1} and the second

reference voltage V_{REF2}. As described previously, the feedback voltage V_{FB} that is developed from the output voltage V_{OUT} at common connection of the second terminal of the inductor **L1** and the first terminal of the output capacitor C_{OUT} of the filter section **235**.

[0033] The outputs **216** and **218** of the first comparator **217** and a second comparator **219** are the inputs to the switching control circuit **225**. The first comparator **217** provides the first control signal **216** is applied to a data input **D** of a first data flip-flop **227** of the switching control circuit **225.** The second comparator **219** provides the second control signal **218** that is applied to a data input **D** of a second data flip-flop **229** of the switching control circuit **225**. An oscillator **250** generates the clock pulse signal **252** that is applied to the clock **CK** input of the first data flip-flop **227** and the second data flip-flop **229**. The output of the first data flip-flop **227** is applied to the input of the positive driver circuit **230a** and the output of the second data flip-flop **229** is applied to the input of the negative driver circuit **230b**. The output of the first driver circuit **230a** is applied to the gate of the PMOS transistor **MP1** and the output of the second driver circuit **230b** is applied to the gate of the NMOS transistor **MN1**.

[0034] The source of the PMOS transistor **MP1** is connected to the power supply voltage source **VDD** and the source of the NMOS transistor **MN1** is connected to the substrate supply voltage source **VSS.** The substrate supply voltage source **VSS** is often the ground reference voltage source, but in some applications is a negative voltage level. The commonly connected drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** are connected to an input terminal of the filter section **235**. The input terminal is a first terminal of an inductor **L1**. The control signals **216** and **218** are applied to the driver circuit **230a** and the driver circuit **230b** such that the PMOS transistor **MP1** is turned on and the NMOS transistor **MN1** is turned off, a current from the power supply voltage source **VDD** from the first terminal of the inductor **L1** out the second terminal of the inductor **L1** into the first terminal of the output capacitor C_{OUT} and to the substrate supply voltage source **VSS.** The output voltage V_{OUT} is present at the junction of the second terminal of the inductor **L1** and the output capacitor C_{OUT}.

[0035] A first current limit circuit is designated as a positive current limit circuit **240a** that is connected in proximity with the PMOS transistor **MP1** and second current limit circuit is designated as the negative current limit circuit **240b** is connected in proximity with the NMOS transistor **MN1**. The positive current limit circuit **240a** and the negative current limit circuit **240b** are connected between the power supply voltage source **VDD** and the substrate supply voltage source **VSS**. The output of the driver circuit **230a** is connected to the positive current limit circuit **240a** and the driver circuit **230b** is connected to the negative current limit circuit **240b**. The output of the positive current limit circuit **240a** is a first reference limit signal designated as a positive reference limit voltage **242** and the output of the negative current limit circuit **240b** is a second reference limit signal designated as a negative reference limit voltage **244**. The positive reference limit voltage **242** and the negative reference limit voltage **244** are the inputs to the pulse width modulation/pulse frequency modulation control circuit **245.** The pulse width modulation/pulse frequency modulation control circuit **245** compares the positive reference limit voltage **242** with the voltage V_{LX} developed at the first terminal of an inductor **L1** for selectively resetting of the first data flip-flop **227** to control operation of PMOS transistor **MP1**. The pulse width modulation/pulse frequency modulation control circuit **245** compares the negative reference limit voltage **244** with the voltage V_{LX} developed at the first terminal of an inductor **L1** for selectively resetting of the second data flip-flop **229** to control operation of the NMOS transistor **MN1**.

[0036] Fig. 3 is a schematic of the positive current limit circuit **240a** and the negative current limit circuit **240b** incorporated within a DC-to-DC converter embodying the principals of the present disclosure. The positive current limit circuit **240a** has a PMOS transistor **MP2** that is a dummy transistor having characteristic that are matched to the geometry and impurity implantations of the PMOS transistor **MP1**. The PMOS transistor **MP2** is used to generate the reference voltage V_{LIM+} for the current limit of the current passing through the PMOS transistor **MP1** across the positive reference current source I_1. The PMOS transistor **MP2** has a gate connected to the output of the positive driver circuit **230a.** The source of the PMOS transistor **MP2** is connected to the power supply voltage source **VDD** and the drain of the PMOS transistor **MP2** is connected to a first terminal of the positive reference current source I_1. The second terminal of the positive reference current source I_1 is connected to the substrate supply voltage source **VSS**.

[0037] The negative current limit circuit **240a** has an NMOS transistor **MN2** that is a dummy transistor characteristic that are matched to the geometry and impurity implantations of the NMOS transistor **MN1.** The NMOS transistor **MN2** is used to generate the reference voltage V_{LIM-} for the current limit of the current passing through the NMOS transistor **MN1** across the negative reference current source I_2. The first terminal of the negative reference current source I_2 is connected to the power supply voltage source **VDD.** The drain of the NMOS transistor **MN2** is connected to a second terminal of the negative reference current source I_2 and the source of the NMOS transistor **MN2** is connected to the substrate supply voltage source **VSS**. The NMOS transistor **MN2** has a gate connected to the output of the negative driver circuit **230b**.

[0038] The junction **242** of the PMOS transistor **MP2** and the first terminal of the first current source I_1 is connected to a first terminal of the third comparator **247** of the pulse width modulation/pulse frequency modulation control circuit **245**. Similarly, the junction **244** of the NMOS transistor **MN2** and the second terminal of the second current source I_2 is connected to a first terminal

of the fourth comparator **249** of the pulse width modulation/pulse frequency modulation control circuit **245.** The second terminals of the third comparator **247** and fourth comparator **249** are connected to the connection of the drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** with the first terminal of the inductor **L1** of Fig. 2. The reference voltage $\mathbf{V_{LIM+}}$ and reference voltage $\mathbf{V_{LIM-}}$ are compared with the voltage $\mathbf{V_{LX}}$ developed at the connection of the drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** with the first terminal of the inductor **L1** during the corresponding part of the duty cycle to determine when the output current is too high. The results of the comparison of the reference voltage $\mathbf{V_{LIM+}}$ and reference voltage $\mathbf{V_{LIM-}}$ with the voltage $\mathbf{V_{LX}}$ are applied to the control logic circuit **246** to generate the reset signals $\mathbf{V_{RST+}}$ and $\mathbf{V_{RST-}}$ that are transferred respectively to the reset terminals **R** of the first data flip-flop **227** and the second data flip-flop **229**.

[0039] As noted above, the output of the first driver circuit **230a** controls the gate of the PMOS transistor **MP1** and the output of the second driver circuit **230b** controls the gate of the NMOS transistor **MN1.** With the input of the driver circuit **230a** being controlled by the output of the first data flip-flop **227** and the input of the driver circuit **230b** being controlled by the second data flip-flop **229**. If the first control signal **216** or the second control signal **218** as applied to the data inputs of the first data flip-flop **227** and the input of the second data flip-flop **229** are active at the receipt of the triggering edge of the clock pulse signal **252**, the output of the first data flip-flop **227** and the output of the second data flip-flop **229** turn on the corresponding PMOS transistor **MP1** or NMOS transistor **MN1**. The activated PMOS transistor **MP1** or NMOS transistor **MN1** is then turned off by the corresponding reset signals $\mathbf{V_{RST+}}$ and $\mathbf{V_{RST}}$.

[0040] It should be noted that the control logic circuit **246** has circuitry that will permit the reset signals $\mathbf{V_{RST+}}$ and $\mathbf{V_{RST-}}$ to turn on the either the activated PMOS transistor **MP1** or NMOS transistor **MN1,** as required. In some embodiments, the second comparator **219** is offset by approximately 10mV as determined by the second reference voltage $\mathbf{V_{ref2}}$ to allow a small range of output voltages for which the PMOS transistor **MP1** or NMOS transistor are not switched to provide a saving in power for very low loads.

[0041] Fig. 4 is a schematic of an embodiment of a positive dynamic current limit circuit **240a** and a negative dynamic current limit circuit **240b** incorporated within a DC-to-DC converter of Fig. 2. In the embodiment as shown, a first differential amplifier **241** receives the first reference voltage $\mathbf{V_{REF1}}$ and the feedback voltage $\mathbf{V_{FB}}$ to be compared. The output of the differential amplifier **241** is connected to a gate of a first NMOS switching transistor **N1**. The drain of the first NMOS switching transistor **N1** is connected to a first terminal of a third current source $\mathbf{I_3}$ that sources a maximum positive reference current $\mathbf{I_{MAX+}}$. A second terminal of the third current source $\mathbf{I_3}$ is connected to the power supply voltage source **VDD**.

[0042] The NMOS transistors **N2** and **N3** form a first limit current mirror designated as a positive limit current mirror. The NMOS transistor **N2** is a diode-connected transistor that forms the reference leg of the positive limit current mirror and has its gate and drain commonly connected to the first terminal of the third current source $\mathbf{I_3}$. The source of the NMOS transistor **N2** is connected to the substrate supply voltage source **VSS**. The NMOS transistor **N3** forms the mirror leg of the positive limit current source and has its gate connected to the commonly connected gate and drain of the NMOS transistor **N2** of the reference leg. The drain of the NMOS transistor **N3** is connected to the drain of a dummy PMOS transistor **P1**. The source of the dummy PMOS transistor **P1** is connected to the power supply voltage source **VDD** and the gate of the dummy PMOS transistor **P1** is connected to the substrate supply voltage source **VSS**. The dummy PMOS transistor **P1** is matched to the geometry and impurity implantations of the PMOS transistor **MP1** of Fig. 2.

[0043] The first differential amplifier **241** compares the first reference voltage $\mathbf{V_{REF1}}$ and the feedback voltage $\mathbf{V_{FB}}$ voltage. The voltage level of the output of the differential amplifier **241** causes the NMOS transistor **N1** to steal current from the third current source $\mathbf{I_3}$ that sources a maximum positive reference current $\mathbf{I_{MAX+}}$. The maximum positive reference current $\mathbf{I_{MAX+}}$ sets the maximum current limit possible. The current mirror formed by the NMOS transistors **N2** and **N3** then mirrors the remaining current through the dummy PMOS transistor P1. In various embodiments, a fourth current source $\mathbf{I_4}$ provides a fixed minimum current that may optionally be necessary. The output reference voltage $\mathbf{V_{LIM+}}$ is applied to the input of the pulse width modulation/pulse frequency modulation control circuit **245**.

[0044] A second differential amplifier **243** receives the second reference voltage $\mathbf{V_{REF2}}$ and the feedback voltage $\mathbf{V_{FB}}$ to be compared. The output of the differential amplifier **243** is connected to a gate of a second PMOS switching transistor **P2**. The drain of the second PMOS switching transistor **P2** is connected to a first terminal of a fifth current source $\mathbf{I_5}$ that sources a maximum negative reference current $\mathbf{I_{MAX-}}$. A second terminal of the fifth current source $\mathbf{I_5}$ is connected to the substrate supply voltage source **VSS**.

[0045] The PMOS transistors **P3** and **P4** form a second limit current mirror designated as a negative limit current mirror. The PMOS transistor **P3** is a diode-connected transistor that forms the reference leg of the positive limit current mirror and has its gate and drain commonly connected to the first terminal of the fifth current source $\mathbf{I_5}$. The source of the PMOS transistor **P3** is connected to the power supply voltage source **VDD**. The PMOS transistor **P4** forms the mirror leg of the negative limit current source and has its gate connected to the commonly connected gate and drain of the PMOS transistor **P3** of the reference leg. The drain of the PMOS transistor **P4** is connected to the drain of a dummy NMOS transistor **N4**. The source of the dummy NMOS transistor **N4** is con-

nected to the substrate supply voltage source **VSS** and the gate of the dummy PMOS transistor **P1** is connected to the power supply voltage source **VDD**. The dummy NMOS transistor **N4** is matched to the geometry and impurity implantations of the NMOS transistor **MN1** of Fig. 2.

[0046] The second differential amplifier **243** compares the second reference voltage V_{REF2} and the feedback voltage V_{FB} voltage. The voltage level of the output of the second differential amplifier **243** causes the PMOS transistor **P2** to steal current from the fifth current source I_5 that sinks a maximum negative reference current I_{MAX-}. The maximum negative reference current I_{MAX-} sets the maximum negative current limit possible. The current mirror formed by the PMOS transistors **P3** and **P4** then mirrors the remaining current through the dummy NMOS transistor **N4**. In various embodiments, a sixth current source I_6 provides a fixed minimum current that may optionally be necessary. The output reference voltage V_{LIM-} is applied to the input of the pulse width modulation/pulse frequency modulation control circuit **245**.

[0047] The reference voltage V_{LIM+} and reference voltage V_{LIM-} are compared in the comparators **247** and **249** with the voltage V_{LX} developed at the connection of the drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** with the first terminal of the inductor **L1** during the corresponding part of the duty cycle to determine when the output current is too high. The results of the comparison of the reference voltage V_{LIM+} and reference voltage V_{LIM-} with the voltage V_{LX} are applied to the control logic circuit **246** to generate the reset signals V_{RST+} and V_{RST-} that are transferred respectively to the reset terminals **R** of the first data flip-flop **227** and the second data flip-flop **229.**

[0048] As noted above, the output of the first driver circuit **230a** controls the gate of the PMOS transistor **MP1** and the output of the second driver circuit **230b** controls the gate of the NMOS transistor **MN1**. The input of the driver circuit **230a** is controlled by the output of the first data flip-flop **227** and the input of the driver circuit **230b** is controlled by the second data flip-flop **229**. If the first control signal **216** or the second control signal **218** as applied to the data inputs of the first data flip-flop **227** and the input of the second data flip-flop **229** are active at the receipt of the triggering edge of the clock pulse signal **252**, the output of the first data flip-flop **227** and the output of the second data flip-flop **229** turn on the corresponding PMOS transistor **MP1** or NMOS transistor **MN1**. The activated PMOS transistor **MP1** or NMOS transistor **MN1** is then turned off by the corresponding reset signals V_{RST+} and V_{RST-}.

[0049] As noted above, the control logic circuit **246** has circuitry that will permit the reset signals V_{RST+} and V_{RST-} to turn on the either the PMOS transistor **MP1** or the NMOS transistor **MN1**, as required. In some embodiments, the second comparator **219** is offset by approximately 10mV as determined by the second reference voltage V_{ref2} to allow a small range of output voltages for which the PMOS transistor **MP1** or NMOS transistor **MN1** are not switched to provide a saving in power for very low loads.

[0050] Fig. 5 is a schematic of a DC-to-DC converter with a dynamic sleep mode embodying the principals of the present disclosure. In various embodiments, the switch control circuit **305** has a digital-to-analog converter **310** that receives a reference control word **314**. The digital-to-analog converter **310** converts the reference control word **314** to the reference voltage V_{REF}. The reference voltage V_{REF} is one of the two inputs to the feedback stage **315**. The feedback stage **315** has a first comparator **317** and a differential amplifier **319** that receive the reference voltage V_{REF}. The second input **307** of the feedback stage **315** receives the feedback voltage V_{FB} that is compared to the reference voltage V_{REF}. As described previously, the feedback voltage V_{FB} is developed from the output voltage V_{OUT} at common connection of the second terminal of the inductor **L1** and the first terminal of the output capacitor C_{OUT} of the filter section **235**.

[0051] The output **316** of the first comparator **317** is the first input to the switching control circuit **325**. The first comparator **317** provides the positive control signal V_{UNDER+} that is applied to a data input of a first data flip-flop **326** of the switching control circuit **325**. The output **318** of the differential amplifier **319** provides a current control signal that is applied to a differential current source I_7. The differential current source I_7 develops a reference limit current I_{LIM}. The sense circuit **340** provides a load for the differential current source I_7 and thus the current limit flag signal $V_{ILIMFLG}$.

[0052] . The current control signal from the output **318** of the differential amplifier **319** adjusts the differential current source I_7 such that the voltage levels are such that the data input of the second data flip-flop **328** of the switching control circuit **325** are at the correct logic levels for controlling the switching of the NMOS transistor **MN1.**

[0053] An oscillator **350** generates the clock pulse signal **352** that is applied to the clock **CK** input of the first data flip-flop **326** and the second data flip-flop **328**. The output of the first data flip-flop **326** is applied to the input of the positive driver circuit **330a** and the output of the second data flip-flop **329** is applied to the input of the negative driver circuit **330b**. The output of the first driver circuit **330a** is applied to the gate of the PMOS transistor **MP1** and the output of the second driver circuit **330b** is applied to the gate of the NMOS transistor **MN1**.

[0054] The source of the PMOS transistor **MP1** is connected to the power supply voltage source **VDD** and the source of the NMOS transistor **MN1** is connected to the substrate supply voltage source **VSS**. The substrate supply voltage source **VSS** is often the ground reference voltage source, but in some applications is a negative voltage level. The commonly connected drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** are connected to an input terminal of the filter section **235**. The input terminal is a first terminal of an inductor **L1**. The data output of the first data flip-flop **326** is applied to

the driver circuit **330a** and the data output of the second data flip-flop **327** is applied to the driver circuit **330b**. When states of the first flip-flop **326** and the second flip-flop **327** are such that the PMOS transistor **MP1** is turned on and the NMOS transistor **MN1** is turned off, a current from the power supply voltage source **VDD** from the first terminal of the inductor **L1** out the second terminal of the inductor **L1** into the first terminal of the output capacitor $\mathbf{C_{OUT}}$ and to the substrate supply voltage source **VSS**. The output voltage $\mathbf{V_{OUT}}$ is present at the junction of the second terminal of the inductor **L1** and the output capacitor $\mathbf{C_{OUT}}$.

[0055] In the dynamic sleep mode, the reference limit current $\mathbf{I_{LIM}}$ from the differential current source $\mathbf{I_7}$ is allowed to vary and thus enable the DC-to-DC converter to support very high loads. The sense circuit **340** senses the output current $\mathbf{I_{OUT}}$ when the PMOS transistor **MP1** is turned on. The sense circuit **340** generates a sense current $\mathbf{I_{SENSE}}$ produces a current proportional to the current in the PMOS transistor **MP1**. The sense current $\mathbf{I_{SENSE}}$ is compared to the reference limit current $\mathbf{I_{LIM}}$. When the sense current $\mathbf{I_{SENSE}}$ from sense circuit **340** is greater than the reference limit current $\mathbf{I_{LIM}}$ then the voltage on current limit flag signal $\mathbf{V_{ILIMFLG}}$ assumes a first logic level (1). When the sense current $\mathbf{I_{SENSE}}$ from sense circuit **340** is less than the reference limit current $\mathbf{I_{LIM}}$ then the voltage on current limit flag signal $\mathbf{V_{ILIMFLG}}$ assumes a second logic level (0).

[0056] When the sense current $\mathbf{I_{SENSE}}$ is greater than the reference limit current $\mathbf{I_{LIM}}$, the current limit flag signal $\mathbf{V_{ILIMFLG}}$ indicates that current limit is achieved and the control circuit **328** generates the data applied to the input of the first flip-flop **326** that will force the first driver circuit **330a** to turnoff the PMOS transistor **MP1.** The reference limit current $\mathbf{I_{LIM}}$ is modulated by the output voltage of the differential amplifier **319** as a result of the comparison of the feedback voltage $\mathbf{V_{FB}}$ with the reference voltage $\mathbf{V_{REF}}$. As the feedback voltage $\mathbf{V_{FB}}$ falls below the reference voltage $\mathbf{V_{REF}}$, the reference current is increased, and so the current limit value is also increased.

[0057] Fig. 6 is a plot of the waveforms of the signals the DC-to-DC converter in dynamic sleep mode operation of Fig. 5. When the feedback voltage $\mathbf{V_{FB}}$ falls below the reference voltage $\mathbf{V_{REF}}$ from digital-to-analog converter **310**, the output of the first comparator **317** rises from the second level (0) to the first level (1) at the time τ_0 to activate the positive control signal $\mathbf{V_{UNDER+}}$. The first level (1) is applied through the control circuit **328** to the first data flip-flop **326**. The data present at the data input **D** of the first data flip-flop **326** is not transferred to the output of the first data flip-flop **326** until the rising edge of the clock **CLK** at the time τ_1 at which time the gate of the PMOS transistor **MP1** is brought to the first level (0) to turn on the PMOS transistor **MP1** such that current $\mathbf{I_{COIL}}$ passes to the first terminal of the inductor **L1**.

[0058] The current $\mathbf{I_{COIL}}$ through the inductor **L1** rises from the time τ_1 to the time τ_2 when the current $\mathbf{I_{COIL}}$ reaches the magnitude of the reference limit current $\mathbf{I_{LIM}}$. The voltage of the current limit flag signal $\mathbf{V_{ILIMFLG}}$, developed at the top of the differential current source $\mathbf{I_7}$ is applied to the control circuit **328** and the control circuit **328** sets the data at the data inputs **D** of the first and second data flip-flops **326** and **327** such that the PMOS transistor **MP1** and the NMOS transistor **MN1** are turned off. With the PMOS transistor **MP1** and the NMOS transistor **MN1** are turned off, the current $\mathbf{I_{COIL}}$ falls toward zero and the DC-to-DC converter operates in the discontinuous mode. When the current $\mathbf{I_{COIL}}$ falls sufficiently less than the reference limit current $\mathbf{I_{LIM}}$, the voltage of the current limit flag signal $\mathbf{I_{LIMFLG}}$ is deactivated to essentially the first level (0) at the time τ_1.

[0059] In some embodiments as shown in Fig. 5, the limit current $\mathbf{I_{LIM}}$ is controlled by the sum of two reference currents. The first reference current is provided by the adjustable differential current source $\mathbf{I_7}$, as described above. The second reference current is fixed ramp current source $\mathbf{I_8}$**.** The reference limit current $\mathbf{I_{LIM}}$ of the adjustable differential current source $\mathbf{I_7}$ and the compensation current $\mathbf{I_{COMP}}$ of the fixed ramp current source $\mathbf{I_8}$ are additively combined to provide a degree of compensation to prevent sub-harmonic oscillation. The ramp waveform of the compensation current $\mathbf{I_{COMP}}$ should start at a high value and have a negative slope. In some embodiments, the compensation current $\mathbf{I_{COMP}}$ has a negative value thus subtracting current from differential current source $\mathbf{I_7}$.

[0060] Fig. 7 is a plot of the waveforms of the signals the DC-to-DC converter of Fig. 5 in dynamic sleep mode operation illustrating a change in output current $\mathbf{I_{OUT}}$ to the external load circuit. When the output current $\mathbf{I_{OUT}}$ increases at the time τ_0, the feedback voltage $\mathbf{V_{FB}}$ starts to fall until it is below the below the reference voltage $\mathbf{V_{REF}}$ from digital-to-analog converter **310**, the output of the first comparator **317** rises at the time τ_1 from the second logic level (0) to the first logic level (1) to activate the positive control signal $\mathbf{V_{UNDER+}}$**.** The first logic level (1) is applied through the control circuit **328** to the first data flip-flop **326.** The data present at the data input **D** of the first data flip-flop **326** is not transferred to the output of the first data flip-flop **326** until the rising edge of the clock **CLK** at the time τ_2 at which time the gate of the PMOS transistor **MP1** is brought to the first level (0) to turn on the PMOS transistor **MP1** such that current $\mathbf{I_{COIL}}$ passes to the first terminal of the inductor **L1.**

[0061] The current $\mathbf{I_{COIL}}$ through the inductor **L1** rises from the time τ_2 to the time τ_3 when the coil current $\mathbf{I_{COIL}}$ reaches the magnitude of the reference limit current $\mathbf{I_{LIM1}}$. The voltage of the current limit flag signal $\mathbf{V_{ILIMFLG}}$, developed at the top of the differential current source $\mathbf{I_7}$ is applied at the time time τ_3 to the control circuit **328** and the control circuit **328** sets the data at the data inputs **D** of the first and second data flip-flops **326** and **327** such that the PMOS transistor **MP1** and the NMOS transistor **MN1** are turned off. With the PMOS transistor **MP1** and the NMOS transistor **MN1** are turned off, the current $\mathbf{I_{COIL}}$ falls toward zero from the time τ_3 to the time τ_4 and the

DC-to-DC converter operates in the discontinuous mode. When the current I_{COIL} falls sufficiently less than the first reference limit current I_{LIM1}, the voltage of the current limit flag signal $V_{ILIMFLG}$ is deactivated to essentially the first level (0) shortly after the time τ_3.

[0062] The feedback voltage V_{FB} has also decreased from the time τ_3 to the time τ_4 and remains less than the reference voltage V_{REF} such that at the time τ_4, the gate of the PMOS transistor **MP1** is activated with the rising edge of the clock pulse **CLK.** The coil current I_{COIL} begins to rise between the time τ_4 and the time τ_5. In the time between the time τ_4 and the time τ_5, the first reference limit current I_{LIM1} from the differential current source I_7 is adjusted by the differential voltage ΔV from the differential amplifier **319** to a second reference limit current I_{LIM2}. When the coil current I_{COIL} reaches the level of the second reference limit current I_{LIM2}, the current limit flag signal $V_{ILIMFLG}$ is activated shortly before the time τ_5. The gate of the PMOS transistor **MP1** is set to the first logic level (1) and the PMOS transistor **MP1** is turned off at the time at the time τ_5. When the current I_{COIL} falls sufficiently less than the second reference limit current I_{LIM2}, the voltage of the current limit flag signal $V_{ILIMFLG}$ is deactivated to essentially the second level (0) shortly after the time τ_5. The coil current I_{COIL} falls between the time τ_5 and the time τ_6 such that the feedback voltage V_{FB} is decreasing from the time τ_5 to the time τ_6 and remains less than the reference voltage V_{REF} such that at the time τ_6 gate of the PMOS transistor **MP1** is activated with the rising edge of the clock pulse **CLK.**

[0063] The cyclic operation from the time τ_4 to the time τ_{12} is equivalent to that described between the time τ_4 and the time τ_6. This process continues until the output current I_{OUT} decreases the normal dynamic sleep mode or the system commands the DC-to-DC converter to resume the normal continuous operation mode.

[0064] Fig. 8 is flowchart of a method for providing hysteretic mode control within a DC-to-DC converter **200** of Fig. 2. The most positive voltage limit V_{ILM+} representing a maximum current I_{LIM+} to pass through the inductor **L1** of the low pass filter section **235** is determined (Box **400**). Similarly, the most negative voltage limit V_{ILM-} representing a minimum current I_{LIM-} to pass through the inductor **L1** of the low pass filter section **235** is determined (Box **405**). The voltage V_{LX} present at the junction of the drains of the PMOS transistor **MP1** and the NMOS transistor **MN1** with the first terminal of the inductor **L1** is compared (Box **405**) with the positive voltage limit V_{ILM+}. If the voltage V_{LX} is greater than or equal to the positive voltage limit V_{ILM+}, the first data flip-flop **227** is reset (Box **405**) and the PMOS transistor **MP1** is turned off. The voltage V_{LX} is compared (Box **430**) with the negative voltage limit V_{ILM-}. If the voltage V_{LX} is not greater than or equal to the negative voltage limit V_{ILM-}, the NMOS transistor **MN1** is turned on (Box **445**). The operational mode of the DC-to-DC converter **200** is queried (Box **450**) to determine if the dynamic sleep mode is to be terminated and the normal continuous operational mode resumed.

[0065] If the dynamic sleep mode is to be continued, the process then returns to the comparing (Box **405**) of the voltage V_{LX} with the positive voltage limit V_{ILM+}. If, this instance, the voltage V_{LX} is not greater than or equal to the positive voltage limit V_{ILM+}, the PMOS transistor **MP1** is turned on. The voltage V_{LX} is compared (Box **430**) with the negative voltage limit V_{ILM-}. If the voltage V_{LX} is greater than or equal to the negative voltage limit V_{ILM-}, the data flip-flop **229** is reset (Box **435)** and the NMOS transistor **MN1** is turned off (Box **440**). The operational mode of the DC-to-DC converter **200** is again queried (Box **450**) to determine if the dynamic sleep mode is to be terminated and the normal continuous operational mode resumed. If the normal continuous operational mode is to be resumed the process is ended. If the dynamic sleep mode is to be continued, the process as above described, continues.

[0066] Fig. 9 is flowchart of a method for providing hysteretic mode control within a DC-to-DC converter **300** of Fig. 5. When the DC-to-DC converter **300** is set to begin (Box **500**) the dynamic sleep mode, the voltage reference V_{ref} and the feedback voltage V_{FB} are compared (Box **505**) to determine the positive control signal V_{UNDER+}. The differential ΔV between the voltage reference V_{ref} and the feedback voltage V_{FB} is amplified (Box **510**) and then converted (Box **515**) to a differential current ΔV. The limiting current I_{LIM} is set (Box **520)** as the subtractive combination of the sense current I_{SENSE} and the differential current ΔV. The limiting current I_{LIM} determines (Box **525**) a current limit flag signal $V_{ILIMFLG}$.

[0067] From the positive control signal V_{UNDER+} and the current limit flag signal $V_{ILIMFLG}$, the state of the voltage to be applied to the gate of the PMOS transistor **MP1** and the gate of the NMOS transistor **MN1** are determined (Box **530**). The states of the voltage applied to the gate of the PMOS transistor **MP1** and the gate of the NMOS transistor **MN1** may be such that either the PMOS transistor **MP1** is turned on and the NMOS transistor **MN1** is turned off, or the PMOS transistor **MP1** is turned off and the NMOS transistor **MN1** is turned on, or the PMOS transistor **MP1** is turned off and the NMOS transistor **MN1** is turned off. The state of the gate of the PMOS transistor **MP1** is examined (Box **535**) to determine if the PMOS transistor **MP1** is turned on. The NMOS transistor **MN1** is turned off (Box **540**) and the PMOS transistor **MP1** is turned on (Box **545**), if the state of the gate of the PMOS transistor **MP1** indicates the PMOS transistor **MP1** is to be turned on. If the state of the gate of the PMOS transistor **MP1** indicates the PMOS transistor **MP1** is to be turned off, the PMOS transistor **MP1** is turned off (Box **545**) and the state of the gate of the NMOS transistor **MN1** is examined (Box **555**) to determine if the NMOS transistor **MN1** is turned on. The NMOS transistor **MN1** is turned on (Box **560**), if the state of the gate of the NMOS transistor **MN1** indicates the NMOS transistor **MN1** is to be turned on. If the state of the gate of the NMOS transistor **MN1** indicates the NMOS transistor **MN1** is to be turned off, the NMOS transistor **MN1** is turned off (Box

565). If the PMOS transistor **MP1** is turned on (Box **545**) or the NMOS transistor **MN1** is turned on (Box **560**), or the PMOS transistor **MP1** is turned off (Box 550) and NMOS transistor **MN1** is turned off (Box **565**), the sleep mode is examined (Box **570**) to determine if the continuous mode is to be resumed. If the sleep mode is to be continue, the next cycle is started **500** and the process as described above is repeated. If the sleep mode is to be discontinued, the continuous mode is resumed and the dynamic sleep mode is ended.

[0068] While this disclosure has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the scope of the disclosure.

Claims

1. A hysteretic mode control circuit within a DC-to-DC converter (200) that is configured for operating in a continuous mode or a discontinuous mode, the DC-to-DC converter comprising a switching section (220) and a low pass filter section (235) that removes the high frequency harmonics created by the switching section (220) to generate a desired DC output voltage level to a load device placed at an output of the DC-to-DC converter (200), the switching section (220) comprising a first switch (MP1) and a second switch (MP2), the hysteretic mode control circuit being **characterized by** comprising :

- a first dynamic current limit circuit (240a) configured for determining a first reference limit signal (242) that is used for controlling activation of the first switch (MP1) of the switching section (220) of the DC-to-DC converter (200) for transferring current (I_{OUT}) to the load device placed at an output of the DC-to-DC converter (200), wherein the first dynamic current limit circuit (240a) comprises
a first reference current source (I_3) configured for providing a first maximum reference current (I_{MAX+});
a first limit current mirror (N2 and N3) connected such that a reference leg (N2) of the first limit current mirror (N2 and N3) receives the first maximum reference current (I_{MAX+}) and configured such that a mirror leg (N3) of the first limit current mirror (N2 and N3) is connected to provide the first reference limit signal (242) for an output of the first current limit circuit (240a) for determining the switching interval and duration of the first switch (MP1) to provide a current to the filter section (235) of the DC-to-DC converter (200);
a comparator (241) connected to receive a first reference signal (V_{REF1}) and a feedback signal (V_{FB}) from the output of the DC-to-DC converter (200) and configured for determining if the feedback signal (V_{FB}) is greater than or less than the first reference signal (V_{REF1}) to generate an output signal; and
a comparison switching device (N1) connected to receive the output signal of the comparator (241) that is activated or deactivated for diverting a current from the reference leg (N2) of the first limit current mirror (N2 and N3) and thus modify the current in the reference leg (N2) and thus the mirror leg (N3) of the first limit current mirror (N2 and N3) and thus adjust the voltage level of the first reference limit signal (242); and
- a pulse width modulation/pulse frequency modulation control circuit (245) configured for receiving the first reference limit signal (242), configured for comparing an amplitude of the first reference limit signal (242) with a feedback signal (V_{LX}) from the input of the low pass filter (235) and configured for generating a first reset control signal (V_{RST+}) and a second reset control signal (V_{RST-}) for controlling deactivation of the first switch (MP1) and the second switch (MP2) of the DC-to-DC converter (200); wherein the first current limit circuit (240a) and the pulse width modulation/pulse frequency modulation control circuit (246) are configured for varying a current limit that controls an interval and duration of time at which the switching section (220) of the DC-to-DC converter (200) is switched to permit the DC-to-DC converter (200) to manage large changes in an output current load (I_{OUT})of the DC-to-DC converter (200) while operating in the discontinuous operation mode.

2. The hysteretic mode control circuit of claim 1 wherein the dynamic current limit circuit (240a) comprises:

- a first matching switch (P1) configured with geometry and impurity implantations matching the first switch (MP1) of the DC-to-DC converter (200) and connected to a ground reference voltage source (VSS); and
- a second reference current source (I_4) connected to the first matching switch (P2) to develop the first reference limit signal (242) for controlling the turning on and turning off the first switch (MP1).

3. The hysteretic mode control circuit of claim 1 further comprising:

- a second dynamic current limit circuit (240b) configured for determining a second reference limit signal (244) that is used for controlling activation of the second switch (MN2) of the power

switching section (220) of the DC-to-DC converter (200) for transferring current (I_{OUT}) to the load device placed at the output of the DC-to-DC converter (200); and

wherein the pulse width modulation/pulse frequency modulation control circuit (245) is configured for receiving the second reference limit signal (244), configured for comparing an amplitude of the second reference limit signal (244) with the feedback signal (V_{LX}) from the power switching section (220) of the DC-to-DC converter (200), and configured for employing the first and second reference limit signals (242, 244) for generating the first and second reset controls (V_{RST+} and V_{RST-}) for activation of the first switch (MP1) and the second switch (MN1).

4. The hysteretic mode control circuit of claim 3 wherein the second dynamic current limit circuit (240b) comprises:

- a second matching switch (N4) configured with geometry and impurity implantations matching the second switch (MN1) and connected to the power supply voltage source (VDD); and
- a second reference current source (I_6) connected to the second matching switch (N4) to develop the second reference limit signal (244) for controlling the turning on and turning off the second switch (MN1).

5. The hysteretic mode control circuit of claim 3 wherein the second dynamic current limit circuit (240b) comprises:

- a second reference current source (I_5) configured for providing a second maximum reference current (I_{MAX-});
- a second limit current mirror (P3, P4) connected such that a reference leg (P3) of the second limit current mirror (P3, P4) receives the second maximum reference current (I_{MAX-}) and configured such that a mirror leg (P4) of the second limit current mirror (P3, P4) is connected to provide the second reference limit signal (244) for an output of the second current limit circuit (240b) to determine an interval and duration of time at which the second switch (MN1) of the power switching section (220) is switched to provide current to the filter section (235) of the DC-to-DC converter (200);
- a comparator (243) connected to receive a second reference limit signal (V_{REF2}) and the feedback signal I (V_{FB}) from the output of the DC-to-DC converter (200) and configured for determining if the feedback signal (V_{FB}) is greater than or less than the second reference limit signal (V_{REF2}) to generate an output signal; and
- a comparison switching device (P2) connected to receive the output signal of the comparator (243) that is activated or deactivated to divert current from the reference leg (P3) of the second limit current mirror (P3, P4) and thus modify the current in reference leg (P3) and thus the mirror leg (P4) of the second limit current mirror (P3, P4) and thus adjust the voltage level of the second reference limit signal (244).

6. The hysteretic mode control circuit of claim 1 wherein the first dynamic current limit circuit (240a) further comprises a first load device (P1) connected to the mirror leg (N3) of the first limit current mirror (N2, N3) for developing the first reference limit voltage (V_{LIM+}).

7. The hysteretic mode control circuit of claim 5 wherein the second dynamic current limit circuit (240b) further comprises a second load device (N4) connected to the mirror leg (P4) of the second limit current mirror (P3, P4) for developing the second reference limit voltage (V_{LIM-}).

8. A DC-to-DC converter comprising a hysteretic mode control circuit according to anyone of claim 1 to 7.

9. A method for providing hysteretic mode control by supervising a switching interval and duration of a power switching section (220) of a DC-to-DC converter (200) to permit the DC-to-DC converter (200) to manage large changes in an output load current (I_{OUT}) of the DC-to-DC converter (200) during a sleep mode, the DC-to-DC converter comprising a low pass filter section (235) that removes the high frequency harmonics created by the switching section (220) to generate a desired DC output voltage level to a load device placed at an output of the DC-to-DC converter (200), the switching section (220) comprising a first switch (MP1) and a second switch (MP2), the method being **characterized in that** it comprises the steps of:

- determining (400) a first limit signal (242) proportional to a first limit current (I_{MAX+}) flowing in the low pass filter (235) of the DC-to-DC converter (200) wherein determining the first limit signal (242) comprises the steps of:

  setting a maximum reference current (I_{MAX+});
  determining a difference between a reference voltage (V_{REF1}) of the DC-to-DC converter (200) and a feedback voltage (V_{FB}) of the DC-to-DC converter (200) as a difference voltage;
  converting the difference voltage to a difference current;

subtracting the difference current from the maximum reference current (I_{MAX+}) to form a first variable limit current;
mirroring the first variable limit current; and
converting the first variable limit current to the first limit signal (242),

- comparing (410) an input signal (V_{LX}) of the low pass filter (235) with the first limit signal (242);
- resetting (435) a first latching circuit (227) for disabling a first switching device (MP1) to prevent a current from flowing into the low pass filter (235), when the input signal (V_{LX}) is greater than a first limit signal (242); and
- allowing the current to continue to flow into the low pass filter (235), when the input signal (V_{LX}) is less than the first limit signal (242) by not resetting the first latching circuit (227) and not disabling the first switching device (MP1).

10. The method for providing hysteretic mode control of claim 9 further comprising the steps of:

- determining (405) a second limit signal (244) proportional to a second limit current flowing in the low pass filter (235) of the DC-to-DC converter (200) ;
- comparing (430) the input signal (V_{LX}) of the low pass filter (235) with the second limit signal (244) ;
- resetting (435) a second latching circuit (229) for disabling a second switching device (MN1) to prevent a current from flowing from the low pass filter (235), when the input signal (V_{LX}) is less than a second limit signal (244); and
- allowing a current to continue to flow from the low pass filter (235), when the input signal (V_{LX}) is greater than the first limit signal (244) by not resetting the second latching circuit (229) and not disabling the second switching device (MN1).

11. The method for providing hysteretic mode control of claim 10 wherein determining the second limit signal comprises the steps of:

- setting a minimum reference current (I_{MAX-});
- determining a difference between a reference voltage (V_{REF}) of the DC-to-DC converter (200) and a feedback voltage (V_{FB}) of the DC-to-DC converter (200) as a difference voltage;
- converting the difference voltage to a difference current;
- subtracting the difference current from the minimum reference current (I_{MAX-}) to form a second variable limit current;
- mirroring the second variable limit current; and
- converting the second variable limit current to the second limit signal (244).

Patentansprüche

1. Hysterese-Modus-Steuerschaltung innerhalb eines DC/DC-Wandlers (200), die zum Betrieb in einem kontinuierlichen Modus oder einem diskontinuierlichen Modus konfiguriert ist, wobei die Hysterese-Modus-Steuerschaltung **gekennzeichnet ist durch** :

- eine erste dynamische Strombegrenzungsschaltung (240a), die zum Bestimmen eines ersten Referenzbegrenzungssignals (242) konfiguriert ist, das zum Steuern der Aktivierung eines ersten Schalters (MP1) eines Schaltabschnitts (220) des DC/DC-Wandlers (200) zum Übertragen von Strom (I_{OUT}) an eine Lastvorrichtung verwendet wird, die an einem Ausgang des DC/DC-Wandlers (200) angeordnet ist, wobei die erste dynamische Strombegrenzungsschaltung (240a) umfasst

eine erste Referenzstromquelle (I_3), die zum Bereitstellen eines ersten maximalen Referenzstroms (I_{MAX+}) konfiguriert ist;
einen ersten Grenzstromspiegel (N2 und N3), der so geschaltet ist, dass ein Referenzschenkel (N2) des ersten Grenzstromspiegels (N2 und N3) den ersten maximalen Referenzstrom (I_3) empfängt, und so konfiguriert ist, dass ein Spiegelschenkel (N3) des ersten Grenzstromspiegels (N2 und N3) verbunden ist, um das erste Referenzgrenzsignal (242) zu liefern.für einen Ausgang der ersten Strombegrenzungsschaltung (240a) zum Bestimmen des Schaltintervalls und der Dauer des ersten Schalters (MP1) zum Bereitstellen eines Stroms für den Filterabschnitt (235) des DC-DC-Wandler (200);
einen Vergleicher (241), der verbunden ist, um das erste Referenzsignal (V_{REF1}) und ein Rückkopplungssignal (V_{FB}) vom Ausgang des DC/DC-Wandlers (200) zu empfangen, und der konfiguriert ist, um zu bestimmen, ob das Rückkopplungssignal (V_{FB}) größer oder kleiner als das erste Referenzgrenzsignal (242) ist, um ein Ausgangssignal zu erzeugen; und
eine Vergleichsschaltvorrichtung (N1), die angeschlossen ist, um das Ausgangssignal des Vergleichers (241) zu empfangen, der aktiviert oder deaktiviert ist, um einen Strom vom Referenzschenkel (N1) des ersten Grenzstromspiegels (N2 und N3) abzulen-

ken und so den Strom im Referenzschenkel (N2) und damit den Spiegelschenkel (N3) des ersten Grenzstromspiegels (N2 und N3) zu ändern und so den Spannungspegel des ersten Referenzstromsignals (242) einzustellen; und

- eine Pulsweitenmodulations-/Impulsfrequenzmodulationssteuerschaltung (245), die zum Empfangen des ersten Referenzgrenzsignals (242) konfiguriert ist, die zum Vergleichen einer Amplitude des ersten Referenzgrenzsignals (242) mit einem Rückkopplungssignal (V_{LX}) aus einem Leistungsschaltabschnitt (220) des DC/DC-Wandlers (200) konfiguriert ist und zum Erzeugen eines ersten Rückstellsteuersignals (V_{RST}) und eines zweiten Rückstellsteuersignals ($_{VRST1}$) zum Steuern der Abschaltung des ersten Schalters (MP1) und eines zweiten Schalters (MP2) des DC/DC-Wandlers (200) konfiguriert ist;

wobei die erste Strombegrenzungsschaltung (240a) und die Pulsweitenmodulations-/Impulsfrequenzmodulationssteuerschaltung (246) konfiguriert sind, um eine Strombegrenzung zu variieren, die ein Intervall und eine Zeitdauer steuert, in der der Schaltabschnitt (220) des DC/DC-Wandlers (200) geschaltet wird, um es dem DC/DC-Wandler (200) zu ermöglichen, große Änderungen in einer Ausgangsstromlast (IOUT) des DC/DC-Wandlers (200) während des Betriebs im diskontinuierlichen Betriebsmodus zu verwalten.

2. Die hysteretische Modus-Steuerschaltung nach Anspruch 1, wobei die dynamische Strombegrenzungsschaltung (240a) umfasst:

- einen ersten Anpassungsschalter (P1), der mit Geometrie- und Verunreinigungsimplantaten konfiguriert ist, die dem ersten Schalter (MP1) des DC/DC-Wandlers (200) entsprechen und mit einer Erdungsreferenzspannungsquelle (VSS) verbunden sind; und
- eine zweite Referenzstromquelle (I_4), die mit dem ersten Anpassungsschalter (P2) verbunden ist, um das erste Referenzgrenzsignal (242) zum Steuern des Ein- und Ausschaltens des ersten Schalters (MP1) zu entwickeln.

3. Die hysteretische Modus-Steuerschaltung nach Anspruch 1, ferner umfassend:

- eine zweite dynamische Strombegrenzungsschaltung (240b), die zum Bestimmen eines zweiten Referenzbegrenzungssignals (244) konfiguriert ist, das zum Steuern der Aktivierung des zweiten Schalters (MN2) des Leistungsschaltabschnitts (220) des DC/DC-Wandlers (200) zum Übertragen von Strom (I_{OUT}) an die am Ausgang des DC/DC-Wandlers (200) angeordnete Lastvorrichtung verwendet wird; und wobei die Pulsweitenmodulations-/Impulsfrequenzmodulationssteuerschaltung (245) zum Empfangen des zweiten Referenzgrenzsignals (244) konfiguriert ist, konfiguriert zum Vergleichen einer Amplitude des zweiten Referenzgrenzsignals (244) mit dem Rückkopplungssignal (V_{LX}) aus dem Leistungsschaltabschnitt (220) des DC/DC-Wandlers (200), und konfiguriert zum Verwenden des ersten und zweiten Referenzgrenzsignals (242, 244) zum Erzeugen der ersten und zweiten Rücksetzsteuerung (V_{RST+} undV_{RST-}) zum Aktivieren des ersten Schalters (MP1) und des zweiten Schalters (MN1).

4. Die hysterese-Modus-Steuerschaltung nach Anspruch 3, wobei die zweite dynamische Strombegrenzungsschaltung (240b) umfasst:

- einen zweiten Anpassungsschalter (N4), der mit Geometrie- und Verunreinigungsimplantaten konfiguriert ist, die dem zweiten Schalter (MN1) entsprechen und mit der Spannungsquelle (VDD) der Stromversorgung verbunden sind; und
- eine zweite Referenzstromquelle (I6), die mit dem zweiten Anpassungsschalter (N4) verbunden ist, um das zweite Referenzgrenzsignal (244) zum Steuern des Ein- und Ausschaltens des zweiten Schalters (MN1) zu entwickeln.

5. Die hysterese-Modus-Steuerschaltung nach Anspruch 3, wobei die zweite dynamische Strombegrenzungsschaltung (240b) umfasst:

- eine zweite Referenzstromquelle (I5), die zum Bereitstellen eines zweiten maximalen Referenzstroms (I_{MAX}-) konfiguriert ist;
- einen zweiten Grenzstromspiegel (P3, P4), der so geschaltet ist, dass ein Referenzschenkel (P3) des zweiten Grenzstromspiegels (P3, P4) den zweiten maximalen Referenzstrom (I_{MAX-}) empfängt und so konfiguriert ist, dass ein Spiegelschenkel (P4) des zweiten Grenzstromspiegels (P3, P4) verbunden ist, um das zweite Referenzgrenzsignal (244) für einen Ausgang der zweiten Stromgrenzschaltung (240b) bereitzustellen, um ein Intervall und eine Zeitdauer zu bestimmen, in der der zweite Schalter (MN1) des Leistungsschaltabschnitts (220) geschaltet wird, um dem Filterabschnitt (235) des DC/DC-Wandlers (200) Strom zuzuführen;
- einen Vergleicher (243), der angeschlossen ist, um ein zweites Referenzgrenzsignal (V_{REF2})

und das Rückkopplungssignal I (V_{FB}) vom Ausgang des DC/DC-Wandlers (200) zu empfangen, und der konfiguriert ist, um zu bestimmen, ob das Rückkopplungssignal (V_{FB}) größer oder kleiner als das zweite Referenzgrenzsignal (V_{REF2}) ist, um ein Ausgangssignal zu erzeugen; und

- eine Vergleichsschaltvorrichtung (P2), die angeschlossen ist, um das Ausgangssignal des Vergleichers (243) zu empfangen, der aktiviert oder deaktiviert ist, um den Strom vom Referenzschenkel (P3) des zweiten Grenzstromspiegels (P3, P4) abzuleiten und so den Strom im Referenzschenkel (P3) und damit den Spiegelschenkel (P4) des zweiten Grenzstromspiegels (P3, P4) zu modifizieren und so den Spannungspegel des zweiten Referenzstromsignals (244) einzustellen.

6. Die hysterese-Modus-Steuerschaltung nach Anspruch 1, wobei die erste dynamische Strombegrenzungsschaltung (240a) ferner eine erste Lastvorrichtung (P1) umfasst, die mit dem Spiegelschenkel (N3) des ersten Grenzstromspiegels (N2, N3) verbunden ist, um die erste Referenzgrenzspannung (V_{LIM+}) zu entwickeln.

7. Die hysterese-Modus-Steuerschaltung nach Anspruch 5, wobei die zweite dynamische Strombegrenzungsschaltung (240b) ferner eine zweite Lastvorrichtung (N4) umfasst, die mit dem Spiegelschenkel (P4) des zweiten Grenzstromspiegels (P3, P4) verbunden ist, um die zweite Referenzgrenzspannung (V_{LIM-}) zu entwickeln.

8. DC/DC-Wandler, umfassend eine hysteretische Modussteuerschaltung nach einem beliebigen der Ansprüche 1 bis 7.

9. Verfahren zum Bereitstellen einer hysteretischen Modussteuerung durch Überwachen eines Schaltintervalls und einer Dauer eines Leistungsschaltabschnitts (220) eines DC/DC-Wandlers (200), um es dem DC/DC-Wandler (200) zu ermöglichen, große Änderungen in einem Ausgangslaststrom (I_{OUT}) des DC/DC-Wandlers (200) während eines Schlafmodus zu verwalten, wobei das Verfahren **dadurch gekennzeichnet ist, dass** es die folgenden Schritte umfasst:

- Bestimmen (400) eines ersten Grenzsignals (242), das proportional zu einem ersten Grenzstrom (I_{MAX+}) ist, der in dem Tiefpassfilter (235) des DC/DC-Wandlers (200) fließt, wobei das Bestimmen des ersten Grenzsignals (242) die folgenden Schritte umfasst:

Einstellen eines maximalen Referenzstroms (I_{MAX+});

Bestimmen einer Differenz zwischen einer Referenzspannung (V_{REF1}) des DC/DC-Wandlers (200) und einer Rückkopplungspannung(V_{FB}) des DC/DC-Wandlers (200) als Differenzspannung;

Umwandeln der Differenzspannung in einen Differenzstrom;

Subtrahieren des Differenzstroms vom maximalen Referenzstrom (I_{MAX+}), um einen ersten variablen Grenzstrom zu bilden;

Spiegeln des ersten variablen Grenzstroms; und Umwandeln des ersten variablen Grenzstroms in das erste Grenzsignal (242),

- Vergleichen (410) eines Eingangssignals (V_{LX}) des Tiefpassfilters (235) mit dem ersten Grenzsignal (242);
- Zurücksetzen (435) einer ersten Verriegelungsschaltung (227) zum Deaktivieren einer ersten Schaltvorrichtung (MP1), um zu verhindern, dass ein Strom in den Tiefpassfilter (235) fließt, wenn das Eingangssignal (V_{LX}) größer als ein erstes Grenzsignal (242) ist; und
- Ermöglichen, dass der Strom weiterhin in den Tiefpassfilter (235) fließt, wenn das Eingangssignal (V_{LX}) kleiner als das erste Grenzsignal (242) ist, indem die erste Verriegelungsschaltung (227) nicht zurückgesetzt und die erste Schaltvorrichtung (MP1) nicht deaktiviert wird.

10. Verfahren zum Bereitstellen einer hysteretischen Modussteuerung nach Anspruch 9, ferner umfassend die Schritte:

- Bestimmen (405) eines zweiten Grenzsignals (244), das proportional zu einem zweiten Grenzstrom ist, der in dem Tiefpassfilter (235) des DC/DC-Wandlers (200) fließt;
- Vergleichen (430) des Eingangssignals (V_{LX}) des Tiefpassfilters (235) mit dem zweiten Grenzsignal (244) ;
- Zurücksetzen (435) einer zweiten Verriegelungsschaltung (229) zum Deaktivieren einer zweiten Schaltvorrichtung (MN1), um zu verhindern, dass ein Strom aus dem Tiefpassfilter (235) fließt, wenn das Eingangssignal (V_{LX}) kleiner als ein zweites Grenzsignal (244) ist; und
- Ermöglichen, dass ein Strom aus dem Tiefpassfilter (235) weiterfließt, wenn das Eingangssignal (V_{LX}) größer als das erste Grenzsignal (244) ist, indem die zweite Verriegelungsschaltung (229) nicht zurückgesetzt und die zweite Schaltvorrichtung (MN1) nicht deaktiviert wird.

11. Verfahren zum Bereitstellen einer hysteretischen Modussteuerung nach Anspruch 10, wobei das Be-

stimmen des zweiten Grenzsignals die folgenden Schritte umfasst:

- Einstellen eines minimalen Referenzstroms (I_{MAX-});
- Bestimmen einer Differenz zwischen einer Referenzspannung (V_{REF}) des DC/DC-Wandlers (200) und einer Rückführspannung (V_{FB}) des DC/DC-Wandlers (200) als Differenzspannung;
- Umwandeln der Differenzspannung in einen Differenzstrom;
- Subtrahieren des Differenzstroms vom minimalen Referenzstrom (I_{MAX-}), um einen zweiten variablen Grenzstrom zu bilden;
- Spiegeln des zweiten variablen Grenzstroms; und
- Umwandeln des zweiten variablen Grenzstroms in das zweite Grenzsignal (244).

Revendications

1. Un circuit de commande de mode hystérétique au sein d'un convertisseur DC-DC (200) qui est configuré pour fonctionner en mode continu ou en mode discontinu, le convertisseur DC-DC comprenant une partie de commutation (220) et une partie de filtre passe-bas (235) supprimant les harmoniques haute-fréquences créées par la partie de commutation (220) pour générer un niveau de tension de sortie DC à une charge placée à une sortie du convertisseur DC-DC (200), la partie de commutation (220) comprenant une première partie de commutation (MP1) et une seconde partie de commutation (MP2), le circuit de commande de mode hystérétique étant **caractérisé en ce qu'**il comporte :

- un premier circuit de limitation de courant dynamique (240a) configure pour déterminer un premier signal limite de référence (242) qui est utilisé pour commander l'activation du premier commutateur (MP1) de la partie de commutation (220) du convertisseur DC-DC (200) pour le transfert de courant (I_{OUT}) vers une charge disposée à une sortie du convertisseur DC-DC (200), dans lequel le premier circuit de limitation de courant dynamique (240a) comprend :

une première source de courant de référence (I_3) configurée pour fournir un premier courant de référence maximal (I_{MAX+});
un premier miroir de courant de limitation (N2 et N3) connectés de telle sorte qu'une branche de référence (N2) du premier miroir de courant de limitation (N2 et N3) reçoit le premier courant de référence maximal (I_{MAX+}) et configurée de telle sorte qu'une branche de miroir (N3) du premier miroir de courant de limitation (N2 et N3) est connectée pour fournir le premier signal de limitation de référence (é42) pour une sortie du premier circuit de limitation de courant (240a) pour déterminer l'intervalle et la durée de commutation du premier commutateur (MP1) pour fournir un courant à la partie de filtrage (235) du convertisseur DC-DC ;
un comparateur (241) connecté pour recevoir un premier signal de référence (V_{REF1}) et un signal de rétroaction (V_{FB}) de la sortie du convertisseur DC-DC (200) et configuré pour déterminer si le signal de rétroaction (V_{FB}) est supérieur ou inférieur au premier signal limitation de référence (V_{REF1}) pour générer un signal de sortie; et
un dispositif de commutation de comparaison (N1) connecté pour recevoir le signal de sortie du comparateur (241) qui est activé ou désactivé pour dévier un courant de la branche de référence (N1) du premier miroir de courant de limitation (N2 et N3) et ainsi modifier le courant de la branche de référence (n2) et ainsi de la branche miroir (N3) du premier miroir de courant de limitation (N2 et N3) et ainsi ajuster le niveau de tension du premier signal de limitation de référence (242) ; et

- un circuit de commande de modulation de fréquence d'impulsion/modulation de largeur d'impulsion (245) configuré pour recevoir le premier signal de limitation de référence (242), configuré pour comparer une amplitude du premier signal de limitation de référence (242) avec un signal de rétroaction (V_{LX}) de l'entrée du filtre passe bas (235) et configuré pour générer un premier signal de commande de réinitialisation (V_{RST}) et un seconde signal de commande de réinitialisation (V_{RST-}) pour commander la désactivation du premier commutateur (MP1) et du second commutateur (MP2) du convertisseur DC-DC (200) ;

dans lequel le premier circuit de limitation de courant (240a) et le circuit de commande de modulation de fréquence d'impulsion/modulation (246) sont configurés pour varier une limite de courant qui commande une intervalle et durée à laquelle la partie de commutation (220) de la partie de commutation DC-DC (200) commute pour permettre au convertisseur DC-DC de réaliser de larges modification dans une charge de courant de sortie (I_{out}) du convertisseur DC-DC (200) tout en fonctionnant dans le mode de fonctionnement discontinu.

2. Le circuit de commande de mode hystérétique de la revendication 1 dans lequel le circuit de limitation de

courant dynamique (240a) comporte :

- un premier commutateur de correspondance (P1) configuré avec des implantations d'impuretés et de géométrie correspondant au premier commutateur (MP1) du convertisseur DC-DC (200) et connecté à une source de tension de référence de terre (VSS) ; et
- une seconde source de courant de référence (I_4) connectée au premier commutateur de correspondance (P2) pour développer le premier signal de limitation de référence (242) pour commander la mise sous tension ou hors tension du premier commutateur (MP1).

3. Le circuit de commande de mode hystérétique de la revendication 1 comprenant en outre:

- un second circuit de limitation de courant dynamique (240b) configuré pour déterminer un second signal de limitation de référence (244) qui est utilisé pour commander l'activation du second commutateur (244) de la partie de commutation de puissance (220) du convertisseur DC-DC (200) pour transférer le courant (I_{OUT}) à la charge placée à la sortie du convertisseur DC-DC (200); et

dans lequel le circuit de commande de modulation de fréquence d'impulsion/modulation à largeur d'impulsion (245) est configuré pour recevoir le second signal de limitation de référence (244), configuré pour comparer une amplitude du second signal de limitation de référence (244) avec le signal de rétroaction (V_{LX}) de la partie de commutation de puissance (220) du convertisseur DC-DC (200), et configuré pour employer les premier et second signaux de limitation de référence (242, 244) pour générer les premières et secondes commandes de réinitialisation (V_{RST+} et V_{RST-}) pour activer le premier commutateur (MP1) et le second commutateur (MN1).

4. Le circuit de commande de mode hystérétique de la revendication 3 dans lequel le second circuit de limitation de courant dynamique (240b) comporte :

- un second commutateur de correspondance (N4) configure avec des implémentations d'impuretés et de géométrie correspondant au second commutateur (MN1) et connecté à la source de tension d'alimentation de puissance (VDD) ; et
- une seconde source de courant de référence (I_6) connectée au second commutateur de correspondance (N4) pour développer le second signal de limitation de référence (244) pour commander la mise sous tension et la mise hors tension du second commutateur (MN1).

5. Le circuit de commande de mode hystérétique de la revendication 3 dans lequel le second circuit de limitation de courant dynamique (240b) comporte :

- une seconde source de courant de référence (I_5) configurée pour fournir un second courant de référence maximal (I_{MAX-});
- un second miroir de courant de limitation (P3, P4) connecté de telle sorte qu'une branche de référence (P3) du second miroir de courant de limitation (P3, P4) reçoit le second courant de référence maximal (I_{MAX-}) et configuré de telle sorte qu'une branche de miroir (P4) du second miroir de courant de limitation (P3, P4) est connecté pour fournir le second signal de limitation de référence (244) pour une sortie du second circuit de limitation de courant (240b) pour déterminer un intervalle et une durée auxquels le second commutateur (MN1) de la partie de commutation de puissance (220) est commuté pour fournir du courant à la partie de filtrage (235) du convertisseur DC-DC (200);
- un comparateur (243) connecté pour recevoir un second signal de limitation de référence (V_{REF2}) et le signal de retroaction I (V_{FB}) de la sortie du convertisseur DC-DC (200) et configuré pour déterminer si le signal de rétroaction (V_{FB}) est plus grand ou inférieur au second signal de limitation de référence (V_{REF2}) pour générer un signal de sortie ; and
- un dispositif de commutation de comparaison (P2) connecté pour recevoir le signal de sortie du comparateur (243) qui est active ou désactivé pour dévier le courant de la branche de référence (P3) du second miroir de courant de limitation (P3, P4) et ainsi modifier le courant dans la branche de référence (P3) et ainsi la branche miroir (P4) du second miroir de courant de limitation (P3, P4) et ajuster ainsi le niveau de tension du second signal de limitation de référence (244).

6. Le circuit de commande de mode hystérétique de la revendication 1 dans lequel le premier circuit de limitation de courant dynamique (240a) comporte en outre une première charge (P1) connectée à la branche de miroir (N3) du premier miroir de courant de limitation (N2, N3) pour développer la première tension limite de référence (V_{LIM+}).

7. Le circuit de commande de mode hystérétique de la revendication 5 dans lequel le second circuit de limitation de courant dynamique (240b) comporte en outré une seconde charge (N4) connectée à la branche de miroir (P4) du second miroir de courant de limitation (P3, P4) pour développer la seconde tension limite de référence (V_{LIM-}).

8. Un convertisseur DC-DC comprenant un circuit de

commande de mode hystérétique selon l'une quelconque des revendications 1 à 7.

9. Un procédé pour fournir une commande de mode hystérétique par la supervision d'un intervalle et d'une durée de commutation d'une partie de commutation de puissance (220) d'un convertisseur DC-DC (200) pour permettre au convertisseur DC-DC (200) de gérer de larges changements dans un courant de charge de sortie (I_{OUT}) du convertisseur DC-DC (200) durant un mode de veille,
le convertisseur DC-DC comprenant une partie de filtrage passe-bas (235) qui supprime les harmoniques de fréquence élevées créées par la partie de commutation (220) pour générer un niveau de tension de sortie DC désiré à une charge placée à une sortie du convertisseur DC-DC (200), la partie de commutation (220) comprenant un premier commutateur (MP1) et un second commutateur (MP2),
le procédé étant **caractérisé en ce qu'**il comporte les étapes consistant à :

- déterminer (400) un premier signal de limitation (242) proportionnel à un premier courant limite (I_{MAX+}) s'écoulant dans le filtre passe-bas (235) du convertisseur DC-DC (200) dans lequel la détermination du premier signal de limitation (242) comporte les étapes consistant à :

  fixer un courant de référence maximal (I_{MAX+});
  déterminer une différence entre une tension de référence (V_{REF1}) du convertisseur DC-DC (200) et une tension de rétroaction (V_{FB}) du convertisseur DC-DC (200) comme étant une tension de différence ;
  convertir la tension de différence en un courant de différence ;
  soustraire le courant de différence au courant de référence maximal (I_{MAX+}) pour former un premier courant limite variable ;
  effectuer le miroir du premier courant limite variable; et
  convertir le premier courant limite variable en un premier signal limite (242),

- comparer (4100) un signal d'entrée (V_{LX}) du filtre passe-bas (235) avec le premier signal limite (242);
- réinitialiser (435) un premier circuit de bascule (227) pour désactiver un premier dispositif de commutation (MP1) pour empêcher l'écoulement d'un courant dans le filtre passe-bas (235), lorsque le signal d'entrée (V_{LX}) est plus grand qu'une premier signal limite (242); et
- permettre au courant de continuer à s'écouler dans le filtre passe-bas (235), lorsque le signal d'entrée (V_{LX}) est inférieur au premier signal limite (242) en ne réinitialisant pas le premier circuit de bascule (227) et en ne désactivant pas le premier dispositif de commutation (MP1).

10. Le procédé pour fournir une commande de mode hystérétique de la revendication 9 comprenant en outre les étapes consistant à :

- déterminer (405) un second signal limite (244) proportionnel à un second courant limite s'écoulant dans le filtre passe-bas (235) du convertisseur DC-DC (200) ;
- comparer (430) le signal d'entrée (V_{LX}) du filtre passe-bas (235) avec le second signal limite (244) ;
- réinitialiser (435) un second circuit de bascule (229) pour désactiver un second dispositif de commutation (MN1) pour empêcher un écoulement de courant du filtre passe-bas (235), lorsque le signal d'entrée (V_{LX}) est inférieur à un second signal limite (244); et
- permettre à un courant de continuer de s'écouler du filtre passe-bas (235), lorsque le signal d'entrée (V_{LX}) est supérieur au premier signal limite en ne réinitialisant pas le second circuit de bascule (229) et en ne désactivant pas le second dispositif de commutation (MN1).

11. Le procédé pour fournir une commande de mode hystérétique de la revendication 10 dans lequel la détermination du second signal limite comporte les étapes consistant à :

- fixer un courant de référence minimal (I_{MAX-});
- déterminer une différence entre une tension de référence (V_{REF}) du convertisseur DC-DC (200) et une tension de rétroaction (V_{FB}) du convertisseur DC-DC (200) en tant que tension de différence;
- convertir la tension de différence en un courant de différence;
- soustraire le courant de différence du courant de référence minimal (I_{MAX-}) afin de former un second courant limite variable ;
- effectuer un miroir du second courant limite variable; et
- convertir le second courant limite variable en second signal limite (244).

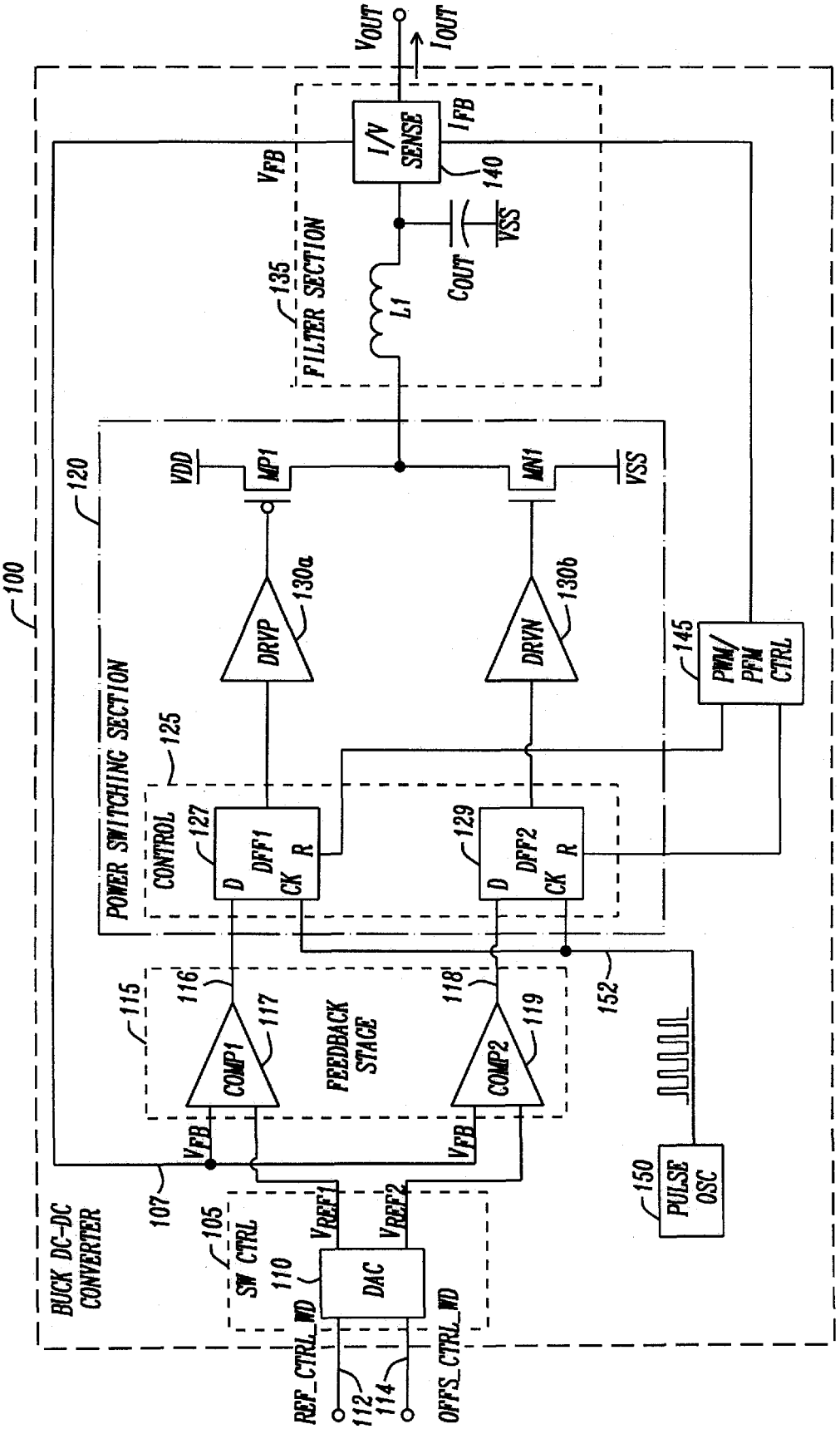
BUCK DC-DC CONVERTER
100
VOUT
IOUT
I/V SENSE
IFB
140
VFB
FILTER SECTION
135
L1
COUT
VSS
120
POWER SWITCHING SECTION
VDD
MP1
MN1
VSS
130a
DRVP
130b
DRVN
145
PWM/ PFM CTRL
125
CONTROL
127
DFF1
129
DFF2
D
CK
R
115
116
117
COMP1
FEEDBACK STAGE
118
119
COMP2
152
107
105
SW CTRL
110
DAC
VREF1
VREF2
150
PULSE OSC
REF_CTRL_WD
OFFS_CTRL_WD
112
114

FIG. 1

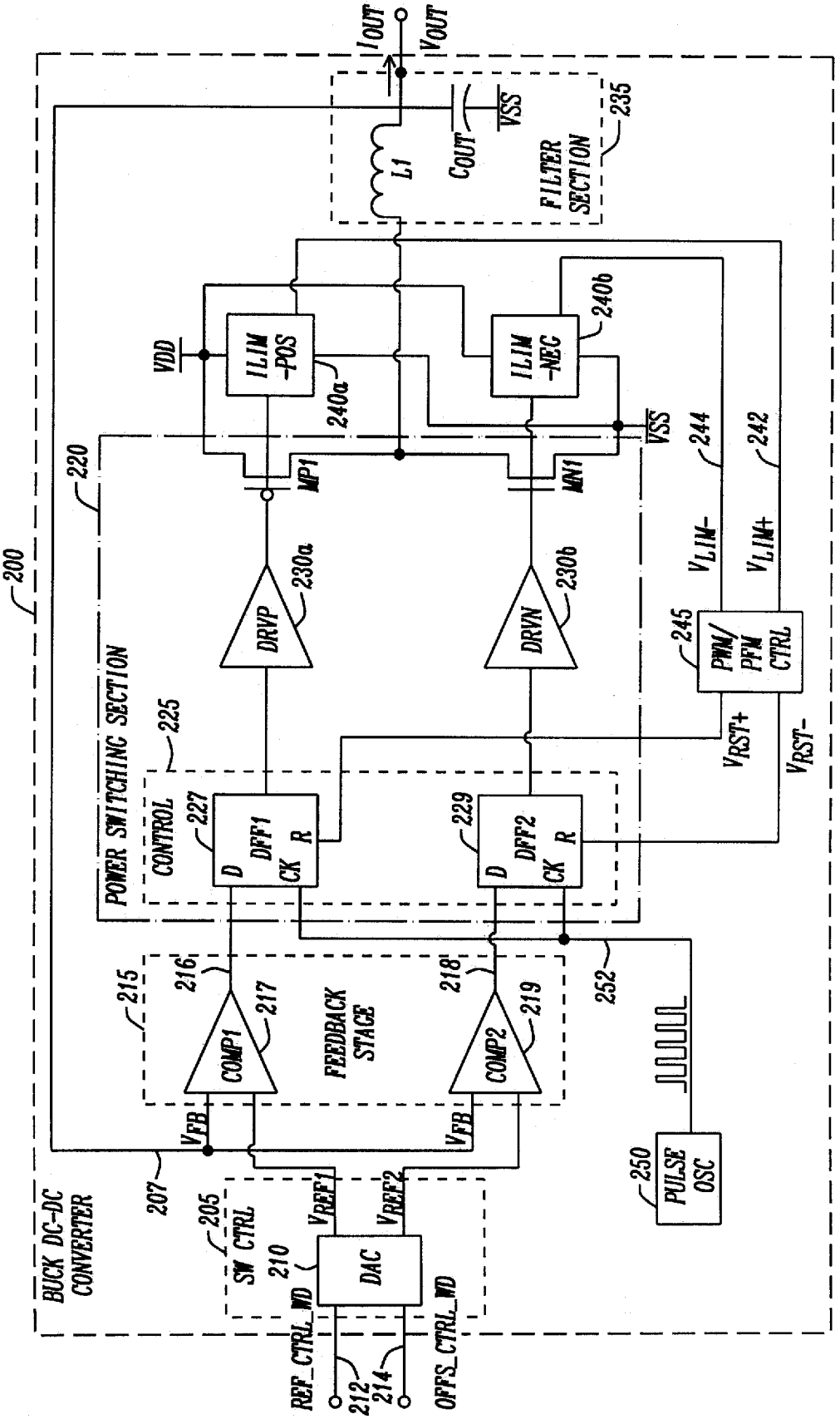
BUCK DC-DC CONVERTER
200
IOUT
VOUT
L1
COUT
VSS
FILTER SECTION
235
VDD
ILIM -POS
240a
ILIM -NEC
240b
VSS
220
MP1
MN1
244
242
VLIM-
VLIM+
230a
DRVP
230b
DRVN
245
PWM/ PFM CTRL
POWER SWITCHING SECTION
225
CONTROL
227
DFF1
D
CK
R
229
DFF2
215
216
217
COMP1
FEEDBACK STAGE
218
219
COMP2
252
VRST+
VRST-
VFB
VFB
207
205
SW CTRL
210
VREF1
VREF2
DAC
250
PULSE OSC
REF_CTRL_WD
OFFS_CTRL_WD
212
214

FIG. 2

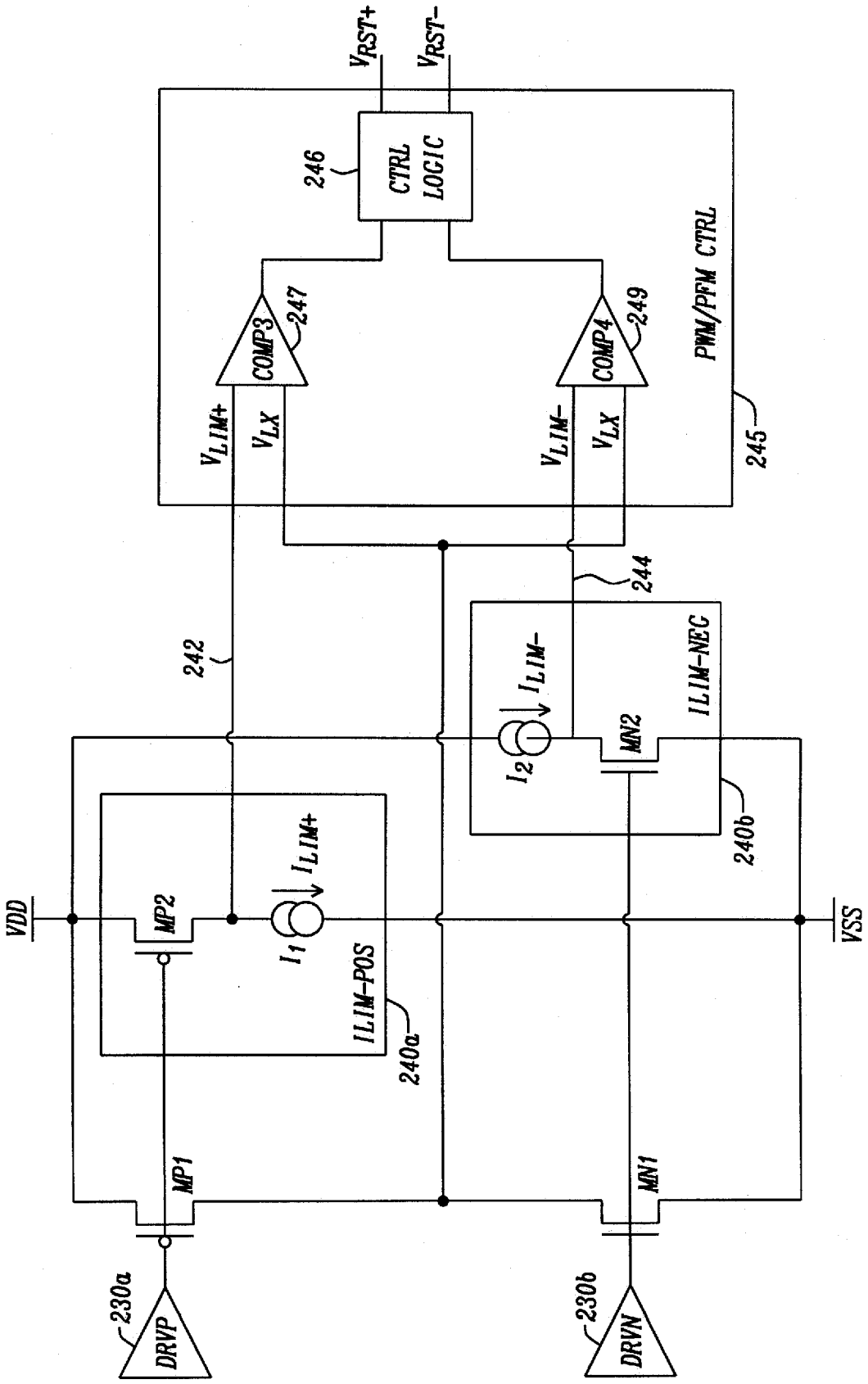
VRST+
VRST-
246
CTRL LOGIC
247
COMP3
249
COMP4
PWM/PFM CTRL
VLIM+
VLX
VLIM-
VLX
245
244
242
ILIM-
ILIM-NEC
I2
MN2
240b
VDD
MP2
ILIM+
I1
ILIM-POS
240a
VSS
MP1
MN1
230a
DRVP
230b
DRVN

FIG. 3

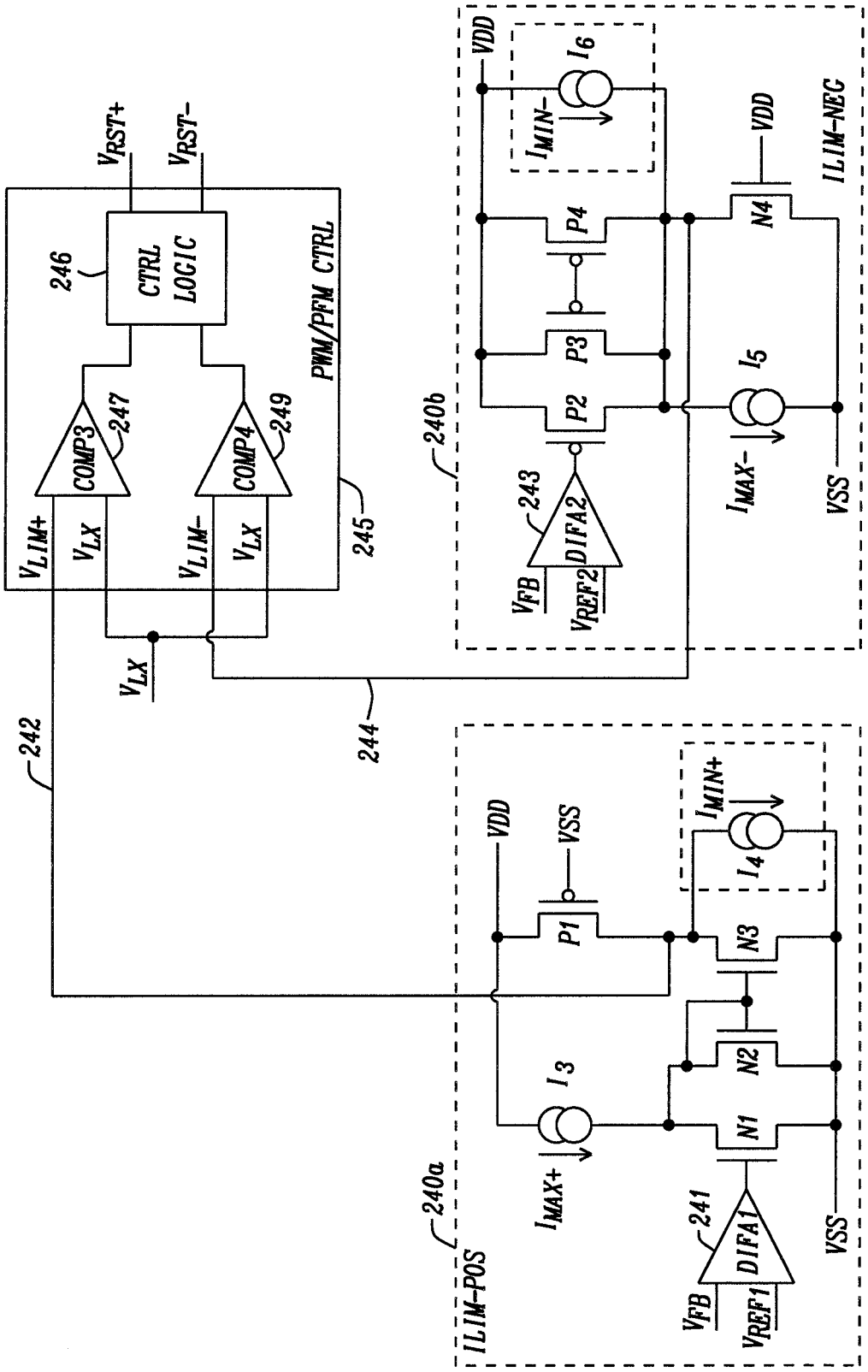
VRST+
VRST-
246
CTRL LOGIC
PWM/PFM CTRL
245
247
COMP3
249
COMP4
VLIM+
VLX
VLIM-
VLX
VLX
242
244
240b
VDD
I6
IMIN-
P4
P3
P2
243
DIFA2
VFB
VREF2
N4
I5
IMAX-
VSS
ILIM-NEC
240a
ILIM-POS
VDD
VSS
P1
IMIN+
I4
N3
N2
N1
I3
IMAX+
241
DIFA1
VFB
VREF1
VSS

FIG. 4

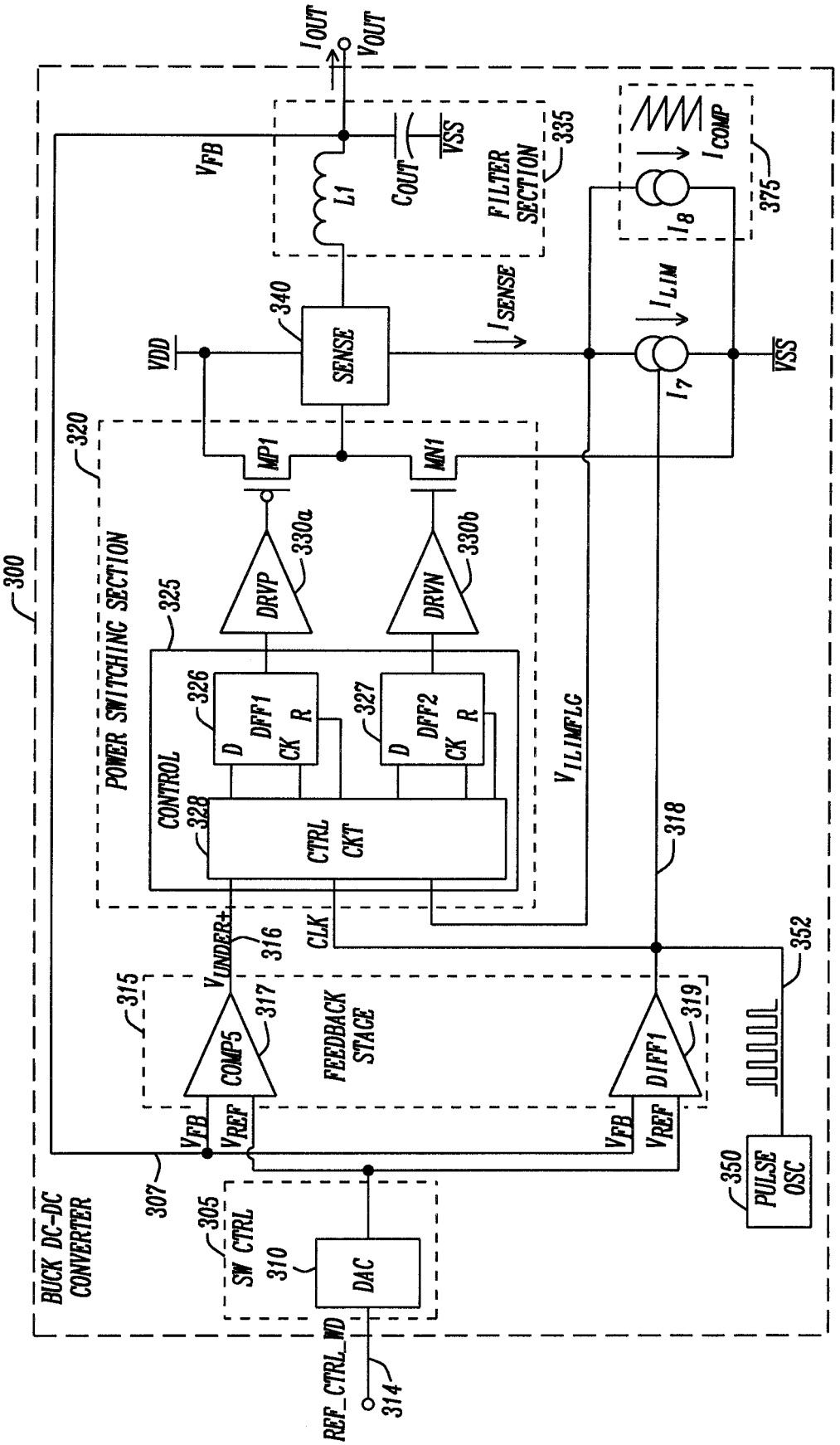
IOUT
VOUT
VFB
L1
COUT
VSS
FILTER SECTION
335
ICOMP
375
I8
ILIM
ISENSE
340
SENSE
VDD
I7
VSS
320
MP1
MN1
330a
DRVP
330b
DRVN
300
325
POWER SWITCHING SECTION
326
DFF1
D
CK
R
327
DFF2
CONTROL
328
CTRL CKT
VILIMFLG
318
VUNDER
316
CLK
352
315
317
COMP5
FEEDBACK STAGE
319
DIFF1
VFB
VREF
350
PULSE OSC
307
305
SW CTRL
310
DAC
BUCK DC-DC CONVERTER
REF_CTRL_WD
314

FIG. 5

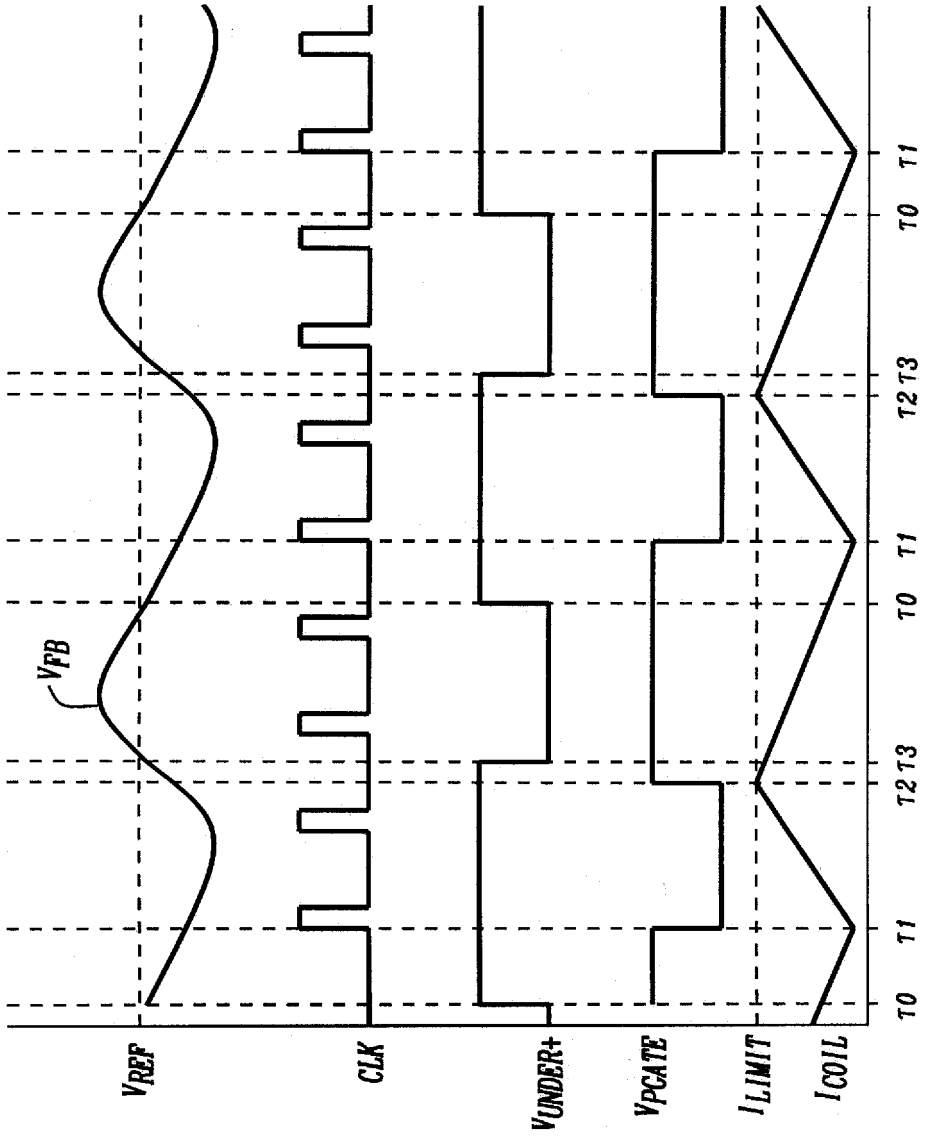
VREF
VFB
CLK
VUNDER+
VPGATE
ILIMIT
ICOIL
T0
T1
T2
T3
T0
T1
T2
T3
T0
T1

FIG. 6

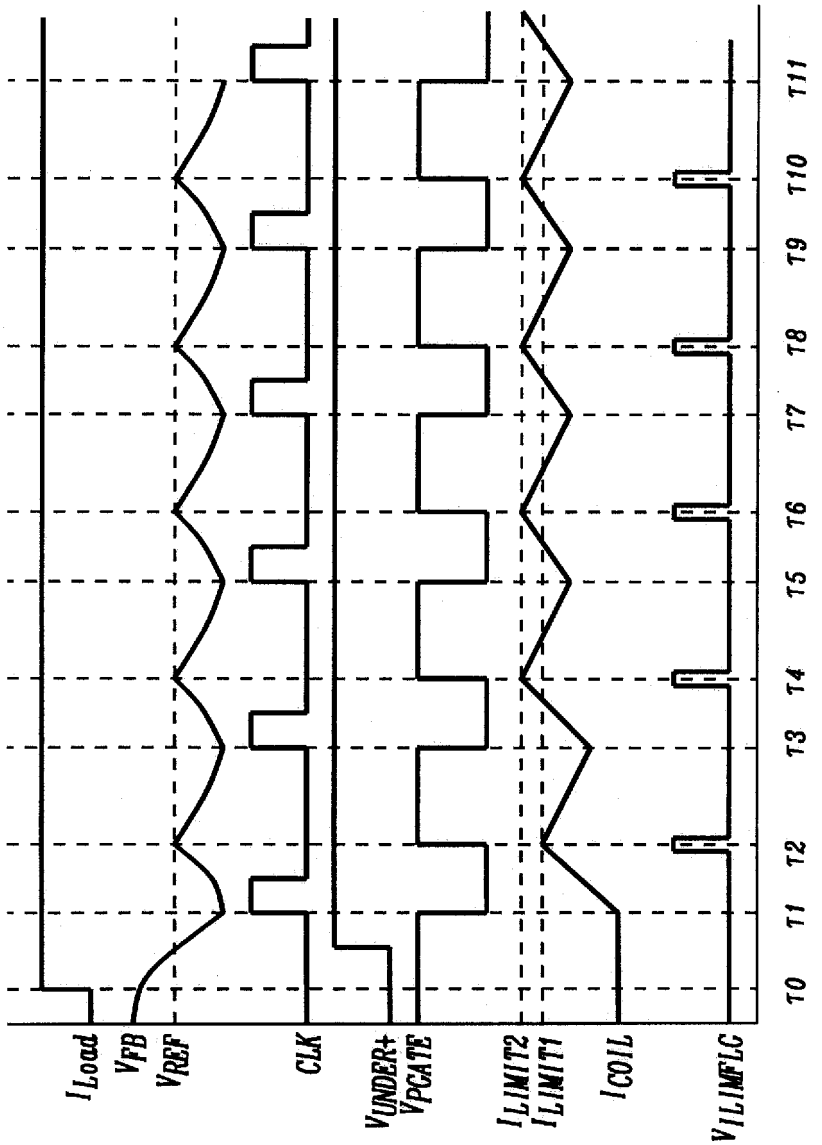
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
I_{Load}
V_{FB}
V_{REF}
CLK
V_{UNDER+}
V_{PGATE}
I_{LIMIT2}
I_{LIMIT1}
I_{COIL}
$V_{ILIMFLG}$

FIG. 7

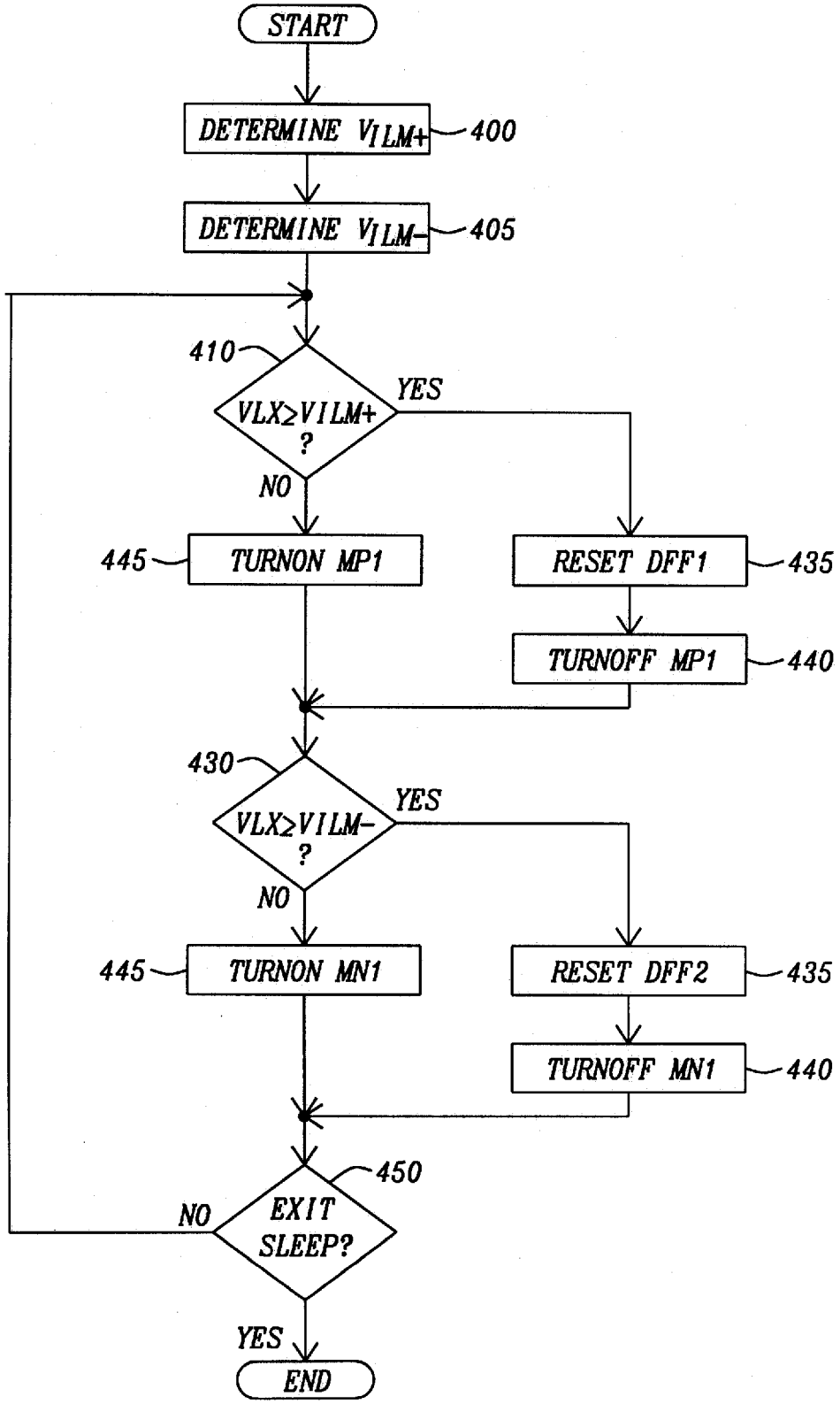
START
DETERMINE V_{ILM+}
400
DETERMINE V_{ILM-}
405
410
VLX≥VILM+ ?
YES
NO
445
TURNON MP1
RESET DFF1
435
TURNOFF MP1
440
430
VLX≥VILM- ?
YES
NO
445
TURNON MN1
RESET DFF2
435
TURNOFF MN1
440
450
NO
EXIT SLEEP?
YES
END

FIG. 8

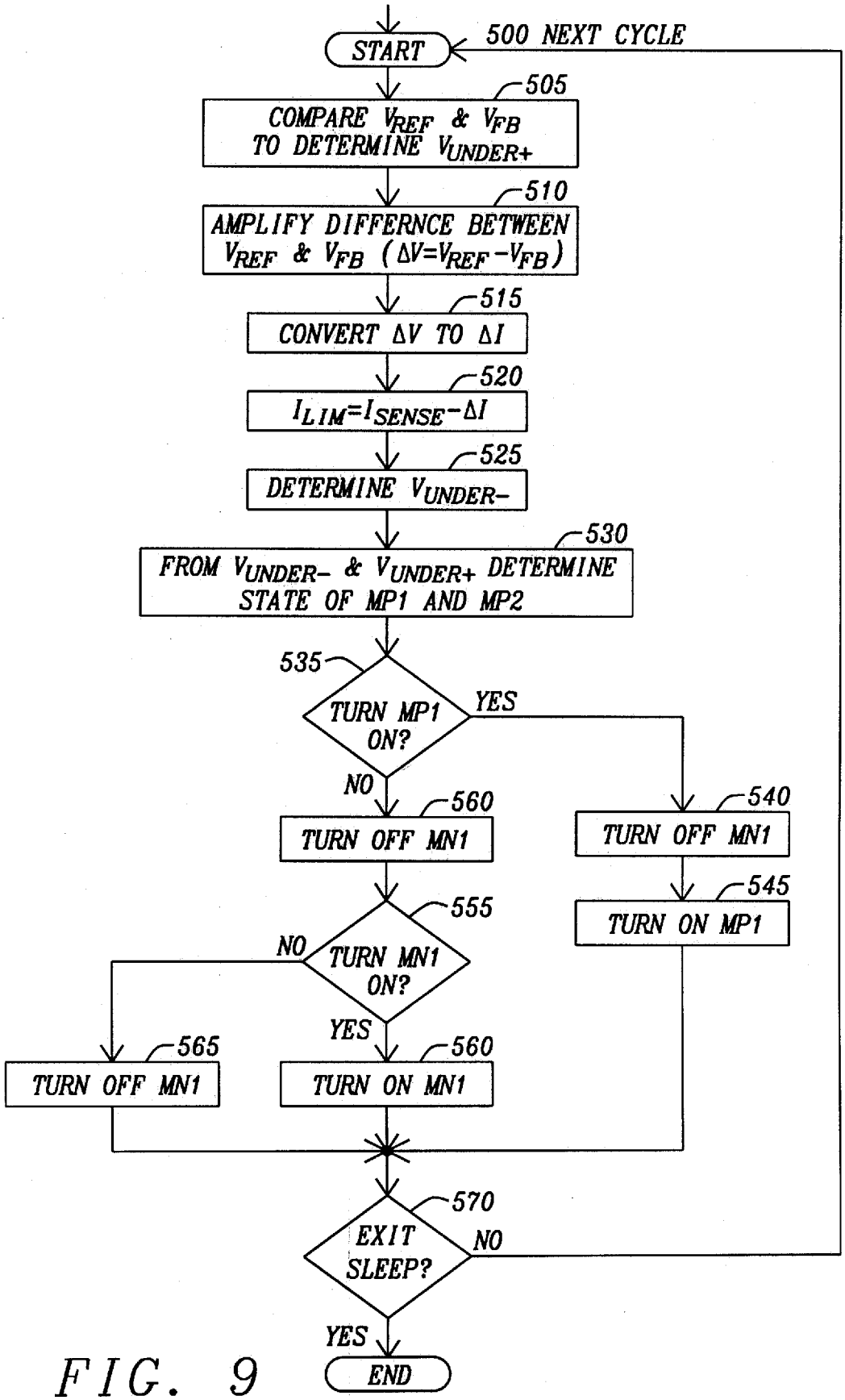
START
500 NEXT CYCLE
505
COMPARE V_{REF} & V_{FB} TO DETERMINE V_{UNDER+}
510
AMPLIFY DIFFERNCE BETWEEN V_{REF} & V_{FB} ($\Delta V=V_{REF}-V_{FB}$)
515
CONVERT ΔV TO ΔI
520
$I_{LIM}=I_{SENSE}-\Delta I$
525
DETERMINE V_{UNDER-}
530
FROM V_{UNDER-} & V_{UNDER+} DETERMINE STATE OF MP1 AND MP2
535
TURN MP1 ON?
YES
NO
560
TURN OFF MN1
540
TURN OFF MN1
545
TURN ON MP1
555
TURN MN1 ON?
NO
YES
565
TURN OFF MN1
560
TURN ON MN1
570
EXIT SLEEP?
NO
YES
END

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20090040791 A, Qahouq **[0008]**
- US 20050111149 A, Motomori **[0009]**