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(54) **VERTICAL MEANDER INDUCTOR FOR SMALL CORE VOLTAGE REGULATORS**

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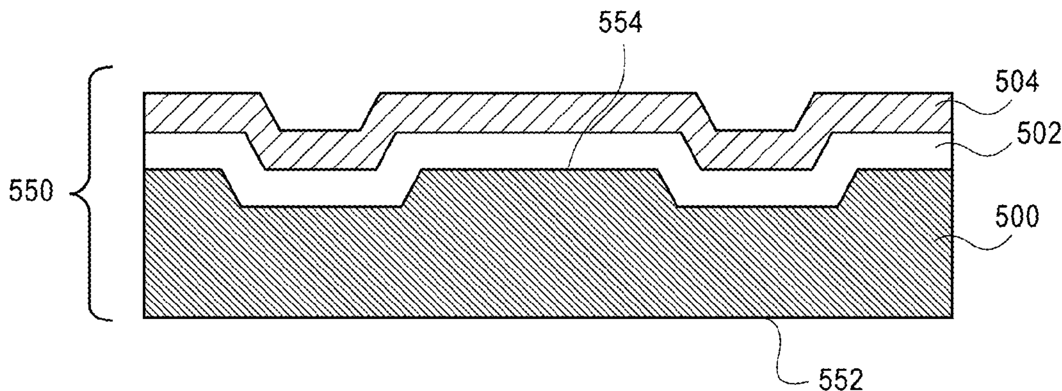
CPC ***H01L 28/10*** (2013.01); ***H01L 23/5227*** (2013.01); ***H01L 23/481*** (2013.01)

(57) **ABSTRACT**

Vertical meander inductors for small core voltage regulators and approaches to fabricating vertical meander inductors for small core voltage regulators are described. For example, a semiconductor die includes a substrate. An integrated circuit is disposed on an active surface of the substrate. An inductor is coupled to the integrated circuit. The inductor is disposed conformal with an insulating layer disposed on an essentially planar surface of the substrate. The insulating layer has an undulating topography.



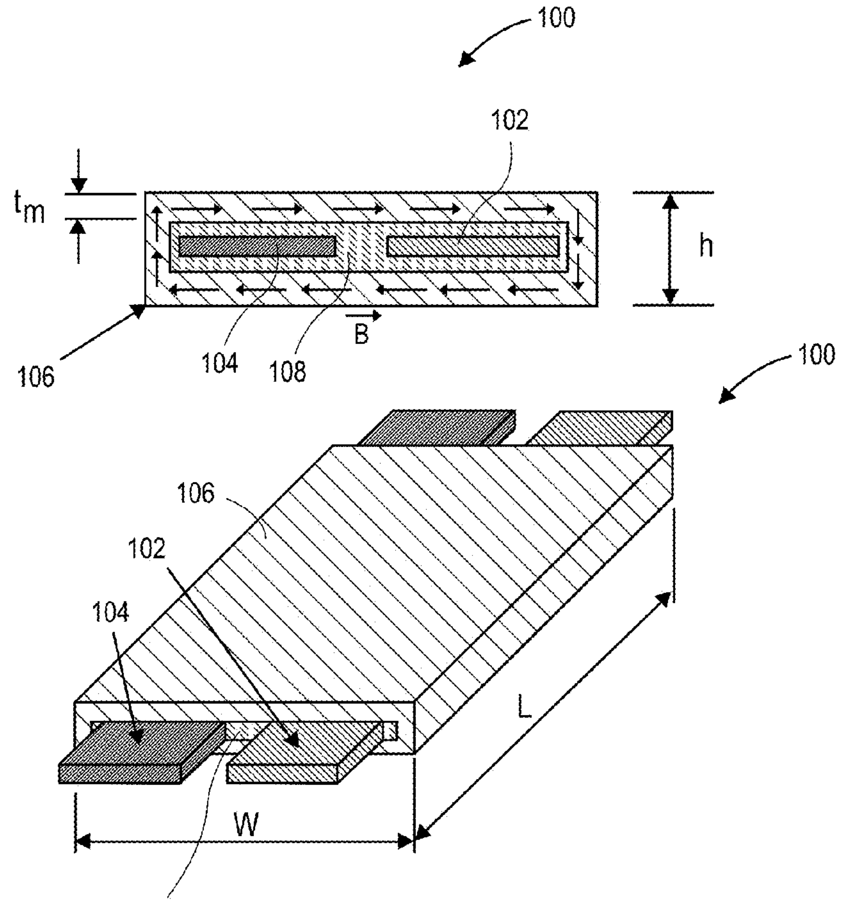


FIG. 1

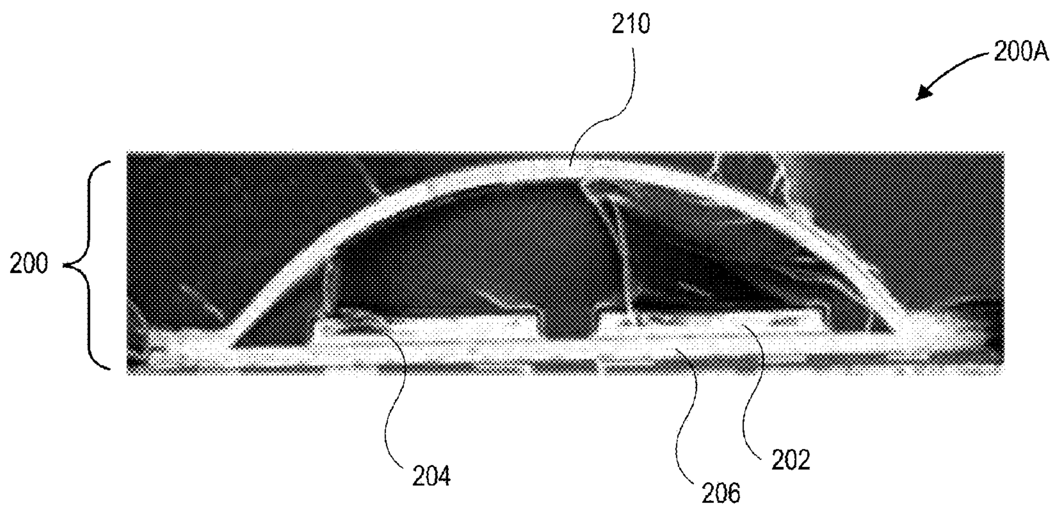


FIG. 2A

FIG. 2B

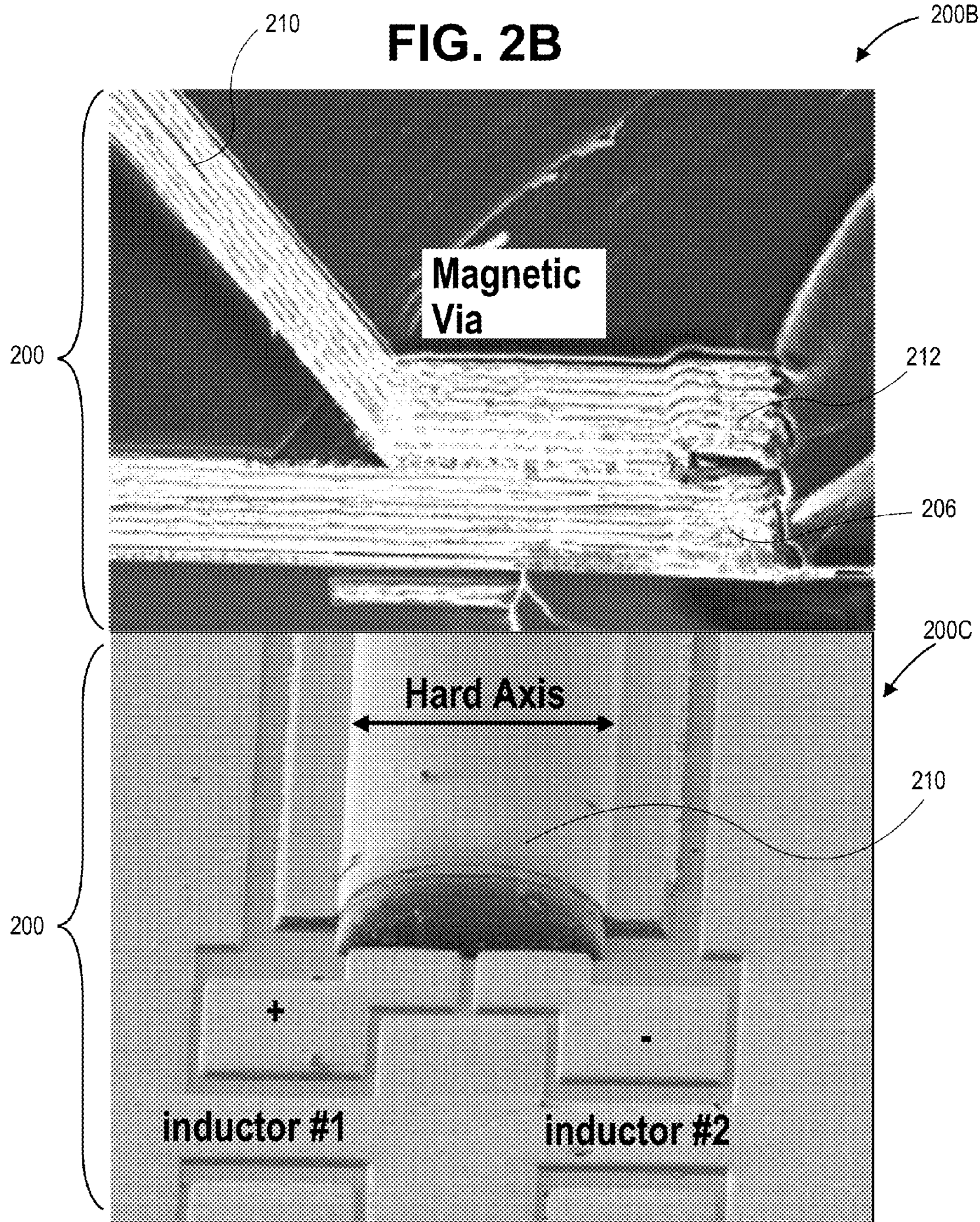


FIG. 2C

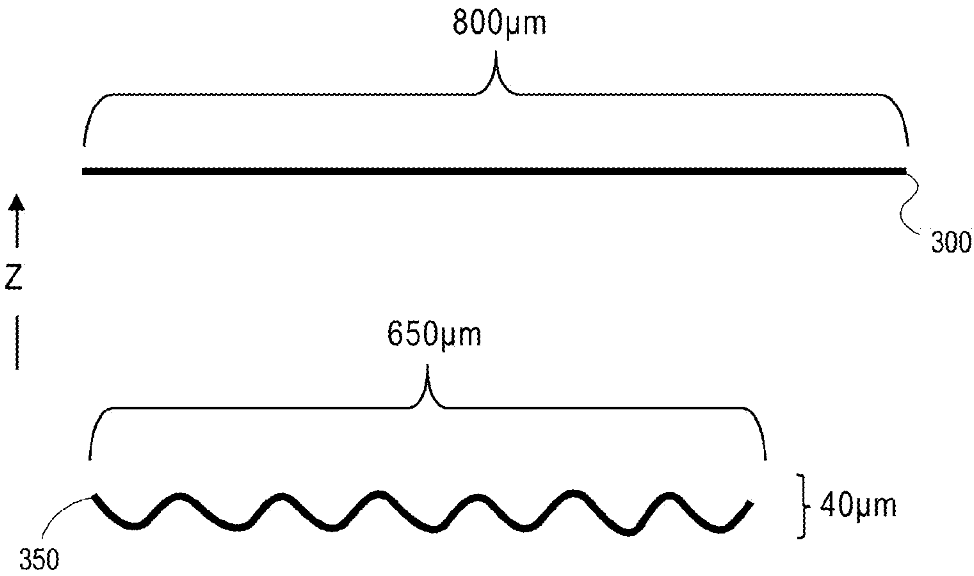


FIG. 3

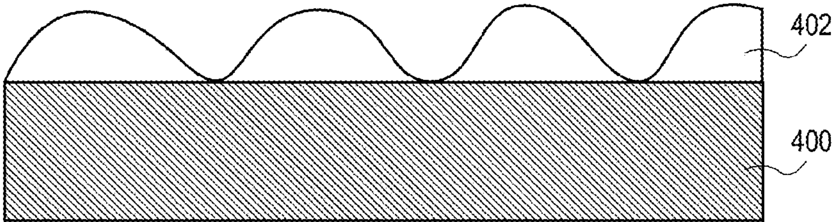


FIG. 4A

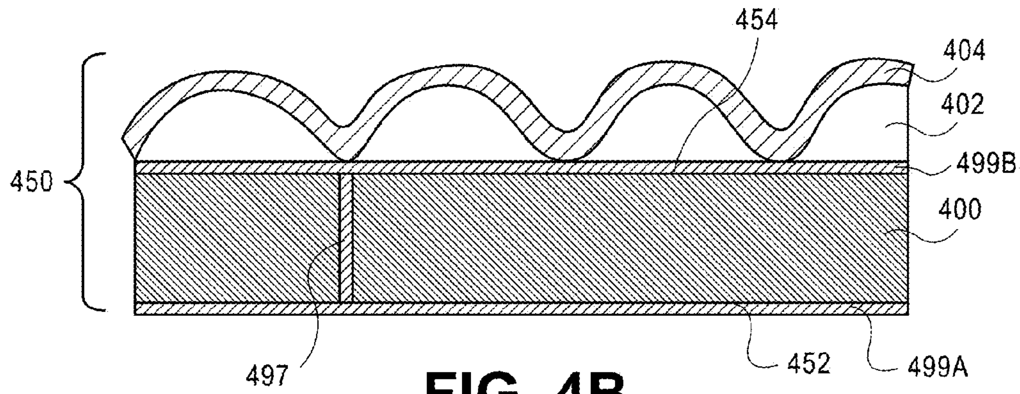


FIG. 4B

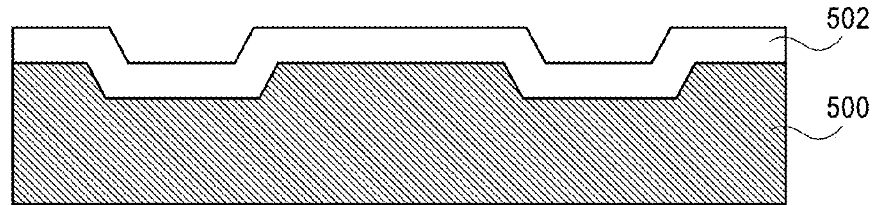


FIG. 5A

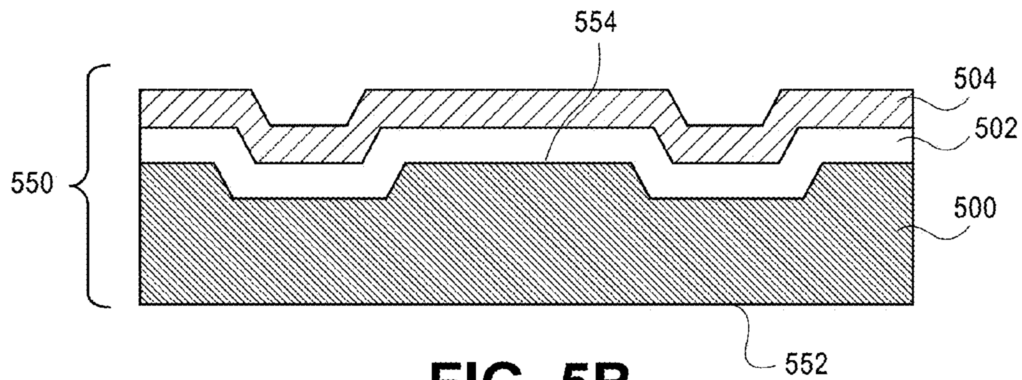


FIG. 5B

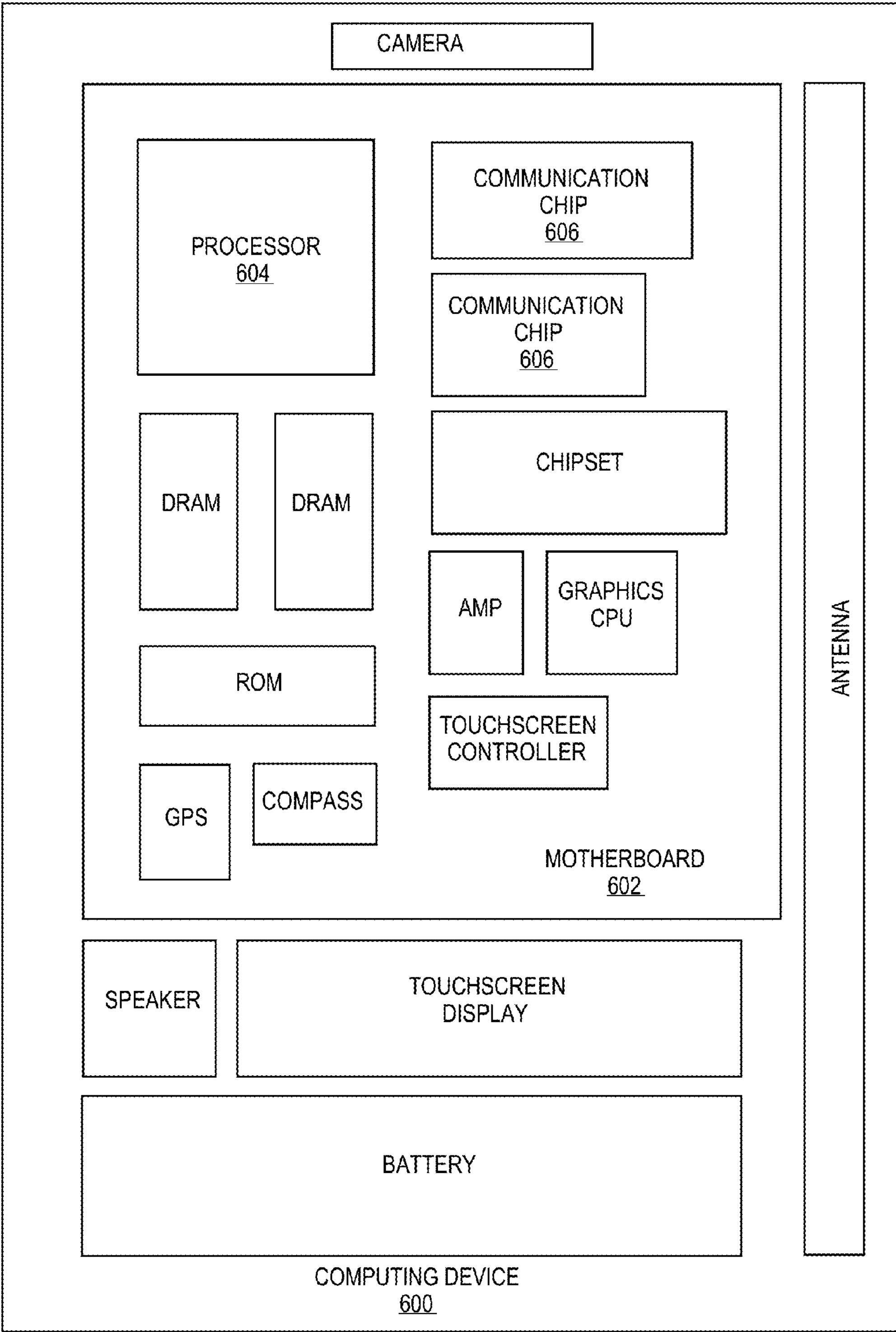


FIG. 6

VERTICAL MEANDER INDUCTOR FOR SMALL CORE VOLTAGE REGULATORS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 14/815,149, filed on Jul. 31, 2015, which is a continuation of U.S. patent application Ser. No. 14/319,429, filed on Jun. 30, 2014, now U.S. Pat. No. 9,129,844, issued on Sep. 8, 2015, which is a continuation of U.S. patent application Ser. No. 13/629,168, filed on Sep. 27, 2012, now U.S. Pat. No. 8,803,283, issued on Aug. 12, 2014, the entire contents of which are hereby incorporated by reference herein.

TECHNICAL FIELD

[0002] Embodiments of the invention are in the field of on-die inductors and, in particular, vertical meander inductors for small core voltage regulators.

BACKGROUND

[0003] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0004] On-die voltage regulation is designed to automatically maintain a constant voltage level for an associated semiconductor die. A voltage regulator may be a simple "feed-forward" design or may include negative feedback control loops. It may use an electromechanical mechanism, or electronic components. Depending on the design, it may be used to regulate one or more AC or DC voltages.

[0005] Electronic components, such as inductors, may be implemented on substrates such as an integrated circuit die or a printed circuit board (PCB). Such implementations involve placing patterns of material (e.g., as conductive material) on one or more substrate layers. This placement may be through lithographic techniques. Inductors used for RF applications in complementary metal oxide semiconductor (CMOS) technology are typically air-core spiral inductors. Various drawbacks are associated with these inductors. For instance, air-core spiral inductors typically require a substantial amount of space (area) on a substrate (e.g., an IC die). Moreover, such inductors require a high-resistivity substrate.

[0006] Thus, significant improvements are still needed in the area of on-die inductors for voltage regulation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** illustrates an angled view and corresponding cross-sectional view of a strip-line inductor for on-die voltage regulation, in accordance with an embodiment of the present invention.

[0008] FIG. **2**A is an SEM image of a cross-sectional view of a portion of an inductor structure, in accordance with an embodiment of the present invention.

[0009] FIG. **2**B is an SEM image of another cross-sectional view of a portion of an inductor structure, in accordance with an embodiment of the present invention.

[0010] FIG. **2**C is an SEM image of a top angled view of an inductor structure, in accordance with an embodiment of the present invention.

[0011] FIG. **3** illustrates scaling of a micro-strip or strip-line inductor from a total physical length of 800 microns to 650 microns by fabrication of an inductor that meanders vertically, in accordance with an embodiment of the present invention.

[0012] FIGS. **4**A and **4**B illustrate cross-sectional views of operations in, and the resulting structure of, a method of fabricating a meandering inductor, in accordance with an embodiment of the present invention.

[0013] FIGS. **5**A and **5**B illustrate cross-sectional views of operations in, and the resulting structure of, another method of fabricating a meandering inductor, in accordance with an embodiment of the present invention.

[0014] FIG. **6** illustrates a computing device in accordance with one implementation of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0015] Vertical meander inductors for small core voltage regulators and approaches to fabricating vertical meander inductors for small core voltage regulators are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0016] One or more embodiments described herein are targeted to the fabrication of an undulating inductor for, e.g., voltage regulation via an on-die voltage regulator. Conventional voltage regulators may occupy a substantial volume. For example, large ferrite inductors running at low frequency have provided previous solutions for voltage regulation by including the large ferrite inductors as mounted on a motherboard. By contrast, new approaches include incorporation of a voltage regulator closer in proximity to a microprocessor. Such approaches have associated benefits such as, but not limited to, reduced inductor volume, system factor gains from increased ferromagnetic, minimization of V_{droop}, a fast response time and small volume to enable granularity, and improved overall efficiency.

[0017] Accordingly, more recent approaches to voltage regulation for integrated circuits involves moving the voltage regulator on-die to allow improved voltage regulation performance. To this end, micro-strip (strip-line) inductors are being investigated. Strip-line inductors may offer the lowest DC resistance option (since they travel in a straight line) and inherent coupling which allows higher currents prior to magnetic saturation. As an example, FIG. **1** illustrates an angled view and corresponding cross-sectional view of a strip-line inductor for on-die voltage regulation, in accordance with an embodiment of the present invention. Referring to FIG. **1**, a strip line inductor **100** includes

conductive wires **102** and **104** (such as copper wires). In an example, wire **102** is an output winding for the inductor **100** and wire **104** is an input winding for inductor **100**. The wires **102** and **104** are housed in a magnetic material **106** by an insulating layer **108**. The inductor **100** has a height (h), a width (w), and a length (**1**). The magnetic material **106** has a thickness (t_m) and a magnetic field direction (B) shown by the arrows in the cross-sectional view of FIG. **1**. Thus, the inductor **100** is a magnetic core inductor as opposed to an air core inductor.

[0018] FIGS. **2**A-**2**C are scanning electron microscope (SEM) images of various views of a strip-line inductor, in accordance with an embodiment of the present invention. FIG. **2**A is an SEM image **200**A of a cross-sectional view of a portion of an inductor structure **200**. Referring to FIG. **2**A, first and second wires **202** and **204**, such as output winding and input winding wires are housed in a magnetic dome **210**, above a magnetic material **206**. FIG. **2**B is an SEM image **200**B of another cross-sectional view of a portion of the inductor structure **200**. Referring to FIG. **2**B, a magnetic via **212** couples the magnetic dome **210** with the underlying magnetic material **206** to surround the wires **202** and **204** (wires not shown in this view). FIG. **2**C is an SEM image of a top angled view of the inductor structure **200**. Referring to FIG. **2**C, more than one inductor may share the same magnetic material, such as inductors #**1** and #**2**, depicted in FIG. **2**C. Also seen is the top of magnetic dome **210**.

[0019] Since an inductor structure is a key component in modern voltage regulator circuits based on buck or hybrid circuit topologies, the inductor structure needs to occupy less volume or real estate yet without impacting performance of the inductor structure, as components scale. To maximize efficiency during average and peak current loads, it may be necessary that the voltage regulator inductor area be equal to or less than the microprocessor core area. As such, currently there is no known inductor-based voltage regulator solution that will fit inside an XY layout area of future core products based on scaling of today's dimensions. An issue is that as the core (and other components such as graphics) shrink they may require more turbo current density (even though the overall power is dropping). Current materials for planar straight inductors may only be useful for the next generation or so, otherwise new material or multi-level inductors may be needed if planarity of the inductors is maintained. Although material solutions may address some efficiency gains, there may not be sufficient inductance (L) achieved upon shrinking of the associated inductor. Nonetheless, voltage regulation scaling may be critical to future products such as system-on-chip (SoC) components.

[0020] Thus, in an embodiment, the above described micro-strip or strip-line inductors may be further scaled to accommodate scaling in the semiconductor industry. For example, in accordance with an embodiment of the present invention, the wire strips (typically flat and straight) are provided with a meandering or undulating third dimension to provide a longer strip relative to a give planar surface dimension. As such, inductance is increased per XY area by shrinking area when the inductor meanders vertically. Such an approach may be used regardless of eventual location of the inductors, including the possibility to process on a wafer or substrate backside. Such embodiments may enable scaling of modern devices in volume, which will likely be accommodated by scaling of the voltage regulator as well.

[0021] As an example, FIG. **3** illustrates scaling of a micro-strip or strip-line inductor from a total physical length of 800 microns to 650 microns by fabrication of an inductor that meanders vertically, in accordance with an embodiment of the present invention. Referring to FIG. **3**, a planar or flat strip-line inductor **300** is shown to run a length of approximately 800 microns. Beyond thickness, the planar or flat strip-line inductor **300** has no dimension vertically, e.g., in the z-direction. By contrast, a meandering (or undulating) strip-line inductor **350** has a length of 800 microns, but only occupies approximately 650 microns in actual length. The meandering or undulating inductor has a dimension vertically (e.g., beyond mere thickness in the z-direction). For example, the inductor structure **350** meanders or undulates in the vertical direction by approximately 40 microns. This approach effectively accomplishes a shrink of the actual length (e.g., 650 microns instead of 800 microns) needed to accommodate the inductor **350** without actually reducing the length (e.g., 800 microns) of the inductor **350**.

[0022] In a first example, FIGS. **4**A and **4**B illustrate cross-sectional views of operations in, and the resulting structure of, a method of fabricating a meandering inductor, in accordance with an embodiment of the present invention.

[0023] Referring to FIG. **4**A, an insulating layer **402**, such as a layer of silicon dioxide, is formed above a substrate **400**, such as a silicon substrate of a semiconductor die. The insulating layer **402** is formed to have an undulating topography. In an embodiment, the undulating topography of the insulating layer **402** is formed by reflow of a lithographically patterned insulating layer. In another embodiment, the undulating topography of the insulating layer **402** is formed by using grayscale lithography.

[0024] In the latter case, using grayscale lithography, three-dimensional microstructures are formed in a thick layer of photoresist. The fastest and easiest way to perform this is with a maskless laser lithography system, which uses an intensity modulated laser beam to write the structures directly into the resist. The resist is applied to the insulating layer of the substrate by spin- or spray-coating and can be several hundred microns thick, but most applications only require a thickness of less than 50 microns. Using data from an electronic design, the laser lithography system exposes the resist with a variable dose and the three-dimensional structures remain in the resist after the development process. The final result of this entire process depends on the electronic data, the laser writing and the development, and all of these operations can be independently tuned to produce the best result. The optical structures in the photoresist can subsequently be transferred into insulating layer on the substrate by reactive ion etching. In another embodiment, however, gray tone masks are used to pattern the insulating layer to have an undulating topography.

[0025] Referring to FIG. **4**B, a meandering inductor structure **404**, such as a meandering version of the strip-line inductors described in association with FIGS. **1** and **2**A-**2**C is formed above the insulating layer **402** having the undulating topography. Thus, in an embodiment, a semiconductor die **450** includes a substrate **400**. An integrated circuit **499**A or **499**B is disposed on an active surface (**452** or **454**, respectively) of the substrate **400**. The inductor **404** is coupled to the integrated circuit **499**A or **499**B. The inductor **404** is disposed conformal with the insulating layer **402**

disposed on an essentially planar surface of the substrate **400**. However, the insulating layer **402** has an undulating topography.

[0026] In one such embodiment, the insulating layer **402** having the undulating topography is disposed above the active surface of the substrate **400**, above the integrated circuit **499**B, in which case the integrated circuit is formed on active surface **454**. In another such embodiment, the insulating layer **402** having the undulating topography is disposed on a back surface of the substrate **400**, in which case the integrated circuit **499**A is formed on active surface **452**. In a specific embodiment of the latter arrangement, the inductor **404** is coupled to the integrated circuit **499**A on active surface **452** by one or more through silicon vias **497** disposed in substrate **400**.

[0027] In a second example, FIGS. **5**A and **5**B illustrate cross-sectional views of operations in, and the resulting structure of, another method of fabricating a meandering inductor, in accordance with an embodiment of the present invention.

[0028] Referring to FIG. **5**A, a substrate **500**, such as a silicon substrate of a semiconductor die, is formed to have an undulating topography. In an embodiment (as shown), an insulating layer **502**, such as a layer of silicon dioxide, is formed above the substrate **500**, conformal with the undulating topography. In one embodiment, the undulating topography is faceted, as depicted in FIG. **4**A. However, in other embodiments, the undulating topography of the substrate **500** is not faceted.

[0029] In an embodiment, the undulating topography of the substrate **500** is formed by etching a silicon substrate. In one such embodiment, isotropic etching is used which involves an etching process which progresses at the same speed in all directions. In another embodiment, long and narrow holes in a mask are used to produce v-shaped grooves in the silicon substrate. The surface of these grooves can be atomically smooth if the etch is carried out correctly, with dimensions and angles being extremely accurate. In another embodiment, anisotropic etching is used. For example, some single crystal materials, such as silicon, have different etching rates depending on the crystallographic orientation of the substrate. This is known as anisotropic etching and one of the most common examples is the etching of silicon in KOH (potassium hydroxide), where Si <111> planes etch approximately 100 times slower than other planes (crystallographic orientations). Therefore, etching a rectangular hole in a (100)-Si wafer results in a pyramid shaped etch pit with 54.7° walls, instead of a hole with curved sidewalls as with isotropic etching. In other embodiments, dry etching, such as vapor or plasma etching is used.

[0030] Referring to FIG. **5**B, a meandering inductor structure **504**, such as a meandering version of the strip-line inductors described in association with FIGS. **1** and **2**A-**2**C is formed above the surface of the substrate having the undulating topography. Thus, in an embodiment, a semiconductor die **550** includes a substrate **500**. An integrated circuit (not shown) is disposed on an active surface **552** of the substrate **500**. The inductor **504** is coupled to the integrated circuit. The inductor **504** is disposed conformal with a back surface **554** of the substrate **500**, the back surface having the undulating topography.

[0031] In one such embodiment, the inductor is disposed on an insulating layer **502** disposed on the back surface **554** of the substrate **500**. The insulating layer **502** is conformal with the back surface **554** having the undulating topography, as depicted in FIG. **5**B. In an embodiment, the inductor **504** is coupled to the integrated circuit on active surface **552** by one or more through silicon vias disposed in substrate **500** (not shown).

[0032] More generally, various embodiments described herein may be directed to techniques involving electronic components fabrication. For instance, in some embodiments, an apparatus may include a first magnetic layer, a second magnetic layer, and a conductive pattern. The conductive pattern is at a third layer between the first and second magnetic layers, and is composed of a metal such as copper or aluminum. Moreover, one or more magnetic vias connect the first and second magnetic layers. In some embodiments, the magnetic layers and vias may operate as ferromagnetic cores or shields, e.g., and may be composed of materials that can be formed to have ferromagnetism such as Co, Ni, or iron oxide. Furthermore, the magnetic layers and vias may be integrated on a chip (e.g., for on-die magnetics). Also, they may be implemented with CMOS technology or processes or, alternatively, on lower cost panel level processing. The apparatus may be included in inductors, transformers, transmission lines, RF circuits, wireless applications, voltage regulators and so forth.

[0033] As described herein, embodiments may advantageously provide inductors of comparable or better performance than current approaches, and that have a much smaller footprint. Furthermore, some embodiments enable avoidance of the blockage of space underneath inductors. Also, some embodiments may be implemented with low-resistivity substrates. This allows, for example, co-integration of digital and RF circuits using a high-speed CMOS process.

[0034] Moreover, embodiments may provide inductors that may be used at lower frequencies. Exemplary lower frequency applications may include switching amplifiers used as envelope generators for high-efficiency RF power amplifiers. Such applications may involve modulation schemes requiring class-A linear RF power amplifiers, which have a theoretical efficiency of less than 12.5%. Other applications include resonant gate drivers for high-power DC-DC converters, low to mid-power on-die DC-DC converters. Furthermore, inductors described herein may be an integral collateral for system-on-chip (SoC) designers.

[0035] FIG. **6** illustrates a computing device **600** in accordance with one implementation of the invention. The computing device **600** houses a board **602**. The board **602** may include a number of components, including but not limited to a processor **604** and at least one communication chip **606**. The processor **604** is physically and electrically coupled to the board **602**. In some implementations the at least one communication chip **606** is also physically and electrically coupled to the board **602**. In further implementations, the communication chip **606** is part of the processor **604**.

[0036] Depending on its applications, computing device **600** may include other components that may or may not be physically and electrically coupled to the board **602**. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerom-

eter, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0037] The communication chip **606** enables wireless communications for the transfer of data to and from the computing device **600**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **606** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **600** may include a plurality of communication chips **606**. For instance, a first communication chip **606** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **606** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0038] The processor **604** of the computing device **600** includes an integrated circuit die packaged within the processor **604**. In some implementations of the invention, the integrated circuit die of the processor includes one or more passive devices, such as on-die inductors built in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0039] The communication chip **606** also includes an integrated circuit die packaged within the communication chip **606**. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more passive devices, such as on-die inductors built in accordance with implementations of the invention.

[0040] In further implementations, another component housed within the computing device **600** may contain an integrated circuit die that includes one or more passive devices, such as on-die inductors built in accordance with implementations of the invention.

[0041] In various implementations, the computing device **600** may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device **600** may be any other electronic device that processes data.

[0042] The specific implementations described above are not meant to be limiting to the spirit and scope of embodiments of the present invention. For example, in another embodiment, a voltage regulator (VR) circuit is included as a separate chip—often referred to as a power management integrated circuit (PMIC) chip. Another embodiments includes using of surface mount meandering inductors on a package, yet using transistors of an associated IC for switches. Another embodiment includes surface mount of an entire VR on a package or embedded in a package.

[0043] Thus, embodiments of the present invention include vertical meander inductors for small core voltage regulators and approaches to fabricating vertical meander inductors for small core voltage regulators.

[0044] In an embodiment, a semiconductor die includes a substrate. An integrated circuit is disposed on an active surface of the substrate. An inductor is coupled to the integrated circuit. The inductor is disposed conformal with an insulating layer disposed on an essentially planar surface of the substrate. The insulating layer has an undulating topography.

[0045] In one embodiment, the insulating layer having the undulating topography is disposed on a back surface of the substrate.

[0046] In one embodiment, the inductor is coupled to the integrated circuit by one or more through silicon vias (TSVs) disposed in the substrate.

[0047] In one embodiment, the insulating layer having the undulating topography is disposed above the active surface of the substrate, above the integrated circuit.

[0048] In one embodiment, the inductor is a magnetic core inductor.

[0049] In one embodiment, the inductor is included in an on-die voltage regulator.

[0050] In an embodiment, a semiconductor die includes a substrate. An integrated circuit is disposed on an active surface of the substrate. An inductor is coupled to the integrated circuit. The inductor is disposed conformal with a back surface of the substrate, the back surface having an undulating topography.

[0051] In one embodiment, the inductor is disposed on an insulating layer disposed on the back surface of the substrate. The insulating layer is conformal with the back surface having the undulating topography.

[0052] In one embodiment, the inductor is coupled to the integrated circuit by one or more through silicon vias (TSVs) disposed in the substrate.

[0053] In one embodiment, the undulating topography of the back surface is faceted.

[0054] In one embodiment, the undulating topography of the back surface is non-faceted.

[0055] In one embodiment, the inductor is a magnetic core inductor.

[0056] In one embodiment, the inductor is included in an on-die voltage regulator.

[0057] In an embodiment, a method of fabricating a semiconductor structure includes forming an integrated circuit on an active surface of a substrate. The method also includes forming an insulating layer on an essentially planar surface of the substrate, the insulating layer having an undulating topography. The method also includes forming an inductor coupled to the integrated circuit, the inductor formed conformal with the insulating layer.

[0058] In one embodiment, forming the insulating layer having the undulating topography includes reflowing a lithographically patterned insulating layer.

[0059] In one embodiment, forming the insulating layer having the undulating topography includes using grayscale lithography.

[0060] In one embodiment, forming the insulating layer having the undulating topography includes forming the insulating layer on a back surface of the substrate.

[0061] In one embodiment, forming the inductor coupled to the integrated circuit includes coupling the inductor to the integrated circuit by one or more through silicon vias (TSVs) formed in the substrate.

[0062] In one embodiment, forming the insulating layer having the undulating topography includes forming the insulating layer above the active surface of the substrate, above the integrated circuit.

[0063] In one embodiment, forming the inductor includes forming a magnetic core inductor.

[0064] In one embodiment, forming the inductor includes forming an on-die voltage regulator.

[0065] In an embodiment, a method of fabricating a semiconductor structure includes forming an integrated circuit on an active surface of a substrate. The method also includes forming an undulating topography on a back surface of the substrate. The method also includes forming an inductor coupled to the integrated circuit, the inductor formed conformal with the back surface of the substrate.

[0066] In one embodiment, forming the undulating topography on the back surface of the substrate includes using an isotropic etch of a silicon substrate.

[0067] In one embodiment, forming the undulating topography on the back surface of the substrate includes using an isotropic etch of a silicon substrate.

[0068] In one embodiment, the method further includes, prior to forming the inductor, forming an insulating layer conformal with the back surface having the undulating topography. The inductor is formed on the insulating layer formed on the back surface of the substrate.

[0069] In one embodiment, forming the inductor coupled to the integrated circuit includes coupling the inductor to the integrated circuit by one or more through silicon vias (TSVs) formed in the substrate.

[0070] In one embodiment, forming the undulating topography includes forming a faceted topography.

[0071] In one embodiment, forming the undulating topography includes forming a non-faceted topography.

[0072] In one embodiment, forming the inductor includes forming a magnetic core inductor.

[0073] In one embodiment, forming the inductor includes forming an on-die voltage regulator.

What is claimed is:

1. A semiconductor die, comprising:

a substrate having an active front surface and a back surface;

an integrated circuit disposed on the active front surface of the substrate;

an inductor disposed above the back surface of the substrate, wherein both an uppermost surface and a lowermost surface of the inductor have an undulating topography; and

one or more conductive vias disposed through the substrate, the one or more conductive vias electrically coupling the inductor to the integrated circuit.

2. The semiconductor die of claim **1**, wherein the inductor is a strip-line inductor, and the semiconductor die further comprises a magnetic dome over the strip-line inductor.

3. The semiconductor die of claim **1**, wherein the inductor is a magnetic core inductor.

4. The semiconductor die of claim **1**, wherein the inductor is included in an on-die voltage regulator.

5. The semiconductor die of claim **1**, wherein the undulating topography of the uppermost surface and a lowermost surface of the inductor is based on a faceted topography.

6. The semiconductor die of claim **1**, wherein the undulating topography of the uppermost surface and the lowermost surface of the inductor is based on a non-faceted topography.

7. The semiconductor die of claim **1**, wherein the substrate is a silicon substrate, and wherein the one or more conductive vias are one or more through silicon vias (TSVs).

8. A semiconductor die, comprising:

a substrate;

an integrated circuit disposed on an active front surface of the substrate;

an inductor disposed conformal with an insulating layer disposed on, but not through, an essentially planar back surface of the substrate, wherein an uppermost surface of the insulating layer has a non-planar topography, and wherein both an uppermost surface and a lowermost surface of the inductor have the non-planar topography; and

one or more conductive vias disposed through the substrate, the one or more conductive vias electrically coupling the inductor to the integrated circuit.

9. The semiconductor die of claim **8**, wherein the inductor is a magnetic core inductor.

10. The semiconductor die of claim **8**, wherein the inductor is included in an on-die voltage regulator.

11. The semiconductor die of claim **8**, wherein the non-planar topography of the uppermost surface of the insulating layer, and the non-planar topography of the uppermost surface and the lowermost surface of the inductor is based on a non-faceted topography.

12. The semiconductor die of claim **8**, wherein the substrate is a silicon substrate, and wherein the one or more conductive vias are one or more through silicon vias (TSVs).

13. The semiconductor die of claim **8**, wherein the insulating layer comprises a layer of silicon dioxide.

14. A semiconductor die, comprising:

a substrate;

an integrated circuit disposed on an active front surface of the substrate;

an inductor coupled to the integrated circuit, the inductor disposed on and conformal with an insulating layer disposed on and conformal with, but not through, a back surface of the substrate, wherein the back surface of the substrate has a non-planar topography, wherein both an uppermost surface and a lowermost surface of the insulating layer have the non-planar topography, and wherein both an uppermost surface and a lowermost surface of the inductor have the non-planar topography; and

one or more conductive vias disposed through the substrate, the one or more conductive vias electrically coupling the inductor to the integrated circuit.

15. The semiconductor die of claim **14**, wherein the non-planar topography of the back surface, the non-planar topography of the uppermost surface and the lowermost surface of the insulating layer, and the non-planar topography of the uppermost surface and the lowermost surface of the inductor is based on a faceted topography.

16. The semiconductor die of claim **14**, wherein the non-planar topography of the back surface, the non-planar topography of the uppermost surface and the lowermost surface of the insulating layer, and the non-planar topography of the uppermost surface and the lowermost surface of the inductor is based on a non-faceted topography.

17. The semiconductor die of claim **14**, wherein the inductor is a magnetic core inductor.

18. The semiconductor die of claim **14**, wherein the inductor is included in an on-die voltage regulator.

19. The semiconductor die of claim **14**, wherein the substrate is a silicon substrate, and wherein the one or more conductive vias are one or more through silicon vias (TSVs).

20. The semiconductor die of claim **14**, wherein the insulating layer comprises a layer of silicon dioxide.

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