United States Patent

[11] 3,573,441

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[54] **AUTOMATIC TRAIN LENGTH COMPUTER**
4 Claims, 9 Drawing Figs.

[52] **U.S. Cl.** **235/150.24,** 235/151.3, 235/151.32, 246/1, 246/249, 324/68
[51] **Int. Cl.** **G06f 15/48,** G06g 7/78
[50] **Field of Search** ..... - 235/150.20-150.24, 151.3, 151.32; 246/1, 182, 249; 324/70 (B), 68 (C)

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ABSTRACT: An apparatus for measuring the length of a moving railroad train is provided. The apparatus includes two sensors mounted on a rail of the track in relatively close proximity to one another and two counting circuits, each of which is operatively connected to the sensors and counts the pulses from an associated fixed frequency pulse generator. The first counting circuit is enabled when a wheel passes the first sensor and disabled when that wheel passes the second sensor. The second counting circuit counts the pulses during the time interval between successive wheels passing one of the sensors. An arithmetic unit is also provided which computes the quotient of the counts of the first and second counting circuits. The quotient is directly proportional to the distance between the successive wheels. The arithmetic unit also sums the quotient for each set of successive wheels and this sum is directly proportional to the total length of the train.

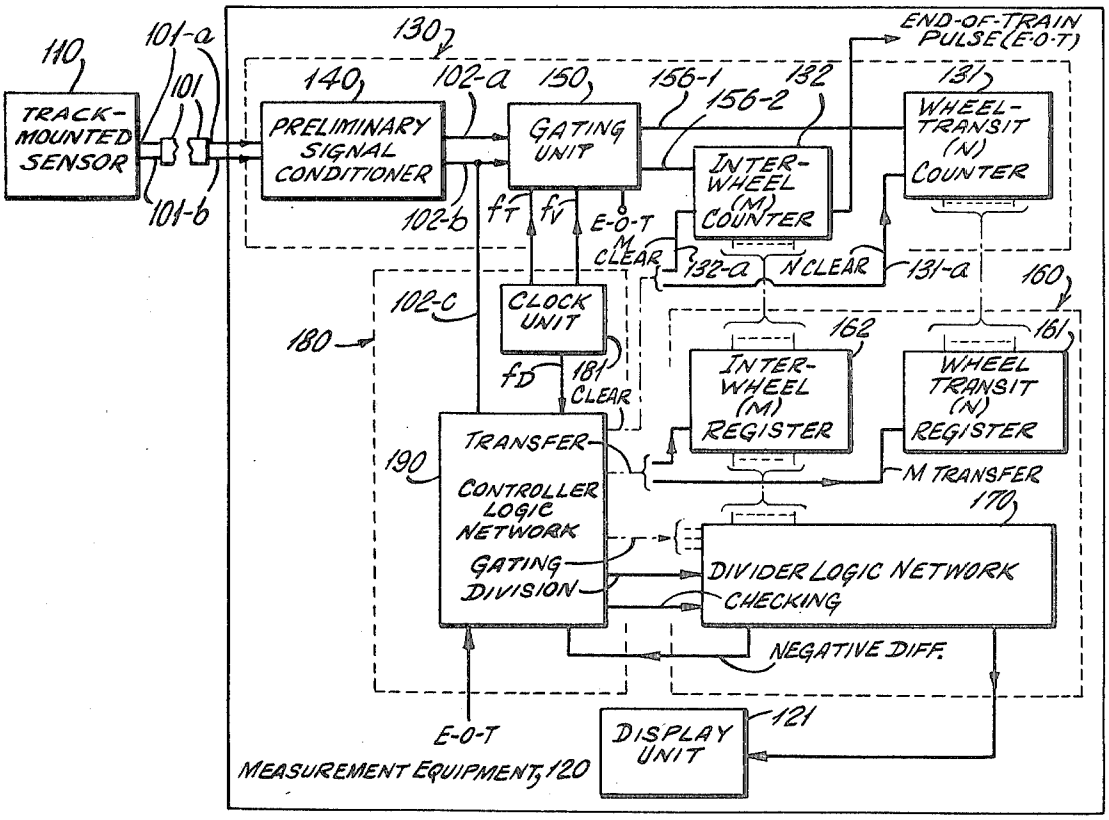

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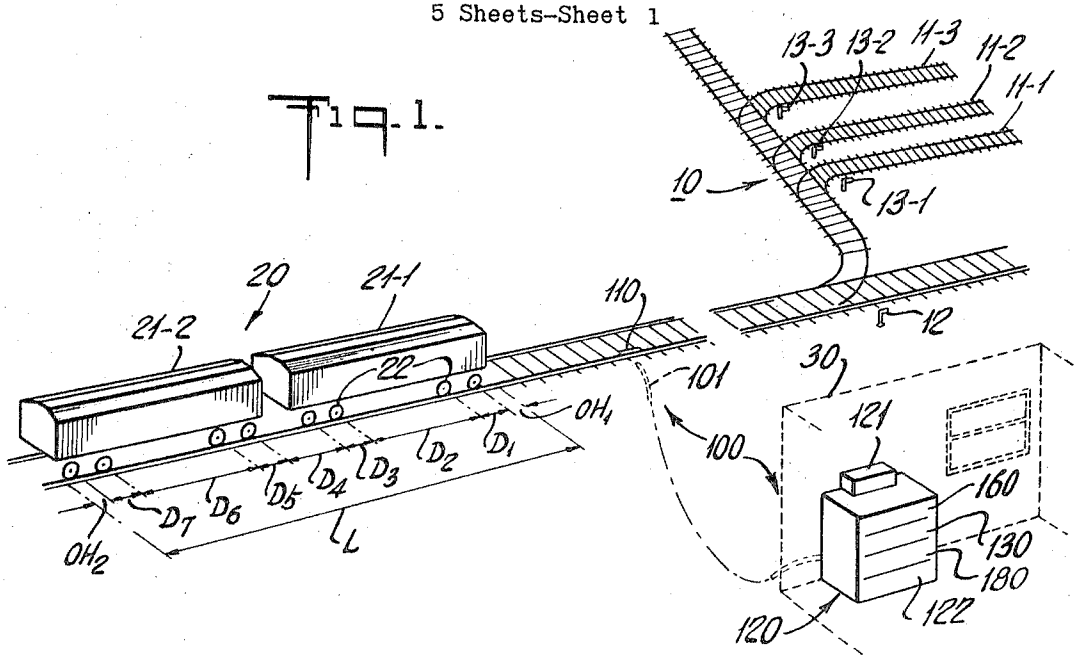
Fig. 1.



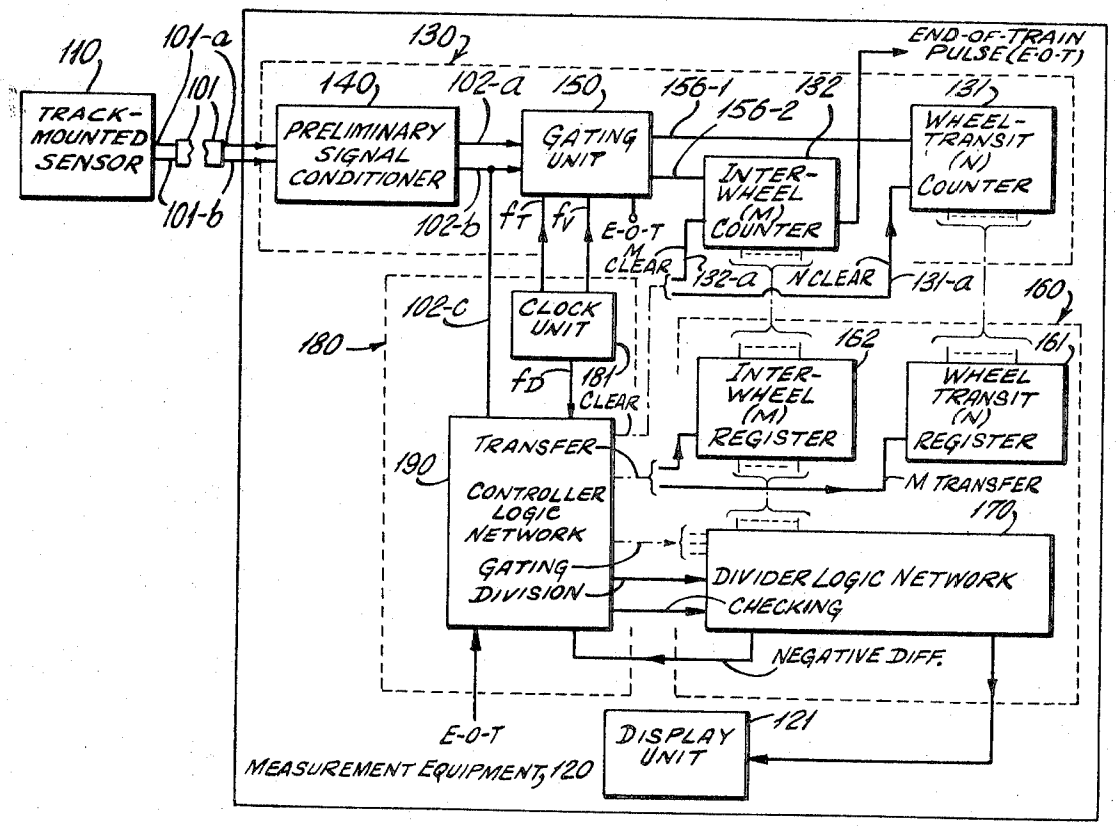


Fig. 2.

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Fig. 3A.

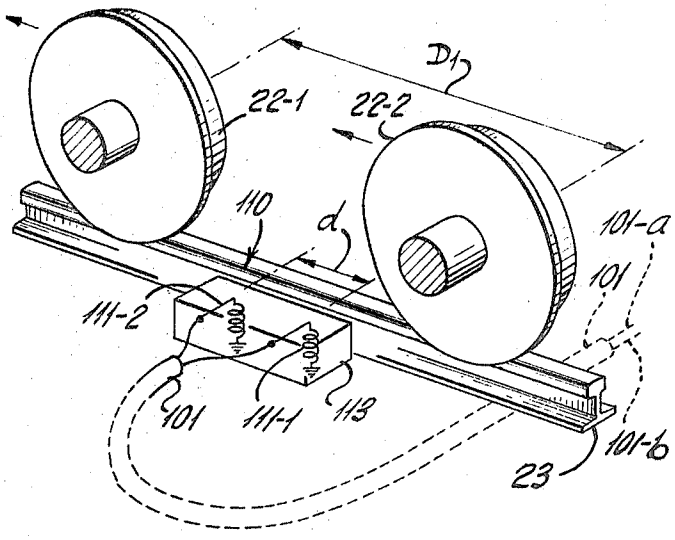

Fig. 3B.

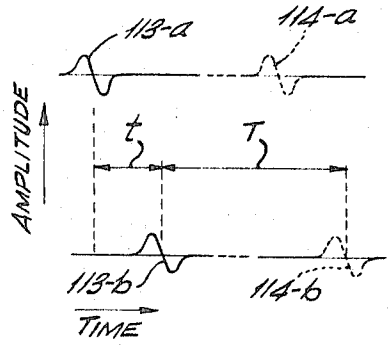

Fig. 4A.

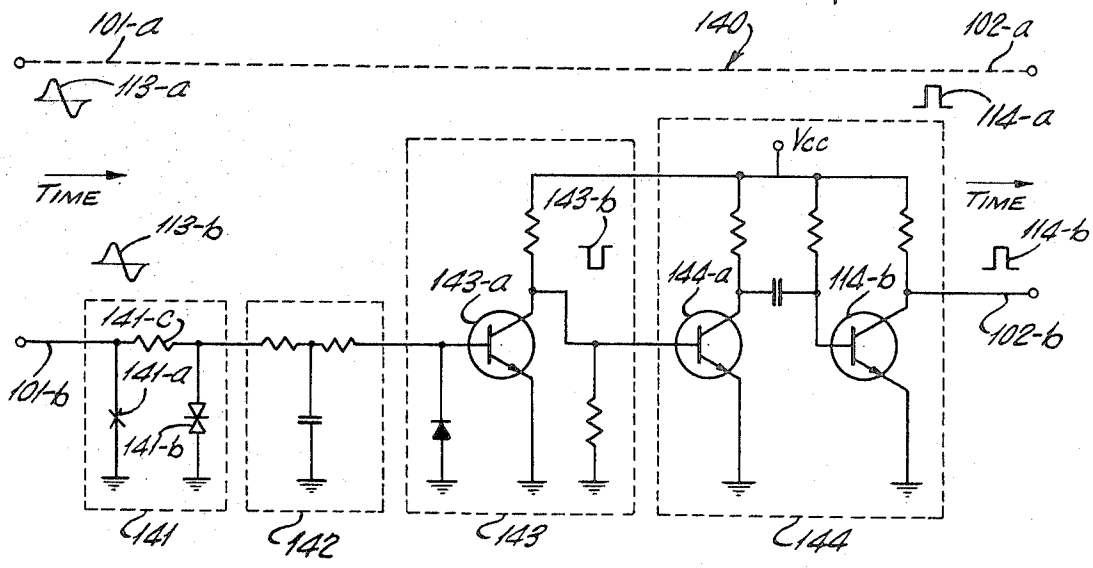

Fig. 4B.

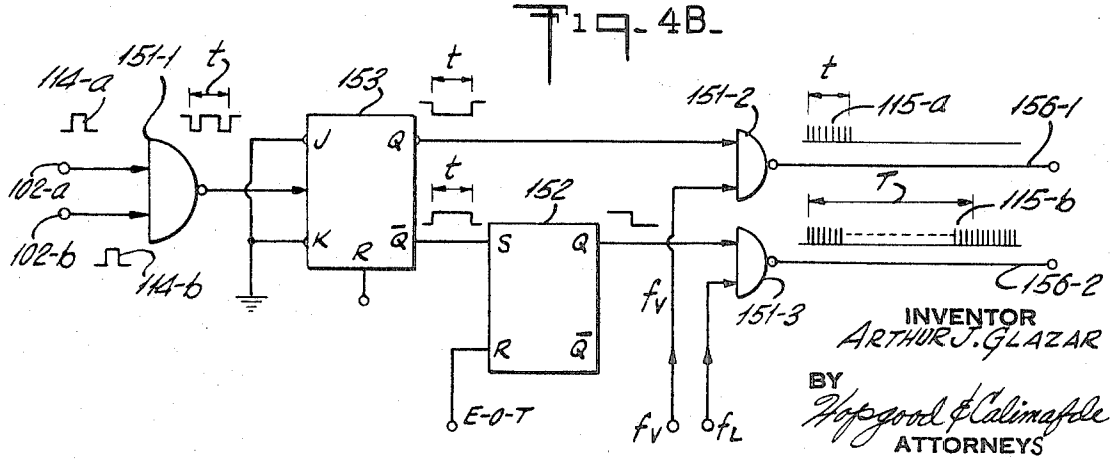

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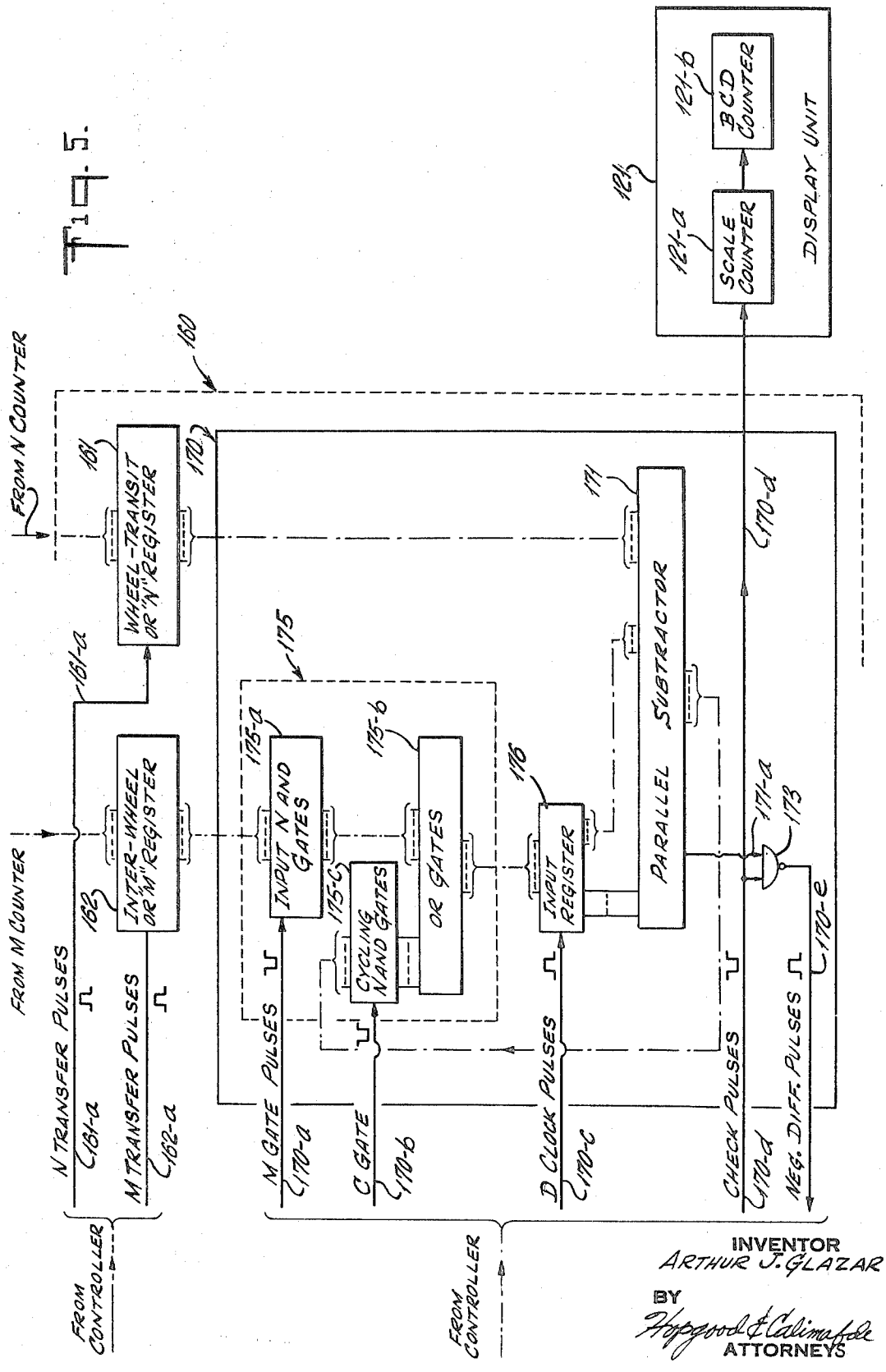
FIG. 5.



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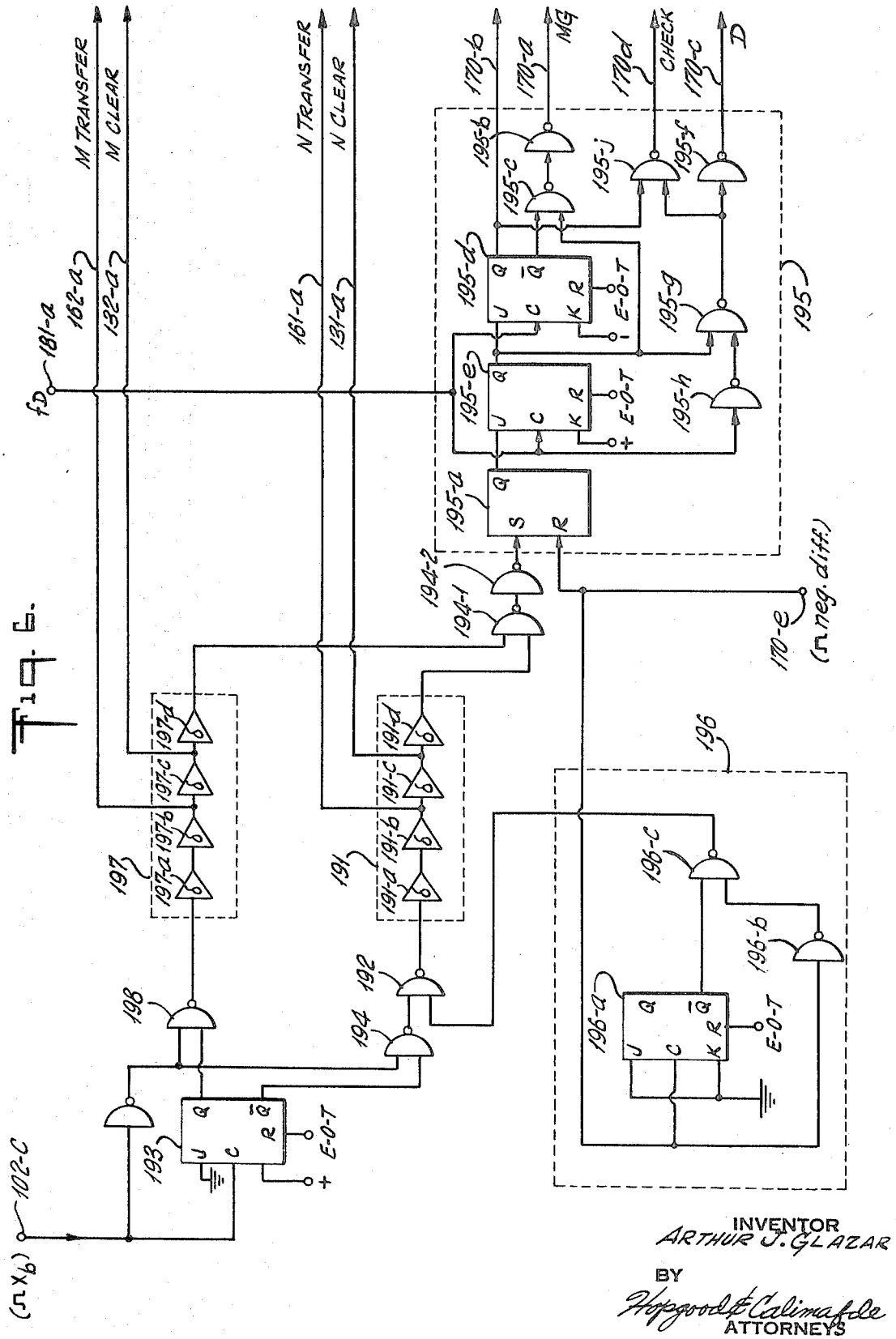

FIG. 6.

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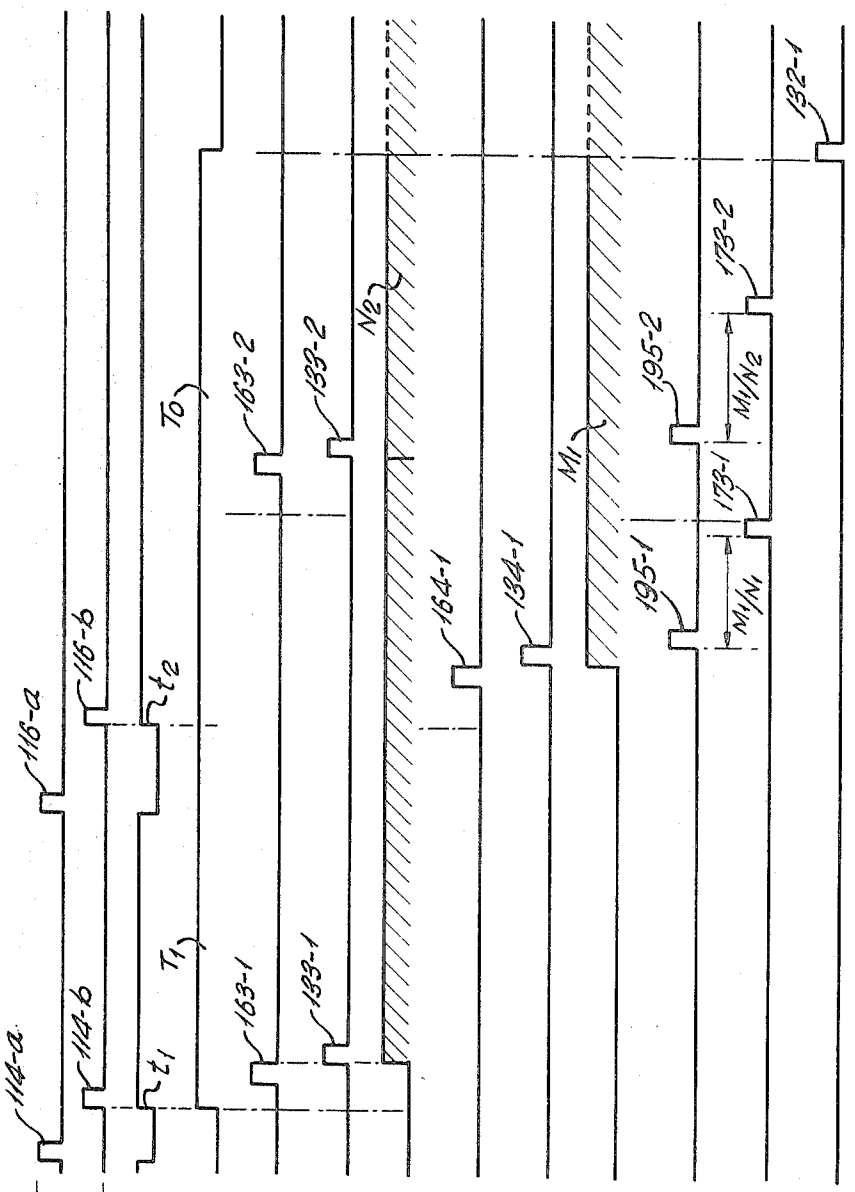
Fig. 7.



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AUTOMATIC TRAIN LENGTH COMPUTER

In particular, the overall length of a train of moving railroad cars is determined by sensing the passage of each wheel, on one side of the train, and using the sensings to obtain (1) a measure of the rate of travel of each car during each sensing interval and (2) a measure of the time interval between successive sensings. From these measures of rate and time, the wheel-to-wheel distances of and between the various cars are calculated and summed to give the desired train length.

In the disclosed embodiment of the invention, the sensing of each wheel is by a track-mounted magnetic transducer with two spaced-apart sensing heads. As a result, the wheel transit produces respective signals at the beginning and at the end of the transit interval.

The transducer signals, in turn, control the gating of constant-frequency signals which are counted to provide measures of rate and time. The number of constant-frequency signals counted during the sensing of each wheel gives a direct measure of the wheel-transit interval and an inverse measure of the average rate of travel of the associated car in that interval. The number of constant-frequency signals counted between wheel sensings is a direct measure of the interwheel interval.

Processing of the interwheel count signals and the associated wheel-transit count signals gives a measure of interwheel distance. The totality of such distances is a measure of the overall train length. In processing, each set of interwheel count signals is divided successively by the wheel-transit count signals at the beginning and at the end of the associated interwheel interval. The use of two sets of wheel-transit count signals with each set of interwheel count signals gives, in effect, an average rate of travel for the interwheel interval and thus takes into account changes in the rate of travel between successive wheel sensings.

BACKGROUND OF THE INVENTION

This invention relates to the determination of prescribed parameters, such as length and rate of travel, for moving items, and more particularly to the determination of overall length for a train of moving railroad cars.

The determination of length and rate parameters for moving items is important, for example, in traffic control. In the case of railroad traffic, information as to the length of a moving train is used to indicate when switching is to take place and whether or not the train can be accommodated by a particular siding.

Conventionally, the length of a moving train has been determined manually by counting the number of individual cars and multiplying the count by an average length per car. This method is slow and inaccurate. A manual car count is adversely affected by such factors as operator fatigue, lack of attention and impaired visibility, which may be due to inclement weather. Moreover, the difficulty of making an accurate count is increased when the train is in motion, particularly at the changing speeds often encountered in switching.

Nor are the problems encountered in measuring the length of a moving train significantly remedied by employing an automatic car counter. Such a counter may pose problems of reliability, complexity and cost. In some cases it may be necessary to make extensive modifications in the railroad right-of-way, or even in the cars themselves. In addition, any computed length obtained by multiplying the car count by an average length per car is likely to be in error because of variations in the lengths of the individual cars.

Accordingly, it is an object of the invention to facilitate the measurement of prescribed parameters, such as length and rate of travel, for items in motion. A related object is to facilitate the measurement of length and rate parameters for moving railroad trains.

Another object of the invention is to make precision measurements of moving items and to do so automatically. A related object is to make precise automatic measurements for moving railroad trains.

Still another object of the invention is to make precise measurements of moving items despite variations in the individual items. A related object is to make precise overall length measurements of moving railroad trains despite variations in the lengths of the individual cars.

Yet another object of the invention is to make rapid and precise measurements of moving items in the face of changes in rate of travel while the measurements are being made. A related object is to make rapid and precise measurements of overall lengths for moving railroad trains even while undergoing acceleration or deceleration as the measurements are being made.

A further object of the invention is to sense moving items and to use the sensings in making prescribed measurements without requiring structural modifications of the items, or mechanically moving parts in the sensing device. A related object is to sense the passing cars of a railroad train in order to make overall length measurements without the need for structural changes in the cars or mechanically moving parts in the sensing device.

Still a further object of the invention is to make desired length and rate measurements without interference by climatic conditions and without requiring a critical location for the sensing device.

Additional objects of the invention are to achieve relative simplicity, reliability and moderate cost in the realization of precision automatic measuring equipment for determining overall train length. A companion object is to realize a length measurement system that is readily converted to other measurement functions as well.

SUMMARY OF THE INVENTION

In accomplishing the foregoing and related objects, the invention provides for sensing a unit in motion a plurality of times and establishing a plurality of measures of time with respect to the various sensings. The unit in motion may be constituted, for example, by a train of tandem-connected items.

Signals corresponding to the measures of time thus established are processed to provide a measure of the desired parameter, such as overall length, or rate of travel during each sensing interval.

Since there is more than one sensing during the passage of the unit, each time interval between sensings is associated with a subordinate length of the unit, while the time interval of the sensing gives a measure of rate of travel for the unit. As a result, time and rate information is available for determining a measure of the subordinate length. The totality of the subordinate lengths provides the overall length of the unit.

In particular, signals representing the quotient of the measures of time for (1) the interval between sensings and (2) the interval of one of the sensings, give an indication of the intersensing distance. Where the further quotient of signals is obtained for (1) the interval between sensings and (2) the interval of the other of the sensings, signals corresponding to the sum of the two quotients, disregarding a multiplying factor, are a measure of the intersensing distance which takes rate of travel changes into account.

In accordance with one aspect of the invention, the sensings are made for a train of tandem-connected railroad cars by using a track-mounted transducer with two spaced-apart, magnetic sensing heads. As a wheel passes over the transducer, it produces respective signals marking the beginning and the end of the wheel-transit interval. The transducer signals are used in generating other signals which are measures of time for the wheel-transit and interwheel intervals. Such a transducer has no moving parts and requires little maintenance. It is not affected by inclement weather.

In accordance with another aspect of the invention, the transducer signals are used to gate constant-frequency signals that are counted to establish the respective wheel-transit and interwheel intervals. The wheel-transit count is a reciprocal

measure of the rate of travel of the car being sensed. Where the sensing heads of the transducer are closely spaced, compared with any interwheel distance, the wheel-transit counts are accurate reciprocal measures of the rates of car travel at the beginning, and at the end, of the interwheel interval. Thus the computation of interwheel distance with such counts makes allowance for changes in the rate of travel during the interwheel interval.

According to a further aspect of the invention, the desired measure of overall train length is obtained by summing successive measures of interwheel distance. Each such distance is determined by dividing the signals of the interwheel count by the signals of successive wheel-transit counts at the beginning and at end of the corresponding interwheel interval. Hence the resulting distance determination is accurate even if the train is undergoing linear acceleration or deceleration during measurement.

According to a still further aspect of the invention, the count quotients are obtained by the parallel subtraction of binary count signals, with the wheel-transit count signals being repeatedly subtracted from the residue of the interwheel count signals, until a negative difference is obtained. The number of such subtractions is the desired measure of interwheel distance, and their totality for all interwheel distances is the desired overall train length. A count of the subtractions is made at a rate indicated by a system scale factor. The latter is adjustable by changing the constant-frequency counting signals. Operation of the measurement equipment is terminated by an end-of-train pulse signal, illustratively produced by an overflow count which exceeds the maximum anticipated count for any interwheel interval.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the invention will become apparent after considering an illustrative embodiment thereof, taken in conjunction with the drawings in which:

FIG. 1 is a perspective view of an illustrative environmental setting for a train length measurement system in accordance with the invention;

FIG. 2 is a block diagram of constituents for the measurement system of FIG. 1;

FIGS. 3A and 3B are diagrams for a track-mounted sensor in the measurement systems of FIGS. 1 and 2, of which FIG. 3A is a partial perspective and schematic diagram of the track-mounted sensor and FIG. 3B is a graphical diagram of signals generated by the sensor;

FIGS. 4A and 4B are diagrams for a measurement signals generator in the measurement system of FIGS. 1 and 2, of which FIG. 4A is a wiring and schematic diagram of a preliminary signal conditioner and FIG. 4B is a logic diagram of a gating unit;

FIG. 5 is a block diagram of a divider logic network for an arithmetic unit in the measurement system of FIGS. 1 and 2;

FIG. 6 is a block diagram of a controller logic network for a controller in the measurement system of FIGS. 1 and 2; and

FIG. 7 is a timing diagram for the measurement system of FIGS. 1 and 2.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

Turning to the drawings, an illustrative setting for a measurement system **100** in accordance with the invention is the switching yard **10** of FIG. **1**, with various sidings **11–1** thru **11–3** for the temporary storage of railroad rolling stock. The particular siding to which an incoming train **20** is to be routed depends upon the unused capacity of the sidings **11–1** thru **11–3** and the length L of the train **20**. For simplicity the train **20** is shown with only two cars **21–1** and **21–2**.

To obtain a measure of the train length L while the cars **21–1** and **21–2** are in motion, a measurement system **100** is used to sense the wheels **22** and establish measures of the time intervals between sensings, from which a measure of the desired length L is determined, even if the train **20** is undergoing linear acceleration or deceleration during the measurement period.

A representative measurement system **100** includes a rail mounted sensor **110** in advance of a spur line switching position **12** and measurement equipment **120** at a control center **30**.

As the wheels **22** of the incoming cars **21–1** and **21–2** pass over the sensor **110**, indicating signals are produced and transmitted over a cable **101** to the center **30** where they are used in generating measurement signals by a generator **130**. Digital processing then takes place in an arithmetic unit **160** under the supervision of a controller **180** to produce a direct reading of the train length L by a display unit **121**. The equipment **120** is powered in known fashion by a power supply **122**.

More specifically, the passage of the wheels **22** over the sensor **110** produces indicating signals from which measurement signals are generated for (1) transit time of each wheel over the sensor **110** and (2) the time interval between wheel transits. These measurement signals, in turn, permit a determination of successive wheel-to-wheel distances D_1 thru D_7.

Consequently, except for overhang distances OH_1 and OH_2 at the beginning and end of the train **20**, a measure of the overall length L is obtained as a summation of signals representing the wheel-to-wheel distances D_1 thru D_7. Representative overhang distances can be preprogrammed into the arithmetic unit **160** or an allowance made for them.

Each wheel-to-wheel distance D_1 thru D_7 is determined using two wheel transit times so that the determination of the train length L takes into account changes in rate of travel caused by linear acceleration and deceleration, as explained below.

Once the train length L is established, a selected switch **13–1**, **13–2** or **13–3** is operated for one of the sidings **11–1**, **11–2** or **11–3** in accordance with the desired routing of the train **20**. The control exercised in response to the length indication L of the display unit **121** may be manual or automatic. While the signals from the sensor **110** are shown applied to a cable **101**, other suitable modes of transmission may be employed instead.

I. GENERAL BLOCK DIAGRAM CONSIDERATION OF THE SYSTEM 100

A block diagram of the measurement system **100** is set forth in FIG. **2**. The signals produced by the track mounted sensor **110** are applied to the measurement signals generator **130** where they are converted to a form which is suitable for processing by the arithmetic unit **160**. Both the generator **130** and the arithmetic unit **160** are acted upon by the controller **180**.

As explained in detail below, the sensor **110** is a transducer with two internally positioned and separate sensing heads, so that the transit of each wheel **22** in (FIG. 1) gives rise to outputs on separate leads **101–*a*** and **101–*b*** of the cable **101**.

The sensor outputs are shaped into pulse signals by a preliminary signal conditioner **140** and operate a gating unit **150**. A sensor pulse output indicating the end of each wheel transit interval also activates a logic network **190** of the controller **180**.

Within the controller **180**, a clock unit generates three sets of pulse signals of frequencies f_D, f_V and f_L. The frequency f_D is the master clock frequency for timing division operations by the arithmetic unit **160** through the logic network **190**. Signals at the frequencies f_V and f_L appear on respective leads to the gating unit **150**, from which they are gated to counters **131** and **132**.

In the operation of the gating unit **150**, signals from the sensor **110**, after being shaped by the preliminary signal conditioner **140**, gate a burst of pulse signals to the counter **131** for each wheel-transit interval. Another burst of pulse signals associated with the interwheel interval enters the second counter **132**.

Signals corresponding to the two counts then enter associated registers 161 and 162 of the arithmetic unit 160 and are processed under the direction of the controller logic network 190 to provide the desired train length indication on the display unit 121.

II. THE TRACK MOUNTED SENSOR 110

Considering the details and operation of the track-mounted sensor 110, as shown mounted on a rail 23 in the view of FIG. 3A, two transducer heads, represented by coils 111–1 and 111–2 and separated by a fixed distance *d*, are embedded within a housing 113.

A suitable sensor 110 is an adaptation of the "railroad-wheel trip" disclosed in Gallagher et al., U.S. Pat. No. 3,151,827, Oct. 6, 1964. The Gallagher wheel trip employs a magnetic structure with a single coil, but any number of such structures can be included in a single housing. A sensor with two magnetic structures is marketed and sold by the Servo Corporation of America under the trademark and trade name SERVOPOLE. In this sensor, each of the coils 111–1 and 111–2 is wound about a separate magnetic core structure which includes the rail 23 against which the housing 113 is mounted.

For illustration, the sensor 110 of FIG. 3A is shown after it has just been traversed, in the direction indicated by the arrow, by the first wheel 22–1 on the measurement side of the first car 21–1. The second wheel 22–2 is approaching the sensor 110 and is separated from the first wheel 22–1 by the first measurement distance D_1.

As the flange of each wheel 22–1 or 22–2 passes over the sensor 110, there is a change in the reluctance of the magnetic core structure associated with the coils 111–1 and 111–2, and thus of the magnetic flux.

For each core, the reluctance first decreases and then returns to its original value according to the extent of its coupling with the wheel 22–1 or 22–2. Correspondingly, the magnetic flux linking the associated coil 111–1 or 111–1 first increases and returns to its original value, generating a quasi-sinusoidal signal.

Illustratively, the quasi-sinusoids generated by the transit of the forward wheel 22–1 over the respective coils 111–1 and 111–2 are as pictured by the waveforms 113–*a* and 113–*b* of FIG. 3B for respective leads 101–*a* and 101–*b* of the cable 101. The subsequent transit of the second wheel 22–2 generates the dashed-line quasi-sinusoids 114–*a* and 114–*b*.

Each interval between successive quasi-sinusoids 113–*a*, *b* or 114–*a*, *b* generated by the coils 111–1 and 111–2 is the transit time *t* of the wheel 22–1 or 22–2. The interval between successive pairs of quasi-sinusoids 113–*a*, *b* and 114–*a*, *b* is the interwheel time T. For precision, the transit and interwheel times *t* and T are measured with respect to the zero-crossing points of the quasi-sinusoids 113–*a*, *b* and 114–*a*, *b*. These signals are applied to the generator 130 (FIG. 2) to produce measurement signals from which a measure of the desired train length L is obtained.

III. THE MEASUREMENT SIGNALS GENERATOR 130

In the generator 130, signals from the sensor 110 are shaped by a preliminary signal conditioner 140 and used in the controlled gating of recurrent pulse signals to the counters 131 and 132.

a. The Preliminary Signal Conditioner 140

Constituting the preliminary signal conditioner 140 are two similar units for the signals on the leads 101–*a* and 101–*b*.

Details of the unit for the lead 101–*b* are set forth in FIG. 4A. This unit includes a protector 141, filter 142, amplifier 143 and multivibrator 144 connected in cascade. The cascaded stages convert each incoming quasi-sinusoid on the lead 101–*b*, such as the quasi-sinusoid 113–*b*, into a single outgoing pulse signal on the output lead 102–*b*, such as the outgoing pulse 114–*b*.

The leading edge of the outgoing pulse 114–*b* is generated at the approximate "zero-crossing point" of the quasi-sinusoid 113–*b* where it is of zero magnitude between its positive and negative peaks. Each unit of the preliminary signal conditioner 140 is therefore a zero-crossing detector and pulse generator.

The protector 141 of the preliminary signal conditioner 140 guards against damage to the measurement equipment 120 (FIG. 2) by high-voltage transients, for example, by lightning surges on the rail 23 (FIG 3). For that purpose the protector 141 has a high-voltage breakdown device 141–*a* with a spark gap, followed by a medium-voltage breakdown device 141–*b* in the form of a diode. A suitable breakdown diode is sold and marketed under the trade name "THYRECTOR". Between the high-voltage and medium-voltage breakdown devices 141–*a* and 141–*b*, the protector 141 has an isolating resistor 141–*c*.

Beyond the protector 141, the filter 142 is of conventional resistor-capacitor construction to remove noise from incoming signals, such as the sensor signal 113–*b*.

The stage 143 is a high-gain saturating amplifier of conventional construction. It includes a transistor 143–*a* which is driven to saturation so that the output 143–*b* is at ground level during the positive half-cycle of the input 113–*b*.

The output stage for each unit of the preliminary signal conditioner 140 is a "one-shot multivibrator" 144. The stage 144 is a multivibrator in the sense of having alternative output signal states. It is a "one-shot" device in the sense of changing state in response to an applied input and producing a single output pulse.

During operation of the multivibrator 144, a first transistor 144–*a* responds to the output pulse 143–*b* of the high-gain saturating amplifier 143. When the amplifier pulse 143–*b* terminates, the multivibrator 144 changes state and its second transistor 144–*b* generates an output pulse 144–*b* on line 102–*b*. The pulse 144–*b* therefore has its leading edge at the approximate zero-crossing point of the input waveform 113–*b*. The duration of the output pulse 114–*b* is governed by the time constant of the multivibrator 144.

Similar stages to those discussed above for one unit of the signal conditioner 140 are included between the input line 101–*a* and the output line 102–*a* to form a unit for producing an output pulse 114–*a* corresponding to the input quasi-sinusoid 113–*a*. The relative delay between the outputs 114–*a* and 114–*b* is the wheel transit interval *t*.

b. The Gating Unit 150

From the preliminary signal conditioner 140 (FIGS. 2 and 4A), the output pulses 114–*a* and *b* are applied to the gating unit 150 detailed in FIG. 4B. As mentioned previously, the unit 150 gates two bursts of pulse signals of respective frequencies f_V and f_L from the clock unit 181 (FIG. 2) to respective counters 131 and 132 of the signal conditioner 130.

The gating unit 150 illustratively employs negative NAND logic with three different kinds of components: NAND gates 151–1 through 3, a regular flip-flop 152 and a clocked flip-flop 153.

Each of the NAND gates 151–1 through 3 produces a high output level whenever both inputs are low. In the case of negative logic, a ground level signal condition is associated with a binary 1. The NAND gates 151–1 through 3 are standard, such as supplied by Motorola Semiconductor Products, Inc.

The regular flip-flop 152 changes state, i.e. flips forward and then flops back, under the control of pulses applied at respective setting and resetting terminals S and R. There are outputs at direct and complimentary terminals Q and $\overline{Q}$. When the output at the Q terminal is a binary 1, as produced by a setting signal, the output at the $\overline{Q}$ terminal is a binary 0. The output are interchanged when a resetting signal is applied at the resetting terminal R, i.e. the Q output becomes a binary 0 and the $\overline{Q}$ output becomes a binary 1. The regular flip-flop 152 is of conventional design, being formed by the cross-coupling of two NAND gates in known fashion.

The clocked flip-flop **153** also changes state, except that it does so under the control of signals applied to a clocking terminal C. The output state, following clocking, depends upon the signals, before clocking, at input terminals J and K in accordance with TABLE I, which is known as a "truth table."

TABLE I

J input (before clocking)	K input (before clocking)	Q output (following clocking)
0	0	Q (no change).
1	0	1.
0	1	0.
1	1	$\overline{Q}$ (interchange).

The clocked flip-flop **153** can be directly reset by a signal applied to a reset terminal R (not connected in the gating unit **150** of FIG. 4B). Structurally the clocked flip-flop **152** is of known construction as supplied, for example, by Motorola Semiconductor Products, Inc.

Because of the input pulses **114**–*a* and **114**–*b* applied to the first NAND gate **151**–**1** of the gating unit **150**, the Q output of the clocked flip-flop **153** enables the second NAND gate **151**–**2** for a duration equal to the wheel transit time *t*. This allows a burst **115**–*a* of pulse signals of frequency f_V from the clock unit **181** (FIG. **2**) to appear on an output line **156**–**1**. Since the separation distance *d* of the coils **111**–**1** and **111**–**2** (FIG. **3**) is fixed, the number of pulses in the burst **115**–*a* is a measure of the wheel transit time *t*. The subscript "V" in the frequency designation f_V indicates that the wheel-transit signals are used to provide a measure of rate of travel, i.e. velocity, as explained below.

In addition, the $\overline{Q}$ output of clocked flip-flop **153** sets the regular flip-flop **152** at the end of each wheel-transit interval *t*. This enables the third NAND gate **151**–**3** and permits pulses of frequency f_L to appear on a second output line **156**–**2** at the beginning of the first interwheel interval T_1. It is not necessary to terminate the operation of the third NAND gate **151**–**3** at the end of the first interwheel interval T_1 since that interval is immediately followed by second and successive intervals T_2, T_3, etc. At the end of the final interwheel interval T_n, the third NAND gate **151**–**3** is disabled by a change of state of the regular flip-flop **152**. This change of state is brought about by an end-of-train pulse signal, generated in a manner described subsequently, at the reset terminal R.

c. The Counters **131** and **132**

From the gating unit, the output leads **156**–**1** and **156**–**2** are connected to the wheel-transit and interwheel counters **131** and **132**. Hence the number N of wheel-transit pulses in each burst **115**–*a* is counted by the unit **131**, while the number M of interwheel transit pulses in each burst **115**–*b* is counted by the unit **132**.

Both the N counter **131** and the M counter **132** are formed by regular binary counting chains, illustratively by the cascading of clocked flip-flops, each of the same type as the flip-flop **153** of the gating unit.

The first stage of each such counting chain has its clock terminal connected to an input lead **156**–**1** or **156**–**2**. For the remaining stages, the output of each preceding stage is connected to a clock terminal input of the succeeding stage. Consequently, a change in state of a preceeding stage is propagated to the succeeding stage and the pulse count therefore "ripples" through the chain. A delay interval, on the order of 1.5 microseconds, is needed before the counters settle to their final values.

IV. THE ARITHMETIC UNIT **160** AND ITS OPERATION

When the counters **131** and **132** are in a settled condition following counting, the N and M count signals are processed by the arithmetic unit **160** to give the desired train length measurement L.

a. The Processing Algorithm

During processing, the N and M count signals are manipulated to satisfy the algorithm of equation (1)

$$L=K\left(\frac{M_1}{N_1}+\frac{M_1}{N_2}+\frac{M_2}{N_2}+\cdots\frac{M_n}{N_n}+\frac{M_n}{N_{n+1}}\right) \quad (1)$$

where the subscripts
counting N and M indicate the
associated wheel-transit and interwheel
counting intervals,
K is a constant,
and L is the desired train length.

The fact that the manipulation of the N and M count signals in accordance with the algorithm of equation (1) will give the desired train length measurement L is demonstrated below.

Beginning with the count N for each wheel-transit interval *t*, equation (2) applies

$$N=f_V t \quad (2)$$

where f_V is the frequency, i.e. number of pulses
per second gated to the N-counter **131** (FIG. **2**)
by the second NAND gate **151**–**2** (FIG. **4B**)
and N and *t* are as defined above.

The transit time *t* of equation (2) can also be expressed as stated in equation (3)

$$t=\frac{d}{V} \quad (3)$$

where *d* is the distance of separation of the core
structures in the sensor **110** (FIG 3A)
and V is the average rate of travel of the car **21**–**1**
or **21**–**2** during the wheel transit interval *t*.

Consequently, the count N is also a measure of the rate of travel of a moving car during the wheel-transit interval *t*, as seen by substituting equation (3) into equation (2) with the result given by equation (4)

$$N=\frac{f_V d}{V}$$

or

$$V=\frac{f_V d}{N} \quad (4)$$

where the symbols are as defined for equations (2) and (3).

Considering next the count M for each interwheel interval T, the relationship of equation (5) applies

$$M=f_L T$$

or

$$T=\frac{M}{f_L} \quad (5)$$

where Where f_L is the frequency, i.e. number of pulses per
second, gated to the M-counter **132** (FIG. **2**) by
the third NAND gate **151**–**3** (FIG. **4B**)
and M and T are as defined above.

The distance D_1, D_2, etc. corresponding to each interwheel interval T_1, T_2, etc. is given by equation (6)

$$D_K=\overline{V}_k T_k \quad (6)$$

where the subscripts of D, $\overline{V}$ and T indicate the
particular interwheel interval, *k*,
$\overline{V}$ is the average rate of travel during the
associated interwheel interval,
and D and T are as defined above.

In the case of constant acceleration or deceleration of the cars of a train which closely approximates the situation encountered in practice when there is a change in the rate of travel, the average rate $\overline{V}$ of equation (6) is given by the average of the rates at the beginning and end of each interwheel interval, i.e. the average for successive wheel-transit times *t*.

Thus, for the first distance D_1 (FIG. **1**), the first average interwheel rate of travel $\overline{V}_1$ of equation (6) is given by equation (7) and substituting equation (4)

$$\overline{V}_1=\tfrac{1}{2}(V_1+V_2)$$
$$=\tfrac{1}{2}\left(\frac{f_V d}{N_1}+\frac{f_V d}{N_2}\right)$$
$$=\frac{f_V d}{2}\left(\frac{1}{N_1}+\frac{1}{N_2}\right) \quad (7)$$

where N_1 is the count for the transit of the first wheel 22–1,
N_2 is the count for the transit of the second wheel 22–2,
and the other symbols are as defined above.

Accordingly, the first distance D_1 is given by substituting equations (7) and (5) into equation (6), resulting in equation (8)

$$D_1=\frac{f_V d}{2}\left(\frac{1}{N_1}+\frac{1}{N_2}\right)\frac{M_1}{f_L}$$
$$=\frac{f_V d}{2f_L}\left(\frac{M_1}{N_1}+\frac{M_1}{N_2}\right)$$
$$=K\left(\frac{M_1}{N_1}+\frac{M_1}{N_2}\right) \quad (8)$$

where M_1 is the count during the interval T_1 between the transit of wheels 22–1 and 22–2,

$$K \text{ is a constant}=\frac{f_V d}{2f_L}$$

and the other symbols are as defined above.

Thus, in general, the overall length L is a summation of the various distances D_1, D_2, etc. with the result stated by equation (1) above.

b. Details of the Arithmetic Unit 160

From the counters 131 and 132, the N and M count signals enter respective registers 161 and 162 of the arithmetic unit 160 shown in FIG. 5. The registers 161 and 162 provide temporary storage and are of conventional design also making use, for example, of parallel clocked flip-flop stages, which are operated from the controller 180 to make the N and M count signals available to the divider logic network 170.

The central unit of the divider logic network 170 is a parallel subtractor 171 of conventional construction, which performs, for each different set of N and M count signals, successive subtractions of the N count signals from the residue of the M count signals.

Following each subtraction that does not produce a negative difference between minuend and subtrahend, a check pulse from the controller 180 is sent to the display unit 121 over a line 170–*d*. When a negative difference occurs, the magnitude of the residue of the M count signals is smaller than that of N count signals, and a borrow signal from the subtractor 171 enables a check gate 173. Upon the next occurrence of a check pulse, the check gate 173 sends an output to the controller 180 over a line 170–*e* to indicate that division has been completed for the particular set of N and M count signals.

The integral number of check signal outputs sent to the display unit 121 over the line 170–*d* is therefore a measure of the M and N quotient. Successive sets of N and M count signals are then acted upon by the subtractor 171 until the last wheel of the train has passed over the sensor 110 (FIG. 1). Hence the total number of outputs over the line 170–*d* to the display unit 121 is a measure of the overall train length L in accordance with equation (1).

A different set of N count signals appears at the subtractor 171 whenever an N transfer pulse is applied to the N register 161 over a line 161–*a* from the controller 180 (FIG. 2). When the N register 161 is formed by parallel clocked flip-flops, the line 161–*a* is connected to the clock terminals of the individual stages.

Similarly, a different set of M count signals is available from the M register 162 whenever an M transfer pulse appears on a line 162–*a*. The M register signals are subsequently applied to the subtractor 171 from an input register 176 after being sent through a subtractor gating network 175.

The purpose of the subtractor gating network 175 is to permit the initial entry of a full complement of M count signals and the subsequent recycling, until each division is completed, of the residual signals that result from successive subtractions.

Illustratively, in the case of negative NAND logic the subtractor gating network 175 passes the M count signals through input NAND gates 175–*a* and inverting OR gates 175–*b* at the beginning of each division cycle. Enablement of the NAND gates 175–*a* is by ground level M gate pulses over a line 170–*a* from the controller 180. Subsequently during the cycle, the signals resulting from each subtraction are reentered into the subtractor 171 by NAND gates 175–*c* of the gating network 175. These gates are operated by ground level C (for cycling) gate pulses on a line 170–*b* from the controller 180. A further set of pulse signals at the division clocking rate appears on a line 170–*c* of the input register 176.

The units within the divider logic network 170 of the arithmetic unit 160 are standard. Thus the NAND gates 175–*a* and 175–*c* can consist of parallel sets of individual NAND gates with an input terminal for one of the M count bit signals and a second input terminal for an enablement line 170–*a* or 170–*b*.

In the case of the inverting OR gates 175–*b*, each constituent gate has terminals connected to corresponding individual gates of the NAND gates 165–*a* and 175–*c*.

The construction of the input register 176 is similar to that of the interwheel and wheel-transit registers 161 and 162 discussed previously.

For the subtractor 171, the well-known parallel binary arrangement is advantageously employed for enhanced computational speed. In an *n*-bit subtractor of this type, a total of $(n-1)$ full subtractors stages are required for the $(n-1)$ most significant or highest order bit signals, and a single half subtractor stage is used for the least significant or lowest order bit signal.

Each full subtractor stage has minuend, complementary subtrahend and borrow signal inputs, conventionally designated as X, $\overline{Y}$ and B. The borrow input B represents the value borrowed from the order under consideration by the next lower order. The half subtractor stage has no borrow input since it is used for the least significant or lowest order bit signal and therefore has no borrow from a next lower order.

All subtractor stage have difference and borrow signal outputs, conventionally designated as D and B′. The borrow output B′ represents the value borrowed from the next higher order by the order under consideration.

As is well known, the Boolean logic expressions for the difference and borrow outputs D and B′ of the half subtractor are as given in equation (9)

$$D=\overline{X}Y+X\overline{Y} \quad (9)$$
$$B'=\overline{X}Y$$

where the symbols are as defined above. Corresponding expressions for the difference and borrow output D and B′ of each full subtractor stage are as stated in equation (10)

$$D=B(XY+\overline{X}\overline{Y})+\overline{B}(X\overline{Y}+\overline{X}Y) \quad (10)$$
$$B'=\overline{X}Y+B(XY+\overline{X}\overline{Y})$$

where the symbols are as defined above.

From the standpoint of connection, the minuend input terminals are tied to the input register 176. Depending on scale factor K of equation (1), as explained subsequently, only a limited number of the complementary subtrahend inputs $\overline{Y}$, beginning with the least significant, are connected to the N–register 161. The remaining $\overline{Y}$ inputs are grounded in order to apply the complement of O input, as required by negative NAND logic, to the highest order stages.

The process of successive subtractions for each different sets of N and M count signals, and therefore the division of the corresponding counts, is completed when there is B′ output for the highest order stage of the subtractor **171**. This indicates that the successive subtractions have proceeded to a point where the subtrahend exceeds the minuend and results in a signal representing the "most significant borrow" on output terminal **171**–*a*.

Operation of the subtractor **171** is completed following an end-of-train pulse to the controller **180**. This terminates the signals on the various controller leads **170**–*a* thru **170**–*e*.

The end-of-train pulse is generated by including an additional (overflow) stage in the M counter **132** of FIG. **2**. The number of stages in the counter **132** is chosen so that an overflow occurs, and a corresponding signal generated, whenever the count exceeds the maximum anticipated interwheel interval. There is such a count following the transit of the last wheel of each train over the sensor **110** (FIG. **1**). The value of the count is established from a knowledge of the minimum rate of train speed, for example, 5 miles per hour, and the maximum interwheel distance.

When the end-of-train signal occurs, the accumulated count of the display unit **121** is the desired train length measurement L.

As shown in FIG. **5**, the display unit **121** accumulates check pulse outputs that result from successive N and M count quotients using a scale counter **121**–*a* and a binary-coded-decimal (BCD) counter **121**–*b*. The scale counter **121**–*a* takes the scale factor K of equation (1) into account. Since the arithmetic unit **160** processes binary signals, the scale factor K is desirably selected so that there are 2^n check pulse outputs per foot (or other suitable dimension) of train length. Consequently if the scale counter **121**–*a* has *n* stages it will produce a single output for every 2^n inputs. Where it is desired to have the length indication L of the display **121** in terms of decimal notation, the output from the scale counter **121**–*a* is applied to a binary-coded-decimal (BCD) counter **121**–*b*. Counters of the latter type are well known and can be formed by using decade-counting binary units, with each unit being reset at a count of **10**.

V. THE CONTROLLER **180**

The operations of the measurements equipment **110** are directed by the controller **180**. Included are a unit **181** for generating clock signals and a logic network **190** for timing the various operations of the measurement equipment (FIG. **2**)

a. The Clock Unit **181**

There are three different clock signals of frequencies f_L, f_V and F_D. As discussed previously, clock signals at frequencies f_L and f_V are gated to provide respective measures of interwheel and wheel-transit time. In addition, as shown by equation (8) above, the magnitudes of these frequencies determine the length-measurement scale factor K. Consequently, the scale factor of the measurement equipment **100** is readily adjusted by changing either frequency f_L or f_V.

Clock signals at the third frequency f_D govern the operation of the divide logic network **190**. This frequency is at the highest operating rate in the system since the successive subtractions of the N and M count signals must be completed during the shortest anticipated interwheel interval. Representative magnitudes for the various frequencies f_L, f_V and f_D are considered subsequently.

Although the division control frequency f_D is at the highest rate in the system, its stability is not critical. However, accuracy of measurement dictates relative stability for the other frequencies f_V and f_L, and it is desirable to generate one of them by using a conventional scaling counter to subdivide the division control frequency f_D. Accordingly, the division control frequency f_D is advantageously generated by a crystal-controlled oscillator so that the associated subfrequency f_V or f_L is relatively stable.

The other subordinate frequency f_L or f_V is made variable to permit calibration adjustments. A suitable variable-frequency generator is an adjustable multivibrator which is placed in a temperature-regulated oven to assure stability.

b. The Controller-Logic Network **190**

Suitable constituents for the controller network **190** are illustrated by the logic diagram of FIG. **6**.

There are three inputs. The first is the gating pulse signal, such as the pulse **114**–*b* (FIG. 4A), derived from the sensor **110** at the end of each wheel-transit interval and appearing on the line **102**–*c*. These signals set the controller network **190** into operation at the beginning and during each division cycle. The second input is on the line **181**–*a* and is at the master clock frequency f_D to time the division operations of the divider logic network **170**. The final input is the negative difference signal on the line **170**–*e* produced by the divider logic network whenever the division cycle of a particular set of N and M count signals has been completed. This signal initiates every other cycle of division operation. To set the controller network **190** into operation, the initial sensor-derived gating pulse **114**–*b* on the line **102**–*c* is applied to a delay amplifier chain **191**, through NAND gate **192**. This produces N-Register transfer and N-Counter clear pulses on output lines **161**–*a* and **131**–*a*. The clocked flip-flop **193**, together with NAND gate **194**, serves to select the first-occurring sensor-derived gating pulse. All succeeding input pulses to delay amplifier chain **191** are applied through a second input on NAND gate **192**, connected to a switch unit **196**. The function of the switch unit **196** is to select the first, third, fifth, and all other odd-numbered negative-difference pulses for application to the delay chain **191**. Thus, pulses appear on output lines **161**–*a* and **131**–*a* following the initial sensor-derived gating pulse **114**–*b*, and thereafter following each odd-numbered negative-difference signal.

Flip-flop **193**, in conjunction with NAND gate **198**, selects all but the initial sensor-derived gating pulses **114**–*b* for application to the input of delay-amplifier chain **197**. This produces M—Register transfer and M—Counter clear pulses on output line **162**–*a* and **132**–*a*, following all sensor-derived gating pulses except the first.

Flip-flops **196**–*a* and **193** are reset to their original states by an end-of-train (E-O-T) pulse which is generated, as explained previously, but overflow of the M-counter **132**, which occurs after the last wheel of the train has crossed the sensor.

The delay amplifier chains **191** and **193** act through NAND gates **194**–**1** and **194**–**2** to periodically enable a distributor **195** for clock pulses at the master timing frequency f_D. The first NAND gate **194**–**1** produces an output for pulse signals on either chain **191** or **197**.

Once a divide start flip-flop **195**–*a* of the distributor **195** is set, the desired pulses for the divider logic network **170** (FIG. **5**) appear in succession on MG (Mgate) and C (cycling) lines **170**–*a* and *b*, and then on D (division clocking and check pulse lines **170**–*c* and *d*. A pulse at the division clocking rate appears only at the beginning of each division cycle on the MG line **170**–*a* from an inverter **195**–*b* through a NAND gate **195**–*c*. The latter is connected to the $\overline{Q}$ terminal of a flip-flop **195**–*d* that is clocked from the f_D line **181**–*a*. The NAND gate **195**–*c* is also connected to the Q terminal of another similarly clocked flip-flop **195**–*e*.

Subsequent pulses at the division clocking rate appear during each division cycle on the C line **170**–*b*. Additional division clocking pulses appear throughout the division cycle on the D line **170**–*c* from an inverter **195**–*f* by way of a NAND gate **195**–*g* and an input inverter **195**–*h*.

The check pulses which appear on the check line **170**–*d*, and are totaled by the display unit **121** (FIG. **5**) to give the desired overall length measurement, are supplied from a NAND gate **195**–*j*.

(*c*.) The Timing Diagram of FIG. **7**

A timing diagram which summarizes relationships among various signals and components of the measurement system is shown in FIG. **7**. For simplicity it has been assumed that the

train has only two wheels on its measurement side, and that they are spaced apart by the first interwheel distance D_1 of FIG. 1. Consequently, the desired length measurement, excluding overhang, is given directly by equation (8).

As indicated by FIG. 7, the first sensor-derived pulse 114–*a* initiates gating during the first wheel-transit interval t_1, which is terminated by the succeeding pulse 114–*b*. During this interval, the N-counter 131 makes the first interwheel count N_1. The terminal wheel-transit pulse 114–*b* then acts upon the controller logic network 190 (FIG. 6) to produce the delayed N-transfer pulse 163–1. This causes the first count N_1 to enter the N-register 161, where it remains until the occurrence of the next N-transfer pulse 163–2. Once the N-count has been transferred, the counter 131 is cleared by a pulse 133–1 to be ready for the next interwheel count N_2. Thus the N-register 161 stores the first interwheel count N_1 until the succeeding interwheel count N_2 is entered.

In the meantime the output of the interwheel gate 152 (FIG. 4B) permits clock pulses f_L to be counted by the M-counter 132 for the first interwheel interval T_1. Before this interval is terminated, the next wheel-transit interval t_2 commences with a sensor-derived pulse 116–*a* and is terminated by a succeeding pulse 116–*b*.

To indicate that the car being sensed is illustratively being slowed while measurements are being made, the second wheel-transit interval t_2 is shown to be longer than the first wheel-transit interval t_1.

As before, the terminal wheel-transit pulse 11614 *b* acts upon the controller logic network 170, and M-delay pulses 164–1 and 134–1 are produced.

The first M-delay pulse 164–1 transfers the count M_1, for the first interwheel interval T_1, from the M-counter 132 to the M-register 162. The M-counter 132 is then cleared by the second M-pulse 134–1. Since the interwheel gate 152 is not disabled until an end-of-train pulse is generated, the M-counter 132 proceeds to count what in the ordinary case would be the second interwheel count M_2 but which in the specific example under consideration is an end-of-train counting sequence, since it has been assumed that the train is constituted of a single car with a single interwheel distance D_1.

Following the pulse 134–1 the N-register 161 has the first wheel-transit count N_1 and the M-register 162 has the first interwheel count M_1. A divide start pulse 195–1 then appears at the divide-start flip-flop 195–*a* of the controller logic network 190 (FIG. 6). The previously described divisional process by successive subtraction proceeds to give a measure of the M_1/N_1 quotient, until a first negative difference pulse 173–1 is produced from the most significant borrow bit lead 171–*a* of the subtractor 171.

This negative difference pulse 173–1 acts upon the delay chain 191 of the controller logic network 190 and gives rise to the second set of delay pulses 163–2 and 133–2. These pulses respectively (1) transfer the N_2 count, made in the wheel-transit interval t_2, from the N-counter 131 to the N-register 161 and (2) clear the N-counter 131. Upon the occurrence of the next divide-start pulse 195–2, the arithmetic unit 170 proceeds to evaluate the quotient M_1/N_2, until the second negative difference pulse 173–2 is produced.

Subsequently, the count of the M-counter 132 exceeds the maximum anticipated interwheel count and an end-of-train pulse 132–1 is generated. This terminates the arithmetic operations of the divider logic network 170.

VI. ILLUSTRATIVE DESIGN CONSIDERATIONS

In an illustrative embodiment of the invention, representative operating specifications are set forth in TABLE II.

Table II

Specification:	Value
Minimum train speed ($V_{min.}$)_____ft. sec__	7. 35
Maximum train speed ($V_{max.}$)_____ft.'sec__	55. 00
Minimum inter-wheel distance ($D_{min.}$)_ft__	5. 00
Maximum inter-wheel distance ($D_{max.}$)_ft__	62. 00
Spacing (d) of the sensing heads (coils) in the sensor 110 (FIG. 3A)_____in__	9. 60
Measurement accuracy_____	±1%

(*a.*) The Counting Frequencies f_V and f_L

The signals f_V and f_L are asynchronously gated by the unit 150 (FIG. 4B) and are therefore subject to a count ambiguity of plus or minus one. If the M/N count ratio is to be in error by no more than 1 percent, a minimum count of 201 must be accumulated by either counter 131 or 132.

Accordingly, the minimum values for the counting frequencies f_V and f_L are determined from equation (11).

$$f_{min.}=\frac{K_{min.}V_{max.}}{S_{min.}}$$

where:

$$f_{min.} \text{ is either } f_V \text{ or } f_L$$
$$k_{min.} \text{ is either } N_{min.} \text{ or } M_{min.}$$
$$S_{min.} \text{ is either d or } D_{min.} \qquad (11)$$

and the other symbols are as defined above.

For the illustrative specifications of TABLE II, $f_{V(min)}$ is 13,819 Hz. and $f_{L(min)}$ is 2,211 Hz. For practical reasons these would be rounded out to 14,000 Hz. and 2,250 Hz., respectively.

(*b.*) The Scale Factor K of Equation (8)

Equation (11) is used in determining the minimum values of the counting frequencies f_V and f_L. As seen from equation (8) the values of these frequencies also control the scale factor

$$K=\frac{f_V d}{2f_L}$$

In addition, to obtain a resolution of 1 percent in the arithmetic unit 160, a factor m is selected such that $m\times K$ (m times K) is greater than or equal to 100. Since the arithmetic unit 160 operates on a binary basis, a binary value is selected, the nearest being $2^7=128$.

The factor m should also be a binary quantity 2^n, so that multiplication by m can be accomplished by shifting each interwheel count M by n bit positions away from the least significant bit position of the input register 176 (FIG. 6). If f_L is given the value of $f_{L(min)}$, f_V is given by equation (12).

$$f_V=\frac{2mf_{L(min.)}}{128d} \qquad (12)$$

where the symbols are as defined previously.

The value of m such that f_V equals or exceeds $f_{V(min)}$ is $m=2^9$, which gives f_V a value of 22,500 Hz.

(*c.*) The N and M Counter Capacities

The capacities of the N and M-counters 131 and 132 are determined by the maximum anticipated counts, which, with f_V and f_L established, are governed by (1) d and V_{min} and (2) by D_{max} and V_{min}, respectively. For the frequencies f_V and f_L considered above, the corresponding counts are $N_{max}=3{,}600$ and $M_{max}=27{,}900$. Consequently the N-counter 131 has a capacity of 12 bits and the M-counter 132 has a capacity of 15 bits. With the addition of an overflow stage to the M-counter 132, for generating an end-of-train pulse, overflow takes place at a count of $2^{16}=32{,}768$.

(*d.*) The Arithmetic Unit 170

For the specifications of Table II, the time available for performing each double division of M and N counts for each interwheel distance D is approximately 76 milliseconds. During this time the arithmetic unit produces a total number of output check pulses which is 128 times the measure of the interwheel distance D in feet. Therefore, the division clock frequency f_D must be at least 105,000 Hz. By selecting a division clock frequency of 225,000 Hz. there is at least a two-fold safety factor for timing the division operations, and the subfrequency f_V is obtained by dividing by 10.

Because the of the factor m in equation (12) the M count signals are multiplied by 2^9. This is accomplished by shifting the M count signals by nine places with respect to the least significant bit position of the arithmetic unit 160.

Further, for design specifications resulting in $2^7=128$ times the number of pulses per foot for each interwheel distance D, the scale counter 121–*a* has seven stages and the binary-coded

decimal output of the counter 121–*b* gives a direct measure of the desired train length L.

While various aspects of the invention have been set forth by the drawings, it it to be understood that the foregoing detailed description is for illustration only and that various changes in shape, proportion, arrangement of parts, as well as the substitution of equivalent elements for those shown and described, may be made without departing from the spirit and scope of the invention as set forth in the appended claims.

I claim:

1. An apparatus for measuring the length between successive wheels of a moving multiwheel train comprising:

first and second sensing means spaced-apart from each other along the path of motion of said train, each of said sensing means being adapted to generate a signal in response to the passage of a wheel there passed; first means operatively connected to said sensing means and responsive to said signals for establishing a measure of the time interval between the passage of each wheel past said first and second sensing means and generating a count indicative of said interval;

second means operatively connected to said sensing means and responsive to said signals for establishing a measure of the time interval between the passage of successive wheels past one of said sensing means and generating a count indicative of said interval; and

arithmetic logic means adapted to receive said generated counts and compute the sum of the quotients of (1) the count indicative of the time interval between the passage of successive wheels past one of said sensors and (2) the count indicative of the time interval between the passage of each of said successive wheels between said two sensors, said sum of the quotients being directly proportional to the linear distance between said successive wheels.

2. Apparatus in accordance with claim 1 further comprising a housing mounted against a section of one rail of the track of said moving train below the level thereof and said first and second sensing means each include coils wound about magnetic structures contained within said housing whereby the reluctance of said magnetic structures changes during the passage of a train upon said section.

3. Apparatus in accordance with claim 2 wherein said first time interval measuring means includes first means for generating recurring pulse signals of a first fixed, predetermined frequency; counter means operatively connected to said first pulse generator; gate means interposed between said first pulse generator and said counter; and means for enabling said gate means when each wheel of said train passes said first sensor and disabling said gate when said wheel passes said second sensor.

4. Apparatus in accordance with claim 3 further comprising second means for generating recurring pulse signals of a fixed, predetermined frequency; counter means operatively connected to said second pulse generator; second gate means interposed between said second generator and said second counter; and means for enabling said second gate when each wheel passes one of said sensors and for disabling said second gate when the next subsequent wheel passes the other of said sensors.