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(54) **DUAL-PORT NEGATIVE LEVEL SENSITIVE DATA RETENTION LATCH**

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(57)   **ABSTRACT**
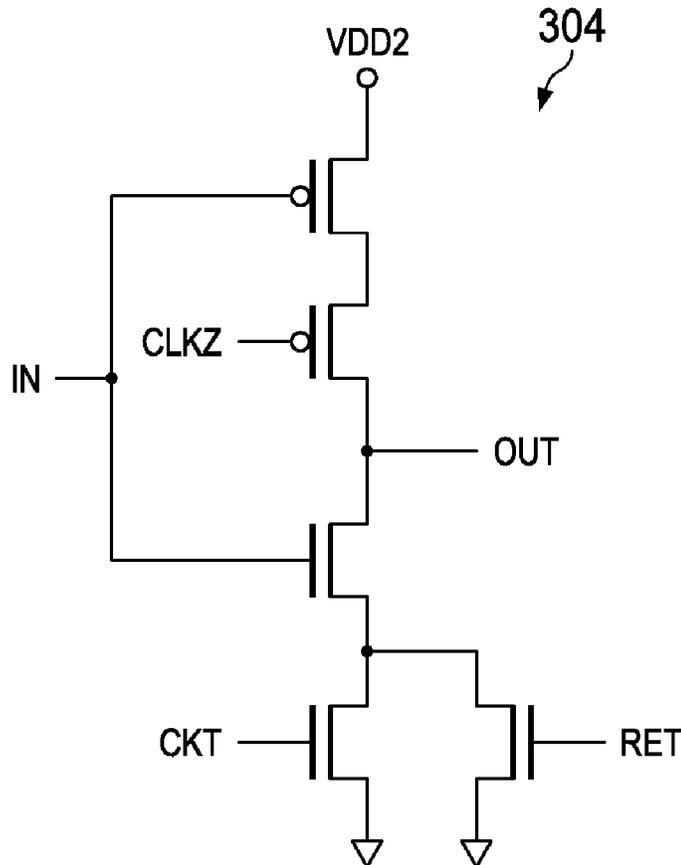
In an embodiment of the invention, a dual-port negative level sensitive data retention latch contains a clocked inverter and a dual-port latch. Data is clocked through the clocked inverter when clock signal CKT goes high, CLKZ goes low and retention control signal RET is low. The dual-port latch is configured to receive the output of the clocked inverter, a second data bit D2, the clock signals CKT and CLN, the retain control signals RET and the control signals SS and SSN. The signals CKT, CLKZ, RET, SS and SSN determine whether the output of the clocked inverter or the second data bit D2 is latched in the dual-port latch. Control signal RET determines when data is stored in the dual-port latch during retention mode.

304

FIG. 1

FIG. 2

108

302

QN

SS
VDD2

SSN

VDD2

SSN

SX

D2

306

SS

RET
VDD2

CKT

CLKZ

304

FIG. 3

VDD2

SS

IN

OUT

SSN

302

FIG. 4
(PRIOR ART)

VDD2

304

CLKZ

IN

OUT

CKT

RET

FIG. 5

VDD2

306

SSN

IN

OUT

SS

FIG. 6
(PRIOR ART)

SS

RET

CKT

D1

QN

SX

Q

QN LATCHED
AT THIS TIME

FIG. 7

RET

CKT

REN

D2

SS

SX

QN

Q

t_1 t_2 t_3

FIG. 8

DATA LATCHED IN
DUAL-PORT LATCH 108

RET

D2

SS

SX

QN

Q

t_1 t_2 t_4 t_3

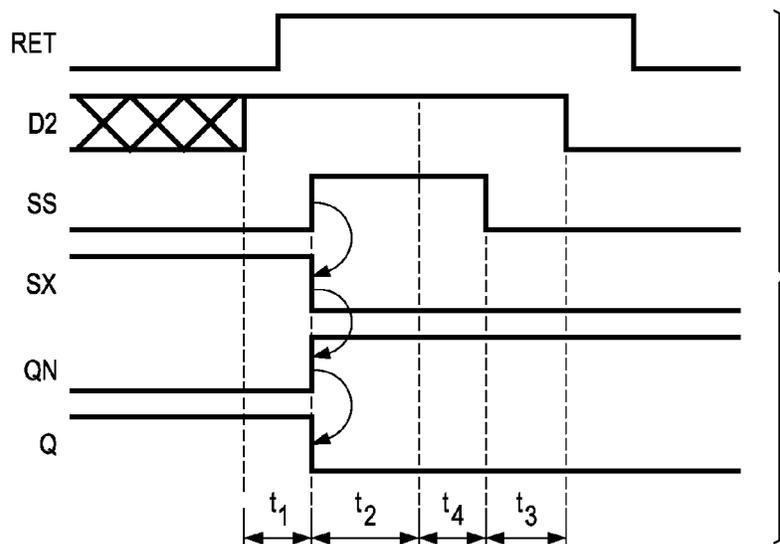**FIG. 9**

DATA LATCHED IN
DUAL-PORT LATCH 108

DUAL-PORT NEGATIVE LEVEL SENSITIVE DATA RETENTION LATCH

[0001] This application claims priority from Provisional Application No. 61/870,594, filed Aug. 27, 2013.

BACKGROUND

[0002] Several trends presently exist in the semiconductor and electronics industry. Devices are continually being made smaller, faster and requiring less power. One reason for these trends is that more personal devices are being fabricated that are relatively small and portable, thereby relying on a battery as theft primary supply. For example, cellular phones, personal computing devices, and personal sound systems are devices that are in great demand in the consumer market. It is also important that data on these devices be retained even when no power is supplied to the electronic device. Non-volatile memory circuits and non-volatile logic circuits are often used to meet these requirements.

[0003] Non-volatile logic implementation often requires updating sequential elements, such as latches, from a source external to the sequential element, such as a non-volatile memory. When non-volatile logic circuits are implemented to allow the updating of sequential elements, it is desired that the implementation of the non-volatile logic circuit does not significantly slow the operation of a sequential element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a block diagram of a dual-port negative level sensitive data retention latch according to an embodiment of the invention.

[0005] FIG. 2 is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

[0006] FIG. 3 is a schematic diagram of a dual-port latch according to an embodiment of the invention.

[0007] FIG. 4 is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

[0008] FIG. 5 is a schematic diagram of a clocked inverter according to an embodiment of the invention. (Prior Art)

[0009] FIG. 6 is a schematic diagram of a tri-state inverter according to an embodiment of the invention. (Prior Art)

[0010] FIG. 7 is a timing diagram showing signals SS, RET, D1, CLK, QN and the output of the latch Q according to an embodiment of the invention.

[0011] FIG. 8 is a timing diagram showing signals RET, CKT, D2, SS, SX, QN, and Q according to an embodiment of the invention.

[0012] FIG. 9 is a timing diagram showing signals RET, D2, SS, SX, QN, and Q according to an embodiment of the invention.

DETAILED DESCRIPTION

[0013] In an embodiment of the invention a dual-port negative level sensitive data retention latch 100 contains a clocked inverter 102, an inverter 110, a dual-port latch and a logic circuit 112 used to create clock CLKZ. The clocked inverter 102 is configured to receive a first data bit D1, a retain control signal RET, and internal clock signals CLKZ and CKT. The dual-port latch 108 is configured to receive the output QN from the clocked inverter 102, data input D2, clock signals CLKZ and CKT, the retain control signal RET and control signals SS and SSN. The signals CKT, CLKZ, RET, SS and SSN determine whether the output QN of the clocked inverter 102 or the second data bit D2 is latched in the dual-port latch 108.

[0014] Non-volatile logic implementations often require updating sequential elements (e.g. flip-flops and latches) from an external source (e.g. non-volatile memory). In an embodiment of the invention, the dual-port latch includes 108 a second data input (port). The second data input is used to insert data from an external source. A tri-state inverter is added to the dual-port latch 108 to accommodate the second data input. This will be explained in more detail later in the specification. When external data needs to be inserted into the dual-port latch, the tri-state inverter is enabled.

[0015] The circuitry used to add the second input to the dual-port latch 108 is not part of the critical timing path of the dual-port negative level sensitive data retention latch 100. As a result, change to the regular performance of the dual-port negative level sensitive data retention latch 100 is negligible.

[0016] FIG. 1 is a block diagram of a dual-port negative level sensitive data retention latch 100 according to an embodiment of the invention. In a functional (i.e. normal) mode of operation, the retention mode signal RET is held at a logical low level, the control signal SS is held at a logical low level and the binary compliment signal SSN of the control signal SS is held a logical high level. Power is needed for functional mode operation so power supply VDD1 and power supply VDD2 are applied to the dual-port negative level sensitive data retention latch 100.

[0017] FIG. 7 is a timing diagram showing data bit D1, clock signals CKT and CLKZ and the output Q of the dual-port negative level sensitive data retention latch 100 during the functional mode of operation. Because the RET is held at a logical low level, the binary logical compliment of D1 is passed to the output QN when clock signal CKT transitions from a high to low logical value. FIG. 2 illustrates an embodiment of a clocked inverter 102. QN is then presented to an input of the dual-port latch 108 and the inverter 110. The output of inverter 110 drives the signal Q.

[0018] FIG. 3 is a schematic diagram of a dual-port latch 108 according to an embodiment of the invention. The dual-port latch 108 includes a first tri-state inverter 302 (see FIG. 4 for an embodiment of the first tri-state inverter 302) with tri-state controls SS and SSN, a clocked inverter 304 (see FIG. 5 for an embodiment of the clocked inverter 304) with control RET and a second tri-state inverter 306 (see FIG. 6 for an embodiment of the second tri-state inverter 306) with tri-state controls SS and SSN.

[0019] When the dual-port negative level sensitive data retention latch 100 is operating in the functional mode, the tri-state inverter 302 is active and drives node SX of the dual-port latch 108 to the complimentary logical value of QN. When the clock signal CKT transitions from a low logical level to a high logical level, the logical level on the QN is latched by the clocked inverter 304. In this embodiment of the invention, an inverter 110 is used to buffer QN. However, non-inverting buffers may be used as well. The tri-state inverter 306 is tri-stated in this mode because SS is a logical low level and SSN is a logical high level. As a result, D2 is not transferred to node SX.

[0020] However, during another functional mode of operation (e.g. when RET=0), data D2 may be written directly to the dual-port latch 108 (See FIG. 8). During this functional mode, the clock signal CKT is held at a high logical level and

CLKZ is held at a low logical level with control signal SS held at a logical high level and control signal SSN held at logical low level.

[0021] When control signal SS is held at a logical high level and control signal SSN is held at logical low level, tri-state inverter **306** is able to drive the complimentary value of D**2** onto node SX of the dual-port latch **108**. Because CLKZ and RET are held at logical low levels and CKT is held at logical high level, the clocked inverter **304** is active and drives node QN to the logical value of D**2**. The inverter **110** then inverts the logical value on node QN to its compliment. In this example, the compliment of D**2** is presented on node Q. Data signal D**2** must be held for the period t3 to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time t2 to insure that the correct value D**2** is latched.

[0022] When control signal SS is driven from a logical high level to a logical low level and SSN is driven from a logical low level to a logical high level, the tri-state inverter **306** is tri-stated and tri-state inverter **302** becomes active latching the logical value on node QN of the dual-port latch **108**.

[0023] The dual-port negative level sensitive data retention latch **100** can also be operated to retain data (RET mode) in the dual-port latch **108** (power supply VDD2 is active) when clocked inverter **102**, logic circuit **112** and inverter **110** are powered off (i.e. power supply VDD1 is inactivated). Because the dual-port negative level sensitive data retention latch **100** is being operated in the RET mode, the retention mode signal RET is held at a logical high level and the SS and SSn signals are at a logic 0 and logic 1 respectively. Because power is not supplied to clocked inverter **102** and the inverter **110**, QN is not actively driven by clocked inverter **102**. In this manner, the data being retained in the dual-port latch **108** will not be inadvertently corrupted by the indeterminate output value of the clocked inverter **102** (the input is indeterminate as the supply VDD1 is inactive or floating). All other inputs are don't-cares.

[0024] During retention mode of operation, data D**2** may be written directly to the dual-port latch **108**. During this retention mode, the control signal SS is driven to a logical high level following RET being driven to a logical high value (see FIG. 9). The clock signals CKT and CLKZ are don't cares in this mode of operation in this embodiment. Before time t1, D**2** does not have to be driven to a logical level (i.e. D**2** may be a logical one, a logical zero, floating or tri-stated). D**2** must be driven to a logical one or a logical zero some time t1 before the control signal SS transitions from a logical zero to a logical one. D**2** must be stable for time t4 before the control signal SS transitions from a logical one to a logical zero and remain stable for time t3 afterwards in order to ensure D**2** will be correctly latched.

[0025] Because the control signal SS is driven to a logical high level following RET being driven to a logical high value, the tri-state inverter **302** is tri-stated and does not drive node SX of the dual-port latch **108**. Because the control signal SS is driven to a logical high and control signal SSN is driven to a logical low value, the tri-state inverter **306** is active and drives node SX to the complimentary value presented on D**2**. Because RET is a logical high value, the clocked inverter **304** is active and drives node QN. When the control signal SS returns to a logic low level and SSN returns to a logic high level, the value stored on node QN is latched between tri-state inverter **302** and clocked inverter **304** while tri-state inverter **306** is tri-stated. Data signal D**2** must be held for the period t3

to insure that the correct value of D**2** is latched. Also, control signal SS must remain at logical high value for time (t2+t4) to insure that the correct value D**2** is latched. Under this condition, the data written from D**2** remains latched in the dual-port latch **108** during retention mode.

[0026] The foregoing description has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiments were chosen and described in order to best explain the applicable principles and their practical application to thereby enable others skilled in the art to best utilize various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments except insofar as limited by the prior art.

What is claimed is:

1. A dual-port negative level sensitive data retention latch comprising:
   a clocked inverter configured to receive a first data bit (D**1**), clock signal (CKT), clock signal (CLKZ) and a retention mode control signal (RET) wherein (CKT), (CLKZ) and (RET) determine whether the data output (QN) from the clocked inverter is the binary compliment of data bit (D**1**) or an indeterminate value;
   a dual-port latch configured to receive the output (QN) of the clocked inverter, a second data bit (D**2**), the clock signal (CKT), the clock signal (CLKZ), the retain control signal (RET), a latch control signal (SS) and a latch control signal (SSN) wherein signals (CKT), (CLKZ), (RET), SS) and (SSN) determine whether the output (QN) of the clocked inverter or the second data bit (D**2**) is latched in the dual-port latch.

2. The dual-port negative level sensitive data retention latch of claim **1**, further comprising a first inverter wherein the first inverter receives the output (QN) and the first inverter outputs (Q).

3. The dual-port negative level sensitive data retention latch of claim **1**, further comprising a buffer wherein the buffer receives the output (QN) and the buffer outputs the same logical value of (QN).

4. The dual-port negative level sensitive data retention latch of claim **2** wherein the clocked inverter and the first inverter receive power from a first power supply (VDD1); wherein the dual-port latch receives power form a second power supply (VDD2).

5. The dual-port negative level sensitive data retention latch of claim **4** wherein the first power supply (VDD1) is turned off and the second power supply (VDD2) is turned on during operation of a retention mode; wherein power is only supplied to the dual-port latch.

6. The dual-port negative level sensitive data retention latch of claim **1** wherein control signals (SS), (SSN) and (RET) are controlled external to the dual-port negative level sensitive data retention latch to prevent data contention between (QN) and the second data bit (D**2**).

7. The dual-port negative level sensitive data retention latch of claim **1** wherein the dual-port latch comprises:
   a first tri-state inverter, the first tri-state inverter having a data input, two control inputs and a data output wherein the data input is electrically connected (QN), the first control input is electrically connected to (SS), and the second control input is connected to (SSN);

a second tri-state inverter, the second tri-state inverter having a data input, two control inputs and a data output wherein the data input is electrically connected to the second data bit (D2), the first control input is electrically connected to (SS), and the second control input is connected to (SSN) and the outputs of the first and second tri-state inverter are electrically connected to each other;

a clocked inverter, the clocked inverter having a data input, three control inputs and a data output wherein the data input is electrically connected to the data output of the first and second tri-state inverters, a first control input is electrically connected to (CKT), a second control input is connected to (CLKZ), a third control input is electrically connected to (RET), and the output of the clocked inverter is electrically connected to the input (QN) of the first tri-state inverter.

8. A method of writing data into a dual-port latch of a dual-port negative level sensitive data retention latch in retention mode comprising:

entering retention mode by driving the retain control signal (RET) to a logical high value;

disconnecting a first power supply (VDD1) from a clocked inverter configured to receive a first data bit (D1), clock signal (CKT), clock signal CLKZ and a retention mode control signal (RET) wherein (CKT), (CLKZ) and (RET) determine whether the data output (QN) from the clocked inverter is the binary compliment of data bit (D1) or an indeterminate value;

connecting a second power supply (VDD2) to the dual-port latch wherein the dual-port latch is configured to receive the output (QN) of the clocked inverter, a second data bit (D2), the clock signal (CKT), the clock signal (CLKZ), the retain control signal (RET), a latch control signal (SS) and a latch control signal (SSN) wherein signals (CKT), (CLKZ), (RET), SS) and (SSN) determine whether the output (QN) of the clocked inverter or the second data bit (D2) is latched in the dual-port latch;

driving the second data bit (D2) to a binary logical level;

writing the second data bit (D2) into the dual-port latch by driving the control signal (SS) to a logical high value and driving the control signal (SSN) to a logical low value;

latching the second data bit (D2) into the dual-port latch by driving the control signal (SS) to a logical low value and driving the control signal (SSN) to a logical high value;

connecting the first power supply (VDD1) to clocked inverter;

exiting the retention mode and entering a functional mode by driving control signal (RET) to a logical low.

9. A method of writing data to a dual-port latch of a dual-port negative level sensitive data retention latch while in a functional mode comprising;

entering the functional mode by driving retain control signal (RET) to a logical low value;

tri-stating an output of a clocked inverter by driving a clock signal (CKT) to a logical high level and by driving a clock signal (CKZ) to a logical low level;

driving a second data bit (D2) of the dual port latch to a binary logical level wherein the dual-port latch is configured to receive the output of the clocked inverter, a second data bit (D2), the clock signal (CKT), the binary logical compliment signal (CLKZ) of the clock signal (CKT), the retain control signal (RET), a control signal (SS) and the binary logical compliment signal (SSN) of the control signal (SS) wherein signals (CKT), (CLKZ), (RET), (SS) and (SSN) determine whether the output (QN) of the clocked inverter or the second data bit (D2) is latched in the dual-port latch;

writing the second data bit (D2) into the dual-port latch by driving the control signal (SS) to a logical high value and driving the control signal (SSN) to a logical low value;

latching the second data bit (D2) into the dual-port latch by driving the control signal (SS) to a logical low value and driving the control signal (SSN) to a logical high value;

allowing CKT and CLKZ to toggle.

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