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Hyde et al.

(54) **MULTI-CORE PROCESSING IN MEMORY**

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(73) Assignee: **Elwha LLC, a limited liability corporation of the State of Delaware**, Bellevue, WA (US)

(21) Appl. No.: **13/738,788**

(22) Filed: **Jan. 10, 2013**

Related U.S. Application Data

(63) Continuation-in-part of application No. 13/738,747, filed on Jan. 10, 2013, which is a continuation-in-part of application No. 13/725,788, filed on Dec. 21, 2012, which is a continuation-in-part of application No. 13/691,448, filed on Nov. 30, 2012, which is a continuation-in-part of application No. 13/687,983, filed on Nov. 28, 2012, which is a continuation-in-part of application No. 13/678,439, filed on Nov. 15, 2012, which is a continuation-in-part of application No. 13/678,430, filed on Nov. 15, 2012.

Publication Classification

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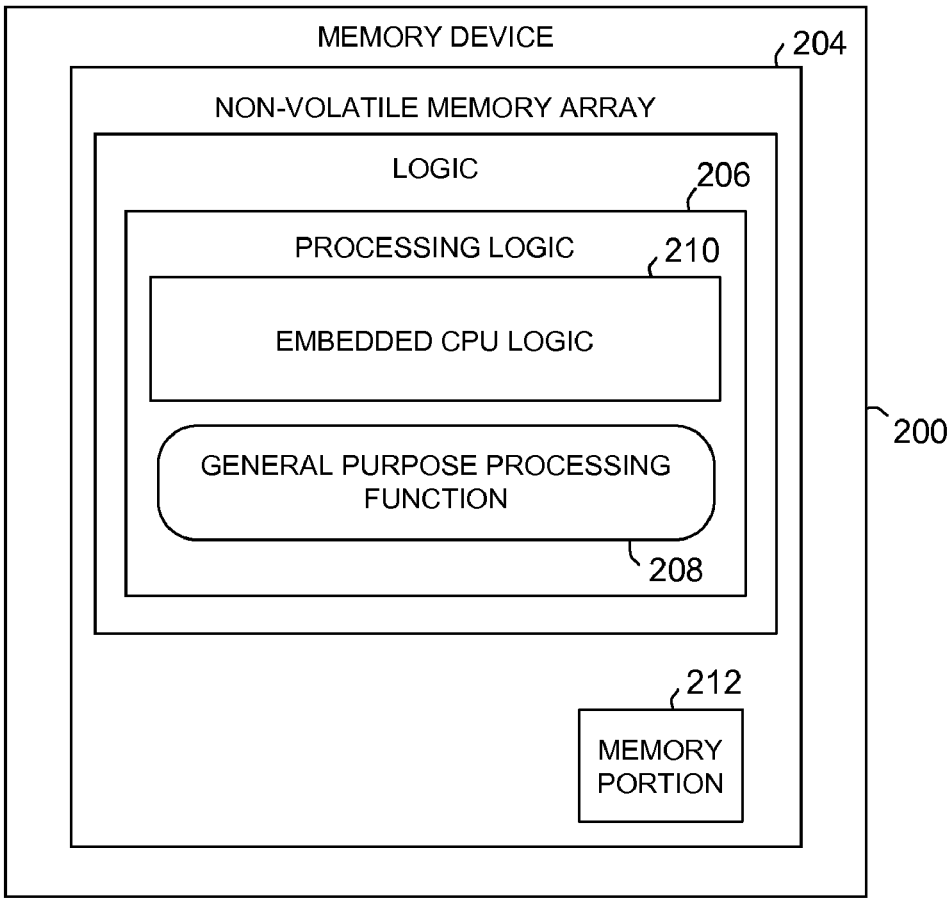
G06F 9/46 (2006.01)

(52) **U.S. Cl.**
CPC ***G06F 9/46*** (2013.01)
USPC **718/100**

(57) **ABSTRACT**

A memory device includes but is not limited to a substrate, a non-volatile memory array integrated on the substrate, and processing logic integrated with the non-volatile memory array on the substrate. The processing logic is operable to perform at least one general purpose processing function associated with the non-volatile memory array.



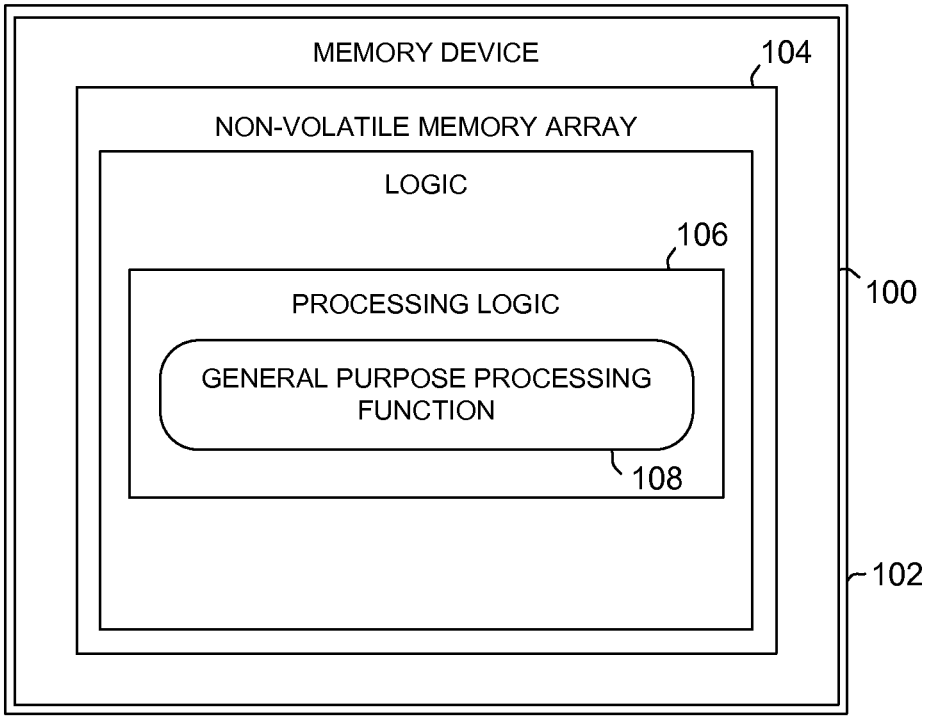

MEMORY DEVICE
104
NON-VOLATILE MEMORY ARRAY
LOGIC
106
PROCESSING LOGIC
GENERAL PURPOSE PROCESSING FUNCTION
108
100
102

FIG. 1A

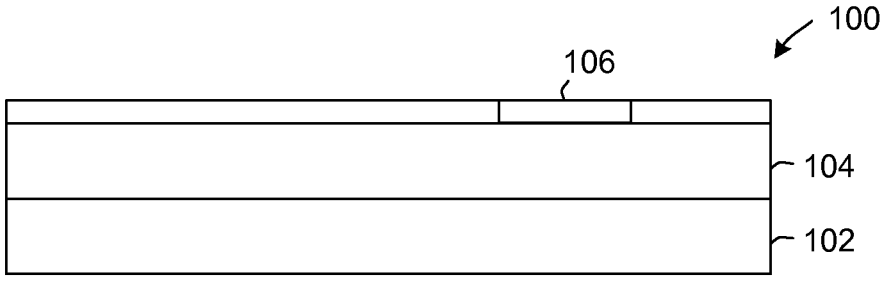

100
106
104
102

FIG. 1B

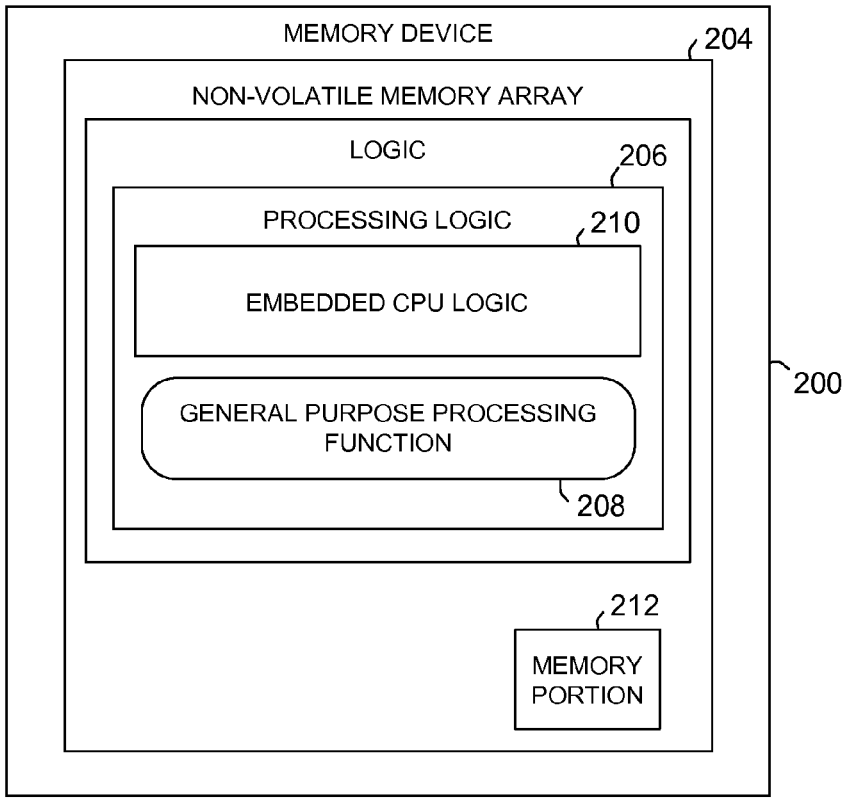

MEMORY DEVICE
204
NON-VOLATILE MEMORY ARRAY
LOGIC
206
PROCESSING LOGIC
210
EMBEDDED CPU LOGIC
GENERAL PURPOSE PROCESSING FUNCTION
208
212
MEMORY PORTION
200

FIG. 2A

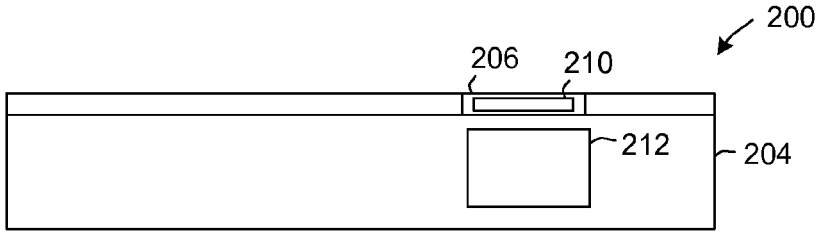

200
206
210
212
204

FIG. 2B

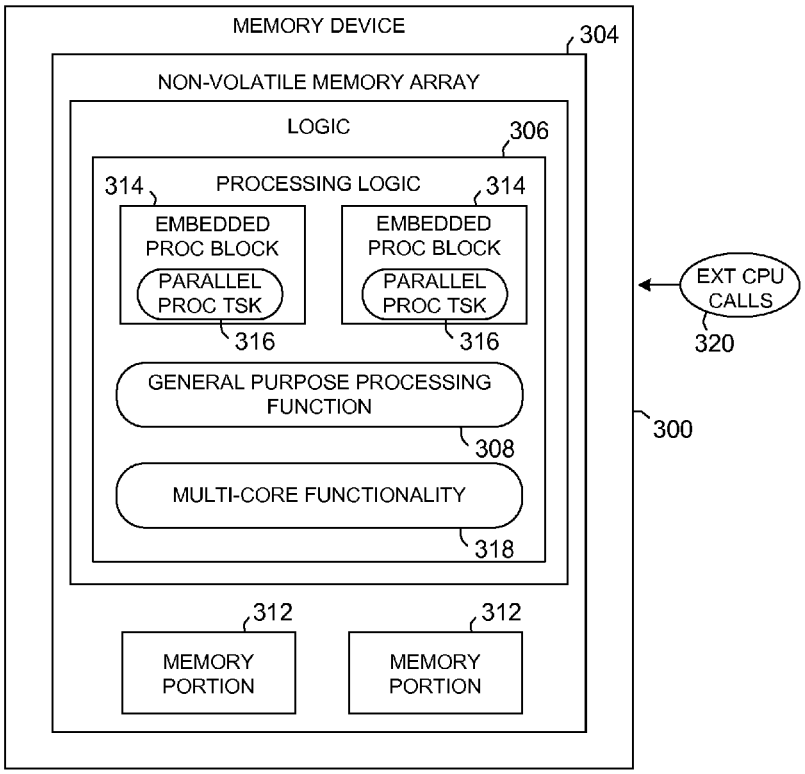

MEMORY DEVICE
304
NON-VOLATILE MEMORY ARRAY
LOGIC
306
314
PROCESSING LOGIC
314
EMBEDDED PROC BLOCK
PARALLEL PROC TSK
316
EMBEDDED PROC BLOCK
PARALLEL PROC TSK
316
EXT CPU CALLS
320
GENERAL PURPOSE PROCESSING FUNCTION
308
MULTI-CORE FUNCTIONALITY
318
300
312
MEMORY PORTION
312
MEMORY PORTION

FIG. 3A

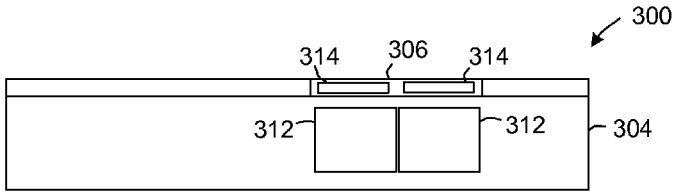

300
314
306
314
312
312
304

FIG. 3B

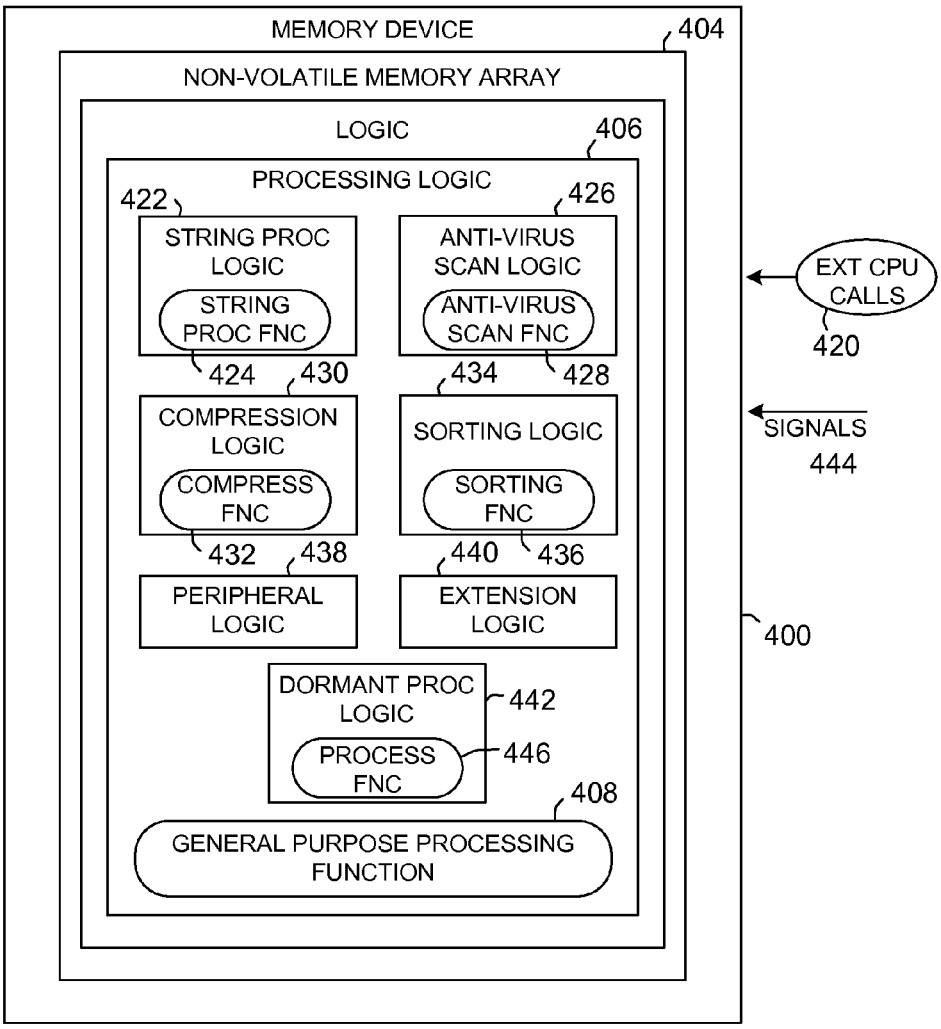

MEMORY DEVICE
404
NON-VOLATILE MEMORY ARRAY
LOGIC
406
PROCESSING LOGIC
422
426
STRING PROC LOGIC
STRING PROC FNC
ANTI-VIRUS SCAN LOGIC
ANTI-VIRUS SCAN FNC
424
430
434
428
COMPRESSION LOGIC
COMPRESS FNC
SORTING LOGIC
SORTING FNC
432
438
440
436
PERIPHERAL LOGIC
EXTENSION LOGIC
DORMANT PROC LOGIC
442
PROCESS FNC
446
408
GENERAL PURPOSE PROCESSING FUNCTION
EXT CPU CALLS
420
SIGNALS
444
400

FIG. 4A

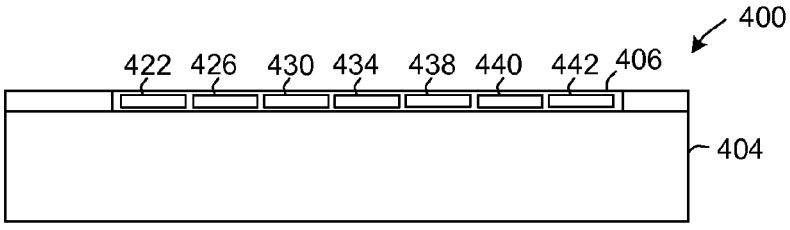

400
422
426
430
434
438
440
442
406
404

FIG. 4B

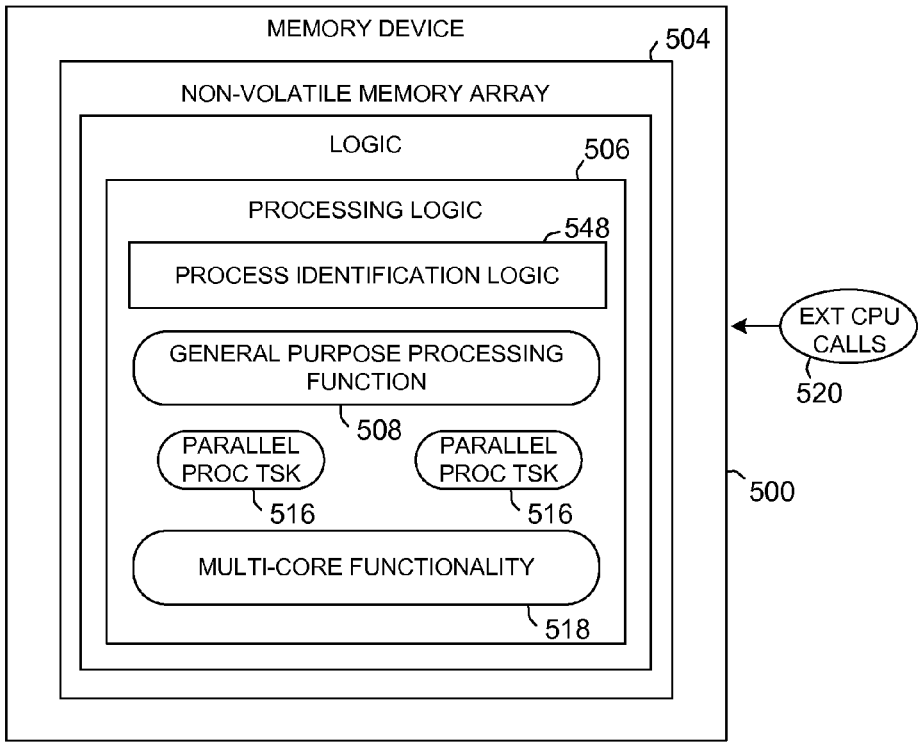

MEMORY DEVICE
504
NON-VOLATILE MEMORY ARRAY
LOGIC
506
PROCESSING LOGIC
548
PROCESS IDENTIFICATION LOGIC
GENERAL PURPOSE PROCESSING FUNCTION
508
PARALLEL PROC TSK
516
PARALLEL PROC TSK
516
MULTI-CORE FUNCTIONALITY
518
EXT CPU CALLS
520
500

FIG. 5A

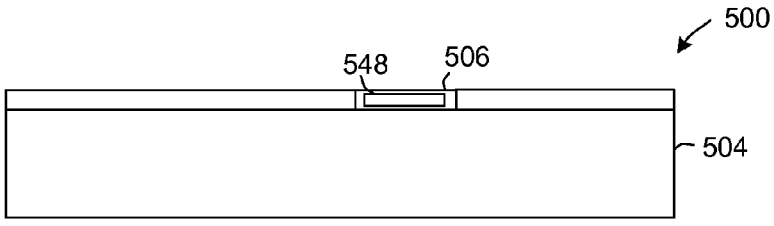

500
548
506
504

FIG. 5B

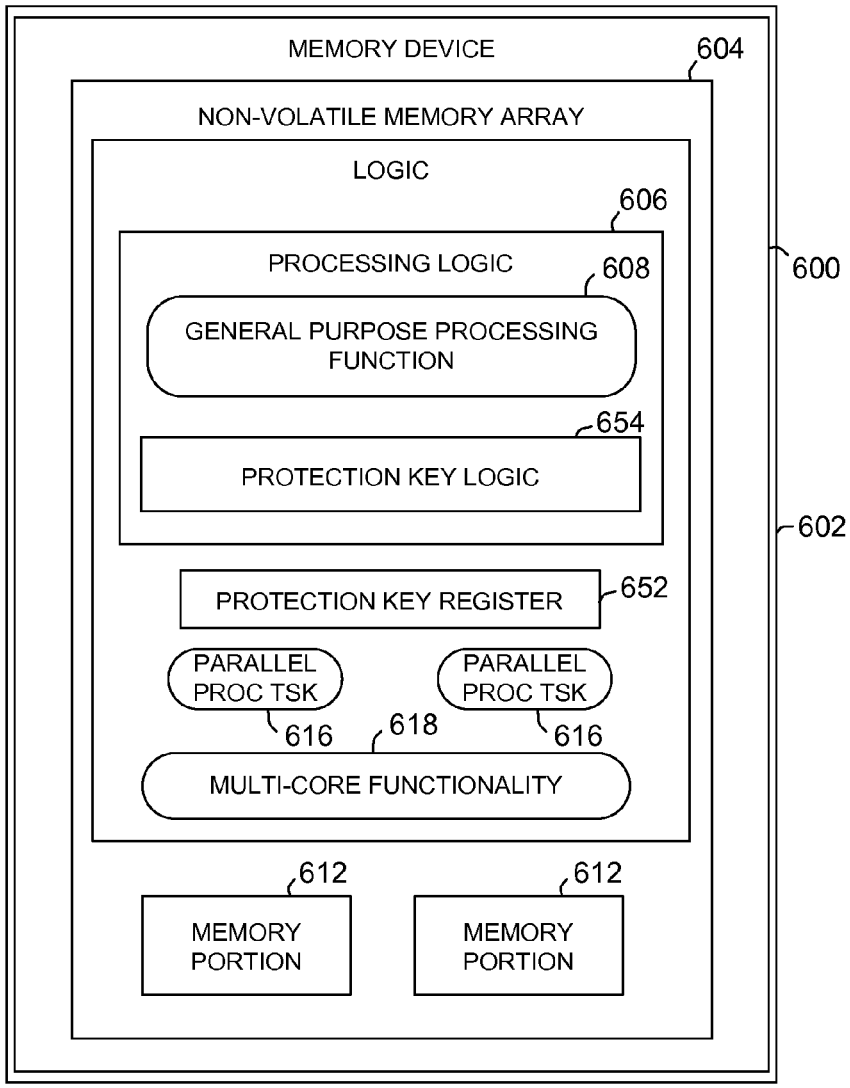

MEMORY DEVICE
604
NON-VOLATILE MEMORY ARRAY
LOGIC
606
PROCESSING LOGIC
608
GENERAL PURPOSE PROCESSING FUNCTION
654
PROTECTION KEY LOGIC
600
602
PROTECTION KEY REGISTER
652
PARALLEL PROC TSK
PARALLEL PROC TSK
616
618
616
MULTI-CORE FUNCTIONALITY
612
612
MEMORY PORTION
MEMORY PORTION

FIG. 6A

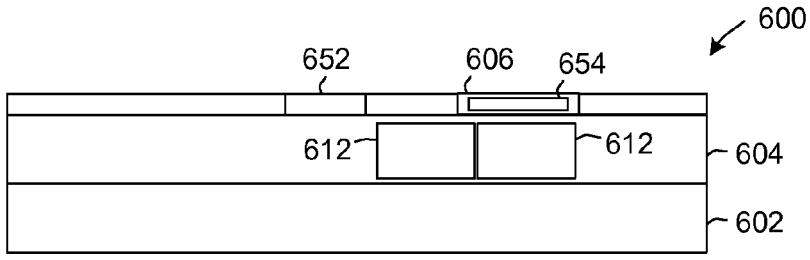

600
652
606
654
612
612
604
602

FIG. 6B

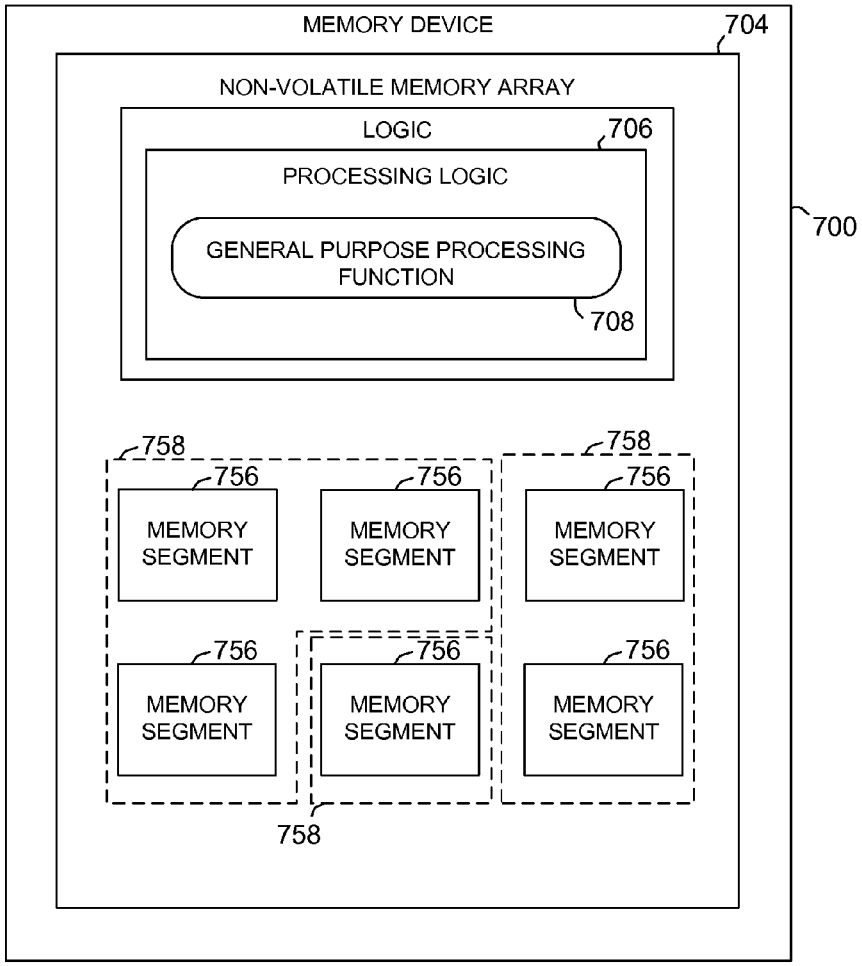

MEMORY DEVICE
704
NON-VOLATILE MEMORY ARRAY
LOGIC
706
PROCESSING LOGIC
GENERAL PURPOSE PROCESSING FUNCTION
708
700
758
756
MEMORY SEGMENT

FIG. 7A

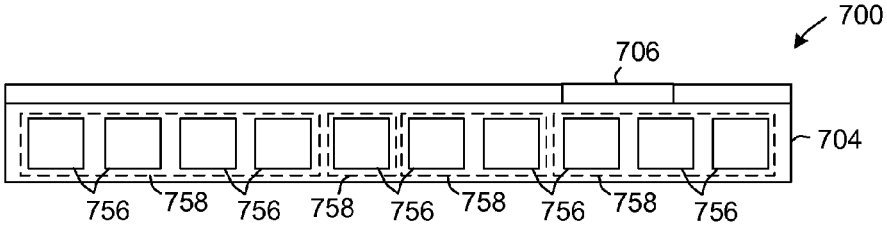

700
706
704
756
758

FIG. 7B

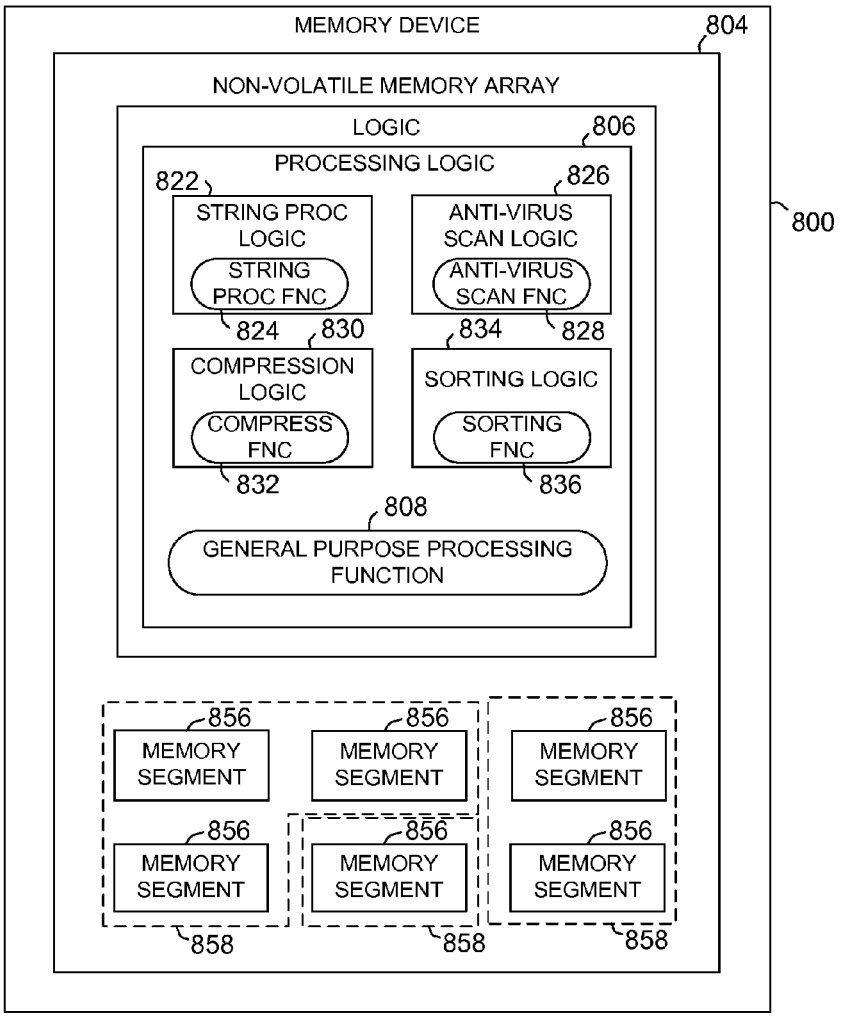

MEMORY DEVICE
804
NON-VOLATILE MEMORY ARRAY
LOGIC
806
PROCESSING LOGIC
822
826
STRING PROC LOGIC
STRING PROC FNC
ANTI-VIRUS SCAN LOGIC
ANTI-VIRUS SCAN FNC
824
830
834
828
COMPRESSION LOGIC
COMPRESS FNC
SORTING LOGIC
SORTING FNC
832
836
808
GENERAL PURPOSE PROCESSING FUNCTION
856
MEMORY SEGMENT
858
800

FIG. 8A

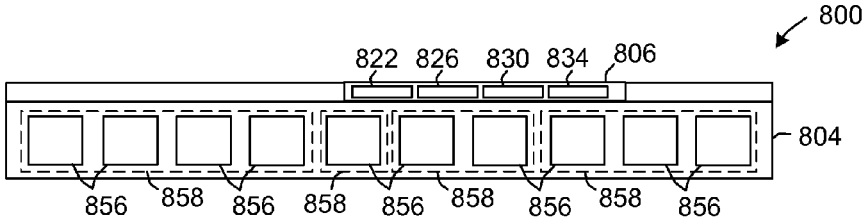

800
822
826
830
834
806
804
856
858

FIG. 8B

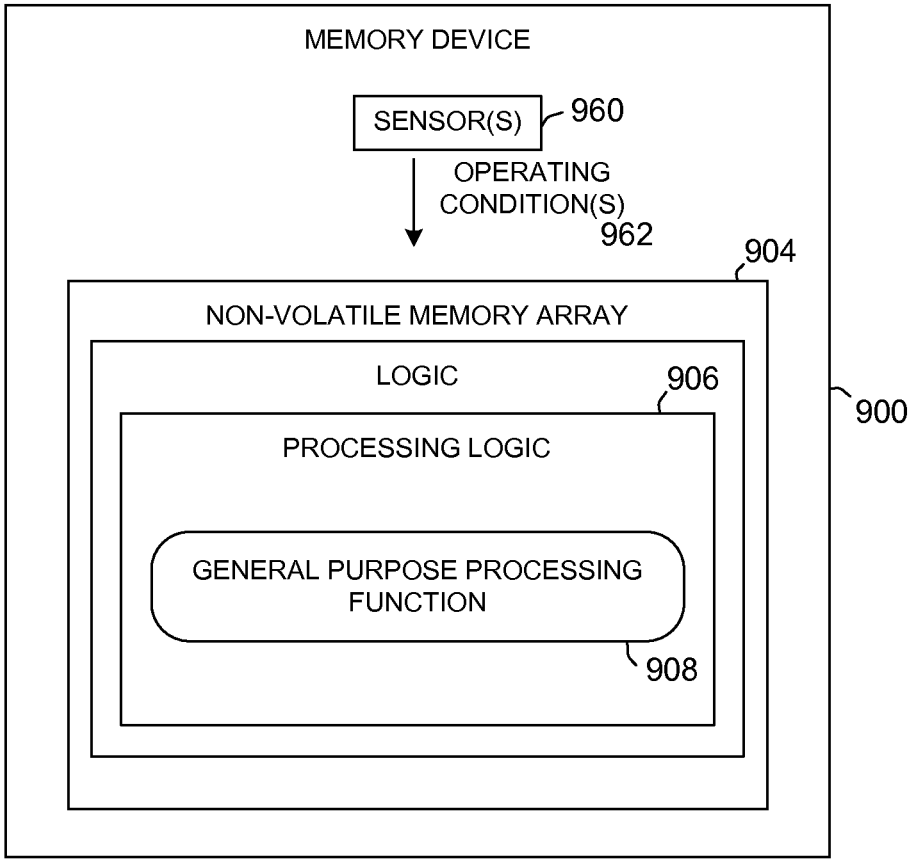

MEMORY DEVICE
SENSOR(S)
960
OPERATING CONDITION(S)
962
904
NON-VOLATILE MEMORY ARRAY
LOGIC
906
PROCESSING LOGIC
GENERAL PURPOSE PROCESSING FUNCTION
908
900

FIG. 9A

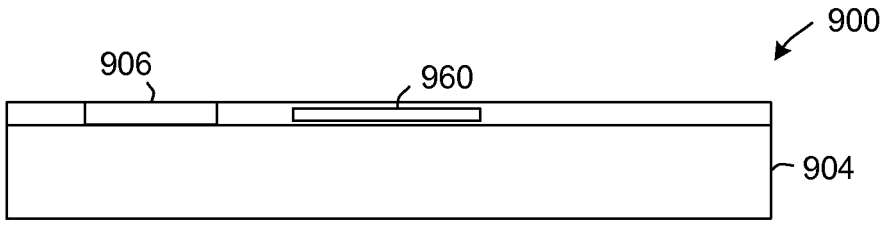

900
906
960
904

FIG. 9B

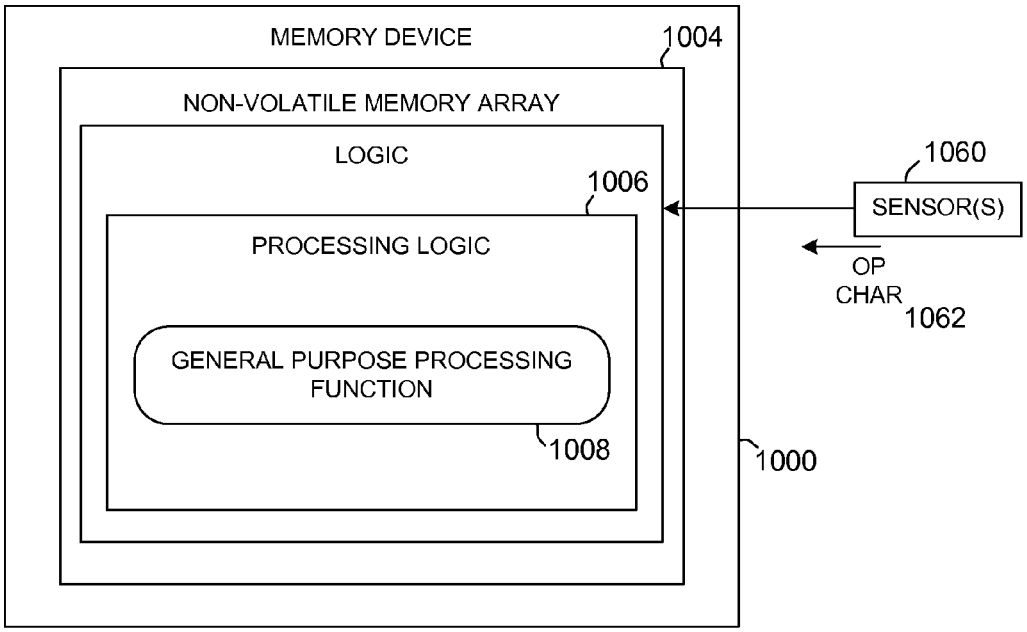


FIG. 10A

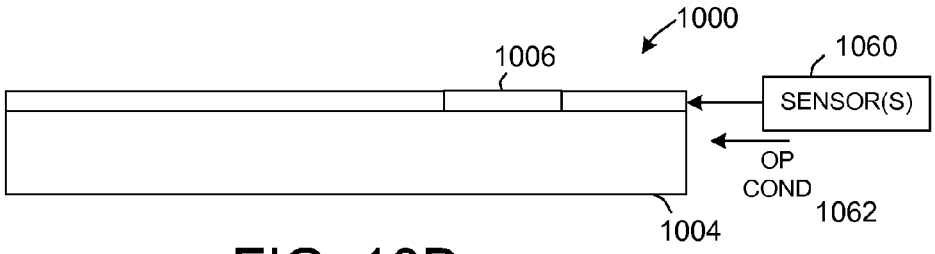


FIG. 10B

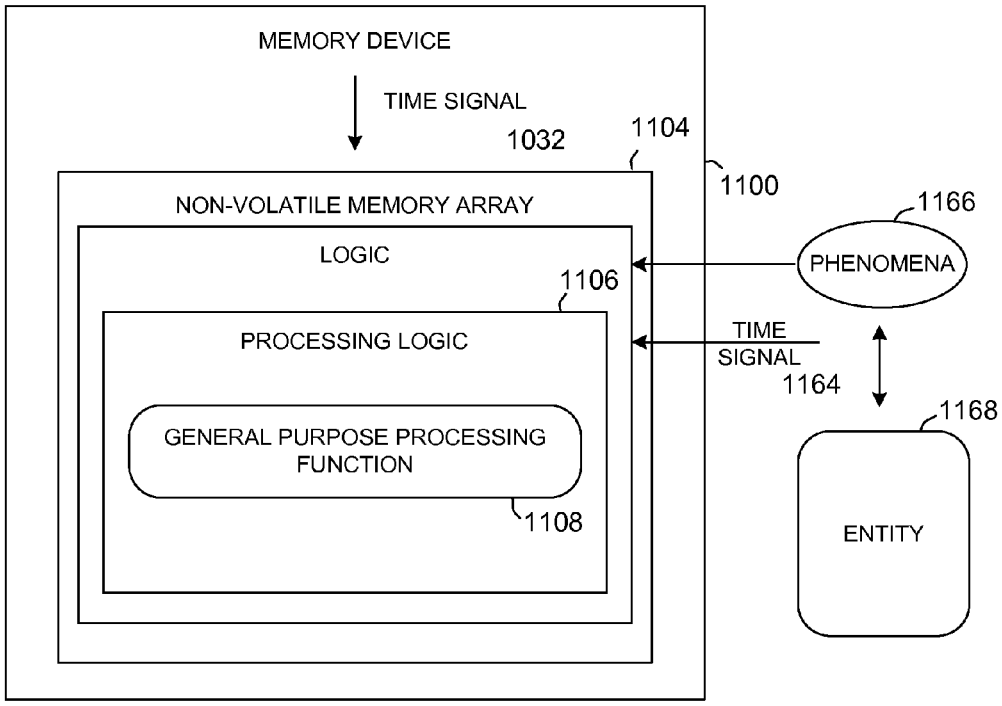


FIG. 11A

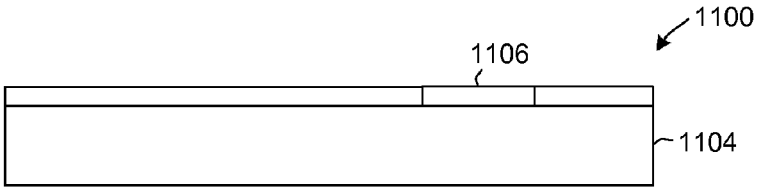


FIG. 11B

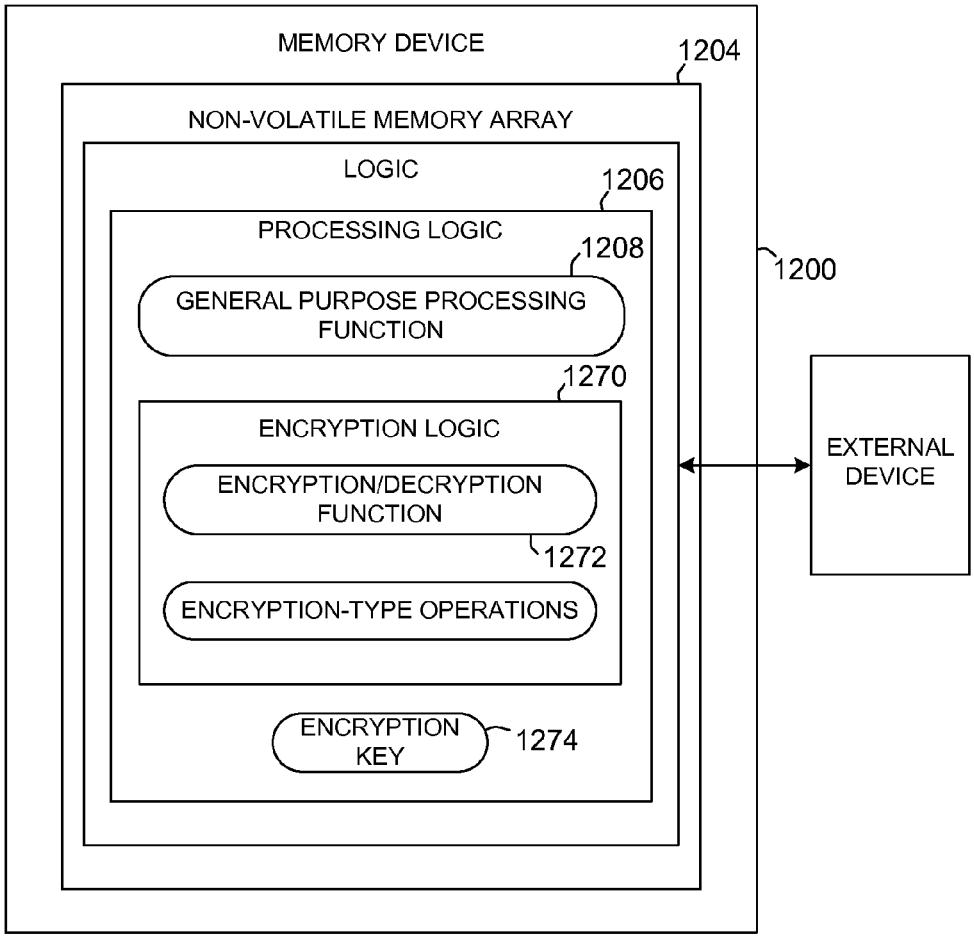


FIG. 12A

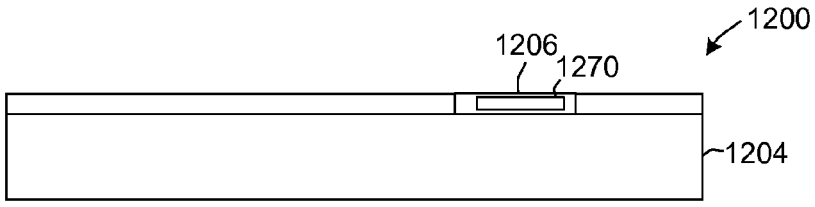


FIG. 12B

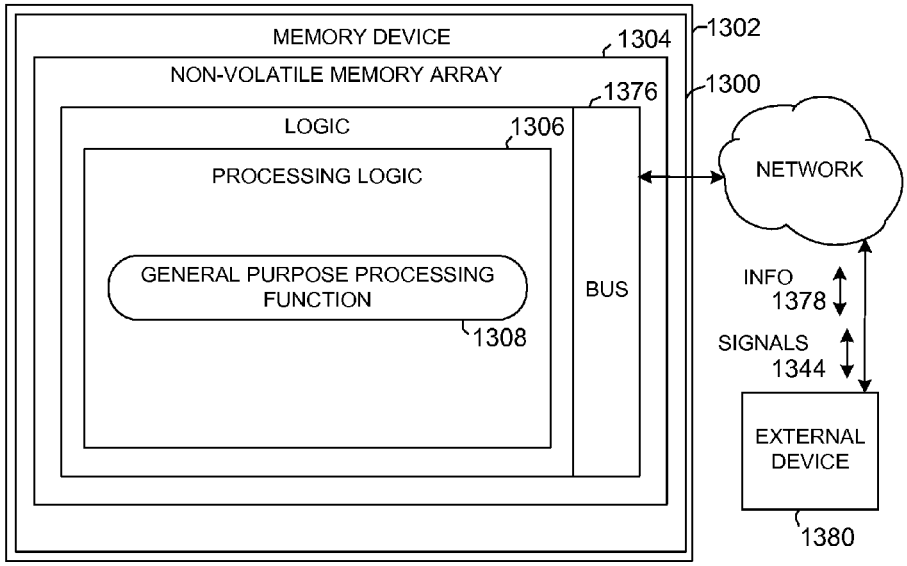


FIG. 13A

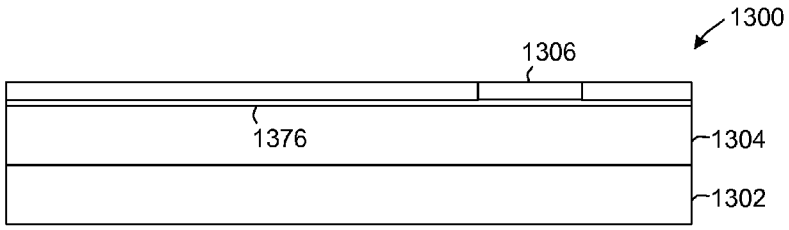


FIG. 13B

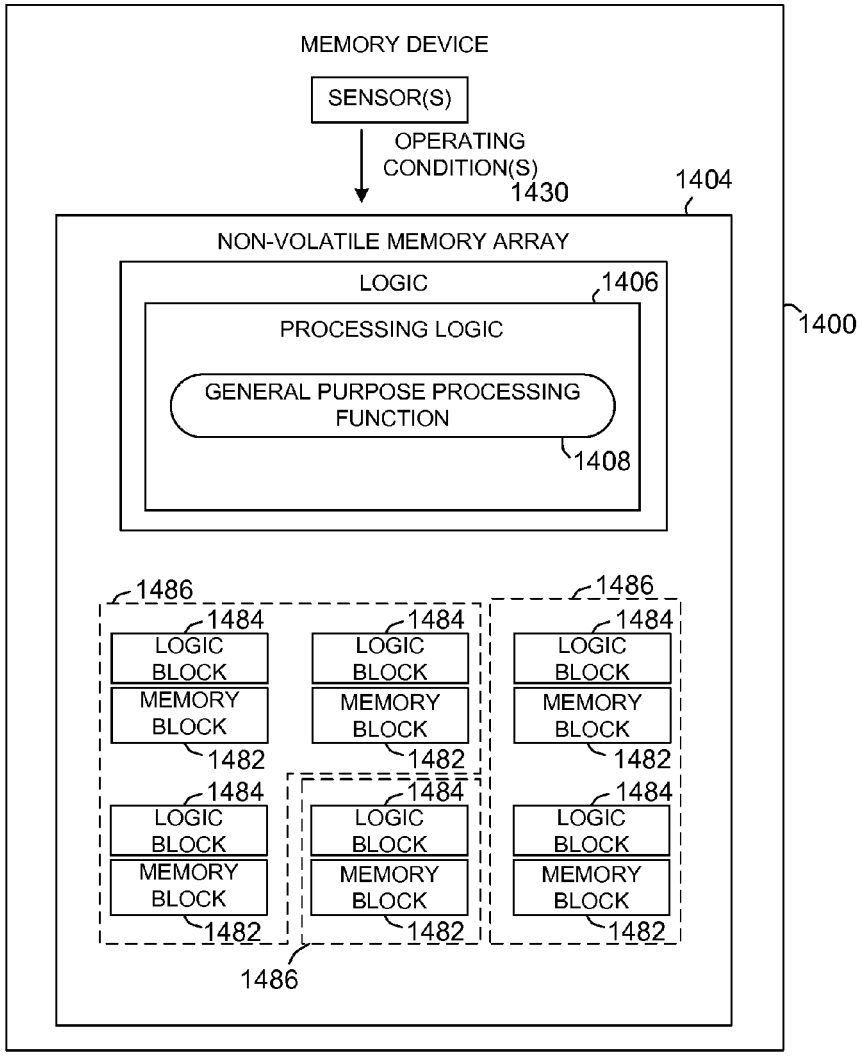


FIG. 14A

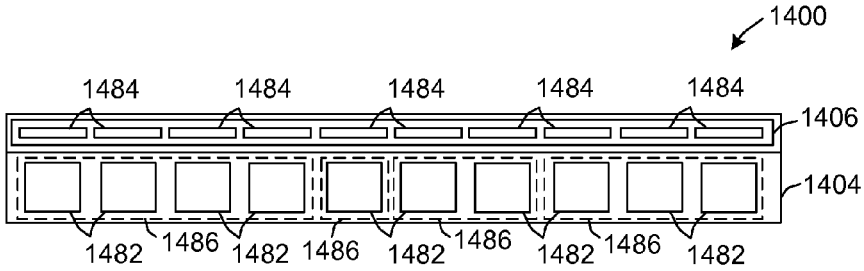


FIG. 14B

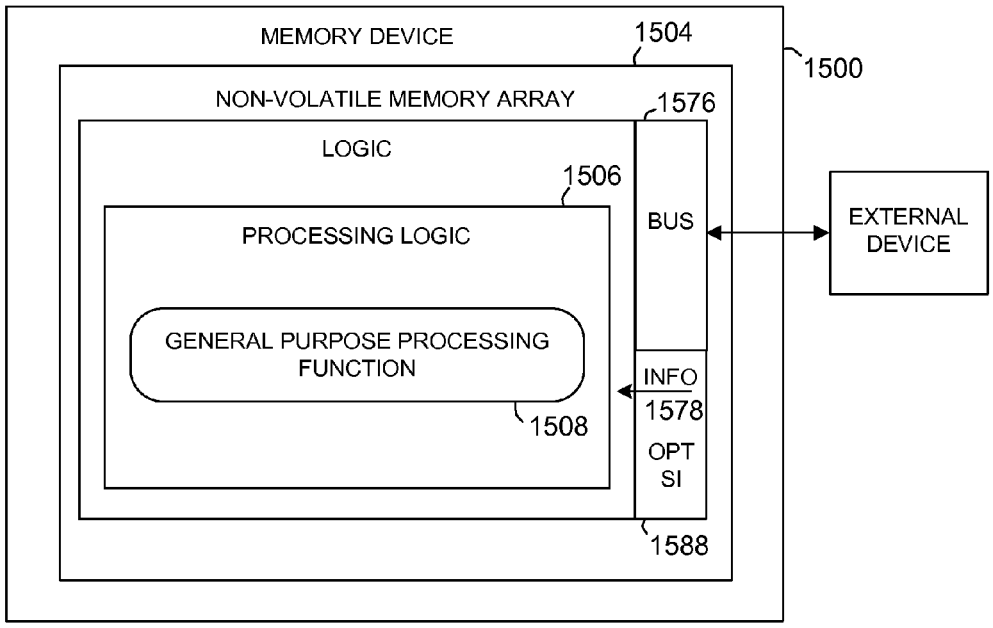


FIG. 15A

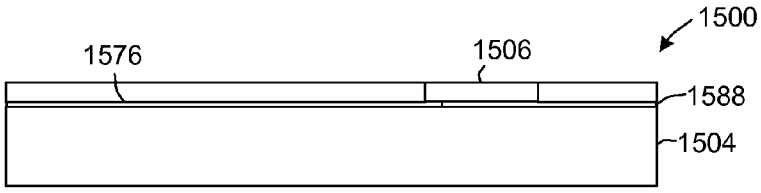


FIG. 15B

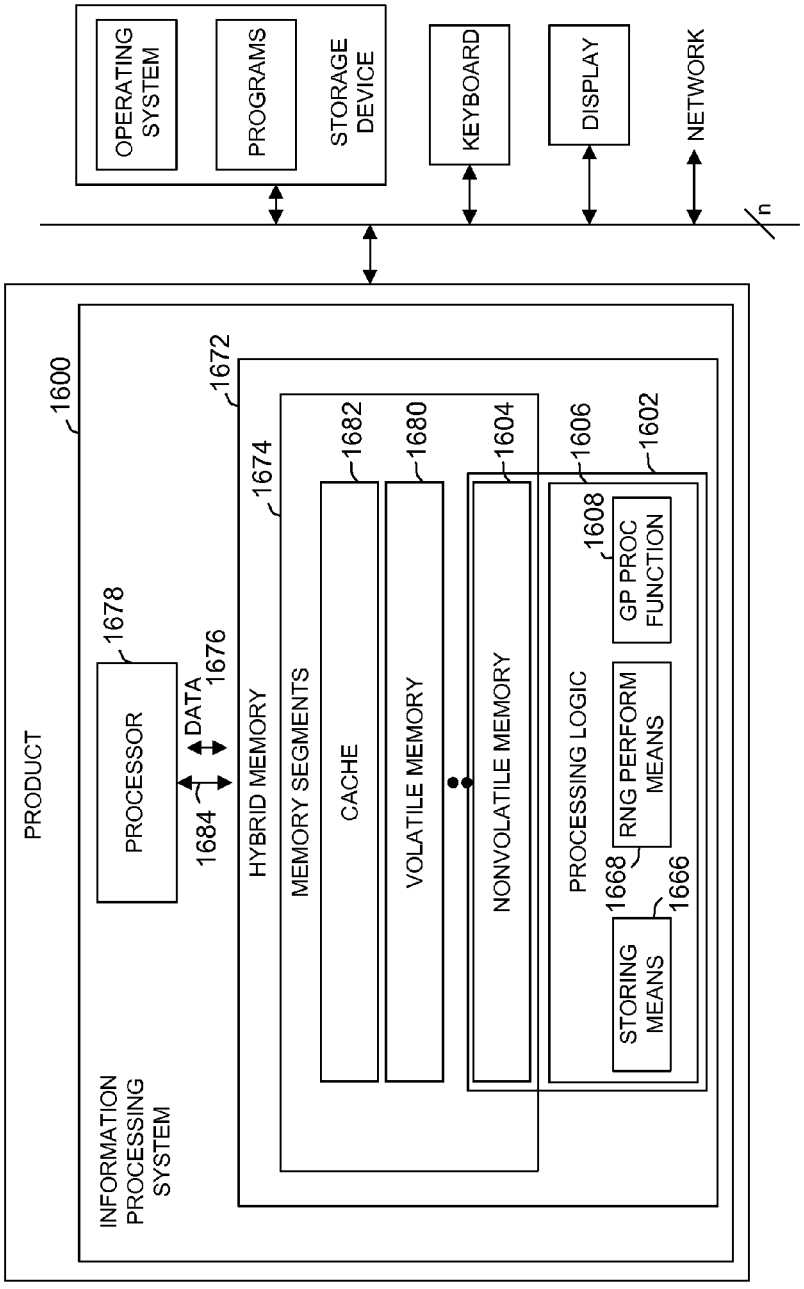

OPERATING SYSTEM
PROGRAMS
STORAGE DEVICE
KEYBOARD
DISPLAY
NETWORK
n
PRODUCT
1600
INFORMATION PROCESSING SYSTEM
PROCESSOR
1678
DATA
1676
1684
1672
HYBRID MEMORY
1674
MEMORY SEGMENTS
CACHE
1682
VOLATILE MEMORY
1680
NONVOLATILE MEMORY
1604
PROCESSING LOGIC
1606
1602
GP PROC FUNCTION
1608
RNG PERFORM MEANS
STORING MEANS
1668
1666

FIG. 16

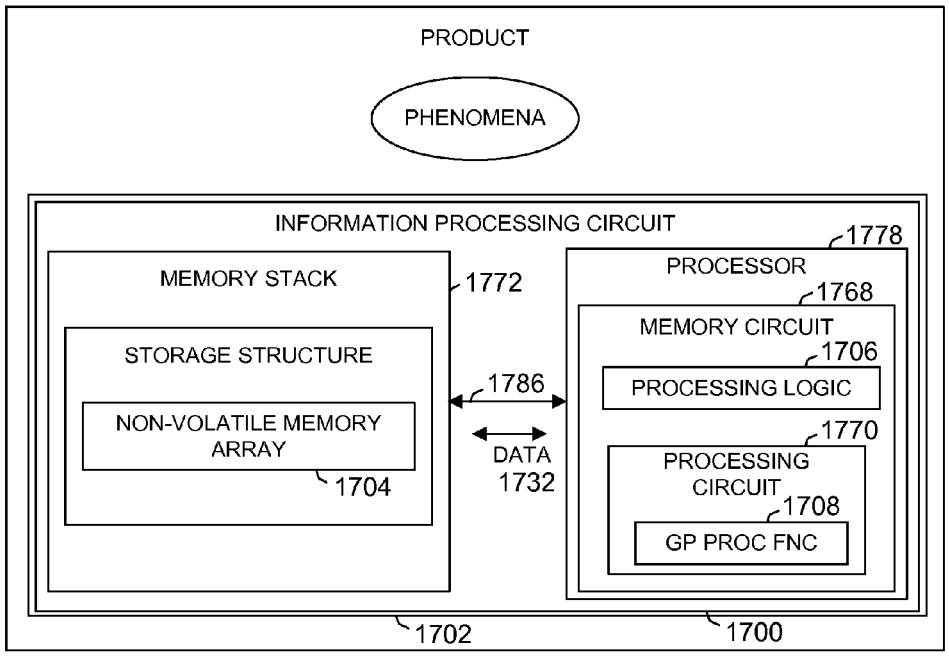


FIG. 17A

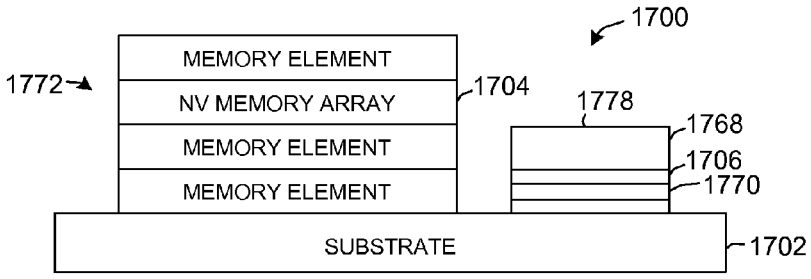


FIG. 17B

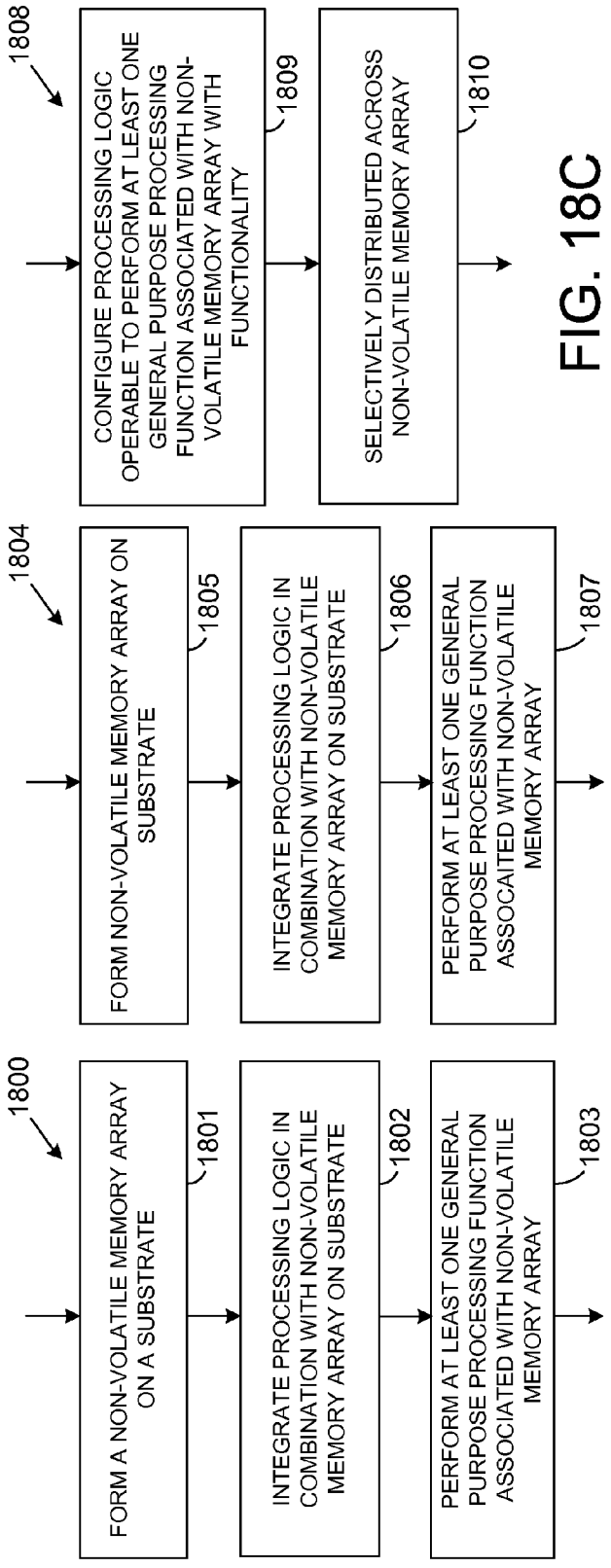


FIG. 18A

FIG. 18B

FIG. 18C

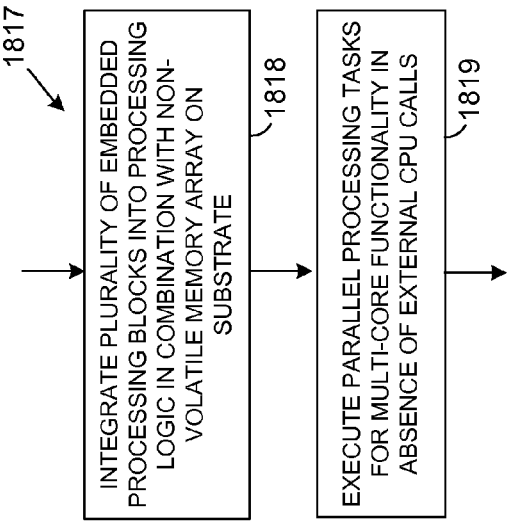


FIG. 18D

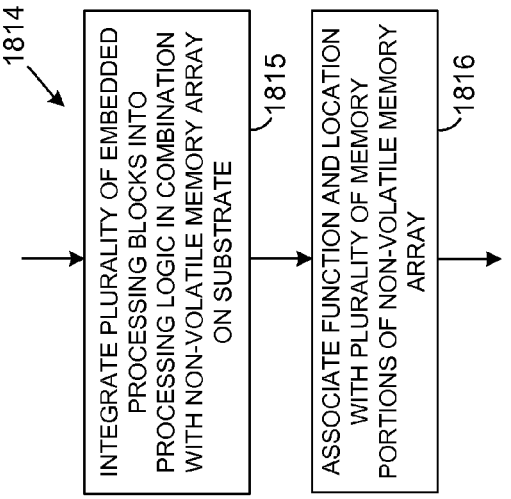


FIG. 18E

FIG. 18F

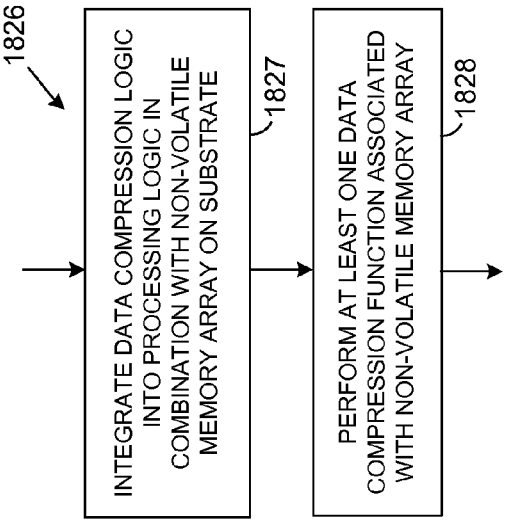


FIG. 18G

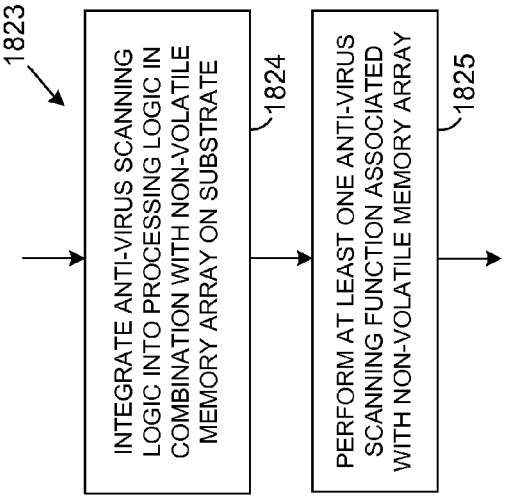


FIG. 18H

FIG. 18I

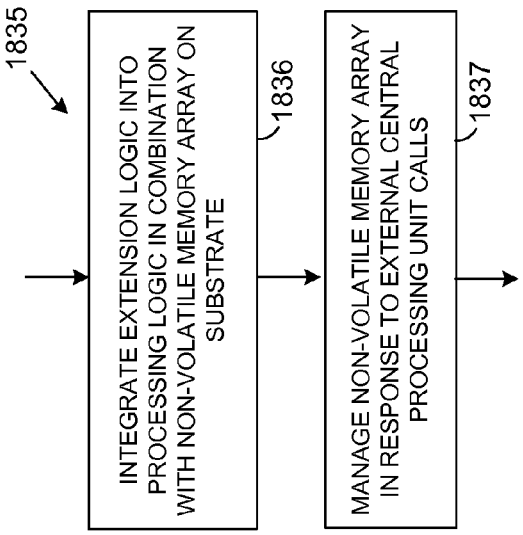


FIG. 18L

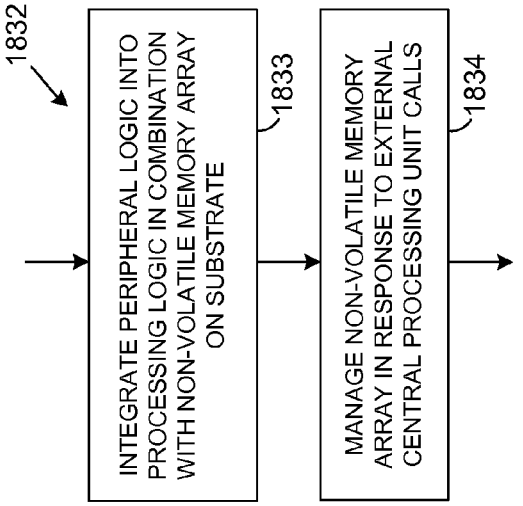


FIG. 18K

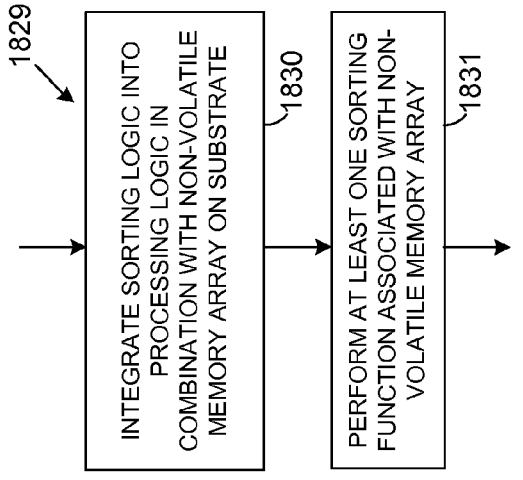


FIG. 18J

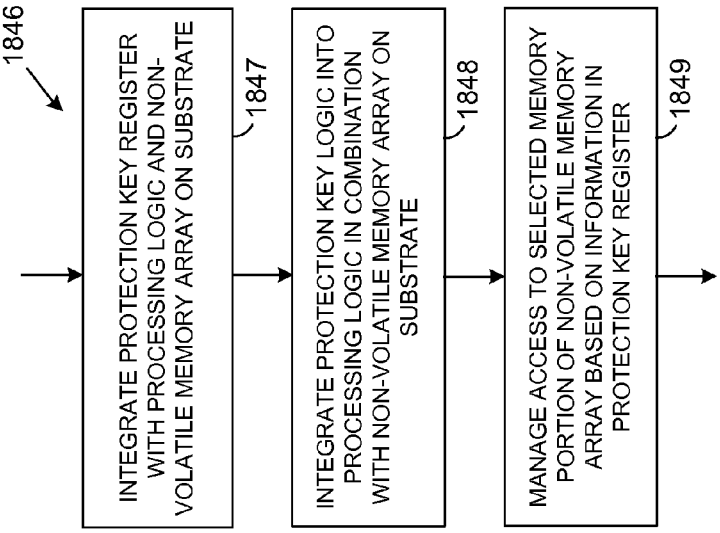


FIG. 18M

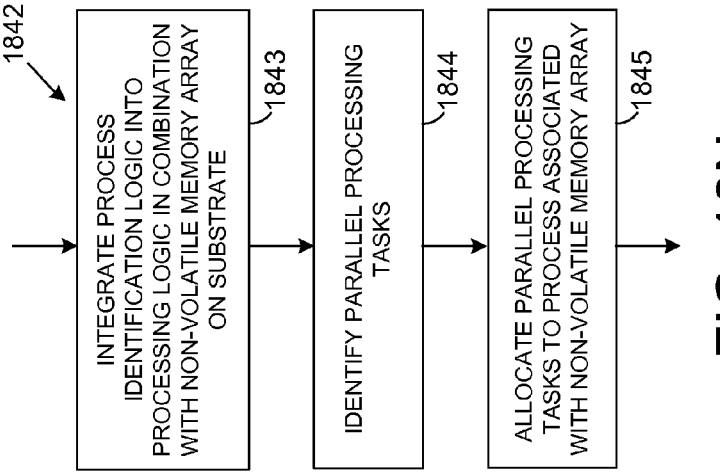


FIG. 18N

FIG. 18O

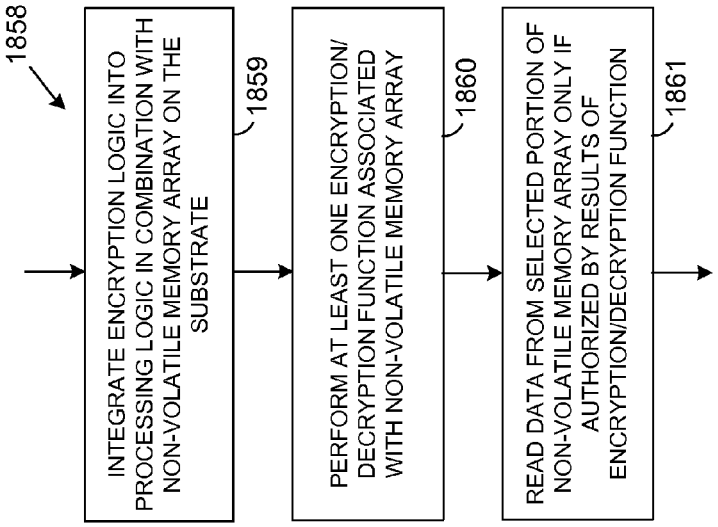


FIG. 18R

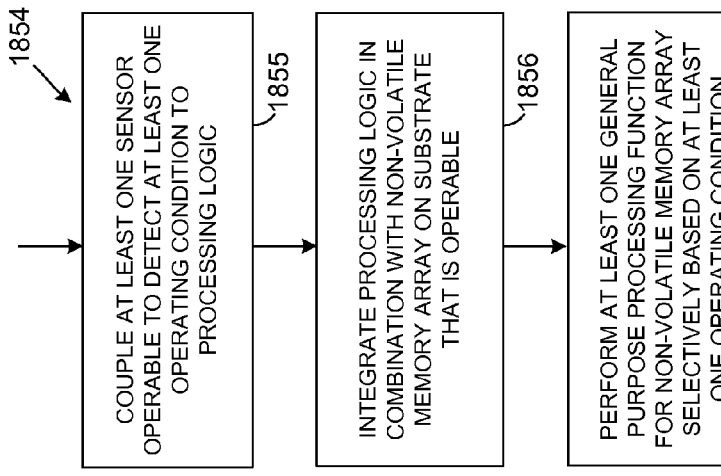


FIG. 18Q

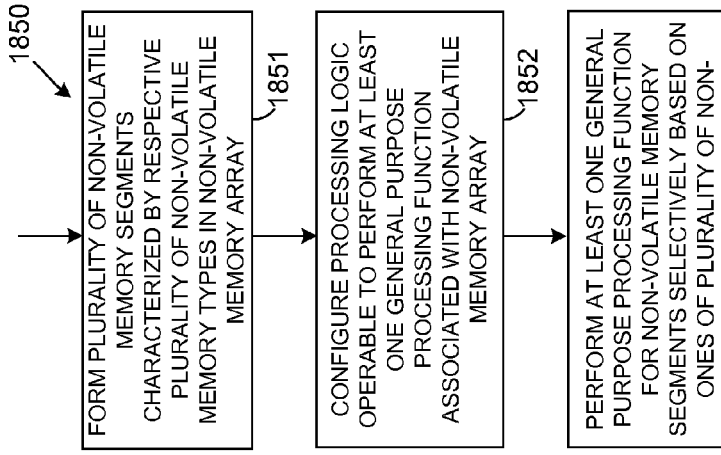


FIG. 18P

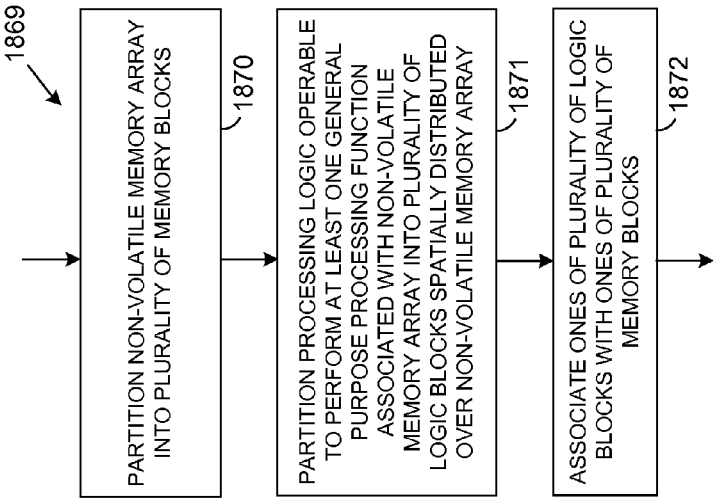


FIG. 18U

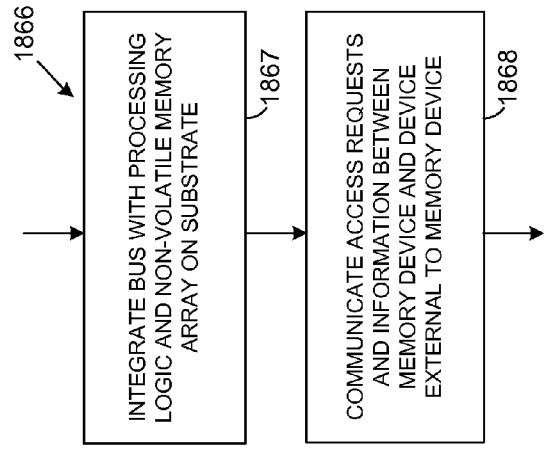


FIG. 18T

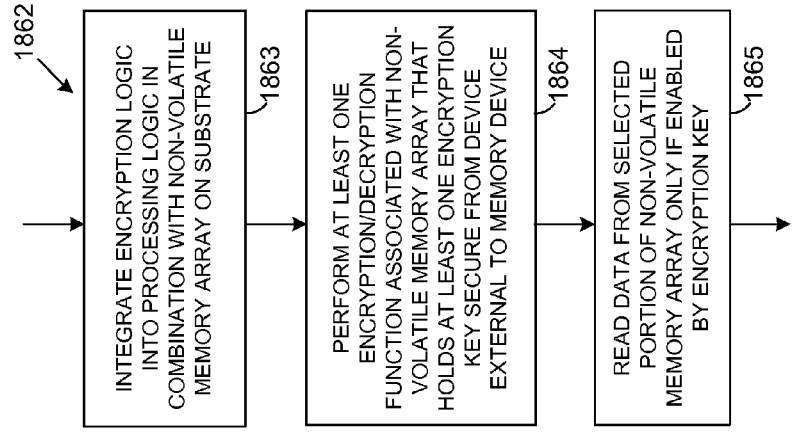


FIG. 18S

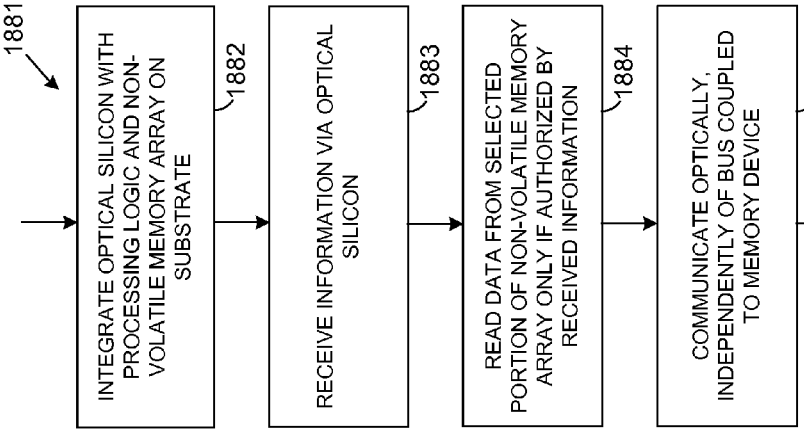


FIG. 18X

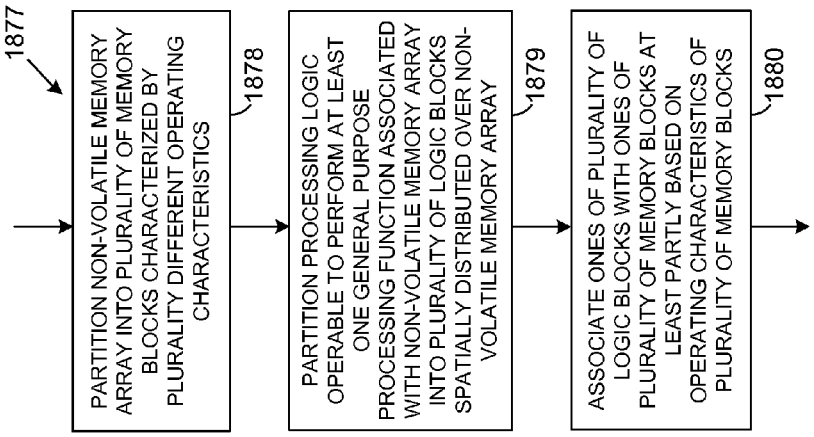


FIG. 18W

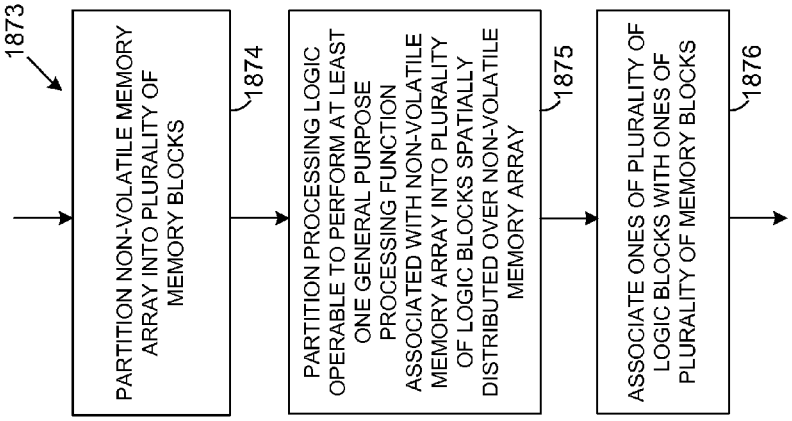


FIG. 18V

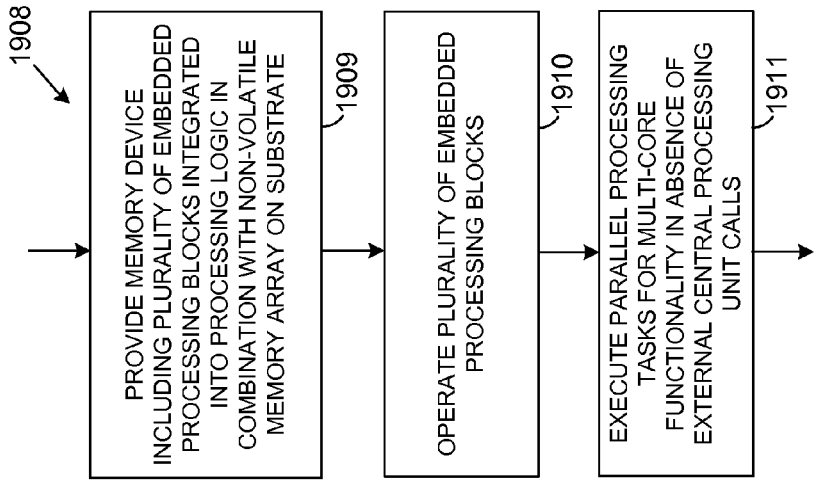


FIG. 19C

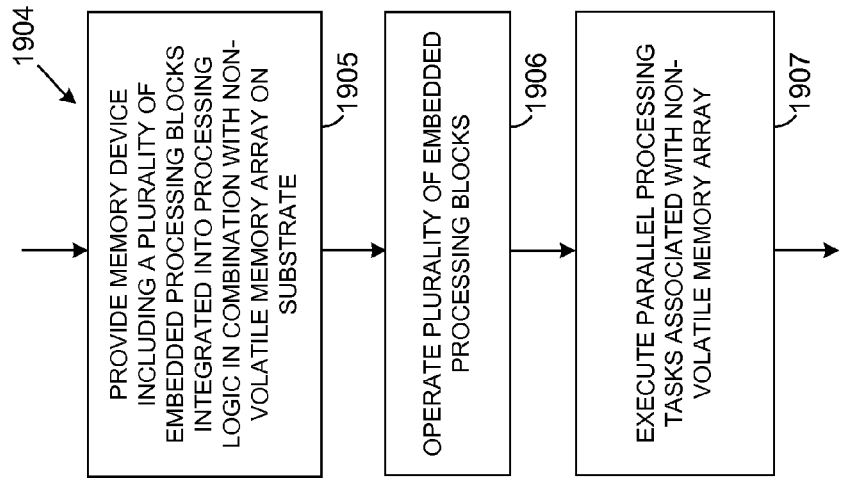


FIG. 19B

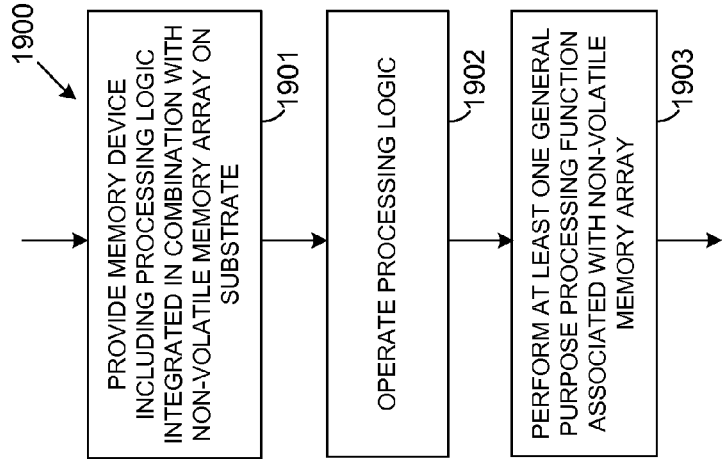


FIG. 19A

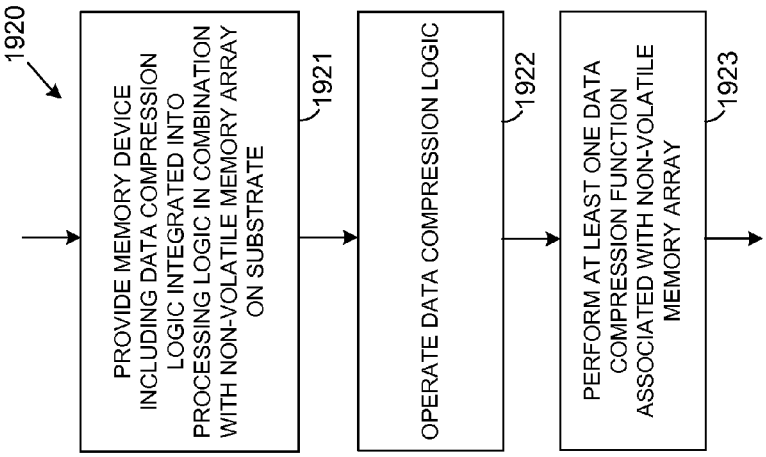


FIG. 19F

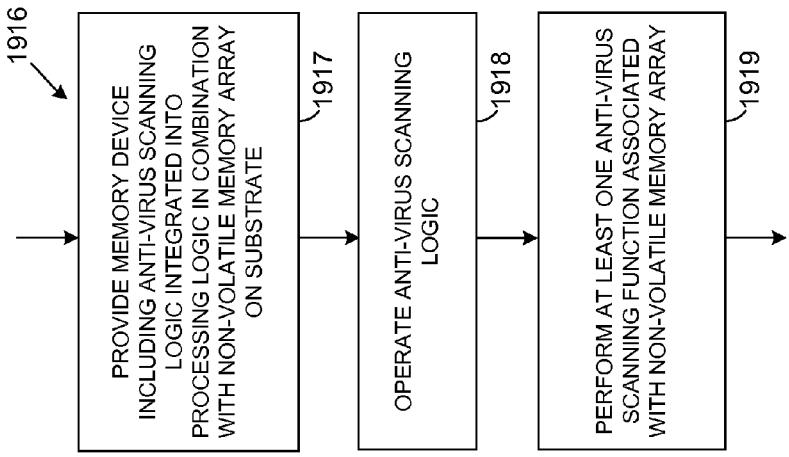


FIG. 19E

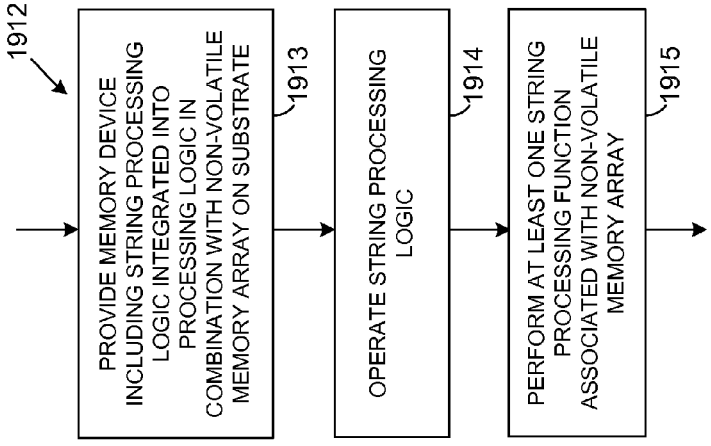


FIG. 19D

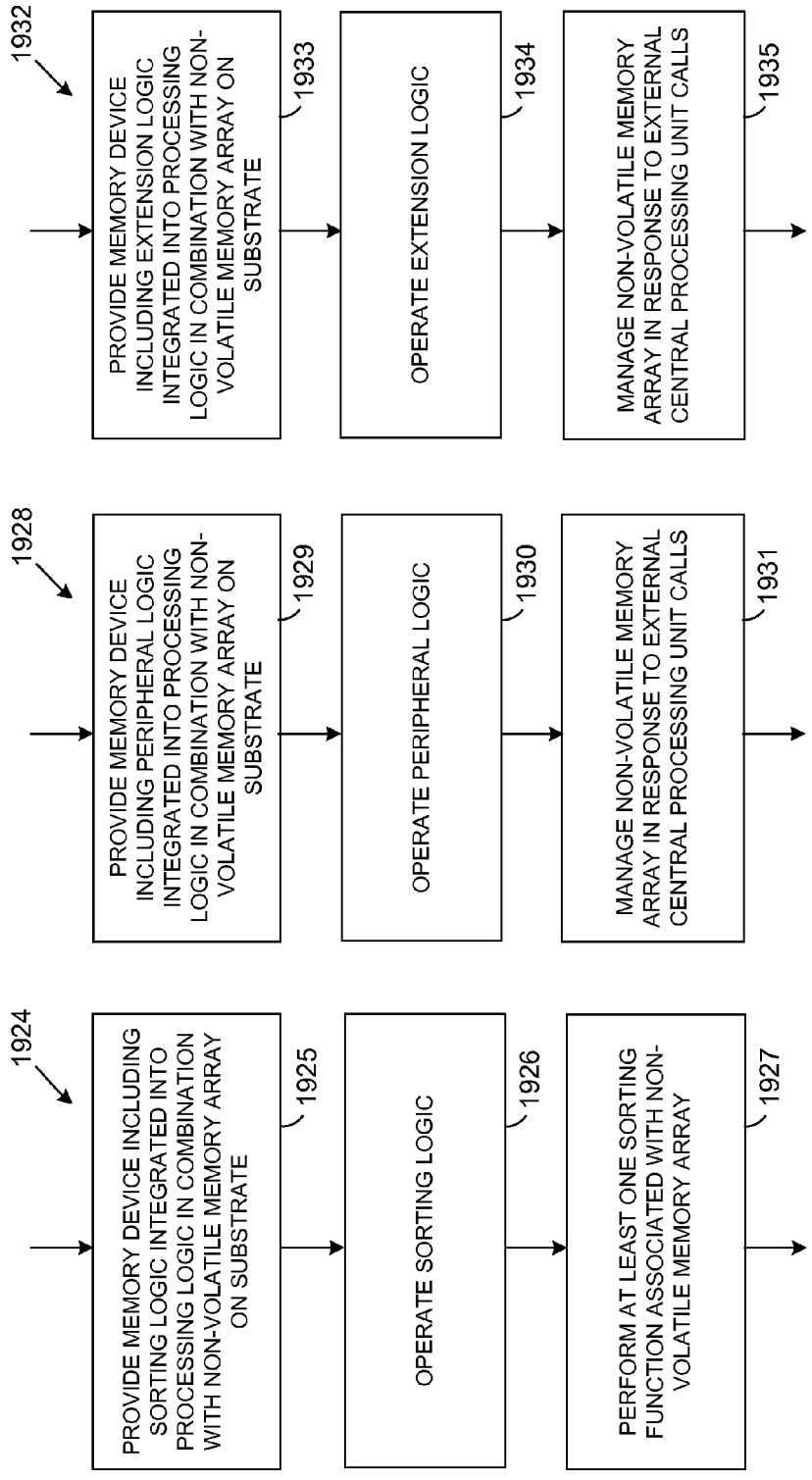


FIG. 19G

FIG. 19H

FIG. 19I

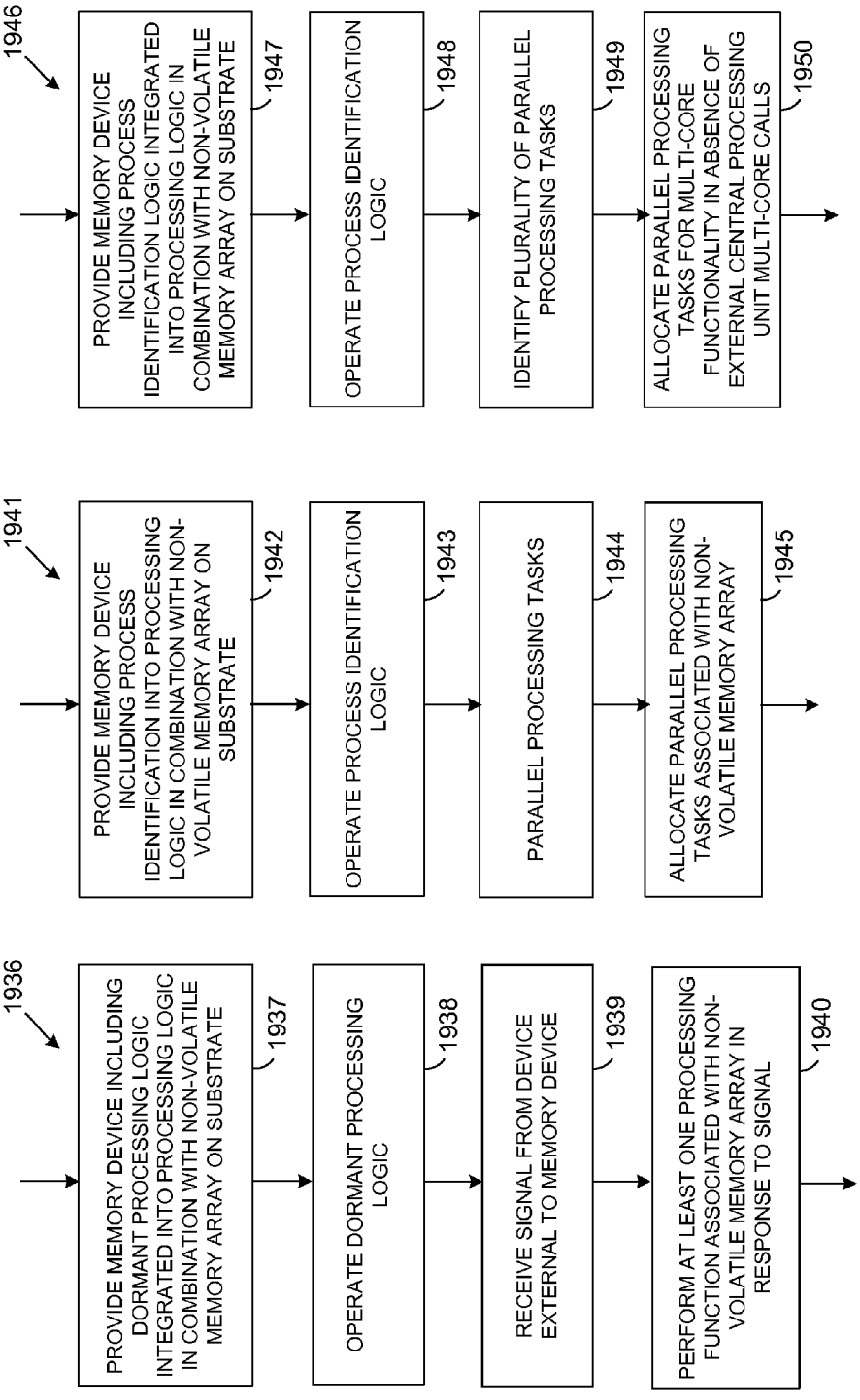


FIG. 19J

FIG. 19K

FIG. 19L

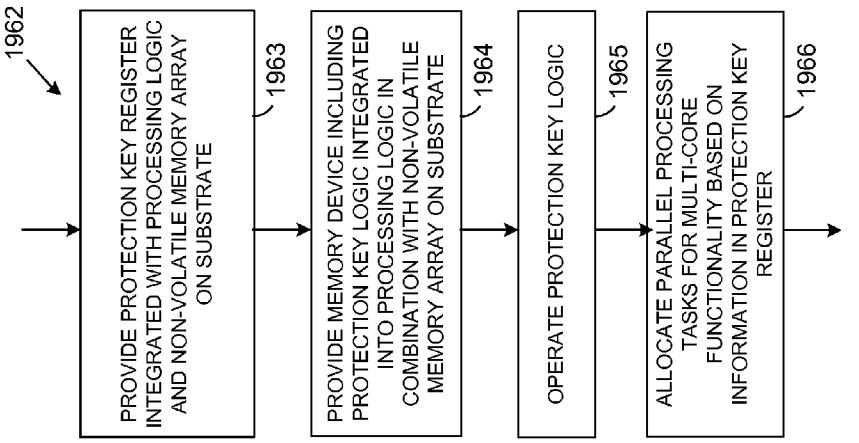


FIG. 19O

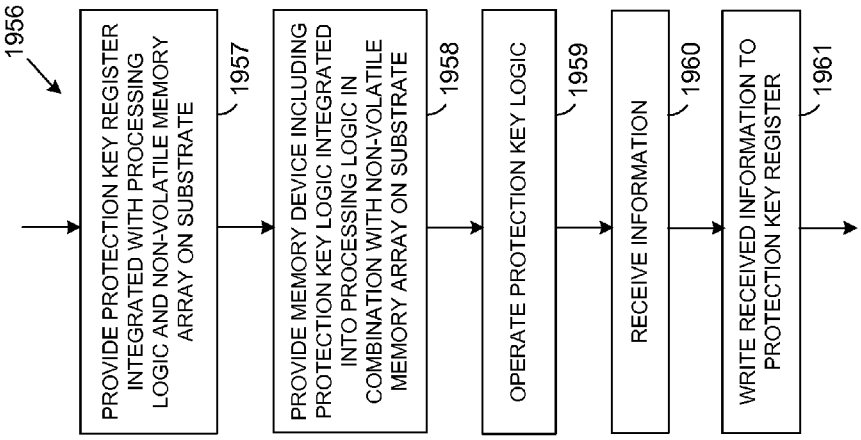


FIG. 19N

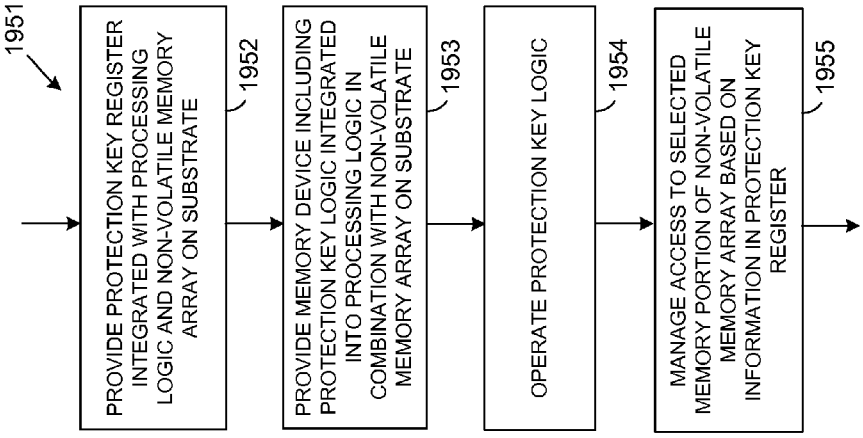


FIG. 19M

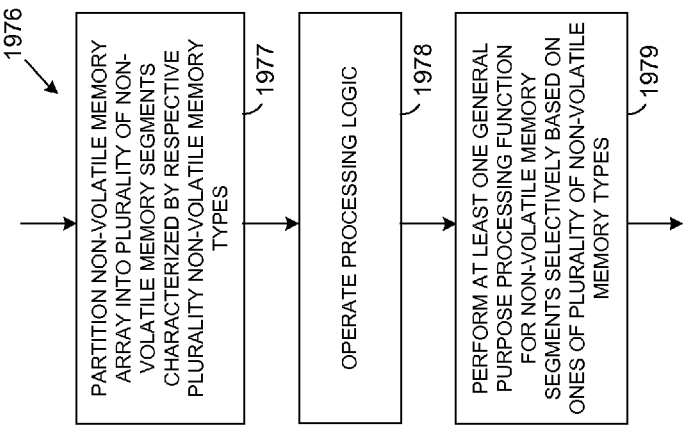


FIG. 19R

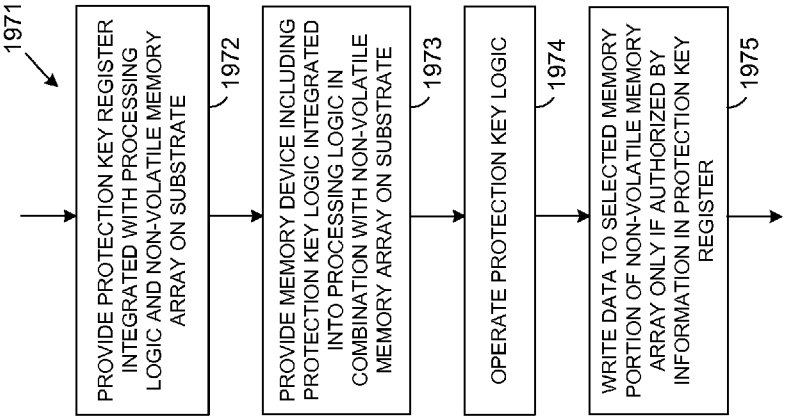


FIG. 19Q

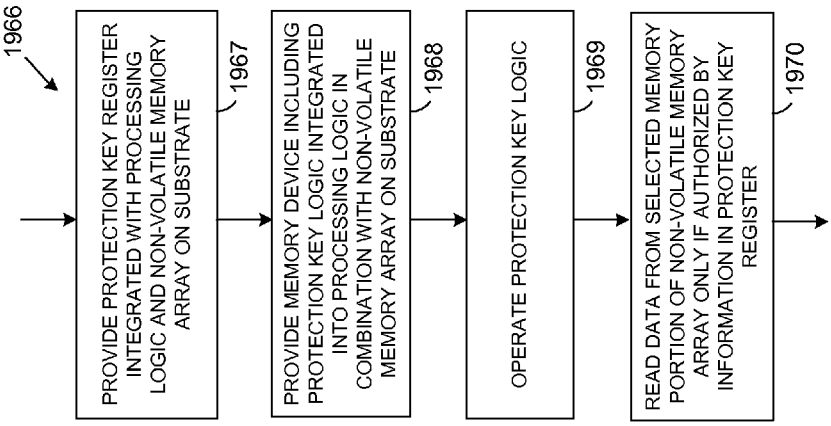


FIG. 19P

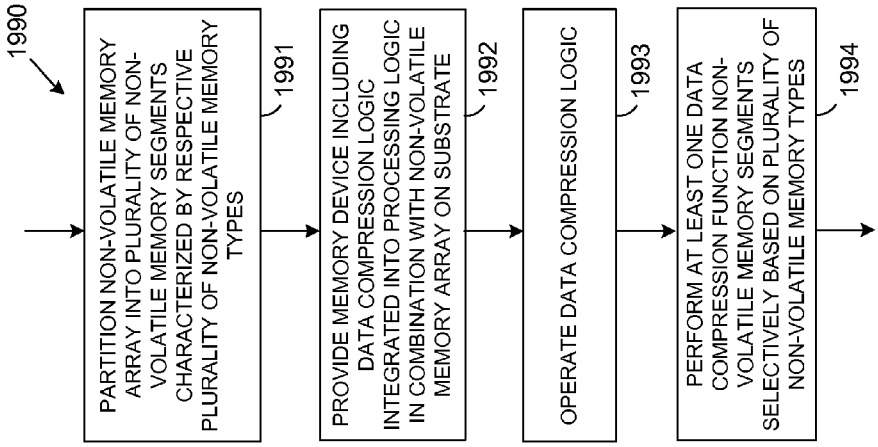


FIG. 19U

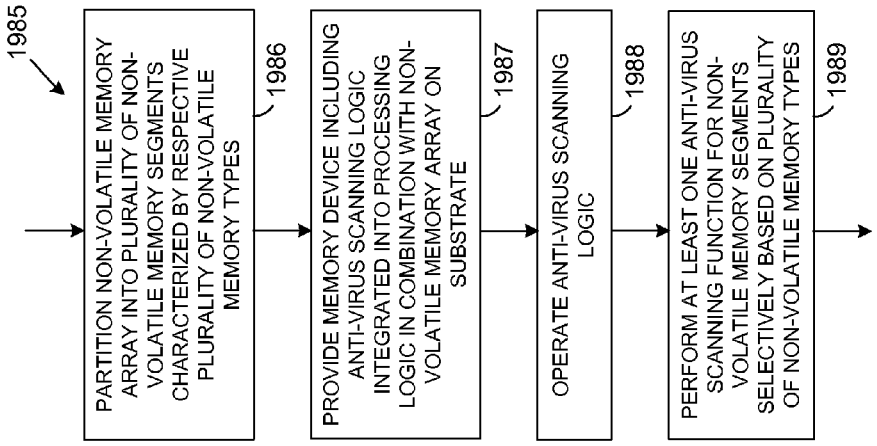


FIG. 19T

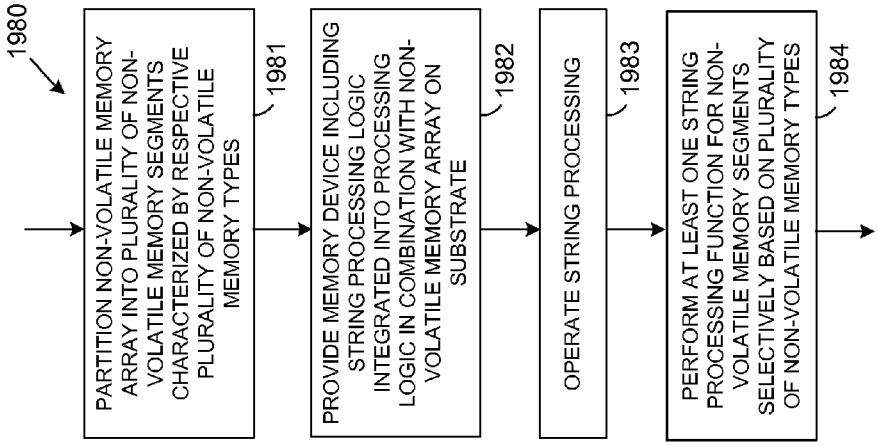


FIG. 19S

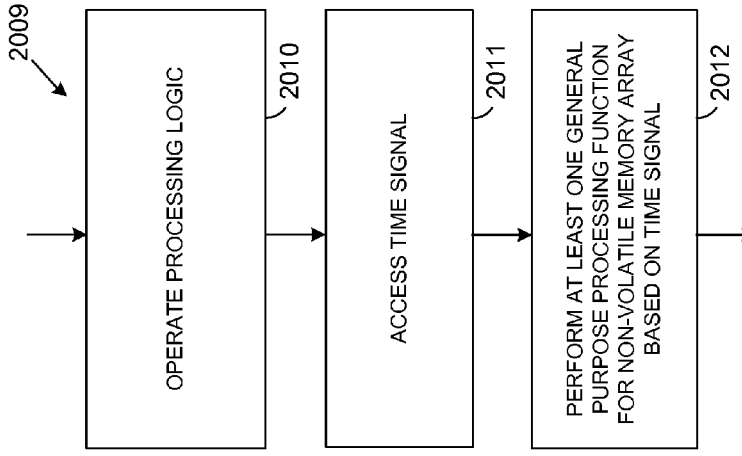


FIG. 20C

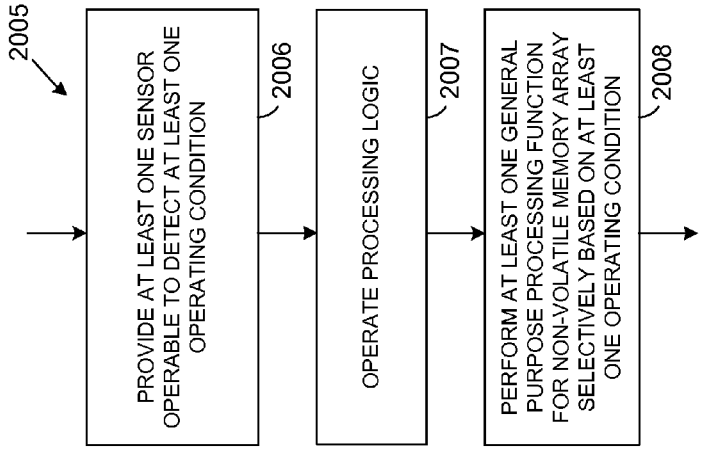


FIG. 20B

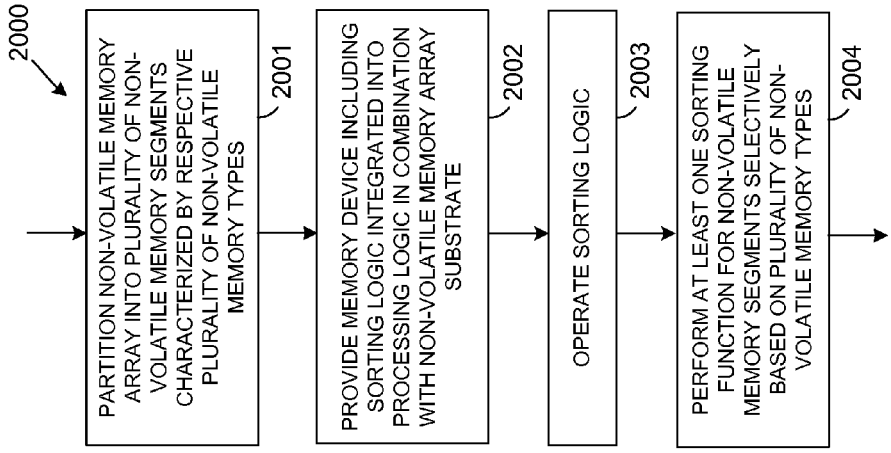


FIG. 20A

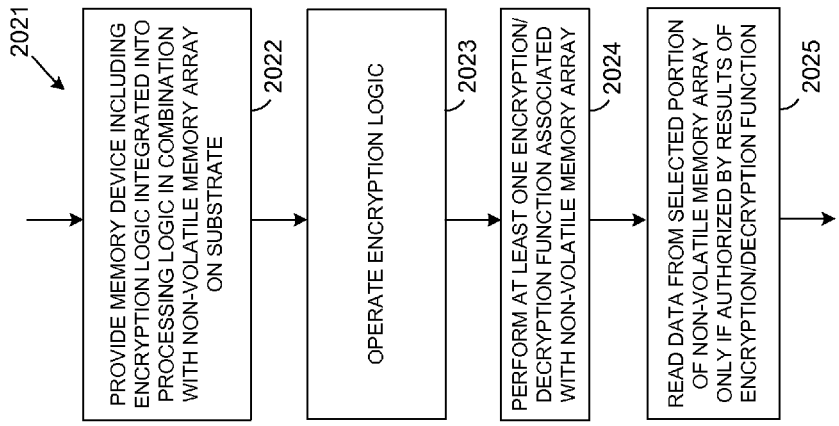


FIG. 20D

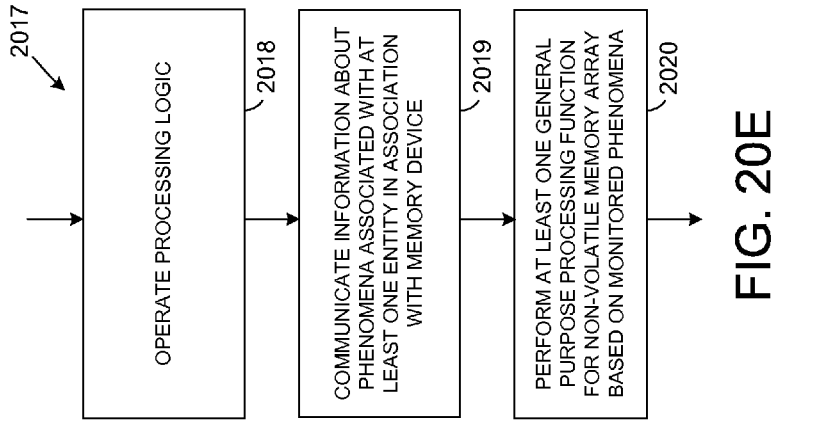


FIG. 20E

FIG. 20F

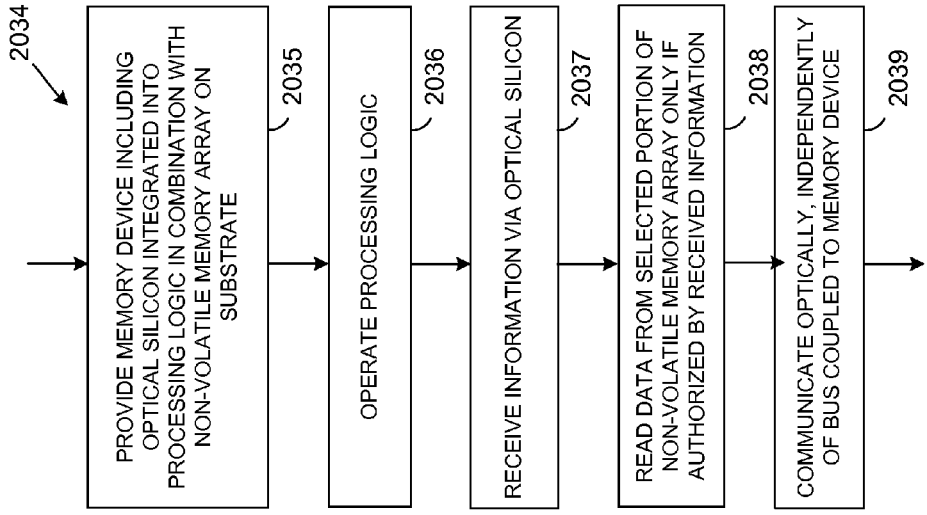


FIG. 20G

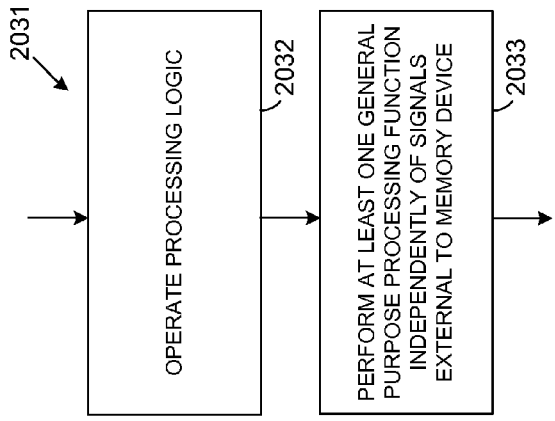


FIG. 20H

FIG. 20I

MULTI-CORE PROCESSING IN MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to and/or claims the benefit of the earliest available effective filing date(s) from the following listed application(s) (the "Priority Applications"), if any, listed below (e.g., claims earliest available priority dates for other than provisional patent applications or claims benefits under 35 USC §119(e) for provisional patent applications, for any and all parent, grandparent, great-grandparent, etc. applications of the Priority Application(s)). In addition, the present application is related to the "Related Applications," if any, listed below.

Priority Applications

[0002] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/678,430 entitled Intelligent Monitoring for Computation in Memory, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 15 Nov. 2012 with attorney docket no. SE1-0765-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date;

[0003] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/687,983 entitled Error Correction with Non-Volatile Memory on an Integrated Circuit, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 28 Nov. 2012 with attorney docket no. SE1-0766-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date; and

[0004] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/678,439 entitled Redundancy for Loss-Tolerant Data in Non-Volatile Memory, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 15 Nov. 2012 with attorney docket no. SE1-0767-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date;

[0005] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/691,448 entitled Flexible Processors and Flexible Memory, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 30 Nov. 2012 with attorney docket no. SE1-0768-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date; and

[0006] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/725,788 entitled Random Number Generator Functions in Memory, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 21 Dec. 2012 with attorney docket no. SE1-0800-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date.

[0007] For purposes of the USPTO extra-statutory requirements, the present application constitutes a continuation-in-part of U.S. patent application Ser. No. 13/738,747 entitled Data Security and Access Tracking in Memory, naming Roderick Hyde, Nicholas Pasch, and Clarence T. Tegreene as inventors, filed 10 Jan. 2013 with attorney docket no. SE1-0801-US, which is currently co-pending or is an application of which a currently co-pending application is entitled to the benefit of the filing date.

RELATED APPLICATIONS

[0008] None.

[0009] The United States Patent Office (USPTO) has published a notice to the effect that the USPTO's computer programs require that patent applicants reference both a serial number and indicate whether an application is a continuation, continuation-in-part, or divisional of a parent application. Stephen G. Kunin, Benefit of Prior-Filed Application, USPTO Official Gazette Mar. 18, 2003. The USPTO further has provided forms for the Application Data Sheet which allow automatic loading of bibliographic data but which require identification of each application as a continuation, continuation-in-part, or divisional of a parent application. The present Applicant Entity (hereinafter "Applicant") has provided above a specific reference to the application(s) from which priority is being claimed as recited by statute. Applicant understands that the statute is unambiguous in its specific reference language and does not require either a serial number or any characterization, such as "continuation" or "continuation-in-part," for claiming priority to U.S. patent applications. Notwithstanding the foregoing, Applicant understands that the USPTO's computer programs have certain data entry requirements, and hence Applicant has provided designation (s) of a relationship between the present application and its parent application(s) as set forth above and in any ADS filed in this application, but expressly points out that such designation(s) are not to be construed in any way as any type of commentary and/or admission as to whether or not the present application contains any new matter in addition to the matter of its parent application(s).

[0010] If the listings of applications provided above are inconsistent with the listings provided via an ADS, it is the intent of the Applicant to claim priority to each application that appears in the Priority Applications section of the ADS and to each application that appears in the Priority Applications section of this application.

[0011] All subject matter of the Priority Applications and the Related Applications and of any and all parent, grandparent, great-grandparent, etc. applications of the Priority Applications and the Related Applications, including any priority claims, is incorporated herein by reference to the extent such subject matter is not inconsistent herewith.

TECHNICAL FIELD

[0012] The present disclosure relates to electronic memory and systems associated with electronic memory.

SUMMARY

[0013] In one aspect, a memory device includes but is not limited to a substrate, a non-volatile memory array integrated on the substrate, and processing logic integrated with the non-volatile memory array on the substrate. The processing logic is operable to perform at least one general purpose processing function associated with the non-volatile memory array. In addition to the foregoing, other aspects are described in the claims, drawings, and text forming a part of the present disclosure.

[0014] In one aspect, an information processing system includes but is not limited to a means for storing information including processing logic integrated in combination with non-volatile memory array integrated on a substrate, and means for performing at least one general purpose processing function associated with the non-volatile memory array. In addition to the foregoing, other aspects are described in the claims, drawings, and text forming a part of the present disclosure.

[0015] In one aspect, an information processing circuit includes but is not limited to a memory circuit including processing logic integrated with non-volatile memory array on a substrate, and circuitry for performing at least one general purpose processing function associated with the non-volatile memory array. In addition to the foregoing, other aspects are described in the claims, drawings, and text forming a part of the present disclosure.

[0016] In one aspect, a method of manufacturing a memory device includes but is not limited to forming a non-volatile memory array on a substrate, and integrating processing logic in combination with the non-volatile memory array on the substrate that is operable to perform at least one general purpose processing function associated with the non-volatile memory array. In addition to the foregoing, other aspects are described in the claims, drawings, and text forming a part of the present disclosure.

[0017] In one aspect, a method of operating a memory device includes but is not limited to providing the memory device including processing logic integrated in combination with non-volatile memory array on a substrate, and operating the processing logic. Operating the processing logic can include performing at least one general purpose processing function associated with the non-volatile memory array. In addition to the foregoing, other aspects are described in the claims, drawings, and text forming a part of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Embodiments of the invention relating to both structure and method of operation may best be understood by referring to the following description and accompanying drawings:

[0019] FIGS. **1**A and **1**B are schematic block diagrams depicting top and side views of embodiments of a memory device that supports multi-core processing functionality integrated into memory.

[0020] FIGS. **2**A and **2**B are respective top and side views of schematic block diagrams illustrating embodiments of a memory device that supports multi-core processing functionality including one or more embedded central processing units (CPU) integrated into memory.

[0021] FIGS. **3**A and **3**B are schematic block diagrams illustrating respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including multiple embedded processing blocks integrated into memory.

[0022] FIGS. **4**A and **4**B are schematic block diagrams showing respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including logic for managing one or more of multiple aspects of functionality integrated into memory.

[0023] FIGS. **5**A and **5**B are schematic block diagrams depicting respective top and side view of an embodiment of a memory device that supports multi-core processing functionality using process identification logic that can identify and allocate parallel processing tasks using functionality integrated into memory.

[0024] FIGS. **6**A and **6**B are schematic block diagrams illustrating respective top and side view of an embodiment of a memory device that supports multi-core processing functionality using a protection key to secure information and memory in a selected memory portion using functionality integrated into memory.

[0025] FIGS. **7**A and **7**B are respective top and side views of schematic block diagrams showing embodiments of a memory device that supports multi-core processing functionality using logic integrated into memory including multiple memory types.

[0026] FIGS. **8**A and **8**B are schematic block diagrams depicting respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including logic integrated into memory including multiple memory types.

[0027] FIGS. **9**A and **9**B are respective top and side views of schematic block diagrams illustrating embodiments of a memory device that supports multi-core processing functionality integrated into memory and is capable of operating in combination with one or more sensors integrated with the apparatus to detect and react to operating conditions.

[0028] FIGS. **10**A and **10**B are respective top and side views of schematic block diagrams showing embodiments of a memory device that supports multi-core processing functionality integrated into memory and is capable of operating in combination with one or more sensors external to the apparatus to detect and react to operating conditions.

[0029] FIGS. **11**A and **11**B are schematic block diagrams depicting respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory that is responsive to various signals and phenomena using functionality integrated into memory.

[0030] FIGS. **12**A and **12**B are schematic block diagrams illustrating respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory using encryption logic to secure information and memory in a selected memory portion using functionality integrated into memory.

[0031] FIGS. **13**A and **13**B are schematic block diagrams depicting respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory and includes a bus which is functionality integrated into memory.

[0032] FIGS. **14**A and **14**B are schematic block diagrams illustrating respective top and side view of an embodiment of a memory device that supports multi-core processing func-

tionality in memory partitioned into multiple memory blocks in a selected memory portion using functionality integrated into memory.

[0033] FIGS. **15**A and **15**B are schematic block diagrams showing respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory and includes optical silicon enabling communication independent of a bus structure which is functionality integrated into memory.

[0034] FIG. **16** is a schematic block diagram depicting an embodiment of an information processing system including a memory device that supports multi-core processing functionality integrated into memory.

[0035] FIGS. **17**A and **17**B are a schematic block diagram and a side pictorial view illustrating an embodiment of an information processing circuit including memory that supports multi-core processing functionality and is functionality integrated into memory.

[0036] FIGS. **18**A through **18**X are multiple schematic flow charts showing several embodiments and/or aspects of a method of manufacturing a memory device that supports multi-core processing functionality integrated into memory.

[0037] FIGS. **19**A through **19**U and **20**A through **201** are multiple schematic flow charts depicting several embodiments and/or aspects of a method of operating a memory device that supports multi-core processing functionality integrated into memory.

DETAILED DESCRIPTION

[0038] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented here.

[0039] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those having ordinary skill in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

[0040] The various memory systems and devices disclosed herein are expected to be useful in many applications and contexts, and are further anticipated to be particularly useful in cloud computing and mobile contexts. In some configurations, the disclosed memory systems and devices can be used in system-on-a-chip (SOC) applications as processing and memory are distributed in more and more locations and applications throughout our technologically advancing society. The various memory systems and devices can include non-volatile memory including flash memory and electrically erasable programmable read-only memory (EEPROM) for usage in many electronic devices, such as mobile and cell phones, notebook computers, personal digital assistants, medical devices, medical diagnostic systems, digital cameras, audio players, digital televisions, automotive and transportation engine control units, USB flash personal discs, and global positioning systems.

[0041] In various applications and contexts, memory systems can include non-volatile memory integrated with a processor or other logic, and a bus or other communications interface. As non-volatile memories and integrated system continue to evolve, their role in overall systems continue to expand to include various aspects of computation that is facilitated, for example, by phase-change memory in which passage of current switches a memory material between two states, crystalline and amorphous, or additional states that further elevate storage capacity.

[0042] Referring to FIGS. **1**A and **1**B, schematic block diagrams depict top and side views of embodiments of a memory device that supports multi-core processing functionality integrated into memory. In an illustrative embodiment, a memory device **100** can include but is not limited to a substrate **102**, a non-volatile memory array **104** integrated on the substrate **102**, and processing logic **106** integrated with the non-volatile memory array **104** on the substrate **102**. The processing logic **106** is operable to perform at least one general purpose processing function **108** associated with the non-volatile memory array **104**.

[0043] Various techniques may be used for forming an integrated circuit with a combination of the non-volatile memory array and the logic. In one example technique, an integrated circuit for a non-volatile memory cell transistor can be formed by constructing a layer of discrete storage cells over a substrate in two substrate regions, applying a dielectric layer over the layer of discrete storage cells in the two substrate regions, and building a barrier layer over the dielectric layer in the two regions. The barrier layer, dielectric layer, and the layer of discrete storage cells are then removed in one of the two substrate regions, leaving the layers intact in the other of the two substrate regions. An additional barrier layer is then formed over the substrate in the two substrate regions, then removed from the substrate region from which the barrier layer, dielectric layer, and the layer of discrete storage cells were previously removed. Two gates of a memory element are then formed respectively in the two substrate regions with one gate including a portion of the first barrier layer and another gate including a portion of the additional barrier layer. One aspect of fabricating a circuit that integrates the non-volatile memory array and the logic on the system is selection of a suitable annealing process. For example, the illustrative integrated circuit can include a charge storage layer and a barrier layer formed over both a non-volatile memory region and a logic region. The charge storage layer can be formed of one or more layers and can include multiple discrete storage cells for storing charge which are isolated by a dielectric layer of insulating material with a suitably high dielectric constant. The charge storage layer can be constructed by depositing and annealing the discrete storage cells (for example, one or more of a silicon material such as polysilicon, silicon carbide, or the like, or a suitable metal such as germanium) on a dielectric area. The thermal annealing action can be performed by rapid thermal annealing (RTA) or a slower annealing process such as laser spike annealing (LSA). Memory properties can be selected and controlled by optimizing the annealing condition, thereby resulting in an improved reliability, write durability, and failure resistance.

[0044] In another example technique for forming an integrated circuit with a combination of the non-volatile memory array and the logic, a non-volatile memory cell with improved charge retention on a substrate common with logic devices using a single-gate logic process in which a silicide-blocking dielectric barrier is formed over a floating gate of a non-volatile memory cell so that silicide cannot be formed over the floating gate but is formed over logic devices, thereby pre-

venting bridging and silicide spiking in the non-volatile memory cell. The silicide-blocking dielectric barrier prevents silicide metal from contacting the floating gate or sidewall spacers while allowing the silicide metal in parts of active regions of the non-volatile memory cell at locations removed from the floating gate and spacers. The silicide regions can be constructed by initially depositing a refractory metal layer over the surface of the non-volatile memory cell, followed by a reactive anneal which causes the metal layer to react with the underlying contacted silicon regions to form silicide regions. A metal strip removed unreacted portions of the metal layer but leaves the silicide regions which are formed by a logic process using metals such as titanium, cobalt, nickel, or the like. A relatively slow annealing process can be used to produce suitable memory performance.

[0045] In a further example technique for forming an integrated circuit with a combination of the non-volatile memory array and the logic, a scalable, logic transistor can be constructed with drain and source formed as a pair of doped regions and a gate insulator layer formed over the substrate and between the drain and source. A gate stack can include a gate layer (polysilicon or metal) between two metal nitride layers. A non-volatile memory transistor that is compatible with the logic transistor can be added via a high-K dielectric constant film with an embedded metal nano-dot layer between a tunnel insulator and the gate stack. The drain and source doped regions can be n+ regions doped into a p-type substrate to form an n-channel Field Effect Transistor (FET) device. The diffusion regions can be formed using n+ doped amorphous silicon, followed by an anneal such as a rapid thermal anneal (RTA) to reduce thermal budget and silicidation. A p-channel FET can similarly be formed via p+ diffusion source/drain regions applied over an n-well region. In other embodiments, annealing can be performed using a slow annealing process to improve memory performance and write durability while reducing stress and defects.

[0046] In an additional example technique for forming an integrated circuit with a combination of the non-volatile memory array and the logic, non-volatile memory process steps can be added to a processor for forming high-voltage complementary metal-oxide semiconductor (CMOS) devices. The fabrication technique can include formation of isolation areas for the non-volatile memory and the high-voltage CMOS elements, forming high thermal drive process elements of both the memory and CMOS cells, forming mid thermal drive process elements of the logic CMOS cells, and forming low thermal process elements for logic CMOS, non-volatile memory, and high-voltage CMOS cells. Dopants for forming the devices can include masked implantation of boron, phosphorus and other species and subsequent annealing of the dopings, for example, using a slow annealing process to enhance charge retention in the system.

[0047] In some applications and/or embodiments, the memory device can include the multi-core processing capability a processor or other logic integrated in a distributed manner with non-volatile memory. Accordingly, the memory device **100** can be configured such that the processing logic **106** operable to perform at least one general purpose processing function **108** associated with the non-volatile memory array **104** is formed with functionality selectively distributed across the non-volatile memory array **104**. The memory device that includes logic integrated with non-volatile memory can include processing logic that is closely connected and can be distributed over the memory. Integrating the processing logic with memory enables general purpose processing operations immediate to the data stored in memory, increasing efficiency by avoiding delay awaiting transfer of instructions and data over a bus.

[0048] In particular applications, the processing capability can be implemented with relatively low speed requirement to enable processors to be available in a variety of relatively low performance operations, possibly in an ubiquitous manner. Accordingly, information can be acquired in a dispersed manner and intercommunicated over vast systems. Thus processors can be inexpensive and memory readily available for various consumer items. Custom versions of memory including non-volatile memory and RAM can be integrated into virtually any product, enabling widespread preprocessing such as security preprocessing in items such as door handles to determine who has accessed a location and how the access was made to allow any type of processing on the information. In applications where unpredictability is highly useful, such as multi-core processing applications, the processing logic can enhance redundant parallel processing that can be used to detect and correct for erroneous processing, for example by selection of a majority result.

[0049] The memory device can facilitate intelligent applications including multi-core processing functions by virtue of a large distributed area of processing or logic which can be spread over a relatively large area of memory storage. In some embodiments, the processor can be formed of logic that is relatively low capability or relatively low quality, for example to enable a small number of relatively simple operations, thereby reducing the number of layers of silicon in the integrated circuit chip, and possibly reducing power requirements and heat dissipation. The processing logic of such a processor-in-memory (PIM) can be widely distributed over the area of memory storage. The intelligent monitoring memory device can be formed as at least part of a system-on-a-chip (SOC).

[0050] In various embodiments, the memory device can include logic integrated with memory that is formed in a limited number of metal layers within the memory logic. To avoid stacking of multiple layers of silicon processing on the memory chip, the logic can be spread laterally across the memory array circuitry. Limited complexity of operations implemented on the memory device circuit enables slower computation speed in comparison to a typical central processing unit (CPU). Such slower computation speeds are suitable since the limiting factor in transfers of data from a processor to memory is the data bus.

[0051] The logic, including multi-core processing logic, can be configured to reduce the percentage of transistor underutilization, called "dark silicon", by breaking up of the command structure of central blocks. The logic can be further configured to enhance efficiency by performing background operations such as sorting of data within the memory while the system is idle. For example, the logic can access, if available, background information about data characteristics and applications to tailor the memory to the currently-executing application.

[0052] In some embodiments, the memory device can be configured with logic with an abbreviated set of specific, basic functions in which simple operations can be off-loaded from a processor external to the memory device and moved onto the memory device. For example, context request blocks can be removed from the processor into the memory device,

for example for security purposes since the context request blocks are typically not located in the memory.

[0053] Embodiments of the memory device with a reduced-functionality logic can facilitate efficient operation of the memory device while maintaining the integrated circuit simplicity and yield of the memory device. Typically, the number of metal layers in a memory integrated circuit is substantially smaller than that of a processor circuit. Reducing the complexity of the logic can allow fabrication with fewer metal layers.

[0054] In various embodiments, functionality logic can be attained by one or more of several techniques. For example, computations can be simplified by implementing relatively simple tasks in the logic or by acknowledging that a particular section of the memory is predominantly subject to a limited number of simple operations which can be implemented in the logic while other operations that rarely are applied to the memory section can be performed by processing external to the memory device. In another example, for operations or applications characterized by a limited or coarse accuracy, such as relatively low-grade video signals, processing can be based on estimation. In a further example, the logic can include support for multiple functions in which circuitry for the different functions can be spread over a distributed area of the non-volatile memory array, forming a large distributed area of simple processing functionality.

[0055] Referring to FIGS. **2**A and **2**B, respective top and side views of schematic block diagrams illustrate embodiments of a memory device that supports multi-core processing functionality including one or more embedded central processing units (CPU) integrated into memory. In particular embodiments, the memory device **200** can be arranged in a manner that the processing logic **206** operable to perform at least one general purpose processing function **208** associated with the non-volatile memory array **204** further includes embedded central processing unit logic **210** closely associated in function and location with a memory portion **212** of the non-volatile memory array **204**.

[0056] In an example configuration, basic general purpose processing functions can be placed into small embedded CPUs near portions of the memory. In various arrangements, the processing logic can be implemented to attain a selected parallelism including instruction level parallelism, superscalar pipelining, thread level parallelism and other aspects of parallelism. In arrangements adapted for thread level parallelism, the processing logic can be arranged in the manner of multiple independent CPUs.

[0057] Referring to FIGS. **3**A and **3**B, schematic block diagrams illustrate respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including multiple embedded processing blocks integrated into memory. Hence, the memory device **300** can be formed in a way that the processing logic **306** operable to perform at least one general purpose processing function **308** associated with the non-volatile memory array **304** further includes a plurality of embedded processing blocks **314** respectively closely associated in function and location with a plurality of memory portions **312** of the non-volatile memory array **304**.

[0058] In various embodiments, the processing logic can include multiple embedded processing blocks to form a multi-core processor with multiple executing cores on the same memory device chip. The multi-core processing blocks can operate in a different manner from superscalar processors which can issue multiple instructions per cycle from one thread or instruction stream. In contrast, the multi-core processing blocks can issue multiple instructions per cycle from multiple instruction streams. Each core in the multi-core processor can also be superscalar so that on every cycle, each core can issue multiple instructions from one instruction stream.

[0059] For example, the memory device **300** can be constructed in an arrangement that the processing logic **306** operable to perform at least one general purpose processing function **308** associated with the non-volatile memory array **304** further includes a plurality of embedded processing blocks **314** operable to execute parallel processing tasks **316** associated with the non-volatile memory array **304**.

[0060] In an example embodiment, the processing logic can be arranged in the form of multiple small processors, each coupled with a portion of system memory. Simple parallel processing tasks can run to attain multi-core functionality without running main CPU multi-core calls. A suitable configuration can include any number of processors, such as two, four, eight, to 512 or more. In some implementations, the processing logic can support ordinary CPU instructions such as add, move data, branch, and the like, which can be run in parallel in the manner of multiple cores running multiple instructions concurrently, thereby increasing overall speed for applications appropriate for parallel computing.

[0061] In certain applications and/or embodiments, the memory device **300** can be configured such that the processing logic **306** operable to perform at least one general purpose processing function **308** associated with the non-volatile memory array **304** further includes a plurality of embedded processing blocks **314** operable to execute parallel processing tasks **316** for multi-core functionality **318** in the absence of external central processing unit multi-core calls **320**.

[0062] The processing logic can be configured to facilitate instruction level parallelism. An application is a stream of instructions executed by one or more of the CPUs formed in the processing logic. The instructions can be re-ordered and combined into groups which are executed in parallel by the embedded processing blocks without changing the result of the application. The embedded processing blocks can be constructed with multi-stage instruction pipelines with each stage in the pipeline corresponding to a different action performed by the processing block on an instruction in a stage. For example, a processor with an N-stage pipeline can have up to N different instructions at different stages of completion. In addition to instruction level parallelism, the embedded logic blocks can be formed to issue more than one instruction at a time in the manner of superscalar processors. Instructions can be grouped only if no data dependencies exist between the instructions. In some embodiments, scoreboarding can be used to implement out-of-order execution and instruction level parallelism. In some arrangements, the embedded logic blocks can be constructed for task parallelism in which different calculations can be performed on either the same or different sets of data.

[0063] Referring to FIGS. **4**A and **4**B, schematic block diagrams show respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including logic for managing one or more of multiple aspects of functionality integrated into memory. Thus, in an example embodiment, the memory device **400** can be patterned with the processing logic **406** operable to perform at least one general purpose processing function **408**

associated with the non-volatile memory array **404** further including string processing logic **422** operable to perform at least one string processing function **424** associated with the non-volatile memory array **404**.

[0064] The string processing logic can be used to perform string processing such as comparing blocks of memory, anti-virus scanning, data compression, sorting, and the like. In various embodiments, the string processing logic can perform operations that manipulate a string or query of information including actions such as compare (numerical or relational operator-based), concatenation, equality, find (or contains), format, inequality, join, left, length, replace, reverse, right, split, substring, and the like.

[0065] In some embodiments, the memory device **400** can be arranged in a manner that the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further includes anti-virus scanning logic **426** operable to perform at least one anti-virus scanning function **428** associated with the non-volatile memory array **404**.

[0066] In example embodiments, the anti-virus scanning logic can perform various strategies, such as signature-based detection in which the anti-virus scanning logic searches for known patterns of data within executable code or uses a heuristic approach using generic signatures to identify new viruses or variants of existing viruses by looking for known or slight variations of malicious code. In some implementations, the anti-virus scanning logic can predict actions by executing code in a scratch space or "sandbox" in the memory device and analyze for malicious actions.

[0067] In a particular embodiment, the memory device **400** can be formed in a way that the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further includes data compression logic **430** operable to perform at least one data compression function **432** associated with the non-volatile memory array **404**.

[0068] In example embodiments, the data compression logic can be a type of data differencing which determines a difference between a source and a target. Data compression can be performed by producing a compressed file given a target, and decompression can be production of a target given only a compressed file. Thus, data compression can be data differencing with empty source data with the compressed file being the difference from a null record.

[0069] In another example application, the data compression logic can be used for audio compression such as via use of transforms such as modified discrete cosine transform (MDCT) to convert time domain sampled waveforms into a transform domain such as the frequency domain. The transformed signal component frequencies can be allocated bits according to audibility of spectral components, for example by calculating a masking threshold that eliminates sounds outside the limits of human perception. Another audio compression technique can be via linear predictive coding that use a model of the sound's generator to whiten the audio signal prior to quantization. The data compression can perform other known compression techniques including speech compression schemes.

[0070] In further example applications, the data compression logic can perform video compression such as interframe compression which uses one or more earlier or later frames in a sequence to compress the current frame, or intraframe compression using only the current frame. Similarly, the data compression logic can compare each frame in the video with the previous frame. If the frame contains areas with no changes, the area from the previous frame can be copied, bit-for-bit, to the next frame. If areas of the frame move in a simple manner, the data compression logic can shift, rotate, lighten, or darken the frame. Other suitable video compression techniques can be implemented.

[0071] In some applications and/or embodiments, the memory device **400** can be configured such that the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further includes sorting logic **434** operable to perform at least one sorting function **436** associated with the non-volatile memory array **404**.

[0072] In various embodiments and/or applications, the sorting logic can perform any suitable sorting function, typically involving comparison and swapping of data. The sorting logic, for example, can perform a bubble sort in which elements are compared and swapped if out of order, repeating until no swaps have occurred. In another example scheme, the sorting logic can perform an in-place comparison sort or selection sort by finding the minimum value, swapping with the value in the first position, and repeating for the remainder of the list. In a further technique, the sorting logic can perform an insertion sort by taking elements from a list sequentially and inserting in the correct position into a new sorted list. Similarly, the sorting logic can perform a shell sort by moving out-of-order elements more than one position at a time, for example arranging the data sequence in a two-dimensional array and then sorting the columns of the array using the insertion sort. Other suitable sorting techniques include a merge sort which merges already sorted lists into a combined list by comparing every two elements sequentially multiple times, quiksort, counting sort, bucket sort, radix sort, distribution sort, and the like.

[0073] In a further example embodiment configuration, the memory device **400** can be constructed in an arrangement that the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further includes peripheral logic **438** operable to manage the non-volatile memory array **404** in response to external central processing unit calls **420**.

[0074] The processing logic can be configured to operate as peripherals or extensions of instruction sets in a manner that is transparent to an external device such as a CPU that sends commands and instructions to the memory device. In some embodiments, the memory device can support peripherals and extensions to instructions of various processors such as Intel x86 family processors, Reduced Instruction Set Computing (RISC) architectures such as ARM, SPARC, Power, PowerPC, MIPS, and the like.

[0075] In some example embodiments, the memory device **400** can be arranged in a manner that the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further includes extension logic **440** operable to manage the non-volatile memory array **404** in response to external central processing unit calls **420**.

[0076] Peripheral or extension logic in the processing logic can be formed in close proximity in the manner of multiple CPU cores on the same integrated circuit chip (the memory device) to facilitate cache coherency circuitry to operate at relatively high clock-rates in comparison to architectures in which signals have to travel off-chip. Combining similar

CPUs on a single chip improves cache snoop operations in that signals between the multiple different on-chip CPU cores travel shorter distances and thus have lower signal degradation. The elevated-quality signals enable more data to be send in a time click since individual signals can be shorter and need not be repeated as frequently.

[0077] In various embodiments, the processing logic can include peripherals or extensions of instruction sets executed by a processor or CPU external to the memory device that uses the memory device for storage. For example, an external CPU performing parallel processing functions can store data in the memory device and the peripherals or extensions of the instruction set implemented in the processing logic can include support for data dependency handling. The external CPU can send instructions to the memory device and the memory device can handle the instructions in the correct order to address data dependency issues. Similarly, the processing logic can include support for instruction pipelining, superscalar execution, out-of-order execution, register renaming, speculative execution, branch prediction, and the like. In some embodiments, a superscalar CPU external to the memory device can read instructions from the memory device and the processing logic in the memory device can be configured to determine which instructions can be run in parallel and respond to the reads accordingly, facilitating dispatch of the instructions to redundant functional units in the external CPU.

[0078] In some embodiments, the processing logic can include multiple fine-grained functional units such as arithmetic logic units (ALU), integer multiplier, integer shifter, floating point unit and the like. The processing logic can include multiple versions of each functional unit to enable execution of many instructions in parallel that operate in cooperation with a CPU external to the memory device.

[0079] In further applications and/or embodiments, the memory device **400** can be patterned with the processing logic **406** operable to perform at least one general purpose processing function **408** associated with the non-volatile memory array **404** further including dormant processing logic **442** operable upon activation by a signal **444** from a device external to the memory device **400** to perform at least one processing function **446** associated with the non-volatile memory array **404**. The dormant processing logic can be used to perform various operations such as sorting and anti-virus scanning when the memory device is dormant with respect to a device such as a CPU that is external to the memory device.

[0080] Referring to FIGS. **5**A and **5**B, schematic block diagrams depict respective top and side view of an embodiment of a memory device that supports multi-core processing functionality using process identification logic that can identify and allocate parallel processing tasks using functionality integrated into memory. Accordingly, in various embodiments, the memory device **500** can be constructed in an arrangement that the processing logic **506** operable to perform at least one general purpose processing function **508** associated with the non-volatile memory array **504** further includes process identification logic **548** operable to identify and allocate parallel processing tasks **516** associated with the non-volatile memory array **504**.

[0081] For example, the processing logic and process identification logic can map memory to different, but not necessarily concurrent processes, and control access to different portions of memory based on identity of a processor such as in the manner of file system access control.

[0082] Within a computer system, that processing logic can be used to protect, for example, components of an operating system and other program components from one another's operations and actions. In a particular example situation, a global address space can be shared among multiple software components and the processing logic can ensure that memory, files, objects, data, code, information, and the like can be accessed or operated upon by only those components granted proper authorization. Thus, in sample embodiments and/or applications, the memory device **500** can be formed in a way that the processing logic **506** operable to perform at least one general purpose processing function **508** associated with the non-volatile memory array **504** further includes process identification logic **548** operable to identify and allocate a plurality of parallel processing tasks **516** for multi-core functionality **518** in the absence of external central processing unit multi-core calls **520**.

[0083] The processing logic can additionally ensure proper information processing by assuring integrity of an interaction between two or more parallel processes, for example to deter eavesdropping or other security breach, or to ensure that two processes are operating in concert and not overwriting one another's data.

[0084] In an example application, the processing logic can copy data from a first location of memory to a second redundant section of memory and the process identification logic can limit access to the memory sections based on identification of a process. For a memory that includes sufficiently large and inexpensive memory, the processor or logic can perform a copy function at selected intervals, for example in a selected range of cycle rates, to copy the state to a redundant fast memory for copying to a slow memory, and to facilitate decision-making in memory. Thus, the memory can control sampling with the logic including sampling functionality, and sampling of fast memory. For applications or contexts such as video handling in which only intermittent frames are sufficient to produce a suitable video image, a backup into lossy memory may be suitable to enable a basic recovery of data. In some embodiments, the memory may include excess memory in the form of flip-chip via a dedicated bus to send data from a first fast memory to a second fast memory. Variability of performance in the lossy memory can be exploited to destroy data such as image data, for example by transferring an video data into a lossy media from which video streaming cannot be recovered.

[0085] In some applications, what is desired is a capability to store large amounts of data while allowing some amount of inaccuracy or error. Such an application can be video streaming. The memory device can thus be formed with at least a portion of the memory that is very inexpensive but lossy.

[0086] Referring to FIGS. **6**A and **6**B, schematic block diagrams illustrate respective top and side view of an embodiment of a memory device that supports multi-core processing functionality using a protection key to secure information and memory in a selected memory portion using functionality integrated into memory. In some embodiments and/or applications, the memory device **600** can further include a protection key register **652** integrated with the processing logic **606** and the non-volatile memory array **604** on the substrate **602**. The processing logic **606** operable to perform at least one general purpose processing function **608** associated with the non-volatile memory array **604** can further include protection key logic **654** operable to manage access to a selected

memory portion **612** of the non-volatile memory array **604** based on information in the protection key register **652**.

[0087] In a specific example embodiment, the protection key logic can manage allocation of resources among multiple processes or tasks using keys which can be allocated at a selected granularity to indicate an association with a data object. Individual processes or modules can be allowed access to memory portions assigned to one or more data objects. The protection key logic can control access to selected memory portions based on whether a protection key currently loaded in the protection key register allows access to the memory portion(s). In a specific example, an individual portion of memory can be assigned a key number that indexes into a protection key set. The currently loaded protection key set identified memory portion key numbers that can be accessed by a process attempting access. A key in the protection key set can be associated with one or more data objects or groups of data objects, identifying currently accessible data objects or groups of data objects.

[0088] In a particular example embodiment, the memory device **600** can further include a protection key register **652** integrated with the processing logic **606** and the non-volatile memory array **604** on the substrate **602**. The processing logic **606** operable to perform at least one general purpose processing function **608** associated with the non-volatile memory array **604** can further include protection key logic **654** operable to operable to receive information and write the received information to the protection key register **652**.

[0089] In a specific example embodiment, the protection key logic can manage access to resources among multiple processes and/or tasks using control of a translation lookaside buffer in the memory integrated with the protection key logic. A request directed to a memory portion can be received from an external device such as a CPU and the protection key logic can search the translation lookaside buffer for the memory portion request. If an entry for the memory portion request is located in the translation look-aside buffer, then the key number stored with the entry is retrieved. Otherwise, a table is accessed to retrieve the key number for the request. The key number can be compared with the protection key set to determine whether access to memory portions assigned to the key number is enabled. If the protection key set enables access, the protection bit is also checked to determine whether access to the memory portion is enabled.

[0090] In some embodiments, the memory device **600** can further include a protection key register **652** integrated with the processing logic **606** and the non-volatile memory array **604** on the substrate **602**. The processing logic **606** operable to perform at least one general purpose processing function **608** associated with the non-volatile memory array **604** can further include protection key logic **654** operable to allocate parallel processing tasks **616** for multi-core functionality **618** based on information in the protection key register **652**.

[0091] In a particular example embodiment, the protection key logic can manage access to memory using a protection key set in the form of a bit vector indexed to memory portion key numbers. The protection key set can be indexed to memory portion key numbers for read requests and indexed to memory portion key numbers for write requests. A bit set at individual indexed key number locations can identify whether a particular type of access is enabled.

[0092] In various embodiments and/or applications, the memory device **600** can further include a protection key register **652** integrated with the processing logic **606** and the non-volatile memory array **604** on the substrate **602**. The processing logic **606** operable to perform at least one general purpose processing function **608** associated with the non-volatile memory array **604** can further include protection key logic **654** operable to read data from a selected memory portion **612** of the non-volatile memory array **604** only if authorized by information in the protection key register **652**.

[0093] In a particular example embodiment, the protection key logic can manage multiple process or task access to memory in a memory with a flat address space. The protection key logic can updating memory segment table entries which hold a memory address for individual memory portions with a memory portion protector that identifies access allowed to the memory portion by a process or module as the process or module is loaded for execution. The protection key logic can efficiently manage changes in memory protection using memory protectors in table entries by addressing multiple portions of memory, for example different types of memory integrated into the memory device, by having a single address mirrored over multiple memory segments. For example, a memory portion protector for a single memory portion stored in multiple locations can have an address mirrored in memory segments including translation lookaside buffer, cache, and table in which the protection key logic integrated into the memory can simultaneously change the protector value in the multiple segments in a single operation.

[0094] In various embodiments, the memory device **600** can further include a protection key register **652** integrated with the processing logic **606** and the non-volatile memory array **604** on the substrate **602**. The processing logic **606** operable to perform at least one general purpose processing function **608** associated with the non-volatile memory array **604** can further include protection key logic **654** operable to write data to a selected memory portion **612** of the non-volatile memory array **604** only if authorized by information in the protection key register **652**.

[0095] In some arrangements, memory can include portions with different memory types. In embodiments of the memory device depicted in FIGS. **7**A and **7**B, respective top and side views of schematic block diagrams show embodiments of a memory device that supports multi-core processing functionality using logic integrated into memory including multiple memory types. The memory device **700** can be configured such that the non-volatile memory array **704** further includes a plurality of non-volatile memory segments **756** characterized by a respective plurality of non-volatile memory types **758**. The processing logic **706** operable to perform at least one general purpose processing function **708** associated with the non-volatile memory array **704** can be operable to perform at least one general purpose processing function **708** for the non-volatile memory segments **756** selectively based on ones of the plurality of non-volatile memory types **758**. In an example embodiment, the processing logic can include multiple general purpose processing functions associated with different non-volatile memory segments with possible differences in the allocation of processing functionality applied.

[0096] In various embodiments, the memory device can include multiple types of memory technology, for example including charge memory or resistive memory. An memory device can include sections of charge memory and resistive memory and the logic can assign applications to exploit the advantages and diminish the consequences of disadvantages of either type of memory. Charge memories induce a voltage

which is detected during read operations in response to require amounts of charge. In nonvolatile storage, flash memories precisely control the discrete charge placed on a floating gate. In volatile storage, DRAM not only places charge in a storage capacitor but also mitigate subthreshold charge leakage through the access device using capacitors that are sufficiently large to store charge for reliable sensing and using transistors that are sufficiently large to exert effective control over the channel. Resistive memories use electrical current to induce a change in atomic structure, changing the resistance detected during reads. Resistive memories are more suitable for scaling than charge memories by avoiding precise charge placement and control. Programming via techniques such as current injection scale with cell size. Phase-change memory (PCM), spin-torque transfer (STT) magneto-resistive RAM (M-RAM), and ferroelectric RAM (FRAM) are examples of resistive memories.

[0097] The logic can allow less-than-perfect performance for suitable applications and/or contexts. The logic can determine and use Quality-of-Service (QoS) ratings for processor in memory (POM), and assign priority of performance to sections of memory. For relatively high performance applications, the device may be configured to work perfectly and the logic can specify that only highly reliable memory is used. Other applications can operate at a lower QoS and the logic can select memory accordingly. Other examples of non-volatile memory technologies with various QoS ratings can include resistive RAM (R-RAM) and spin-transfer torque RAM (STT-RAM). R-RAM can be any memory technology that relies of resistance change to store information, for example including space-charge-limited-current (SCLC), filament, programmable-metallization-cell (PMC), Schottkey contact and traps (SCT). R-RAM can be characterized by non-volatility, high-speed, high-performance, zero standby power, and, in some arrangements, high density. For an memory device that includes at least a portion of the memory in the form of R-RAM, the logic can monitor memory accesses and determine whether a particular application is characterized by high-speed and high-performance, and assign the R-RAM memory portion for the application.

[0098] For example, the logic can determine and use QoS ratings, and assign priority of performance to sections of memory. For relatively high performance applications, the device may be configured to work perfectly and the logic can specify that only highly reliable memory is used. The logic can perform an error detection operation and determine whether too many errors are occurring according to a predetermined threshold and, if so, the logic can shift to higher performing memory. The logic can start an application with a determined QoS rating and monitor errors to iteratively select an appropriate memory segment that is tailored to application characteristics and performance.

[0099] In another example application, an memory device can include a non-volatile memory array and includes at least a portion of the memory in the form of STT-RAM. STT-RAM can be characterized by improved performance via overdriving. Overdriving the gate voltage of an NMOS transistor in the STT-RAM can increase V_{GS} and thus enhance the driving strength of the NMOS transistor. The logic can be configured to manage overdriving, for example, by monitoring memory access operations such as reading, writing, erasing, driving write-line voltage, and the like, and control overdriving according to the particular application.

[0100] In various embodiments, the memory device can include a non-volatile memory array which includes one or more suitable memory technology. For example, memory technologies in the memory device can include embedded flash, read-only memory (ROM), electrical fuse (one-time programmable), CMOS floating gate (multiple time programmable), CMOS floating gate (one-time programmable), and anti-fuse (one-time programmable). The different memory technologies can have various advantages and disadvantages for particular operations or applications. Some memory technologies can have relatively high density such as ROM and antifuse, while others have low density (for example electrical fuse and CMOS floating gate). Some technologies have good endurance such as embedded flash, and CMOS floating gate, while others have poor endurance, for example ROM, electrical fuse, CMOS floating gate, and antifuse. Various technologies can have different standby and active current including high current (electrical fuse), medium current (embedded flash and CMOS floating gate), and low current (ROM and antifuse). The memory technologies vary in random access time including fast (ROM and antifuse), medium (embedded flash and CMOS floating gate), and slow (electrical fuse). The memory technologies vary in security including high security (antifuse), medium security (embedded flash and CMOS floating gate), and slow security (ROM and electrical fuse). The memory technologies vary in high and low temperature and voltage tolerance including high tolerance (ROM and antifuse), medium tolerance (electrical fuse), and low tolerance (embedded flash and CMOS floating gate). In a memory device that includes multiple memory sections with more than one memory technology, the logic can monitor a history and pattern of memory accesses and assign memory usage depending on the monitoring. For data or code that changes very frequently, the logic can assign embedded flash. For high volume storage, the logic can assign more dense memory technologies. For applications in which the code changes infrequently, the logic can allocate, for example, ROM and antifuse. The logic can assign memory accesses depending on temperature and voltage conditions that can be measured using sensors or otherwise communicated to the memory device. The logic can determine the security level of an application and assign the memory technology accordingly.

[0101] In some embodiments and/or applications, the non-volatile memory can be formed of one or more of any non-volatile memory type or technology including read-only memory, flash memory, ferroelectric random access memory (F-RAM), magneto-resistive RAM (M-RAM) or the like.

[0102] In some embodiments or applications, a capability for the memory device to efficiently support both bit maps and vector graphics may be useful. Accordingly, the memory device can be configured so that the memory includes a portion that is bit-mapped and a portion that is vector memory. For example, part of the memory can be optimized for pictures and video (JPEG) and another portion optimized for more computational applications. An example of such that context that would benefit from both memory types is a mobile telephone with camera and/or video functionality.

[0103] Referring to FIGS. **8**A and **8**B, schematic block diagrams depict respective top and side view of an embodiment of a memory device that supports multi-core processing functionality including logic integrated into memory including multiple memory types. Thus, memory device **800** can be arranged in a manner that the non-volatile memory array **804**

further includes a plurality of non-volatile memory segments **856** characterized by a respective plurality of non-volatile memory types **858**. The processing logic **806** operable to perform at least one general purpose processing function **808** associated with the non-volatile memory array **804** can further include string processing logic **822** operable to perform at least one string processing function **824** for the non-volatile memory segments **856** selectively based on ones of the plurality of non-volatile memory types **858**.

[0104] In further embodiments, the memory device **800** can be constructed in an arrangement that the non-volatile memory array **804** further includes a plurality of non-volatile memory segments **856** characterized by a respective plurality of non-volatile memory types **858**. The processing logic **806** operable to perform at least one general purpose processing function **808** associated with the non-volatile memory array **804** can further include anti-virus scanning logic **826** operable to perform at least one anti-virus scanning function **828** for the non-volatile memory segments **856** selectively based on ones of the plurality of non-volatile memory types **858**.

[0105] In additional embodiments, the memory device **800** can be formed in a way that the non-volatile memory array **804** further includes a plurality of non-volatile memory segments **856** characterized by a respective plurality of non-volatile memory types **858**. The processing logic **806** operable to perform at least one general purpose processing function **808** associated with the non-volatile memory array **804** can further include data compression logic **830** operable to perform at least one data compression function **832** for the non-volatile memory segments **856** selectively based on ones of the plurality of non-volatile memory types **858**.

[0106] In example embodiments, the memory device **800** can be patterned with the non-volatile memory array **804** further including a plurality of non-volatile memory segments **856** characterized by a respective plurality of non-volatile memory types **858**. The processing logic **806** operable to perform at least one general purpose processing function **808** associated with the non-volatile memory array **804** can further include sorting logic **834** operable to perform at least one sorting function **836** for the non-volatile memory segments **856** selectively based on ones of the plurality of non-volatile memory types **858**.

[0107] Referring to FIGS. **9**A and **9**B, respective top and side views of schematic block diagrams illustrate embodiments of a memory device that supports multi-core processing functionality integrated into memory and is capable of operating in combination with one or more sensors integrated with the apparatus to detect and react to operating conditions. For example, the memory device can be integrated used in a medical implant such as an orthopedic implant (knee, hip, shoulder, elbow, and the like), a cardiology implant such as a pacemaker, anti-tachycardia device, defibrillator, and the like. The memory device can include any suitable type of sensor such as motion or position sensors, electrical signal sensors, pressure sensors, oxygen sensors, and the like. The processor and memory can be configured to facilitate monitoring for therapeutic and diagnostic purposes, and delivery of therapy.

[0108] Referring to FIGS. **10**A and **10**B, respective top and side views of schematic block diagrams show embodiments of a memory device that supports multi-core processing functionality integrated into memory and is capable of operating in combination with one or more sensors external to the apparatus to detect and react to operating conditions. For example, the memory device can be used in a product in the form of an environmental monitor such as for usage in environmental-critical applications such as computer and network data centers, hospitals, and museums. The memory device can be used with any suitable type of environment sensor such as thermometers, pressure sensors, magnetic field sensors, moisture sensors, and the like. The environmental monitor can be used to monitor and maintain the environment within selected limits.

[0109] Referring to FIGS. **9**A, **9**B, **10**A, and **10**B, the memory device **900**, **1000** can further include at least one sensor **960**, **1060** operable to detect at least one operating condition **962**, **1062**. The processing logic **906**, **1006** operable to perform at least one general purpose processing function **908**, **1008** associated with the non-volatile memory array **904**, **1004** can be operable to perform at least one general purpose processing function **908**, **1008** for the non-volatile memory array **904**, **1004** selectively based on the at least one operating condition **962**, **1062**.

[0110] Thus, the processing logic can be operable to determine whether a portion of memory can be accessed based on physical phenomena detected by a sensor. For example, the memory device can incorporate sensors or other components that detect phenomena which can be monitored by the logic to detect aspects of magnetic fields, temperature, velocity, rotation, acceleration, inclination, gravity, humidity, moisture, vibration, pressure, sound, electrical fields or conditions such as voltage, current, power, resistance, and other physical aspects of the environment to enable the processing logic to perform actions to improve multi-core processing of parallel processing tasks.

[0111] The non-volatile memory array can include memory portions formed of memory technologies characterized by high performance under particular operating conditions. Phase change RAM (PCRAM) is a memory technology with highly favorable small cell size and thus density. The memory device which includes at least a portion of PCRAM can further include logic that monitors and determines operating conditions and can assign memory accesses to PCRAM in low power high performance conditions.

[0112] In an example application, the processing logic can include a thread scheduler that takes operating condition of the non-volatile memory array into consideration for scheduling threads. The thread scheduler rapidly selects from among a list of ready-to-execute threads as well as maintaining a ready-to-execute and stalled thread lists. Thread priority can be selected at least in part based on the detected operating conditions.

[0113] The memory device can include any suitable sensor for detecting a condition that may be useful for improving multi-core processing of parallel processing tasks. Example sensors can measure voltage, current, capacitance, resistance, inductance, capacitive/resistive, and other electrical or magnetic phenomena. Other suitable sensors can sense touch, tactile phenomena, pressure, vibration, velocity, acceleration, rotation, angular acceleration, angular velocity, and the like. Some sensors can sense ionic potential, optical radiation, electrochemical potential, infrared radiation, temperature, ionizing radiation, moisture, and the like.

[0114] In an embodiment of a memory device that includes multiple memory types or technologies, the sensor can detect electrical characteristics such as voltage or current and the processing logic can use the electrical characteristics to perform multi-core processing of parallel processing task opera-

tions such as determining whether a portion of memory can most efficiently handle a particular parallel processing task.

[0115] In an embodiment of a memory device that includes multiple memory types or technologies, the sensor can detect electrical characteristics such as voltage or current and the logic can determine whether the energy drive is sufficient to drive the memory reliably. If the energy drive is insufficient for a particular type of memory, the logic can shift memory accesses to a memory type that can be reliably driven.

[0116] In various embodiments, logic can be operable to monitor the operating condition, monitor memory accesses, analyze the monitored operating conditions and memory accesses, predict expected outcomes based on the monitored operating conditions and memory accesses, and allocate memory accesses based on the predicted expected outcomes. In a particular application, the memory device can include logic configured to predict different possible outcomes, for example predicting several possible outcomes and preparing for each, then use sensors, measurements, and monitoring to determine which outcome to activate at a particular time.

[0117] The processing logic can be used to efficiently allocate memory among multiple parallel processing tasks or to deter attacks from malware running on a CPU external to the memory device, and attempted accesses of data stored on the memory device from a network. Referring to FIGS. **11**A and **11**B, schematic block diagrams depict respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory that is responsive to various signals and phenomena using functionality integrated into memory. In embodiments according to FIGS. **11**A and **11**B, the memory device **1100** can be configured such that the processing logic **1106** operable to perform at least one general purpose processing function **1108** associated with the non-volatile memory array **1104** is operable to access a time signal **1164** and perform at least one general purpose processing function **1108** for the non-volatile memory array **1104** based on the time signal **1164**. The time signal can be used to limit access to one or more memory locations based on time. In an example embodiment and/or application, the memory may have access enabled as specified for a particular tick count since boot time, current time, various high-performance performance counters, high-precision logic counters that are internal to the memory device integrated circuit, high-precision processor or CPU counters external to the memory device integrated circuit, and the like.

[0118] For example, the memory device can include logic that takes into consideration that, at different times, the loads are expected to be different. In a particular instance, the memory device may be used in a data center in which some of the activity is work-related, and other activity is recreational. The logic can be configured to allocated different types of memory accordingly, for example to handle volumes of streaming video and audio content during non-working hours.

[0119] In another example operation, the processing logic can be configured to programmably select times at which a particular user, entity, or process can access a specified memory location. According to a predetermined arrangement, the processing logic can allow different entities to access the specified memory at particular times, or allow some entities read access at selected times and other entities write access, for example to avoid a race condition and ensure the correct data is available according to a predetermine arrangement.

[0120] In an example embodiment, the memory device **1100** can be arranged in a manner that the processing logic **1106** operable to perform at least one general purpose processing function **1108** associated with the non-volatile memory array **1104** is operable to monitor phenomena **1166** detectable at the memory device **1100** and perform at least one general purpose processing function **1108** for the non-volatile memory array **1104** based on the monitored phenomena **1166**. Detected or received information associated with various phenomena can be used to supply constraints limiting access to memory. In an example embodiment and/or application, the processing logic can limit memory accessibility to a variety of phenomena such as current process identifier (ID), current thread ID, a hash of a user's environmental block including user name, computer name, search path, and others. Other memory device phenomena can include system information fields, performance counters, and the like. Additional physical phenomena can be monitored via sensors or other components incorporated into the memory device that detect phenomena which can be monitored by the control logic to detect magnetic fields, temperature, velocity, rotation, acceleration, inclination, gravity, humidity, moisture, vibration, pressure, sound, electrical fields or conditions such as voltage, current, power, resistance, and other physical aspects of the environment to enable the control logic to perform actions to maintain, repair, clean, or other operations applied to the memory.

[0121] In various embodiments and/or applications, the memory device **1100** can be patterned with the processing logic **1106** operable to perform at least one general purpose processing function **1108** associated with the non-volatile memory array **1104** operable to accumulate and communicate information about phenomena **1166** associated with at least one entity **1168** in association with the memory device **1100** and perform at least one general purpose processing function **1108** for the non-volatile memory array **1104** based on the monitored phenomena **1166**. In various embodiments and/or applications, an entity can be a person, a living being, a non-living being, an organization (business, political, or otherwise), a device, a computer, a network, or the like. For purposes of example, the memory device can be integrated into a biocompatible, biodegradable form for hemodynamic monitoring of pressure and blood flow within the circulatory system. Thus, the processor and integrated memory in the memory device can include encryption logic in which security is facilitated by processing logic to control access to algorithm control parameters specific to the patient or to limit access to patient data accumulated and stored in the memory device, for example in a product for Holter monitoring of an ambulatory patient independently of any external device, although supporting communication with a device external to the patient's body via telemetry for exchange of commands, instructions, control information, and data. Other embodiments of the memory device can be used in combination with suitable sensors that can sense touch, tactile phenomena, pressure, vibration, velocity, acceleration, rotation, angular acceleration, angular velocity, ionic potential, optical radiation, electrochemical potential, infrared radiation, temperature, ionizing radiation, moisture, and the like that can supply phenomena information associated with an entity.

[0122] Referring to FIGS. **12**A and **12**B, schematic block diagrams illustrate respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory using encryption logic to secure information and memory in a selected memory portion using functionality integrated into memory. In example embodiments, the memory device **1200** can be constructed in an arrangement that the processing logic **1206** operable to perform at least one general purpose processing function **1208** associated with the non-volatile memory array **1204** further includes encryption logic **1270** operable to perform at least one encryption/decryption function **1272** associated with the non-volatile memory array **1204** and operable to read data from a selected portion of the non-volatile memory array **1204** only if authorized by results of the encryption/decryption function **1272**.

[0123] In a particular example embodiment, the encryption logic can be used in a parallel processing environment to protect secret information and/or instructions stored in selected blocks of the nonvolatile memory array. The secret information and/or instructions can be used for security operations, such as public and/or shared key cryptographic processing, copy protection, and the like. The encryption logic can protect the secret information and/or instructions from access subsequent to prescribed usage to prevent unauthorized access by malware, hackers, viruses, and the like.

[0124] In various embodiments, the processing logic can virtually lock predetermined locations in the nonvolatile memory, ensuring protection of secret code and data in a block of the nonvolatile memory array and enabling a computing system to prevent access to the secret code and/or data by other programs after allowed processing is complete. Memory locking protects selected blocks of memory against malware or hacking and flags the security breach for subsequent analysis and action.

[0125] Accordingly, the memory device further can be beneficial on the basis of improving security in multiple parallel processes, for example by retaining encryption keys in the memory device, outside of main memory, until the keys are required in main memory. Holding (hiding) the encryption keys in the memory device, outside the main memory, until essential guards against malware. Typically, malware reads passcodes or encryption keys from main memory and uses the violated passcodes and encryption keys to perform decryption and/or decryption, generally impersonating an authorized user. In a secure environment, a user or system can transfer the passcodes and encryption keys to main memory only when essential, and otherwise maintain them securely in the memory device.

[0126] The memory device, by virtue of distributed processing with the memory, can enable the processing logic to improve security by holding data in a secure location on the non-volatile memory and hide a substantial amount of information secure from attacks that would affect a CPU and main memory. The distributed logic can execute simple or minor, dedicated processing due to the substantial amount of silicon available on the memory device.

[0127] In sample embodiments and/or applications, the memory device **1200** can be formed in a way that the processing logic **1206** operable to perform at least one general purpose processing function **1208** associated with the non-volatile memory array **1204** further includes encryption logic **1270** operable to perform at least one encryption/decryption function **1272** associated with the non-volatile memory array **1204** that holds at least one encryption key **1272** secure from a device external to the memory device **1200** and operable to read data from a selected portion of the non-volatile memory array **1204** only if enabled by the encryption key **1272**.

[0128] By distributing processing and encryption functionality in combination with the memory, outside a main CPU and main memory in a computer system, throughput can be increased for general purpose processing and encryption-type activities at least partly because transfer of data between the memory device and the CPU and main memory can be greatly reduced.

[0129] In some embodiments, the encryption logic can be configured to perform a hash function, an algorithm or subroutine that maps large data sets of variable length, called keys, to smaller data sets of a fixed length. The values returned by a hash function can be called hash values, hash codes, hash sums, checksums, or hashes.

[0130] Hash logic can be used in both symmetric and asymmetric cryptography to generate keys and random values used in operations. In some embodiments, the encryption logic can support symmetric-key cryptography (block ciphers or stream ciphers) in which both the sender and receiver share the same key or different, related keys which are computable. The encryption logic can implement Data Encryption Standard (DES) and/or Advanced Encryption Standard (AES) block cipher designs in which data is input in blocks of plaintext. Embodiments of the encryption logic can also implement stream ciphers which create an arbitrarily long stream of key material, which is combined with the plaintext bit-by-bit or character-by-character. An output stream is formed based on a hidden internal state which changes as the cipher operates and is initialized up using the secret key material. The encryption logic can also implement cryptographic hash functions that can receive a message of any length as an input signal, and can produce a short, fixed length hash for use, for example, as a digital signature.

[0131] In some embodiments, the encryption logic can support public key cryptography in which a public key may be freely distributed, while a paired private key remains secret. In a public-key encryption system, the public key is used for encryption, while the private or secret key is used for decryption. Public-key cryptography can be used, for example, for implementing digital signature techniques.

[0132] The hash logic can be used in conjunction with the processing logic on the memory device for various purposes. For example, a pseudo-random number generator function P(key) can be uniform on an interval $[0, 2^{b-1}]$ and a hash function uniform on the interval [0, n−1] is nP[key]/2^b so that a division operation can be replaced by a more simple and possibly faster right bit shift, nP(key)>>b, in an operation that can simplify the logic in the memory device. In another example operation, hashing logic in the memory device can be formed to perform hashing by nonlinear table lookup in which tables of random numbers can enable high-quality nonlinear functions to be used as hash functions or other purposes such as cryptography. The key to be hashed can be divided into parts with individual parts used as an index for a non-linear table. Table values can be added by arithmetic or XOR addition to the hash value, reducing memory size and enabling fast hash execution, which can be particularly beneficial in a memory device that includes simplified logic integrated with the non-volatile memory.

[0133] Referring to FIGS. **13**A and **13**B, schematic block diagrams depict respective top and side view of an embodi-

ment of a memory device that supports multi-core processing functionality integrated into memory and includes a bus which is functionality integrated into memory. Consequently, the memory device **1300** can further include a bus **1376** integrated with the processing logic **1306** and the non-volatile memory array **1304** on the substrate **1302**. The bus **1376** is operable to communicate access requests and information **1378** between the memory device **1300** and a device external to the memory device **1380**. The memory device can facilitate communication and handle additional bandwidth via usage of logic that can predict subsequent transfers and write to memory accordingly to enable processing on the predicted data values. In some embodiments, the memory device can include communication channels in addition to the bus to facilitate transfer of information for various management functions, alleviating the traffic on the bus.

[0134] In some embodiments, the processing logic can be configured as a symmetric multiprocessor (SMP) with multiple identical processors that share the memory and connect via the bus.

[0135] A memory device that includes a communication interface or bus can communicate with other such devices or any type of device or system to enable multiple distributed devices to intercommunicate or to communicate with a network, for example in a cloud system. Thus, the memory device can be widely distributed or even ubiquitous, to perform selected local processing regarding usage and environment, for example to enable history tracking, data pre-processing, and sharing to other devices or through the cloud.

[0136] In some embodiments, the memory device **1300** can be composed so that the processing logic **106** operable to perform at least one general purpose processing function **1308** associated with the non-volatile memory array **1304** is operable to perform the at least one general purpose processing function **1308** independently of signals **1344** external to the memory device **1300**.

[0137] In particular embodiments, the logic, including processing logic adapted for executing multiple parallel processing tasks, can perform pattern recognition in an integrated circuit chip and perform analysis in operations that are background to data communication via a bus to a device such as a processor external to the memory device. Background tasks that are local to the memory device can include maximum and minimum sorting, medium, and mode computation. Operations perform by the logic can include statistical measurements, indexing, synchronizing, detection of repetitive tasks, and the like.

[0138] Referring to FIGS. **14**A and **14**B, schematic block diagrams illustrate respective top and side view of an embodiment of a memory device that supports multi-core processing functionality in memory partitioned into multiple memory blocks in a selected memory portion using functionality integrated into memory. Thus in some embodiments, the memory device **1400** can be configured such that the non-volatile memory array **1404** is partitioned into a plurality of memory blocks **1482**. The processing logic **1406** operable to perform at least one general purpose processing function **1408** associated with the non-volatile memory array **1404** can be partitioned into a plurality of logic blocks **1484** spatially distributed over the non-volatile memory array **1404** wherein ones of the plurality of logic blocks **1484** are associated with ones of the plurality of memory blocks **1482**.

[0139] The processing logic can thus be formed into tens or even hundreds of cores. The multi-core chips can be adapted for simultaneous multi-threading and special-purpose heterogeneous cores or homogeneous cores to enhance performance and efficiency, particularly in applications such as multimedia, pattern recognition, networking, and the like. The processing logic can be configured to improve energy-efficiency by enhancing performance-per-watt with fine-grain or ultra-fine-grain power management, and dynamic voltage and frequency scaling.

[0140] In some embodiments and/or applications, the processing logic can be configured for multi-threading in an arrangement for efficiently executing multiple threads, as distinguished from multi-processing or multi-core systems. In multi-threading applications, the threads share resources of a single core. Multi-threading increases utilization of the single core via thread-level, as well as instruction level, parallelism. In some arrangements, the processing logic can support multi-processing as well as multi-threading in which multiple cores are adapted for multi-threading.

[0141] Embodiments of the processing logic can also support simultaneous multi-threading (SMT) in a configuration as a scalar processor that can issue instructions from multiple threads for each execution cycle, exploiting parallelism across multiple threads.

[0142] In some embodiments, the logic blocks and memory blocks in the memory device can be configured with multiple multi-core processors allocated to the logic blocks and inter-logic block interrupts for signaling between the multiple processing elements of the multi-core processors. The logic blocks can include interrupt controllers that generate inter-logic block interrupts for write operations directed to selected locations in the memory blocks. The write-responsive interrupts assist communication between routines and programs executing on different cores. One example inter-logic block communication technique can use a polling method for phenomena detection. One or more of the multi-core processors can poll a component such as a register for detection of phenomena, such as by performing an execution loop that includes reading the component. Once the phenomena is detected, execution is directed to a handling routine. In another example inter-logic block communication technique, a timer can be set to activate the handling routine, rather than using polling. In a further example inter-logic block communication technique, an interrupt controller can generate one or more types of interrupts that can be assigned a priority which use interrupt vectors to direct execution to an interrupt service routine executing in selected multi-core processors in the logic blocks. Interrupt-based phenomena detection improves efficiency over polling.

[0143] Accordingly, processing logic adapted for multi-core processing can be operable to monitor memory accesses, determine statistics on type and number of instructions of the monitored memory accesses, and predict a sequence of instructions and data using the determined statistics. The logic can oversee operations of an overall system, maintaining statistics on the type and number of instructions communicated and processed. In some embodiments, logic can be operable to monitor memory accesses, detect a pattern of instructions and data from the monitored memory accesses, predict expected instructions and data from the detected pattern of instructions and data using, for example, a probability sampling, and preprocessing the predicted expected instructions. In probability sampling, instructions and/or data in the population of instructions and/or data can have a greater than zero probability of being selected in the sample, and the

probability can be accurately determined. In some applications, the logic can use the statistics to predict a future sequence of instructions and data. The logic can detect patterns in which a first sequence of data and/or instructions is commonly followed by a second sequence. Upon detection of such a first sequence, the logic can apply the second sequence to the memory without actually receiving the second sequence, for example from a processor via the data bus. Thus, the logic can accelerate data handling and work throughput. The logic can monitor data and/or instructions and anticipate requests for memory. The logic can also detect an indexing pattern of instructions and interactions with memory using specialized logic that is integrated into the non-volatile memory area, enabling preprocessing of expected instructions within the memory. The logic thus can perform statistical operations that analyze instruction sequences to predict the type of instructions to perform using logic that is distributed within the non-volatile memory arrays of the memory device.

[0144] In example embodiments, the memory device **1400** can be arranged in a manner that the non-volatile memory array **1404** is partitioned into a plurality of memory blocks **1482** characterized by a plurality of different operating characteristics **1486**. The processing logic **1406** operable to perform at least one general purpose processing function **1408** associated with the non-volatile memory array **1404** can be partitioned into a plurality of logic blocks **1484** spatially distributed over the non-volatile memory array **1404** wherein ones of the plurality of logic blocks **1484** are associated with ones of the plurality of memory blocks **1482** at least partly based on the operating characteristics **1486** of the plurality of memory blocks **1482**. An operation at bootstrap loading can cause the system to report on the operating condition of all components (including all chunks of memory) to enable allocation of functionality based on performance of the components.

[0145] The partitioned logic blocks and memory blocks can be exploited to improve parallel execution wherein a large number of small tasks can be specified to attain a fine-grained decomposition of an application. Tasks allocated to partitions can execute concurrently, but typically not independently. The computation to be performed in one task typically uses data associated with another task. Data is transferred between tasks to proceed with the computation with a specified information flow that is facilitated by intercommunication among the different partitioned logic blocks and memory blocks.

[0146] In some applications and/or embodiments, different memory blocks can be allocated for respective different functionality so that the logic blocks can support functionality that is specific to the appropriate memory blocks.

[0147] In some embodiments, the memory device can be constructed with standard blocks for creating customized configurations for multi-core processing. The interface to external devices can be a standard interface with additional support for advanced functions in the memory device.

[0148] In example embodiments, the multiple logic blocks and corresponding memory blocks can be configured for dynamic voltage scaling that is allocated among the different blocks according to operating characteristics to facilitate power management so that the voltage used in a block is increased or decreased to conserve power, increase performance, increase reliability, and the like. Similarly, the memory device can be configured for dynamic frequency scaling in which the frequency of the logic blocks and associated memory blocks can be adjusted dynamically to conserve power or to reduce generated heat on the memory device.

[0149] In a particular application, the memory device can include logic that restores a persistent application state by mapping non-volatile memory pages across system reboot operations, for example by mapping non-volatile RAM pages in different processes including processes that are not necessarily concurrent. The logic can also support access control in portions of the non-volatile RAM in the manner of file system access control.

[0150] Some types of memory can be susceptible to failure under specified conditions. For example, two-terminal non-volatile memory devices based on resistance switching effects, called memristors, are susceptible to damage from temperature and bias field conditions. Placing a memristor in an oven or applying a bias field can erase the entire memory. A memory device can include a portion of memory which is susceptible to a particular condition and another, redundant portion which is resistant to the condition, thereby enabling operation in a RAID (redundant array of independent disk) array fashion to ensure retention of data during condition episodes. In case of accidental erasure, the logic can perform functionality analogous to that of a RAID array, for example, to use a slow memory that is impervious to magnetic fields to rebuild the erased data. In a particular embodiment, the slow memory can maintain hash tables are can be heat or magnetic-resistant. A two-way hash can be used to represent data as a hash, thereby reducing memory size.

[0151] The memory device can include logic that facilitates accessing of memory based on a determination of the type of operations being performed. For example, the logic can detect high traffic in video streaming and modify data handling to shift from 16-bit byte memory accesses to accessing of blocks of data. For cloud computing applications which are limited by bandwidth, the logic in the locally-controlled memory device can push all physical parameters off an external processor into the memory device, avoiding the bandwidth limitation and enabling additional memory-local capability including potentially different error correction algorithms. The memory device can thus enable a large scale memory with local control, such as a video memory with frame buffers or a dedicated image memory.

[0152] In some applications and/or embodiments, a memory device can incorporate reduced data set redundancy in which a data copy can be compressed in a suitable manner. The logic can perform redundant data management relatively slowly, avoiding the heat buildup that can result from a fast data transfer. Thus, redundant backup memory buses can be run at comparatively slow speed, thereby avoiding a significant increase in the heat budget for redundancy processing.

[0153] The control store can be configured to enable new operations. For example, the logic can be configured to facilitate efficient memory accesses. In a particular example, the logic can support a particular type of special image store which stores information of a particular size and form efficiently in memory, that writes different memory elements concurrently to a value that is suitable according to characteristics of the incoming image data. Special instructions can be used that can efficiently perform transforms on the image data.

[0154] Different types of memory can have different operating characteristics. The memory device can be formed of multiple memory segments that have different operating

characteristics, for example in aspects of speed, power consumption, size, as well as susceptibility or resistance to particular operating conditions such as magnetic field characteristics, temperature, and voltage. The logic can operate as a memory controller integrated with the non-volatile memory array to optimize for the particular memory type depending, for example, on application constraints such as the amount of computation, energy consumption load, and many other conditions. For example, logic metadata can supplies intra-memory hints about heat generation.

[0155] For example, in some embodiments, the memory device can include both phase change memory (PCRAM) and other memory types and the logic can assign memory usage according to various operating characteristics such as available power. In a specific example, PCRAM and DRAM may be selected based on power considerations. PCRAM access latencies are typically in the range of tens of nanoseconds, but remain several times slower than DRAM. PCRAM writes use energy-intensive current injection, causing thermal stress within a storage cell that degrades current-injection contacts and limits endurance to hundreds of millions of writes per cell. In a memory device that uses both PCRAM and DRAM, the logic can allocate memory usage according to the write density of an application.

[0156] A memory device can allocate memory for a particular application or operation based on scalability, for example by determining whether a substantial number of storage cells is to be used. PCRAM can be a highly scalable memory technology since thermal resistivity increases, contact area decreases, and the volume of phase-change material to block current flow decreases with feature size. As feature size becomes smaller, contact area decreases quadratically, and reduced contact area causes resistivity to increase linearly, causing programming current to decrease linearly. Thus PCRAM can attain not only smaller storage elements but also smaller access devices for current injection, leading to lower memory subsystem energy. Thus, the logic can allocate PCRAM segments to applications characterized by large memory use and density.

[0157] In some embodiments and/or applications, the memory device can be configured to allocate different portions of memory that have differing characteristics to specific applications. Some characteristics of memory can be better for some applications. For example, the logic can assign data in high-speed operations to high-speed memory while assigning less time-critical applications to slower memory. The logic can assign frequently updated information to memory types that are more durable to writes. In another example application, the memory device can be used in an end-to-end image storage system which includes multiple types of memory including multiple types of non-volatile RAM. For example, the memory device can be used to supply inexpensive memory such as memory stripes that are not part of a device such as a picture telephone, but is used to accumulate data (such as pictures) using some mirror communications that are facilitated by intelligence supplied by the logic. In an example application, the logic can activate to perform data communication when the memory device is in a location sufficiently proximal to the picture telephone to enable data transfer. The logic can be used to detect that the picture telephone and the memory device are sufficiently close to perform a data transfer and, if so, operate in a low operation, low power mode to perform the data communication. Accordingly, the intelligence of the logic can enable data transmission when the memory is in any location that is sufficiently close to the data source.

[0158] In some embodiments, the memory device can include some memory that is unacceptable for standard processing but very inexpensive and thus may have some usefulness and cost-effectiveness in some operations. For example, a relatively fast but error-prone memory may be useful for video processing. In various applications, the basis of memory quality may vary, for example, error rate, speed, and the like.

[0159] The memory device can thus be used for a wide variety of data communication operations to enable concentration of data originating from many sources. In particular arrangements, a memory device can include multiple types of memory with multiple memory characteristics in terms of cost, price, power, reliability, and the like. A memory device can be optimized to any desired characteristic such as memory quality, memory power, cost in terms of number of electrons, noise, power consumption, and others. For example, power consumption can be optimized by lowering access threshold. The logic can be configured to determine the source of noise, for example if noisy during writing, the logic can determine how little write current can be used, thereby reducing power consumption. The logic can be used to monitor electrical characteristics such as power or charge. Only so many electrons are available in a memory and the logic can be configured to determine how few electrons can be used to perform a particular operation such as read/write operations.

[0160] The memory device can include multiple types of memory including the non-volatile memory array in the form of multiple types of non-volatile memory technologies, in addition to portions of memory that may be volatile. The memory device may include multiple types of memory for use in a redundant fashion. Accordingly, the memory device can include two or more memory segments of any non-volatile memory type or technology including read-only memory, flash memory, ferroelectric random access memory (F-RAM), magneto-resistive RAM (M-RAM) or the like. The logic can operate a segment of M-RAM which is comparable in speed and capacity to volatile RAM while enabling conservation of energy, rapid or instantaneous start-up and shutdown sequences. In other applications, the memory device can include memory in the form of charge-coupled devices (CCDs) that are not directly addressable or other pure solid state memory that is reliable and inexpensive for use as separate memory device for various applications such as cell phones, and the like.

[0161] In a memory device that includes multiple different types of memory including a spin-transfer M-RAM, the logic can assign functionality at least in part based on the magnetic properties of memory. In a system that includes at least one portion of F-RAM, the logic can exploit operating characteristics of extremely high endurance, very low power consumption (since F-RAM does not require a charge pump like other non-volatile memories), single-cycle write speeds, and gamma radiation tolerance. The memory device can include different segments of different types of memory including volatile and non-volatile memory, flash, dynamic RAM (DRAM) and the like, and use the logic to attain different performance/cost benefits.

[0162] The memory device can, in addition to including multiple types of memory, can include multiple different

classes of memory of the same memory type to attain a desired operating characteristic. The different classes of memory may include memory of the same technology with different operating parameters or different fabrication process parameters. The different classes of memory may be formed with different polysilicon types, different metal types, different silicides or salicides, various source, gate, and spacer dimensions, different annealing processes, and any other suitable variation in fabrication technique.

[0163] In some embodiments and/or applications, the logic can allocate instruction cache and data cache depending on the application and environment. In further arrangements, the logic can also select physical locations of memory depending on application and operating environment.

[0164] Thus, the logic can be operable to perform maintenance operations of the memory in response to physical phenomena imposes on the memory. For example, the memory device can incorporate sensors or other components that detect phenomena which can be monitored by the logic to detect magnetic fields, electrical conditions, temperature, and the like to enable the logic to perform actions to maintain, repair, clean, or other operations applied to the memory.

[0165] In a particular application, the processing logic can be used to facilitate sampling, for example in seeking knowledge about the cause system of which an observed condition is an outcome. Sampling theory can treat the observed condition as a sample of a larger super-condition or for handling a condition from which a sample is drawn may not be the same as a condition for which information is sought. In the application of failure prediction, the logic can analyze the monitored operating characteristics, detect a precursor to a memory failure based on the analysis, and allocate memory accesses based on the detected precursor. Accordingly, the logic can be used to predict how and when failures will take place using any suitable information for making the prediction. For example, the logic can use temperature measurements to predict failure or use various forms of information to make predictions. In a particular embodiment, the logic can enable writing data at a high rate in some conditions and limit writing speed in other conditions. For example, at high temperatures for a memory that is susceptible to failure, the logic can limit writing speed to a low rate while allowing higher write data rates at lower temperature. In some applications or contexts, the logic can perform performance mapping at selected time intervals, for example updating a map of sections of memory every 10,000 writes. The operating logic can determine how the memory is used and project back to determine characteristics of the operating environment.

[0166] One problem inherent to non-volatile memory is failure that results from multiple writes to a memory element. The logic can operate to suitably allocate and distribute writes to non-volatile memory cells to avoid or prevent failure, for example by shifting through memory as particular cells are written or by allocating newer or less-written memory to operations, applications, or contexts characterized by a requirement for higher accuracy.

[0167] In an example embodiment, the memory device can include logic can allocate writes according to memory type. For example, the memory device can include a section of PCRAM. Writes can result in substantial wear in PCRAM. When current is injected into a volume of phase-change material, thermal expansion and contraction degrade the electrode storage contact, resulting in programming currents injected into the memory cell that are insufficiently reliable. PCRAM material resistivity is highly dependent on current injection so that current variability leads to resistance variability, degrading the read window of suitable programmed minimum and maximum resistances. Accordingly, the logic and monitor and determine applications characterized by repeated and enduring writes, and allocate such applications to memory segments other than PCRAM segments.

[0168] A memory device can be configured with logic that is operable to mitigate wear and energy. For example, PCRAM, which is susceptible to wear and failure for high levels of writing to a PCRAM cell over a memory lifetime, can be managed using mitigation techniques of write reduction and leveling to improve PCRAM endurance. In a particular operation, the logic can allocate some memory to function as a cache and track written cache lines and written cache words to implement partial writes and reduce wear. In another technique, the logic can monitor writes to eliminate redundant bit writes. In a typical memory access, a write updates an entire row of memory cells, many of which are redundant. The logic can remove the redundant bit writes and thereby substantially increase memory lifetimes, for example by preceding a write with a read and compare. Following the read, an XNOR gate can be used to filter redundant bit-writes. A PCRAM read is sufficiently faster than a PCM write and writes are less latency critical, so the performance reduction from reading before a write is in consequential.

[0169] In addition to eliminating redundant writes, the logic can also improve write wear performance by row shifting. After removing redundant bit writes, bits most written in a row tend to be localized so that the logic can perform simple shifting to more evenly distribute writes within a row.

[0170] The logic can attain additional wear improvement by segment swapping in which memory segments of high and low write accesses are periodically swapped. The logic can track write counts and manage a mapping table between segments.

[0171] In another example embodiment, the memory device can include logic operable to allocate memory according to wear such as by limiting the frequency of allocation for a particular memory block and by maintaining frequently changing metadata in DRAM that is separate from managed blocks of non-volatile memory.

[0172] Embodiments of the memory device can perform wear-leveling via managed allocation. For example, the logic can avoid allocation of a newly released memory block but rather time-stamp the block and add the block to a first-in-first-out queue. On subsequent allocations or releases, the logic can examine the block at the head of the queue and, if resident on the queue for a sufficient time, can remove the block from the queue and mark eligible for re-allocation. The logic can maintain list pointers in headers and footers of freed blocks and update the list pointers when adjacent free blocks are merged into a larger free region. In another technique, the logic can track the allocated or free state of memory blocks using a DRAM bitmap and manage the bitmap dynamically during operations.

[0173] In an example arrangement, the memory device can include memory of two types, such as non-volatile RAM (NVRAM) and DRAM in combination with logic that allocates memory accesses for the NVRAM. The logic prevents frequent reuse of memory locations and stores frequently-changing metadata in DRAM. Processing logic can also add checksums to detect and correct corruption.

[0174] In embodiments adapted to promote write durability, the memory device can include a non-volatile memory array with multiple types of memory including at least one portion of memory characterized by elevated write endurance. In a particular embodiment, the non-volatile memory array can include at least on portion formed of M-RAM which is based on a tunneling magneto-resistive (TMR) effect. The individual M-RAM memory cells include a magnetic tunnel junction (MTJ) which can be a metal-insulator-metal structure with ferromagnetic electrodes. A small bias voltage applied between the electrode causes a tunnel current to flow. The MTJ is exposed to an external magnetic field and forms a hysteresis loop with two stable states, corresponding to 0 and 1 data states at zero magnetic field. M-RAM is characterized among non-volatile memory technologies as having excellent write endurance with essentially no significant degradation in magneto-resistance or tunnel junction resistance through millions of write cycles. Accordingly, the logic can monitor and determine whether a particular application or process is characterized by frequent, enduring write operations and assign a portion of M-RAM to handle memory accesses.

[0175] Another memory technology characterized by write endurance is ferroelectric RAM (FeRAM). FeRAM can be constructed using material such as lead-zirconate-titanate (PZT), strontium-bismuth-tantalate (SBT), lanthanum substituted bismuth-tantalate (BLT), and others. An externally applied electric field causes polarization of the FeRAM material to be switched and information retained even upon removal of the field. In absence of the electric field, polarization has two distinct stable states to enable usage in memory storage. FeRAM can have write endurance at the level of M-RAM and is further characterized by a reduced cell size and thus higher density. Thus, the logic can monitor and determine whether a particular application or process is characterized by frequent, enduring write operations in combination with a relatively large number of storage cells. The logic can assign a portion of FeRAM to handle memory accesses.

[0176] In a particular embodiment, the memory device can include the non-volatile memory array which is inexpensive and can be maintained in close proximity to other types of memory either internal to the memory device or in a nearby integrated circuit chip. The logic can be configured to perform bit-error correction by maintaining multiple copies of data in the high capacity enabled by non-volatile memory arrays, rather than the bit-checks of other error correction techniques. The multiple copies of data in the non-volatile memory can be used to occasionally detect errors using the multiple data copies. Accordingly, the memory device can include a relatively high capacity non-volatile memory array with high capacity and logic operable to perform error correction. The high capacity in non-volatile memory can be used for error detection and correction in which redundant data is held in the non-volatile memory for error correction in the form of multiple data copies to enable recovery by the receiving memory even when a number of errors up to the capability of the code in use are introduced during transmission or on storage. Errors can be corrected without requesting retransmission by the sender.

[0177] Referring to FIGS. **15**A and **15**B, schematic block diagrams show respective top and side view of an embodiment of a memory device that supports multi-core processing functionality integrated into memory and includes optical silicon enabling communication independent of a bus structure which is functionality integrated into memory. Accordingly, the memory device **1500** can further include optical silicon **1588** operable to communicate optically, independently of a bus **1576** coupled to the memory device **1500**. The processing logic **1506** operable to perform at least one general purpose processing function **1508** associated with the non-volatile memory array **1504** can be operable to receive information via the optical silicon **1588** and read data from a selected portion of the non-volatile memory array **1504** only if authorized by the received information **1578**. Usage of optical silicon can enable the memory device to avoid the bandwidth and bottleneck problems of a system bus. The optical silicon can enable data to pass more quickly from outside the memory device to the memory. The memory device can support a WiFi network which optimizes memory for a particular application. Optical silicon can be used to alleviate some of the bandwidth problem for reading high volumes of data, such as for moving photographs from a camera or camera-phone to a storage device such as a computer or library.

[0178] For example, an optical sensor or silicon-based optical data connection can use silicon photonics and a hybrid silicon laser for communication between integrated circuit chips at distributed locations using plasmons (quanta of plasma oscillation) to communicate over relatively long distances, for example 2-3 inches on a narrow nano-wire coupler. The plasmon is a quasiparticle that results from quantization of plasma oscillations. Data can be received and converted using an optical antenna, a nano-cavity, or a quantum dot. The communication field can travel independently of a wired bus structure. For example, the memory device can receive information via the optical link, independently of the system bus connected to a processor, and the logic can use the extra-bus information to perform management or housekeeping functions to track applications and/or processes (or, for example, bit correction) via data sent optically to the memory device. The optical link thus enables low-bandwidth, back-channel communication, enabling formation of a memory that can communicate with large bursts of data for placement with optical accessibility.

[0179] The memory device can use the optical communication interface to substantially increase bandwidth. For example, dynamic random access memory (DRAM) cannot maintain synchrony over a distance of about four inches so that DRAM must be within four inches or less of a communicating processor, resulting in the memory bus becoming a data choke point, which can be relieved by the optical communication interface. Embodiments of the memory device with an optical interface can use the logic to perform bus control operations using an optical clock and interferometry using interfering optical beams to accelerate data communication.

[0180] In some specific embodiments, the optical silicon interface can be operated by the logic to increase data communication speed and reliability by constructing signals in the form of a sine-wave in a piece-wise manner, measuring segments above and below a base line and assigning digital values as 0 or 1 depending on wave position. Accordingly, formation of square wave signals is avoided, which attains benefits to heat dissipation, which is proportional to frequency squared.

[0181] Referring to FIG. **16**, a schematic block diagram shows an embodiment of an information processing system including a memory device that supports multi-core process-

ing functionality integrated into memory. Accordingly, in some embodiments, an information processing system **1600** can include means **1666** for storing information including processing logic **1606** integrated in combination with non-volatile memory array **1604** integrated on a substrate **1602**, and means **1668** for performing at least one general purpose processing function **1608** associated with the non-volatile memory array **1604**.

[0182] In an example embodiment, the information processing system **1600** can include a hybrid memory **1672** that includes multiple memory segments **1674** characterized by a multiple different operating characteristics. The hybrid memory **1672** can store data **1676** communicated from a processor **1678**. The information processing system **1600** can further include logic for performing encryption operations on the data **1676** during transfers between the memory segments **1674**.

[0183] In some embodiments, the information processing system **1600** can be constituted wherein the logic operable to perform encryption operations is operable to perform encryption operations on the data **1676** during transfers between the processor **1678** and the multiple memory segments **1674**.

[0184] The multiple memory segments **1674** can be arranged to include various types of memory with different characteristics and speeds, for example the multiple memory segments **1674** can comprise volatile main memory **1680**, non-volatile main memory **1604**, or a combination of memory types.

[0185] In particular embodiments, the multiple memory segments **1674** can constitute a volatile main memory **1680** and a non-volatile main memory **1604** wherein the volatile main memory **1680** has faster operating characteristics than the non-volatile main memory **1604**. For example, the multiple memory segments **1674** can be formed in memory subsystem combining DRAM and a large amount of nonvolatile memory such as flash or phase change memory (PCM).

[0186] In some information processing system **1600** embodiments, the multiple memory segments **1674** can include a cache **1682**. In an example embodiment, DRAM can operate as a cache **1682** for the PCM or nonvolatile memory, facilitating channel encryption between the processor **1678** and the information processing system **1600**. The logic operable to perform encryption operations can decrypt the information encrypted by the processor **1678** and sent over the channel and store the decrypted information in the DRAM, then can use storage encryption when passing the information from the DRAM to the PCM or nonvolatile memory **1604**.

[0187] Various embodiments of the information processing system **1600** can be configured for channel encryption. For instance, the logic operable to perform encryption operations can function to encrypt data **1676** on a communication channel **1684** that communicates information between the processor **1678** and the hybrid memory **1672**.

[0188] The information processing system **1600** can be configured to perform one or more of several channel encryption operations in cooperation with a processor **1678**. For instance, the logic operable to perform encryption operations can operable to decrypt information encrypted by the processor **1678**. In some embodiments and/or conditions, the logic operable to perform encryption operations is operable to decrypt address and data information encrypted by the processor **1678** and store data at the address in the hybrid memory **1672**. Similarly, the information processing system **1600** can be configured wherein the logic operable to perform encryption operations is operable to partially decrypt information encrypted by the processor **1678**.

[0189] Some embodiments of the information processing system **1600** can include processing logic **1606**, for example which can be closely associated to and integrated onto the information processing system **1600** chip. Accordingly, the processor **1678** can implement at least one general purpose processing function **1608** in association with the hybrid memory **1672** and coupled to the logic operable to perform encryption operations. The processing logic **1606** can be operable to perform general purpose processing functions **1608** using encrypted information.

[0190] The information processing system **1600** can be configured to implement one or more of a variety of security schemes including channel encryption, storage encryption, RSA (Rivest, Shamir, Adleman) cryptography and key distribution, Public Key Infrastructure (PKI). Accordingly, the logic operable to perform encryption operations can be operable to perform stream encryption of communicated information wherein processor and memory sides are assigned a key. In another example functionality, the logic operable to perform encryption operations can be operable to encrypt information that is storage encrypted wherein the storage-encrypted information is encrypted by the processor **1678**, stored in the hybrid memory **1672**, accessed from the hybrid memory **1672**, and decrypted by the processor **1678**.

[0191] In some embodiments and/or applications, the information processing system **1600** can be configured to use of cryptographic processing to facilitate information handling. For example, data can be copied for redundant storage and the redundant copy can be secured by encryption and stored in the non-volatile memory in encrypted form. The encrypted redundant copy of the data can be used for restoration in the event of a detected error. In another example, A cryptographic hash function generates information indicative of data integrity, whether changes in data are accidental or maliciously and intentional. Modification to the data can be detected through a mismatching hash value. For a particular hash value, finding of input data that yields the same hash value is not easily possible, if an attacker can change not only the message but also the hash value, then a keyed hash or message authentication code (MAC) can supply additional security. Without knowing the key, for the attacker to calculate the correct keyed hash value for a modified message is not feasible.

[0192] In a particular applications and/or arrangements, the security perimeter can be formed within the information processing system **1600** and, for example, enclose the entire information processing system **1600**, between dynamic random access memory (DRAM) and the information processing system **1600**, between non-volatile random access memory (RAM) and the information processing system **1600**, or any other suitable position. The cryptographic and/or tamper-handling perimeter can further be generalized for positioning between a smaller amount of memory and a larger amount of memory in the information processing system **1600**. Some embodiments can include a cryptographic perimeter in the absence of a tamper-handling perimeter.

[0193] In some embodiments, the logic operable to perform encryption operations can be operable to perform time-varying encryption. For example, channel encryption assisted by the information processing system **1600** can enable randomization of encrypted information wherein encrypted data is

read back and encryption can be stripped off by the receiving processor **1678**. The information processing system **1600** with logic or other smart component can enable time-varying encryption. Data can be written to an address which, when read back, is different, but no information is lost since the reading processor **1678** or other reading device at the opposite side of the channel from the smart memory has sufficient intelligence capability to strip off the encryption.

[0194] In an example embodiment, the information processing system can include logic can allocate writes according to memory type. For example, the information processing system can include a section of PCRAM. Writes can result in substantial wear in PCRAM. When current is injected into a volume of phase-change material, thermal expansion and contraction degrade the electrode storage contact, resulting in programming currents injected into the memory cell that are insufficiently reliable. PCRAM material resistivity is highly dependent on current injection so that current variability leads to resistance variability, degrading the read window of suitable programmed minimum and maximum resistances. Accordingly, the logic and monitor and determine applications characterized by repeated and enduring writes, and allocate such applications to memory segments other than PCRAM segments.

[0195] A information processing system can be configured with logic that is operable to mitigate wear and energy. For example, PCRAM, which is susceptible to wear and failure for high levels of writing to a PCRAM cell over a memory lifetime, can be managed using mitigation techniques of write reduction and leveling to improve PCRAM endurance. In a particular operation, the logic can allocate some memory to function as a cache and track written cache lines and written cache words to implement partial writes and reduce wear. In another technique, the logic can monitor writes to eliminate redundant bit writes. In a typical memory access, a write updates an entire row of memory cells, many of which are redundant. The logic can remove the redundant bit writes and thereby substantially increase memory lifetimes, for example by preceding a write with a read and compare. Following the read, an XNOR gate can be used to filter redundant bit-writes. A PCRAM read is sufficiently faster than a PCM write and writes are less latency critical, so the performance reduction from reading before a write is in consequential.

[0196] In some embodiments and/or applications, the logic can allocate instruction cache and data cache depending on the application and environment. In further arrangements, the logic can also select physical locations of memory depending on application and operating environment.

[0197] In addition to eliminating redundant writes, the logic can also improve write wear performance by row shifting. After removing redundant bit writes, bits most written in a row tend to be localized so that the logic can perform simple shifting to more evenly distribute writes within a row.

[0198] The logic can attain additional wear improvement by segment swapping in which memory segments of high and low write accesses are periodically swapped. The logic can track write counts and manage a mapping table between segments.

[0199] In another example embodiment, the information processing system can include logic operable to allocate memory according to wear such as by limiting the frequency of allocation for a particular memory block and by maintaining frequently changing metadata in DRAM that is separate from managed blocks of non-volatile memory.

[0200] Embodiments of the information processing system can perform wear-leveling via managed allocation. For example, the logic can avoid allocation of a newly released memory block but rather time-stamp the block and add the block to a first-in-first-out queue. On subsequent allocations or releases, the logic can examine the block at the head of the queue and, if resident on the queue for a sufficient time, can remove the block from the queue and mark eligible for re-allocation. The logic can maintain list pointers in headers and footers of freed blocks and update the list pointers when adjacent free blocks are merged into a larger free region. In another technique, the logic can track the allocated or free state of memory blocks using a DRAM bitmap and manage the bitmap dynamically during operations.

[0201] Referring to FIGS. **17**A and **17**B, a schematic block diagram and a side pictorial view illustrate an embodiment of an information processing circuit including memory that supports multi-core processing functionality and is functionality integrated into memory. An embodiment of an information processing circuit **1700** can include a memory circuit **1768** including processing logic **1706** integrated with non-volatile memory array **1704** on a substrate **1702**, and circuitry **1770** for performing at least one general purpose processing function **1708** associated with the non-volatile memory array **1704**.

[0202] Embodiments of an information processing circuit **1700** can make use of a memory stack **1772** to facilitate intelligent memory computation. In a particular example embodiment, intelligent memory computation can include security capabilities, including cryptographic security. The information processing circuit **1700** can be constituted to facilitate channel encryption through operation of the logic operable to perform encryption operations. Accordingly, the logic operable to perform encryption operations can be operable to perform channel encryption operations on a communication channel **1786** that communicates information between the processor **1778** and the memory stack **1772**. Channel encryption can improve performance and economy in various applications and conditions in comparison to expensive storage encryption. The logic operable to perform encryption operations can facilitate good memory encryption, for example between the processor **1778** and the memory stack **1772**. An illustrative configuration can include a CPU that interacts with the memory stack **1772** comprising multiple DRAM chips and the logic operable to perform encryption operations integrated into a logic chip operable to perform strong channel encryption between the CPU and the memory stack **1772**.

[0203] In various embodiments, the information processing circuit **1700**, the memory stack **1772**, and the logic operable to perform encryption operations can be constituted to perform one or more of several security operations. For example, the logic operable to perform encryption operations is operable to decrypt information encrypted by the processor **1778**. Similarly, the logic operable to perform encryption operations is operable to partially decrypt information encrypted by the processor **1778**. The logic can also be operable to perform encryption operations is operable to perform stream encryption of information communicated on a communication channel **1786** wherein processor and memory sides of the communication channel **1786** are assigned a key. In an embodiment or circumstances where security can be best attained by using a combination of storage encryption and channel encryption, the logic operable to perform encryp-

tion operations is operable to perform channel encryption operations on a communication channel **1786** for information that is storage encrypted wherein the storage-encrypted information is encrypted by the processor **1778**, stored in the memory stack **1772**, accessed from the memory stack **1772**, and decrypted by the processor **1778**. The logic operable to perform encryption operations can also be operable to perform time-varying encryption.

[0204] Information can be stored in the memory stack **1772** unencrypted or the logic can encrypt the data for storage. Thus, channel encryption can be performed between the CPU and a logic chip, enabling cryptographic security without requiring storage encryption of data stored in the logic chip.

[0205] In various embodiments, a memory device with integrated logic and memory can be integrated into a product. For example, the memory device can be integrated to a product in the form of a security device for securing an item such as a home, an automobile, or any other item of value. The memory device can monitor conditions of the product autonomously of devices external to the product, while supporting updates to the memory device.

[0206] In other embodiments, the memory device can be integrated into other products, for example electronic devices, such as mobile and cell phones, notebook computers, personal digital assistants, medical devices, medical diagnostic systems, digital cameras, audio players, digital televisions, automotive and transportation engine control units, USB flash personal discs, and global positioning systems.

[0207] In other applications and/or contexts, a memory system can be formed of printed non-volatile memory on polymer. In some arrangements, a printed non-volatile memory on polymer can form flexible memories. For example, a flexible memory can be integrated with processors for further integration into any type of product, even very simple products such as bottles, cans, or packaging materials. A non-volatile memory can be integrated in a system of any suitable product such as, for example, a door handle sleeve to detect and record who, what, when, and how anyone has touched the door handle. Such a system can be used to facilitate access or to provide security. In other examples, a non-volatile memory and processor in some applications with sensors and/or a communication interface can be used in a flexible device for a medical product such as bandages or implants. These products can be formed of dissolvable materials for temporary usage, for example in biocompatible electronic or medical devices that can dissolve in a body environment, or environmental monitors and consumer electronics that can dissolve in compost. Other applications of products incorporating non-volatile memory and processor can include sporting equipment, tags such as for rental cars, patient armbands in hospitals tied to sensors, smart glasses, or any type of device.

[0208] In further embodiments, instead of a flexible polymer, the non-volatile memory and processor can be formed of silicon that is sufficiently thin to become flexible and thus formed as an inexpensive printed circuit component. Flexible memory in ubiquitous items, using polymer memory or silicon memory, can enable various profitable services, for example in conjunction with medical devices, security services, automotive products, and the like.

[0209] In embodiments of the memory device with processing capability of logic integrated in a distributed manner with non-volatile memory, the processing capability can be implemented with relatively low speed requirement to enable processors to be available in a ubiquitous manner. Accordingly, information can be acquired in a dispersed manner and intercommunicated over vast systems. Thus processors can be inexpensive and memory readily available for various consumer items. Custom versions of memory including non-volatile memory and RAM can be integrated into virtually any product, enabling widespread preprocessing in items such as door handles to determine who has accessed a location and how the access was made to allow any type of processing on the information.

[0210] Referring to FIGS. **18**A through **18**X, multiple schematic flow charts show several embodiments and/or aspects of a method of manufacturing a memory device that supports multi-core processing functionality integrated into memory. The illustrative method **1800**, depicted in FIG. **18**A, of manufacturing a memory device can include forming **1801** a non-volatile memory array on a substrate, and integrating **1802** processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1803** at least one general purpose processing function associated with the non-volatile memory array.

[0211] Referring to FIG. **18**B, in some embodiments, the method **1804** of manufacturing a memory device can include forming **1805** a non-volatile memory array on a substrate, and integrating **1806** processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1807** at least one general purpose processing function associated with the non-volatile memory array.

[0212] In further embodiments and/or applications, as shown in FIG. **18**C, the method **1808** of manufacturing the memory device can further include configuring **1809** the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array with functionality selectively distributed **1810** across the non-volatile memory array.

[0213] In various embodiments, as depicted in FIG. **18**D, the method **1811** of manufacturing the memory device can further include integrating **1812** embedded central processing unit logic into the processing logic in combination with the non-volatile memory array on the substrate in close association **1813** in function and location with a memory portion of the non-volatile memory array.

[0214] Referring to FIG. **18**E, in some embodiments, the method **1814** of manufacturing the memory device can further include integrating **1815** a plurality of embedded processing blocks into the processing logic in combination with the non-volatile memory array on the substrate in respective close association **1816** in function and location with a plurality of memory portions of the non-volatile memory array.

[0215] As shown in FIG. **18**F, in various embodiments and/or applications, the method **1817** of manufacturing the memory device can further include integrating **1818** a plurality of embedded processing blocks into the processing logic in combination with the non-volatile memory array on the substrate that is operable to execute **1819** parallel processing tasks for multi-core functionality in the absence of external central processing unit calls.

[0216] In some embodiments, illustrated in FIG. **18**G, the method **1820** of manufacturing the memory device can further include integrating **1821** string processing logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1822** at least one string processing function associated with the non-volatile memory array.

[0217] In various embodiments and/or applications, as shown in FIG. **18**H, the method **1823** of manufacturing the memory device can further include integrating **1824** anti-virus scanning logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1825** at least one anti-virus scanning function associated with the non-volatile memory array.

[0218] Referring to FIG. **18**I, selected embodiments of the method **1826** of manufacturing the memory device can further include integrating **1827** data compression logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1828** at least one data compression function associated with the non-volatile memory array.

[0219] As illustrated in FIG. **18**J, some embodiments of the method **1829** of manufacturing the memory device can further include integrating **1830** sorting logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1831** at least one sorting function associated with the non-volatile memory array.

[0220] As shown in FIG. **18**K, an embodiment of the method **1832** of manufacturing the memory device can further include integrating **1833** peripheral logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to manage **1834** the non-volatile memory array in response to external central processing unit calls.

[0221] Referring to FIG. **18**L, in some embodiments, the method **1835** of manufacturing the memory device can further include integrating **1836** extension logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to manage **1837** the non-volatile memory array in response to external central processing unit calls.

[0222] In further embodiments and/or applications, as shown in FIG. **18**M, the method **1838** of manufacturing the memory device can further include integrating **1839** dormant processing logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable upon activation **1840** by a signal from a device external to the memory device to perform **1841** at least one processing function associated with the non-volatile memory array.

[0223] In various embodiments, as depicted in FIG. **18**N, the method **1842** of manufacturing the memory device can further include integrating **1843** process identification logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to identify **1844** parallel processing tasks and allocating **1845** the parallel processing tasks associated with the non-volatile memory array.

[0224] Referring to FIG. **18**O, in some embodiments, the method **1846** of manufacturing the memory device can further include integrating **1847** a protection key register with the processing logic and the non-volatile memory array on the substrate, and integrating **1848** protection key logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to manage **1849** access to a selected memory portion of the non-volatile memory array based on information in the protection key register.

[0225] As shown in FIG. **18**P, in various embodiments and/or applications, the method **1850** of manufacturing the memory device can further include forming **1851** a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types in the non-volatile memory array, and configuring **1852** the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array to perform **1853** at least one general purpose processing function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0226] In various embodiments, as depicted in FIG. **18**Q, the method **1854** of manufacturing the memory device can further include coupling **1855** at least one sensor operable to detect at least one operating condition to the processing logic, and integrating **1856** processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1857** at least one general purpose processing function for the non-volatile memory array selectively based on the at least one operating condition.

[0227] Referring to FIG. **18**R, in some embodiments, the method **1858** of manufacturing the memory device can further include integrating **1859** encryption logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1860** at least one encryption/decryption function associated with the non-volatile memory array and to read **1861** data from a selected portion of the non-volatile memory array only if authorized by results of the encryption/decryption function.

[0228] As shown in FIG. **18**S, in various embodiments and/or applications, the method **1862** of manufacturing the memory device can further include integrating **1863** encryption logic into the processing logic in combination with the non-volatile memory array on the substrate that is operable to perform **1864** at least one encryption/decryption function associated with the non-volatile memory array that holds at least one encryption key secure from a device external to the memory device and operable to read **1865** data from a selected portion of the non-volatile memory array only if enabled by the encryption key.

[0229] In some embodiments, illustrated in FIG. **18**T, the method **1866** of manufacturing the memory device can further include integrating **1867** a bus with the processing logic and the non-volatile memory array on the substrate that is operable to communicate **1868** access requests and information between the memory device and a device external to the memory device.

[0230] In various embodiments and/or applications, as shown in FIG. **18**U, the method **1869** of manufacturing the memory device can further include partitioning **1870** the non-volatile memory array into a plurality of memory blocks, and partitioning **1871** the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array into a plurality of logic blocks spatially distributed over the non-volatile memory array. The method **1869** of manufacturing the memory device can further include associating **1872** ones of the plurality of logic blocks with ones of the plurality of memory blocks.

[0231] Referring to FIG. **18**V, selected embodiments of the method **1873** of manufacturing the memory device can further include partitioning **1874** the non-volatile memory array into a plurality of memory blocks, and partitioning **1875** the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array into a plurality of logic blocks spatially dis-

tributed over the non-volatile memory array. The method **1873** of manufacturing the memory device can further include associating **1876** ones of the plurality of logic blocks with ones of the plurality of memory blocks.

[0232] In various embodiments, as depicted in FIG. **18**W, the method **1877** of manufacturing the memory device can further include partitioning **1878** the non-volatile memory array into a plurality of memory blocks characterized by a plurality of different operating characteristics, and partitioning **1879** the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array into a plurality of logic blocks spatially distributed over the non-volatile memory array. The method **1877** of manufacturing the memory device can further include associating **1880** ones of the plurality of logic blocks with ones of the plurality of memory blocks at least partly based on the operating characteristics of the plurality of memory blocks.

[0233] Referring to FIG. **18**X, in some embodiments, the method **1881** of manufacturing the memory device can further include integrating **1882** optical silicon with the processing logic and the non-volatile memory array on the substrate. The processing logic is operable to receive **1883** information via the optical silicon and read **1884** data from a selected portion of the non-volatile memory array only if authorized by the received information. The optical silicon is operable to communicate **1885** optically, independently of a bus coupled to the memory device.

[0234] Referring to FIGS. **19**A through **19**U and **20**A through **201**, multiple schematic flow charts depict several embodiments and/or aspects of a method of operating a memory device that supports multi-core processing functionality integrated into memory. The illustrative method **1900**, depicted in FIG. **19**A, of operating a memory device can include providing **1901** the memory device including processing logic integrated in combination with non-volatile memory array on a substrate, and operating **1902** the processing logic. Operating **1902** the processing logic can include performing **1903** at least one general purpose processing function associated with the non-volatile memory array.

[0235] Referring to FIG. **19**B, in some embodiments, the method **1904** of operating the memory device can include providing **1905** the memory device including a plurality of embedded processing blocks integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1906** the plurality of embedded processing blocks. Operating **1906** the plurality of embedded processing blocks can include executing **1907** parallel processing tasks associated with the non-volatile memory array.

[0236] In further embodiments and/or applications, as shown in FIG. **19**C, the method **1908** of operating the memory device can include providing **1909** the memory device including a plurality of embedded processing blocks integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1910** the plurality of embedded processing blocks. Operating **1910** the plurality of embedded processing blocks can include executing **1911** parallel processing tasks for multi-core functionality in the absence of external central processing unit calls.

[0237] In various embodiments, as depicted in FIG. **19**D, the method **1912** of operating the memory device can include providing **1913** the memory device including string processing logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1914** the string processing logic. Operating **1914** the string processing logic can include performing **1915** at least one string processing function associated with the non-volatile memory array.

[0238] Referring to FIG. **19**E, in some embodiments, the method **1916** of operating the memory device can include providing **1917** the memory device including anti-virus scanning logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1918** the anti-virus scanning logic. Operating **1918** the anti-virus scanning logic can include performing **1919** at least one anti-virus scanning function associated with the non-volatile memory array.

[0239] As shown in FIG. **19**F, in various embodiments and/or applications, the method **1920** of operating the memory device can include providing **1921** the memory device including data compression logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1922** the data compression logic. Operating **1922** the data compression logic can include performing **1923** at least one data compression function associated with the non-volatile memory array.

[0240] In some embodiments, illustrated in FIG. **19**G, the method **1924** of operating the memory device can include providing **1925** the memory device including sorting logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1926** the sorting logic. Operating **1926** the sorting logic can include performing **1927** at least one sorting function associated with the non-volatile memory array.

[0241] In various embodiments and/or applications, as shown in FIG. **19**H, the method **1928** of operating the memory device can include providing **1929** the memory device including peripheral logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1930** the peripheral logic. Operating **1930** the peripheral logic can include managing **1931** the non-volatile memory array in response to external central processing unit calls.

[0242] Referring to FIG. **19**I, selected embodiments of the method **1932** of operating the memory device can include providing **1933** the memory device including extension logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1934** the extension logic. Operating **1934** the extension logic can include managing **1935** the non-volatile memory array in response to external central processing unit calls.

[0243] As illustrated in FIG. **19**J, some embodiments of the method **1936** of operating the memory device can include providing **1937** the memory device including dormant processing logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1938** the dormant processing logic. Operating **1938** the dormant processing logic can include receiving **1939** a signal from a device external to the memory device, and performing **1940** at least one processing function associated with the non-volatile memory array in response to the signal.

[0244] As shown in FIG. **19**K, an embodiment of the method **1941** of operating the memory device can include providing **1942** the memory device including process identification logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1943** the process identification logic. Operating

1943 the process identification logic can include identifying **1944** parallel processing tasks, and allocating **1945** the parallel processing tasks associated with the non-volatile memory array.

[0245] Referring to FIG. **19**L, in some embodiments, the method **1946** of operating the memory device can include providing **1947** the memory device including process identification logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1948** the process identification logic. Operating **1948** the process identification logic can include identifying **1949** a plurality of parallel processing tasks, and allocating **1950** the parallel processing tasks for multi-core functionality in the absence of external central processing unit multi-core calls.

[0246] In further embodiments and/or applications, as shown in FIG. **19**M, the method **1951** of operating the memory device can include providing **1952** a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, providing **1953** the memory device including protection key logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1954** the protection key logic. Operating **1954** the protection key logic can include managing **1955** access to a selected memory portion of the non-volatile memory array based on information in the protection key register.

[0247] In various embodiments, as depicted in FIG. **19**N, the method **1956** of operating the memory device can include providing **1957** a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, providing **1958** the memory device including protection key logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1959** the protection key logic. Operating **1959** the protection key logic can include receiving **1960** information and writing **1961** the received information to the protection key register.

[0248] Referring to FIG. **19**O, in some embodiments, the method **1962** of operating the memory device can include providing **1963** a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, providing **1964** the memory device including protection key logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1965** the protection key logic. Operating **1965** the protection key logic can include allocating **1966** parallel processing tasks for multi-core functionality based on information in the protection key register.

[0249] As shown in FIG. **19**P, in various embodiments and/or applications, the method **1966** of operating the memory device can include providing **1967** a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, providing **1968** the memory device including protection key logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1969** the protection key logic. Operating **1969** the protection key logic can include reading **1970** data from a selected memory portion of the non-volatile memory array only if authorized by information in the protection key register.

[0250] In various embodiments, as depicted in FIG. **19**Q, the method **1971** of operating the memory device can include providing **1972** a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, providing **1973** the memory device including protection key logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1974** the protection key logic. Operating **1974** the protection key logic can include writing **1975** data to a selected memory portion of the non-volatile memory array only if authorized by information in the protection key register.

[0251] Referring to FIG. **19**R, in some embodiments, the method **1976** of operating the memory device can include partitioning **1977** the non-volatile memory array into a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types, and operating **1978** the processing logic. Operating **1978** the processing logic can include performing **1979** at least one general purpose processing function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0252] As shown in FIG. **19**S, in various embodiments and/or applications, the method **1980** of operating the memory device can include partitioning **1981** the non-volatile memory array into a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types, providing **1982** the memory device including string processing logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1983** the string processing logic. Operating **1983** the string processing logic can include performing **1984** at least one string processing function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0253] In some embodiments, illustrated in FIG. **19**T, the method **1985** of operating the memory device can include partitioning **1986** the non-volatile memory array into a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types, providing **1987** the memory device including anti-virus scanning logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1988** the anti-virus scanning logic. Operating **1988** the anti-virus scanning logic can include performing **1989** at least one anti-virus scanning function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0254] In various embodiments and/or applications, as shown in FIG. **19**U, the method **1990** of operating the memory device can include partitioning **1991** the non-volatile memory array into a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types, providing **1992** the memory device including data compression logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **1993** the data compression logic. Operating **1993** the data compression logic can include performing **1994** at least one data compression function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0255] Referring to FIG. **20**A, selected embodiments of the method **2000** of operating the memory device can include partitioning **2001** the non-volatile memory array into a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types, providing **2002** the memory device including sorting logic integrated

into the processing logic in combination with non-volatile memory array on the substrate, and operating **2003** the sorting logic. Operating **2003** the sorting logic can include performing **2004** at least one sorting function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

[0256] In various embodiments, as depicted in FIG. **20**B, the method **2005** of operating the memory device can include providing **2006** at least one sensor operable to detect at least one operating condition, and operating **2007** the processing logic. Operating **2007** the processing logic can include performing **2008** at least one general purpose processing function for the non-volatile memory array selectively based on the at least one operating condition.

[0257] The illustrative method **2009**, depicted in FIG. **20**C, of operating the memory device can be arranged in a manner that operating **2010** the processing logic further includes accessing **2011** a time signal, and performing **2012** at least one general purpose processing function for the non-volatile memory array based on the time signal.

[0258] Referring to FIG. **20**D, in some embodiments, the method **2013** of operating the memory device can be configured such that operating **2014** the processing logic further includes monitoring **2015** phenomena detectable at the memory device, and performing **2016** at least one general purpose processing function for the non-volatile memory array based on the monitored phenomena.

[0259] In further embodiments and/or applications, as shown in FIG. **20**E, the method **2017** of operating the memory device can be configured such that operating **2018** the processing logic further includes accumulating and communicating **2019** information about phenomena associated with at least one entity in association with the memory device, and performing **2020** at least one general purpose processing function for the non-volatile memory array based on the monitored phenomena.

[0260] In various embodiments, as depicted in FIG. **20**F, the method **2021** of operating a memory device can include providing **2022** the memory device including encryption logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **2023** the encryption logic. Operating **2023** the encryption logic can include performing **2024** at least one encryption/decryption function associated with the non-volatile memory array, and reading **2025** data from a selected portion of the non-volatile memory array only if authorized by results of the encryption/decryption function.

[0261] Referring to FIG. **20**G, in some embodiments, the method **2026** of operating a memory device can include providing **2027** the memory device including encryption logic integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **2028** the encryption logic. Operating **2028** the encryption logic can include performing **2029** at least one encryption/decryption function associated with the non-volatile memory array that holds at least one encryption key secure from a device external to the memory device, and reading **2030** data from a selected portion of the non-volatile memory array only if enabled by the encryption key.

[0262] As shown in FIG. **20**H, in various embodiments and/or applications, the method **2031** of operating a memory device can be formed with operating **2032** the processing logic including performing **2033** the at least one general purpose processing function independently of signals external to the memory device.

[0263] In some embodiments, illustrated in FIG. **20**I, the method **2034** of operating the memory device can include providing **2035** the memory device including optical silicon integrated into the processing logic in combination with non-volatile memory array on the substrate, and operating **2036** the processing logic. Operating **2036** the processing logic can include receiving **2037** information via the optical silicon, and reading **2038** data from a selected portion of the non-volatile memory array only if authorized by the received information. The optical silicon is operable to communicate **2039** optically, independently of a bus coupled to the memory device.

[0264] Modules, logic, circuitry, hardware and software combinations, firmware, or so forth may be realized or implemented as one or more general-purpose processors, one or more processing cores, one or more special-purpose processors, one or more microprocessors, at least one Application-Specific Integrated Circuit (ASIC), at least one Field Programmable Gate Array (FPGA), at least one digital signal processor (DSP), some combination thereof, or so forth that is executing or is configured to execute instructions, a special-purpose program, an application, software, code, some combination thereof, or so forth as at least one special-purpose computing apparatus or specific computing component. One or more modules, logic, or circuitry, etc. may, by way of example but not limitation, be implemented using one processor or multiple processors that are configured to execute instructions (e.g., sequentially, in parallel, at least partially overlapping in a time-multiplexed fashion, at least partially overlapping across multiple cores, or a combination thereof, etc.) to perform a method or realize a particular computing machine. For example, a first module may be embodied by a given processor executing a first set of instructions at or during a first time, and a second module may be embodied by the same given processor executing a second set of instructions at or during a second time. Moreover, the first and second times may be at least partially interleaved or overlapping, such as in a multi-threading, pipelined, or predictive processing environment. As an alternative example, a first module may be embodied by a first processor executing a first set of instructions, and a second module may be embodied by a second processor executing a second set of instructions. As another alternative example, a particular module may be embodied partially by a first processor executing at least a portion of a particular set of instructions and embodied partially by a second processor executing at least a portion of the particular set of instructions. Other combinations of instructions, a program, an application, software, or code, etc. in conjunction with at least one processor or other execution machinery may be utilized to realize one or more modules, logic, or circuitry, etc. to implement any of the processing algorithms described herein.

[0265] Those having ordinary skill in the art will recognize that the state of the art has progressed to the point where there is little distinction left between hardware, software, and/or firmware implementations of aspects of systems; the use of hardware, software, and/or firmware is generally (but not always, in that in certain contexts the choice between hardware and software can become significant) a design choice representing cost vs. efficiency tradeoffs. Those having skill in the art will appreciate that there are various vehicles by

which processes and/or systems and/or other technologies described herein can be effected (e.g., hardware, software, and/or firmware), and that the preferred vehicle will vary with the context in which the processes and/or systems and/or other technologies are deployed. For example, if an implementer determines that speed and accuracy are paramount, the implementer may opt for a mainly hardware and/or firmware vehicle; alternatively, if flexibility is paramount, the implementer may opt for a mainly software implementation; or, yet again alternatively, the implementer may opt for some combination of hardware, software, and/or firmware. Hence, there are several possible vehicles by which the processes and/or devices and/or other technologies described herein may be effected, none of which is inherently superior to the other in that any vehicle to be utilized is a choice dependent upon the context in which the vehicle will be deployed and the specific concerns (e.g., speed, flexibility, or predictability) of the implementer, any of which may vary. Those having ordinary skill in the art will recognize that optical aspects of implementations will typically employ optically-oriented hardware, software, and or firmware.

[0266] In some implementations described herein, logic and similar implementations may include software or other control structures suitable to operation. Electronic circuitry, for example, may manifest one or more paths of electrical current constructed and arranged to implement various logic functions as described herein. In some implementations, one or more media are configured to bear a device-detectable implementation if such media hold or transmit a special-purpose device instruction set operable to perform as described herein. In some variants, for example, this may manifest as an update or other modification of existing software or firmware, or of gate arrays or other programmable hardware, such as by performing a reception of or a transmission of one or more instructions in relation to one or more operations described herein. Alternatively or additionally, in some variants, an implementation may include special-purpose hardware, software, firmware components, and/or general-purpose components executing or otherwise invoking special-purpose components. Specifications or other implementations may be transmitted by one or more instances of tangible transmission media as described herein, optionally by packet transmission or otherwise by passing through distributed media at various times.

[0267] Alternatively or additionally, implementations may include executing a special-purpose instruction sequence or otherwise invoking circuitry for enabling, triggering, coordinating, requesting, or otherwise causing one or more occurrences of any functional operations described above. In some variants, operational or other logical descriptions herein may be expressed directly as source code and compiled or otherwise invoked as an executable instruction sequence. In some contexts, for example, C++ or other code sequences can be compiled directly or otherwise implemented in high-level descriptor languages (e.g., a logic-synthesizable language, a hardware description language, a hardware design simulation, and/or other such similar mode(s) of expression). Alternatively or additionally, some or all of the logical expression may be manifested as a Verilog-type hardware description or other circuitry model before physical implementation in hardware, especially for basic operations or timing-critical applications. Those having ordinary skill in the art will recognize how to obtain, configure, and optimize suitable transmission or computational elements, material supplies, actuators, or other common structures in light of these teachings.

[0268] The foregoing detailed description has set forth various embodiments of the devices and/or processes via the use of block diagrams, flowcharts, and/or examples. Insofar as such block diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood by those within the art that each function and/or operation within such block diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof. In one embodiment, several portions of the subject matter described herein may be implemented via Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, those having ordinary skill in the art will recognize that some aspects of the embodiments disclosed herein, in whole or in part, can be equivalently implemented in integrated circuits, as one or more computer programs running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and or firmware would be well within the skill of one of skill in the art in light of this disclosure. In addition, those having ordinary skill in the art will appreciate that the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies regardless of the particular type of signal bearing medium used to actually carry out the distribution. Examples of a signal bearing medium include, but are not limited to, the following: a recordable type medium such as a floppy disk, a hard disk drive, a Compact Disc (CD), a Digital Video Disk (DVD), a digital tape, a computer memory, etc.; and a transmission type medium such as a digital and/or an analog communication medium (e.g., a fiber optic cable, a waveguide, a wired communications link, a wireless communication link (e.g., transmitter, receiver, transmission logic, reception logic, etc.), etc.).

[0269] In a general sense, those having ordinary skill in the art will recognize that the various embodiments described herein can be implemented, individually and/or collectively, by various types of electro-mechanical systems having a wide range of electrical components such as hardware, software, firmware, and/or virtually any combination thereof; and a wide range of components that may impart mechanical force or motion such as rigid bodies, spring or torsional bodies, hydraulics, electro-magnetically actuated devices, and/or virtually any combination thereof. Consequently, as used herein "electro-mechanical system" includes, but is not limited to, electrical circuitry operably coupled with a transducer (e.g., an actuator, a motor, a piezoelectric crystal, a Micro Electro Mechanical System (MEMS), etc.), electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described

herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of memory (e.g., random access, flash, read only, etc.)), electrical circuitry forming a communications device (e.g., a modem, communications switch, optical-electrical equipment, etc.), and/or any non-electrical analog thereto, such as optical or other analogs. Those having ordinary skill in the art will also appreciate that examples of electro-mechanical systems include but are not limited to a variety of consumer electronics systems, medical devices, as well as other systems such as motorized transport systems, factory automation systems, security systems, and/or communication/computing systems. Those having ordinary skill in the art will recognize that electro-mechanical as used herein is not necessarily limited to a system that has both electrical and mechanical actuation except as context may dictate otherwise.

[0270] In a general sense, those having ordinary skill in the art will recognize that the various aspects described herein which can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, and/or any combination thereof can be viewed as being composed of various types of "electrical circuitry." Consequently, as used herein "electrical circuitry" includes, but is not limited to, electrical circuitry having at least one discrete electrical circuit, electrical circuitry having at least one integrated circuit, electrical circuitry having at least one application specific integrated circuit, electrical circuitry forming a general purpose computing device configured by a computer program (e.g., a general purpose computer configured by a computer program which at least partially carries out processes and/or devices described herein, or a microprocessor configured by a computer program which at least partially carries out processes and/or devices described herein), electrical circuitry forming a memory device (e.g., forms of memory (e.g., random access, flash, read only, etc.)), and/or electrical circuitry forming a communications device (e.g., a modem, communications switch, optical-electrical equipment, etc.). Those having skill in the art will recognize that the subject matter described herein may be implemented in an analog or digital fashion or some combination thereof.

[0271] Those having ordinary skill in the art will recognize that at least a portion of the devices and/or processes described herein can be integrated into an image processing system. Those having skill in the art will recognize that a typical image processing system generally includes one or more of a system unit housing, a video display device, memory such as volatile or non-volatile memory, processors such as microprocessors or digital signal processors, computational entities such as operating systems, drivers, applications programs, one or more interaction devices (e.g., a touch pad, a touch screen, an antenna, etc.), control systems including feedback loops and control motors (e.g., feedback for sensing lens position and/or velocity; control motors for moving/distorting lenses to give desired focuses). An image processing system may be implemented utilizing suitable commercially available components, such as those typically found in digital still systems and/or digital motion systems.

[0272] Those having ordinary skill in the art will recognize that at least a portion of the devices and/or processes described herein can be integrated into a data processing system. Those having skill in the art will recognize that a data processing system generally includes one or more of a system unit housing, a video display device, memory such as volatile or non-volatile memory, processors such as microprocessors or digital signal processors, computational entities such as operating systems, drivers, graphical user interfaces, and applications programs, one or more interaction devices (e.g., a touch pad, a touch screen, an antenna, etc.), and/or control systems including feedback loops and control motors (e.g., feedback for sensing position and/or velocity; control motors for moving and/or adjusting components and/or quantities). A data processing system may be implemented utilizing suitable commercially available components, such as those typically found in data computing/communication and/or network computing/communication systems. Those having ordinary skill in the art will recognize that at least a portion of the devices and/or processes described herein can be integrated into a mote system. Those having skill in the art will recognize that a typical mote system generally includes one or more memories such as volatile or non-volatile memories, processors such as microprocessors or digital signal processors, computational entities such as operating systems, user interfaces, drivers, sensors, actuators, applications programs, one or more interaction devices (e.g., an antenna USB ports, acoustic ports, etc.), control systems including feedback loops and control motors (e.g., feedback for sensing or estimating position and/or velocity; control motors for moving and/or adjusting components and/or quantities). A mote system may be implemented utilizing suitable components, such as those found in mote computing/communication systems. Specific examples of such components entail such as Intel Corporation's and/or Crossbow Corporation's mote components and supporting hardware, software, and/or firmware.

[0273] Those having ordinary skill in the art will recognize that it is common within the art to implement devices and/or processes and/or systems, and thereafter use engineering and/or other practices to integrate such implemented devices and/or processes and/or systems into more comprehensive devices and/or processes and/or systems. That is, at least a portion of the devices and/or processes and/or systems described herein can be integrated into other devices and/or processes and/or systems via a reasonable amount of experimentation. Those having skill in the art will recognize that examples of such other devices and/or processes and/or systems might include—as appropriate to context and application—all or part of devices and/or processes and/or systems of (a) an air conveyance (e.g., an airplane, rocket, helicopter, etc.), (b) a ground conveyance (e.g., a car, truck, locomotive, tank, armored personnel carrier, etc.), (c) a building (e.g., a home, warehouse, office, etc.), (d) an appliance (e.g., a refrigerator, a washing machine, a dryer, etc.), (e) a communications system (e.g., a networked system, a telephone system, a Voice over IP system, etc.), (f) a business entity (e.g., an Internet Service Provider (ISP) entity such as Comcast Cable, Qwest, Southwestern Bell, etc.), or (g) a wired/wireless services entity (e.g., Sprint, Cingular, Nextel, etc.), etc.

[0274] In certain cases, use of a system or method may occur in a territory even if components are located outside the territory. For example, in a distributed computing context, use of a distributed computing system may occur in a territory even though parts of the system may be located outside of the territory (e.g., relay, server, processor, signal-bearing medium, transmitting computer, receiving computer, etc. located outside the territory). A sale of a system or method may likewise occur in a territory even if components of the system or method are located and/or used outside the terri-

tory. Further, implementation of at least part of a system for performing a method in one territory does not preclude use of the system in another territory.

[0275] One of ordinary skill in the art will recognize that the herein described components (e.g., operations), devices, objects, and the discussion accompanying them are used as examples for the sake of conceptual clarity and that various configuration modifications are contemplated. Consequently, as used herein, the specific exemplars set forth and the accompanying discussion are intended to be representative of their more general classes. In general, use of any specific exemplar is intended to be representative of its class, and the non-inclusion of specific components (e.g., operations), devices, and objects should not be taken limiting.

[0276] Those having ordinary skill in the art will appreciate that a user may be representative of a human user, a robotic user (e.g., computational entity), and/or substantially any combination thereof (e.g., a user may be assisted by one or more robotic agents) unless context dictates otherwise.

[0277] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations are not expressly set forth herein for sake of clarity. The herein described subject matter sometimes illustrates different components contained within, or connected with, different other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures may be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected", or "operably coupled", to each other to achieve the desired functionality, and any two components capable of being so associated can also be viewed as being "operably couplable", to each other to achieve the desired functionality. Specific examples of operably couplable include but are not limited to physically mateable and/or physically interacting components, and/or wirelessly interactable, and/or wirelessly interacting components, and/or logically interacting, and/or logically interactable components.

[0278] In some instances, one or more components may be referred to herein as "configured to," "configurable to," "operable/operative to," "adapted/adaptable," "able to," "conformable/conformed to," etc. Those having ordinary skill in the art will recognize that "configured to" can generally encompass active-state components and/or inactive-state components and/or standby-state components, unless context requires otherwise. While particular aspects of the present subject matter described herein have been shown and described, it will be apparent to those having ordinary skill in the art that, based upon the teachings herein, changes and modifications may be made without departing from the subject matter described herein and its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of the subject matter described herein. It will be understood by those within the art that, in general, terms used herein, and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes but is not limited to," etc.). It will be further understood by those within the art that if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to claims containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should typically be interpreted to mean "at least one" or "one or more"); the same holds true for the use of definite articles used to introduce claim recitations. In addition, even if a specific number of an introduced claim recitation is explicitly recited, those having ordinary skill in the art will recognize that such recitation should typically be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, typically means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, and C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). In those instances where a convention analogous to "at least one of A, B, or C, etc." is used, in general such a construction is intended in the sense one having skill in the art would understand the convention (e.g., "a system having at least one of A, B, or C" would include but not be limited to systems that have A alone, B alone, C alone, A and B together, A and C together, B and C together, and/or A, B, and C together, etc.). It will be further understood by those within the art that typically a disjunctive word and/or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" will be typically understood to include the possibilities of "A" or "B" or "A and B."

[0279] With respect to the appended claims, those having ordinary skill in the art will appreciate that recited operations therein may generally be performed in any order. Also, although various operational flows are presented in a sequence(s), it should be understood that the various operations may be performed in other orders than those which are illustrated, or may be performed concurrently. Examples of such alternate orderings may include overlapping, interleaved, interrupted, reordered, incremental, preparatory, supplemental, simultaneous, reverse, or other variant orderings, unless context dictates otherwise. Furthermore, terms like "responsive to," "related to," or other past-tense adjec-

tives are generally not intended to exclude such variants, unless context dictates otherwise.

1. A memory device comprising:

a substrate;

a non-volatile memory array integrated on the substrate; and

processing logic integrated with the non-volatile memory array on the substrate, the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array.

2. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is configured with functionality selectively distributed across the non-volatile memory array.

3. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes embedded central processing unit logic closely associated in function and location with a memory portion of the non-volatile memory array.

4. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes a plurality of embedded processing blocks respectively closely associated in function and location with a plurality of memory portions of the non-volatile memory array.

5. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes a plurality of embedded processing blocks operable to execute parallel processing tasks associated with the non-volatile memory array.

6. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes a plurality of embedded processing blocks operable to execute parallel processing tasks for multi-core functionality in absence of external central processing unit multi-core calls.

7. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes string processing logic operable to perform at least one string processing function associated with the non-volatile memory array.

8. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes anti-virus scanning logic operable to perform at least one anti-virus scanning function associated with the non-volatile memory array.

9. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes data compression logic operable to perform at least one data compression function associated with the non-volatile memory array.

10. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes sorting logic operable to perform at least one sorting function associated with the non-volatile memory array.

11. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes peripheral logic operable to manage the non-volatile memory array in response to external central processing unit calls.

12. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes extension logic operable to manage the non-volatile memory array in response to external central processing unit calls.

13. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes dormant processing logic operable upon activation by a signal from a device external to The memory device to perform at least one processing function associated with the non-volatile memory array.

14. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes process identification logic operable to identify and allocate parallel processing tasks associated with the non-volatile memory array.

15. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes process identification logic operable to identify and allocate a plurality of parallel processing tasks for multi-core functionality in absence of external central processing unit multi-core calls.

16. The memory device according to claim **1** further comprising:

a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes protection key logic operable to manage access to a selected memory portion of the non-volatile memory array based on information in the protection key register.

17. The memory device according to claim **1** further comprising:

a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes protection

key logic operable to operable to receive information and write the received information to the protection key register.

18. The memory device according to claim **1** further comprising:

a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes protection key logic operable to allocate parallel processing tasks for multi-core functionality based on information in the protection key register.

19. The memory device according to claim **1** further comprising:

a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes protection key logic operable to read data from a selected memory portion of the non-volatile memory array only if authorized by information in the protection key register.

20. The memory device according to claim **1** further comprising:

a protection key register integrated with the processing logic and the non-volatile memory array on the substrate, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes protection key logic operable to write data to a selected memory portion of the non-volatile memory array only if authorized by information in the protection key register.

21. The memory device according to claim **1** wherein:

the non-volatile memory array further includes a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types; and

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to perform at least one general purpose processing function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

22. The memory device according to claim **1** wherein:

the non-volatile memory array further includes a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types; and

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes string processing logic operable to perform at least one string processing function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

23. The memory device according to claim **1** wherein:

the non-volatile memory array further includes a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types; and

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes anti-virus scanning logic operable to perform at least one anti-virus scanning function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

24. The memory device according to claim **1** wherein:

the non-volatile memory array further includes a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types; and

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes data compression logic operable to perform at least one data compression function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

25. The memory device according to claim **1** wherein:

the non-volatile memory array further includes a plurality of non-volatile memory segments characterized by a respective plurality of non-volatile memory types; and

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes sorting logic operable to perform at least one sorting function for the non-volatile memory segments selectively based on ones of the plurality of non-volatile memory types.

26. The memory device according to claim **1** further comprising:

at least one sensor operable to detect at least one operating condition, wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to perform at least one general purpose processing function for the non-volatile memory array selectively based on the at least one operating condition.

27. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to access a time signal and perform at least one general purpose processing function for the non-volatile memory array based on the time signal.

28. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to monitor phenomena detectable at the memory device and perform at least one general purpose processing function for the non-volatile memory array based on the monitored phenomena.

29. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to accumulate and communicate information about phenomena associated with at least one entity in association with the memory device and perform at least one general purpose processing function for the non-volatile memory array based on the monitored phenomena.

30. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes encryption logic operable to perform at least one encryption/de-

cryption function associated with the non-volatile memory array and operable to read data from a selected portion of the non-volatile memory array only if authorized by results of the encryption/decryption function.

31. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array further includes encryption logic operable to perform at least one encryption/decryption function associated with the non-volatile memory array that holds at least one encryption key secure from a device external to the memory device and operable to read data from a selected portion of the non-volatile memory array only if enabled by the encryption key.

32. The memory device according to claim **1** further comprising:

a bus integrated with the processing logic and the non-volatile memory array on the substrate, the bus operable to communicate access requests and information between the memory device and a device external to the memory device.

33. The memory device according to claim **1** wherein:

the processing logic operable to perform at least one general purpose processing function associated with the non-volatile memory array is operable to perform the at least one general purpose processing function independently of signals external to the memory device.

34.-**36**. (canceled)

37. A method of manufacturing a memory device comprising:

forming a non-volatile memory array on a substrate; and

integrating processing logic in combination with the non-volatile memory array on the substrate that is operable to perform at least one general purpose processing function associated with the non-volatile memory array.

38.-**59**. (canceled)

60. A method of operating a memory device comprising:

providing the memory device including processing logic integrated in combination with non-volatile memory array on a substrate; and

operating the processing logic including:

performing at least one general purpose processing function associated with the non-volatile memory array.

61.-**91**. (canceled)

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