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(54) **CLOCK DISTRIBUTION NETWORK FOR 3D INTEGRATED CIRCUIT**

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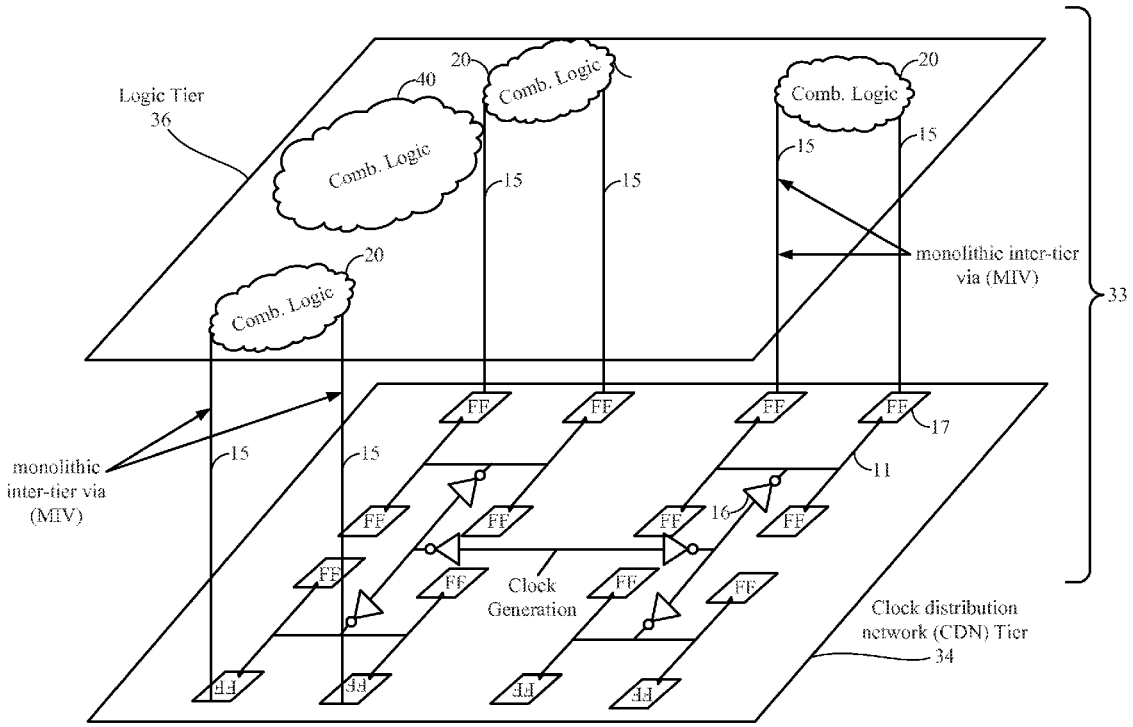
(52) **U.S. Cl.**
CPC ***G06F 17/5072*** (2013.01); ***H01L 23/5226*** (2013.01)
USPC **257/774**; 716/120

(57) **ABSTRACT**

Exemplary embodiments of the invention are directed to systems and method for designing a clock distribution network for an integrated circuit. The embodiments identify critical sources of clock skew, tightly control the timing of the clock and build that timing into the overall clock distribution network and integrated circuit design. The disclosed embodiments separate the clock distribution network (CDN), i.e., clock generation circuitry, wiring, buffering and registers, from the rest of the logic to improve the clock tree design and reduce the area footprint. In one embodiment, the CDN is separated to a separate tier of a 3D integrated circuit, and the CDN is connected to the logic tier(s) via high-density inter-tier vias. The embodiments are particularly advantageous for implementation with monolithic 3D integrated circuits.



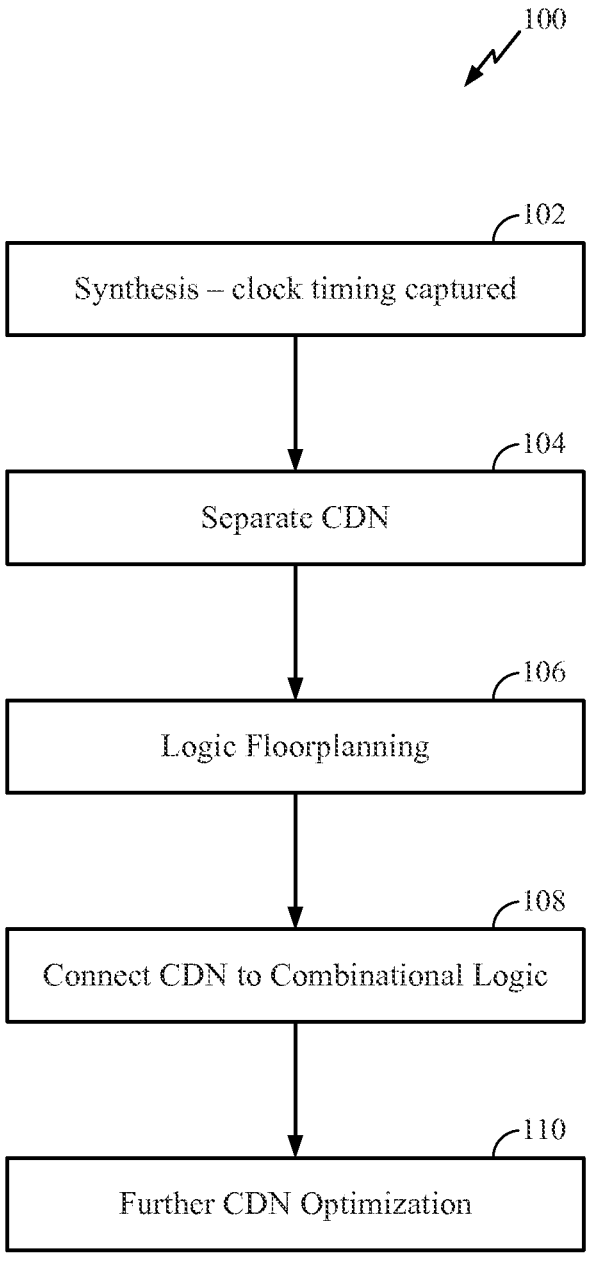

100
102
Synthesis – clock timing captured
104
Separate CDN
106
Logic Floorplanning
108
Connect CDN to Combinational Logic
110
Further CDN Optimization

FIG. 1

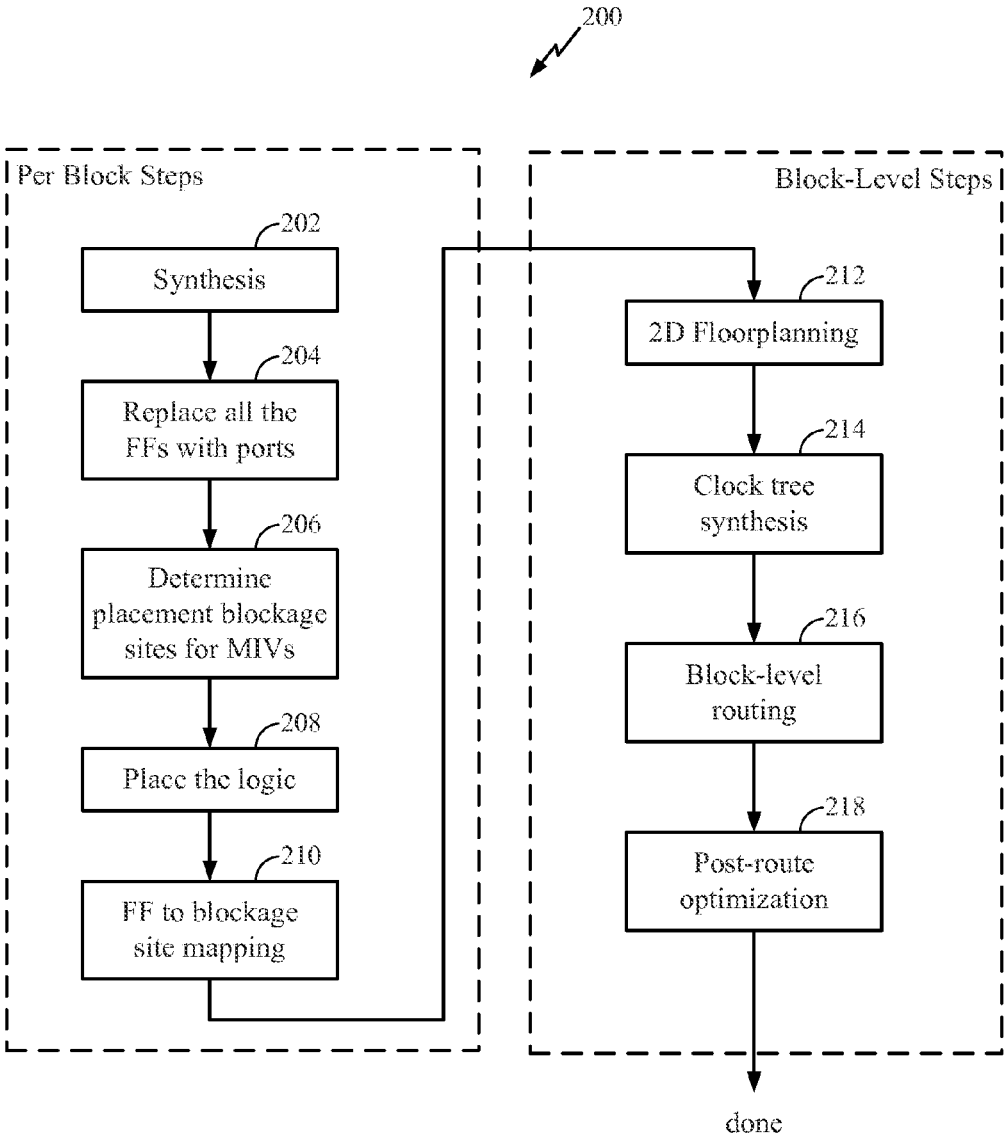

200
Per Block Steps
202
Synthesis
204
Replace all the FFs with ports
206
Determine placement blockage sites for MIVs
208
Place the logic
210
FF to blockage site mapping
Block-Level Steps
212
2D Floorplanning
214
Clock tree synthesis
216
Block-level routing
218
Post-route optimization
done

FIG. 2

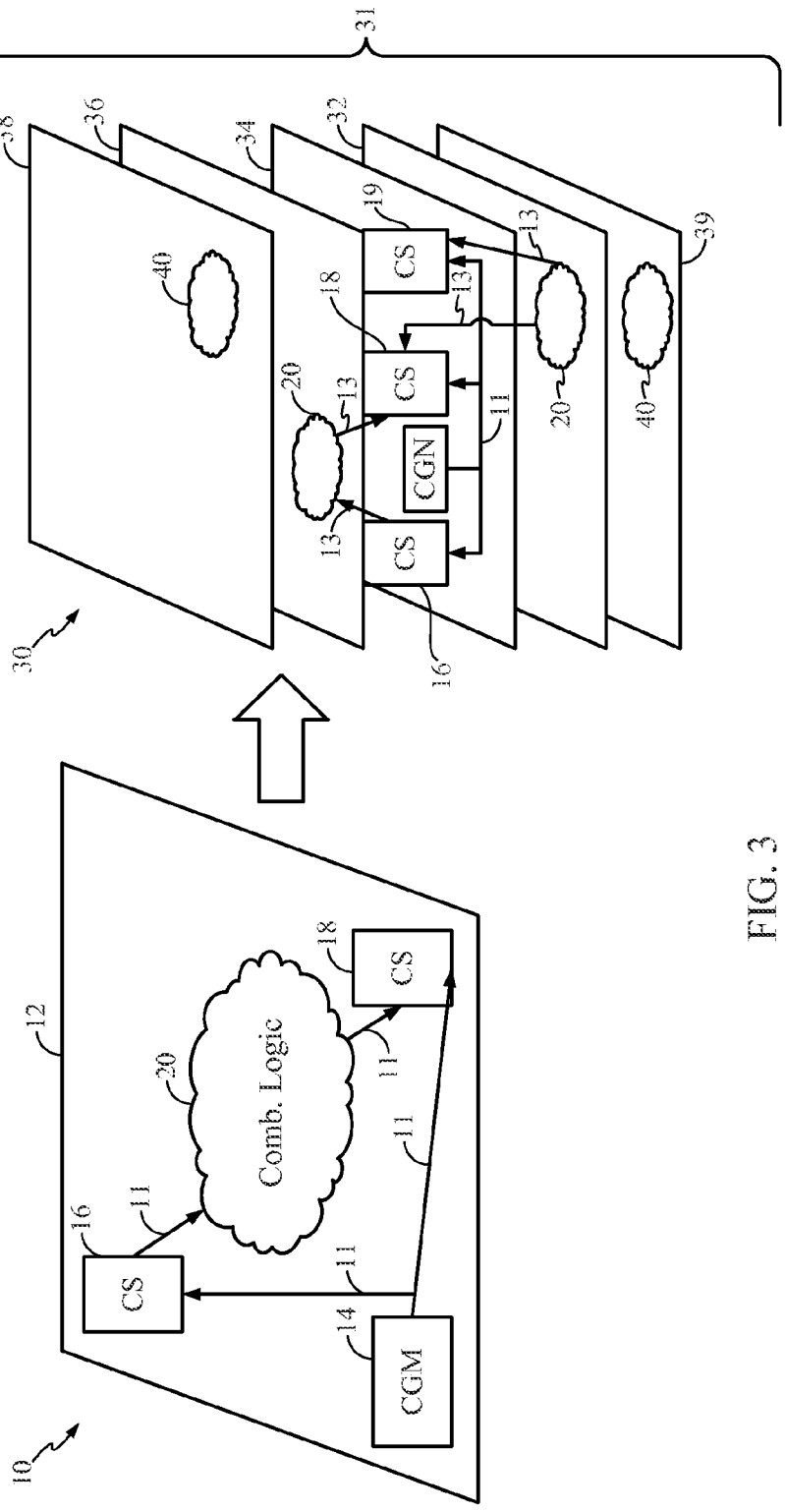

31
38
36
34
32
39
40
19
CS
13
18
CS
20
13
CS
11
CGN
13
CS
16
30
10
12
Comb. Logic
20
18
CS
11
11
16
CS
11
14
CGM

FIG. 3

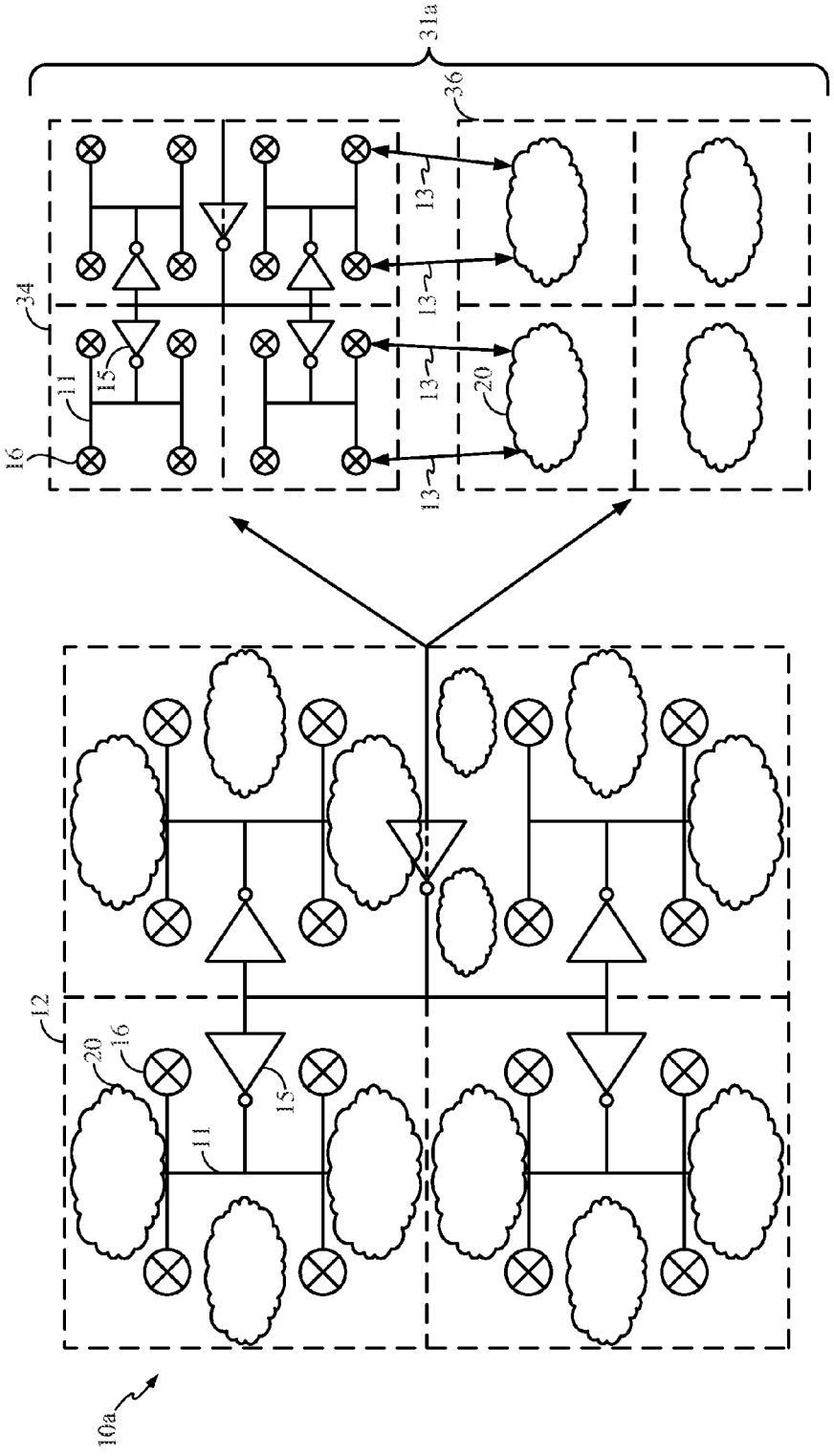


FIG. 4

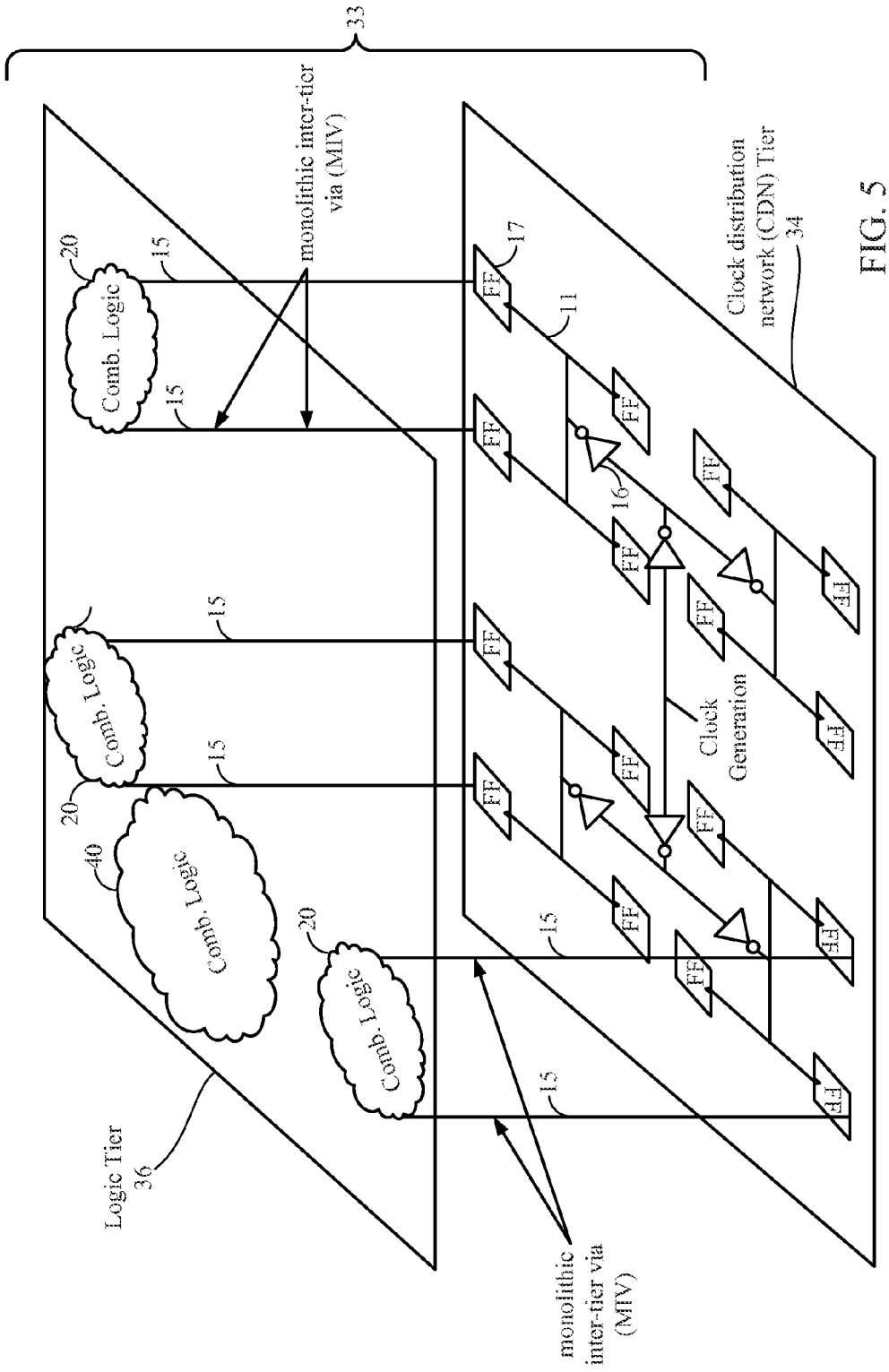

33
monolithic inter-tier via (MIV)
Clock distribution network (CDN) Tier
34
Comb. Logic
20
15
17
11
16
FF
Clock Generation
40
Logic Tier
36
monolithic inter-tier via (MIV)

FIG. 5

CLOCK DISTRIBUTION NETWORK FOR 3D INTEGRATED CIRCUIT

[0001] Claim of Priority under 35 U.S.C. §119

[0002] The present Application for Patent claims priority to the following:

[0003] Provisional Application No. 61/730,755 entitled "CLOCK DISTRIBUTION NETWORK FOR 3D INTEGRATED CIRCUIT," filed Nov. 28, 2012, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

[0004] Provisional Application No. 61/730,767 entitled "DATA TRANSFER ACROSS POWER DOMAINS," filed Nov. 28, 2012, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

REFERENCE TO CO-PENDING APPLICATIONS FOR PATENT

[0005] The present Application for Patent is related to the following co-pending U.S. Patent Application(s):

[0006] "MONOLITHIC 3D IC FLIP-FLOP DESIGN" by Yang Du, Jing Xie and Kambiz Samadi, having Attorney Docket No. 123412, filed Mar. 5, 2013, assigned to the assignee hereof, and expressly incorporated by reference herein;

[0007] "MONOLITHIC THREE DIMENSIONAL INTEGRATION OF SEMICONDUCTOR INTEGRATED CIRCUITS"' by Yang Du, having Attorney Docket No. 120600, filed Mar. 7, 2013, assigned to the assignee hereof, and expressly incorporated by reference herein; and

[0008] "DATA TRANSFER ACROSS POWER DOMAINS" by Jing Xie and Yang Du, having Attorney Docket No. 124716, filed [_____], assigned to the assignee hereof, and expressly incorporated by reference herein.

FIELD OF DISCLOSURE

[0009] The disclosed embodiments are directed in general to the generation of clock signals in integrated circuits. More specifically, the disclosed embodiments are directed to efficient systems and methods for developing a scalable clock distribution network having high-speed, low skew and low power consumption.

BACKGROUND

[0010] In a synchronous integrated circuit (IC), clock signals are used to define a time reference for the movement of data within the circuit. The IC's clock distribution network (e.g., clock generation circuitry, wiring, buffering and registers) generates clock signals and distributes them from a particular point to all of the circuit elements that need them. The performance of a synchronous IC heavily depends on its clock distribution network design. The proper design of the clock distribution network helps ensure that critical timing requirements are satisfied and that clock skew is controlled. As IC's become larger, their clock distribution networks start to take up large portions of the design resources. Clock signals typically have the greatest fan-out and have to operate at the highest speeds of any control or data signal within the entire design. Clock power is typically more than one-third of total power consumption of a typical IC and is due to (i) clock tree wiring, (ii) clock tree buffers and (iii) clock tree sinks (e.g., flip-flops). Therefore, developing a scalable, high-speed, high-performance and low-power clock distribution network design is extremely difficult given the existing skew/slew constraints in large IC's.

[0011] 3D IC's is an emerging technology that can provide higher-performance/lower-power designs. However, known 3D IC implementations tend to exacerbate clock distribution network design challenges because the clock signal has to reliably span across multiple tiers under tight skew/slew constraints. Hence, different tiers will have their own clock tree network. It is also impossible to meet skew/slew constraints across different clock networks spanning different tiers without degrading performance and power. To cope with this problem, asynchronous operation at the chip level is required, which then has its own disadvantages in various parameters including power consumption, speed and area footprint

[0012] Accordingly, there is a need for systems and methods for developing clock distribution networks that are scalable, low--skew, high-speed and high-performance. There is a further need for systems and methods for developing clock distribution networks that are scalable, low-skew, high-speed and high-performance, within a 3D IC.

SUMMARY

[0013] Exemplary embodiments of the invention are directed to systems and method for designing a clock distribution network for an integrated circuit. The embodiments identify critical sources of clock skew, tightly control the timing of the clock and build that timing into the overall clock distribution network and integrated circuit design. The disclosed embodiments separate the clock distribution network (CDN), i.e., clock generation circuitry, wiring, buffering and registers, from the rest of the logic to improve the clock tree design and reduce the area footprint. In one embodiment, the CDN is separated to a separate tier of a 3D integrated circuit, and the CDN is connected to the logic tier(s) via high-density inter-tier vias. The embodiments are particularly advantageous for implementation with monolithic 3D integrated circuits,

[0014] The disclosed embodiments include a method of developing a clock distribution network for an integrated circuit, the steps comprising: capturing sources of clock skew including timing mismatches between clock sinks; synthesizing a higher level behavioral description of the integrated circuit and said sources of clock skew to generate a 2D layout comprising a clock distribution network and combinational logic; separating said clock distribution network from said combinational logic and locating said clock distribution network to a first area of the integrated circuit; and floorplanning said combinational logic of said first area. In a further embodiment, the integrated circuit comprises a multi-tier circuit; said first area comprises a first tier of said multi-tier circuit; and said combinational logic is located to a second tier of said multi-tier circuit.

[0015] The disclosed embodiments also include a clock distribution network of an integrated circuit comprising: the clock distribution network separated to a first area of said integrated circuit; combinational logic of said integrated circuit separated to a. second area of said integrated circuits; and vias connecting said first area to said second area. In a further embodiment, the integrated circuit further comprises: the integrated circuit comprising a multi-tier circuit; said first area comprises a first tier of said multi-tier circuit; and said second area comprises a second tier of said multi-tier circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings are presented to aid in the description of disclosed embodiments and are provided solely for illustration of the embodiments and not limitation thereof.

[0017] FIG. **1** is a high level flow diagram illustrating a methodology of the disclosed embodiments;

[0018] FIG. **2** is a more detailed example of the flow diagram of FIG. **1**;

[0019] FIG. **3** is an example of a 2D timing arc and a 3D timing arc of the disclosed embodiments;

[0020] FIG. **4** is a more detailed example of the clock distribution network of FIGS. **3**; and

[0021] FIG. **5** is another more detailed example of the clock distribution network of FIG. **4**.

DETAILED DESCRIPTION

[0022] Aspects of the invention are disclosed in the following description and related drawings directed to specific embodiments of the invention. Alternate embodiments may be devised without departing from the scope of the invention. Additionally, well-known elements of the invention will not be described in detail or will be omitted so as not to obscure the relevant details of the invention.

[0023] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments. Likewise, the terms "embodiments of the invention" does not require that all embodiments of the invention include the discussed feature, advantage or mode of operation.

[0024] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of embodiments of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises", "comprising,", "includes" and/or "including", when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0025] Further, many embodiments are described in terms of sequences of actions to be performed by, for example, elements of a computing device. It will be recognized that various actions described herein can be performed by specific circuits (e.g., application specific integrated circuits (ASICs)), by program instructions being executed by one or more processors, or by a combination of both. Additionally, the sequence of actions described herein can be considered to be embodied entirely within any form of computer readable storage medium having stored therein a corresponding set of computer instructions that upon execution would cause an associated processor to perform the functionality described herein. Thus, the various aspects of the invention may be embodied in a number of different forms, all of which have been contemplated to be within the scope of the claimed subject matter. In addition, for each of the embodiments described herein, the corresponding form of any such embodiments may be described herein as, for example, "logic configured to" perform the described action.

[0026] FIG. **1** is a high-level block diagram illustrating a design technique **100** of the disclosed embodiments. Design technique **100** develops a clock distribution network (CDN) that tightly controls the timing of the clock and builds that timing into the overall design. The IC may include digital components, analog components, or a combination of both. Reference throughout this disclosure to "logic" circuitry is intended to cover digital circuit components, analog circuit components and combinations of both. Design technique **100** at step **102** performs a synthesis operation, which takes a higher level behavioral description and synthesizes it to complex logic circuits that perform the described operations. The higher level behavioral description may be implemented as a Register Transfer Level (RTL) description that can be mapped to a library of gates. An RTL description describes a circuit's registers and the sequence of transfers between the registers. The synthesis performed at step **102** captures the clock distribution network timing information.

[0027] Step **104** separates the CDN (which includes clock generation circuitry, wiring, buffering and registers) from the remaining combinational logic developed at step **102**. The separated CDN covers a smaller footprint due to separation of the CDN from the rest of the combinational logic. The smaller CDN results in smaller buffers, less wiring and reduced power. Separating the CDN reduces the complexity of the combinational logic for better routablility, reduced wire length, increased performance and a reduction in power consumption. Step **106** applies floorplanning techniques to the separated combinational logic. As described in more detail later in this disclosure, the floorplanning techniques may be 2D or 3D. At step **108**, vias are mapped out to connect the clock sinks of the separated CDN to the corresponding logic of the separated combinational logic. The vias are preferably of a type that can be fabricated at high density in layers on a single semiconductor wafer. Step **110** applies further optimization techniques to the separated and floorplanned CDN until the desired overall performance parameters have been reached.

[0028] FIG. **2** is a flow diagram of a design technique **200** that is a more detailed implementation of the design technique **100** shown in FIG. **1**. Design technique **200** may be advantageously applied to a 3D IC. Steps **202** to **210** are performed for the functional blocks and steps **212** to **218** are performed at the block level of the 3D IC. The synthesis operation performed at step **202** is essentially the same as the synthesis operation performed at step **102**. Step **204** moves the clock sinks to a separate CDN area and replaces the clock sinks of the synthesized circuit with ports to provide an indication of where the clock sinks were actually located inside each functional block, The separate CDN area under design technique **200** is preferably a separate tier of a 3D IC dedicated to the CDN (clock generation circuitry, wiring, buffering, registers, etc.). Step **206** determines the placement blockage sites for the via connections between the CDN tier and the combinational logic. The vias connect where the clock sinks were located in the synthesized circuit. Because the vias are high density, the number of vias for a particular clock sink can correspond to the number of outputs from the clock sink. For example, where the clock sink is a flip-flop and the via is an inter-tier via, k inter-tier vias may be assigned for the particular flip-flop, with k representing the number of connections to the flip-flop output. Step **206** preferably inserts the blockages in a mesh-like fashion to increase the accessibility of the clock sinks across the entire block. Step **208** places the com-

binational logic on the logic tier, and step **210** maps each of the clock sinks to its associated blockage site.

[0029] Steps **212** to **218** are performed at the block level of the 3D IC. Step **212** applies floorplanning techniques to the logic tier. Because the disclosed embodiments are scalable, increasingly larger IC's and CDN's are accommodated by adding more CDN tiers. Thus, the floorplanning techniques at step **212** may be 2D (single CDN tier) or 3D (multiple CDN tiers). Steps **214** to **218** apply further optimization techniques to the separated and floorplanned logic and CDN until the desired overall performance parameters have been reached. Step **214** applies clock tree synthesis to the floorplanned CDN tier. The clock tree synthesis includes clock buffer insertion and utilizes the information on the placement of the blockage sites from step **206**. Step **216** performs block-level routing, and step **218** performs post-route optimization. A conventional 2D post-route optimization engine may be used to accomplish step **218**.

[0030] Thus, the above-described design techniques provide a number of benefits. At least one tier of the multi-tier design is primarily dedicated to housing the CDN, so there is no need to design a clock tree for each tier, thereby reducing design complexity. Also there are fewer metal lavers under the design method of the disclosed embodiments, which saves cost compared with known 3D integrated circuit techniques. The smaller CDN footprint results in less clock power (e.g., approximately 30% power reduction), which results in less wiring and less buffering. The clock tree design that results from the methodology of the disclosed embodiments is cleaner because all the clock sinks and the CDN (which includes the clock buffers) reside on one tier. The separated CDN is significantly more robust against process variation (even more than 2D due to smaller footprint). Wirelength is reduced due to less logic complexity on the logic tier resulting in improved performance. The improved clock tree design results in improved timing closure. Design complexity is reduced because (i) existing 2D timing optimization engines can be used for embodiments where there are no 3D nets with respect to timing optimization, (ii) scan chain routing is simplified as there is no need to go through the logic tier. Where the existing sequential (non-memory) takes up approximately half the design area vs. combinational cells, there is easy balancing between tiers.

[0031] FIGS. **3-5** illustrate general configurations of circuit layouts that can result from implementing the design techniques shown in FIGS. **1** and **2**. FIG. **3** shows an example of a 2D timing arc **10** and a 3D timing arc **30**. FIGS. **3-5** are general configurations broadly representing certain types of circuitry/elements (e.g., clock generation, wiring, combinational logic, clock sinks) but are not intended to convey a particular circuit example. Timing arc **10** includes clock generation module (CGM) **14**, clock sinks (CS) **16**, **18**, wiring **11** and combinational logic **20**, all in 2D and dispersed throughout a single tier **12**. In practice, CGI **14** could be implemented as phase lock loop circuitry, and clock sinks **16**, **18** could be implemented as flip-flop circuitry. In general, the timing arcs **10**, **30** accurately capture the critical sources of clock skew, including for example design and/or delay mismatches from a so-called launch clock sink **16** to a so-called capture clock sink **18**. Thus, the clock timing requirements are tightly controlled and built into the overall IC design.

[0032] Timing arc **30** illustrates the CDN (CGM **14**, CS **16**, **18**, **19** and wiring **11**) separated to a single tier **34** of a multi-tier IC **31**. Combinational logic **20**, which is timing critical, is placed after the CDN is separated. To the extent the CDN does not occupy an entire tier, some or all of the timing-critical combinational logic **20** may be placed on the same CDN tier. Thus, the timing-critical combinational logic **20** may be placed on CDN tier **34** if there is room after placement of the CDN, or on either tier **32**, **36** that is adjacent CDN tier **34**. The non-timing-critical combinational logic **40** may also be placed on CDN tier **34** if there is room after placement of the CDN and any timing-critical combinational logic **20**, or on any other tier **32**, **36**, **38**, **39** whether or not that tier is adjacent to a CDN tier. High density vias **13** are built into the multi-tier circuit **31** and connect CS **16**, **18**, **19** to timing-critical combinational logic **20**.

[0033] Timing arc **30** further illustrates the scalability of the disclosed embodiments. The multi-tier circuit **31** is easily scalable for larger and larger IC's, as long as the CDN is separated to as many tiers as are needed to accommodate the size of the CDN. In the example shown in FIG. **3**, the CDN (**16**, **18**, **19**, **14**, **11**) is on a single tier **34** but may be expanded to more CDN tiers (not shown) if the CDN size increases. Similarly, as the size of timing-critical combinational logic **20** increases, additional tiers may be added to accommodate the larger timing-critical logic as long as the additional tiers are either a CDN tier or adjacent to a CDN tier. Finally, as the size of non-timing-critical combinational logic **40** increases, additional tiers may be added to accommodate the larger non-timing-critical combinational logic.

[0034] FIG. **4** is a further illustration of the general configuration of circuit layouts that can result from implementing the design techniques shown in FIGS. **1** and **2**. Similar to the timing arcs of FIG. **3**, FIG. **4** shows an example of a 2D layout having the CDN and the corresponding logic, along with a multi-tier implementation of the 2D layout. FIG. **4** is a general configuration broadly representing certain types of circuitry/elements (e.g., clock generation, wiring, combinational logic, clock sinks) but is not intended to convey a particular circuit example 2D layout **10***a* includes clock generation module (CGI) **15**, clock sinks (CS) **16**, wiring **11** and combinational logic **20**, all in 2D and dispersed throughout a single tier **12**. In practice, CGM **15** could be implemented as phase lock loop circuitry, and clock sinks **16** could be implemented as flip-flop circuitry, Wiring **11** is shown for simplicity in an H--tree format, but may be implemented in a variety of different clock tree formats (e.g., grid, spines, etc.). In general, 2D layout **10** accurately captures the critical sources of clock skew, including for example design and/or delay mismatches between clock sinks **16**. Thereby, the clock timing requirements are tightly controlled and built into the overall IC design.

[0035] FIG. **4** further illustrates the CDN (clock buffer **15**, CS **16** and wiring **11**) separated to a single tier **34** of a multi-tier IC **31***a*. Combinational logic **20**, which is timing critical, is placed after the CDN is separated. To the extent the CDN does not occupy an entire: tier, some or all of the timing-critical combinational logic **20** may be placed on the same CDN tier. Thus, the timing-critical combinational logic **20** may be placed on CDN tier **34** if there is room after placement of the CDN, or on any tier (e.g., tier **36**) adjacent to CDN tier **34**. The non-timing-critical combinational logic **40** (shown in FIG. **3**) may also be placed on CDN tier **34** if there is room after placement of the CDN and any timing-critical combinational logic **20**, or on any other tier **32**, **36**, **38** (shown in FIG. **3**) whether or not that tier is adjacent to a CDN tier.

High density vias **13** are built into the multi-tier circuit **31***a* and connect CS **16** to timing-critical combinational logic **20**.

[0036] FIG. **5** is a more detailed example of the multi-tier circuit **3** la shown in FIGS. **3** and **4**. The multi-tier circuit of FIG. **5** is shown as a monolithic 3D IC **33** having at least a CDN tier **34** and a logic tier **36**. The clocks sinks of FIG. **5** are implemented as flip-flop (FF) circuitry **17**. The high density vias **13** of FIGS. **3** and **4** are implemented and shown in FIG. **5** as monolithic inter-tier vias (WV) **15**. In monolithic 3D IC's, electronic components and their connections (wiring) are built in layers on a single semiconductor wafer, which is then diced into 3D ICs. There is only one substrate, hence no need for aligning or through-silicon vias.

[0037] Thus, the above-described embodiments separate the clock distribution network from the rest of the logic. Preferably, the clock distribution network is implemented using monolithic 3D integration technology. Thus, a single tier will host the clock subsystem and the other tier(s) will hold the remaining combinational logic. The clock tier under the present disclosure will include the clock generation circuitry (i.e., PLLs or DLLs), clock distribution wiring (H-tree, grid, spines, etc.) and a majority (e.g., 75%) of the sequential elements of the design. The clock tier will contain the widest metal lines for better clock distribution control. The clock distribution network includes a smaller footprint due to separation of the clock distribution from the rest of the logic. The smaller clock network results in smaller buffers, less wiring and reduced power. Separating the clock distribution reduces the complexity of the logic tier for better routablility, reduced wire length, increased performance and a reduction in power consumption. High density inter--tier vias provided by the monolithic 3D integration are used to connect the clock sinks on the clock tier to the corresponding logic on the logic tier.

[0038] While the foregoing disclosure and illustrations show embodiments of the invention, it should be noted that various changes and modifications could be made herein without departing from the scope of the invention as defined by the appended claims. For example, the functions, steps and/or actions of the method claims in accordance with the embodiments of the invention described herein need not be performed in any particular order. Furthermore, although elements of the invention may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

[0039] Those of skill in the relevant arts will also appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

[0040] The methods, sequences and/or algorithms described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. Accordingly, an embodiment of the invention can include a computer readable media embodying a method for performing the disclosed and claimed embodiment. Accordingly, the invention is not limited to illustrated examples and any means for performing the functionality described herein are included in embodiments of the invention.

What is claimed is:

1. A method of developing a clock distribution network for an integrated circuit, the steps comprising:
- capturing sources of clock skew including timing mismatches between clock sinks;
- synthesizing a higher level behavioral description of the integrated circuit and said sources of clock skew to generate a 2D layout comprising a clock distribution network and combinational logic;
- separating said clock distribution network from said combinational logic and locating said clock distribution network to a first area of the integrated circuit; and
- floorplanning said combinational logic of said first area.

2. The method of claim I further comprising the step of applying further optimization to said clock distribution network of said first area.

3. The method of claim **2** wherein said further optimization comprises clock tree synthesis,

4. The method of claim **3** wherein said further optimization comprises block-level routing.

5. The method of claim **4** wherein said further optimization comprises post-route optimization.

6. The method of claim **2** wherein:
- the integrated circuit comprises a multi-tier circuit;
- said first area comprises a first tier of said multi-tier circuit; and
- said combinational logic is located to a second tier of said multi-tier circuit.

7. The method of claim **6** wherein said first tier is adjacent said second tier.

8. The method of claim **6** wherein connections from said clock distribution network to said combinational logic comprise vias.

9. The method of claim **8** wherein said vias comprise inter-tier vias.

10. The method of claim **9** wherein said inter-tier vias comprise high-density.

11. The method of claim **6** wherein:
- said combinational logic further comprises non-timing critical combinational logic; and
- said non-timing critical combinational logic is located to a third tier of said multi-tier circuit.

12. The method of claim **11** wherein said third tier is not adjacent said first tier.

13. The method of claim **6** wherein:
- said timing-critical combinational logic is further located to a fourth tier of said multi-tier circuit; and
- said fourth tier is adjacent said first tier.

14. The method of claim **13** wherein:
- said combinational logic comprises critical combinational logic; and

said non-timing critical combinational logic is located to a fifth tier of said multi-tier circuit.

15. The method of claim **14** wherein said fifth tier is not adjacent said first tier.

16. A clock distribution network of an integrated circuit apparatus comprising:

the clock distribution network separated to a first area of said integrated circuit;

combinational logic of said integrated circuit separated to a second area of said integrated circuit; and

vias connecting said first area to said second area,

17. The apparatus of claim **16** wherein:

the integrated circuit comprises a multi-tier circuit;

said first area comprises a first tier of said multi-tier circuit; and

said second area comprises a second tier of said multi-tier circuit.

18. The apparatus of claim **17** wherein said first tier is adjacent said second tier.

19. The apparatus of claim **16** wherein said vias comprise inter-tier vias.

20. The apparatus of claim **9** wherein said inter-tier vias comprise high-density.

21. The apparatus of claim **17** wherein:

said integrated circuit further comprises non-timing critical combinational logic;

said non-timing critical combinational logic is separated to a third area of said integrated circuit; and

said third area comprises a third net of said multi-tier circuit.

22. The apparatus of claim **21** wherein said third tier is not adjacent said first tier.

23. The apparatus of claim **17** wherein:

said combinational logic is further located to a fourth tier of said multi-tier circuit; and

said fourth tier is adjacent said first tier.

24. The apparatus of claim **23** wherein:

said integrated circuit further comprises non-timing critical combinational logic; and

said non-timing critical combinational logic is located to a fifth tier of said multi-tier circuit.

25. The apparatus of claim **24** wherein said fifth tier is not adjacent said first tier.

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