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(54) **METHOD FOR FORMING MULTI-GATE SEMICONDUCTOR DEVICE**

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(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

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Related U.S. Application Data

(60) Division of application No. 16/681,097, filed on Nov. 12, 2019, now Pat. No. 11,183,560, which is a continuation of application No. 15/979,123, filed on May 14, 2018, now Pat. No. 10,522,622.

Publication Classification

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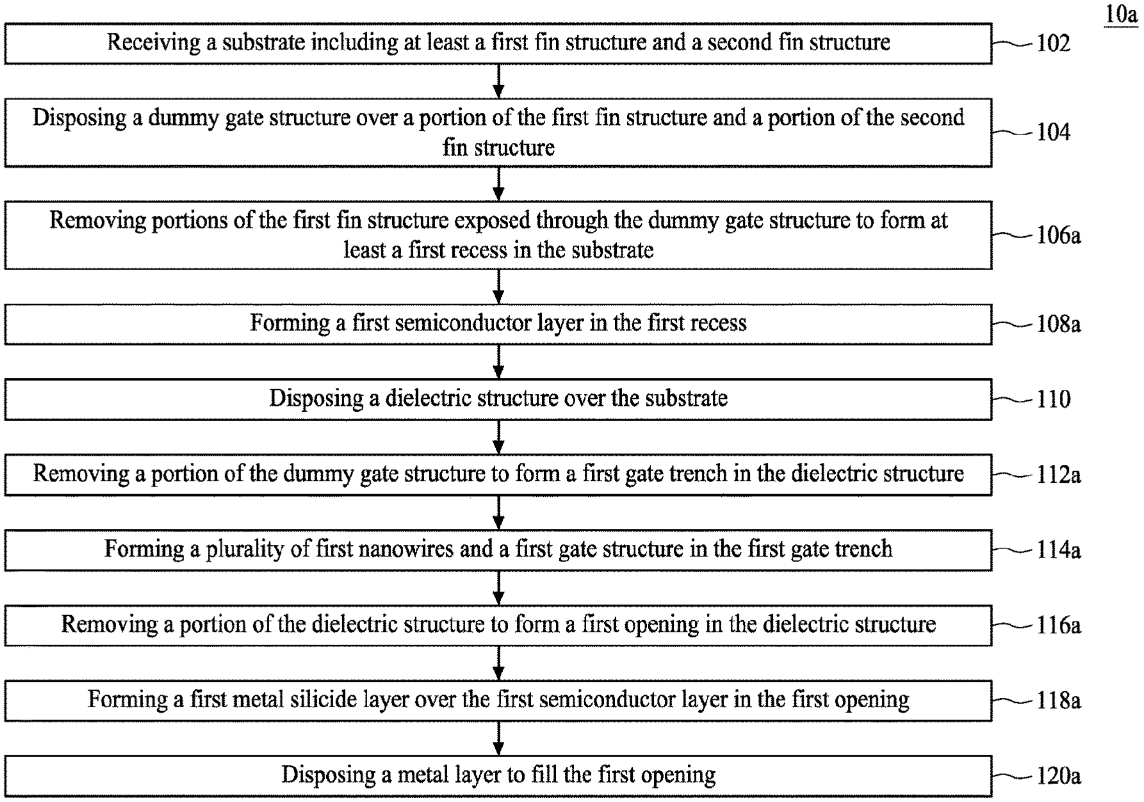
H01L 27/088	(2006.01)
H01L 27/092	(2006.01)
H01L 29/423	(2006.01)
H01L 21/8234	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/0673*** (2013.01); ***H01L 29/785*** (2013.01); ***H01L 29/66795*** (2013.01); ***H01L 21/02603*** (2013.01); ***H01L 21/823431*** (2013.01); ***H01L 21/823821*** (2013.01); ***H01L 27/0886*** (2013.01); ***H01L 27/0924*** (2013.01); ***H01L 29/42392*** (2013.01); ***H01L 29/66545*** (2013.01)

(57) **ABSTRACT**

Semiconductor structures and method for forming the same are provided. The semiconductor structure includes a substrate and first nanostructures and second nanostructures formed over the substrate. The semiconductor structure further includes a first source/drain structure formed adjacent to the first nanostructures and a second source/drain structure formed adjacent to the second nanostructures. The semiconductor structure further includes a first contact plug formed over the first source/drain structure and a second contact plug formed over the second source/drain structure. In addition, a bottom portion of the first contact plug is lower than a bottom portion of the first nanostructures, and a bottom portion of the second contact plug is higher than a top portion of the second nanostructures.



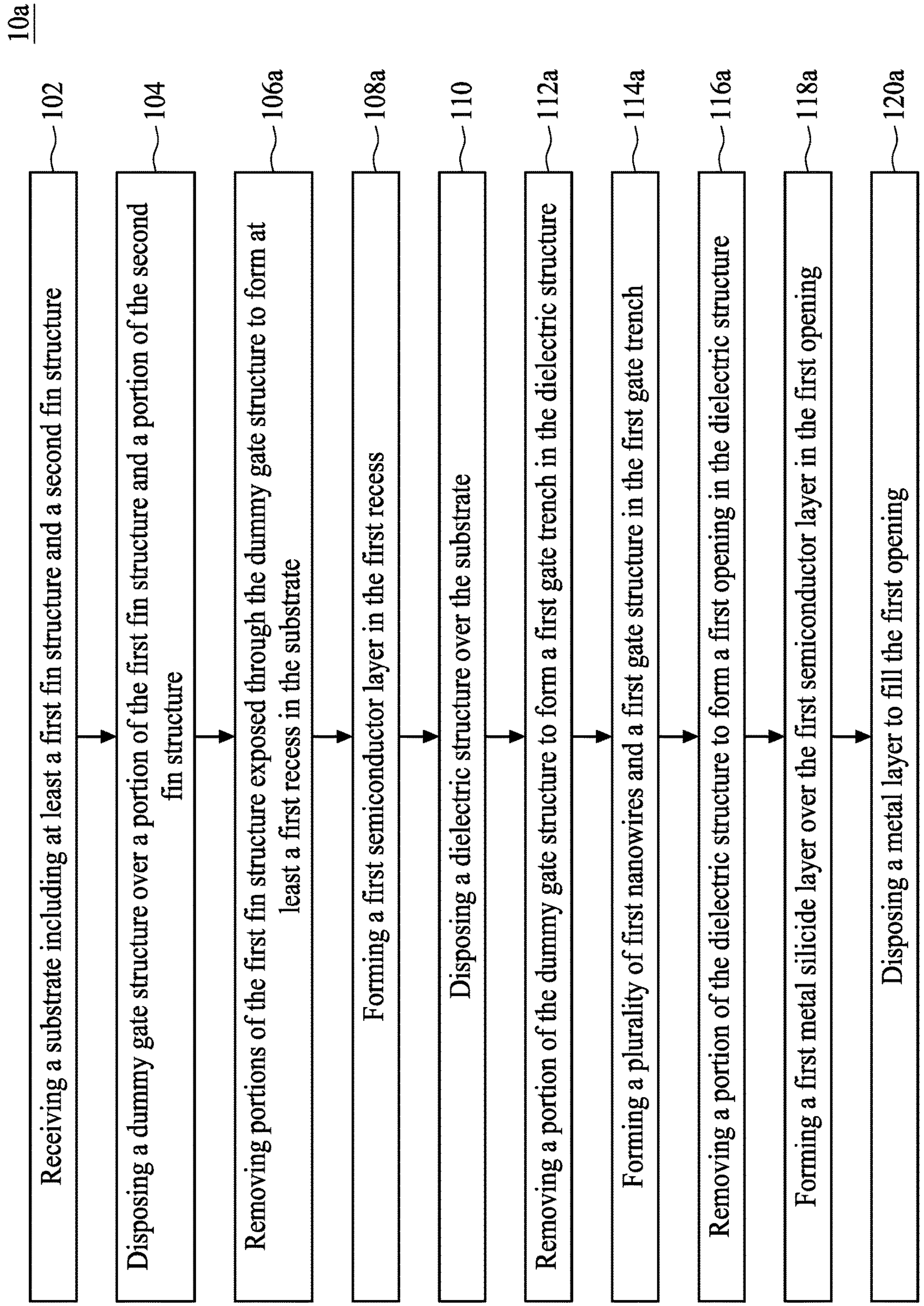

10a
102
Receiving a substrate including at least a first fin structure and a second fin structure
104
Disposing a dummy gate structure over a portion of the first fin structure and a portion of the second fin structure
106a
Removing portions of the first fin structure exposed through the dummy gate structure to form at least a first recess in the substrate
108a
Forming a first semiconductor layer in the first recess
110
Disposing a dielectric structure over the substrate
112a
Removing a portion of the dummy gate structure to form a first gate trench in the dielectric structure
114a
Forming a plurality of first nanowires and a first gate structure in the first gate trench
116a
Removing a portion of the dielectric structure to form a first opening in the dielectric structure
118a
Forming a first metal silicide layer over the first semiconductor layer in the first opening
120a
Disposing a metal layer to fill the first opening

FIG. 1

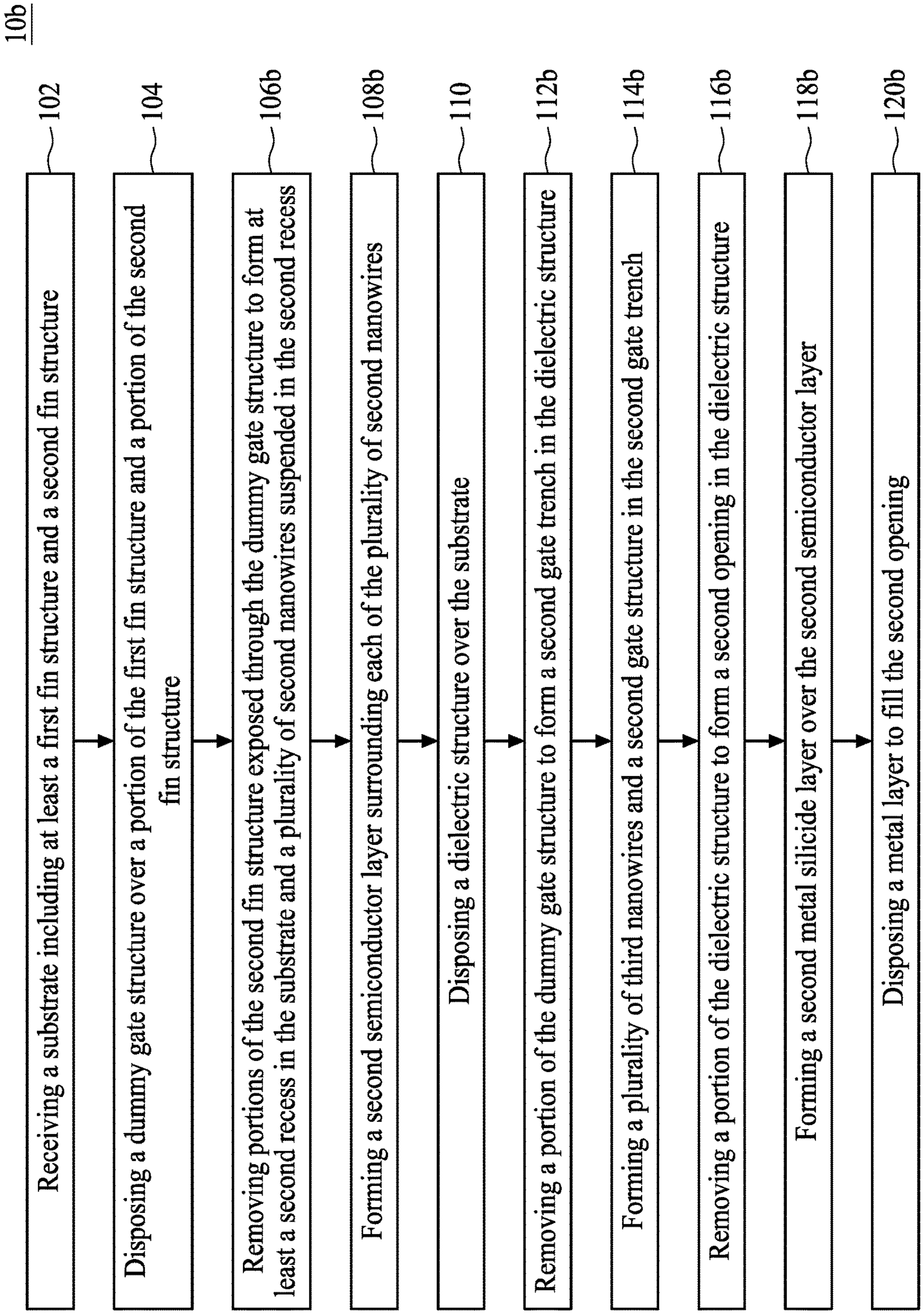

10b
102
Receiving a substrate including at least a first fin structure and a second fin structure
104
Disposing a dummy gate structure over a portion of the first fin structure and a portion of the second fin structure
106b
Removing portions of the second fin structure exposed through the dummy gate structure to form at least a second recess in the substrate and a plurality of second nanowires suspended in the second recess
108b
Forming a second semiconductor layer surrounding each of the plurality of second nanowires
110
Disposing a dielectric structure over the substrate
112b
Removing a portion of the dummy gate structure to form a second gate trench in the dielectric structure
114b
Forming a plurality of third nanowires and a second gate structure in the second gate trench
116b
Removing a portion of the dielectric structure to form a second opening in the dielectric structure
118b
Forming a second metal silicide layer over the second semiconductor layer
120b
Disposing a metal layer to fill the second opening

FIG. 2

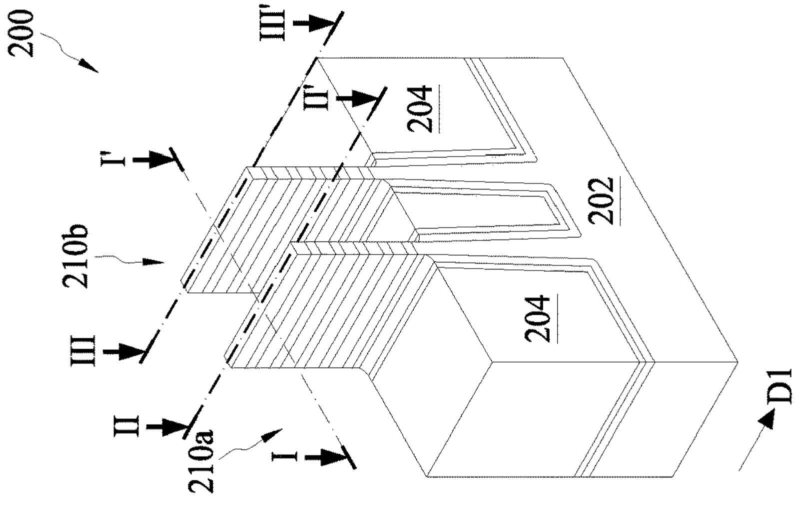


FIG. 3A

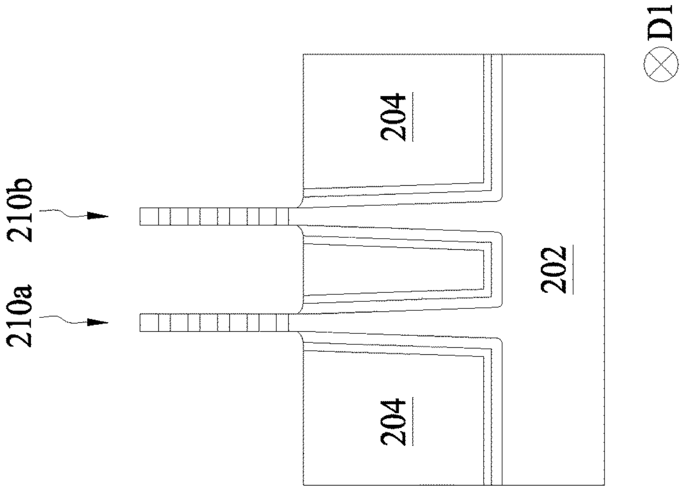


FIG. 3B

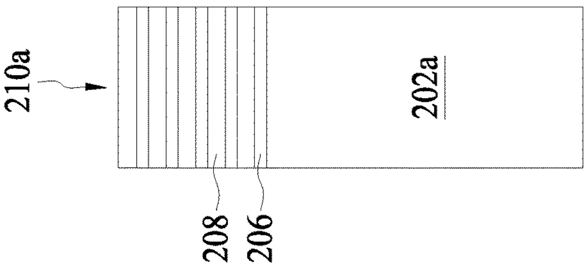


FIG. 3C

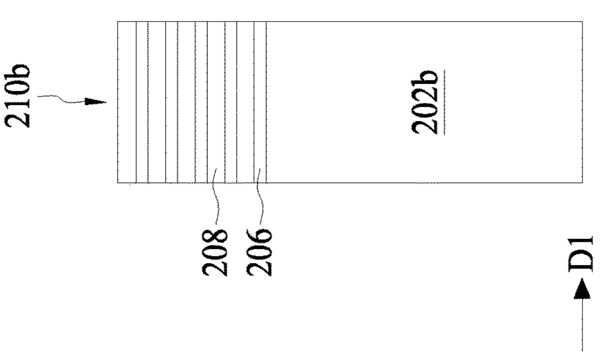


FIG. 3D

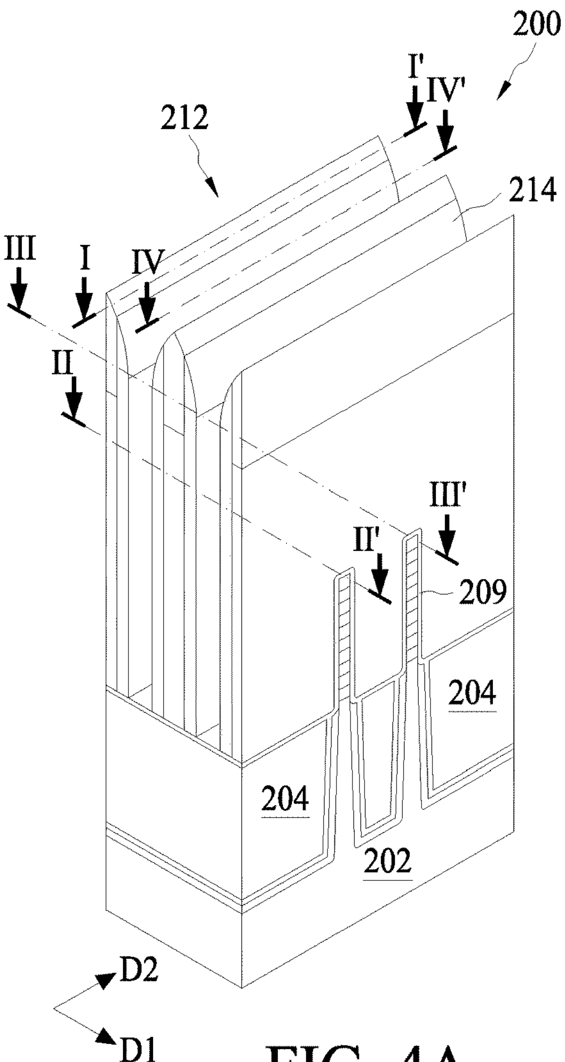


FIG. 4A

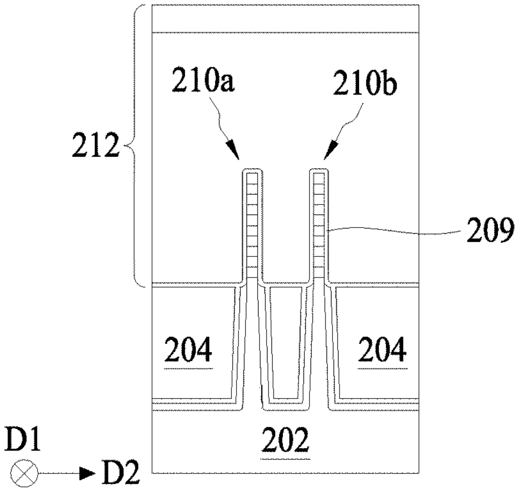


FIG. 4B

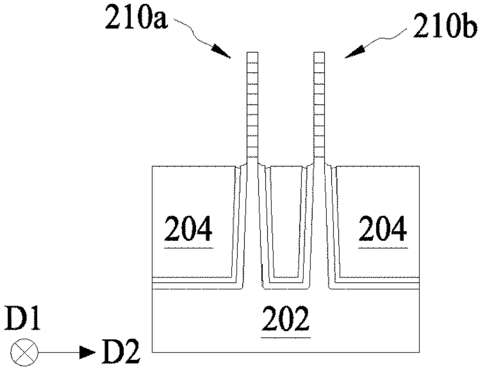


FIG. 4E

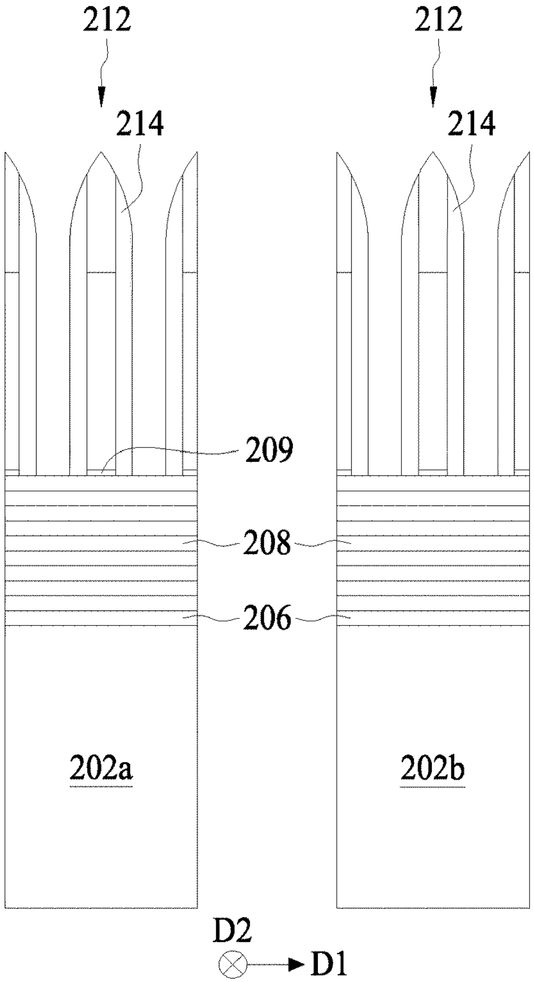


FIG. 4C FIG. 4D

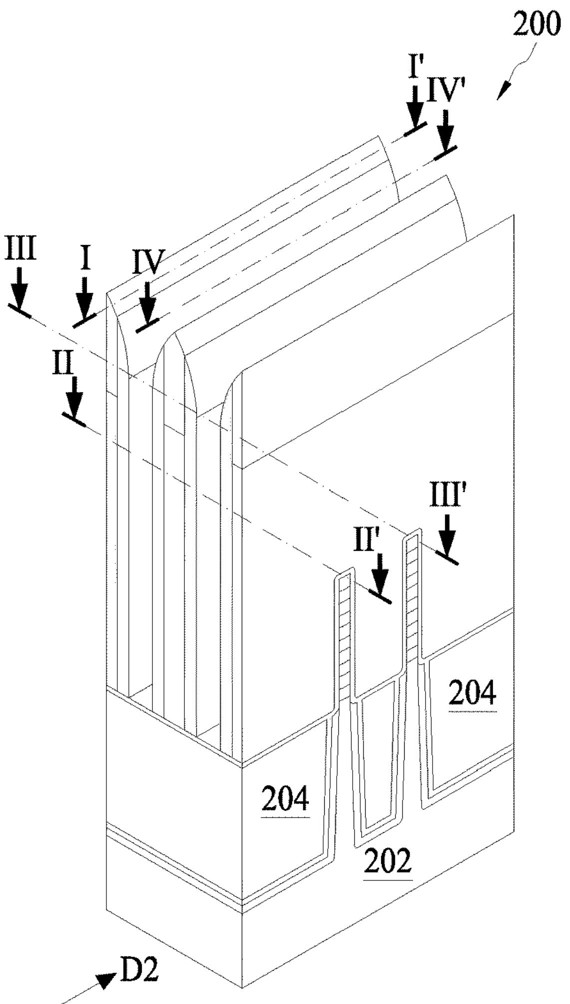


FIG. 5A

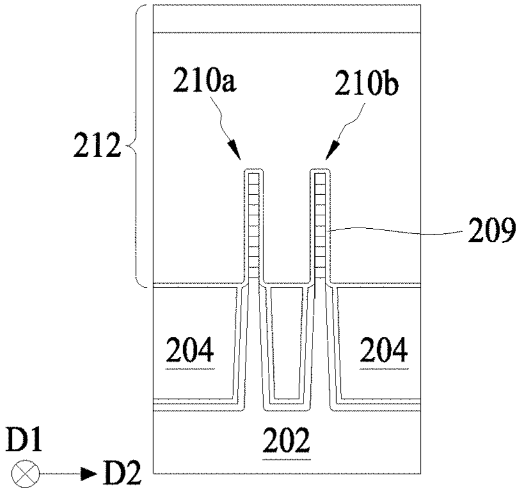


FIG. 5B

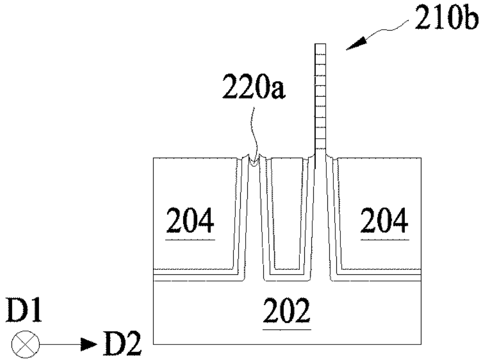


FIG. 5E

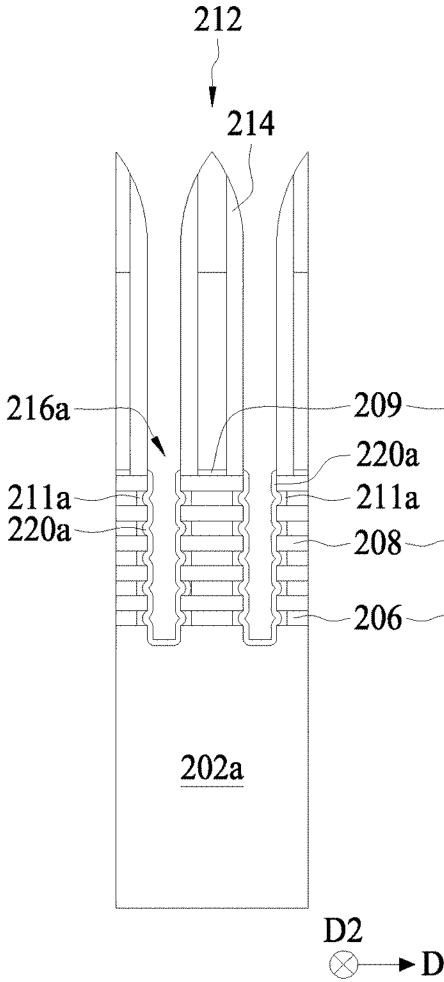


FIG. 5C

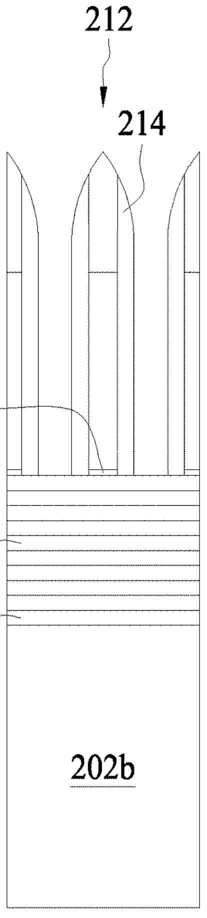
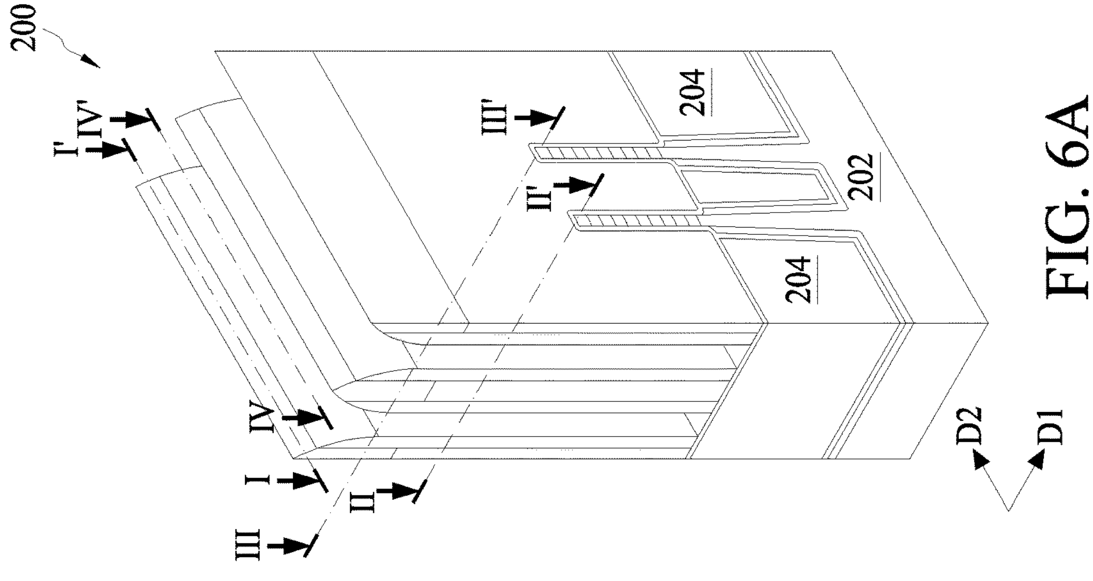


FIG. 5D



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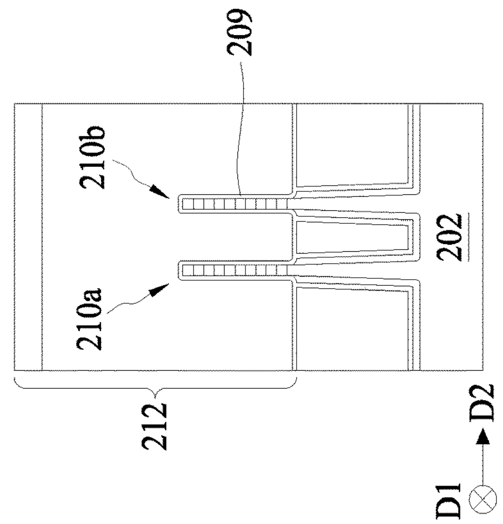


FIG. 6B

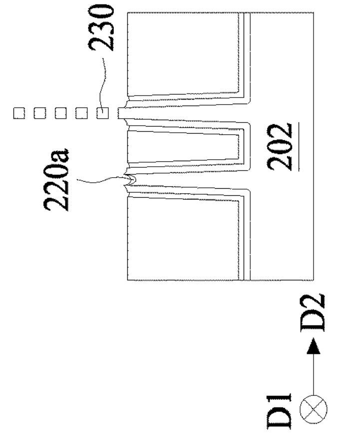


FIG. 6E

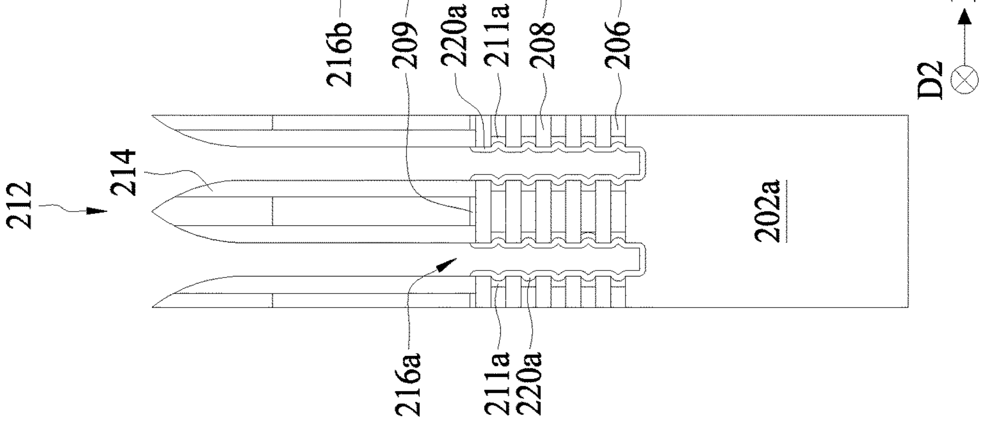


FIG. 6C

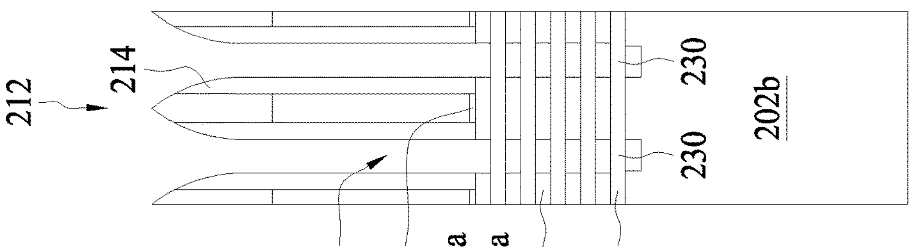


FIG. 6D

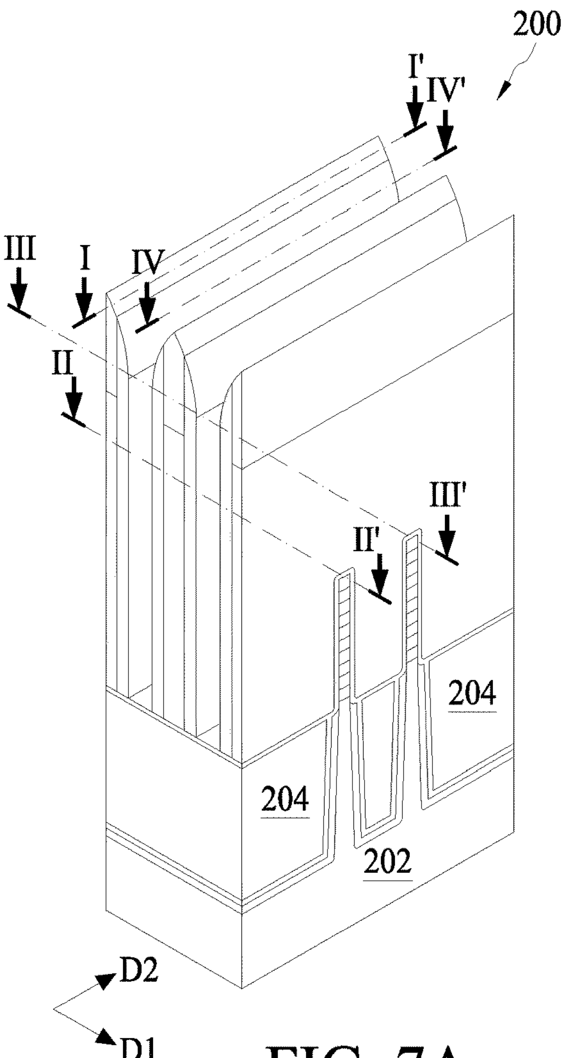


FIG. 7A

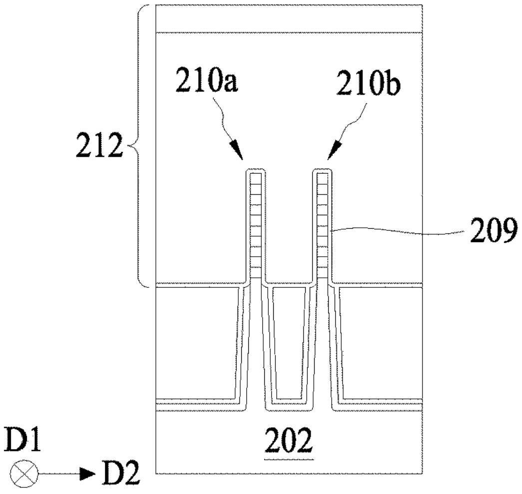
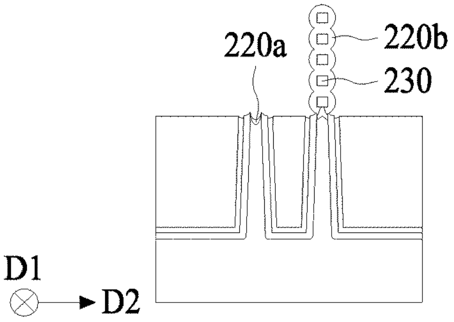


FIG. 7B



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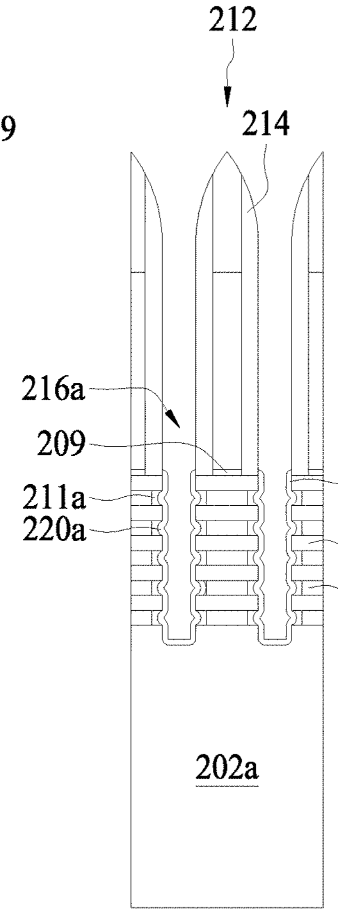

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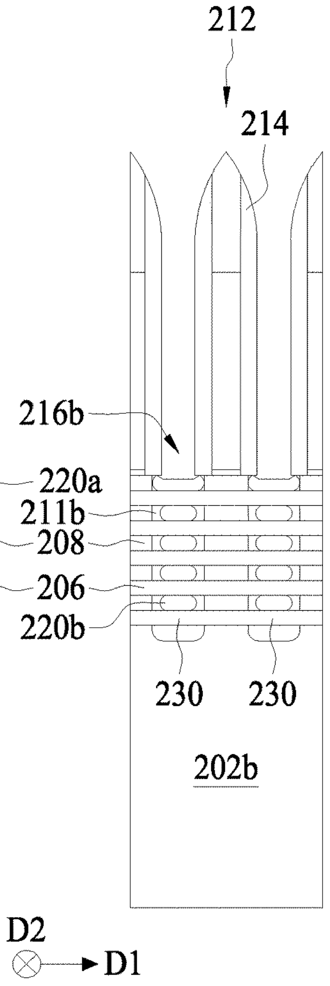


FIG. 7D

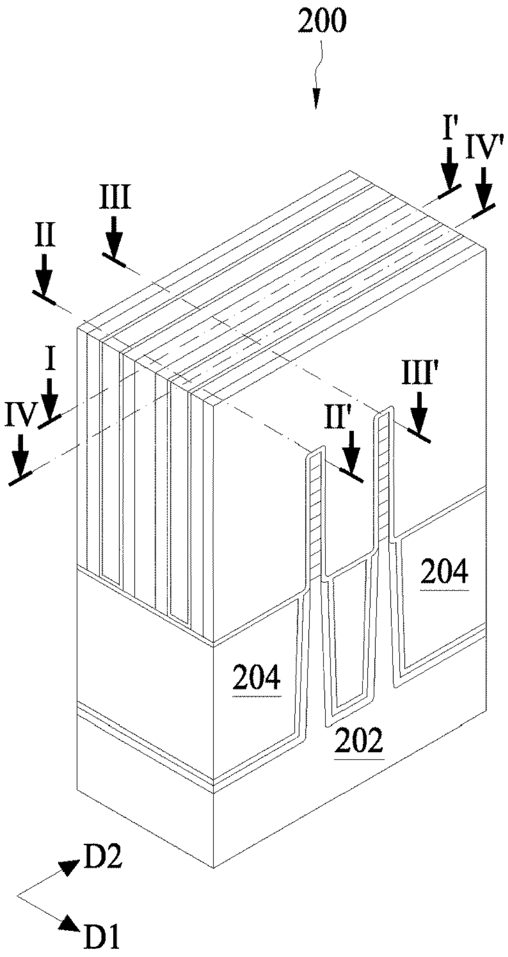


FIG. 8A

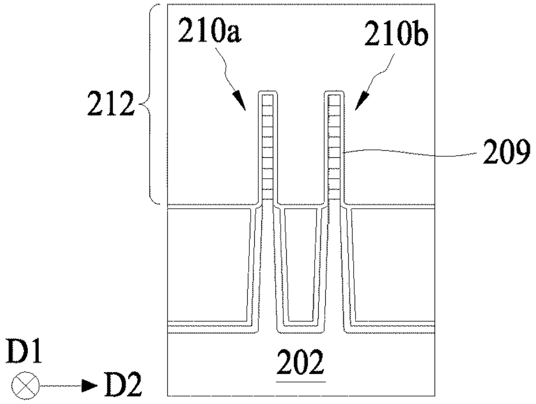
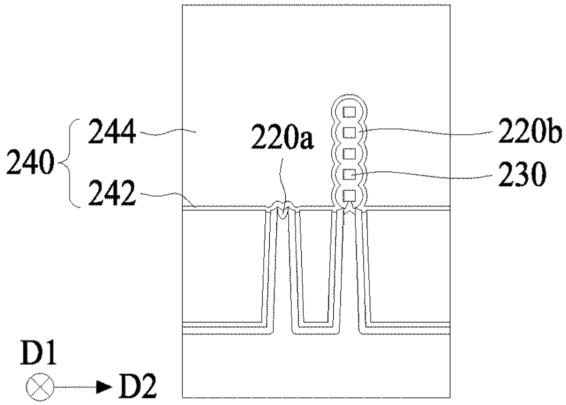


FIG. 8B



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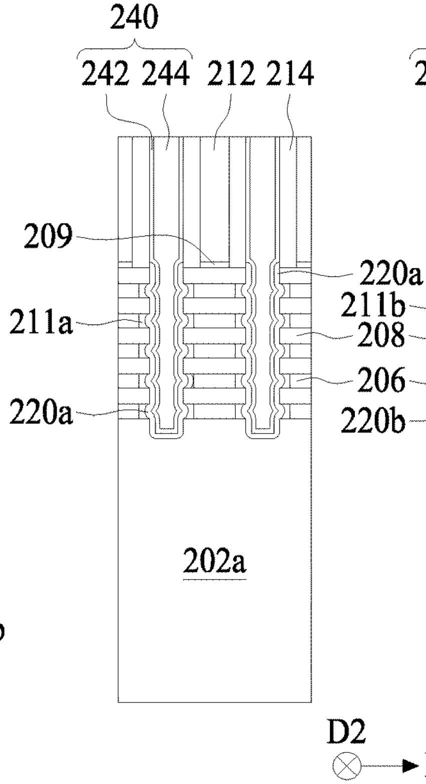

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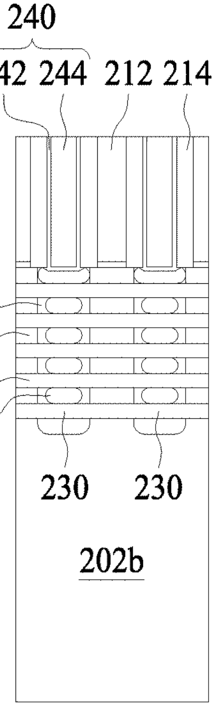

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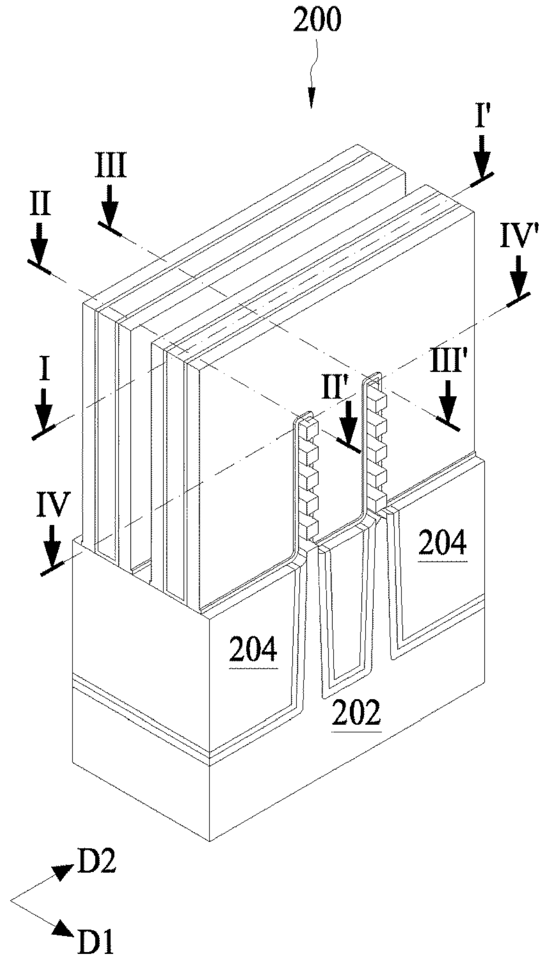


FIG. 9A

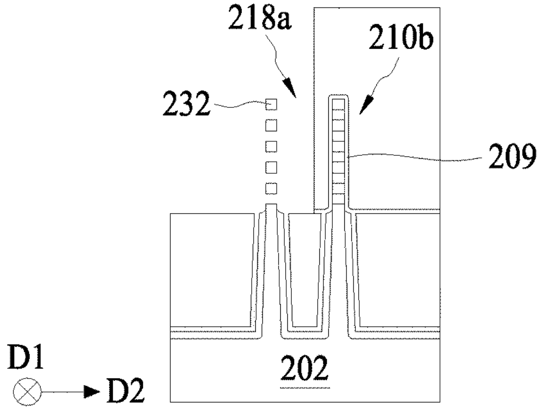


FIG. 9B

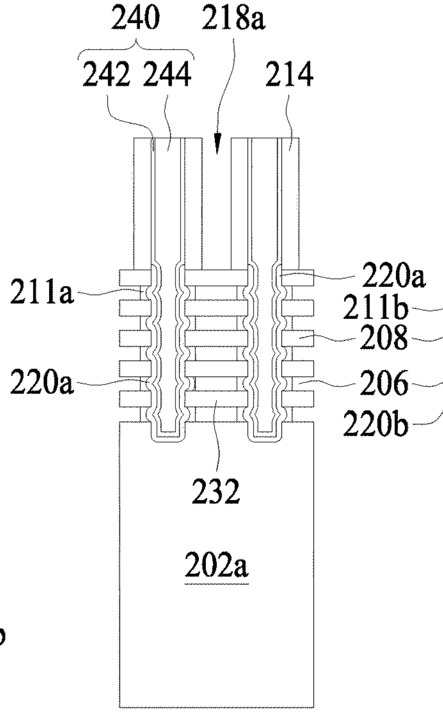


FIG. 9C

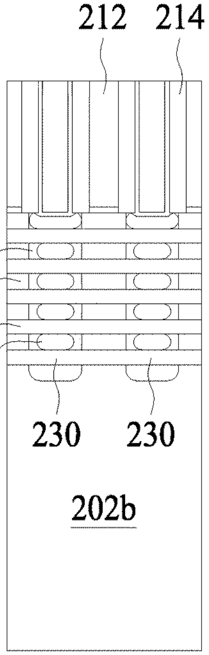


FIG. 9D

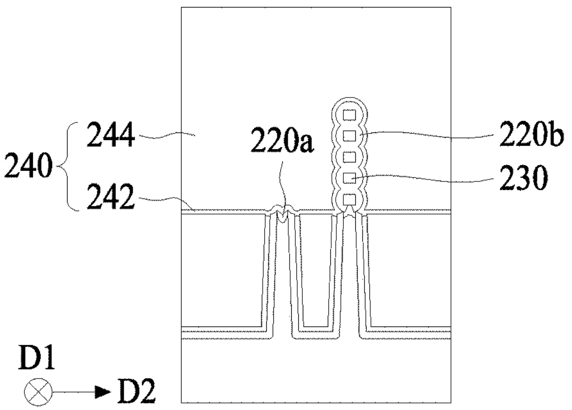


FIG. 9E

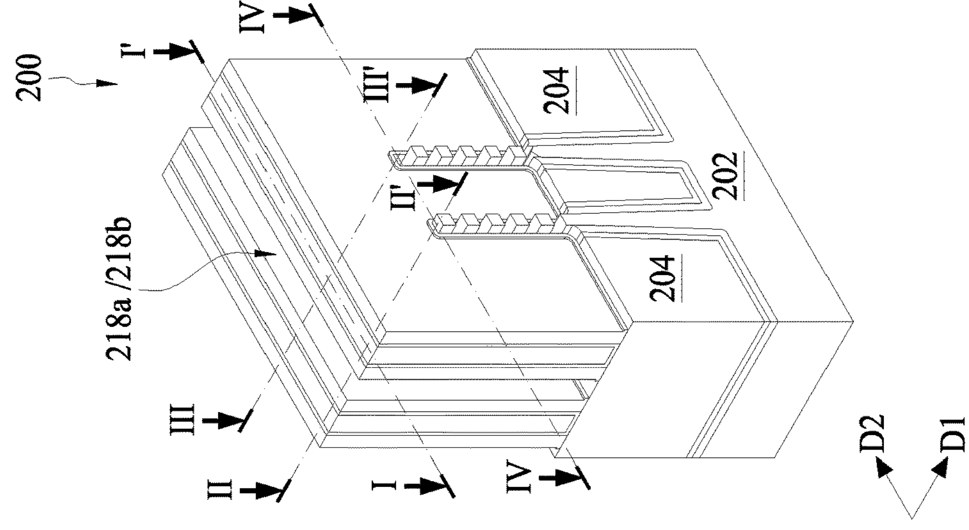


FIG. 10A

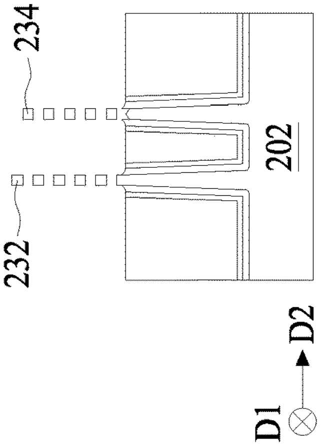


FIG. 10B

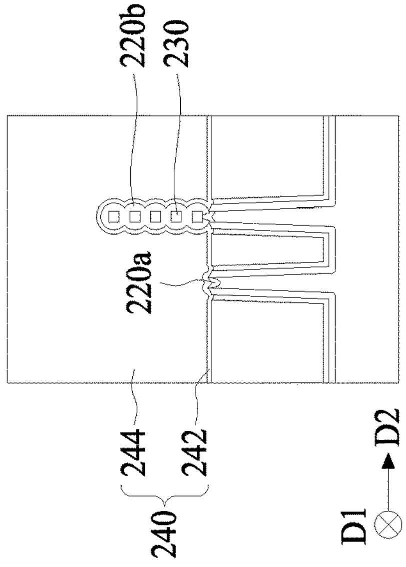


FIG. 10E

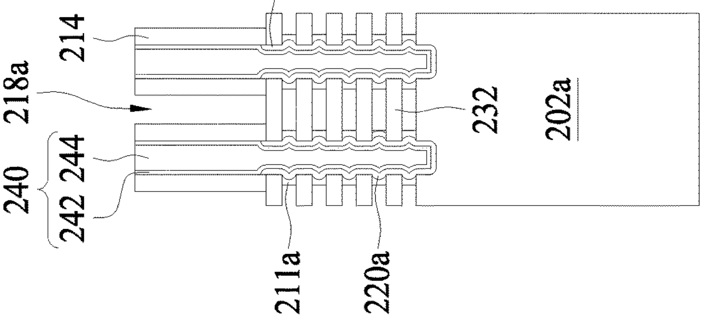


FIG. 10C

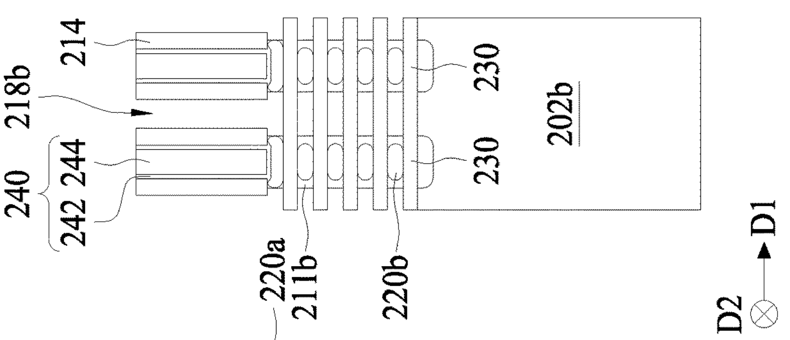


FIG. 10D

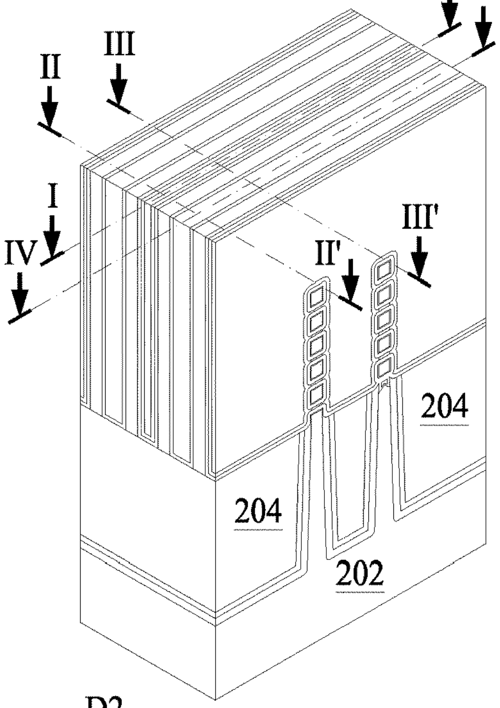


FIG. 11A

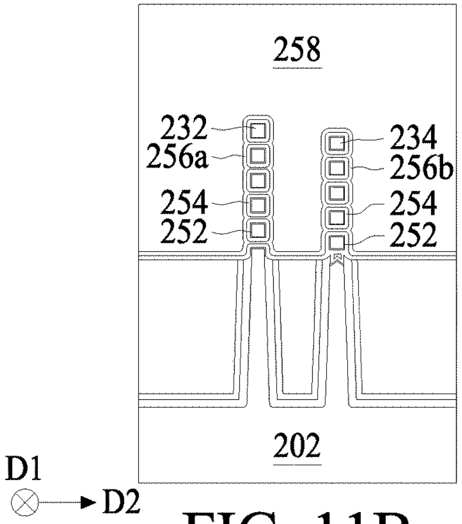


FIG. 11B

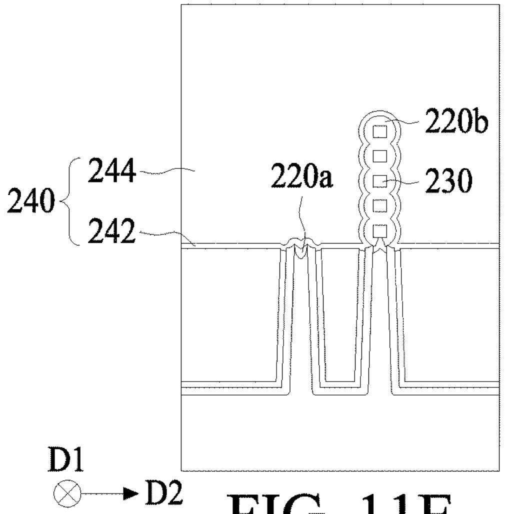


FIG. 11E

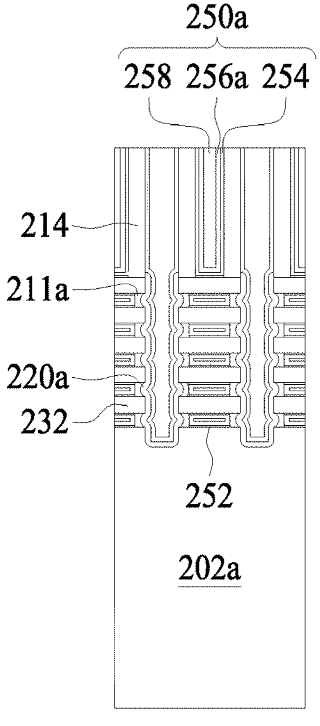


FIG. 11C

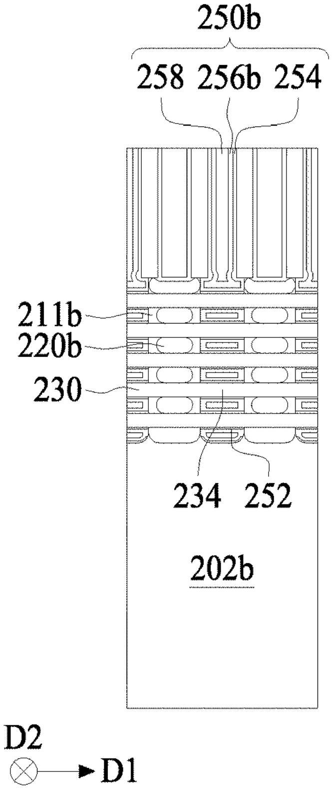


FIG. 11D

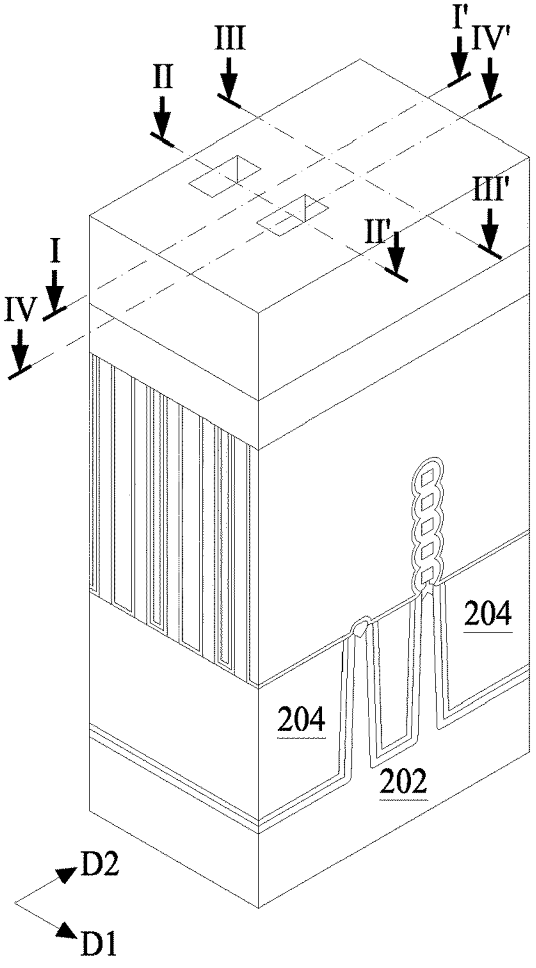


FIG. 12A

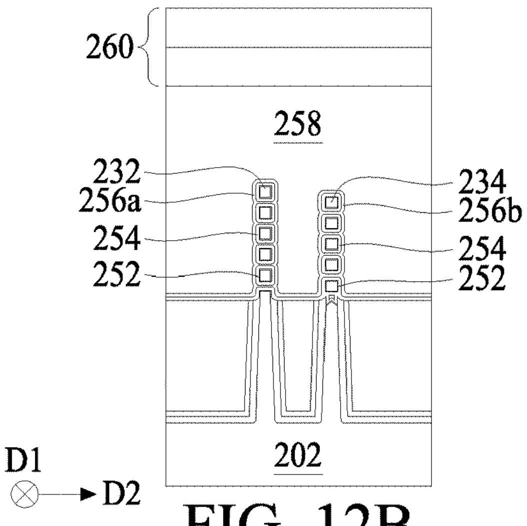
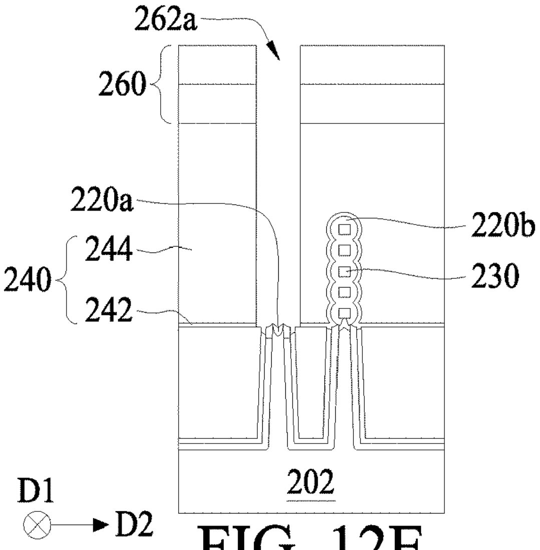


FIG. 12B



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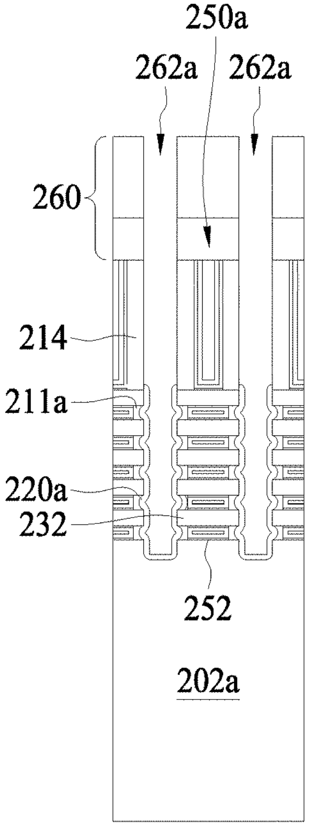

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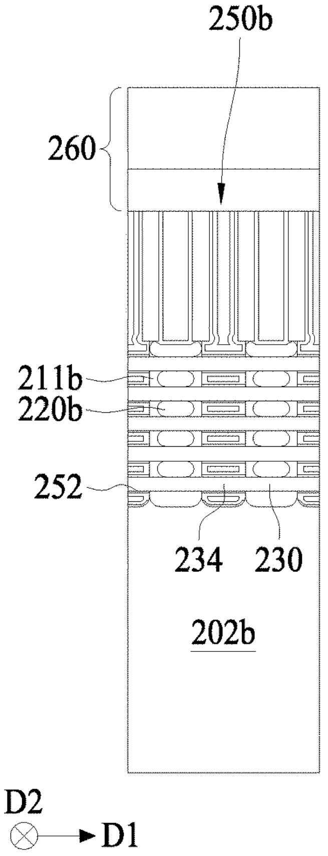


FIG. 12D

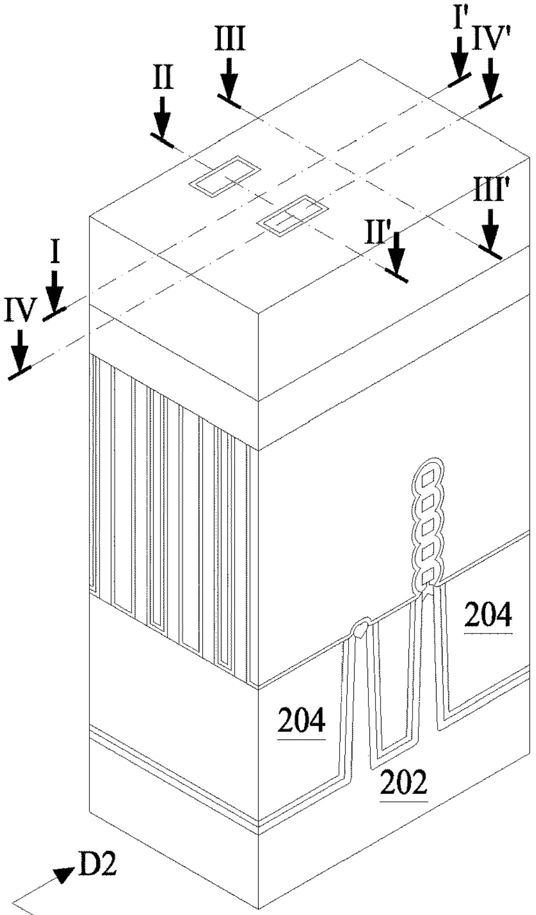


FIG. 13A

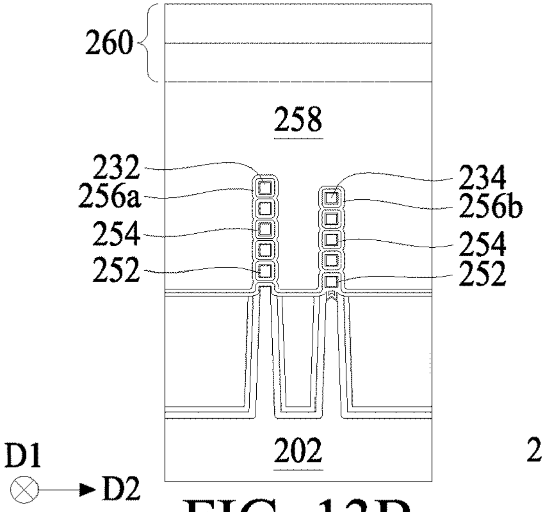


FIG. 13B

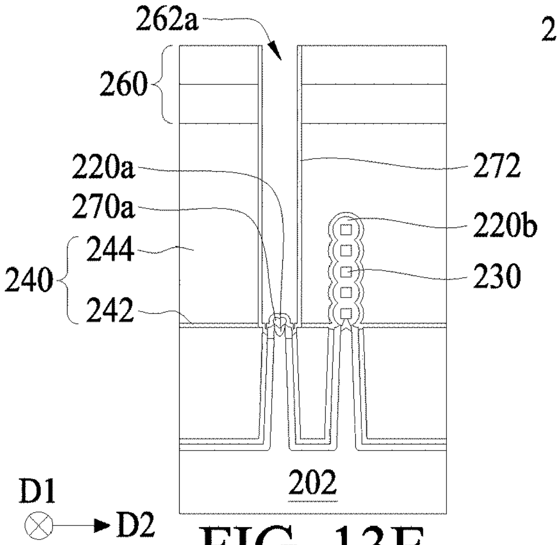


FIG. 13E

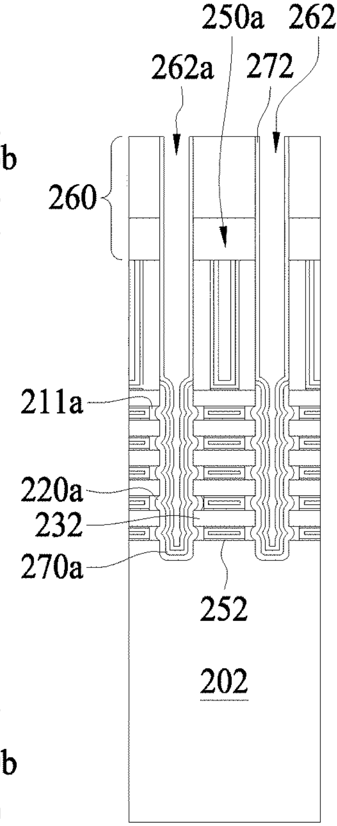


FIG. 13C

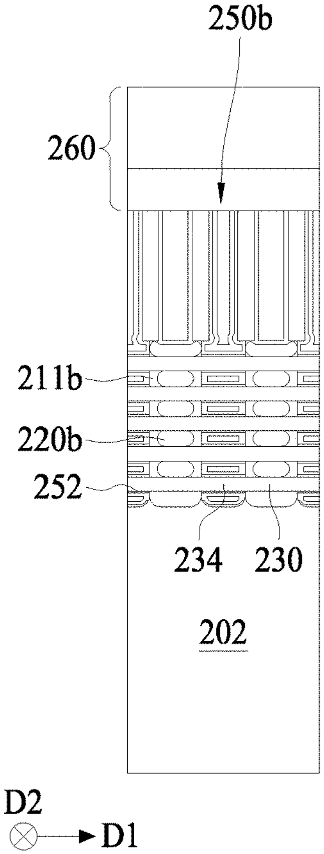


FIG. 13D

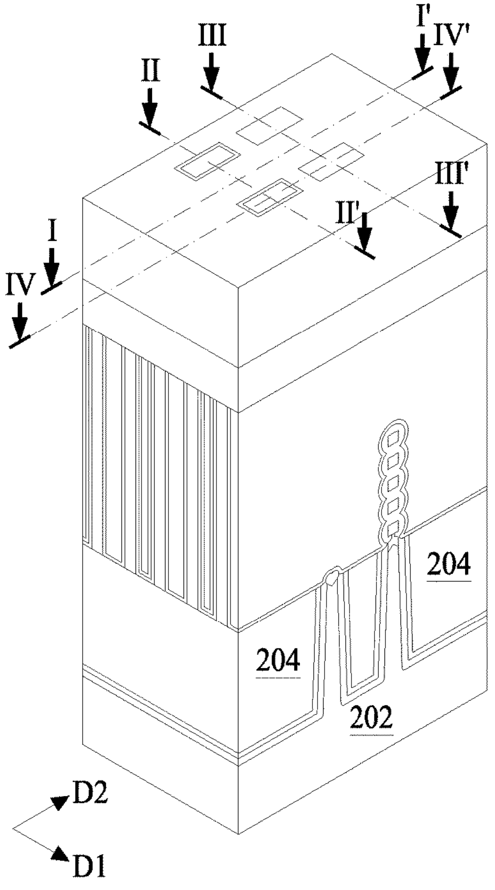


FIG. 14A

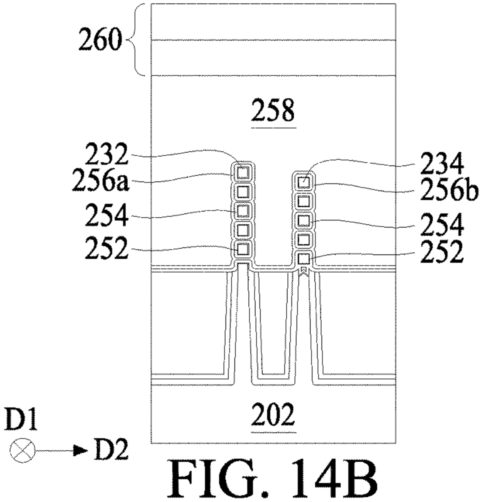


FIG. 14B

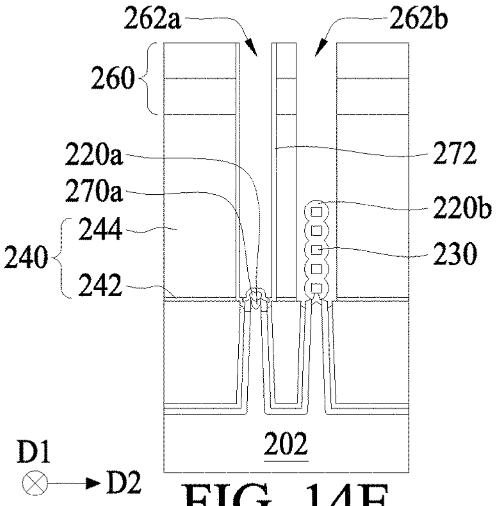
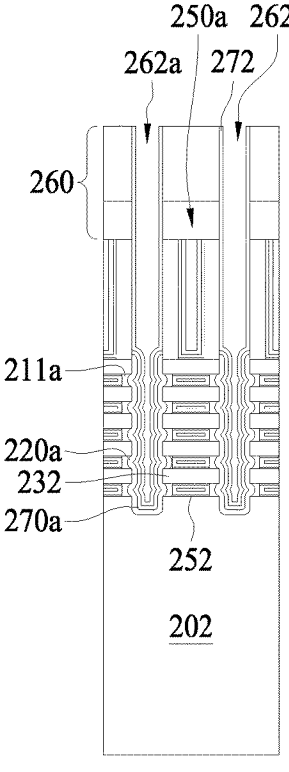


FIG. 14E



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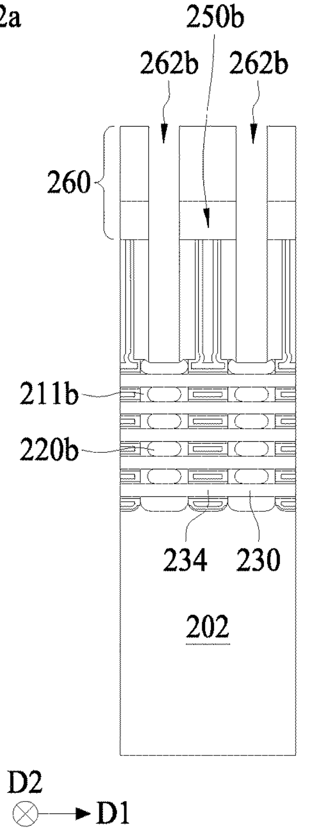

FIG. 14D

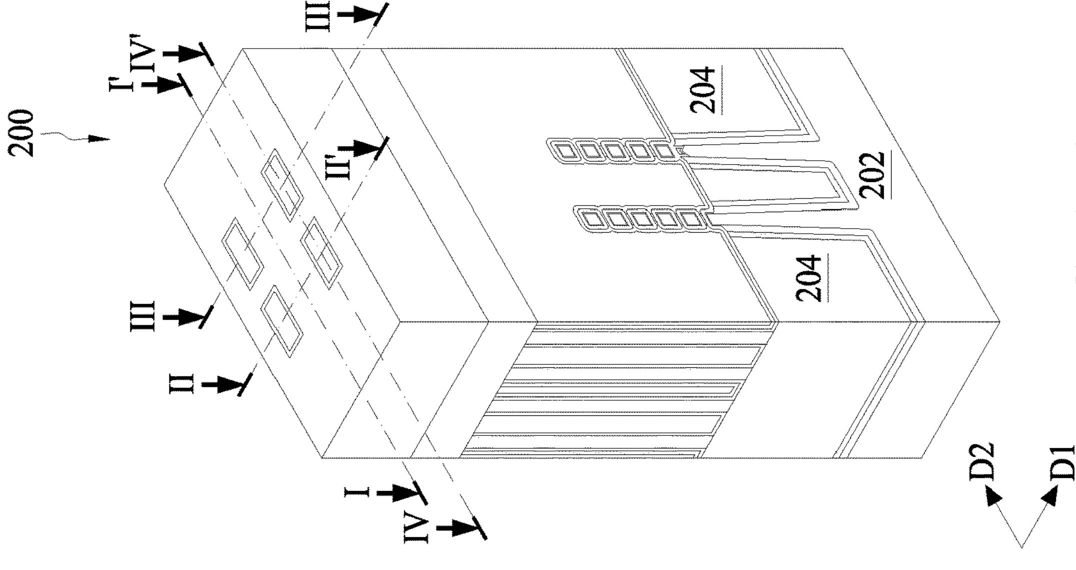

FIG. 15A

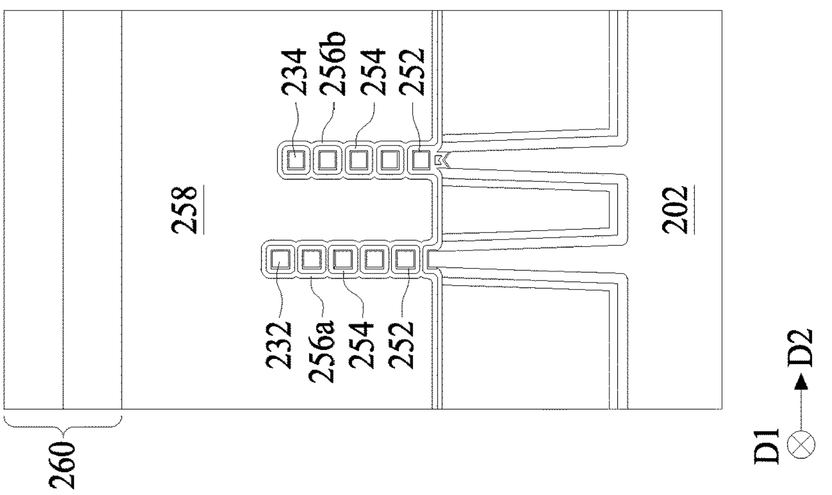

FIG. 15B

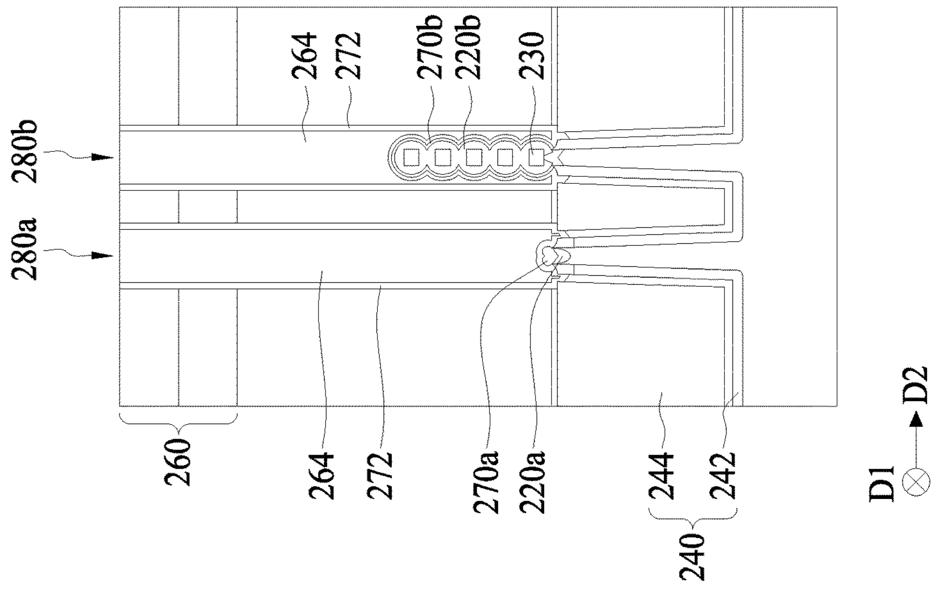

FIG. 15E

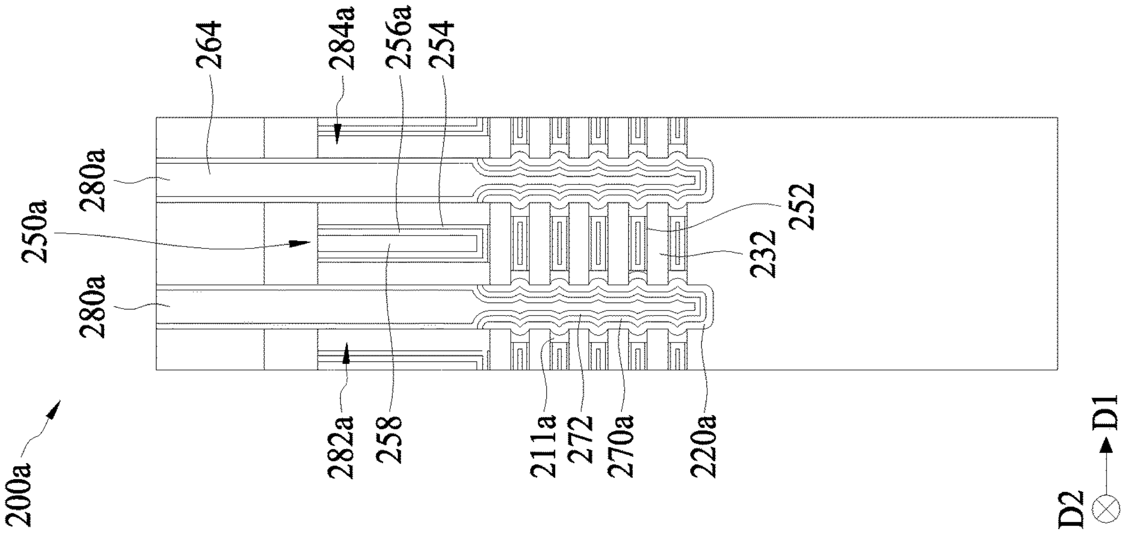

FIG. 15C

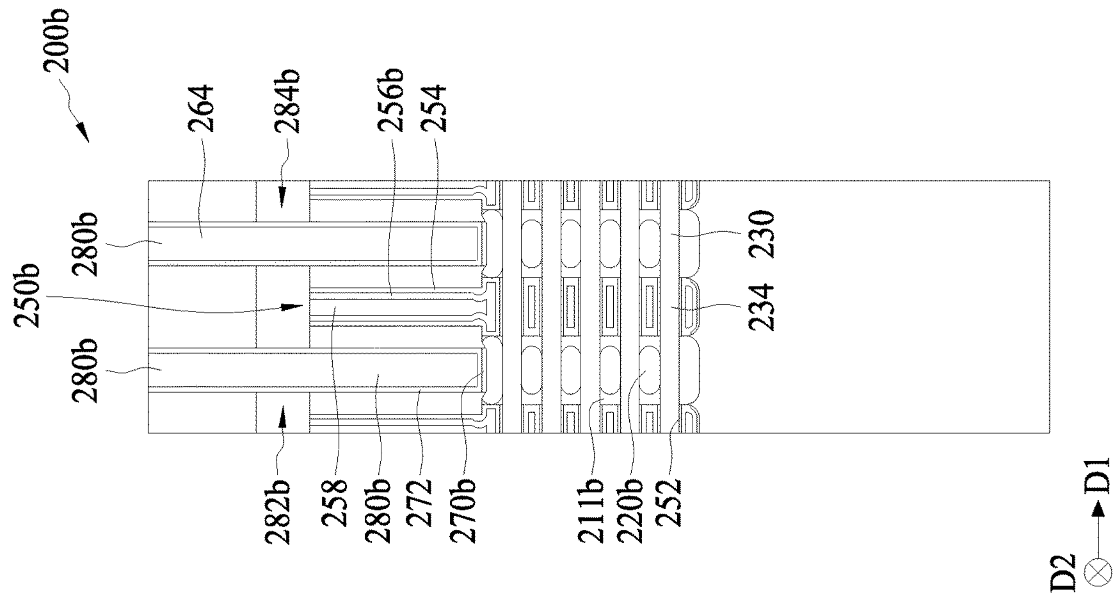

FIG. 15D

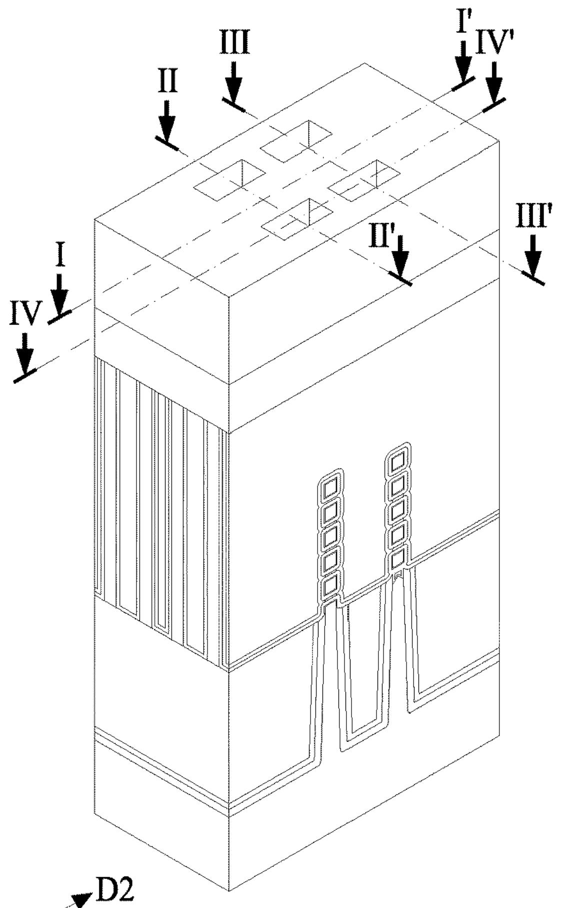

FIG. 16A

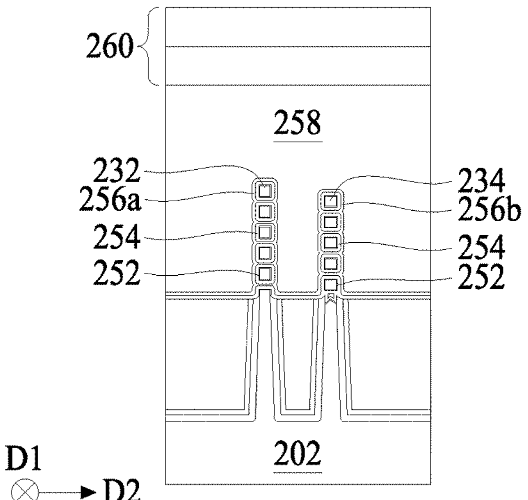

FIG. 16B

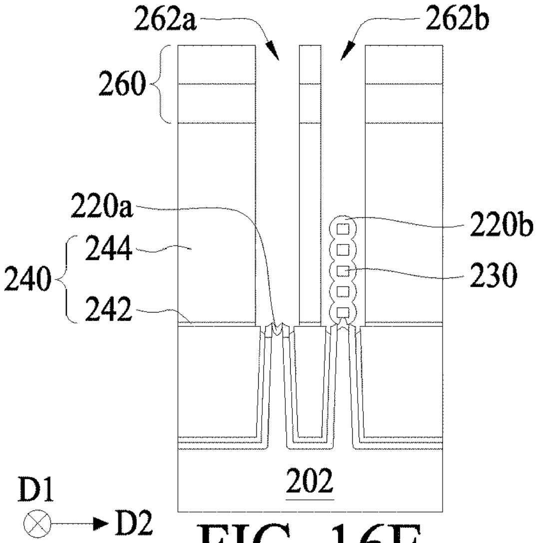

FIG. 16E

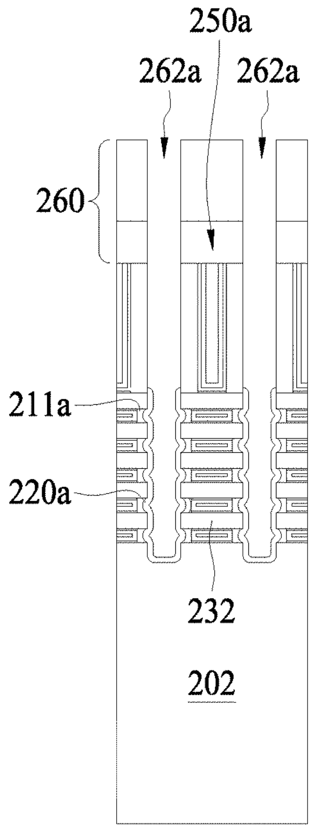

FIG. 16C

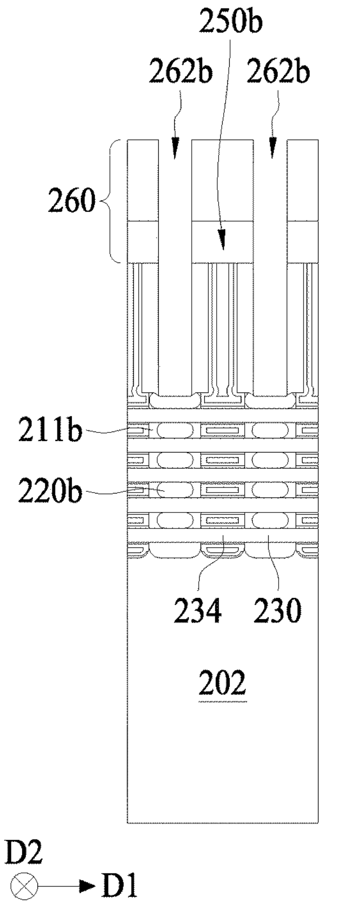

FIG. 16D

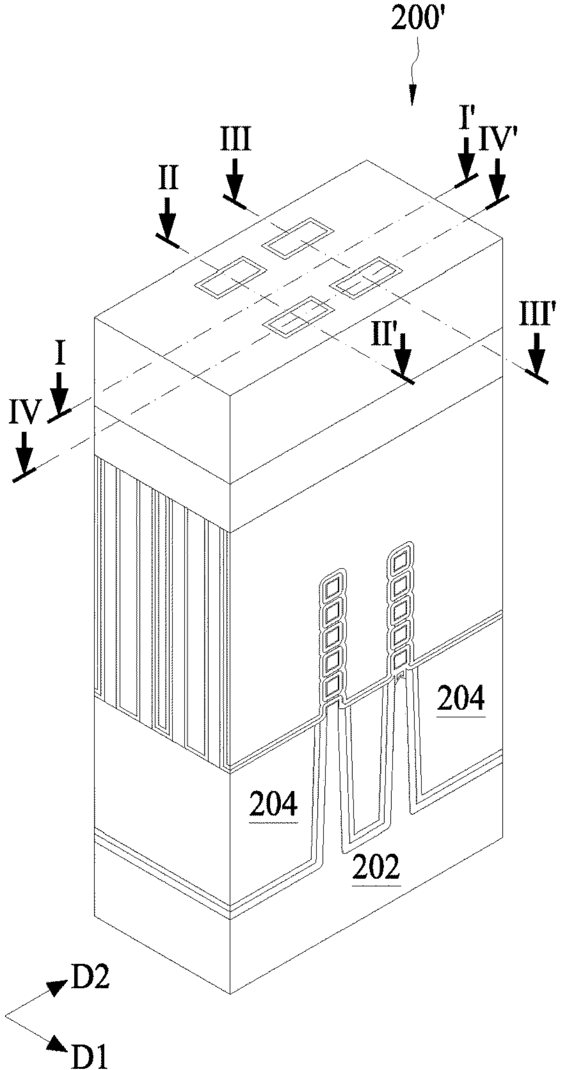

FIG. 17A

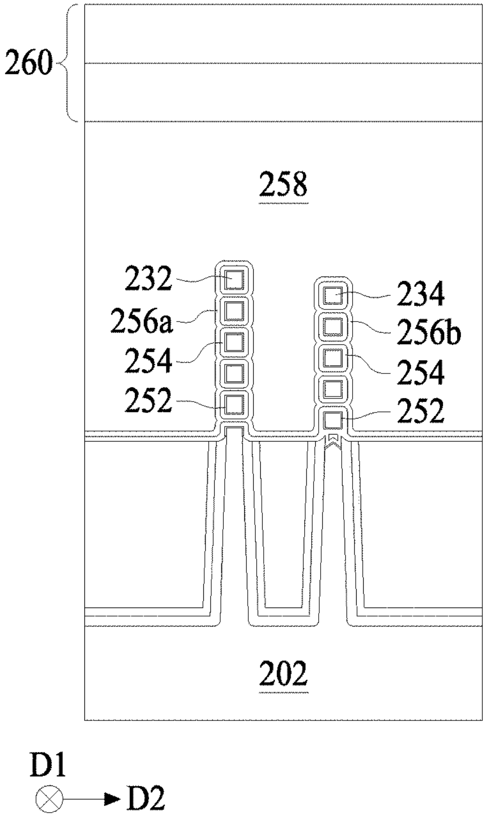

FIG. 17B

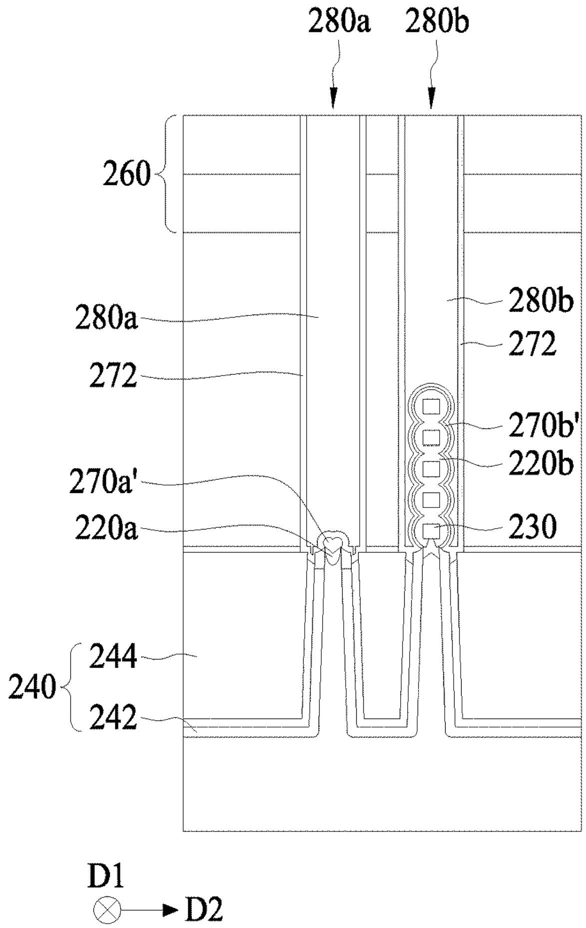

FIG. 17E

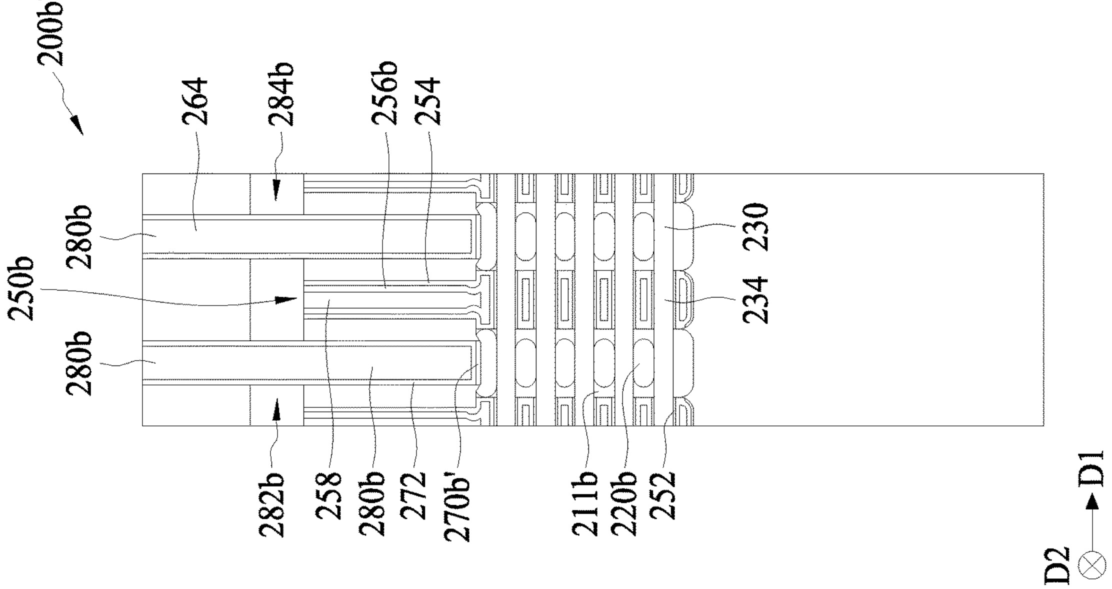

FIG. 17D

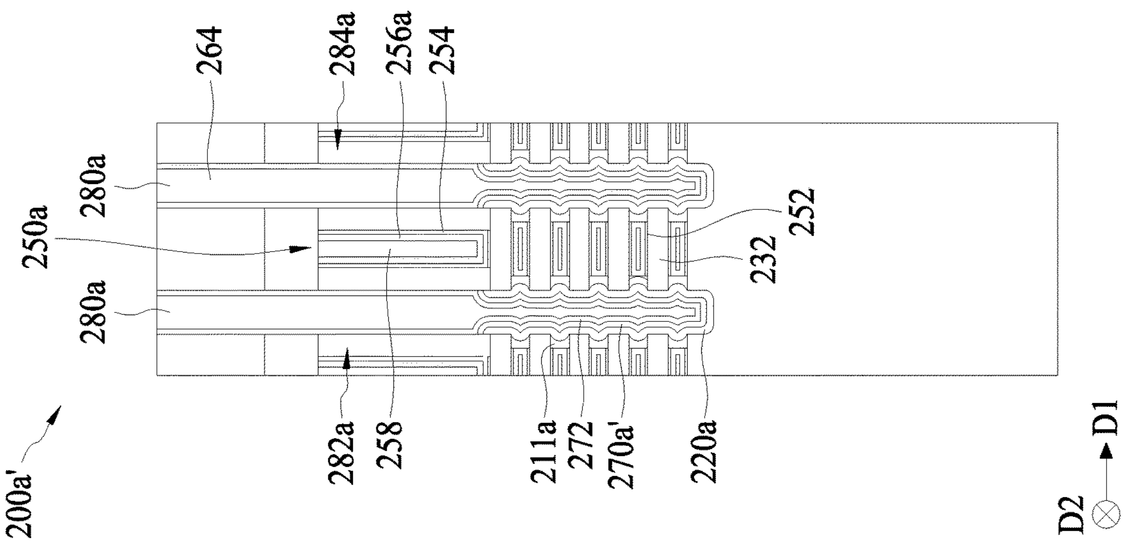

FIG. 17C

METHOD FOR FORMING MULTI-GATE SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Divisional application of U.S. patent application Ser. No. 16/681,097, filed on Nov. 12, 2019, which is a Continuation application of U.S. patent application Ser. No. 15/979,123, filed on May 14, 2018, the entirety of which are incorporated by reference herein.

BACKGROUND

[0002] As the semiconductor industry develops smaller and smaller nanoscale products and processes in pursuit of higher device density, higher performance, and lower costs, the challenges of downscaling both fabrication and design have led to the development of three-dimensional designs, such as multi-gate field effect transistor (FET) including a fin FET (FinFET) and a gate-all-around (GAA) FET. In a FinFET, a gate electrode is positioned adjacent to three side surfaces of a channel region with a gate dielectric layer interposed therebetween. Because the gate structure surrounds the fin on three sides, the transistor essentially has three gates controlling the current through the fin or channel region. However, the fourth side, the bottom part of the channel region, is positioned far away from the gate electrode and thus is not under close gate control. In contrast to a FinFET, a GAA FET includes an arrangement wherein all side surfaces of the channel region are surrounded by the gate electrode, allowing fuller depletion in the channel region and resulting in fewer short-channel effects due to a steeper sub-threshold current swing (SS) and smaller drain induced barrier lower (DIBL).

[0003] Although existing GAA FET devices and methods of fabricating GAA FET devices have been generally adequate for their intended purpose, such devices and methods have not been entirely satisfactory in all aspects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. **1** shows a flow chart representing a method for forming a multi-gate semiconductor structure according to aspects of the present disclosure.

[0006] FIG. **2** shows a flow chart representing a method for forming a multi-gate semiconductor structure according to aspects of the present disclosure.

[0007] FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A and **15**A illustrate a multi-gate semiconductor device at various fabrication stages constructed according to aspects of one or more embodiments of the present disclosure.

[0008] FIGS. **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **12**B, **13**B, **14**B and **15**B are cross-sectional views taken along line I-I' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0009] FIGS. **3**C, **4**C, **5**C, **6**C, **7**C, **8**C, **9**C, **10**C, **11**C, **12**C, **13**C, **14**C and **15**C are cross-sectional views taken along line II-II' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0010] FIGS. **3**D, **4**D, **5**D, **6**D, **7**D, **8**D, **9**D, **10**D, **11**D, **12**D, **13**D, **14**D, and **15**D are cross-sectional views taken along line III-III' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0011] FIGS. **4**E, **5**E, **6**E, **7**E, **8**E, **9**E, **10**E, **11**E, **12**E, **13**E, **14**E, and **15**E are cross-sectional views taken along line IV-IV' of FIGS. **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0012] FIGS. **16**A and **17**A illustrate a multi-gate semiconductor device at various fabrication stages constructed according to aspects of one or more embodiments of the present disclosure.

[0013] FIGS. **16**B and **17**B are cross-sectional views taken along line I-I' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0014] FIGS. **16**C and **17**C are cross-sectional views taken along line II-II' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0015] FIGS. **16**D and **17**D are cross-sectional views taken along line III-III' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure.

[0016] FIGS. **16**E and **17**E are cross-sectional view taken along line IV-IV' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure.

DETAILED DESCRIPTION

[0017] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0018] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” “on” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0019] As used herein, the terms such as "first," "second" and "third" describe various elements, components, regions, layers and/or sections, but these elements, components, regions, layers and/or sections should not be limited by these terms. These terms may be only used to distinguish one element, component, region, layer or section from another. The terms such as "first," "second" and "third" when used herein do not imply a sequence or order unless clearly indicated by the context.

[0020] As used herein, the terms "approximately," "substantially," "substantial" and "about" are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can refer to instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can refer to a range of variation of less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, two numerical values can be deemed to be "substantially" the same or equal if a difference between the values is less than or equal to ±10% of an average of the values, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, "substantially" parallel can refer to a range of angular variation relative to 0° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°. For example, "substantially" perpendicular can refer to a range of angular variation relative to 90° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°.

[0021] The gate-all-around (GAA) transistor structures may be patterned by any suitable method. For example, the structures may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-aligned process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the GAA structure.

[0022] GAA transistor structures may include nanowire structures, which are a promising candidate for logic device applications in future technologies. While downscaling device pitch, external resistance of source/drain and metal contact becomes a dominant factor in determining the device performance, more of a factor than channel resistance. As circuit density and device density increase, metal contact dimensions have to be decreased accordingly in order to minimize the ratio of contact area to the total chip area. Contact resistance is normally inverse to contact area. That is, a smaller contact area will correspond to a greater contact resistance. Further, within a limited contact area, resistance of a metal contact will be increased not only due to a smaller metal volume in the limited contact area, but also due to the inferior current spreading in metal. This makes contact resistance a significant and sometimes dominant factor in very large scale integration (VLSI) metal system performance.

[0023] It is therefore concluded that electrical contacts and associated contact resistance, which are required to conduct both power and signals throughout the integrated circuitry, are important in the manufacturing and subsequent operation of integrated circuit devices.

[0024] It should be noted that the present disclosure presents embodiments in the form of multi-gate transistors or fin-type multi-gate transistors referred to herein as FinFET devices. The FinFET devices may be GAA devices, Omega-gate (a-gate) devices, Pi-gate (H-gate) devices, dual-gate devices, tri-gate devices, bulk devices, silicon-on-insulator (SOI) devices, and/or other configurations. One of ordinary skill may recognize other examples of semiconductor devices that may benefit from aspects of the present disclosure.

[0025] FIG. **1** is a flow chart representing a method for forming a multi-gate semiconductor structure **10***a* according to aspects of the present disclosure. The method **10***a* includes an operation **102**, receiving a substrate including at least a first fin structure and a second fin structure. The method **10***a* further includes an operation **104**, disposing a dummy gate structure over a portion of the first fin structure and a portion of the second fin structure. The method **10***a* further includes an operation **106***a,* removing portions of the first fin structure exposed through the dummy gate structure to form at least a first recess in the substrate. The method **10***a* further includes an operation **108***a,* forming a first semiconductor layer in the first recess. The method **10***a* further includes an operation **110**, disposing a dielectric structure over the substrate. The method **10***a* further includes an operation **112***a*, removing a portion of the dummy gate structure to form a first gate trench in the dielectric structure. The method **10***a* further includes an operation **114***a,* forming a plurality of first nanowires and a first gate structure in the first gate trench. The method **10***a* further includes an operation **116***a,* removing a portion of the dielectric structure to form a first opening in the dielectric structure. The method **10***a* further includes an operation **118***a,* forming a first metal silicide layer over the first semiconductor layer in the first opening. The method **10***a* further includes an operation **120***a,* disposing a metal layer to fill the first opening. The method **10***a* will be further described according to one or more embodiments. It should be noted that the operations of the method for forming the multi-gate semiconductor device **10***a* may be rearranged or otherwise modified within the scope of the various aspects. It should be further noted that additional processes may be provided before, during, and after the method **10***a,* and that some other processes may be only briefly described herein. Thus other implementations are possible within the scope of the various aspects described herein.

[0026] FIG. **2** is a flow chart representing a method for forming a multi-gate semiconductor structure **10***b* according to aspects of the present disclosure. In some embodiments, the method **10***b* and the method **10***a* share similar operations, but the disclosure is not limited thereto. The method **10***b* includes the operation **102**, receiving a substrate including at least a first fin structure and a second fin structure. The method **10***b* further includes the operation **104**, disposing a dummy gate structure over a portion of the first fin structure and a portion of the second fin structure. The method **10***b* further includes an operation **106***b*, removing portions of the second fin structure exposed through the dummy gate structure to form at least a second recess in the substrate and a plurality of nanowires suspended in the second recess. The method **10***b* further includes an operation **108***b,* forming a second semiconductor layer surrounding each of the plurality of second nanowires. The method **10***b* further includes the operation **110**, disposing a dielectric structure over the substrate. The method **10***b* further includes an operation **112***b,* removing a portion of the dummy gate structure to form a second gate trench in the dielectric structure. The method **10***b* further includes an operation **114***b,* forming a plurality of third nanowires and a second gate structure in the second gate trench. The method **10***b* further includes an operation **116***b,* removing a portion of the dielectric structure to form a second opening in the dielectric structure. The method **10***b* further includes an operation **118***b,* forming a second metal silicide layer over the second semiconductor layer. The method **10***b* further includes an operation **120***b,* disposing a metal layer to fill the second opening. The method **10***b* will be further described according to one or more embodiments. It should be noted that the operations of the method for forming the multi-gate semiconductor device **10***b* may be rearranged or otherwise modified within the scope of the various aspects. Further, the method **10***a* and the method **10***b* can be integrated, and thus similar operations can be performed simultaneously. In some embodiments, operations **116***b* and **118***b* of the method **10***b* are performed after operations **116***a* and **118***a* of the method **10***a*. In other embodiments, operations **116***a* and **118***a* of the method **10***a* and operations **116***b* and **118***b* of the method **10***b* are simultaneously performed. It should be further noted that additional processes may be provided before, during, and after the method **10***b,* and that some other processes may be only briefly described herein. Thus other implementations are possible within the scope of the various aspects described herein.

[0027] FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, and **15**A are drawings illustrating a multi-gate semiconductor device **300** at various fabrication stages constructed according to aspects of one or more embodiments the present disclosure. FIGS. **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **12**B, **13**B, **14**B, and **15**B are cross-sectional views taken along line I-I' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure, FIGS. **3**C, **4**C, **5**C, **6**C, **7**C, **8**C, **9**C, **10**C, **11**C, **12**C, **13**C, **14**C, and **15**C are cross-sectional views taken along line II-II' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure, FIGS. **3**D, **4**D, **5**D, **6**D, **7**D, **8**D, **9**D, **10**D, **11**D, **12**D, **13**D, **14**D, and **15**D are cross-sectional views taken along line III-III' of FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure, and FIGS. **4**E, **5**E, **6**E, **7**E, **8**E, **9**E, **10**E, **11**E, **12**E, **13**E, **14**E, and **15**E are cross-sectional views taken along line IV-IV' of FIGS. **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, and **15**A, respectively, according to aspects of one or more embodiments of the present disclosure. As shown in FIGS. **3**A to **3**D, a substrate **202** is provided. In some embodiments, the substrate **202** may be a semiconductor substrate such as a silicon substrate. The substrate **202** may also include other semiconductors such as germanium (Ge), silicon carbide (SiC), silicon germanium (SiGe), or diamond. Alternatively, the substrate **202** may include a compound semiconductor and/or an alloy semiconductor. The substrate **202** may include various layers, including conductive or insulating layers formed on a semiconductor substrate. The substrate **202** may include various doping configurations depending on design requirements as is known in the art. For example, different doping profiles (e.g., n wells, p wells) may be formed on the substrate **202** in regions **202***a* and **202***b* designed for different device types (e.g., n-type field effect transistors (NFET), or p-type field effect transistors (PFET)), as shown in FIGS. **3**C and **3**D. The suitable doping may include ion implantation of dopants and/or diffusion processes. The substrate **202** typically has isolation features (e.g., shallow trench isolation (STI) features) **204** interposing the regions **202***a* and **202***b* providing different device types. Further, the substrate **202** may optionally include an epitaxial layer (epi-layer), may be strained for performance enhancement, may include an SOI structure, and/or may have other suitable enhancement features. A stack including semiconductor layers is formed over the substrate **202**. In some embodiments, a strain relaxed buffer (SRB) layer (not shown) can be formed over the substrate **202**. The SRB layer may be different in composition from the substrate **202** in order to create lattice strain at the interface with the substrate **202**. For example, in some embodiments, the substrate **202** includes silicon and is substantially free of germanium while the SRB layer includes SiGe.

[0028] Still referring to FIGS. **3**A to **3**D, a stack including semiconductor layers is formed over the substrate **202**. In embodiments that include an SRB layer disposed on the substrate **202**, the stack of semiconductor layers may be disposed on the SRB layer. The stack of semiconductor layers may include alternating layers of different compositions. For example, in some embodiments, the stack includes semiconductor layers **206** of a first composition alternating with semiconductor layers **208** of a second composition. By way of example, growth of the layers of the stack may be performed by a molecular beam epitaxy (MBE) process, a metalorganic chemical vapor deposition (MOCVD) process, and/or other suitable epitaxial growth processes. Although five semiconductor layers **206** and five semiconductor layers **208** are shown, it should be understood that the stack may include any number of layers of any suitable composition with various examples including between 2 and 10 semiconductor layers **206** and between 2 and 10 semiconductor layers **208**. As explained below, the different compositions of the layers in the stack (e.g., semiconductor layers **206** and semiconductor layers **208**) may be used to selectively process some of the layers. Accordingly, the compositions may have different oxidation rates, etchant sensitivity, and/or other differing properties. The semiconductor layers **206** and

208 may have thicknesses chosen based on device performance considerations. In some embodiments, the semiconductor layers **206** are substantially uniform in thickness, and the semiconductor layers **208** are substantially uniform in thickness. In some embodiments, the thickness of the semiconductor layers **206** can be less than the thickness of the semiconductor layers **208**, but the disclosure is not limited thereto. For example but not limited thereto, the thickness of the semiconductor layers **206** can be approximately 6 nanometers (nm), and the thickness of the semiconductor layers **208** can be approximately 8 nm.

[0029] In some embodiments, the semiconductor layers **208** may include a first semiconductor material such as Si while the semiconductor layers **206** may include the first semiconductor material and a second semiconductor material with a lattice constant greater than a lattice constant of the first semiconductor material. For example, the semiconductor layers **206** may include SiGe, but the disclosure is not limited thereto. Additionally, Ge concentration in the semiconductor layers **206** can be less than or equal to approximately 50%, but the disclosure is not limited thereto. In other embodiments, the semiconductor layers **206** may include other materials such as a compound semiconductor such as SiC, gallium arsenide (GaAs), gallium phosphide (GaP), indium phosphide (InP), indium arsenide (InAs), and/or indium antimonide (InSb), an alloy semiconductor such as SiGe, GaAsP, AlinAs, AlGaAs, InGaAs, GaInP, and/or GaInAsP, or combinations thereof. In some embodiments, the semiconductor layers **206** and **208** may be undoped or substantially dopant-free, where, for example, no doping is performed during the epitaxial growth process. Alternatively, the semiconductor layers **206** and **208** may be doped. For example, the semiconductor layers **206** or **208** may be doped with a p-type dopant such as boron (B), aluminum (Al), In, and Ga for forming a p-type channel, or an n-type dopant such as P, As, Sb, for forming an n-type channel.

[0030] Still referring to FIGS. **3**A to **3**D, at least a first fin structure **210***a* and at least a second fin structure **210***b* are formed over the substrate **202** from the stack of semiconductor layers **206**/**208**. The first fin structure **210***a* and the second fin structure **210***b* may be fabricated using suitable operations including photolithography and etch operations. In some embodiments, forming the first and second fin structures **210***a* and **210***b* may further include a trim process to decrease the width and/or the height of the first and second fin structures **210***a* and **210***b*. The trim process may include wet or dry etching processes. The height and width of the first and second fin structures **210***a* and **210***b* may be chosen based on device performance considerations. Further, the first and second fin structures **210***a* and **210***b* can extend along a first direction D**1** as shown in FIGS. **3**A to **3**D. Accordingly, the substrate **202** including the at least one first fin structure **210***a* and at least one second fin structure **210***b* is received according to operation **102** of the method **10***a* and the method **10***b*.

[0031] Referring to FIGS. **4**A to **4**E, in some embodiments, a liner **209** can be formed over the first fin structure **210***a*, the second fin structure **210***b* and the substrate **202**. Next, a dummy gate structure **212** is disposed over a portion of the first fin structure **210***a* and a portion of the second fin structure **210***b* according to operation **104** of the method **10***a* and the method **10***b*. The dummy gate structure **212** may be replaced at a later processing stage by a high-K dielectric layer (HK) and metal gate electrode (MG) as discussed below. In some embodiments, the dummy gate structure **212** is formed over the substrate **202** and extends along a second direction D**2**, which is not parallel with the first direction D**1**. Additionally, the first direction D**1** and the second direction D**2** are in the same plane. As shown in FIGS. **4**A to **4**D, the portion of the first fin structure **210***a* underlying the dummy gate structure **212** may be referred to as the channel region, and the portion of the second fin structure **210***b* underlying the dummy gate structure **212** may be referred to as the channel region. The dummy gate structure **212** may also define a source/drain region of the first fin structure **210***a*, for example, portions of the first fin structure **210***a* adjacent to and on opposing sides of the channel region. Similarly, the dummy gate structure **212** may also define a source/drain region of the second fin structure **210***b*, for example, portions of the second fin structure **210***b* adjacent to and on opposing sides of the channel region. In some embodiments, the dummy gate structure **212** can include at least a polysilicon layer and a patterned hard mask for defining the dummy gate structure.

[0032] Still referring to FIGS. **4**A to **4**E, a spacer **214** can be disposed over sidewalls of the dummy gate structure **212**, and portions of the first and second fin structures **210***a* and **210***b* are exposed through the dummy gate structure **212** and the spacer **214**. In some embodiments, the spacer **214** includes insulating materials. As shown in FIGS. **4**A, **4**C and **4**D, the sidewalls of the dummy gate structure **212** are covered by the spacer **214**. In some embodiments, portions of the liner **209** can be removed during or after the forming of the spacer **214**, and thus portions of the first and second fin structures **210***a* and **210***b* are exposed as shown in FIGS. **4**C to **4**E.

[0033] Referring to FIGS. **5**A to **5**E, next, the portions of the first fin structure **210***a* exposed through the dummy gate structure **212** and the spacer **214** are removed according to operation **106***a*. In some embodiments, portions of the semiconductor layers **206** and portions of the semiconductor layers **208** exposed through the dummy gate structure **212** and the spacer **214** are removed, thereby forming at least a first recess **216***a* in the substrate **202** as shown in FIG. **5**C. In some embodiments, a patterned protecting layer (not shown) is formed over the second fin structure **210***b* or deposited over the region **202***b*. Thus the second fin structure **210***b* is protected and impervious to the formation of the first recess **216***a*. The semiconductor layers **206**, and the semiconductor layers **208** are exposed through sidewalls of the first recess **216***a* and the substrate **202** is exposed through a bottom of the first recess **216***a*. In some embodiments, a portion of each of the exposed semiconductor layers **206** is removed and thus a plurality of notches (not shown) are formed. In some embodiments, an insulating layer (not shown) is formed over the substrate **202** and a suitable etching operation is then performed. Thus, a plurality of inner spacers **211***a* are formed in the notches as shown in FIG. **5**C. Consequently, the semiconductor layers **208** and the inner spacers **211***a* are exposed. In other words, the semiconductor layers **206** are enclosed by the semiconductor layers **208** and the inner spacers **211***a*. In some embodiments, the inner spacers **211***a* include one or more insulating materials such as SiN, SiO, SiC, SiOC, SiOCN, other materials, or a combination thereof, but the disclosure is not limited thereto.

[0034] Still referring to FIGS. **5**A to **5**E, a first semiconductor layer **220***a* is formed in the first recess **216***a* according to operation **108***a* of the method **10***a*. In some embodiments, the first semiconductor layer **220***a* is a doped epitaxial semiconductor layer. In some embodiments, the first semiconductor layer **220***a* is a phosphorus-doped silicon (SiP) epitaxial layer, but the disclosure is not limited thereto. Additionally, the first semiconductor layer **220***a* covers the semiconductor layers **208**, the inner spacers **211***a* and the bottom of the first recess **216***a*. Subsequently, the patterned protecting layer is removed from the substrate **202** after the forming of the first semiconductor layer **220***a* as shown in FIGS. **5**A to **5**E. In some embodiments, a thickness of the first semiconductor layer **220***a* is between approximately 10 nm and approximately 20 nm, but the disclosure is not limited thereto.

[0035] Referring to FIGS. **6**A to **6**E, next, portions of the second fin structure **210***b* exposed through the dummy gate structure **212** and the spacer **214** are removed according to operation **106***b* of the method **10***b*. In some embodiments, portions of the semiconductor layers **208** are removed, thereby forming at least a second recess **216***b* in the substrate **202** according to operation **106***b*. Significantly, a plurality of nanowires **230**, which previously comprised the semiconductor layers **206**, are formed in the second recess **216***b* according to operation **106***b*, as shown in FIGS. **6**D and **6**E. In some embodiments, a patterned protecting layer (not shown) is formed to fill the first recess **216***a* or deposited over the region **202***a*, and thus the first semiconductor layer **220***a* is protected and impervious to the formation of the second recess **216***b* and the plurality of nanowires **230**. As shown in FIGS. **6**D and **6**E, the plurality of nanowires **230** are suspended in and exposed through the second recess **216***b*, the semiconductor layers **208** are exposed through sidewalls of the second recess **216***b*, and the substrate **202** is exposed through a bottom of the second recess **216***b*.

[0036] Referring to FIGS. **7**A to **7**E, a portion of the exposed semiconductor layers **208** is then removed and thus a plurality of notches (not shown) are formed. In some embodiments, an insulating layer (not shown) is formed over the substrate **202** and a suitable etching operation is subsequently performed. Thus, a plurality of inner spacers **211***b* are formed in the notches and over the substrate **202**, as shown in FIG. **7**D. In other words, the semiconductor layers **208** are enclosed by the semiconductor layers **206** and the inner spacers **211***b*. In some embodiments, the inner spacers **211***b* include one or more insulating materials such as SiN, SiO, SiC, SiOC, SiOCN, other materials, or a combination thereof, but the disclosure is not limited thereto.

[0037] Still referring to FIGS. **7**A to **7**E, a second semiconductor layer **220***b* is formed in the second recess **216***b* according to operation **108***b* of the method **10***b*. The second semiconductor layer **220***b* is formed to surround each of the nanowires **230**, as shown in FIG. **7**E. In some embodiments, the second semiconductor layer **220***b* includes the first semiconductor material and the second semiconductor material. For example but not limited thereto, the second semiconductor layer **220***b* can include SiGe, and a Ge concentration of the second semiconductor layer **220***b* is greater than the Ge concentration of the plurality of nanowires **230**, which previously comprised the semiconductor layers **206**. In some embodiments, the Ge concentration of the second semiconductor layer **220***b* is greater than 50%, but the disclosure is not limited thereto. In some embodiments, the Ge concentration of the second semiconductor layer **220***b* is between approximately 50% and approximately 70%, but the disclosure is not limited thereto. In some embodiments, the second semiconductor layer **220***b* is a doped epitaxial semiconductor layer. For example but not limited thereto, the second semiconductor layer **220***b* can be a boron-doped silicon germanium (SiGeB) epitaxial layer. Further, the patterned protecting layer is removed from the substrate **202** after the forming of the second semiconductor layer **220***b*. In some embodiments, the method **10***a* and the method **10***b* are integrated such that operations **106***b* and **108***b* of the method **10***b* are performed after operations **106***a* and **108***a* of the method **10***a*. However, operations **106***b* and **108***b* of the method **10***b* can performed before operations **106***a* and **108***a* of the method **10***a* in other embodiments.

[0038] Referring to FIGS. **8**A to **8**E, a dielectric structure **240** is disposed over the substrate **202** according to operation **110** of the method **10***a* and the method **10***b*. The dielectric structure **240** fills the first recess **216***a* and the second recess **216***b*. In some embodiments, the dielectric structure **240** can include an etch-stop layer (e.g., a contact etch stop layer (CESL)) **242** and various dielectric layers (e.g., an inter-layer dielectric (ILD) layer) **244** formed on the substrate **202** after the forming of the second semiconductor layer **220***b*. In some embodiments, the CESL **242** includes a SiN layer, a SiCN layer, a SiON layer, and/or other materials known in the art. In some embodiments, the ILD layer **244** includes materials such as tetraethylorthosilicate (TEOS) oxide, un-doped silicate glass, or doped silicon oxide such as borophosphosilicate glass (BPSG), fused silica glass (FSG), phosphosilicate glass (PSG), boron doped silicon glass (BSG), and/or other suitable dielectric materials. In some embodiments, after the CESL **242** and the ILD layer **244** are deposited, a planarization process, such as a chemical mechanical planarization (CMP) operation, may be performed to form the dielectric structure **240** and to expose a top surface of the dummy gate structure **212** as shown in FIGS. **8**A to **8**D. In some embodiments, the planarization is performed to expose at least a top surface of the polysilicon layer of the dummy gate structure **212**.

[0039] Referring to FIGS. **9**A to **9**E, a portion of the dummy gate structure **212** is subsequently removed to form a first gate trench **218***a* in the dielectric structure **240** according to operation **112***a*. In some embodiments, a patterned protecting layer (not shown) is formed over the region **202***b*, and thus elements in the region **202***b* are protected and impervious to the formation of the first gate trench **218***a*. As shown in FIG. **9**C, the spacer **214** is exposed through sidewalls of the first gate trench **218***a*, and the first fin structure **210***a* is exposed through the first gate trench **218***a*. Subsequently, the liner layer **209** disposed over the first fin structure **209** is removed, and the semiconductor layers **206** are then removed. Accordingly, a plurality of nanowires **232**, which previously comprised the semiconductor layers **208**, are formed in the first gate trench **218***a* according to operation **114***a* of the method **10***a*, as shown in FIGS. **9**B and **9**C. Further, the plurality of nanowires **232** serving as channel regions are suspended in the first gate trench **218***a*. In some embodiments, the nanowires **232** can be slightly etched to obtain various desirable dimensions and shapes, and the various desired dimensions and shapes may be chosen based on device performance considerations. As shown in FIG. **9**C, the plurality of nanowires **232** and the inner spacers **211***a* are therefore exposed through the first gate trench **218***a*. The patterned protecting layer is then removed.

[0040] Referring to FIGS. **10**A to **10**E, another portion of the dummy gate structure **212** is then removed to form a second gate trench **218***b* in the dielectric structure **240** according to operation **112***b* of the method **10***b*. In some embodiments, another patterned protecting layer (not shown) is formed over the region **202***a*, and thus elements in the region **202***a* are protected and impervious to the formation of the second gate trench **218***b*. As shown in FIG. **10**C, the spacer **214** is exposed through sidewalls of the second gate trench **218***b*, and the second fin structure **210***b* is exposed through the second gate trench **218***b*. Subsequently, the liner layer **209** disposed over the second fin structure **210***b* is removed, and the semiconductor layers **208** are removed. Accordingly, a plurality of nanowires **234**, which previously comprised the semiconductor layers **206**, are formed in the second gate trench **218***b* according to operation **114***b* of the method **10***b*, as shown in FIGS. **10**B and **10**D. Further, the plurality of nanowires **234** serving as channel regions are suspended in the second gate trench **218***b*. In some embodiments, the nanowires **234** can be slightly etched to obtain various desirable dimensions and shapes, and the various desired dimensions and shapes may be chosen based on device performance considerations. As shown in FIG. **10**D, the plurality of nanowires **234** and the inner spacers **211***b* are therefore exposed through the second gate trench **218***b*. The patterned protecting layer is then removed. Additionally, the plurality of nanowires **230** and the plurality of nanowires **234**, both of which previously comprised the semiconductor layers **206**, include the same materials. Further, each of the nanowires **234** is coupled to each of the nanowires **230**, as shown in FIG. **10**D. In other words, each of the nanowires **234** is coupled to a corresponding nanowire **230**. In some embodiments, it is referred that the nanowires **230** and nanowires **234** are the same nanowires, as shown in FIG. **10**.

[0041] Referring to FIGS. **11**A to **11**E, an interfacial layer (IL) **252** is formed to surround each of the nanowires **232** exposed in the first gate trench **218***a* and each of the nanowires **234** exposed in the second gate trench **218***b*, as shown in FIG. **11**B. In some embodiments, the IL **252** may include an oxide-containing material such as SiO or SiON. After the forming of the IL **252**, a gate dielectric layer **254** is formed over the IL **252**. As shown in FIG. **11**B, the gate dielectric layer **254** surrounds each of the nanowires **232** and each of the nanowires **234**. In some embodiments, the gate dielectric layer **254** includes a high-k dielectric material having a high dielectric constant, for example, a dielectric constant greater than that of thermal silicon oxide (~3.9). The high-k dielectric material may include hafnium oxide (HfO_2), zirconium oxide (ZrO_2), lanthanum oxide (La_2O_3), aluminum oxide (Al_2O_3), titanium oxide (TiO_2), yttrium oxide (Y_2O_3), strontium titanate ($SrTiO_3$), hafnium oxynitride (HfO_xN_y), other suitable metal-oxides, or combinations thereof.

[0042] Still referring to FIGS. **11**A to **11**E, after the forming of the gate dielectric layer **254**, a first gate conductive layer **256***a* is disposed in the first gate trench **218***a* according to operation **114***a* of the method **10***a*, and a second gate conductive layer **256***b* is disposed in the second gate trench **218***b* according to operation **114***b* of the method **10***b*. The first and second gate conductive layers **256***a* and **256***b* are formed on the gate dielectric layer **254**. In some embodiments, the first gate conductive layer **256***a* is formed for an n-channel FET, and the second gate conductive layer **256***b* is formed for a p-channel FET. In some embodiments, the first gate conductive layer **256***a* can include at least a barrier metal layer (not shown) and a first work function layer, and the second gate conductive layer **256***b* can include at least a barrier metal layer (not shown) and a second work function metal layer. The barrier metal layer can include, for example but not limited to, TiN. The first work function metal layer, which provides proper work function to the n-channel FET, includes one or more of TaN, TaAlC, TiN, TiC, Co, TiAl, HfTi, TiSi and TaSi, but the disclosure is not limited thereto. The second work function metal layer, which provides proper work function to the p-channel FET, includes one or more of TiAlC, Al, TiAl, TaN, TaAlC, TiN, TiC and Co, but the disclosure is not limited thereto. Next, a gap-filling metal layer **258** is formed to fill the first gate trench **218***a* and the second gate trench **218***b*. The gap-filling metal layer **258** can include conductive material, such as Al, Cu, AlCu, or W, but is not limited to the above-mentioned materials. Accordingly, a first gate structure **250***a* is formed in the first gate trench **218***a*, and a second gate structure **250***b* is formed in the second gate trench **218***b*, as shown in FIGS. **11**A to **11**E.

[0043] Referring to FIGS. **12**A to **12**E, a patterned protecting layer **260** is then formed over the dielectric structure **240** and the first and second gate structures **250***a* and **250***b*. The patterned protecting layer **260** serves as an etching mask for the subsequent operations. Next, a portion of the dielectric layer **240** is removed through the patterned protecting layer **260**, and thus at least a first opening **262***a* is formed in the dielectric structure **240** according to operation **116***a* of the method **10***a*. Further, the first semiconductor layer **220***a* is exposed in a lower portion of the first opening **262***a* while the dielectric structure **240** and the spacers **214** are exposed in an upper portion of the first opening **262***a*, as shown in FIGS. **12**C and **12**E.

[0044] Referring to FIGS. **13**A to **13**E, a first metal silicide layer **270***a* is then formed over the first semiconductor layer **220***a* according to operation **118***a* of the method **10***a*. The first metal silicide layer **270***a* includes the first semiconductor material and a first metal material. In some embodiments, the first metal silicide layer **270***a* can be formed by depositing a metallic layer such as a TiN layer over the first semiconductor layer **220***a*. Next, a thermal operation is performed. Consequently, a portion of the first semiconductor layer **220***a* reacts with the metallic layer, and the first metal silicide layer **270***a* is formed. Therefore, the first metal silicide layer **270***a* can include $TiSi_x$, but the disclosure is not limited thereto. A thickness of the first semiconductor layer **220***a* is reduced to between approximately 5 nm and approximately 15 nm, but the disclosure is not limited thereto. Additionally, since the first metal silicide layer **270***a* is formed only over the first semiconductor layer **220***a*, the first metal silicide layer **270***a* is exposed in the lower portion of the first opening **262***a*, as shown in FIG. **13**C. In some embodiments, a glue layer **272** including TiN can be formed over the first metal silicide layer **270***a* and sidewalls of the upper portion of the first opening **262***a*. However, in other embodiments, the glue layer **272** can be omitted.

[0045] Referring to FIGS. **14**A to **14**E, a portion of the dielectric layer **240** is further removed to form at least a second opening **262***b* in the dielectric structure **240** according to operation **116***b* of the method **10***b*. Further, the second semiconductor layer **220***b* is exposed in a lower portion of the second opening **262***b* while the dielectric structure **240** and the spacers **214** are exposed in an upper portion of the second opening **262***b,* as shown in FIGS. **14**D and **14**E.

[0046] Referring to FIGS. **15**A to **15**E, a second metal silicide layer **270***b* is then formed over the second semiconductor layer **220***b* according to operation **118***b* of the method **10***b*. The second metal silicide layer **270***b* includes the first semiconductor material, the second semiconductor material, and a second metal material. In some embodiments, the second metal material of the second metal silicide layer **270***b* is different from the first metal material of the first metal silicide layer **270***a*. In some embodiments, the first metal silicide layer **270***a* includes $TiSi_x$, and the second metal silicide layer **270***b* includes $NiSiGe_x$, but the disclosure is not limited thereto. In some embodiment, a Ni layer is formed over the second semiconductor layer **220***b,* which is exposed in the lower portion of the second opening **262***b*, by suitable operation, such as chemical vapor deposition (CVD). Subsequently, anneal is performed such that Ni and SiGe are reacted and thus $NiSiGe_x$ silicide layer **270***b* is formed. The superfluous Ni layer is then removed. Additionally, since the second metal silicide layer **270***b* is formed only over the second semiconductor layer **220***b,* the second metal silicide layer **270***b* is exposed in the lower portion of the second opening **262***b,* as shown in FIG. **15**E. In some embodiments, a glue layer **272** including TiN can be formed over the second metal silicide layer **270***b* and sidewalls of the upper portion of the second opening **262***b*. However, in other embodiments, the glue layer **272** can be omitted. Additionally, because thermal budget of Ni is lower than that of Ti, the first metal silicide layer **270***a* is formed before forming the second opening **262***b* and the second metal silicide layer **270***b,* but the disclosure is not limited thereto.

[0047] Still referring to FIGS. **15**A to **15**E, a metal layer **264** is next disposed to fill the first opening **262***a* and the second opening **262***b* according to operation **120***a* of the method **10***a* and operation **120***b* of the method **10***b*. In some embodiments, the metal layer **264** includes low-resistivity metal material, such as tungsten (W), but the disclosure is not limited thereto. Accordingly, at least a first conductor, such as a first metal portion **280***a,* is formed in the first opening **262***a* and a second conductor, such as a second metal portion **280***b,* is formed in the second opening **262***b*. As shown in FIGS. **15**C and **15**D, a bottom and sidewalls of a lower portion of the first metal portion **280***a* in the first opening **262***a* are surrounded by the first silicide layer **270***a* while sidewalls of an upper portion of the first metal portion **280***a* in the first openings **262***a* are surrounded by the spacer **214** and patterned protecting layer **260**. Further, the bottom of the second metal portion **280***b* in the first opening **262***a* is lower than the plurality of nanowires **232**, as shown in FIG. **15**C. In contrast to the first metal portion **280***a,* a lower portion of the second metal portion **280***b* in the second openings **262***b* surrounds the second metal silicide layer **270***b,* as shown in FIGS. **15**D and **15**E.

[0048] Accordingly, a multi-gate semiconductor device **200***a* is obtained. As shown in FIG. **15**C, the multi-gate semiconductor device **200***a* includes the plurality of nanowires **232**, the first gate structure **250***a* over the plurality of nanowires **232**, and source/drain structures **282***a* and **284***a* at two ends of each nanowire **232**. The source/drain structures **282***a* and **284***a* include the first semiconductor layer **220***a,* the first metal portion **280***a,* and the first metal silicide layer **270***a* sandwiched between the first semiconductor layer **220***a* and the lower portion of the first metal portion **280***a.* Notably, a bottom surface of the first metal portion **280***a* is lower than the plurality of nanowires **232**, as shown in FIG. **15**C. Further, each of the first semiconductor layer **220***a* and the first metal silicide layer **270***a* substantially includes a U shape. Additionally, the first gate structure **250***a* can include a metal gate structure, but the disclosure is not limited thereto.

[0049] According to the multi-gate semiconductor device **200***a,* after the forming of the first semiconductor layer **220***a* and the first metal silicide layer **270***a,* there is still a space for forming the metal layer **264** in the first opening **262***a,* and thus the first metal portion **280***a* is obtained. Accordingly, the lower region of the first metal portion **280***a* can serve as a portion of the source/drain structures **282***a* and **284***a* while an upper region of the first metal portion **280***a* can serve as a contact plug for providing electrical connection between the source/drain structures **282***a* and **284***a* and other devices or circuits. More importantly, the first metal portion **280***a* can include low-resistivity metal material such as the aforementioned W, thereby reducing contact resistance.

[0050] In another embodiment, a multi-gate semiconductor device **200** is provided. The multi-gate semiconductor device **200** includes the multi-gate semiconductor structure **200***a* and a multi-gate semiconductor structure **200***b*. In some embodiments, the multi-gate semiconductor device **200** is a CMOS device, and the multi-gate semiconductor structure **200***a* is an n-channel FET and the multi-gate semiconductor structure **200***b* is a p-channel FET. As shown in FIGS. **15**A to **15**E, the multi-gate semiconductor device **200** includes the plurality of nanowires **232** serving as channel regions for the n-channel multi-gate semiconductor structure **200***a* and the plurality of nanowires **234** serving as channel regions for the p-channel multi-gate semiconductor structure **200***b*. The multi-gate semiconductor device **200** further includes the first gate structure **250***a* disposed over the plurality of nanowires **232**, the second gate structure **250***b* disposed over the plurality of nanowires **234**, the first source/drain structures **282***a* and **284***a* disposed at two ends of each nanowire **232**, and second source/drain structures **282***b* and **284***b* disposed at two ends of each nanowire **234**. It should be noted that the first source/drain structures **282***a* and **284***a* include a conductor such as the first metal portion **280***a,* the first semiconductor layer **220***a* disposed around sidewalls and a bottom of the lower portion of the first metal portion **280***a,* and the first metal silicide layer **270***a* disposed between the lower portion of the first metal portion **280***a* and the first semiconductor layer **220***a.* The second source/drain structures **282***b* and **284***b* include the plurality of nanowires **230**, the second metal silicide layer **270***b* disposed over the plurality of nanowires **230**, and the second semiconductor layer **220***b* disposed between the second metal silicide layer **270***b* and the plurality of nanowires **230**. Further, the nanowires **230** and the nanowires **234** are the same nanowires. It is referred that a portion of each nanowire surrounded by the second gate structure **250***b* serve as channel regions and are referred to as a first portion **234**, while another portion of each nanowire adjacent to and on opposing sides of the channel region form a part of the second sour/drain structures **282***b* and **284***b* and are referred to as a second portion **230**.

[0051] As mentioned above, the first metal silicide layer **270***a* and the second metal silicide layer **270***b* can include different semiconductor materials and different metal materials. In some embodiments, the first metal silicide layer **270***a* includes TiSi while the second metal silicide layer **270***b* includes NiSiGe. It should be noted that for the n-channel multi-gate semiconductor structure **200***a,* the contact resistance is reduced by forming the low-resistivity first metal portion **280***a* having the bottom surface lower than the plurality of nanowires **232**. For the p-channel multi-gate semiconductor structure **200***b,* the contact resistance is reduced by forming the Ni-silicide layer, because Ni resistance is lower than Ti resistance. Accordingly, the contact resistance of the multi-gate semiconductor device **200** is reduced by the dual contact formation.

[0052] FIGS. **16**A and **17**A illustrate a multi-gate semiconductor device **200'** at various fabrication stages constructed according to aspects of one or more embodiments of the present disclosure. FIGS. **16**B and FIG. **17**B are cross-sectional views taken along line I-I' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure, FIGS. **16**C and **17**C are cross-sectional views taken along line II-II' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure, FIGS. **16**D and **17**D are cross-sectional views taken along line III-III' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure, and FIGS. **16**E and **17**E are cross-sectional views taken along line IV-IV' of FIGS. **16**A and **17**A, respectively, according to aspects of one or more embodiments of the present disclosure. It should be noted that similar elements in FIGS. **3**A to **15**E and FIGS. **16**A to **17**E are designated by the same numerals. Further, similar elements in FIGS. **3**A to **15**E and FIGS. **16**A to **17**E can include similar materials and can be formed by similar steps; therefore such redundant details are omitted in the interest of brevity.

[0053] Please refer to FIGS. **16**A to **16**E. In some embodiments, operations **102**, **104**, **106***a* and **108***a,* **106***b* and **108***b,* **110**, **112***a* and **114***a,* and **112***b* and **114***b* are performed, and operations **116***a* and **116***b* are simultaneously performed after the forming of the first and second gate structures **250***a* and **250***b.* Consequently, a first opening **262***a* and a second opening **262***b* are simultaneously formed in the dielectric layer **240**. As shown in FIGS. **16**A to **16**E, the first semiconductor layer **220***a* is exposed in the first opening **262***a* and the second semiconductor layer **220***b* is exposed in the second opening **262***b*. In some embodiments, the first semiconductor layer **220***a* forms a bottom and sidewalls of a lower portion of the first opening **262***a* while the second semiconductor layer **220***b* protrudes from a bottom of the second opening **262***b,* as shown in FIGS. **16**C and **16**E.

[0054] Referring to FIGS. **17**A to **17**E, a first metal silicide layer **270***a*' is formed over the first semiconductor layer **220***a* and a second metal silicide layer **270***b*' is formed over the second semiconductor layer **220***b* according to operations **118***a* and **118***b*. Notably, the operations **118***a* and **118***b* are performed at the same time, and thus the first metal silicide layer **270***a*' and the second metal silicide layer **270***b*' are simultaneously formed. The first metal silicide layer **270***a*' includes the first semiconductor material and a first metal material, and the second metal silicide layer **270***b*' includes the first semiconductor material, the second semiconductor material and a second metal material. Notably, the first metal material and the second metal material are the same. In some embodiments, the first metal silicide layer **270***a*' includes TiSi, and the second metal silicide layer **270***b*' includes TiSiGe, but the disclosure is not limited thereto.

[0055] Still referring to FIGS. **17**A to **17**E, a glue layer such as a TiN layer is then formed over the first metal silicide layer **270***a*', the second metal silicide layer **270***b*', sidewalls of an upper portion of the first opening **262***a,* and sidewalls of an upper portion of the second opening **262***b*. However, in some embodiments, formation of the glue layer can be omitted. Subsequently, a metal layer **264** is formed to fill the first opening **262***a* and the second opening **262***b* according to operation **120**.

[0056] Accordingly, a multi-gate semiconductor device **200'** is provided. The multi-gate semiconductor device **200'** includes the multi-gate semiconductor structure **200***a*' and a multi-gate semiconductor structure **200***b*'. In some embodiments, the multi-gate semiconductor device **200'** is a CMOS device, the multi-gate semiconductor structure **200***a*' is an n-channel FET, and the multi-gate semiconductor structure **200***b*' is a p-channel FET. As shown in FIGS. **17**A to **17**E, the multi-gate semiconductor device **200'** includes the plurality of nanowires **232** serving as channel regions for the n-channel multi-gate semiconductor structure **200***a*' and the plurality of nanowires **234** serving as channel regions for the p-channel multi-gate semiconductor structure **200***b*'. The multi-gate semiconductor device **200'** further includes the first gate structure **250***a* disposed over the plurality of nanowires **232**, the second gate structure **250***b* disposed over the plurality of nanowires **234**, the first source/drain structures **282***a* and **284***a* disposed at two ends of each nanowire **232**, and the second source/drain structures **282***b* and **284***b* disposed at two ends of each nanowire **234**. It should be noted that the first source/drain structures **282***a* and **284***a* include the first conductor such as the first metal portion **280***a,* the first semiconductor layer **220***a* disposed around sidewalls and a bottom of the lower portion of the first metal portion **280***a,* and the first metal silicide layer **270***a*' disposed between the lower portion of the first metal portion **280***a* and the first semiconductor layer **220***a.* The second source/drain structures **282***b* and **284***b* include the plurality of nanowires **230**, the second metal silicide layer **270***b*' disposed over the plurality of nanowires **230**, and the second semiconductor layer **220***b* disposed between the second metal silicide layer **270***b*' and the plurality of nanowires **230**. Further, the nanowires **230** and the nanowires **234** are the same nanowires. It is referred that a portion of each nanowire surrounded by the second gate structure **250***b* serve as channel regions and are referred to as a first portion **234**, while another portion of each nanowire adjacent to and on opposing sides of the channel region form a part of the second sour/drain structures **282***b* and **284***b* and are referred to as a second portion **230**.

[0057] As mentioned above, the first metal silicide layer **270***a*' and the second metal silicide layer **270***b*' can include different semiconductor materials but the same metal materials. In some embodiments, the first metal silicide layer **270***a*' includes TiSi while the second metal silicide layer **270***b*' includes TiSiGe. It should be noted that for the n-channel multi-gate semiconductor structure **200***a*', the contact resistance is reduced by forming the low-resistivity first metal portion **280***a.* However, by simultaneously forming the first opening **262***a* and the second opening **262***b* and simultaneously forming the first metal silicide layer **270***a*' and the second metal silicide layer **270***b*', the methods **10***a* and **10**b are integrated and simplified while contact resistance of the multi-gate semiconductor device **200'** is reduced.

[0058] Embodiments for semiconductor structures and method for manufacturing the same may be provided. The semiconductor structure may include nanowire structures, a gate structure formed around the nanowire structures, a source/drain structure, and a contact plug. The contact plug may extend below the top surface of the nanostructures, so that the contact plug is partially surrounded by the source/drain structure and therefore has a larger contact area with the source/drain structure.

[0059] In some embodiments, a semiconductor structure is provided. The semiconductor structure includes a substrate and first nanostructures and second nanostructures formed over the substrate. The semiconductor structure further includes a first source/drain structure formed adjacent to the first nanostructures and a second source/drain structure formed adjacent to the second nanostructures. The semiconductor structure further includes a first contact plug formed over the first source/drain structure and a second contact plug formed over the second source/drain structure. In addition, a bottom portion of the first contact plug is lower than a bottom portion of the first nanostructures, and a bottom portion of the second contact plug is higher than a top portion of the second nanostructures.

[0060] In some embodiments, a semiconductor structure is provided. The semiconductor structure includes a substrate and first nanostructures and second nanostructures formed over the substrate. The semiconductor structure further includes a first gate structure surrounding the first nanostructure and a second gate structure surrounding first portions of the second nanostructures and a first source/drain semiconductor layer formed adjacent to the first gate structure. The semiconductor structure further includes a second source/drain semiconductor layer surrounding second portions of the second nanostructures and a first contact plug formed over the first source/drain semiconductor layer. The semiconductor structure further includes a second contact plug formed over the second source/drain semiconductor layer. In addition, the first contact plug extends below a topmost surface of the first nanostructures.

[0061] In some embodiments, a method for forming a semiconductor structure is provided. The method includes alternately stacking first semiconductor layers and second semiconductor layers over a substrate and patterning the first semiconductor layers and the second semiconductor layers to form a fin structure. The method further includes recessing the fin structure to form a recess and conformally forming a source/drain semiconductor layer over the recess. The method further includes filling the recess by a conductive material to form a contact plug over the source/drain semiconductor layer.

[0062] In some embodiments, a method for forming a semiconductor structure is provided. The method includes forming a fin structure over a substrate, and the fin structure includes first semiconductor layers and second semiconductor layers alternately stacked. The method further includes removing a portion of the fin structure to form a recess in a first source/drain region and forming a source/drain semiconductor layer in the recess. The method further includes forming a silicide layer over the source/drain semiconductor layer in the recess and forming a contact plug over the silicide layer in the recess. In addition, the source/drain semiconductor layer extends between the silicide layer and the first semiconductor layers.

[0063] In some embodiments, a method for forming a semiconductor structure is provided. The method includes alternately stacking first semiconductor layers and second semiconductor layers over a substrate and patterning the first semiconductor layers and the second semiconductor layers to form a first fin structure and a second fin structure. The method further includes recessing the first fin structure in a first source/drain region to form a first recess and forming a first source/drain semiconductor layer over the first recess. The method further includes removing the first semiconductor layers of the second fin structure in a second source/drain region to form gaps between the second semiconductor layers of the second fin structure in the second source/drain region and filling the gaps between second semiconductor layers in the second source/drain region by a second source/drain semiconductor layer. The method further includes filling the gaps between second semiconductor layers in the second source/drain region by a second source/drain semiconductor layer and filling the first recess by a conductive material to form a first contact plug over the first source/drain semiconductor layer.

[0064] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method for manufacturing a semiconductor structure, comprising:

alternately stacking first semiconductor layers and second semiconductor layers over a substrate;

patterning the first semiconductor layers and the second semiconductor layers to form a fin structure;

recessing the fin structure to form a recess;

conformally forming a source/drain semiconductor layer over the recess; and

filling the recess by a conductive material to form a contact plug over the source/drain semiconductor layer.

2. The method for manufacturing the semiconductor structure as claimed in claim **1**, wherein a bottom portion of the contact plug is lower than a bottom portion of a topmost layer of the first semiconductor layers.

3. The method for manufacturing the semiconductor structure as claimed in claim **2**, wherein the bottom portion of the contact plug is lower than a bottom portion of a bottommost layer of the first semiconductor layers.

4. The method for manufacturing the semiconductor structure as claimed in claim **1**, further comprising:

removing the second semiconductor layers; and

forming a gate structure wrapping around the first semiconductor layers.

5. The method for manufacturing the semiconductor structure as claimed in claim **4**, wherein a bottom portion of the contact plug is lower than a bottom portion of the gate structure.

6. The method for manufacturing the semiconductor structure as claimed in claim **5**, wherein a top surface of the contact plug is higher than a top surface of the gate structure.

7. The method for manufacturing the semiconductor structure as claimed in claim **1**, further comprising:

forming a silicide layer over the source/drain semiconductor layer,

wherein the source/drain semiconductor layer is sandwiched between the silicide layer and the first semiconductor layers.

8. The method for manufacturing the semiconductor structure as claimed in claim **1**, wherein the source/drain semiconductor layer has a wavy sidewall.

9. A method for manufacturing a semiconductor structure, comprising:

forming a fin structure over a substrate, wherein the fin structure comprises first semiconductor layers and second semiconductor layers alternately stacked;

removing a portion of the fin structure to form a recess in a first source/drain region;

forming a source/drain semiconductor layer in the recess;

forming a silicide layer over the source/drain semiconductor layer in the recess; and

forming a contact plug over the silicide layer in the recess,

wherein the source/drain semiconductor layer extends between the silicide layer and the first semiconductor layers.

10. The method for manufacturing the semiconductor structure as claimed in claim **9**, further comprising:

removing portions of the second semiconductor layers of the fin structure exposed by the recess to form notches between the first semiconductor layers of the fin structure; and

forming inner spacers in the notches,

wherein the inner spacers have curved sidewalls.

11. The method for manufacturing the semiconductor structure as claimed in claim **10**, wherein the source/drain semiconductor layer further extends between the silicide layer and the inner spacers.

12. The method for manufacturing the semiconductor structure as claimed in claim **9**, further comprising:

filling the recess by a dielectric layer before forming the silicide layer;

removing the second semiconductor layers of the fin structure in a gate region to expose the first semiconductor layers of the fin structure; and

forming a gate structure around the first semiconductor layers.

13. The method for manufacturing the semiconductor structure as claimed in claim **12**, wherein a bottom portion of the silicide layer is lower than a bottom surface of the gate structure.

14. The method for manufacturing the semiconductor structure as claimed in claim **12**, further comprising:

forming a contact opening through the dielectric layer in the source/drain region to expose the source/drain semiconductor layer,

wherein a bottom portion of the contact opening is lower than the first semiconductor layers.

15. A method for manufacturing a semiconductor structure, comprising:

alternately stacking first semiconductor layers and second semiconductor layers over a substrate;

patterning the first semiconductor layers and the second semiconductor layers to form a first fin structure and a second fin structure;

recessing the first fin structure in a first source/drain region to form a first recess;

forming a first source/drain semiconductor layer over the first recess;

removing the first semiconductor layers of the second fin structure in a second source/drain region to form gaps between the second semiconductor layers of the second fin structure in the second source/drain region;

filling the gaps between second semiconductor layers in the second source/drain region by a second source/drain semiconductor layer; and

forming a first contact plug over the first source/drain semiconductor layer.

16. The method for manufacturing the semiconductor structure as claimed in claim **15**, further comprising:

forming a second contact plug over the second source/drain semiconductor layer, wherein the first contact plug and the second contact plug have different shapes.

17. The method for manufacturing the semiconductor structure as claimed in claim **15**, further comprising:

removing the second semiconductor layers of the first fin structure in a first channel region to form first nanostructures;

forming a first gate structure surrounding the first nanostructures;

removing the first semiconductor layers of the second fin structure in a second channel region to form second nanostructures; and

forming a second gate structure surrounding the second nanostructures.

18. The method for manufacturing the semiconductor structure as claimed in claim **17**, further comprising:

forming a first silicide layer over the first source/drain semiconductor layer, wherein the first silicide layer extends below the first nanostructures.

19. The method for manufacturing the semiconductor structure as claimed in claim **18**, further comprising:

forming a second silicide layer over the second source/drain semiconductor layer, wherein a bottom portion of the second silicide layer is higher than a bottom portion of the first silicide layer.

20. The method for manufacturing the semiconductor structure as claimed in claim **15**, further comprising:

forming a dielectric layer over the first source/drain semiconductor layer to fill in the first recess in the first source/drain region before removing the first semiconductor layers of the second fin structure in the second source/drain region;

removing the second semiconductor layers of the first fin structure in a channel region to form first nanostructures;

forming a first gate structure surrounding the first nanostructures; and

removing the dielectric layer in the first recess to expose the first source/drain semiconductor layer.

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