[54] **R. F. REMOTE CONTROLLER FOR ELECTRICAL LOADS HAVING RESISTIVE OR COMPLEX IMPEDANCES**

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[57] **ABSTRACT**

Apparatus and method for remotely controlling electrical loads having resistive or complex impedances. The apparatus features a controller having a transmitter and a companion receiver. The transmitter is preferably hand-held and includes a command generator at which commands are selected; a modulator responsive to the command signals for generating modulation signals containing the load control information; an oscillator responsive to the modulation signals for generation short-duration bursts of r.f. carrier whose positions in time convey the load control information; and an antenna for radiating the modulated, r.f. carrier. The receiver includes an antenna responsive to the transmitter; a detector responsive to the receiver antenna for generating signals corresponding to the transmitter modulation signals; a converter responsive to the detector signals for changing the detector signals to a form convenient for processing; a decoder responsive to the converter for generating load control signals; and a driver connected to the loads and responsive to the control signals for implementing the commands selected at the transmitter. The method includes steps for generating command signals including control data; generating short-duration modulation signals in response to the command signals; varying the amplitude of an r.f. carrier with the modulation signal to generate bursts of r.f. carrier having positions in time that convey the load control information and, thereafter, radiating the r.f. carrier. Additionally the method includes steps for receiving the modulated carrier; demodulating the carrier; converting the detector signal for processing; decoding the load control information; and generating load control signals for driving the loads.
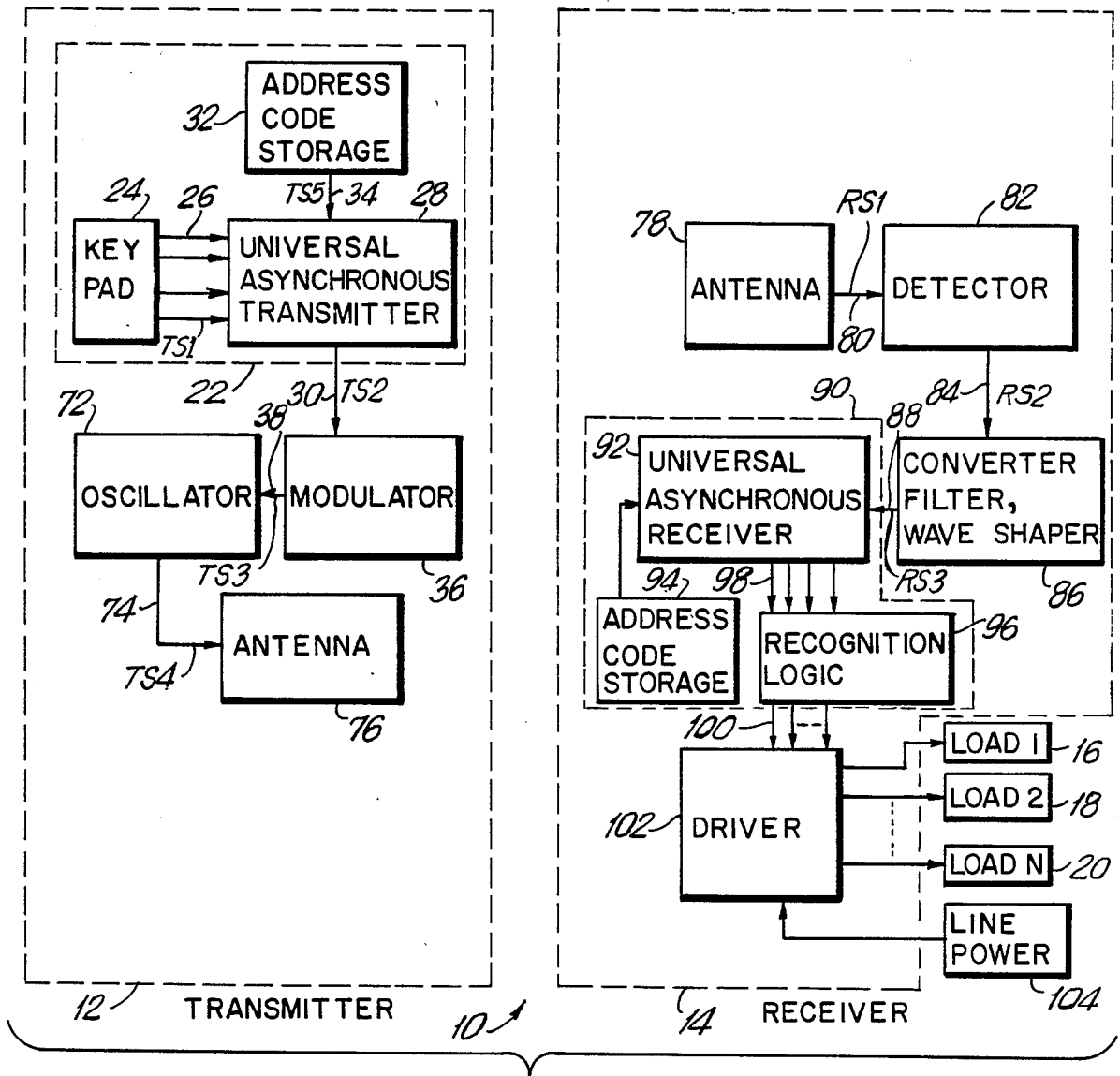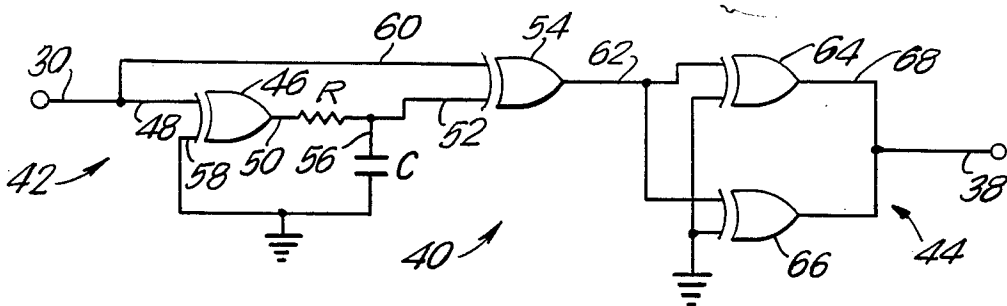
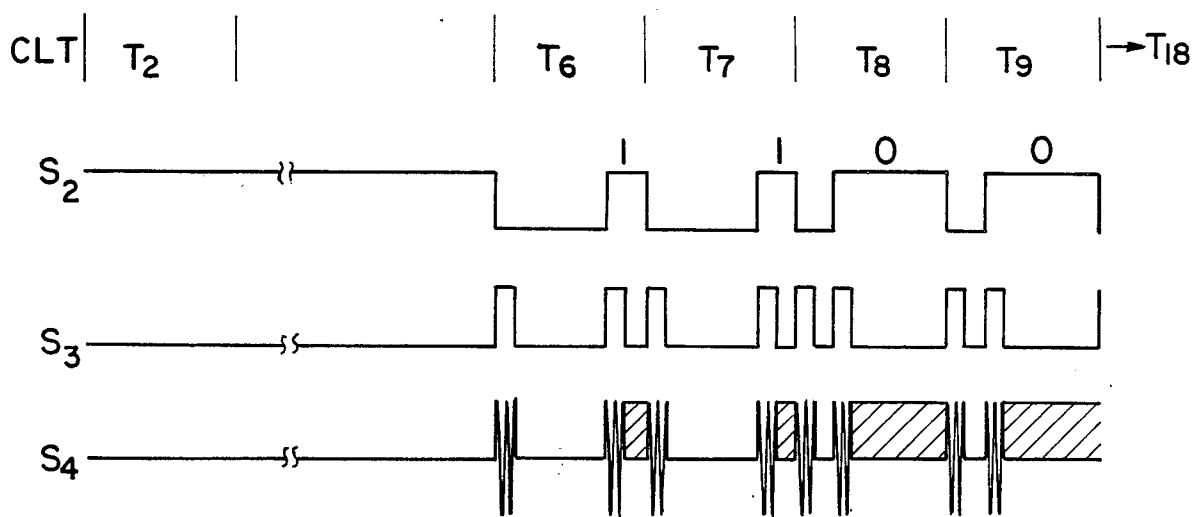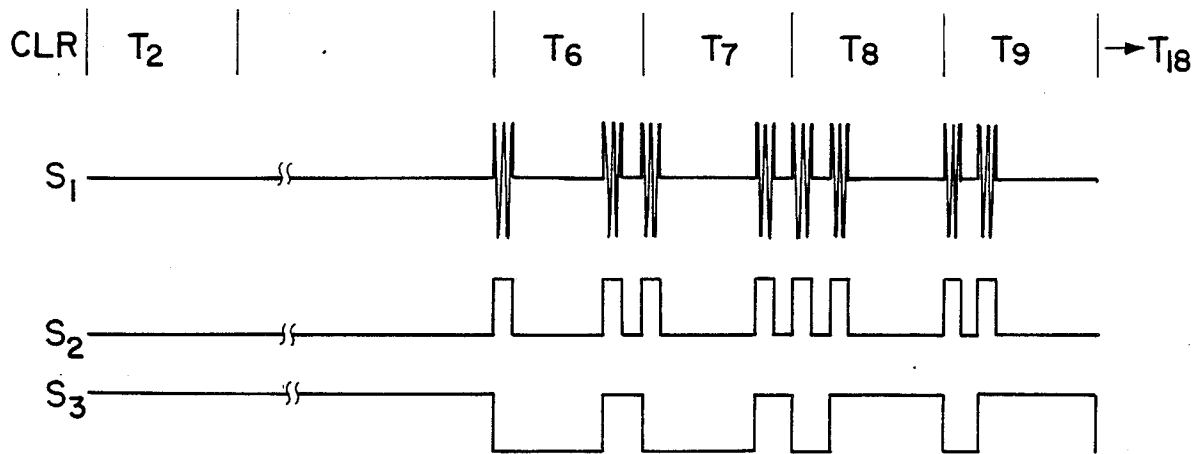**36 Claims, 4 Drawing Sheets**
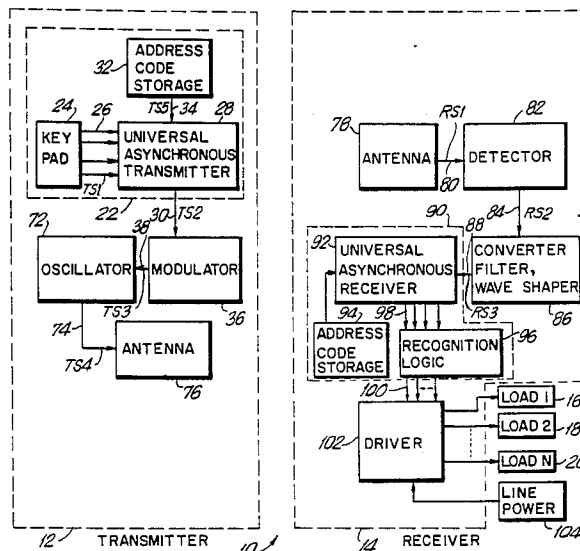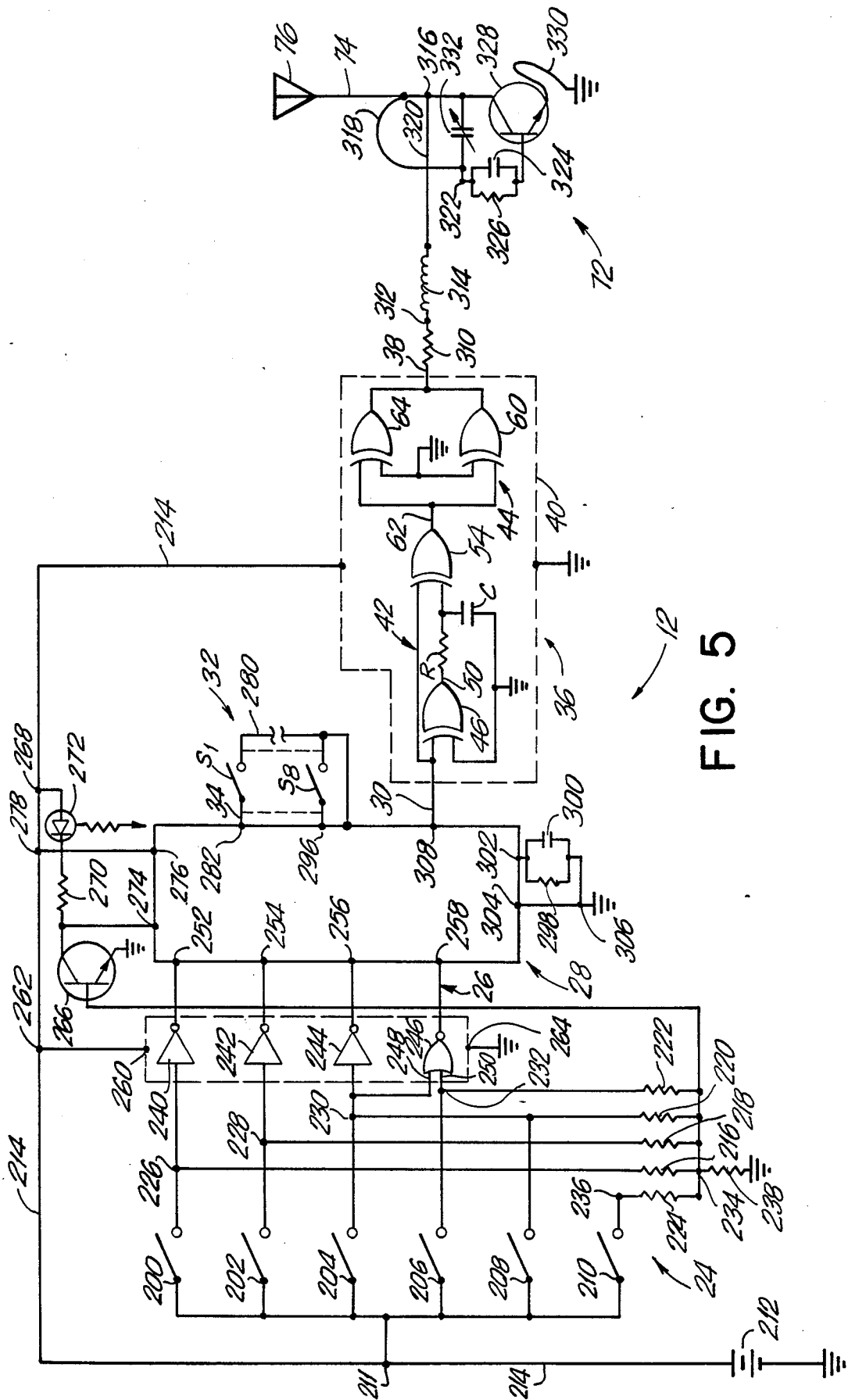
FIG. 1

FIG. 4

FIG.2

FIG.3

FIG. 5

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1

R. F. REMOTE CONTROLLER FOR ELECTRICAL LOADS HAVING RESISTIVE OR COMPLEX IMPEDANCES

BACKGROUND OF THE INVENTION

1. Field of The Invention

This invention concerns the remote control of appliances, such as ceiling fans, and/or associated lighting by transmission and reception of radio frequency signals containing control information, and more particularly a radio frequency, remote controller featuring pulsed bursts of r.f. carrier signal, wherein the position of the pulses in time convey the information for controlling the fan and/or associated lighting.

2. Description of Related Art

The remote control of business and home appliances, particularly ceiling fans and companion lighting, has become increasingly more popular. Such features as variable fan speed, fan reversibility, light intensity adjustment, and decorative appearance have made the ceiling fan and companion light a sought after addition to households and work environments. Further, these popular features have been made even more attractive with the advent of controllers that permit the user to vary the fan and light functions at a distance and without the need for manipulating a pull chain or string unattractively hanging from the fan or light.

However, there have been drawbacks associated with certain forms of remote control. For example, remote control by infrared or ultrasound suffer from "line-of-sight" limitation. Particularly, these forms experience signal interruption in the presence of physical obstructions such as walls, floors, etcetera, or even the blades of the fan itself. Additionally, these approaches are susceptible to interference from "noise", e.g., background light and sound, which may cause false control of the system.

Still further, the technique of power-current modulation, while referred to as remote control, is only a "qualified" form, in that it requires fixed mounting of the controller to the fan and lamp power circuits. As a result of the required fixed mounting, typically in a wall, the controller is rendered immovable, limiting flexibility of use and making the installation awkward and more expensive, and thus, less attractive.

On the other hand, however, remote control of appliances such as ceiling fans and associated lighting has been effectively accomplished with radio frequency (r.f.) signals. Physical objects such as walls, floors, and the like, while obstructions to light and sound forms of remote control, are transparent to r.f. signals. Further, an r.f. transmitter can be easily carried and manipulated by hand thereby permitting the operator freedom of use.

While r.f. controllers for combined ceiling fan and lighting fixtures have been known, problems have existed with them. For example, certain designs have been elaborate and complicated raising questions of cost and reliability. As an illustration, U.S. Pat. No. 4,538,973, issued Sept. 3, 1985, to Angott et al. describes an r.f. controller having a transmitter and receiver for controlling the fan motor and lighting circuits of a combined ceiling fan and light. However, in accordance with the Angott et al. design, the pulse counting technique proposed for processing the control data requires use of separate channels and frequencies to manage fan operation and light intensity. Accordingly, this multiplication

2

of channels and frequencies results in an increase in system complexity and duplication of system components. As will be appreciated, increased complexity and component duplication raise cost and reduce reliability; results which are commercially unattractive.

Controllers, however, have been developed which permit control of multiple fan features as well as operation of associated lighting, with a single frequency and channel. MEDCO, Ltd. of Deer Park, N.Y., has offered a fan and light controller of digital designs which features a pulse-width modulation scheme in a single-channel system. The Medco controller permits control of fan activation, speed selection and direction as well as the intensity of associated lighting with a single modulated r.f. carrier signal.

Even in single-channel systems of the type offered by MEDCO, Ltd., however, difficulties remain. Particularly, in order to stay price competitive, the system component costs must be kept low. But, where component costs are cut, as for example, where a low-cost detector such as one of the superregenerative type is used in the receiver, system sensitivity is reduced. And, where receiver sensitivity is reduced, the distance the transmitter can be spaced from the receiver and still maintain control; i.e., system range, is, likewise, reduced. Unfortunately, the effect of reducing system range may be to prevent use of the remote controller in those applications where it can be particularly attractive; for example, large rooms or high ceilings commonly found in commercial or industrial buildings, or from adjoining rooms or outside residential structures.

More specifically, to satisfy the requirements of current and anticipated remote control applications, it has been found desirable to maintain system range at between 50 to 100 feet; a range which discourages use of low-sensitivity, low-cost systems. Moreover, simply increasing transmitter power to compensate for reduced receiver sensitivity may not be possible. The Federal Communications Commission (F.C.C.) maintains and enforces strict limits on the average signal power allowed to be transmitted by an r.f. remote control transmitter. This is done to avoid injury and inconvenience which may result from r.f. energy transmissions. As is well known, r.f. energy can cause skin burns, eye damage and disrupt heart pacers, as well as interfere with services such as television and telephone.

SUMMARY OF INVENTION

Accordingly, it is an object of this invention to provide an r.f. controller of simple design and low cost, capable of remotely controlling electrical loads having resistive or complex impedances.

It is a yet further object of this invention to provide an r.f. controller capable of remotely controlling activation, speed and direction of a fan and the intensity of an associated light using a single transmission frequency.

It is yet another object of this invention to provide an r.f. controller having commercially desirable range.

It is yet a further object of this invention to provide an r.f. controller that has improved system controlability with reduced average transmission power.

It is a still further object of this invention to provide an r.f. controller that has increased resistance to spurious control signals which may arise from background noise.

Briefly, the controller of this invention features use of a transmitter capable of transmitting short, pulsed bursts

of r.f. signals, wherein the position of the pulses in time communicate the load control information. With this approach, the average power of the r.f. transmission can be reduced in order to stay within F.C.C. limits, while, at the same time, permitting the peak power of the transmission to be increased so that inexpensive, low-sensitivity receivers, spaced at commercially attractive distances from the transmitter, can be used.

Additionally, in preferred form, the controller features a receiver capable of filtering the load command signals received to pass only signals conforming to the anticipated wave shape of valid command signals. This enables the controller to reject noise and other spurious signals, such as auto ignition pulses and radiation from appliance motors, etcetera, which may look to the receiver like command signals.

In preferred form, the controller of this invention includes a transmitter having a command generator which generates coded command signals for controlling the electrical loads. The coded command signals are sequences of pulses having modulated widths that communicate the load control data. In preferred form, the command generator includes a command selector, such as a key pad, that may be hand-held by an operator for the selection of load commands. Additionally, the command generator includes universal asynchronous transmitter circuits responsive to the command selector for generating the coded command signals. In this arrangement, the command selector supplies multibit, parallel, digital, data words containing the selected load control information to the universal asynchronous circuits. The universal asynchronous circuits in response generate a sequence of serial, pulse-width modulated pulses that constitute the coded command signals.

Further, the transmitter includes a modulator which generates signals for modulating the amplitude of an r.f. oscillator also included in the transmitter. In accordance with the invention, the modulator, in response to the command generator signals, generates short-duration pulses at the leading and trailing edges of the command signal pulses. In turn, the pulses of the modulator activate the r.f. oscillator. During the time between the modulation signal pulses, the oscillator is maintained off. The transmitter also includes an antenna coupled to the oscillator for radiating the modulated r.f. oscillator signals.

The controller further includes a receiver located at or proximate the electrical load to be controlled, which, typically, is spaced from the transmitter. In preferred form, the receiver includes an antenna which picks up the transmitted, r.f. signals and passes them along in the form of receiver antenna signals to the other elements of the receiver.

In accordance with the invention, the receiver also includes a detector connected to the antenna and responsive to the receiver antenna signals for demodulating the antenna signal and producing detector signals corresponding to the transmitter modulation signals; particularly, a series of short-duration pulses positioned in time at approximately the leading and trailing edges of the transmitter command signal pulses.

While the detector signals may immediately be decoded to drive the loads in accordance with the control information, in preferred form, the receiver includes a converter responsive to the detector signals for producing a sequence of pulse-width modulated pulses that correspond to the transmitter command signals. In preferred form, the converter may also include a signal filter designed to anticipate the form of the transmitter modulator signals and pass only detector pulses of a width and position in time within the range permissible for the modulator signals. Additionally, in preferred form, the receiver convertor includes a wave shaper responsive to the detector signals to form them into uniform, rectangular pulses.

In accordance with this approach, the converter includes a signal transformer responsive to the filtered and shaped detector signals for generating the pulse-width modulated pulses corresponding to the command signals of the transmitter. In preferred form, the transformer can be a flip-flop.

Continuing, the receiver also includes a decoder responsive to the detector signals, or in preferred form, the converter signals for producing load control signals. Preferably, the decoder includes universal asynchronous receiver circuits which are responsive to the sequence of pulse-width modulated pulses of the converter for generating multibit, parallel, digital data words containing the control data of the command signals.

In accordance with the invention, the receiver also includes a load driver responsive to the decoder load-control signals for driving the loads in accordance with the command signals initiated by the user at the command selector, e.g., the key pad.

In preferred form, the transmitter command generator may include address storage elements capable of storing and reproducing receiver address information for inclusion in the command signals. Additionally, address storage elements and comparator means may be provided at the receiver decoder to permit only control data which is intended for the loads to be processed by the receiver. The address information permits the transmitter and receiver to be matched so that transmitter signals will be processed only by the companion receiver and, thereby, control only loads associated with the companion receiver.

In addition to the controller briefly described above, this invention also embraces a method for remotely controlling one or more electrical loads having resistive or complex impedances.

In accordance with the invention, a preferred form of the method includes the generating of coded load command signals containing load control data in the form of sequences of pulse-width modulated pulses. Thereafter, the method includes generating modulation signals in the form of pulses whose position in time correspond to the leading and trailing edges of the pulse-width modulated command signals. Next, the modulation signals are used to modulate the amplitude of an r.f. oscillator to create controlled bursts of r.f. signals at predetermined points in time. In preferred form, the modulation signals activate the r.f. oscillator during the modulation signal pulses and deactivate the r.f. oscillator between the pulses of the modulation signals, the duration of the pulses being many times longer than the period of the r.f. oscillator signals. Following modulation, the r.f. signals containing the load control information are radiated.

In accordance with the method of the invention, following radiation of the modulated r.f. signals, the signals are received proximate the loads to be controlled; for example a fan and associated lighting. Thereafter, the r.f. signals are demodulated and detection signals produced having pulses whose position in time correspond to the modulation pulses.

5

Next, the detection signals may be decoded and, thereafter, used to drive the loads in accordance with the command signals. However, in preferred form, detection signals are filtered to pass only detection pulses having a width and position in time within the range predetermined for the modulation signals. Modulation signal pulses not within the anticipated range are rejected as noise. Subsequently, the filtered detection signal pulses are shaped to give them a substantially uniform, rectangular shape.

In preferred form, following filtering and shaping, the detection signals, are converted to sequences of pulses whose widths are set to approximate the time between the pulses of the detection signals. The converted detection signals created in this fashion correspond to the coded command signals.

Next, the converted detection signals are decoded to generate the load control signals. Particularly, the pulse-width modulated, serial, data pulses of the converted detection signals are further converted to multi-bit, parallel, digital, data words containing the control information. The parallel, digital, data words contain the appropriate data to both identify the particular receiver and load to be controlled and the data to implement the control command originally selected.

DESCRIPTION OF THE DRAWINGS

The above and further objects, features and advantages of the invention will become clear from the following more detailed description read with reference to the accompanying drawings in which:

FIG. 1 is a block diagram of the r.f. controller and the loads to be controlled in accordance with the invention.

FIG. 2 is an illustration of portions of certain signals produced by the transmitter of the r.f. controller in accordance with this invention.

FIG. 3 is an illustration of portions of certain signals produced by the receiver of the r.f. controller in accordance with this invention.

FIG. 4 is a logic diagram of a signal transformer which may be used in the transmitter modulator of the r.f. controller in accordance with this invention.

FIG. 5 is a schematic diagram of the electrical circuitry associated with the transmitter of the r.f. controller in accordance with this invention.

FIG. 6 is a schematic diagram of the electrical circuitry associated with the receiver of the r.f. controller in accordance with this invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

A preferred embodiment of the controller in accordance with this invention is shown in block form in FIG. 1. With reference to FIG. 1, controller 10 includes a transmitter 12 and a receiver 14 for controlling a plurality of electrical loads 16, 18, 20. Although not shown for the sake of simplicity, receiver 14 is typically mounted displaced from transmitter 12 proximate loads 16, 18, 20. As shown, controller 10 is capable of controlling multiple loads, the maximum number being determined by the controller data structure and receiver configuration to be described more fully hereafter.

In accordance with the invention, the impedances of the loads to be controlled may be either purely resistive or complex; i.e., either resistive, inductive or capacitive, or have some combination of these components. More particularly, controller 10 is capable of controlling predominantly resistive loads such as heaters, predomi-

6

nantly inductive loads such as fan motors, or predominantly capacitive loads such as fluorescent lamps or loads that respond to power as if they were capacitive such as the tungsten filaments of incandescent lamps.

In the case of a ceiling fan and companion light, receiver 14 may be conveniently mounted in the fan housing connected to the fan motor and lighting circuits. In this arrangement, receiver 14 would be connected to control the turning on and off of the fan, its speed and direction, as well as the activation of the lamp and its light intensity. As will be appreciated by those skilled in the art, controller 10 could equally well be used to control the fan alone or the lighting alone, or a plurality of fans or plurality of lights.

Continuing with reference to FIG. 1, in use, transmitter 12 may be either hand-held or mounted at some convenient location. The maximum distance transmitter 12 may be separated from receiver 14 is determined by the controller range. Since controller 10 is of the r.f. type, physical obstructions such as walls and floors are transparent to the r.f. signals, and, accordingly, do not impede control if located between transmitter 12 and receiver 14. Accordingly, remote control of the loads may be conveniently effected form adjacent rooms or even outside the structure in which the loads are located.

As shown in FIG. 1, transmitter 12 includes a command generator 22 for generating coded load command signals TS2. More particularly, generator 22 includes a command selector 24, which in preferred form is a key pad.

As is well known in the art, key pad 24 may include a plurality of keys having identifying alphanumeric or symbolic indicia thereon. The keys are typically coupled to electrical circuitry within the pad for generating digital, data signals. Accordingly, when a key corresponding to a desired load command is depressed the user, a unique, multibit, parallel, digital, data word signal, TS1, representing the selected load control command appears at pad output lines 26.

In accordance with the design of controller 10, command selection signals TS1 are formulated to both uniquely identify the command chosen and to, additionally, provide the data required to control the load. This approach has the economy of avoiding later generation of load control data in response to the command selection signals. As is well known, a digital data word having N bits is capable of representing 2^N unique states. Command selection signals TS1 are, therefore, fashioned as multibit, digital, data words so that each state of a word can represent a separate command; for example, selection of a particular fan speed, fan direction, or lighting level, etc. Further, in addition to defining the particular command, the state of the selection signal also constitutes the binary coded data used to control the load; i.e., the command selection signals contain the coded load control information.

In preferred form, to control a basic ceiling fan and light combination, a 6-button, 6-data line pad is used. Further, for this arrangement, only 4 lines i.e., 4 data bits, are used to represent 6 basic commands; e.g., fan forward; fan reverse; high fan speed; medium fan speed; low fan speed; and light intensity incrementation. As will be appreciated, if additional commands are desired, additional keys, lines, and data bits may be used as required. Further, and as is known in art, the technique of multiplexing may also be used to increase the number of commands that may be supplied over the data lines.

7

For simplicity and economy, controllers 10, in accordance with the invention, features single-channel transmission of the control information to loads 16, 18, 20. Accordingly, the multi-line, parallel, digital, data originated by key pad 24, must be converted to single-line, serial, data word to facilitate transmission.

Additionally, because the form of digital data from key pad 24; i.e., amplitude modulated, is not well suited for broadcast, it also is converted prior to transmission. Particularly, signal pulses of varying amplitude from key pad 24 commonly used to represent the 1's and 0's of conventional digital data are susceptible to amplitude distortions during transmission. This distortion can create false 1's or 0's which has the effect of corrupting the data. Accordingly, it is more desirable to communicate pulses of a single amplitude, wherein the width of the pulses is varied to establish the data sequences of 1's and 0's. In this way, variations in the pulse amplitude which commonly occur during transmission are not as likely to confuse the data content represented in the pulse widths.

Universal asynchronous transmitter (UAT) 28 shown included in command generator 22 performs these functions and others. In a manner well known in the art, UAT 28 changes the parallel, digital, command signals, TS1, to serial, and converts the conventional amplitude varying digital signals of TS1 to pulse-width modulated, command signals, TS2.

Continuing, command generator 22 in preferred form also includes means for adding address code information to the command signals, TS2. The address information is supplied in order to uniquely identify the receiver and associated loads to be controlled. As explained, physical obstructions such as wall, floors and the like are transparent to r.f. signals. Additionally, several receivers may be located within a room arranged for control by separate transmitters. Therefore, to avoid unintended control of receivers and loads within the range of transmitter 12, address information specifically identifying the receiver and companion loads can be added to control signals TS2.

For this purpose, as shown in FIG. 1, command generator 22 is provided with an address storage means 32. Storage means 32 is adapted to supply digital data that uniquely identifies the receiver that is companion to transmitter 12. Storage means 32 can take any convenient forms; e.g., a DIP switch, ROM or the like. In preferred form, storage means 32 is an 8-line, DIP switch to permit simple, manual entry of any one of 256 unique receiver addresses.

Still further command generator 22 may include elements for adjusting the repetition rate and nominal pulse width, as well as adding synchronization and start recognition bits to command signals TS2. In preferred form, the pulse-width modulated data words that constitute command signals TS2 are 18 bits in length. They include 5 synchronization bits, 8 receiver address bits, 4 load command bits and 1 start bit.

In the past, once command signals TS2 were generated, they were used to modulate an r.f. carrier which was, thereafter, broadcast to the receiver. However, as noted above, by providing the carrier signal with a modulation envelope corresponding to the pulse-width modulated command signals TS2, average power was added to the r.f. transmission which limited the extent to which the r.f. carrier amplitude could be increased. This, in turn, limited the amount of power that could be added to the transmission to compensate for reduced

8

receiver sensitivity resulting from use of a low-cost superregenerative detector.

In accordance with this invention, rather than use command signals TS2 to modulate the r.f. carrier, special modulations signals are generated which have substantially reduced widths as compared with the command signals, but which retain the receiver address and load control data of the command signals.

More particularly, the narrow-width, special modulation pulses are generated such that their positions in time, rather than their widths, convey the address and load control data, the special modulation pulses being generated at the leading and trailing edges of the pulse-width modulated command signals TS2. In this way, the 1's and 0's of the address and load control data conveyed by the widths of the command signal pulses are transformed to the positions in time of the special modulation pulses, particularly, the difference in position of successive pulses. The narrow-width, modulation pulses can subsequently be used to modulate the r.f. carrier, and, thereby, substantially reduce the contribution to average transmission power that would otherwise result from use of the pulse-width modulated command signals. The advantage of this approach is that the amplitude of the carrier can be increased without exceeding F.C.C. limits on transmission power, and facilitate use of low-sensitivity receivers spaced at desirable distances form the transmitter.

In accordance with the invention, and as shown in FIG. 1, modulator 36 is connected to UAT 28 for this purpose. Particularly, modulator 36 includes a signal transformer responsive to the TS2 signals at UAT output 30 for generating the modulation pulses. As will be appreciated, the process of generating the modulation pulses in this fashion constitutes a differentiation of command signals TS2.

In preferred form, the modulator signal transformer is a compound exclusive OR gate, arranged to trigger on the leading and trailing edges of the pulse-width modulated command signals TS2.

As shown in FIG. 4 exclusive OR gate 40 includes a gate section 42 and a buffer section 44. Gate section 42 includes a first exclusive OR gate element 46 having a first input 48 coupled to UAT output 30. Further, the output 50 of gate element 46 is coupled to a first input 52 of a second exclusive OR gate element 54. First gate output 50 is connected to second gate input 52 through an RC network 56, at the resistor, capacitor node. The second input 58 of gate element 46, as shown, is also coupled to RC network 56, but, at the other side of capacitor C and to ground. Additionally, first input 48 of gate element 46 is coupled to second input 60 of gate element 54. Finally, the output 62 of gate element 54 is coupled to buffer section 44, which, as shown, includes third and fourth exclusive OR gate elements 64, 66, having their respective outputs 68, 70 coupled to the output 38 of modulator 36.

In operation, when pulse-width modulated command signal TS2 goes up (absolute value) at line 30, first input 48 of gate element 46 goes up. Further, since second input 58 of gate element 46 is tied to ground, the inputs to gate element 46 are 1 and 0 respectively. Therefore, output 50 of element 46 attempts to go up. However, output 50 is unable to rise until capacitor C of network 56 charges. Accordingly, first input 52 of gate element 54 initially remains low.

Continuing, since second input 60 of gate element 54 is tied to line 30, it, like first input 48 of gate element 46,

11

order to limit average transmission power to F.C.C. limits, while increasing peak power to achieve acceptable range with a low sensitivity detector. This waveshape, however, is similarly in appearance to "noise" generated by such sources as auto ignitions, lightning, electric motors and the like.

Accordingly, to reduce detector signals which result from noise, filtering means to exclude detector pulses not corresponding to the transmitted carrier envelope are preferably provided in receiver 14. In the preferred form, both high-pass and low-pass filter elements are provided in signal converter 86. The filter elements are selected to anticipate, respectively, the pulse width and pulse position which may be given to the carrier envelope; i.e., the range of forms for the transmitter modulation signals, and to pass only detector pulses having a pulse width and position within the permissible range.

Additionally, in preferred form, converter 86 includes pulse shaping means to provide the detector output pulse signals with a generally rectangular form. In this regard, it has been found convenient to formulate the wave shaper as an operational amplifier having two inputs, to one of which the detector pulses are provided and to the other of which a constant reference potential is provided. This arrangement enables the operational amplifier to produce a predetermined output amplitude (pulse height) for the period the detector signal exceeds the reference potential (pulse widths); i.e., a predetermined, substantially rectangular form.

Following filtering and shaping, the detection signals are ready for decoding. In preferred form, the detection signals are converted from the pulse-position encoded form to a pulse-width encoded form suitable for processing by universal asynchronous receiver circuitry. This can be simply accomplished by using the detection signals to drive a flip-flop whose output goes to a predetermined high level when a first detector pulse is received and goes to a low level when a subsequent detector pulse is received, continuing in this fashion in response to subsequent pulses. The conversion has the effect of shifting; i.e., transforming, the load control data from the positions of the detector pulses to the widths of the pulse-width modulated signals at the flip-flop output. In this way, signals corresponding to the transmitter command signals can be generated at output 88 of the converter, particularly, multibit, pulse-width modulated, serial, digital, data words containing the load control information.

Continuing, receiver 14 further includes a decoder 90 connected to the output 88 of converter 86. As shown in FIG. 1, decoder 90 preferably includes universal asynchronous receiver (UAR) 92. As is well known in the art, UAR 92 includes a combination of circuits capable of changing the serial, pulse-width modulated signals into parallel digital data words that enable the command signals to be implemented.

Additionally, decoder 90 includes receiver address recognition elements to enable decoder 90 to identify control information intended for the receiver and its loads.

Still further, decoder 90 includes load control recognition logic 96 which identify the load control data and generate load control signals that subsequently cause the loads to be driven in accordance with the command entered at key pad 24.

With regard to receiver address recognition, as noted, physical obstructions such as walls and floors are transparent to r.f. signals. Accordingly, since several

12

receivers may be located near one another; e.g., in the same or adjacent rooms, transmitter 12 preferably adds address information to the command signals to avoid unintended control. In accordance with this approach, decoder 90 includes address recognition elements to identify control signals intended for its companion receiver.

Specifically, decoder 90 includes address storage means 94 which contains data corresponding to the data held by address storage means 32 of transmitter 12, and inserted in the command signals to uniquely identify the receiver. Storage means 94 is arranged to supply the address data to a comparator provided at decoder UAR 92. The comparator of UAR 92 is arranged to compare the address information of command signals RS3 from converter 86 with the address data stored at the receiver. If the address data stored at decoder 90 matches the address data encoded in the command signal, UAR 92 processes the load control data associated with the command signal. In preferred form, several successive comparisons showing agreement are required before correspondence is assumed.

Storage means 32 can take a number of convenient forms; e.g., a DIP switch, ROM or the like. In preferred form, storage means 94, like transmitter storage means 32, is an 8-line, DIP switch that permits manual entry of any of 256 unique address codes, and specifically, an address code to match the code entered at address storage means 32 of companion transmitter 12.

Once UAR 92, and address storage means 94 identify a command signal intended for the receiver, UAR 92, thereafter, transforms the load control information from the serial, pulse-width modulated signals of converter 86 to multibit, parallel, digital, data word signals. As noted in connection with the discussion of command generator 22, the command words in preferred form use 4 data bits. Accordingly, UAR 92 provides the load control data as 4 bit, parallel data words at UAR output 98.

As shown in FIG. 1, the parallel, load control data words generated at UAR 92 are, thereafter, supplied to recognition logic 96 which contains elements for converting the control data to load control signals. In preferred form, recognition logic 96 includes a 4 to 16 line demultiplexer which interprets the data content in the parallel digital data word of UAR 92, and provides a signal at an output line dedicated to represent the load command corresponding to the data. The load control signals corresponding to the identified load control data are provided at output 100 of recognition logic 96.

Continuing with reference to FIG. 1, receiver 14 also includes a load driver 102. As shown, driver 102 is connected to the output 100 of decoder logic 96, loads 16, 18, 20 and external power.

As noted, in preferred form, each of the lines at decoder output 100 supplies a unique load control signal, a particular line being activated when a command signal containing the corresponding control data is processed by decoder 90. Accordingly, driver 102 includes drive means connected to the load control signal lines, the loads and the load power so that when a particular load control line is activated, the corresponding load is driven.

In preferred form, the drive means includes a plurality of gated switching elements; e.g., triacs, respectively, connected to the load it is to control, the corresponding load control signal line, and, where appropriate, load power. When a load control signal is provided

by the decoder, a command signal is generated so as to trigger the switching element.

As in the case of transmitter 12, receiver 14 further includes a power source, not shown, to provide electrical power for the receiver elements and, where required, the loads. Since receiver 14 is in a stationary mount proximate the loads, an internal power supply driven by external electrical energy; e.g., 120 volt wall line, may be used.

A better understanding of the various signals generated in transmitter 12 and receiver 14 and their relationships to each other may be had on reference to FIGS. 2 and 3. With regard to transmitter 12, and FIG. 2, TS2 represents the transmitter coded command signals. As explained, the command signals are multibit, serial, digital, data words comprised as sequences of pulse-width modulated pulses.

In preferred form, the command signal data words include 18 bits: 5 synchronization; 8 receiver address; 4 load control and 1 start. In FIG. 2, by way of illustration, 5 bits are shown, particularly, bit 2 and bits 6 to 9. As is well known in the art, the bit length is defined by the interval of the system clock signals CLT. In preferred form, the transmitter clock intervals are approximately 1.8 milliseconds in length. Further, the 1's and 0's of the command word data are comprised of pulses having widths which are modulated between ¼th and ⅜ths, respectively, of the clock interval. For example, the command signal pulses at clock intervals 6 and 7 are 1's, and at intervals 8 and 9, 0's; intervals 2 to 5, partially shown, represent synchronization delay.

In accordance with the invention, to reduce the contribution to average transmission power that would result if the command signal pulses were used to modulate the transmitter oscillator, special signals, as described above, are generated for modulating the transmitter oscillator. These modulation signals, shown in FIG. 2 as TS3 pulses, have substantially reduced pulse widths as compared with the command signal pulses, but, retain the information of the command signals by having positions in time corresponding to the leading and trailing edges of the command signal pulses. In preferred form, the width of the modulation pulses TS3, are between approximately 30 to 80 microseconds, as compared to the widths of the command signal pulses which range from approximately 450 (1's) to 1,350 (0's) microseconds. As shown, the difference between the position in time of successive modulation signal pulses, as measured from the synchronization reference, i.e., the end of the synchronization delay, identifies the 1's and 0's of the address and control data. Thus, the duration of the carrier bursts necessary to convey the control data are substantially reduced when modulation is effected with the TS3 pulses as compared to the time the carrier would be generated if modulation were controlled by the command signal pulses TS2 (hatched). This economy enables the amplitude of the carrier to be substantially increased so that desirable range may be obtained with a controller having a low-sensitivity, low-cost detector operated within average power limits set by the F.C.C.

Regarding receiver 14, FIG. 3 shows that at the receiver, the initially generated pulse-width modulated command signals are reconstituted so that the command information; e.g., receiver address and load control data, may be conveniently extracted. As seen in FIG. 3, the intervals of the receiver system clock, CLR, are substantially the same as those of the transmitter clock,

CLT. Further, the signals presented to the demodulator include the modulated r.f. signals of the transmitter, RS1. Following demodulation; as for example by a superregenerative technique, detection signal pulses, RS2, are generated which correspond to the envelope of the carrier signals; i.e., the modulation signals TS3. As will be appreciated, the form of RS2 shown in FIG. 3 is a form that would result following filtering and shaping. As in the case of the modulation signals, the 1's and 0's of the command information is represented by the position in time of the pulses.

Finally, FIG. 4 shows that following conversion of the detection signals, serial, pulse width modulated signals RS3 are generated which correspond to the serial, pulse-width modulated signals of the transmitter, TS2.

A more detailed understanding of controller 10 and the elements which make up the above described subsystems may be had with reference to FIGS. 5 and 6. Particularly, in FIG. 5, a preferred form of transmitter 12 is shown schematically.

As noted, to enable entry of load commands, transmitter 12 includes a key pad 24 having a plurality of command keys. As shown in FIG. 5, key pad 24 preferably includes 6 key switches, 200, 204, 206, 208, and 210, each of which is dedicated to a specific control command; particularly, lamp intensity stepping, fan forward direction, fan reverse direction, fan medium speed, low speed and high speed, respectively. To facilitate command signal identification and subsequent processing, switches 200 and 210 are connected in circuits configured to provide both a signal specific to activation of each of the keys, and a signal specific to activation of any key. On a first side, each of the switches is connected at node 21 to the positive side of battery 212; e.g., 9 volt. As shown, the negative side of battery 212 is connected to ground. The second sides of switches 200, 202, 204, and 210 are, respectively, connected to resistors 216, 218, 222, and 224 at nodes 226, 228, 232 and 236. In the case of switches 204 and 208, their second sides are connected together, and to resistor 220 at node 230. Further, resistors 216, 218, 220, 222 and 224 are connected to one side of resistor 238 at node 234, the other side of resistor 238 being connected to ground. Accordingly, when any of the key switches is closed, a signal is produced both at the node where the particular switch is connected to its companion resistor, and at node 234 proximate resistor 238. The signal at the companion resistor uniquely identifies the particular switch closed, while the 35 signal at resistor 238 alerts other circuits of the receiver that a command has been entered, and to prepare for its receipt.

Continuing, to enable communication of the load commands to the UAT circuitry without loading the UAT data inputs, key pad 24, as shown in FIG. 5, includes a plurality of inverters 240, 242, 244, as well as NOR gate 246 connected between key pad switches 200 to 210 and UAT 28. As shown, key switch 200 is connected to the input of inverter 240 at node 226; switch 202 to the input of inverter 242 at node 228; and switches 204 and 208 to the input of inverter 244 at node 230. Further, switches 204 and 208 are connected to a first input 248 of gate 246 at node 230, and switch 206 connected to a second input 250 of gate 246 at node 232. The output of inverters, 240, 242, 248 and NOR gate 246 are connected to data inputs 252, 254, 256 and 258, respectively, of UAT 28.

15

As noted earlier, in preferred form, the 6 keys of pad 24 are arranged to provide a 4 bit, parallel, digital, data signal, TS1, at the 4 lines which constitutes output 26 of pad 24. With this arrangement, each of the 6 command signals that can be selected by manipulating the various key switches, may be uniquely encoded to 1 of 6 of the 16 possible states that can be represented on the 4 data lines 26; it will be recalled that N parallel, digital data lines are capable of defining 2^N unique binary state codes.

In preferred form, inverters 240, 242, 244 and NOR gate 246 can be implemented in single integrated circuit. Where a single integrated circuit is used, power may be provided at node 260 by connection to supply line 214 at node 262. Ground is provided at node 264.

Continuing with reference to FIG. 5, in accordance with the invention, to avoid unnecessary drain of battery 212, UAT 28 is not turned on until a control command is entered at pad 24. To facilitate this, a power management switch is provided in the form of transistor 266. As shown, transistor 266 is arranged with its collector tied to power line 214 and its emitter grounded More particularly, the transistor collector is connected to power line 214 at node 268 through resistor 270 and light emitting diode 272. Additionally, the transistor collector is also seen to be strapped to UAT power control input 274. Further, the base of transistor 266 is connected to node 234 of key pad 24. Still further, UAT power input 276 is connected to battery supply line 214 at node 278.

In operation, when any one of the command keys is closed, in addition to generating the corresponding signal pattern at the respective switch nodes, a current is generated at node 234 which drives normally off transistor 266 into conduction. As transistor 266 is caused to conduct, LED 272 lights, thereby indicating power has been turned on. Additionally, a power initiate signal is given to UAT 28 at input 274. The power initiate signal, thereafter, causes UAT 28 to power up and read the command data code provided at inputs 252, 254, 256 and 258. As will be appreciated, in this arrangement, resistor 216 to 224 and 238, as combined with transistor 266, establish an inexpensive OR gate for enabling power up of UAT 28 when any of the command keys is closed.

Since most physical barriers are transparent to r.f. signals, to avoid unintended control of non-companion receivers within the range of transmitter 12, means are provided for adding a unique address to the command signal. As seen in FIG. 5, UAT 28 is provided with an 8-line, DIP switch 280 which constitutes address code storage means 32 in preferred form. Particularly, switch 280 includes switch elements S1 to S8 (two of which are shown) respectively connected to UAT address code inputs 282 to 296. With this arrangement, 1 of 256 address codes may be manually set by closing or leaving open the various switch elements as is known in the art.

Continuing with reference to FIG. 5, UAT 28 is also seen to have external means for controlling its clock frequency. Particularly, resistor 298 and capacitor 300 are connected in parallel between UAT timing input 302 and ground at node 306. As will be appreciated, by varying the valves of resistor 298 and/or capacitor 300, the clock of UAT 28 may be readily adjusted. As also shown in FIG. 5, UAT 28 is strapped to ground at input 304.

In preferred form, UAT 28 is a specially prepared integrated circuit which includes only the transmission

16

circuitry typically found in a conventional universal asynchronous receiver transmitter integrated circuit (UART). As is known, standard integrated circuits are available which include both the transmission and reception circuitry required for asynchronous data communication. However, since by nature, the receiver of an r.f. control system is physically displaced from the transmitter, the receiver circuitry of a conventional UART would not be used in unit 28. Therefore, in the interest of economy, a custom integrated circuit chip having only the circuitry necessary for transmission is preferably used.

As noted, the purpose of UAT 28 is to convert the parallel, digital command word generated by key pad 24 to a form more suitable for transmission; i.e. serial, digital, data word, and to add the receiver address data. To this end, UAT 28 produces a pulse-width modulated data word containing command information and receiver address information at output 308.

As also noted, in order to reduce the contribution to transmission power that would result if the command signals were used to modulate the r.f. oscillator, in accordance with this invention, special signals are generated to modulate the r.f. oscillator. While the special modulation signals include the command and address data needed to control the load, they have substantially reduced pulse widths as compared with the command signals, thereby, reducing the time the carrier is required to be transmitted; i.e., reducing average carrier power.

To facilitate this, modulator 36 which generates the special signals is connected to UAT 28 at output 308. In preferred form, modulator 36 is a compound exclusive OR gate 40 arranged to trigger on the leading and trailing edges of the pulse-width modulated command signals. As shown, exclusive OR gate 40 includes a gate section 42 and buffer section 44. Since gate 40 was explained at length above, its elements and operation need not be again described here. Suffice it to say that at output 38 of gate 40, pulses of width determined by gate capacitor C and resistor R are generated, positioned in time at approximately the leading and trailing edges of the pulse-width modulated command signals.

Once the modulation signals are generated, they are used to modulate the amplitude of transmitter r.f. oscillator 72. As seen in FIG. 5, oscillator 72 includes a transistor 328 having a tuned circuit formed by a variable capacitor 332 and an inductor 318, inductor 318, preferably, being of the hairpin type. In this arrangement, capacitor 332 and inductor 318 are connected in parallel with each other and to the transistor collector at node 316. Additionally, oscillator 72 is seen to include a feedback network formed by the parallel combination of resistor 326 and capacitor 324 connected between the tuned circuit at node 322 and the transistor base. Oscillator 72 also includes a phase-shifting coil 330 connected between the transistor emitter and ground. Still further, oscillator 72 is provided with a drive network which includes series connected current limiting resistor 310 and isolation inductor 314 which, together, couple transistor 328 at collector node 316 to output 38 of modulator 36. Finally, antenna 76 is seen to be connected to inductor 318 of the oscillator tuned circuit, and is, preferably, of the bi-phase type commonly used in applications of the kind described here.

In operation, when a pulse is generated at output 38 of modulator 36, the drive network of oscillator 72 couples the pulse to the tuned circuit formed by capaci-

tor 332 and inductor 318, exciting the circuit and causing it to resonate. The energy from the resonant circuit is, thereafter, fed through capacitor 324 to the base of transistor 328 where it is amplified and supplied to the transistor collector circuit to reinforce the resonance and sustain oscillation. Continued feedback to maintain the oscillation is, again, provided through capacitor 324. Coil 330 located in the transistor emitter circuit provides the required phase shift to assure the amplified feedback signal is in phase with and reinforces the oscillations in the tuned circuit.

As will be appreciated, the average value of the modulation pulse supplied by feedback resistor 326 provides the d.c. bias to maintain transistor 328 on. Accordingly, when the modulation pulse terminates, bias for the transistor is removed, and the transistor action necessary to sustain oscillation is interrupted. Thus, the oscillator signal is generated during the modulation pulses, but not between modulation pulses.

In accordance with conventional design techniques, capacitor 332 of the oscillator tuned circuit is made variable so that the frequency of oscillator 72, which is preferably selected to be approximately 300 megahertz, may be adjusted.

Continuing, in accordance with the invention, inductor 314 of the oscillator drive network is selected to act as a high frequency stop to the oscillator signal in order to insure oscillator signal is not fed into modulator 36. Antenna 76, on the other hand, is connected to inductor 318 of the oscillator tuned circuit so as to couple the r.f. oscillations for radiation to the receiver.

Turning next to the system receiver, a more detailed understanding of it may be had with reference to FIG. 6, where a preferred form is shown schematically. As seen in FIG. 6, receiver 12 includes antenna 78 connected to detector 82 for respectively receiving the modulated carrier signal of transmitter 12 and recovering the load control information. As noted, detector 86 is preferably of the superregenerative type. Accordingly, it includes a first oscillator tuned to the carrier frequency; e.g., 300 megahertz, and a second oscillator arranged to oscillate at frequency which, while substantially lower than the high frequency, is, none the less, higher than the modulation signal frequency; e.g., approximately 400 kilohertz. Further, the high-frequency oscillator is arranged to turn on and off in response to the low-frequency oscillation and at a point in time dependent on the amplitude of the received carrier signal. In this way, the received carrier is able to produce a signal of predetermined strength having a duration and associated d.c. value that depends upon the change in amplitude of the received carrier; i.e., the carrier modulation envelope.

As seen in FIG. 6, detector 82 includes a transistor 400 having its collector connected to a source of power through current limiting resistor 402 and r.f. inductor 404. The emitter of transistor 400 is connected to ground through an inductor 406, preferably of the hairpin type, and, additionally, to antenna 78 through a high-frequency pass capacitor 408 at node 410. Continuing, the base of detector transistor 400 is connected to the transistor collector through a feedback capacitor 412 and a resonant circuit formed by the parallel combination of inductor 414, also preferably of the hairpin type, and a variable capacitor 416.

Still further a smoothing capacitor 418 is connected across transistor 400 between node 420 and ground. Additionally, node 420 is also seen to be connected to a

first input 422 of operational amplifier (op amp) 424. The second input 426 of op amp 424 is connected through current limiting resistor 428 to a constant reference voltage provided from one tap of voltage divided 430.

As shown in FIG. 6, voltage divider 430 is of a conventional type having a plurality of resistors; i.e., 454, 450, 446, and 448 connected in series between power supply tap "B" and ground. As known in the art, a reference voltage of predetermined value may be established at each of the resistors by appropriate selection of component values.

Finally, the output of op amp 424 is seen to be connected to the base of transistor 400 through a feedback resistor 432 connected between the output node 434 of op amp 434 and transistor base input node 436. A feedback capacitor 438 is connected between op amp output 434 and reference signal input 426.

In this arrangement, the high-frequency oscillator of the superregenerative detector is generated by the tank circuit of inductor 414 and capacitor 416 connected through capacitor 412 in feedback relation with transistor 400. The low-frequency oscillator of the detector, on the other hand, is generated by inductor 404 and capacitor 418 as connected to transistor 400. Further, capacitor 408 and inductor 406 connected at the transistor emitter constitute an input circuit for carrier signal received at antenna 78.

In operation, when power is applied to transistor 400, the low-frequency oscillation provided by inductor 404 and capacitor 418 enables the high-frequency oscillation resulting from feedback of tank circuit, to be turned on and off at a rate corresponding to the low frequency signal.

In the absence of received signal at emitter inductor 406, the high-frequency oscillation at the tank circuit arises randomly in response to circuit noise when the low-frequency oscillation of inductor 404 and capacitor 418 provide adequate collector signal for transistor action. The high-frequency oscillation burst so initiated continues until the low-frequency oscillation diminishes the collector signal so as to interrupt transistor action.

However, when carrier signal is received at emitter inductor 406 from antenna 78, it combines with the low-frequency oscillation to cause transistor action and tank circuit oscillation to arise earlier in time than when no carrier was present; i.e., at the occurrence of r.f. signal at emitter inductor 406, and, to, thereafter, continue longer. Thus, the duration of the high-frequency burst is made dependent on the amplitude of the received carrier, while the amplitude of the high-frequency burst is made dependent on predetermined circuit parameter and substantially independent of carrier amplitude.

Since the duration of the high-frequency burst increase with the amplitude of carrier received at emitter inductor 406, the presence or absence of carrier signal at antenna 78 may be indicated by the average value of the transistor output, following smoothing. In this regard, it will be appreciated that inductor 404 and capacitor 418 also function as a low-pass filler to smooth the transistor output. Accordingly, the output of transistor 400 corresponds to the envelope of the modulated carrier received at antenna 78, i.e. the modulation pulses of transmitter 12.

In accordance with the invention following smoothing at inductor 404 and capacitor 418, the output of transistor 400 is supplied to op amp 424 at signal input

422. When the smoothed transistor output, i.e., carrier envelope, exceeds a predetermined value established at op amp difference input 426 by the reference voltage supplied at network 430, a signal is generated at op amp output 434. Further, the signal at output 434 continues until the smooth transistor output presented to op amp input 422 falls below the reference value at input 426; i.e., when the carrier signal at inductor 406 terminates. As will be appreciated, the presence of feedback capacitor 438 between op amp output 434 and reference input 426 permits the high-frequency components of the transistor output to be further reduced.

As will also be appreciated, to maintain proper operation of detector 82, transistor 400 must sustain superregenerative operation; i.e., high frequency oscillation bursts in response to the low-frequency oscillation and received carrier signal. To insure that superregenerative operation is not distorted by transistor operating characteristics, detector 82 in accordance with the invention features means for controlling the operating point, i.e. bias, of transistor 400. Particularly, feedback of the detector output is used to insure transistor bias is maintained at the linear portion of the transistor operating characteristic. In this way, not only is distortion due to bias shift avoided, but also use of inexpensive transistors having limited or variant linear regions is possible, the feedback enabling dynamic control of the bias point at the linear portion of the transistor characteristic.

To facilitate the feedback control of transistor bias, the output 434 of op amp 424 is connected to the base of transistor 400 at node 436, through feedback resistor 432.

Following generation of the detector signals, the receiver has available to it the load control information originally encoded at transmitter 12. Therefore, and as previously noted, the detector output can be immediately decoded to produce the load drive signals. However, in accordance with the invention, to reduce the likelihood that spurious signals arising from radiated noise; e.g., appliance motors, auto ignition, etc., will cause false load control, the detector output is first filtered to verify authenticity of the control information.

To provide signal verification, the detector output is passed through multiple stages of cascaded high-pass and low-pass filtering. As noted in connection with the description of converter 86, the high-pass filtering is configured to pass detector output pulses having widths approximating the width of the transmitter modulation pulses, while the low-pass filtering is configured to pass sequential detector pulses spaced in time within a range anticipated for the transmitter modulation pulses, i.e., the range of widths for the transmitter pulse-width modulated control signals. As will be appreciated detector pulses outside the pass bands of the filtering are rejected, thereby reducing the likelihood of spurious control signals.

As seen in FIG. 6, a first, high-pass filter stage 438 is connected to the output of detector 82. First stage 438 includes a capacitor 440 connected in series with the output of op amp 424 at node 434, and a shunt resistor network including the series combination of resistor 444, 446 and 448 connected between capacitor node 442 and ground. As will be appreciated, capacitor 440 and resistors 444, 446 and 448 are selected to pass the high-frequency anticipated for pulses having a width corresponding approximately to the transmitter modulation

pulses above described; i.e. the output of transmitter exclusive OR gate 40.

Continuing, a first low-pass filter stage 456 is provided connected to high-pass filter stage 438. As shown, low-pass filter 456 is preferably of the operational-amplifier type to facilitate integrated circuit implementation. It includes op amp 458 having a signal input 460 connected in series with capacitor 440 of high-pass filter 438. Further, the reference input 462 of op amp 458 is connected to ground through resistor 464 and capacitor 466, while the parallel combination of feedback capacitor 468 and resistor 470 is connected between op amp reference input 462 and output node 474. As shown, op amp 458 is connected to power at node 473 and to ground at node 471. As will be appreciated, this combination of elements limits the high-frequency components of the filter signal output.

As shown, a feedback diode 472 is also provided between the output and reference input of op amp 458, poled with its anode connected to output node 470. As connected, diode 472 clips, and, thereby, eliminates any positive-going signal portion; e.g., ringing, and allows only the negative portion of the pulse signal to pass.

The elements of low-pass filter stage 458 are selected in a conventional fashion so as to pass the low-frequency anticipated for a waveform comprising sequential, narrow pulses spaced in time within a range corresponding approximately to the range for the transmitter modulation pulses described previously. As will be recalled, the spacing of the modulation pulse corresponds to the leading and trailing edges of the pulse-width modulated load control signals produced at the output of UAT 28.

As seen in FIG. 6, a second, high-pass filter stage 476 is connected to the output of first, low-pass filter stage 458. As shown, like first stage 438, the second, high-pass filter stage 476 includes a capacitor and resistor network. Particularly, second, high-pass stage 476 includes capacitor 478 connected in series with the output node 474 of preceding low-pass stage 456. Additionally, a shunt resistor network is provided including the series combination of resistors 482, 450, 446 and 448 connected between capacitor node 480 and ground. Like first, high-pass stage 438, the elements of second, high-pass stage 476 are selected to pass the high frequencies anticipated for pulses having a width corresponding approximately to the transmitter modulation pulses.

Receiver 14 also includes a second, low-pass filter stage 484. As shown, filter stage 484 is connected to the output of the preceding high-pass filter 476. Like first low-pass stage 458, stage 484 is of the op-amp type, and includes op amp 486 having a signal input 488 connected in series with capacitor 478 of preceding high-pass filter stage 476. The reference input 490 of op amp 486 is connected to ground through resistor 492 and capacitor 494. Further, the parallel combination of feedback capacitor 496 and resistor 498 are connected between op amp reference input 490 and output node 502. As in the case of the first low-pass stage, feedback diode 500 is poled with its anode connected to the op amp output in order to eliminate any positive-going portion of the output signal. As shown, power is supplied to op amp 486 at node 501, and ground at node 497.

Like first stage 456, the elements of second low-pass filter 484 are selected to limit the high-frequency components of the filtered output signal. More particularly, filter stage 484 is intended to pass a waveform corresponding to the sequence of pulses spaced in time within

a range corresponding approximately to the transmitter modulation pulses.

Following filtering, the receiver signals are preferably shaped to provide a waveform more closely approximating that of the transmitter modulation pulses; i.e., short duration rectangular pulses. For this purpose, receiver 12 includes wave shapes 504 connected to the output of second low-pass filter stage 484. As seen in FIG. 6, wave shapes 504 includes a further stage of low-pass filtering 506 and an op amp 508 configured as a threshold detector. More particularly, low-pass filter 506 includes a series resistor 510 connected between output node 502 of second low-pass filter stage 497 and the negative input 512 of op amp 508. Additionally, low-pass filter 500 includes a shunt capacitor 514 connected between op amp input 512 and ground. Still further, the positive input 516 of op amp 508 is connected to voltage divider network 430 at resistor 446. The output of op amp 508 is provided at line 518. Op amp 508 is also seen to be connected to power at node 520 and to ground at node 522.

As noted, op amp 508 is configured as a threshold detector. Accordingly, when the output of filter stage 487; i.e., the detector signals, exceeds (absolute value) the reference signal at op amp input 516, the output of op amp 508 at line 518 rises to a predetermined amplitude at a predetermined rate, the amplitude and rate being established in a conventional manner by selection of circuit parameters. Further, the output of op amp 508 remains at the predetermined amplitude until the signal from filter stage 497 falls below (absolute value) the reference signal established by voltage divider 430, whereupon, the op amp output falls to zero, again at a circuit determined rate. In this way, a well defined rectangular pulse having a predetermined amplitude rise time and fall time may be generated in response to the filtered detector signal.

As noted earlier, since the filtered and shaped detector pulses include the load control and load address information encoded in the pulse positions, they could be used to generate the load control signals without further manipulation. However, in the interests of low-cost and simple decoding, the filtered and shaped detector signals are preferably first converted to pulse-width modulated signals corresponding to the pulse-width modulated command signals generated at transmitter 12. In this way, inexpensive universal asynchronous receiver circuitry can be used to recover the load control information.

To effect signal conversion and decoding, the output of wave shaper 504 at line 518 is connected to a custom integrated circuit chip 524 at input 526. While not shown for simplicity of the drawing, circuit chip 524 includes elements of previously described signal converter 86 and elements of decoder 90; particularly, UAR 92 and recognition logic 96.

In preferred form, the signal transformer of converter 86 is implemented in the circuits of chip 524 as a flip-flop configured to generate pulse-width modulated signals corresponding to the command signals generated at transmitter 12 in response to the filtered and shaped detector signals.

In operation, successive detector pulses presented at chip input 524 cause the converter flip-flop to turn on and off such that the load control and address information encoded in the positions of the pulses; i.e., the time between successive pulses, is converted to the width of the flip-flop output pulses. Thereafter, the resulting

pulse-width modulated signals of the converter can be presented to the decoder UAR also implemented in the circuitry of chip 524.

As noted previously, to assure the UAR decodes only signals intended for loads associated with receiver 14, the decoder includes address recognition elements to enable identification of control signals intended for receiver 14. To facilitate signal recognition, the decoder includes address storage means 94 which is provided with data that uniquely identifies the receiver, the data being selected to correspond to the identification data stored at the transmitter and encoded into the command signal. As seen in FIG. 6, address storage means 94, like that of the transmitter, includes an 8-line, DIP switch 528 having switch elements S1 to S8 (two of which are shown) respectively connected to address code inputs 530 to 544 of chip 524 and receiver power. With this arrangement, 1 of 256 address codes may be manually set by closing or leaving open various switch elements, the pattern being selected to be identical to that of transmitter address code switch 280.

The address code data provided by powered switches S1 to S8 is supplied internally of chip 524 to a comparator of the decoder UAR. At the comparator, the address data of the converter command signal is checked to determine if the control information is intended for the receiver loads. If it is, the command signal is read into the UAR for decoding. As noted, in preferred form, the comparison may be repeated several times; i.e., clock cycles, to assure correspondence.

Once a command signal is recognized as intended for receiver 14, the UAR circuitry of chip 524 transforms the serial, pulse-width modulated converter signal and the load control information it contains into a parallel, digital, data word. Thereafter, and as described above, the parallel, digital, data words may be supplied to recognition logic, also implemented in chip 524, to convert the control information to load control signals. More particularly, the recognition logic, preferably a demultiplexer, interprets the control data content of the command words in a conventional fashion and generates signals at the respective chip outputs dedicated to the load command corresponding to the data. Specifically, and as shown in FIG. 6, control signals for lamp intensity stepping are provided at chip output 548; for fan forward and reverse directions at output 550; for fan low speed at output 552; for fan medium speed at output 554; and for fan high speed at output 556.

As also seen in FIG. 6, line synchronization for chip 524 is provided at chip input 546, input 546 being connected to line power at source 104 through current limiting resistor 650. Capacitor 652 shown connected between input 546 and ground provides high-frequency, bypass filtering. Further, timing stabilization for chip 524 is provided at input 547, input 547 being connected to ground through capacitor 654. Finally, ground for chip 524 is provided at chip input 549.

Continuing with reference to FIG. 6, receiver 14 is seen to further include driver 102 for implementing the control signals of chip 524 at the loads; e.g., the ceiling fan and companion light. Load driver 102 includes a plurality of gated switching elements, specifically, triacs, each of which is connected to a load associated with the fan; e.g., the motor main winding, various speed windings, the lamp and power. In this arrangement, the control signals generated by the decoder of chip 524 control the conduction angles of the triacs,

23

which in turn control the supply of power to the receiver loads.

As seen in FIG. 6, driver 102 includes a triac 558 connected between power distribution line 560 and lamp feed line 562. As shown, triac gate input 564 is connected to the lamp control output 548 of chip 524 through current limiting resistor 566 and a blocking diode 568. Additionally, a varristor 570 is connected across triac 558 between power distribution line 560 and lamp feed line 562.

In operation, when a lamp control signal is generated at chip 524 in response to a command entered at transmitter 12, triac 578 is gated on and power supplied to the fan lamp. In accordance with the invention, chip 524 is arranged to increase the conduction angle of triac 558, so as to power the lamp for longer time intervals, thereby increasing the light intensity of the lamp in response to successive light stepping commands entered at the transmitter. As will be appreciated, resistor 566, diode 568 and varristor 570 are provided for protective purposes. Resistor 566 limits the gate signal level to triac 558, diode 568 protects chip 524 from signals that might be feed back from triac 558, and varristor 570 protects triac 558 from surges arising during switching.

Continuing, load driver 102 also includes a triac 572 connected between power distribution line 560 and feed line 574 for the fan motor high-speed winding. Like triac 558, triac 572 is connected to one of the control outputs of chip 524. Particularly, gate input 576 of triac 572 is connected to output 556 of chip 524 through current limiting resistor 578. Accordingly, when a control for motor high speed is generated at chip 524 responsive to a command entered at transmitter 12, triac 572 is gated on, activating the high-speed winding. As shown, resistor 580 is provided in feed line 574 to limit the drive supplied.

In a like fashion, triac 582 is connected between power distribution line 560 and feed line 584 for the fan motor medium-speed winding. Again, the triac is connected to chip 524 for control. Particularly, gate input 586 is connected to chip control output 554 through current limiting resistors 588 and 590. A current limiting resistor 592 in feed line 584, and a varristor 594 across triac 582 are provided for circuit protection. When a control signal for fan medium speed is generated at chip 523, power is supplied over line 584 to the motor medium-speed winding.

And, again, in like fashion, triac 596 is connected between power distribution line 560 and feed line 598 for the motor low-speed winding. As in the case of the high and medium speed triacs, triac 596 is connected to chip 524 for control. As shown, triac gate input 600 is connected to chip control output 552 through current limiting resistor 602. When a control signal for fan low speed is generated at chip 524, power is fed over line 598 to the motor low-speed winding.

In accordance with the invention, and as will be appreciated, chip 524 is arranged such that the speed control signals are exclusive in time; i.e., chip 524 will generate a control signal for only one fan speed at a time. Further, once a speed is selected, chip 524 manages the conduction angle of the respective triac to supply required power to the appropriate winding until another speed is selected. As will also be appreciated, power for fan action is provided when any of the fan speeds has been selected.

Load driver 102 also includes a triac connected between line power 104 and the receiver internal power

24

supply 626 for effecting fan reversal. Like the other triacs, triac 604 is connected to a control signal output of chip 524. Particularly, triac gate input 606 is connected to output 550 of chip 524 through current limiting resistor 608. To facilitate fan direction reversal, triac 604 is also connected to a fan motor polarity reversing relay 610. As shown, triac 604 is connected to one side of activation winding 612 of relay 610, winding 612 being connected on its other side to line power through diode 614 and current limiting resistor 616. A capacitor 618 is connected across relay winding 612. As also seen, relay 610 is provided with a set of double-pull-double-throw relay contacts 620 connected between line power 104 and fan motor forward feed line 622, reverse feed line 624 and high-speed winding fee line 574.

Accordingly, when a control signal is generated at chip 524 responsive to a command entered at transmitter 12 for forward or reverse fan direction, triac 604 is gated to establish a reversal of current flow in relay winding 612. When the direction of current flow in winding 612 reverses, contacts 620 are reset to reverse the polarity of the fan motor and, thereby, reverse fan direction.

Finally, receiver 14 also includes an internal power supply to provide power both to the receiver loads and the receiver circuitry. As seen in FIG. 6, power supply 626 is a substantially conventional, half-wave, multiplication rectifier including elements for output regulation. Particularly, supply 626 includes a current limiting resistor 628 connected between line power 104 and one side of an input capacitor 630. The other side of capacitor 630 is connected at node 632 to the junction of two oppositely poled rectifier diodes 634, 636. As shown, the unjoined poles of diodes 634, 636, are connected across the parallel combination of output filter capacitor 638 and a zener, regulation diode 640 to form tap "A" of supply 626, at which regulated and filtered half-wave power is provided.

As seen in FIG. 6, supply 626 also includes a second tap "B." As shown, tap "B" is formed by an combination of limiting resistor 642 and filter capacitor 644 connected across supply tap "A", tap "B" being set at node 646 between resistor 642 and capacitor 544. Like tap "A", tap "B" provides regulated and filtered half-wave power. However, the level of power at tap "B" is reduced as compared with that at tap "A" base on the selected values for resistor 642 and capacitor 644, as is known in the art, tap "B" being intended to supply particular components of the receiver as shown.

As noted, this invention also contemplates a method for remotely controlling electrical loads having resistive or complex impedances. In accordance with the invention, a preferred form of the method includes generating coded command signals in the form of pulse-width modulated pulses, wherein the width of the pulses conveys the load control data. The command signals may be generated by first generating a command selection signal; e.g., where a user manually enters a command request at a key pad. As will be appreciated, other steps could be used for generating the command selection requests, particularly, an automated response to a transducer sensitive to a condition intended to control one or more of the loads. An illustration would be control of a room fan in response to room temperature, or control of lamps in response to the level of room lighting.

In preferred form, the command selection signals comprise multibit, parallel, digital, data words contain-

ing the information necessary to uniquely identify the command and effect control of the loads. Following generation of the command selection signals, the signals are prepared for subsequent transmission by first converting them to multibit, serial, pulse-width modulated signals including, in preferred form, address data sufficient to uniquely identify the receiver associated with the loads to be controlled. Additionally, signal synchronization and start recognition data may also be included to aid signal processing.

In accordance with the invention, following generation of the command signals, a modulation signal is generated having pulses whose positions in time correspond to the leading and trailing edges of the pulse-width modulated, command signals. In preferred form, the modulation signals may be generated by differentiating the command signals.

The method, thereafter, calls for the generation of r.f. signals whose amplitude is modulated at points in time corresponding to the pulses of the modulation signals. In preferred form, the modulation signals adjust the amplitude of the r.f. signals by controlling an oscillator which generates the r.f. signals; e.g., by turning the oscillator on and off in response to the modulation signals. Next, the modulated r.f. signals may be radiated in a manner well known in the art.

In this way, the average power of the modulated r.f. signal may be reduced as compared with the r.f. signals that would result if modulation were effected with pulse-width modulated command signals.

Following radiation, the r.f. signals containing the address, load control, and other data are received proximate the loads to be controlled. Thereafter, the r.f. signals are demodulated to generate detection signals having pulses whose position in time correspond to the pulses of the modulation signals. In preferred form, a superregenerative detection method is used to generate the detection signals from the received modulated r.f. signals.

In accordance with the broad aspect of the method, following generation of the detection signals, the detection signals are decoded to generate load control signals. This may be done with pulse-position decoding techniques known to those skilled in the art.

Finally, following generation of the load control signals, the loads are electrically driven in a known manner; e.g., with triggered electrical switches, in accordance with the data contained in the load control signals.

In a preferred form of the method, in order to simplify decoding, the detection signals are first converted to multibit, serial, pulse-width modulated, digital, data word signals containing the load control information which corresponds to the command signals first generated. This may be readily accomplished by driving a flip-flop with the detection signals in a fashion known in the art.

Also in accordance with a preferred form of the method, following generation of the detection signals and prior to the conversion of the detection signals to the pulse-width modulated signals described above, the detection signals are filtered to exclude detection signal pulses not corresponding in width or position in time to the pulses of the modulation signals. As will be appreciated, this filtration has the effect of limiting the presence of spurious control signals.

After filtration, the detection signals may be shaped to give them a substantially rectangular form. This may

be done in any convenient manner; e.g., by driving an operational amplifier at one input with a constant value reference signal and the other input with the filtered detection signals.

In accordance with the preferred form of the method, following conversion, the detection signals are decoded to generate load control signals. More particularly, the pulse-width modulated signals may be examined to determine if the address data contained corresponds to address data made available during decoding; e.g., by comparing the converted signal data with stored address data. In preferred form, the comparison may be made multiple times; e.g., twice, to assure correspondence.

Once the converted detection signals have been confirmed as valid, the load control data contained therein can be converted to multibit, parallel, digital, data words and, thereafter, demultiplexed, in a manner well known in the art; e.g., with the use of data recognition logic, to generate load control signals.

Finally, following generation of the load control signals, the loads may be driven in accordance with the control data to effect the commands initially selected. In preferred form, the load control signals may be used to trigger gated switches connected to the loads to effect the desired control.

While the apparatus and method aspects of this invention has been described in their preferred forms, it will be appreciated that changes may be made in nature, construction, and arrangement of the elements and steps without departing from the true spirit and scope of the invention.

What I claim is:

1. A remote controller for controlling one or more electrical loads, the loads having resistive or complex impedances, the controller comprising:

a. transmitter means for transmitting modulated r.f. signals, the transmitter including:

    i. command generator means for generating command signals containing load control data, the command signals including sequences of pulses, wherein each pulse is produced within a fixed time interval, and has a width defined by the leading and trailing edges thereof that is variable within the fixed interval;

    ii. oscillator means for generating r.f. oscillator signals;

    iii. modulator means responsive to the command signals for generating modulation signals to vary the oscillator signal amplitude at points in time corresponding approximately to the leading and trailing edges of the command signal pulses such that the amplitude of the oscillator signal between the points in time corresponding approximately to the leading and trailing edges of the command signal pulses is reduced relative to the amplitude of the oscillator signals at points in time corresponding approximately to the leading and trailing edges of the command signal pulses;

    iv. transmitter antenna means responsive to the oscillator signals for radiating the modulated r.f. oscillator signals; and

b. receiver means responsive to the r.f. signals radiated by the transmitter, the receiver means including:

    i. receiver antenna means for receiving the signals radiated by the transmitter and supplying signals that correspond to the modulated oscillator r.f. signals;

ii. detector means responsive to the receiver antenna means signals for demodulating the receiver antenna means signals and generating detector signal corresponding to the transmitter modulation signals which contain load control data;

iii. decoder means, responsive to the detector signals for generation load control signals corresponding to the control data contained in the detector signals; and

iv. driver means responsive to the decoder signals for driving the loads in accordance with the load data.

2. The controller of claim 1 wherein the modulator means varies the oscillator signal amplitude such that the portions of the oscillator signals of reduced amplitude during the command signal pulses are spaced approximately equally between the points in time corresponding approximately to the leading and trailing edges of the command signal pulses and wherein the receiver further includes converter means responsive to the detector signals for converting the detector signals into signals which are pulse-width modulated and which contain load control data corresponding to the load control data contained in the control signals of the command generator means, and wherein the receiver decoder means is responsive to the converter signals for generating load control signals corresponding to the control data contained in the converter signals.

3. The controller of claim 2 wherein the converter means includes signal filter means for rejecting detector signals not corresponding to the transmitter modulation signals.

4. The controller of claims 3 wherein the converter means includes wave shaping means to provide the detector signals passed by the filter means with shapes corresponding to those of the modulation signals.

5. The controller of claim 4 wherein the modulation signals are in the form of pulses having a position in time corresponding to the leading and trailing edges of the pulses of the pulse width modulated signals produced by the command generator means.

6. The controller of claim 5 wherein the signal filter means includes filtering elements selected to pass detector signal pulses having shapes and position in time corresponding to the pulses of the modulation signals and reject detector signal pulses not having shapes and positions in time correspond to the pulses of the modulation signals.

7. The controller of claim 6 wherein the converter means includes signal transforming means for converting the filtered and shaped detector signals into pulse-width modulated signals corresponding to the pulse-width modulated command signals of the command generator means, wherein the widths of the converter signal pulses are determined by the position in time of the filtered and shaped detector signal pulses.

8. The controller of claims 7 wherein the signal transforming means includes flip-flop means.

9. The controller of claim 8 wherein the wave shaping means includes an operational amplifier having one input electrically coupled to the filter means and one input coupled to a reference signal means.

10. The controller of claim 7 wherein the decoder means includes universal asynchronous receiver circuits that are responsive to the pulse-width modulated converter signals to produce multibit, parallel, digital, data word signals having a data content corresponding to the load control data of the transmitter command signals.

11. The controller of claim 10 wherein the decoder means includes address storage means containing address data to identify the receiver, the decoded means also including address comparison means responsive to the received address signals and the pulse-width modulated signals of the converter means to identify converter signals corresponding to the command signals intended for the receiver and its associated loads.

12. The controller of claim 11 wherein the detector means includes a superregenerative detector means.

13. The controller of claim 2 wherein the command generator means includes command selector means to permit a user to select command signals.

14. The controller of claim 13 wherein the command selector means generates multibit, parallel, digital, data word signals containing load control data, and wherein the command generator means includes universal asynchronous transmitter circuits responsive to the signals of the command selection means, to produce pulse-width modulated, serial, coded command signals containing the load command data.

15. The controller of claim 14 wherein the command generator means includes address entry means to permit the inclusion of receiver address code data in the pulse-width modulated command signals.

16. The controller of claim 15 wherein the command selector means includes key pad means.

17. The controller of claim 15 wherein the modulator means includes signal differentiator means responsive to the pulse-width modulated command signals for producing pulse signals whose position in time corresponds to the leading and trailing edges of the pulse-width modulated command signals, the signal differentiator means being coupled to the oscillator means to turn the oscillator means on during the differentiator signal pulses and turn the oscillator means off between the differentiator signal pulses.

18. A transmitter means for use in a remote controller the remote controller being adapted to control one or more electrical loads having resistive or complex impedances, the transmitter comprising:

a. command generator means for generating coded command signals containing load control data, the command signals including sequences of pulses wherein each pulse is produced within a fixed time interval and has a variable pulse width within the interval;

b. oscillator means for generating r.f. oscillator signals;

c. modulator means responsive to the command signals for generating modulation signals to vary the oscillator signal amplitude at points in time corresponding approximately to the leading and trailing edges of the command signal pulses such that the amplitude of the oscillator signal between the points in time corresponding approximately to the leading and trailing edges of the command signal pulses is reduced relative to the amplitude of the oscillator signals at points in time corresponding approximately to the leading and trailing edges of the command signal pulses; and

d. antenna means coupled to the oscillator means for radiating the modulated r.f. oscillator signals.

19. Transmitter means in accordance with claim 18 wherein the command generator means includes command selector means for generating multibit, parallel, digital data word signals containing load control data, the command generator means also including universal asynchronous transmitter circuits responsive to the command selector means signals for generating pulse-

width modulated, serial, coded command signals containing load data, and wherein the modulator means varies the oscillator signal amplitude such that the portions of the oscillator signal of reduced amplitude during the command signal pulses are spaced approximately equally between the points in time corresponding approximately to the leading and trailing edges of the command signal pulses.

20. Transmitter means in accordance with claim 19 wherein the modulator means includes signal differentiator means responsive to the pulse-width modulated command signal for producing pulsed differentiator signals wherein the position of the differentiator signal pulses correspond approximately in time to the leading and trailing edges of the pulse-width modulated command signals, the signal differentiator means being coupled to the oscillator means such that the oscillator means is turned on during the differentiator signal pulses and turned off between the differentiator signal pulses.

21. Transmitter means in accordance with claim 20 wherein the command selector means includes key pad means.

22. Receiver means for use in a remote controller, the remote controller being adapted to control one or more electrical loads having resistive or complex impedances by producing coded command signals containing the load control data, the command signals including sequences of pulses wherein each pulse is produced within a fixed time interval and has a variable pulse width within the interval, the receiver means comprising:

a. antenna means for receiving modulated r.f. signals containing coded command signals including load control data, and, thereafter, generating signals among which are included signals corresponding to the received modulated r.f. signals;

b. detector means responsive to the antenna signals for demodulating the antenna signals and generating detector signals having pulses whose positions in time correspond approximately to the leading and trailing edges of the command signal pulses;

c. decoder means responsive to the detector signals for generating decoder signals containing load control data contained in the detector signals; and

d. driver means responsive to the decoder signals for driving the loads in accordance with the received load control data.

23. The receiver means of claim 22 wherein the detector signals generated at approximately the leading and trailing edges of the command signal pulses are of approximately equal duration and wherein the receiver means further includes a converter means responsive to the detector signals for converting the detector signals into pulse-width modulated converter signals containing the load control data corresponding to the load control data of the command signals; and wherein the decoder means is responsive to the converter signals.

24. The receive means of claim 23 wherein the detector signals are in the form of sequential pulses having positions in time corresponding to the leading and trailing edges of the command signal pulses.

25. The receiver in claim 24 wherein the signal converter means includes signal filter means having filtering elements selected to pass detector means pulses having pulse widths and pulse positions within predetermined ranges and reject detector means signals having pulse widths and pulse positions outside predetermined ranges.

26. The receiver means of claim 25 wherein the signal converter means includes wave shaping means to give the detector signals passed by the filter means the form of substantially rectangular pulses.

27. The receiver of claim 26 wherein the signal converter means includes signal transformer means to convert the filtered and shaped detector signals into the pulse-width modulated signals.

28. The receiver of claim 27 wherein the transformer means includes flip-flop means.

29. The receiver of claim 27 wherein the decoder means includes universal asynchronous receives circuits that are responsive to the pulse-width modulated converter means signal to produce multibit, serial, digital data word signals having a data content corresponding to the control data of the received command signals, and wherein the decoder means includes address storage means containing receiver address data, for generating receiver address signals, the decoder means also including address comparison means responsive to the receiver address signals and the pulse-width modulated signals of the converter means to identify converter signals intended to control loads associated with the receiver.

30. A method for remotely controlling one or more electrical loads having resistive or complex impedances using r.f. control signals, the method comprising:

a. generating coded command signals including load control data, the coded command signals being in the form of sequences of pulse-width modulated pulses provided within fixed time intervals;

b. generating modulation signals having pulses whose position in time corresponds approximately to the leading and trailing edges of the pulse-width modulated command signals;

c. generating r.f. signals whose amplitude is modulated at points in time corresponding to the pulses of the modulation signals so that the amplitude of the oscillator signal between the modulation pulses is reduced relative to the amplitude of the oscillator signal during the modulation pulses;

d. radiating the modulated r.f. signals;

e. receiving the modulated r.f. signals proximate the loads to be controlled;

f. demodulating the r.f. signals received and generating detection signals having pulses whose position in time correspond to the pulses of the modulated signals;

h. driving the loads in accordance with the control data of the load command signals.

31. The method of claim 30, wherein the modulation signal pulses generated at approximately the leading and trailing edges of the command signal pulses are generated so that they have approximately equal durations and wherein following generation of the detection signals, the detection signals are converted to pulse-width modulated pulse signals, the width of which are determined by the approximate time between the pulses of the detection signals, to generate a signal corresponding to the command signals, and wherein the converted detection signals are decoded to generate the load control signals.

32. The method of claim 31 wherein converting the detection signals to the pulse-width modulated signals includes filtering the detection signals, which are in the form of pulses, to permit passage of signals having pulse widths and pulse positions are within a range corre-

31

sponding approximately to the pulse widths and pulse positions anticipated for the modulation signals, and rejecting detection signals not having pulse widths and pulse positions approximately within a range anticipated for the modulation signals.

33. The method of claim **32** wherein the converting of the detection signals to the pulse-width modulated signals includes shaping the filtered detection signal pulses to a substantially rectangular form.

34. The method of claim **33** wherein the wave shaping of the filtered detection signals includes comparing the filtered detection signals to a reference signal and transmitting a predetermined signal amplitude during

32

the time period the absolute value of the filtered detection signals exceed the reference signal.

35. The method of claim **30** wherein the modulation signals are produced by generating a pulse of predetermined width at the leading and trailing edges of the pulse-width modulated command signal pulses.

36. The method of claim **35** wherein r.f. signals are generated during the predetermined pulse width of the modulation signal pulses and wherein r.f. signals are not generated during the time interval between that trailing edge and leading edge of sequential modulation signal pulses.

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