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(54) **METHODS AND DEVICES FOR IN-PHASE AND QUADRATURE SIGNAL GENERATION**

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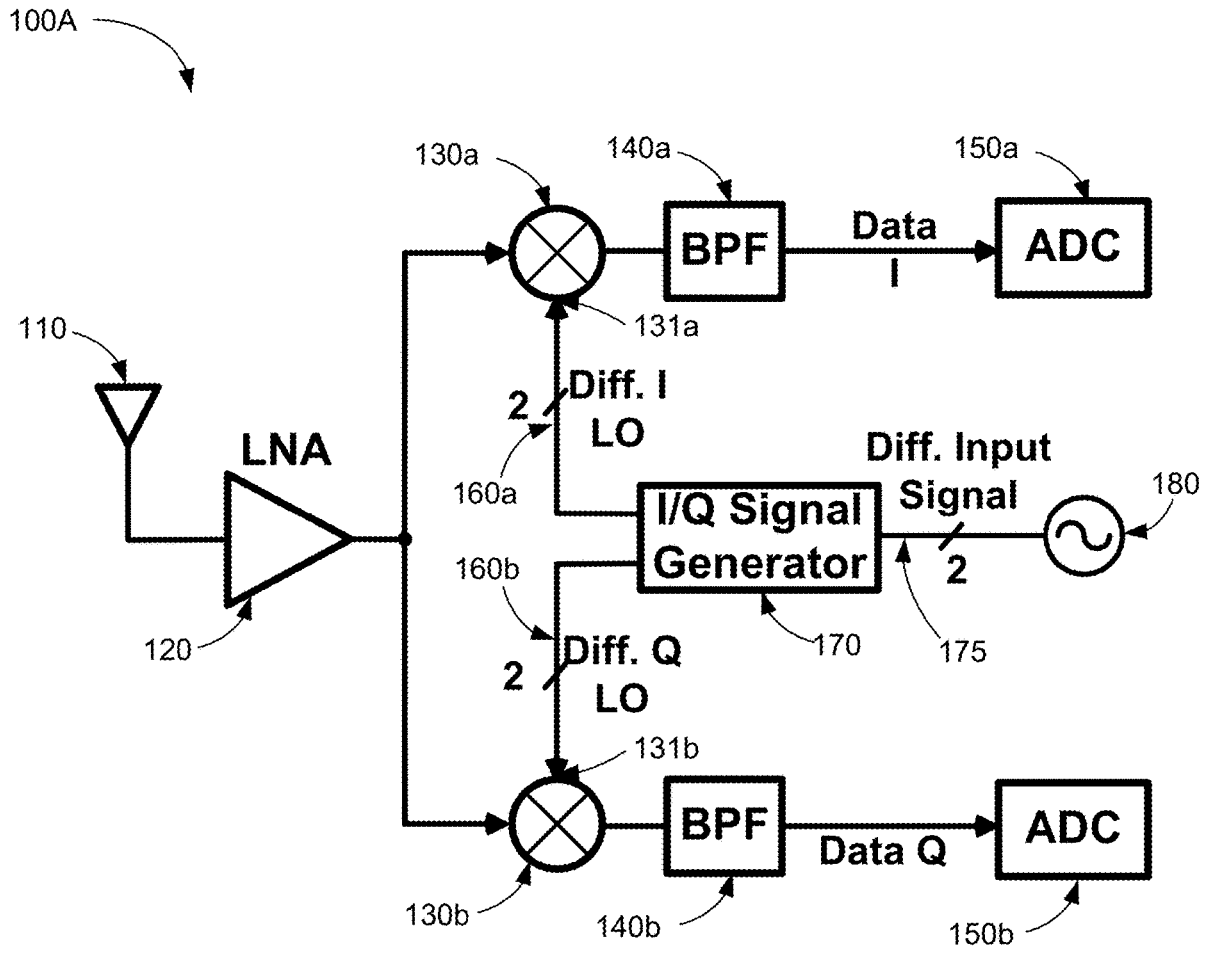
(57) **ABSTRACT**

A method for in-phase (I) and quadrature (Q) signal generation is disclosed. The method may include a first stage receiving a differential input signal. The first stage may also generate first differential in-phase and quadrature output signals, which may be sent by the first stage to a second stage. The second stage may generate second differential in-phase and quadrature output signals, which may have amplitude and phase mismatches less than an amplitude and phase mismatches of the first differential output signals. The second stage may then output the second differential I/Q output signals.



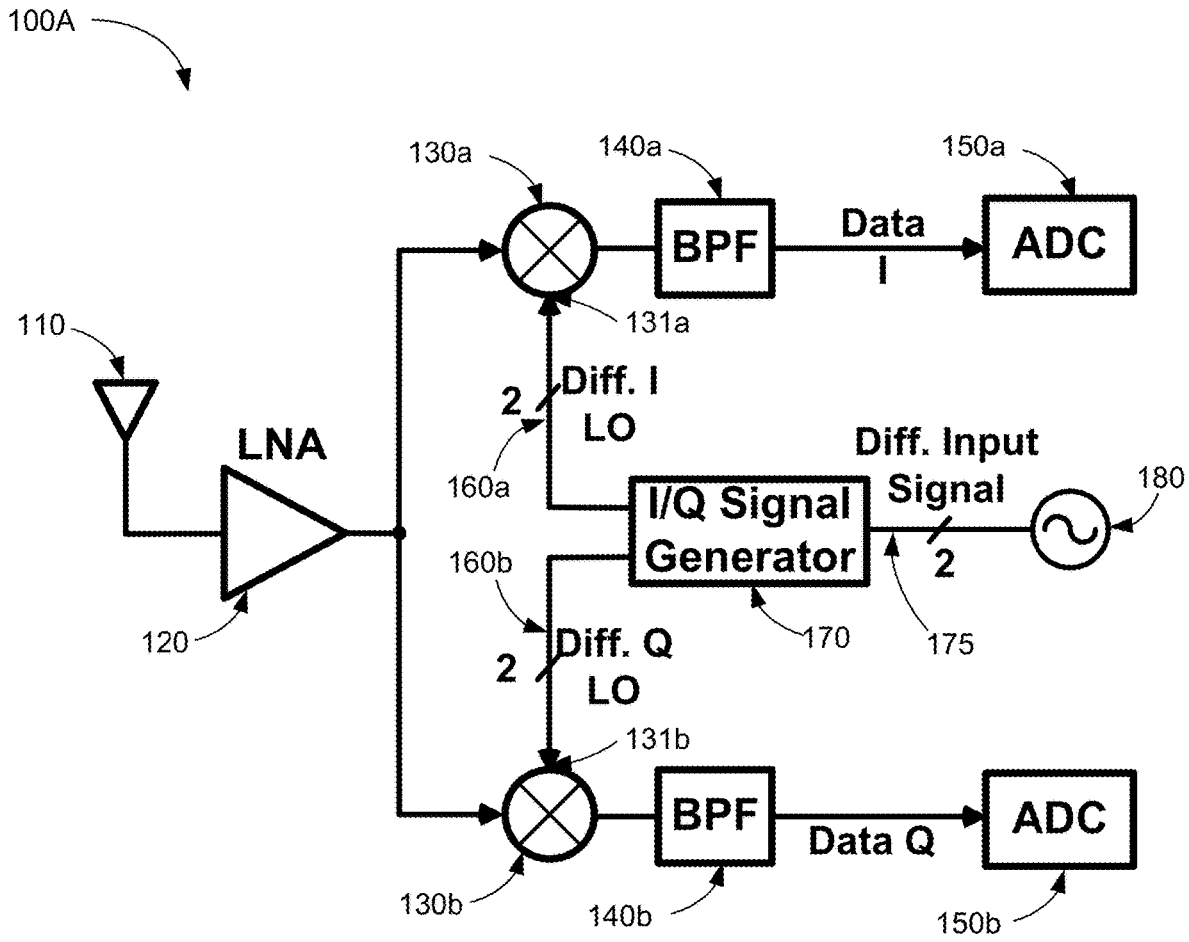

100A
130a
140a
150a
BPF
Data
I
ADC
110
131a
2
Diff. I
LO
LNA
160a
Diff. Input
Signal
180
I/Q Signal
Generator
160b
2
120
170
175
Diff. Q
LO
2
131b
BPF
Data Q
ADC
130b
140b
150b

FIG. 1A

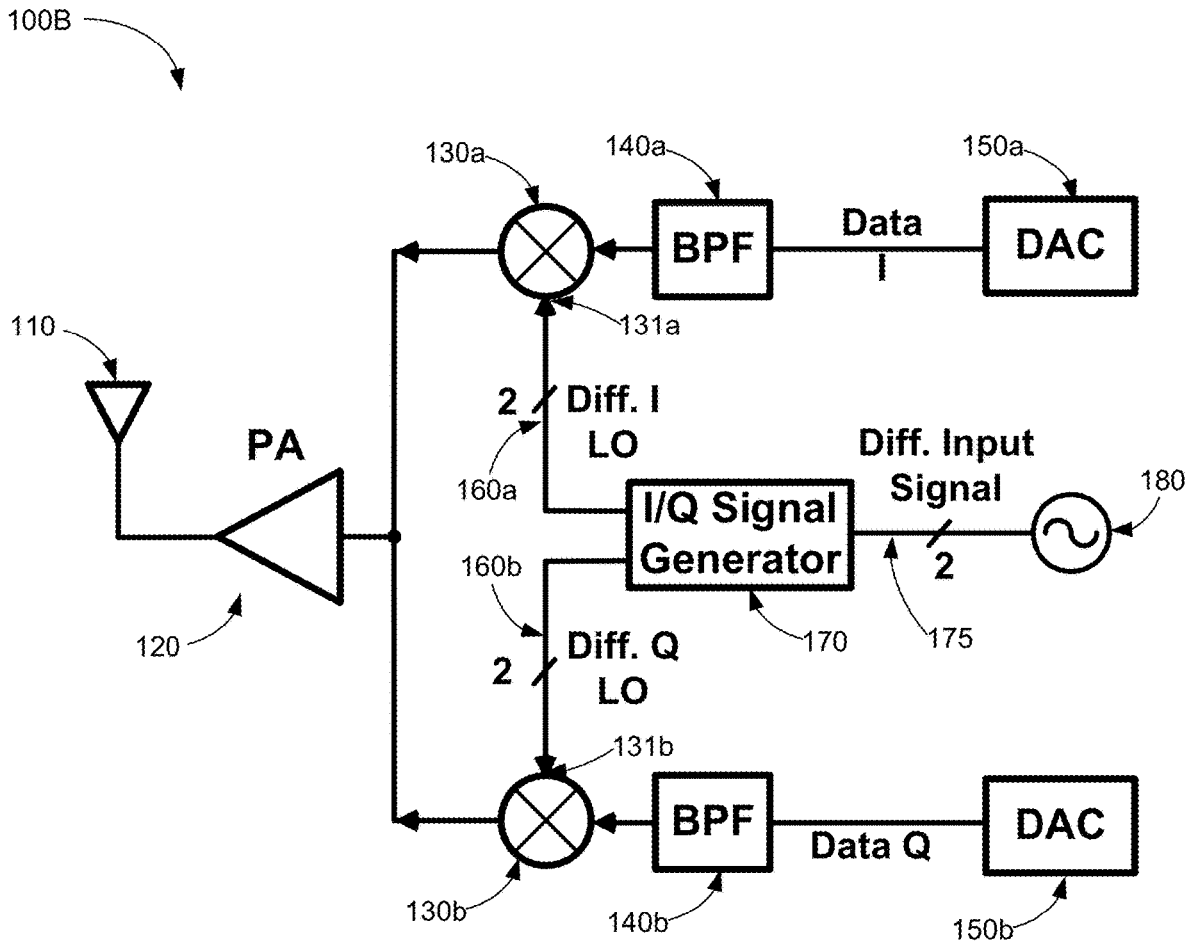

100B
130a
140a
150a
BPF
Data
I
DAC
131a
110
2
Diff. I
LO
PA
160a
I/Q Signal
Generator
Diff. Input
Signal
180
160b
2
170
175
120
2
Diff. Q
LO
131b
BPF
Data Q
DAC
130b
140b
150b

FIG. 1B

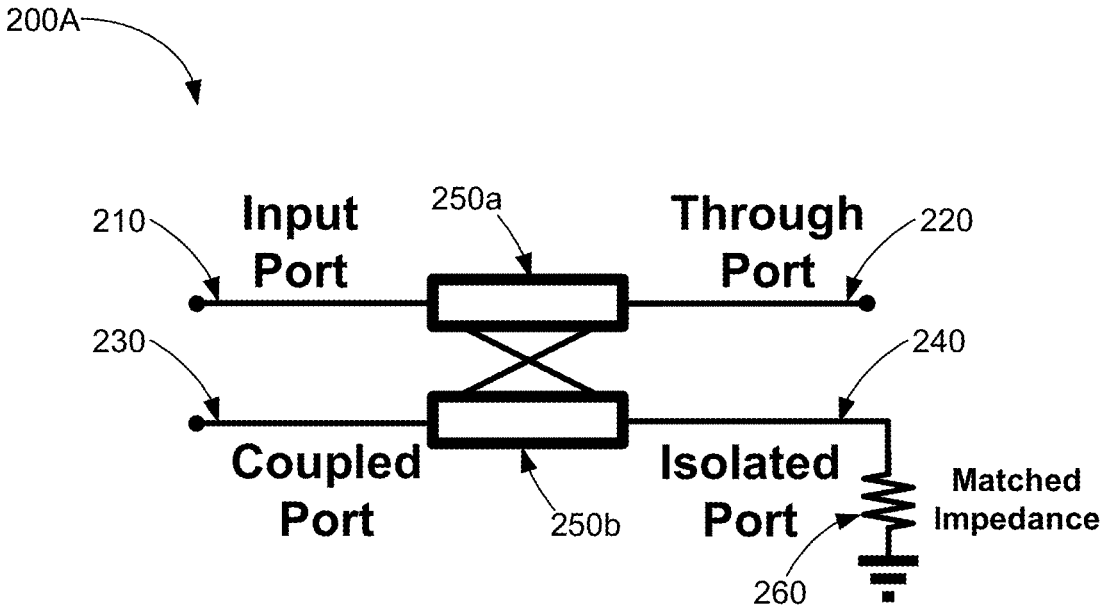

200A
210
Input Port
250a
Through Port
220
230
240
Coupled Port
250b
Isolated Port
Matched Impedance
260

FIG. 2A

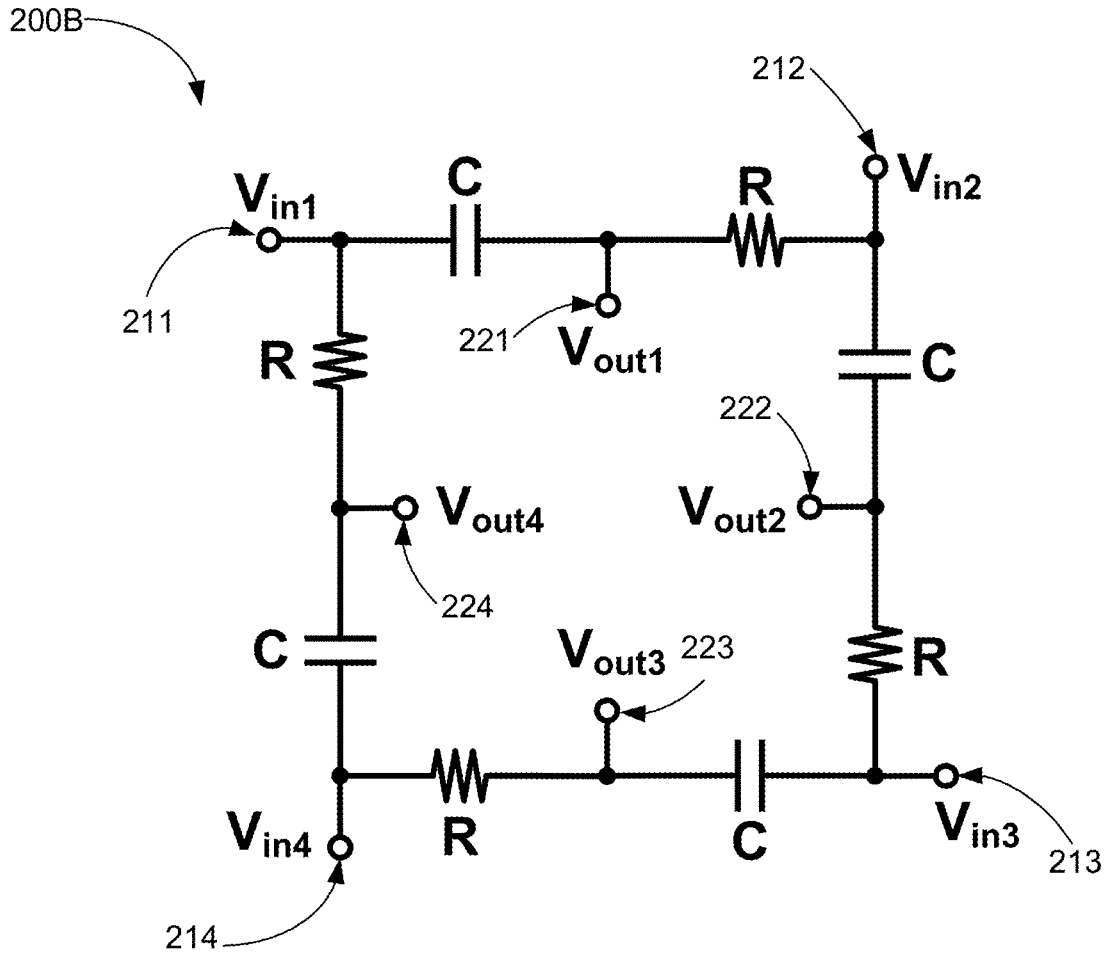

200B
212
V_{in1}
C
R
V_{in2}
211
221
V_{out1}
R
C
222
V_{out4}
V_{out2}
224
C
V_{out3}
223
R
R
C
V_{in4}
V_{in3}
213
214

FIG. 2B

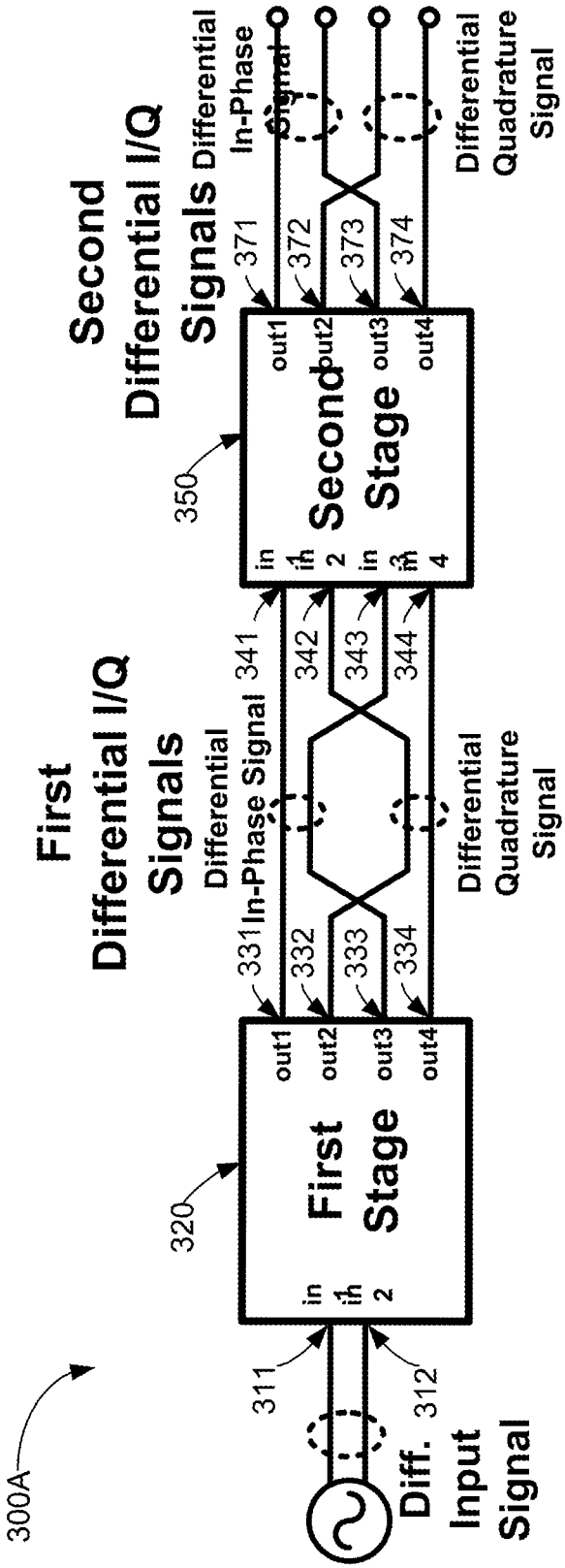

300A
Diff. Input Signal
311
312
320
First Stage
in 1
in 2
out1
out2
out3
out4
First Differential I/Q Signals
Differential In-Phase Signal
331
332
333
334
Differential Quadrature Signal
341
342
343
344
350
Second Stage
Second Differential I/Q Signals
Differential In-Phase Signal
371
372
373
374
Differential Quadrature Signal

FIG. 3A

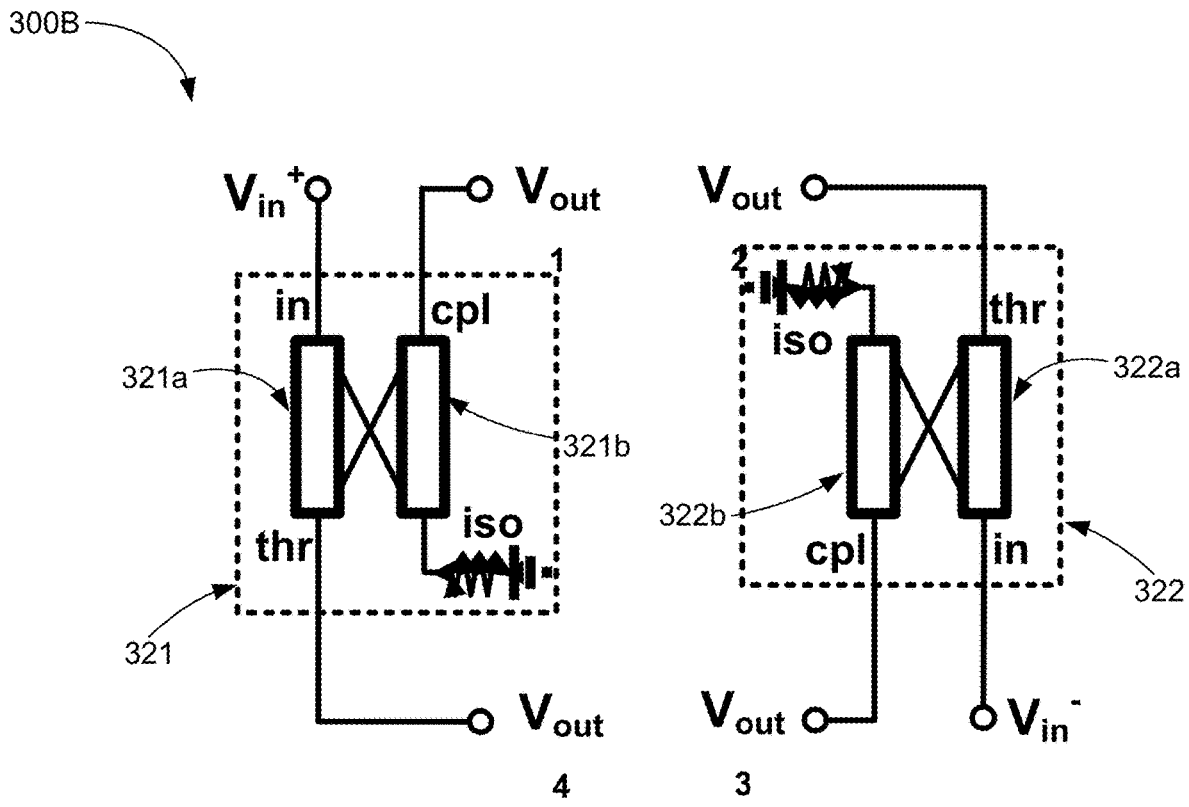

300B
V_{in}^+
V_{out}
1
in
cpl
321a
321b
iso
thr
321
V_{out}
4
V_{out}
2
iso
thr
322a
322b
cpl
in
322
V_{out}
V_{in}^-
3

FIG. 3B

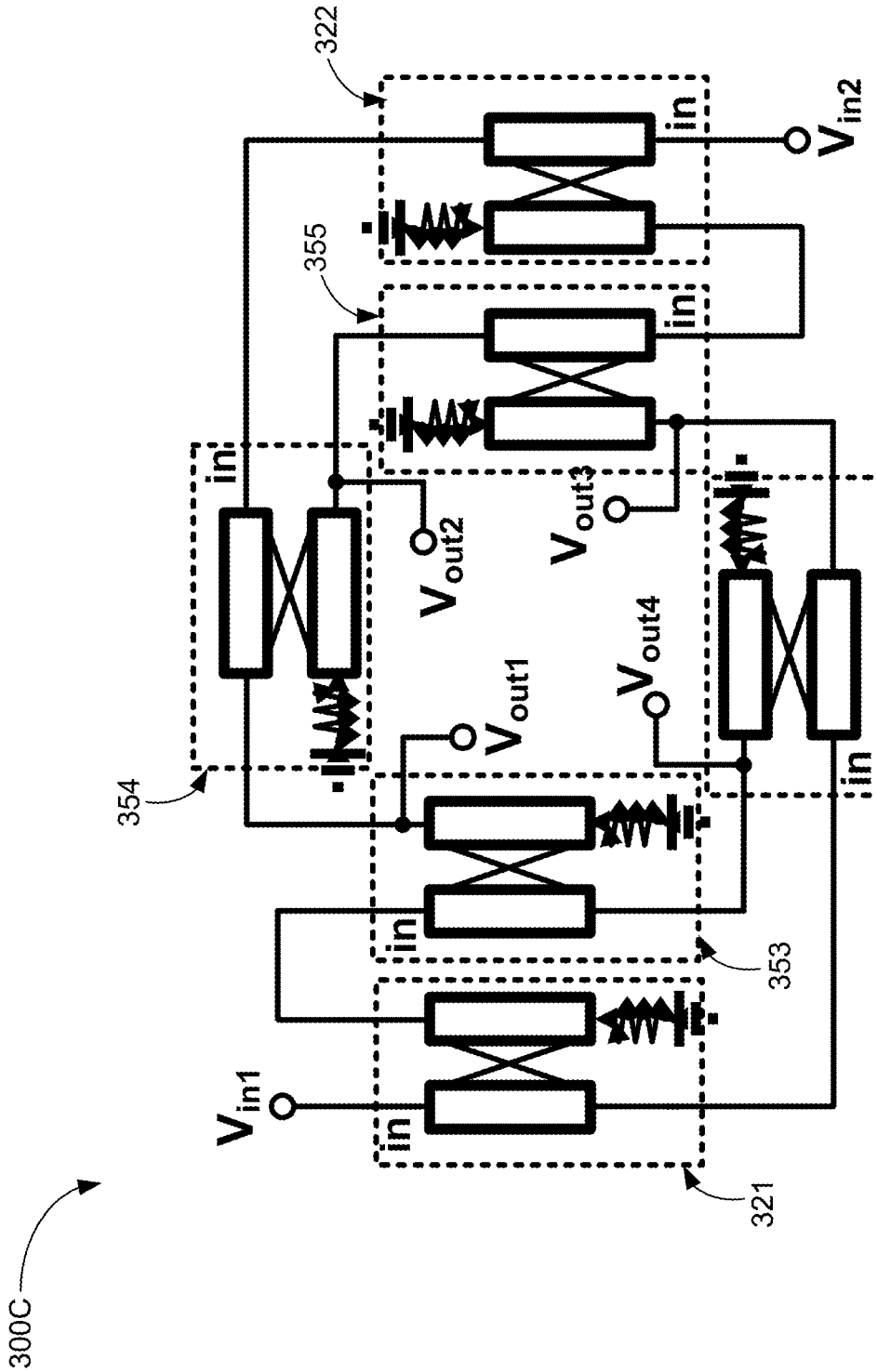

322
355
354
356
353
321
300C
in
V_{in1}
V_{in2}
V_{out1}
V_{out2}
V_{out3}
V_{out4}

FIG. 3C

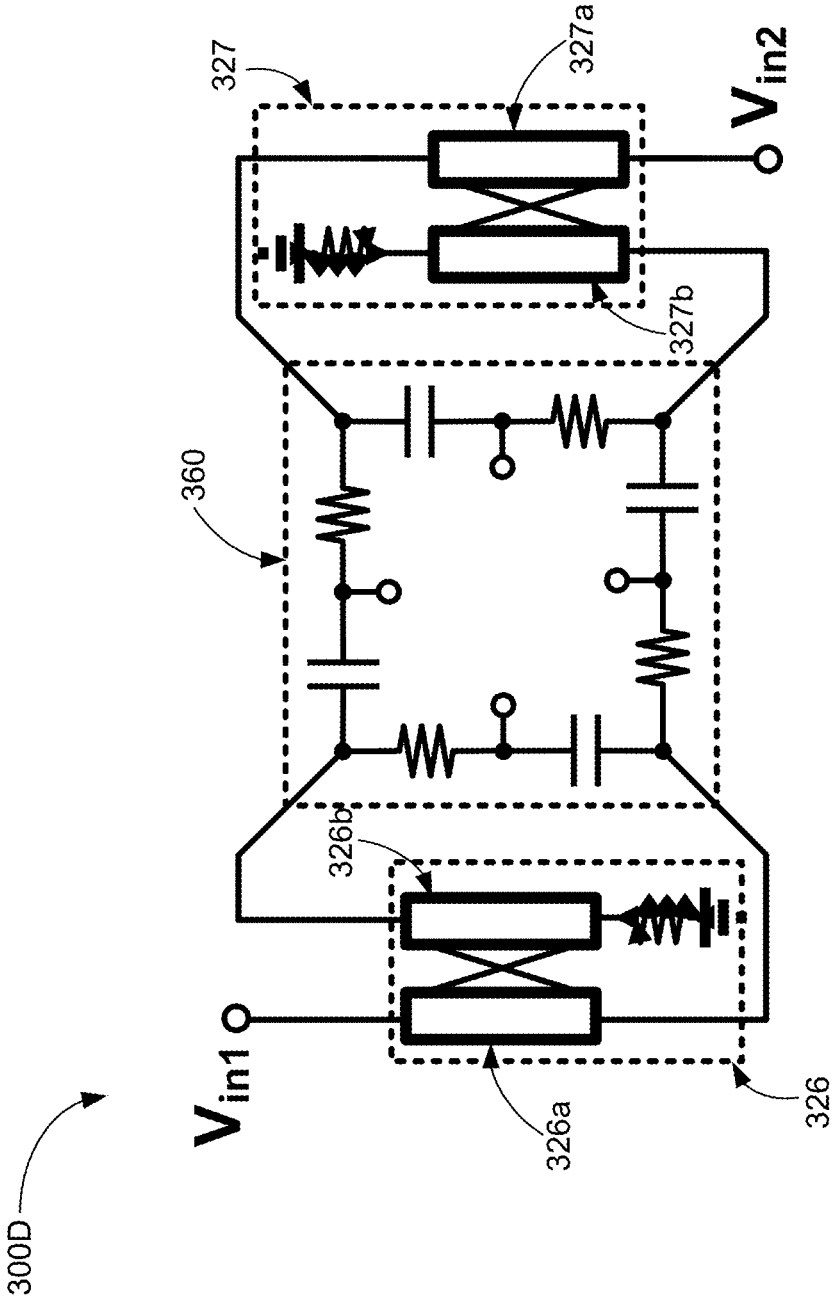


FIG. 3D

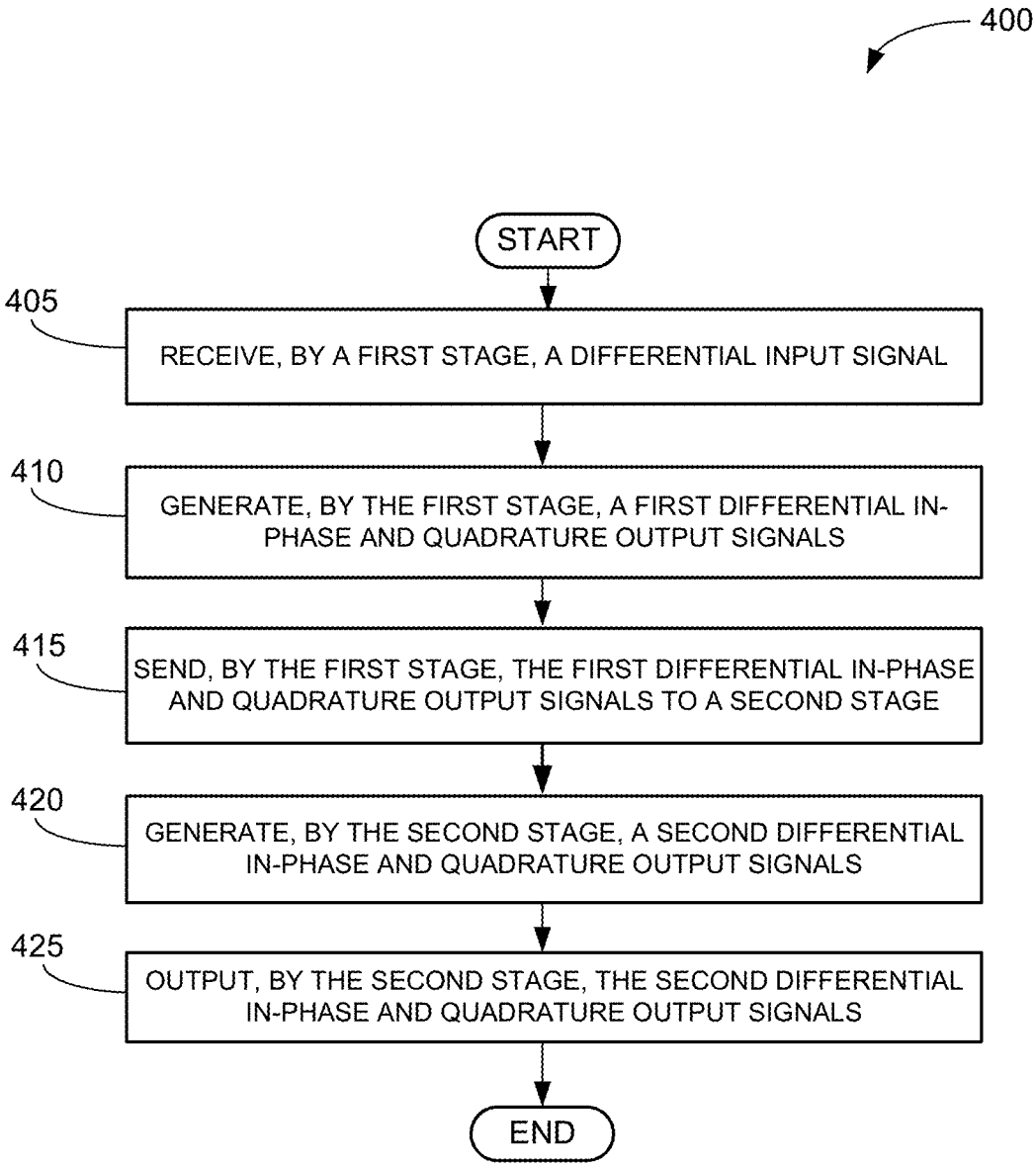

400
START
405
RECEIVE, BY A FIRST STAGE, A DIFFERENTIAL INPUT SIGNAL
410
GENERATE, BY THE FIRST STAGE, A FIRST DIFFERENTIAL IN-PHASE AND QUADRATURE OUTPUT SIGNALS
415
SEND, BY THE FIRST STAGE, THE FIRST DIFFERENTIAL IN-PHASE AND QUADRATURE OUTPUT SIGNALS TO A SECOND STAGE
420
GENERATE, BY THE SECOND STAGE, A SECOND DIFFERENTIAL IN-PHASE AND QUADRATURE OUTPUT SIGNALS
425
OUTPUT, BY THE SECOND STAGE, THE SECOND DIFFERENTIAL IN-PHASE AND QUADRATURE OUTPUT SIGNALS
END

FIG. 4

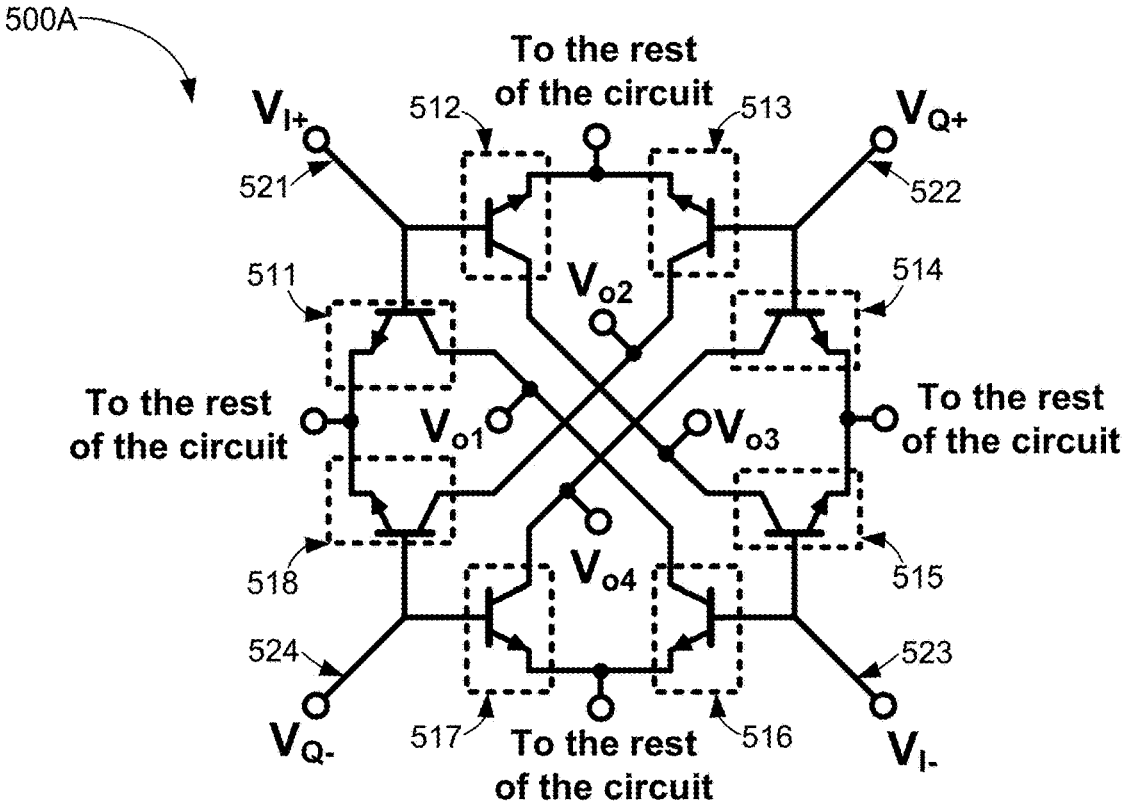

500A
To the rest of the circuit
V_{I+}
512
513
V_{Q+}
521
522
511
V_{o2}
514
To the rest of the circuit
V_{o1}
V_{o3}
To the rest of the circuit
518
V_{o4}
515
524
523
V_{Q-}
517
To the rest of the circuit
516
V_{I-}

FIG. 5A

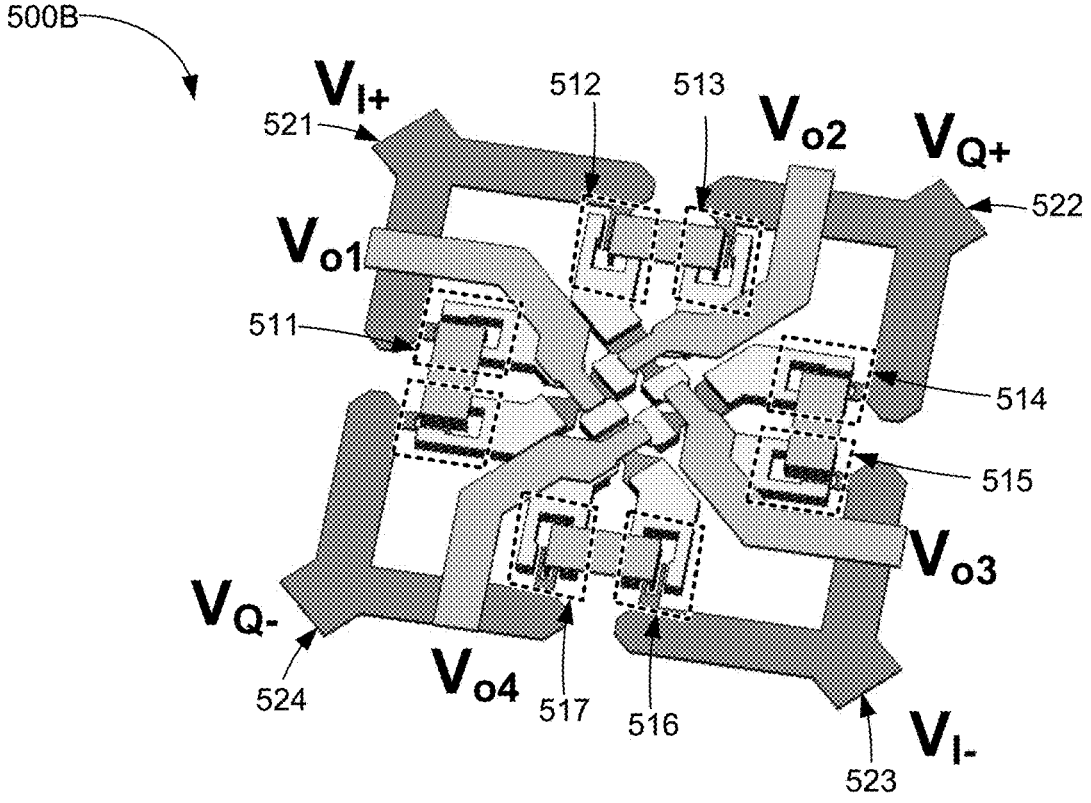

500B
V_{I+}
512
513
V_{o2}
V_{Q+}
521
522
V_{o1}
511
514
515
V_{o3}
V_{Q-}
524
V_{o4}
517
516
523
V_{I-}

FIG. 5B

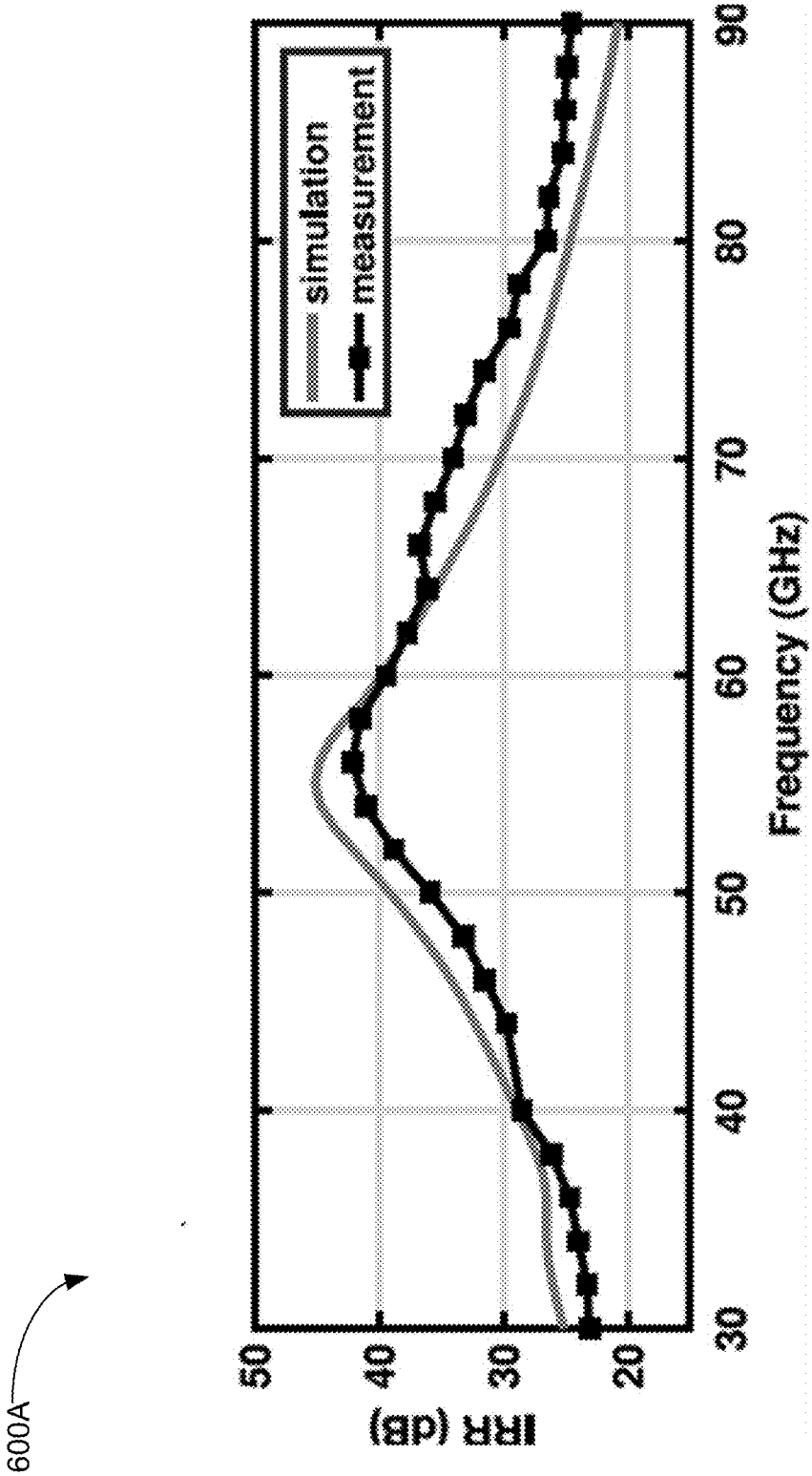

600A
IRR (dB)
50
40
30
20
Frequency (GHz)
30
40
50
60
70
80
90
simulation
measurement

FIG. 6A

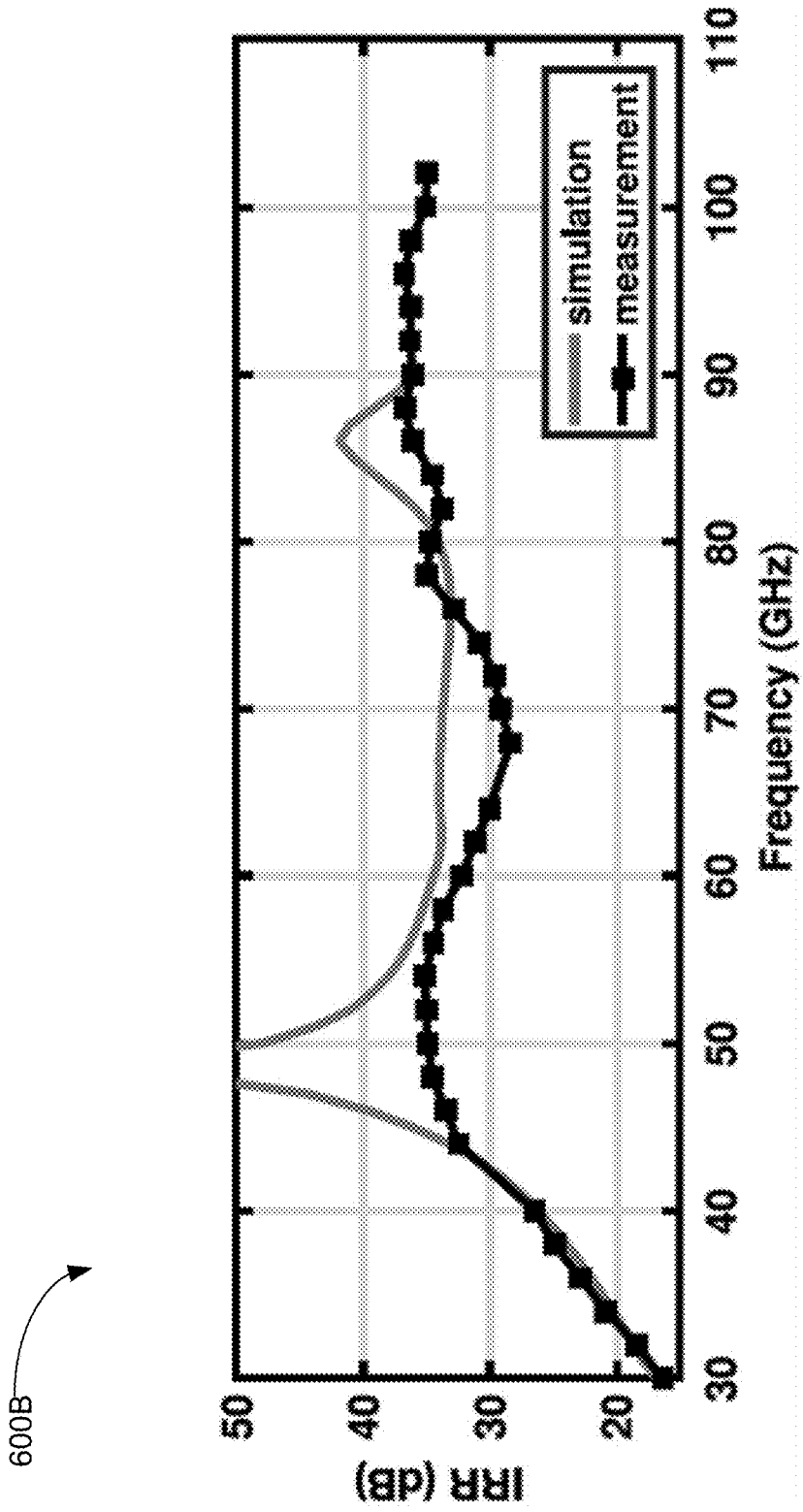

600B
IRR (dB)
50
40
30
20
30
40
50
60
70
80
90
100
110
Frequency (GHz)
simulation
measurement

FIG. 6B

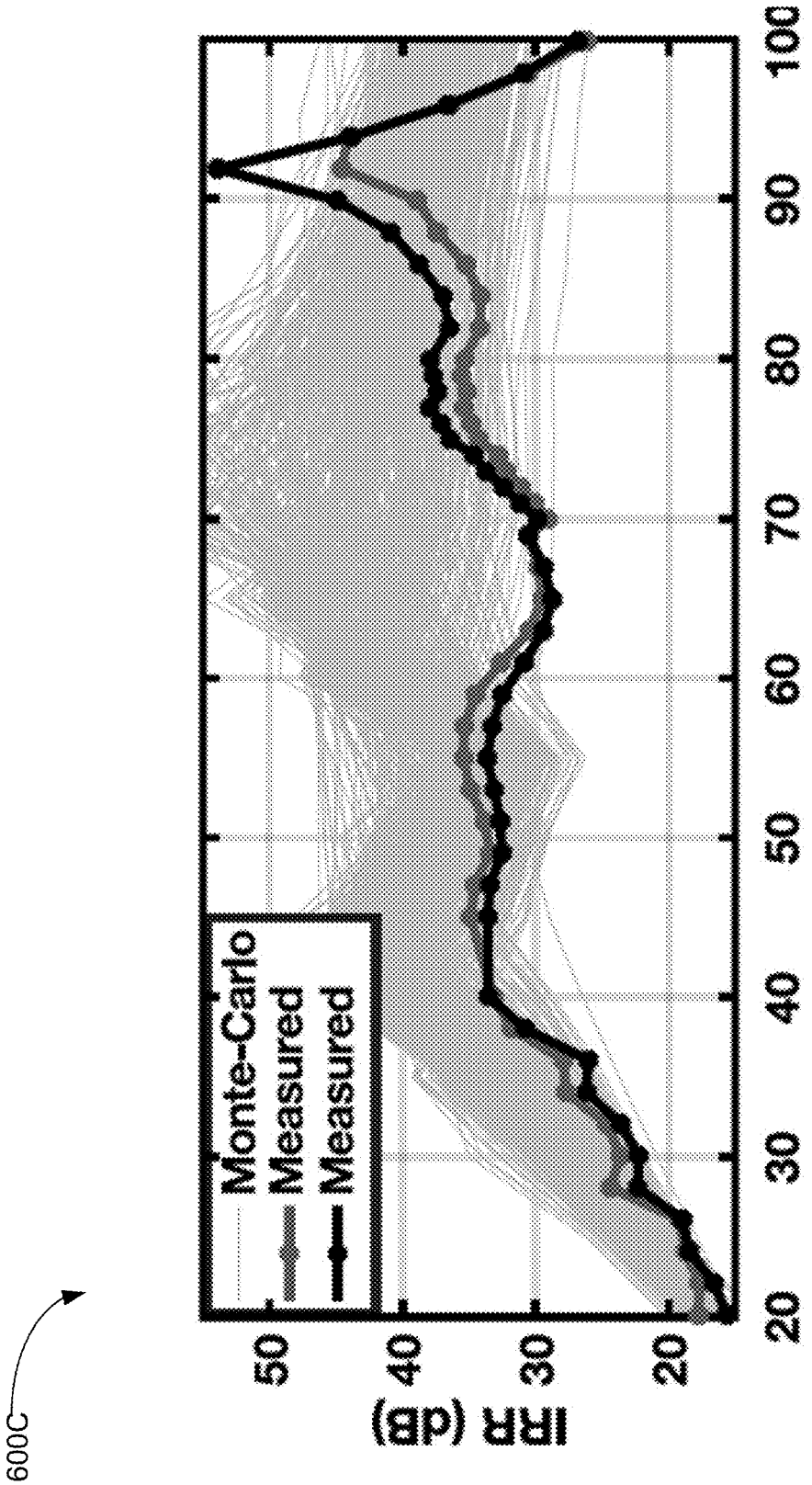

600C
IRR (dB)
50
40
30
20
Frequency (GHz)
20
30
40
50
60
70
80
90
100
Monte-Carlo
Measured
Measured

FIG. 6C

METHODS AND DEVICES FOR IN-PHASE AND QUADRATURE SIGNAL GENERATION

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of, and priority under 35 U.S.C. § 119(e) to, U.S. Provisional Patent Application No. 62/720,851, entitled "A Low-Loss Broadband Quadrature Signal Generation Technique with Symmetric Layout for Millimeter-Wave applications," filed Aug. 21, 2018, the contents of which are hereby incorporated by reference herein in their entirety as if fully set forth below.

FIELD OF THE INVENTION

[0002] The presently disclosed subject matter relates generally to methods and devices for in-phase and quadrature signal generation and, more particularly, to methods and devices for generating in-phase and quadrature signals having reduced amplitude and phase mismatches.

BACKGROUND

[0003] In the last few decades, radio frequency (RF) and millimeter-wave (mm-wave) systems have become popular for imaging, radiometry, automotive radar, and recently for fifth-generation (5G) cellular communications. In these systems, highly balanced in-phase (I) and quadrature (Q) local oscillator (LO) signal generation plays a key role for achieving high data rates and high image rejection ratios (IRRs). FQ signals, also called quadrature signals, are conventionally generated with resistor-capacitor polyphase filters (PPFs), which are lossy, narrowband, and sensitive to process variations. To improve the phase and amplitude matching, PPFs should be cascaded, but this approach may be less attractive at mm-wave frequencies due to the increased insertion loss. Similarly, highly-coupled transformer-based networks can be cascaded to generate low-loss and wideband quadrature signals, but the self-resonance frequency of these transformers are usually in the lower-end of mm-wave frequency range and these transformers cannot be used for high-frequency systems.

[0004] Furthermore, as networks continue to require even higher data rates (multi-Gb/s) for next generation mobile communications, highly accurate in-phase and quadrature (I/Q) signals are needed at mm-wave frequencies. Accordingly, there is a need for improved methods and devices for generating highly accurate I/Q signals.

SUMMARY

[0005] Aspects of the disclosed technology include methods and devices for in-phase (I) and quadrature (Q) signal generation. Consistent with the disclosed embodiments, the methods can include a first stage (e.g., two coupled-line couplers) and a second stage (e.g., four coupled-line couplers or a resistor-capacitor polyphase filter). One exemplary method may include receiving a differential input signal at a first stage. The first stage may generate first differential in-phase and quadrature (I/Q) output signals, which may be based on the differential input signal. The method may further include the first stage sending the first differential I/Q output signals to the second stage. In response, the second stage may generate second differential I/Q output signals, which may be based on the first differential I/Q output signals. The amplitude and phase mismatches of the second differential I/Q output signals may be less than the amplitude and phase mismatches of the first differential I/Q output signals.

[0006] In some embodiments, the second stage may comprise four coupled-line couplers. The isolation port of these coupled-line couplers may be terminated in matched impedances.

[0007] In some embodiments, the second stage may comprise a resistor-capacitor (RC) polyphase filter.

[0008] In some embodiments, the differential input signal may include a first input signal and a second input signal.

[0009] According to some embodiments, the second input signal may have a phase shift of 180 degrees relative to the first input signal.

[0010] In some embodiments, the first stage may include a first input configured to receive the first input signal, and a second input configured to the receive the second input signal.

[0011] In some embodiments, the first differential I/Q output signals may include a first output signal, a second output signal, a third output signal, and a fourth output signal. Further, the second output signal may have a phase shift of ninety degrees relative to the first output signal. Similarly, the fourth output signal may have a phase shift of ninety degrees relative to the third output signal.

[0012] According to some embodiments, the first stage may include a first output configured to send the first output signal, a second output configured to send the second output signal, a third output configured to send the third output signal, and a fourth output configured to send the fourth output signal.

[0013] An exemplary I/Q signal generation system may include a first stage and a second stage. The first stage may comprise two coupled-line couplers. The two coupled-line couplers may receive a differential input signal and generate first differential I/Q output signals, which may be based on the differential input signal. The second stage may comprise a resistor-capacitor polyphase filter or four coupled-line couplers. The coupled-line couplers may include isolation ports that may be terminated in matched impedances. The second stage may be configured to receive the first differential I/Q output signals and generate second differential I/Q output signals. Furthermore, amplitude and phase mismatches of the second differential I/Q output signals may be less than amplitude and phase mismatches of the first differential I/Q output signals.

[0014] In some embodiments, the differential input signal may include a first input signal and a second input signal. The second input signal may have a phase shift of one hundred eighty degrees relative to the first input signal.

[0015] In some embodiments, the first stage may include a first input configured to receive the first input signal. According to some embodiments, the first stage may further include a second input configured to receive the second input signal.

[0016] In some embodiments, the first differential I/Q output signals may include a first output signal, a second output signal, a third output signal, and a fourth output signal. The second output signal may have a phase shift of ninety degrees relative to the first output signal. The third output signal may have a phase shift of ninety degrees relative to the second output signal. The fourth output signal may have a phase shift of ninety degrees relative to the third output signal.

[0017] In some embodiments, the first stage may include a first output configured to send the first output signal, a second output configured to send the second output signal, a third output configured to send the third output signal, and a fourth output configured to send the fourth output signal.

[0018] According to some embodiments, the first, second, third, and fourth output signals may have equal amplitudes and frequencies.

[0019] In some embodiments, the second stage may include a first coupled-line coupler, a second coupled-line coupler, a third coupled-line coupler, and a fourth coupled-line coupler. The isolation ports of the first, second, third, and fourth coupled-line couplers may be terminated in matched impedances.

[0020] In some embodiments, the coupled port of the second coupled-line coupler may be connected to a through port of the first coupled-line coupler.

[0021] In some embodiments, the coupled port of the third coupled-line coupler may be connected to the through port of the second coupled-line coupler.

[0022] In some embodiments, the coupled port of the fourth coupled-line coupler may be connected to the through port of the third coupled-line coupler.

[0023] In some embodiments, the coupled port of the first coupled-line coupler may be connected to the through port of the fourth coupled-line coupler.

[0024] In some embodiments, the quadrature signal generation system may have a symmetrical layout.

[0025] In some embodiments, the quadrature signal generation system may provide for an image rejection ratio of between 29 and 50 dB across a frequency range of 42-102 GHz.

[0026] According to some embodiments, the I/Q signal generation system may be connected to a plurality of transistors. The plurality of transistors may have a symmetrical common-centroid layout. Further, each of the plurality of transistors may have a plurality of interconnects that may have about the same length.

[0027] Further features of the disclosed design, and the advantages offered thereby, are explained in greater detail hereinafter with reference to specific embodiments illustrated in the accompanying drawings, wherein like elements are indicated be like reference designators.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, are incorporated into and constitute a portion of this disclosure, illustrate various implementations and aspects of the disclosed technology, and, together with the description, serve to explain the principles of the disclosed technology. In the drawings:

[0029] FIG. **1**A is a schematic of a receiver frontend block diagram, in accordance with some examples of the present disclosure;

[0030] FIG. **1**B is a schematic of a transmitter frontend block diagram, in accordance with some examples of the present disclosure;

[0031] FIG. **2**A is an image of a coupled-line coupler with port names, where an isolation port of the coupled-line coupler is terminated in a matched impedance, in accordance with some examples of the present disclosure;

[0032] FIG. **2**B is an image of a resistor-capacitor polyphase filter, in accordance with some examples of the present disclosure;

[0033] FIG. **3**A is an image of a two-stage I/Q signal generation system, in accordance with some examples of the present disclosure;

[0034] FIG. **3**B is an image of the first stage of FIG. **3**A showing two coupled-line couplers, where isolation ports of the two coupled-line couplers are terminated in matched impedances, in accordance with some examples of the present disclosure;

[0035] FIG. **3**C is an image of a I/Q signal generation system having two coupled-line couplers in a first stage and four coupled-line couplers in a second stage, where the isolation ports of coupled-line couplers are terminated in matched impedances, in accordance with some examples of the present disclosure;

[0036] FIG. **3**D is an image of another a quadrature signal generation system having two coupled-line couplers in the first stage and a resistor-capacitor (RC) polyphase filter in the second stage, where the isolation port of coupled-line couplers are terminated in matched impedances, in accordance with some examples of the present disclosure;

[0037] FIG. **4** is a flowchart illustrating a method for quadrature signal generation, in accordance with some examples of the present disclosure;

[0038] FIG. **5**A is a schematic of the switching transistors of a Gilbert mixer to which an I/Q signal generation system outputs may be connected, in accordance with some examples of the present disclosure;

[0039] FIG. **5**B is an image of a floorplan and interconnects of switching transistors of a Gilbert mixer to which the I/Q signal generation system outputs may be connected, in accordance with some examples of the present disclosure;

[0040] FIGS. **6**A-C are graphs illustrating the image rejection ratios for various I/Q signal generation systems, in accordance with some examples of the present disclosure.

DETAILED DESCRIPTION

[0041] Some implementations of the disclosed technology will be described more fully with reference to the accompanying drawings. This disclosed technology can be embodied in many different forms, however, and should not be construed as limited to the implementations set forth herein. The components described hereinafter as making up various elements of the disclosed technology are intended to be illustrative and not restrictive. Many suitable components that would perform the same or similar functions as components described herein are intended to be embraced within the scope of the disclosed electronic devices and methods. Such other components not described herein can include, but are not limited to, for example, components developed after development of the disclosed technology.

[0042] It is also to be understood that the mention of one or more method steps does not imply that the methods steps must be performed in a particular order or preclude the presence of additional method steps or intervening method steps between the steps expressly identified.

[0043] Reference will now be made in detail to exemplary embodiments of the disclosed technology, examples of which are illustrated in the accompanying drawings and disclosed herein. Wherever convenient, the same references numbers will be used throughout the drawings to refer to the same or like parts.

[0044] FIG. **1**A illustrates the block diagram of an example receiver frontend **100**A. The receiver frontend **100**A may include a receive path for receiving radio frequency (RF) and millimeter-wave signals from an antenna **110**. The received signal from the antenna **110** may be amplified with a low-noise amplifier (LNA) **120** and passed through two mixers **130***a* and **130***b* for down-conversion. After down-converting the received signals in the mixers **130***a* and **130***b*, the baseband signals may be filtered using bandpass filters (BPF) **140***a* and **140***b* and delivered to analog-to-digital converters (ADCs) **150***a* and **150***b*. The mixer **130***a* may multiply the output signal of the LNA **120** with differential in-phase (I) local oscillator (LO) signals **160***a*. Similarly, the mixer **130***b* may multiply the output signal of the LNA **120** with differential quadrature (Q) local oscillator (LO) signals **160***b*. The differential in-phase LO signals **160***a* may have the same amplitude as the differential quadrature LO signals **160***b*, but the differential in-phase signals may have a phase shift of ninety degrees relative to the differential quadrature LO signals. This differential I and Q signals **160***a* and **160***b* may be generated with an I/Q signal generation system **170**. The I/Q signal generation system **170** may have one differential input **175** to receive continuous wave sinusoidal signals from a frequency synthesizer **180**. The I/Q signal generation system outputs will deliver in-phase and quadrature signals (**160***a* and **160***b*) to the LO ports (**131***a* and **131***b*) of the mixer **130***a* and **130***b*, respectively. The mixers **130***a* and **130***b* may include switching transistors to chop the received RF signal with LO signals to perform frequency conversion. Then, LO ports **131***a* and **131***b* of the mixer may be connected to the switching transistors **132***a* and **132***b* inside the mixer.

[0045] FIG. **1**B illustrates the block diagram of an example transmitter frontend **100**B. The transmitter frontend **100**B may include a transmit path for receiving radio frequency (RF) and millimeter-wave signals from an antenna **110**. T base-band signals may be generated with digital-to-analog converters (DACs) **150***a* and **150***b*. These base-band signals may be filtered using bandpass filters (BPF) **140***a* and **140***b* and passed through two mixers **130***a* and **130***b* for up-conversion. The Up-converted signal may be amplified with a power amplifier (PA) **120** and delivered to the antenna **110**. The mixer **130***a* may multiply the output signal of the BPF **140** with differential in-phase (I) local oscillator (LO) signals **160***a*. Similarly, the mixer **130***b* may multiply the output signal of the BPF **140** with differential quadrature (Q) local oscillator (LO) signals **160***b*. The differential in-phase LO signals **160***a* may have the same amplitude as the differential quadrature LO signals **160***b*, but the differential in-phase signals may have a phase shift of ninety degrees relative to the differential quadrature LO signals. The differential I and Q signals **160***a* and **160***b* may be generated with an I/Q signal generation system **170**. The I/Q signal generation system **170** may have one differential input **175** to receive continuous wave sinusoidal signals from a frequency synthesizer **180**. The I/Q signal generation system outputs may deliver in-phase and quadrature signals, **160***a* and **160***b*, to the LO ports **131***a* and **131***b* of the mixer **130***a* and **130***b*, respectively. The mixers **130***a* and **130***b* may include switching transistors to chop the received RF signal with LO signals to perform frequency conversion. Then, LO ports **131***a* and **131***b* of the mixer may be connected to the switching transistors **132***a* and **132***b* inside the mixer.

[0046] FIG. **2**A illustrates the schematic of a coupled-line coupler **200**A which may be conventionally used to generate in-phase and quadrature signals. The coupled-line coupler **200**A may have an input port **210**, a through port **220**, a coupled port **230**, and an isolation port **240**. The coupled-line coupler may consist of a pair of transmission lines **250***a* and **250***b*. When a signal is applied to the input port **210** of the coupled-line coupler, the coupled-line coupler may deliver a fraction of the input signal to the through port **220** and the rest of the input signal to the coupled port **230**. Ideally, no power is delivered to the isolation port **240**. However, this port may be terminated in a matched impedance **260** (e.g., a resistor) to minimize the reflections.

[0047] FIG. **2**B illustrates the schematic of an example resistor-capacitor (RC) polyphase filter (PPF) **200**B which may be conventionally used for in-phase and quadrature signal generation. The RC PPF **200**B may have four inputs **211**, **212**, **213**, and **214**, and it may have four outputs **221**, **222**, **223**, and **224**. The operation of a RC PPF is explained in detail in a paper by Behbahani, F. and Kishigami, Y. and Leete, J. and Abidi, A. A., titled, "CMOS Mixers and Polyphase Filters for Large Image Rejection," published in the IEEE Journal of Solid-State Circuits, vol. 36, no. 6, pp. 873-887, June 2001. Several stages of RC PPFs **200**B may be cascaded to generate broadband I/Q signals, which may occur at the expense of high insertion loss. At millimeter-wave frequencies, the interconnects of the RC PPF **200**B may introduce phase shift and may degrade the performance of the PPF. The effects of the interconnects are analyzed in detail by M. Frounchi and J. D. Cressler, entitled "Dual-Band Millimeter-Wave Quadrature LO Generation with a Common-Centroid Floorplan," published in IEEE Transactions on Circuits and Systems II: Express Briefs.

[0048] FIG. **3**A shows a block diagram **300**A of an I/Q signal generation system **170**, such as the one shown in FIGS. **1**A-B, having two stages. The first stage **320** may receive a differential input signal, which may include a first input signal and a second input signal. Further, the second input signal **312** may have a phase shift of one-hundred-eighty degrees relative to the first input signal. The first stage may also include a first input **311** that may receive the first input signal. Also, the first stage may include a second input **312** that may receive the second input signal. The first stage may then generate first differential I/Q output signals, which may include a first output signal, a second output signal, a third output signal, and a fourth output signal. The output signals may be based on the input differential signal and the output signals may have the following phase shifts: the second output signal may have a phase shift of ninety degrees relative to the first output signal; the third output signal may have a phase shift of ninety degrees relative to the second output signal; and the fourth output signal may have a phase shift of ninety degrees relative to the third output signal. The first stage may also include a first output **331**, a second output **332**, a third output **333**, and a fourth output **334**. The first output **331**, the second output **332**, the third output **333**, and the fourth output **334** may send the first output signal, the second output signal, the third output signal, and the fourth output signal, respectively. The first output signal, second output signal, third output signal, and fourth output signal may have equal amplitudes and frequencies. Each of the output signals (first, second, third, and fourth output signal) may be sent to the second stage **350** as the first differential I/Q output signals.

[0049] The second stage **350** of the I/Q signal generation system **300**A may receive the first differential I/Q signals, which may include a first output signal, a second output signal, a third output signal, and a fourth output signal. Further, the output signals may have the following phase shifts: the second output signal may have a phase shift of ninety degrees relative to the first output signal; the third output signal may have a phase shift of ninety degrees relative to the second output signal; and the fourth output signal may have a phase shift of ninety degrees relative to the third output signal. The second stage may also include a first input **341** that may receive the first input signal, a second input **342** that may receive the second input signal, a third input **343** that may receive the third input signal, and a fourth input **344** that may receive the fourth input signal. The second stage may then generate second differential I/Q output signals, which may include a first output signal, a second output signal, a third output signal, and a fourth output signal. The second differential I/Q output signals may be based on the first differential I/Q signals and they may have the following phase shifts: the second output signal may have a phase shift of ninety degrees relative to the first output signal; the third output signal may have a phase shift of ninety degrees relative to the second output signal; and the fourth output signal may have a phase shift of ninety degrees relative to the third output signal. The second stage may also include a first output **371**, a second output **372**, a third output **373**, and a fourth output **374**. The first output **371**, the second output **372**, the third output **373**, and the fourth output **374** may send the first output signal, the second output signal, the third output signal, and the fourth output signal, respectively. The first output signal, second output signal, third output signal, and fourth output signal may have equal amplitudes and frequencies. The amplitude and phase mismatches of the second differential I/Q output signal may be less than the amplitude and phase mismatches of the first differential I/Q output signal.

[0050] FIG. **3**B shows an image of the first stage **320** of the I/Q signal generation network **300**A. The first stage may include a first coupled-line coupler **321** and a second coupled-line coupler **322**. The first coupled-line coupler **321** may include a pair of transmission lines **321***a* and **321***b*. Similarly, the second coupled-line coupler **322** may include a pair of transmission lines **322***a* and **322***b*. The input ports of the coupled-line couplers (**321** and **322**) may be connected to the inputs **311** and **312**; the through ports of the coupled-line couplers (**321** and **322**) may be connected to outputs **332** and **334**; the coupled ports of the coupled-line couplers (**321** and **322**) may be connected to outputs **331** and **333**; and the isolated ports of the coupled-line couplers (**321** and **322**) may be terminated in matched impedances.

[0051] FIG. **3**C illustrates both stages of an I/Q signal generation system **300**C. The first stage may include a first coupled-line coupler **321** and a second coupled-line coupler **322**. The second stage may include a third coupled-line coupler **353**, a fourth coupled-line coupler **354**, a fifth coupled-line coupler **355**, a sixth coupled-line coupler **356**. The I/Q signal generation system **300**C may provide differential in-phase and quadrature signals at millimeter-wave frequencies that may eliminate the need for calibration and tuning, and further may help achieve multi-Gb/s data rates. Also, the quadrature signal generation system **300**C may have a zero power consumption, such that it does not require a feedback system. Additionally, the I/Q signal generation system **300**C may be scalable based at least in part on the length of the coupled-line couplers (e.g., **321**, **322**, **353**, **354**, **355**, and **356**). The design of the I/Q signal generation system **300**C may allow for platform-independence, which may allow it to be implemented in various integrated circuits technology platform. Other advantages of the I/Q signal generation system **300**C may include reduced sensitivity to the fabrication process, passive and linear operations, a small foot-print and/or a lower fabrication cost.

[0052] In the second stage of I/Q signal generation system **300**C, a coupled port of the third coupled-line coupler **353** may be connected to a through port of the fourth coupled-line coupler **354**, a coupled port of the fourth coupled-line coupler **354** may be connected to a through port of the fifth coupled-line coupler **355**, a coupled port of the fifth coupled-line coupler **355** may be connected to a through port of the sixth coupled-line coupler **356**, and a coupled port of the sixth coupled-line coupler **356** may be connected to a through port of the third coupled-line coupler **353**. The second stage may generate a second differential I/Q output signals. Further, the amplitude and phase mismatches of the second differential I/Q output signals may be less than the amplitude and phase mismatches of the first differential I/Q output signals. Cascading the coupled-line couplers, as depicted in FIG. **3**C, may help lessen the amplitude and phase mismatches of the second differential I/Q output signals.

[0053] As shown in FIG. **3**C, the quadrature signal generation system **300**C may have a symmetrical layout, which may reduce the sensitivity of the phase and amplitude matching to loading capacitance. Also, the I/Q signal generation system **300**C may provide for an image rejection ratio of between 29 and 50 dB across a frequency range of 42-102 GHz.

[0054] FIG. **3**D depicts a quadrature signal generation system **300**D having two coupled-line couplers (first coupled-line coupler **326** (**326***a* and **326***b*) and second coupled-line coupler **327** (**327***a* and **327***b*)) in the first stage and a resistor-capacitor (RC) polyphase filter **360** in the second stage. The I/Q signal generation system **300**D may have many or all the advantages of the I/Q signal generation system **300**C, which may be provided at least in part by a symmetrical layout. Further, the first coupled-line coupler **326** and the second coupled-line coupler **327** may be substantially similar or the same as the first coupled-line coupler **321** and the second coupled-line coupler **322**, respectively, of FIG. **3**C. Therefore, the first coupled-line coupler **326** may include a pair of transmission lines **326***a* and **326***b*. Similarly, the second coupled-line coupler **327** may include a pair of transmission lines **327***a* and **327***b*. The first stage may include a first input **311** and a second input **312**, which may receive a first input signal and second input signal, respectively. Together, the first input signal and the second input signal may comprise the differential input signal. As mentioned above, the second input signal may have a phase shift of one hundred and eighty degrees relative to the first input signal. Also, similar to the first stage described in FIG. **3**B, the first stage may generate and send the first differential I/Q output signals (the first output signal, the second output signal, the third output signal, and the fourth output signal) to the second stage, which may have the phase shifts according to the requirements set forth in FIG. **3**C.

[0055] The second stage (e.g., RC polyphase filter **360**) may receive the first differential I/Q output signals from the

first stage and generate a second differential I/Q output signals that has amplitude and phase mismatches less than the first differential I/Q output signals. The second stage may have four outputs; first output **371**, second output **372**, third output **373**, and fourth output **374**, which may send the first output signal, the second output signal, the third output signal, and the fourth output signal, respectively. Of course, the first, second, third, and fourth output signals may have equal amplitudes and frequencies.

[0056] FIG. **4** illustrates an example flow chart of a method for I/Q signal generation. The method **400** can be implemented by the quadrature generation system **300**C and the I/Q generation system **300**D. At **405**, the first stage (e.g., coupled-line coupler **321** and **322**, or coupled-line couplers **326** and **327**) may receive a differential input signal. As mentioned above, the differential input signal may include a first input signal and a second input signal, which may be received at a first input (e.g., **311**) and second input (e.g., **312**), respectively. Further, the second input signal may have a phase shift of one hundred eighty degrees relative to the first input signal. At **410**, the first stage may generate a first differential I/Q output signals based on the differential input signal. The first differential I/Q output signals may have four output signals (first, second, third, and fourth output signal). At **415**, the first differential output signal may be sent from the first stage and to the second stage, i.e., each of the four outputs (e.g., **331**, **332**, **333**, and **334**) of the first stage sends an output signal to the second stage. The second stage may be the RC polyphase filter **360** or the four coupled-line couplers (**353**, **353**, **355**, and **356**). At **420**, the second stage may generate a second differential I/Q output signals, which may have a reduced amplitude and phase mismatches compared to the first differential I/Q signals. At, **425**, the second stage may output the second differential I/Q output signals.

[0057] FIG. **5**A shows the schematic **500**A of an exemplary mixer (**130***a* and **130***b*), which may be implemented with double-balanced topology and may include eight switching transistors **511**,**512**, **513**, **514**, **515**, **516**, **517**, and **518** with four I/Q local oscillator (LO) inputs (e.g., **160***a* and **160***b* in FIG. **1**). The first I/Q LO input **521** may be connected to the Base of switching transistors **511** and **512**; the second I/Q LO input **522** may be connected to the Base of switching transistors **513** and **514**; the third I/Q LO input **523** may be connected to the Base of switching transistors **515** and **516**; and the fourth I/Q LO input **524** may be connected to the Base of switching transistors **517** and **518**.

[0058] FIG. **5**B shows a common-centroid symmetric floorplan **500**B of the eight switching transistors **511**,**512**, **513**, **514**, **515**, **516**, **517**, and **518** with all interconnects. The first I/Q LO input **521** may be connected to the Base of switching transistors **511** and **512**; the second I/Q LO input **522** may be connected to the Base of switching transistors **513** and **514**; the third I/Q LO input **523** may be connected to the Base of switching transistors **515** and **516**; and the fourth I/Q LO input **524** may be connected to the Base of switching transistors **517** and **518**.

[0059] FIGS. **6**A-C show the image rejection ratios of various mixers (e.g., **130***a* and **130***b* in FIG. **1**) where the differential I/Q signals were generated with systems **300**C and **300**D. The image rejection ratio of mixers may be a direct function of the phase and amplitude matching of the quadrature signals and it is calculated by

$$IRR = \frac{1 + 2\alpha\cos(\theta) + \alpha^2}{1 - 2\alpha\cos(\theta) + \alpha^2}$$

Where α is the amplitude error, and θ is the phase error.

[0060] Throughout the specification and the claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The term "or" is intended to mean an inclusive "or." Further, the terms "a," "an," and "the" are intended to mean one or more unless specified otherwise or clear from the context to be directed to a singular form.

[0061] In this description, numerous specific details have been set forth. It is to be understood, however, that implementations of the disclosed technology can be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description. References to "one embodiment," "an embodiment," "some embodiments," "example embodiment," "various embodiments," "one implementation," "an implementation," "example implementation," "various implementations," "some implementations," etc., indicate that the implementation(s) of the disclosed technology so described can include a particular feature, structure, or characteristic, but not every implementation necessarily includes the particular feature, structure, or characteristic. Further, repeated use of the phrase "in one implementation" does not necessarily refer to the same implementation, although it can.

[0062] As used herein, unless otherwise specified the use of the ordinal adjectives "first," "second," "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

[0063] While certain implementations of the disclosed technology have been described in connection with what is presently considered to be the most practical and various implementations, it is to be understood that the disclosed technology is not to be limited to the disclosed implementations, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims. Although specific terms are employed herein, they are used in a generic and descriptive sense only and not for purposes of limitation.

[0064] This written description uses examples to disclose certain implementations of the disclosed technology, including the best mode, and also to enable any person skilled in the art to practice certain implementations of the disclosed technology, including making and using any devices or systems and performing any incorporated methods. The patentable scope of certain implementations of the disclosed technology is defined in the claims, and can include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal language of the claims.

What is claimed is:

1. An in-phase and quadrature (I/Q) signal generation system comprising:

a first stage comprising two coupled-line couplers configured to receive a differential input signal and generate first differential I/Q output signals; and

a second stage configured to receive the first differential I/Q output signals and generate second differential I/Q output signals, wherein amplitude and phase mismatches of the second differential I/Q output signals are less than the amplitude and phase mismatches of the first differential I/Q output signals.

2. The system of claim **1**, wherein the differential input signal comprises a first input signal and a second input signal, wherein the second input signal has a phase shift of 180 degrees relative to the first input signal.

3. The system of claim **2**, wherein the first stage further comprises:

a first input configured to receive the first input signal; and

a second input configured to receive the second input signal.

4. The system of claim **1**, wherein the first differential I/Q output signals comprise:

a first output signal,

a second output signal having a phase shift of ninety degrees relative to the first output signal,

a third output signal having a phase shift of ninety degrees relative to the second output signal, and

a fourth output signal having a phase shift of ninety degrees relative to the third output signal.

5. The system of claim **4**, wherein the first stage further comprises:

a first output configured to send the first output signal;

a second output configured to send the second output signal;

a third output configured to send the third output signal; and

a fourth output configured to send the fourth output signal.

6. The system of claim **4**, wherein the first, second, third, and fourth output signals have about equal amplitudes and frequencies.

7. The system of claim **1**, wherein the second stage comprises:

a first coupled-line coupler;

a second coupled-line coupler;

a third coupled-line coupler; and

a fourth coupled-line coupler.

8. The system of claim **7**, wherein

a coupled port of the second coupled-line coupler is connected to a through port of the first coupled-line coupler;

a coupled port of the third coupled-line coupler is connected to a through port of the second coupled-line coupler;

a coupled port of the fourth coupled-line coupler is connected to a through port of the third coupled-line coupler; and

a coupled port of the first coupled-line coupler is connected to a through port of the fourth coupled-line coupler.

9. The system of claim **1**, wherein the second stage comprises a resistor-capacitor (RC) polyphase filter.

10. The system of claim **1**, wherein the I/Q signal generation network has a symmetrical layout.

11. The system of claim **1**, wherein the I/Q signal generation system provides for an image rejection ratio of between 29 and 50 dB across a frequency range of 42-102 GHz.

12. The system of claim **1**, further comprising a plurality of transistors having a symmetrical common-centroid layout, wherein each of the plurality of transistors comprises a plurality of interconnects having about the same length.

13. An in-phase and quadrature signal generation system comprising:

a first stage comprising two first coupled-line couplers configured to receive a differential input signal and generate first differential I/Q output signals; and

a second stage comprising four second coupled-line couplers configured to receive the first differential I/Q output signals and generate second differential I/Q output signals, wherein amplitude and phase mismatches of the second differential I/Q output signals are less than amplitude and phase mismatches of the first differential I/Q output signals.

14. The system of claim **13**, wherein the differential input signal comprises a first input signal and a second input signal, wherein the second input signal has a phase shift of 180 degrees relative to the first input signal.

15. The system of claim **14**, wherein the first stage further comprises:

a first input configured to receive the first input signal; and

a second input configured to receive the second input signal.

16. The system of claim **13**, wherein the first differential I/Q output signals comprises:

a first output signal,

a second output signal having a phase shift of 90 degrees relative to the first output signal,

a third output signal having a phase shift of 90 degrees relative to the second output signal, and

a fourth output signal having a phase shift of 90 degrees relative to the third output signal.

17. The system of claim **16**, wherein the first stage further comprises:

a first output configured to send the first output signal;

a second output configured to send the second output signal;

a third output configured to send the third output signal; and

a fourth output configured to send the fourth output signal.

18. A method for I/Q signal generation comprising:

receiving, by a first stage comprising two first coupled-line couplers, a differential input signal;

generating, by the first stage, first differential I/Q output signals;

sending, by the first stage, the first differential I/Q output signals to a second stage;

generating, by the second stage, second differential I/Q output signals, wherein amplitude and phase mismatches of the second differential I/Q output signals are less than the amplitude and phase mismatches of the first differential I/Q output signal; and

outputting, by the second stage, the second differential I/Q output signals.

19. The method of claim **18**, wherein the second stage comprises four coupled-line couplers or a resistor-capacitor (RC) polyphase filter.

20. The method of claim **18**,
wherein the differential input signal comprises:
a first input signal and a second input signal, wherein the second input signal has a phase shift of 180 degrees relative to the first input signal;
wherein the first stage further comprises:
a first input configured to receive the first input signal, and
a second input configured to receive the second input signal;
wherein the first differential I/Q output signals comprise:
a first output signal,
a second output signal having a phase shift of 90 degrees relative to the first output signal,
a third output signal having a phase shift of 90 degrees relative to the second output signal, and
a fourth output signal having a phase shift of 90 degrees relative to the third output signal; and
wherein the first stage further comprises:
a first output configured to send the first output signal;
a second output configured to send the second output signal;
a third output configured to send the third output signal; and
a fourth output configured to send the fourth output signal.

* * * * *