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(54) **MEMORY DEVICE, CONTROL METHOD FOR THE SAME, CONTROL PROGRAM FOR THE SAME, MEMORY CARD, CIRCUIT BOARD AND ELECTRONIC EQUIPMENT**

SPEICHERBAUSTEIN, STEUERVERFAHREN DAFÜR, STEUERPROGRAMM DAFÜR, SPEICHERKARTE, LEITERPLATTE UND ELEKTRONISCHE GERÄTE

DISPOSITIF MÉMOIRE, PROCÉDÉ ET PROGRAMME DE COMMANDE, CORRESPONDANTS, CARTE MÉMOIRE, CARTE DE CIRCUITS IMPRIMÉS ET DISPOSITIF ÉLECTRONIQUE

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EP 2 003 568 B1

Description

[Technical Field]

[0001] The present invention relates to a memory that is used for data storage in an electronic apparatus such as a personal computer (PC), and, more particularly, to a memory device having an interface function, a control method for the memory device, a control program for the memory device, a memory card, a circuit board and electronic equipment.

[Background Art]

[0002] A PC is provided with such JEDEC (Joint Electron Device Engineering Council) standard memories as a SDRAM (Synchronous Dynamic Random Access Memory) and DDR-SDRAM (Double Data Rate-SDRAM).

[0003] With respect to such a memory, patent document 1 discloses a memory controller that includes a plurality of programmable timing registers that can be programmed to store timing data fit to a memory device. Patent Document 2 discloses a memory card that incorporates therein a microprocessor chip and a nonvolatile memory chip that are connected to each other via an internal card bus, the microprocessor chip containing key data, usage data and program command data. Patent Document 3 discloses a computer system having an input/output processor provided as a built-in processor connected to a local memory. Patent Document 4 discloses a memory having an SPI driver and a memory means that are arranged inside the memory. Patent Document 5 discloses a data processing system including a CPU that is linked to a data memory via a single-direction readout bus, a single-direction writing-in bus and an address bus. Patent Document 6 discloses a memory system in which a memory controller is connected to a memory via a writing-in data transfer bus and a readout data transfer bus that are separately disposed. Patent Document 7 discloses a random-access memory configured in such a way that data transfer to random-access memories is controlled in response to first translation of a period signal and data transfer from an array of random-access memories is controlled in response to second translation of the period signal. Patent Document 8 discloses a semiconductor memory device that includes a DRAM, and a CDRAM having a DRAM control and cache/refresh control unit. Patent Document 9 discloses a synchronous DRAM that has a memory array and a control unit and that allows setting of a mode register only when the data contents of a data bus is equal to operation status check data. Patent Document 10 discloses a mode register control circuit provided as an SDRAM and so on.

[Patent Document 1] Japanese Patent Application Laid-Open Publication No. 2004-110785 (ABSTRACT, Fig. 1, etc.)
[Patent Document 2] Japanese Patent Application Laid-Open Publication No. (H)06-208515 (ABSTRACT, Fig. 1, etc.)
[Patent Document 3] Japanese Patent Application Laid-Open Publication No. (H)09-6722 (ABSTRACT, Fig. 2, etc.)
[Patent Document 4] Japanese Patent Application Laid-Open Publication No. 2005-196486 (paragraph 0029, Fig. 6, etc.)
[Patent Document 5) Published Japanese Translations of PCT International Publication for Patent Applications No. (H)09-507325 (ABSTRACT, Fig. 1, etc.)
[Patent Document 6] Japanese Patent Application Laid-Open Publication No. 2002-63791 (ABSTRACT, Fig. 1, etc.)
[Patent Document 7] Japanese Patent Application Laid-Open Publication No. (H)11-328975 (ABSTRACT, Fig. 2, etc.)
[Patent Document 8] Japanese Patent Application Laid-Open Publication No. (H)07-169271 (paragraph 0038, Fig. 1, etc.)
[Patent Document 9] Japanese Patent Application Laid-Open Publication No. (H)08-124380 (paragraph 0020, Fig. 2, etc.)
[Patent Document 10] Japanese Patent Application Laid-Open Publication No. (H)09-259582 (paragraph 0028, Fig. 1, etc.)

[0004] US 5, 812,491 A shows a mode register control circuit for controlling read and write operations of a mode register of a semiconductor device.

[0005] US 6,691,204 B1 shows a memory device having memory banks as well as a non-volatile mode register and a volatile mode register. When power is turned on, data are tranferred from the non-volatile mode register to the volatile mode register.

[0006] US 6,594,167 B1 shows a memory board carrying a plurality of memory chips each having a mode register and memory banks.

[Disclosure of the Invention]

[Problems to Be Solved by the Invention]

[0007] As shown in Fig. 1, a conventional memory module 2 includes a circuit board that carries a plurality of memory chips 41, 42, ... and 4N and an SPD (Serial Presence Detect) memory unit 6. The memory chips 41, 42, ... and 4N are connected to a memory access bus 8, and the SPD memory unit 6 is connected to an SPD access bus 10. In this memory

[0008] module 2, the specifications and functions of the memory chips 41, 42, ... and 4N, such as types and timing parameters of the memory chips, are stored on the SPD memory unit 6. As a result, consistency of the memory module 2 with a setting environment depends on control data stored on the SPD memory unit 6. The

SPD memory unit 6 stores memory-related control data, which includes memory-related various parameters such as CAS (Column Array Strobe) latency, burst length, and additive latency. These control data are the data for setting different values depending on a chip set and a CPU (Central Processing Unit) that control memories. The SPD memory unit 6 is comprised of such a nonvolatile memory as EEPROM (Electrically Erasable Programmable Read-Only Memory). Keeping control parameters necessary for memories in a component separated from the memories requires handling and control corresponding to the separate parameter storage, leading to an increase in various costs including product cost and writing-in cost.

[0009] Although the memory module 2 has a number of memory chips 41, 42, ... and 4N, the specification of each of the memory chips 41, 42, ... and 4N is regulated by the SPD memory unit 6. This makes impossible separate use of each of the memory chips 41, 42, ... and 4N as a memory chip having a different specification. In other words, such a memory module 2 lacks flexibility in practical use.

[0010] Patent Documents 1 to 10 suggest or disclose nothing about the above problems, and disclose nothing about a solution to the problems, either.

[0011] An object of the present invention is to improve flexibility of a memory device having a plurality of memory chips to enable the memory device to give each of the memory chips separate control data.

[0012] Another object of the present invention is to separately control each of memory chips to optimize a memory and improve its compatibility.

[Means for Solving the Problems]

[0013] To achieve the above objects, a memory device of the present invention is defined in claim 1, wherein a plurality of memory chips includes a memory unit inside each memory chip, which memory part stores control data on the memory chip. The memory device enables writing-in or readout of the control data stored on the memory part to be able to set any desired control data for each memory chip, and, when the memory device has the plurality of memory chips, enables separate use of each of the memory chips.

[0014] To achieve the above objects, a first aspect of the present invention provides a memory device of claim 1 including a plurality of memory chips, comprising each memory chip that has a memory part, which stores control data concerning the memory chip, inside thereof, wherein the control data stored in the memory part is allowed to be written in and read out. In such a configuration, the memory chips are memory component units making up the memory device provided as a memory module and so on. Each memory chip includes a plurality of memory matrixes. In this configuration, control data on the memory chip is stored on the control memory part, and the control data stored on the memory part is rewritable. Hence the above objects are achieved.

[0015] To achieve the above objects, in the above memory device, preferably the memory part should not be provided as an independent EEPROM or mask ROM but may be provided as a control register. Such a configuration also achieves the above objects.

[0016] To achieve the above objects, in the above memory device, the memory chip has plurality of memory matrixes. Such a configuration also achieves the above objects.

[0017] To achieve the above objects, in the above memory device, the memory chip has a fixed data memory part inside thereof, the fixed data memory part storing fixed data out of the control data concerning the memory chip. Such a configuration also achieves the above objects.

[0018] To achieve the above objects, in the above memory device, the fixed data stored in the fixed data memory part is allowed to be transferred to the memory part inside the memory chip. Such a configuration also achieves the above objects.

[0019] To achieve the above objects, a second aspect of the present invention provides a control method of claim 4 with a step of writing in or reading out control data concerning each memory chip to or from a memory part storing the control data. According to such a configuration, a memory chip is identified by using address data on the memory chip, and rewriting control data stored on the memory part of the identified memory chip allows the memory chip to operate in correspondence to a change in a service environment and so on. This improves compatibility of the memory device and optimizes the memory device.

[0020] To achieve the above objects, a third aspect of the present invention provides a control program of claim 5 for a memory device executed by a computer, the control program driving the computer to execute a step of writing in or reading out control data to or from a memory part of a memory chip. According to such a configuration, the control program is executed by a computer apparatus at electronic equipment, such as a computer equipped with the memory device. In execution of the control program, a memory chip is identified by using address data on the memory chip. The computer apparatus rewrites control data stored on the memory part of the identified memory chip to allow the memory chip to deal with a change in a service environment and so on. This improves compatibility of the memory device and optimizes the memory device, thus achieves the above objects.

[0021] To achieve the above objects, the present invention also provides a memory of claim 6 as a card including a plurality of memory chips, comprising each memory chip that has a memory part, which stores control data concerning the memory chip, inside thereof, wherein the control data stored in the memory part is allowed to be written in or read out.

[0022] To achieve the above objects, in the memory card, preferably the memory part may be comprised of

a control register. Such a configuration also achieves the above objects.

[0023] To achieve the above objects, in the memory card, preferably the memory chip may have a single or a plurality of memory matrixes. Such a configuration also achieves the above objects.

[0024] To achieve the above objects, in the memory card, the memory chip has a fixed data memory part inside thereof, the fixed data memory part storing fixed data out of the control data concerning the memory chip. Such a configuration also achieves the above objects.

[0025] To achieve the above objects, in the memory card, the fixed data stored on the fixed data memory part is allowed to be transferred to the memory part. Such a configuration also achieves the above objects.

[0026] To achieve the above objects, the present invention also provides a circuit board provided with the memory device described above comprising each memory chip that has a memory part, which stores control data concerning the memory chip, inside thereof, wherein the control data stored in the memory part is allowed to be written in or read out. Such a configuration also achieves the above objects.

[0027] To achieve the above objects,preferably a circuit board may comprise a slot into which the memory card is fitted. Such a configuration also achieves the above objects.

[0028] To achieve the above objects, the present invention also provides electronic equipment comprising the memory device. This electronic equipment may be provided as any form of equipment such as a computer, as long as it carries out data storage using the memory device. Such a configuration also achieves the above objects.

[0029] To achieve the above objects, the present invention also provides electronic equipment comprising the memory card. In this case, the electronic equipment may be also provided as any form of equipment such as a computer, as long as it carries out data storage using the memory device. Such a configuration also achieves the above objects.

[Effects of the Invention]

[0030] The present invention offers the following effects.

(1) A memory part inside each memory chip stores control data concerning the memory chip, and the control data is used on a memory-chip-to-memory-chip basis. This enables the use of each memory chip as a memory chip having a different specification, thus improves flexibility of the memory device.
(2) Each memory chip is controlled separately based on control data stored on the memory chip to optimize the memory device.
(3) Control data stored on the memory part in each memory chip is rewritten to improve compatibility of the memory device.

[0031] Other objects, features, and advantages will be further clarified by referring to the accompanying drawings and embodiments.

[Brief Description of the Drawings]

[0032]

[Fig. 1] Fig. 1 is a view of a configuration of a conventional memory;
[Fig. 2] Fig. 2 is a view of an exemplary configuration of a memory module;
[Fig. 3] Fig. 3 is a block diagram of an exemplary configuration of a memory chip;
[Fig. 4] Fig. 4 is timing charts showing input/output control of a control register;
[Fig. 5] Fig. 5 is a view of an exemplary configuration of a memory module of a first embodiment;
[Fig. 6] Fig. 6 is a block diagram of an exemplary configuration of a memory chip;
[Fig. 7] Fig. 7 is a view of an exemplary configuration of a personal computer of a second embodiment;
[Fig. 8] Fig. 8 is a flowchart of a procedure of a process of writing in or rewriting control data;
[Fig. 9] Fig. 9 is a view of an exemplary configuration of a memory card of a third embodiment; and
[Fig. 10] Fig. 10 is a view of an exemplary configuration of a circuit board of a fourth embodiment.

[Explanation of Letters or Numerals]

[0033]

100 memory module
201, 202, 203, ..., 20N memory chip
211, 212, 213, 214 memory matrix
220 control register (fluctuation data memory part)
222 SPD memory unit (fixed data memory part)
231, 232, 233 ..., 23N bus
300 personal computer
318 memory module processing program
400 memory card
500 circuit board

[Best Modes for Carrying Out the Invention]

[0034] Fig. 2 depicts an exemplary configuration of a memory module. Fig. 2 depicts an example of a memory device. The configuration of the memory device therefore, is not limited to the configuration shown in Fig. 2.

[0035] The memory module 100 is an example of the memory device. For example, the memory module 100 includes a circuit board that carries a plurality of memory chips 201, 202, ... and 20N. The memory chips 201, 202, ... and 20N are memory component units, and need not to be the minimum component units but may be con-

figured to be different from the memory component units. In this configuration, the memory module 100 is comprised of the plurality of memory chips 201, 202, ... and 20N. The memory module 100, however, may be constructed as a single memory module.

[0036] Each of the memory chips 201, 202, ... and 20N has, for example, four memory matrixes 211, 212, 213 and 214 serving as a plurality of banks, and a control register 220 serving as a memory part storing control data. Each control register 220 stores individual control data on each of the memory chips 201, 202, ... and 20N. This control data includes various memory-related parameters such as CAS (Column Array Strobe) latency, burst length and additive latency. The control data, therefore, may vary for each of the memory chips 201, 202, ... and 20N, or may be the same for every memory chip.

[0037] The memory chips 201, 202, ... and 20N are connected to buses 231, 232, ... and 23N, respectively. This enables data reading/writing from/to any one of the memory chips 201 to 20N that is identified by address data, and also enables writing in and rewriting of such control data as specification data and/or function data stored on the control register 220, based on address data identifying any one of the memory chips 201 to 20N.

[0038] In such a configuration, although the specifications and functions of the memory chips 201 to 20N mounted on the memory module 100 are regulated by control data stored on the control registers 220 of the memory chips, each of the memory chips 201 to 20N can be used as a memory chip having a different configuration by using storage data stored on each control register 220. In other words, control data stored on the control register 220 functions as identification data or function data that identifies each of the memory chips 201 to 20N or the memory module 100 as a whole.

[0039] When control data stored on the control register 220 is allowed to function as identification data on each of the memory chips 201 to 20N, each of the memory chips 201 to 20N is identified by the control data, which enables separate data reading/writing. Despite of being incorporated in the single memory module 100, therefore, each of the memory chips 201 to 20N can be separately used as a memory chip having a different standard, that is, a different specification and function. The memory module 100 thus constitutes the memory device that is highly flexible.

[0040] Since each of the memory chips 201 to 20N can be controlled separately based on control data stored on the control register 220, the parameters of each of the memory chips 201 to 20N or of the memory module 100 may be changed for operation corresponding to a given service environment. This optimizes the memory device and improves compatibility of the memory device.

[0041] The memory chips 201 to 20N arranged on the memory module 100 will then be described with reference to Fig. 3. Fig. 3 is a block diagram of an exemplary configuration of a memory chip. In Fig. 3, the same components as described in Fig. 2 are denoted by the same reference numerals.

[0042] Each of the memory chips 201 to 20N includes a plurality of memory matrixes 211 to 214, row decoders 241, 242, 243 and 244 that correspond to the memory matrixes 211, 212, 213 and 214, respectively, and sense/column decoders 251, 252, 253 and 254 that correspond to the memory matrixes 211, 212, 213, and 214 respectively. Each of the memory matrixes 211 to 214 has a plurality of memory cells arranged in a matrix form, i.e., rows and columns of memory cells. In this case, an N bit address signal passes through an N bit row buffer, and, in response to a row address selection signal RAS, comes into the row decoders 241 to 244, where a row of memory cells are selected. In response to a column address selection signal CAS, the N bit address signal then comes into sense/column decoders 251 to 254, where a column of memory cells are selected, which enables data reading and writing. Each of the memory matrixes 211 to 214 is capable of such an operation.

[0043] As described above, the control register 220 stores CAS (column Address Strobe) latency and so on, as control data, which is read and written based on address data from an address bus AB. Ao to An denote writing-in addresses, and Bo to Bm denote bank addresses.

[0044] The control register 220 is connected to an input/output circuit 280, which is connected to a data bus DB, through which control data and so on are exchanged with an external device. DQo to DQp denote data.

[0045] In such a configuration, the control register 220 receives input of a clock signal CLK (denoted by A in Fig. 4), a chip select signal CS (denoted by B in Fig. 4), the row address selection signal RAS (denoted by C in Fig. 4), the column address selection signal CAS (denoted by D in Fig. 4), a write enable signal WE (denoted by E in Fig. 4), and address data Ao to An and Bo to Bm (denoted by F in Fig. 4) as read commands, as shown in Fig. 4. Receiving such read command signals, the control register 220 sends output data DQo to DQp (denoted by G in Fig. 4) through the input/output circuit 280 into the data bus DB.

[First Embodiment]

[0046] A first embodiment of the present invention will be described with reference to Figs. 5 and 6. Fig. 5 depicts an exemplary configuration of a memory module of the first embodiment, and Fig. 6 is a block diagram of an exemplary configuration of a memory chip. In Figs. 5 and 6, the same components as described in Fig. 2 and 3 are denoted by the same reference numerals. Figs. 5 and 6 depict an example of a memory device of the present invention. The configuration of the memory device of the present invention, therefore, is not limited to the configuration shown in Figs. 5 and 6.

[0047] In the memory module 100 of the embodiment, as shown in Fig. 5, each of the memory chips 201 to 20N has the control register 220 serving as a fluctuation data

memory part and an SPD memory unit 222 serving as a fixed data memory part. The SPD memory unit 222 stores fixed control data, which is, for example, memory-related various parameters such as CAS latency, burst length and additive latency. The control register 220 has stores fixed control data read out from the SPD memory unit 222, which is, for example, such a parameter as CAS latency.

[0048] As shown in Fig. 6, in each of the memory chips 201 to 20N, the control register 220 and the SPD memory unit 222 are juxtaposed with each other, and are each connected to the input/output circuit 280, so that fixed control data read out from the SPD memory unit 222 is output through the input/output circuit 280 to the outside, or to the control register 220 on which the fixed control data is stored. This control data stored on the control register 220 determines the functions and operation of the memory matrixes 211 to 214.

[0049] Other operation and functions of the memory module 100 of the embodiment are the same as that of the configuration shown in Figures 2 and 3, and therefore are omitted in further description.

[Second Embodiment]

[0050] A second embodiment of the present invention will be described with reference to Figs. 7 and 8. Fig. 7 depicts an exemplary configuration of a personal computer (PC) of the second embodiment, and Fig. 8 is a flowchart of a procedure of a process of writing in or reading out storage data to and from a memory part. In Fig. 7, the same components as described in Fig. 2 or 5 are denoted by the same reference numerals.

[0051] The PC 300 is an example of electronic equipment having the memory module 100, and is capable of reading and writing storage data stored on each of the control register 220 of the memory chips 201 to 20N of the memory module 100, based on address data.

[0052] The PC 300 includes a CPU (Central Processing Unit) 302, which is connected to a north bridge (chip set) 306 via a bus 304. The north bridge 306 is connected to the memory module 100, and is also connected to an input/output (I/O) interface 310 via a south bridge 308. The north bridge 306 is a means that carries out data exchange between the CPU 302 and the memory module 100, and the south bridge 308 is a means that carries out data exchange between the CPU 302 and the I/O interface 310.

[0053] The memory module 100 has the above configuration (shown in Figs. 5 and 6), in which the same components as described above are denoted by the same reference numerals for saving further description.

[0054] To a bus 312 interposed between the south bridge 308 and the I/O interface 310, a memory unit 314 composed of a nonvolatile memory and so on is connected. The memory unit 314 stores a BIOS (Basic Input/Output System) 316 and a memory module processing program 318 for writing in or rewriting such control data as specification data and/or function data stored on each control register 220 of the memory module 100. The memory module processing program 318 can be executed by an operation system (OS) that is stored on a memory device 320 composed of such a nonvolatile memory as a hard disc drive (HDD). The I/O interface 310 is connected to input/output devices such as a keyboard 322 and a display device not shown.

[0055] Writing in or rewriting of control data in the memory module 100 in the above configuration will be described with reference to Fig. 8. Fig. 8 is a flowchart of a procedure of a process of writing in or rewriting control data.

[0056] Ordinary memory access is made to an address on a memory. In reading or writing parameters as control data, access is made to an address for parameter data reading/writing, etc., on a command register in the north bridge 306, which is a memory controller, and to an address on a data register for parameter reading and so on.

[0057] In a memory initialization procedure, writing of a command (for reading parameter data) is carried out first (step S1). Subsequently, reading of parameter data is carried out (step S2). Then, writing of a command (for writing parameter data) is carried out (step S3), and the procedure is ended. As a result, control data representing a specification and function is written to the control register 220 of the memory module 100, or control data stored on the control register 220 can be updated.

[Third Embodiment]

[0058] A third embodiment of the present invention will be described with reference to Fig. 9. Fig. 9 depicts an exemplary configuration of a memory card of the fourth embodiment. In Fig. 9, the same components as described in Fig. 2 or 3 are denoted by the same reference numerals.

[0059] The memory card 400 is a specific embodiment of the above described memory module 100. The memory card 400 includes a circuit board 402 having connectors 404 and 406 that are inserted into a socket on a motherboard side to provide electrical connection. The connector 404 carries four memory chips 411, 412, 413 and 414, and the connector 406 carries four memory chips 421, 422, 423 and 424. Each of the memory chips 411 to 414 and 421 to 424 has the above mentioned memory matrixes 211 to 214 and the control register 220. Each memory chip also has the SPD memory unit 222 juxtaposed with the control register 220.

[0060] As described above, this memory card 400 can be used separately as a memory card having a different specification and function, thus serving as a memory device having extremely high flexibility. The memory card 400 allows a change in specification and function and is able to operate in correspondence to a given service environment, thus enables optimization and improvement in compatibility of the memory.

[Fourth Embodiment]

[0061] A fourth embodiment of the present invention will be described with reference to Fig. 10. Fig. 10 depicts an exemplary configuration of a circuit board of the fifth embodiment. In Fig. 10, the same components as described in Fig. 7 or 9 will be denoted by the same reference numerals.

[0062] The circuit board 500 includes a memory slot 502 in which the memory card 400 equipped with the above described memory module 100 is fitted, and a north bridge 306. The north bride 306 and the memory slot 502 are connected to each other via a bus to be able to exchange data with each other.

[0063] According to the circuit board 500, control data is written in on each of the control registers 220 incorporated in the memory card 400 to achieve highly flexible memory access.

[Other Embodiments]

[0064] Modifications, features, etc. of the above embodiments will be enumerated as follows.

(1) As described in the above embodiments, the memory module 100 assumes a function of a memory interface, thus maintaining high compatibility. Maintaining compatibility means, for example, that a module equipped with a memory chip can be used permanently because of its compatibility.

(2) The control register 220 of each of the memory chips 201 to 20N may be given a program-based determining function. In such a case, if timing of interfacing is different depending on the product generation of the memory chips, a separate control interface may be provided for identifying a memory chip.

(3) In the above embodiments, the PC 300 is described as electronic equipment that is an application example of the memory device. The present invention, however, may apply widely to a TV set with a PC function, server, telephone set, etc.

[0065] While the preferred embodiments of the present invention have been described, the description is not intended to limit the present invention. Various modifications and variants will be apparent to those skilled in the art based on the substance of the invention described in the appended claims or disclosed in the specification, and such modifications and variants obviously fall within the true scope of the invention.

[Industrial Applicability]

[0066] According to the present invention, each memory chip has an internal memory part such as a control register, which stores control data on the memory chip. This is useful to enable the use of the memory device on a memory-chip-to-memory-chip basis, allow the memory chips to operate in correspondence to an environment change such as a specification change, thus optimize the memory device and improve flexibility and compatibility of the memory.

Claims

1. A memory device (100) including a plurality of memory chips (201, 202, ..., 20N),

- each memory chip comprising
- a memory part (220), which stores control data concerning the memory chip, inside thereof;
- a plurality of banks, a function and an operation of each of the plurality of banks being controlled based on the control data stored in the memory part, inside the memory chip,
- a fixed data memory part (222) storing fixed data concerning the memory chip,
- an input/output part (280) connected to the memory part (220) and the fixed data memory part (222),
- wherein the control data stored in the memory part (220) is allowed to be read out to an outside of the memory chip via the input/output part (280) and written in,
- wherein the fixed data stored in the fixed data memory part (222) is outputted to the outside of the memory chip via the input/output part (280),
- wherein the fixed data stored in the fixed data memory part (222) is allowed
- to be transferred to the memory part (220) via the input/output part (280) and
- to be written into the memory part (220) and, the fixed data is included into the control data stored in the memory part (220), and

wherein the function and the operation of each of the plurality of banks is determined by the control data stored in the memory part (220).

2. The memory device (100) of claim 1, wherein the memory part (220) is comprised of a control register.

3. The memory device of claim 1, wherein the plurality of banks compose a plurality of memory matrixes (211, 212, 213, 214).

4. A control method for a memory device (100) according to any of claims 1 to 3, **characterized in** comprising a step of

- writing in or reading out control data concerning each memory chip to the memory part (220) storing the control data or from the memory part (220) to an outside of the memory chip via the

input/output part (280);
- controlling a function and an operation of each of a plurality of banks of said each memory chip based on the control data; and
- outputting fixed data stored in the fixed data memory part (222) to the outside of the memory chip via the input/output part (280),
wherein
- the fixed data stored in the fixed data memory part (222) is allowed
- to be transferred to the memory part (220) via the input/output part (280) and
- to be written into the memory part (220) and the fixed data is included into the control data stored in the memory part (220).

5. A control program for a memory device (100) according to any of claims 1 to 3, **characterized in**

- driving a computer (300) to execute the method of claim 4.

6. A memory device according to any of claims 1 to 3, wherein said memory device is a memory card (400).

7. A circuit board provided with a memory device according to claim 1.

8. A circuit board (500) comprising a slot into which the memory device of claim 6 is fitted.

9. Electronic equipment (300) comprising the memory device of any one of claims 1, 2, 3 and 6.

Patentansprüche

1. Speichervorrichtung (100), die mehrere Speicherchips (201, 202, ..., 20N) enthält,

- wobei jeder Speicherchip umfaßt:

- - einen Speicherbereich (220), der den Speicherchip betreffende Steuerdaten speichert,
- - mehrere Speichermodule, wobei Funktion und Betrieb von jedem der mehreren Speichermodule auf Grundlage der im Speicherbereich gespeicherten Steuerdaten innerhalb des Speicherchips gesteuert werden,
- - einen Festdatenspeicherbereich (222), der den Speicherchip betreffende Festdaten speichert,
- - einen Eingabe-/Ausgabe-Bereich (280), der mit dem Speicherbereich (220) und dem Festdatenspeicherbereich (222) verbunden ist,
- wobei es möglich ist, die in dem Speicherbereich gespeicherten Steuerdaten (220) über den Eingabe-/Ausgabe-Bereich (280) außerhalb des Speicherchips auszulesen und einzuschreiben,
- wobei die in dem Festdatenspeicherbereich (222) gespeicherten Festdaten nach außerhalb des Speicherchips über den Eingabe-/Ausgabebereich (280) ausgegeben werden,
- wobei es möglich ist, die im Festdatenspeicherbereich (222) gespeicherten Festdaten

- - mit Hilfe des Eingabe-/Ausgabe-Bereichs auf den Speicherbereich (220) zu übertragen und
- - in den Speicherbereich (220) einzuschreiben, wobei die Festdaten in die im Speicherbereich (220) gespeicherten Steuerdaten eingefügt werden, und

wobei die Funktion und der Betrieb von jedem der mehreren Speichermodule jeweils durch die im Speicherbereich (220) gespeicherten Steuerdaten festgelegt werden.

2. Speichervorrichtung (100) nach Anspruch 1, wobei der Speicherbereich (220) aus einem Steuerregister besteht.

3. Speichervorrichtung nach Anspruch 1, wobei die mehreren Speichermodule mehrere Speichermatrizen (211, 212, 213, 214) bilden.

4. Steuerungsverfahren für eine Speichereinheit (100) nach einem der Ansprüche 1 bis 3,
gekennzeichnet durch Umfassen eines Schritts des:

- Einschreibens oder Auslesens der den jeweiligen Speicherchip betreffenden Steuerdaten in den Speicherbereich (220), der die Steuerdaten speichert, oder aus dem Speicherbereich (220) zu einem Bereich außerhalb des Speicherchips über den Eingabe-/Ausgabe-Bereich,
- Steuern einer Funktion und eines Betriebs von jedem der mehreren Speichermodule des jeweiligen Speicherchips auf Grundlage der Steuerdaten und
- Ausgebens der im Festdatenspeicher (222) gespeicherten Festdaten zu einem Bereich außerhalb des Speicherchips über den Eingabe-/Ausgabe-Bereich (280), wobei
- es möglich ist, die im Festdatenspeicher (222) gespeicherten Festdaten

- - über den Eingabe-/Ausgabe-Bereich auf den Speicherbereich (220) zu übertragen und

- - in den Speicherbereich (220) einzuschreiben, wobei die Festdaten in die im Speicherbereich (220) gespeicherten Steuerdaten eingefügt werden.

5. Steuerungsverfahren für eine Speichereinheit (100) nach einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet, daß** es

- einen Computer (300) steuert, um ein Verfahren nach Anspruch 4 auszuführen.

6. Speichervorrichtung nach einem der Ansprüche 1 bis 3, wobei die besagte Speichereinheit eine Speicherkarte ist (400).

7. Platine, die mit einer Speichereinheit nach Anspruch 1 versehen ist.

8. Platine (500), die einen Slot enthält, in welchen eine Speichereinheit nach Anspruch 6 eingebaut ist.

9. Elektronische Ausrüstung (300), welche eine Speichereinheit nach einem der Ansprüche 1, 2, 3 und 6 enthält.

Revendications

1. Dispositif de mémoire (100) incluant une pluralité de circuits intégrés de mémoire (201, 202, ... , 20N),

- chaque circuit intégré de mémoire comprenant:

- - une section de mémoire (220), qui mémorise, à l'intérieur de celle-ci, des données de commande concernant le circuit intégré de mémoire;
- - une pluralité de blocs, la fonction et le fonctionnement de chacun de la pluralité de blocs étant commandés à partir des données de commande mémorisées dans la section de mémoire, à l'intérieur du circuit intégré de mémoire;
- - une section de mémoire de données fixes (222) mémorisant des données fixes concernant le circuit intégré de mémoire;
- - une section d'entrée/sortie (280) connectée à la section de mémoire (220) et à la section de mémoire de données fixes (222),

- dans lequel les données de commande mémorisées dans la section de mémoire (220) peuvent être lues vers l'extérieur du circuit intégré de mémoire via la section d'entrée/sortie (280) et écrites dans celui-ci,
- dans lequel les données fixes mémorisées dans la section de mémoire de données fixes (222) sont sorties vers l'extérieur du circuit intégré de mémoire via la section d'entrée/sortie (280),
- dans lequel les données fixes mémorisées dans la section de mémoire de données fixes (222) peuvent:

- - être transférées à la section de mémoire (220) via la section d'entrée/sortie (280); et
- - être écrites dans la section de mémoire (220) et, les données fixes sont incluses dans les données de commande mémorisées dans la section de mémoire (220), et

dans lequel la fonction et le fonctionnement de chacun de la pluralité de blocs sont déterminés par les données de commande mémorisées dans la section de mémoire (220).

2. Dispositif de mémoire (100) selon la revendication 1, dans lequel la section de mémoire (220) est composée d'un registre de commande.

3. Dispositif de mémoire selon la revendication 1, dans lequel la pluralité de blocs compose une pluralité de matrices de mémoire (211, 212, 213, 214).

4. Procédé de commande pour un dispositif de mémoire (100) selon l'une quelconque des revendications 1 à 3, **caractérisé en ce qu'**il comprend une étape:

- d'écriture ou de lecture de données de commande concernant chaque circuit intégré de mémoire dans la section de mémoire (220) mémorisant les données de commande ou à partir de la section de mémoire (220) vers l'extérieur du circuit intégré de mémoire via la section d'entrée/sortie (280);
- de commande, à partir des données de commande, de la fonction et du fonctionnement de chacun de la pluralité de blocs de chacun desdits circuits intégrés de mémoire; et
- de sortie de données fixes mémorisées dans la section de mémoire de données fixes (222) vers l'extérieur du circuit intégré de mémoire via la section d'entrée/sortie (280),

dans lequel:
- les données fixes mémorisées dans la section de mémoire de données fixes (222) peuvent:
- être transférées à la section de mémoire (220) via la section d'entrée/sortie (280); et
- être écrites dans la section de mémoire (220) et les données fixes sont incluses dans les données de commande mémorisées dans la section de mémoire (220).

5. Programme de commandes pour un dispositif de mémoire (100) selon l'une quelconque des revendications 1 à 3, **caractérisé par** la commande d'un processeur (300) pour mettre en oeuvre le procédé selon la revendication 4.

6. Dispositif de mémoire selon l'une quelconque des revendications 1 à 3, dans lequel ledit dispositif de mémoire est une carte de mémoire (400).

7. Carte de circuit pourvue d'un dispositif de mémoire selon la revendication 1.

8. Carte de circuit (500) comprenant un logement dans lequel se monte le dispositif de mémoire selon la revendication 6.

9. Équipement électronique (300) comprenant le dispositif de mémoire selon l'une quelconque des revendications 1, 2, 3 et 6.

FIG.1

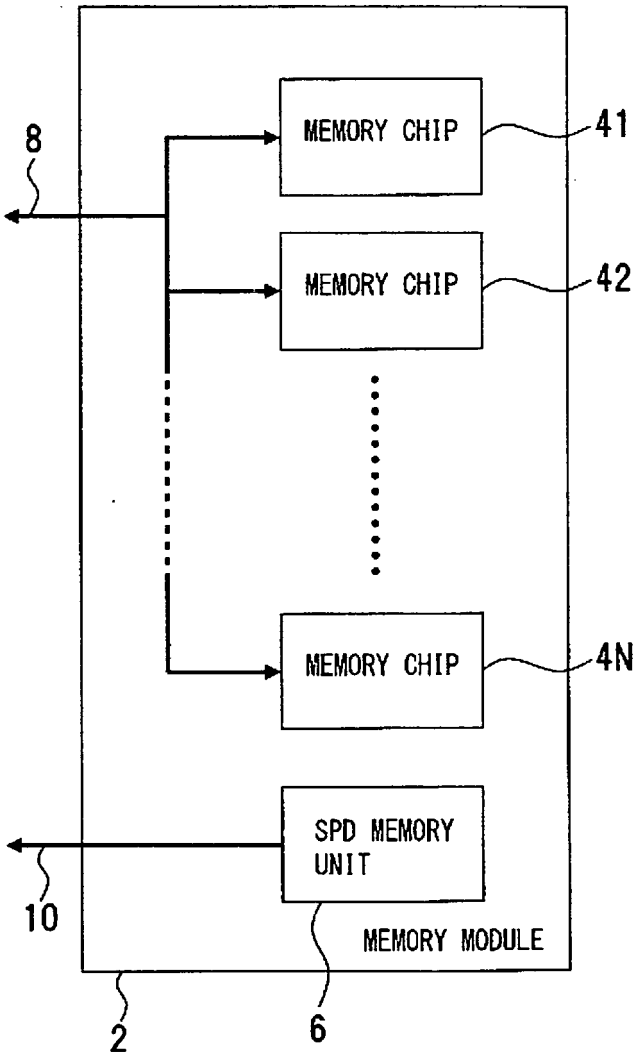

8
MEMORY CHIP
41
MEMORY CHIP
42
MEMORY CHIP
4N
SPD MEMORY UNIT
10
MEMORY MODULE
2
6

FIG.2

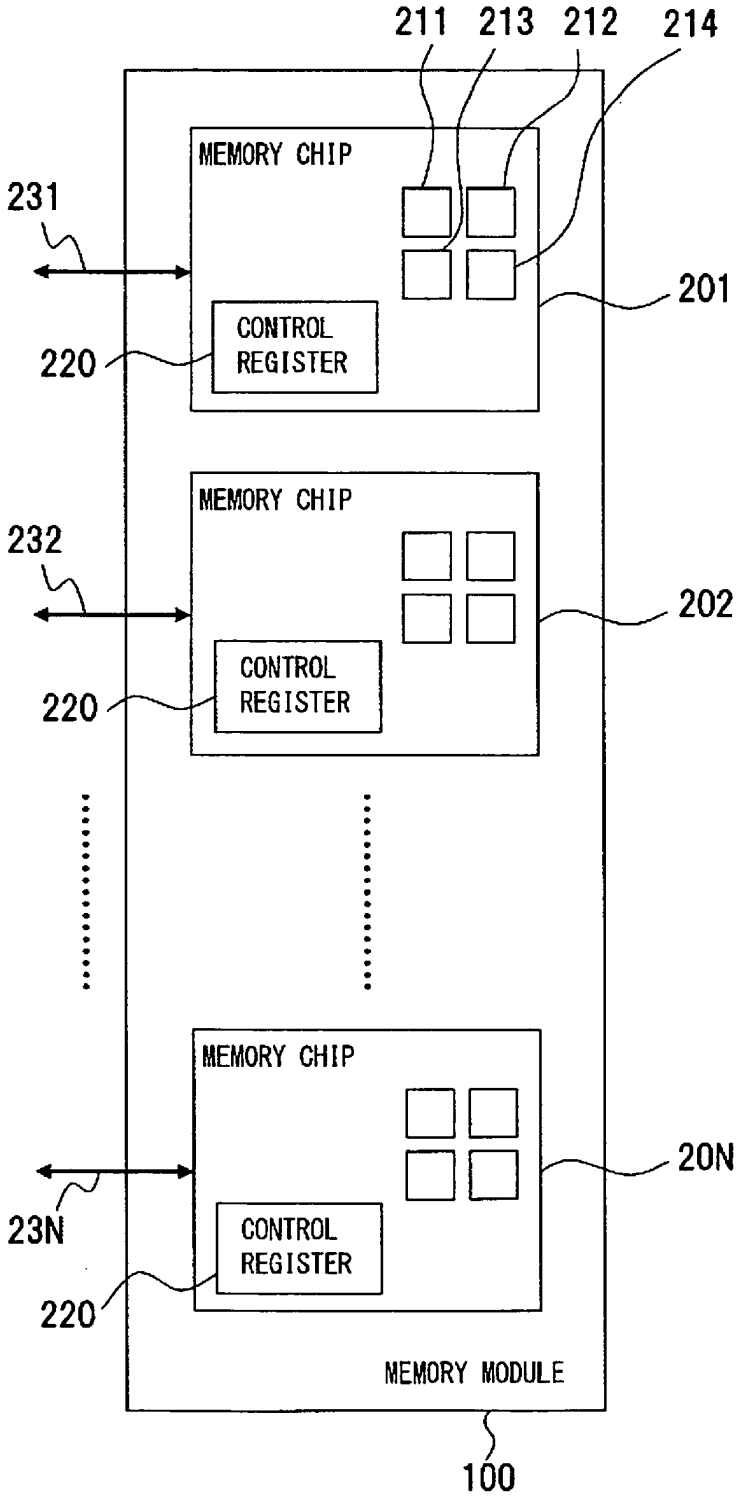

211
213
212
214
MEMORY CHIP
231
201
CONTROL REGISTER
220
MEMORY CHIP
232
202
CONTROL REGISTER
220
MEMORY CHIP
20N
23N
CONTROL REGISTER
220
MEMORY MODULE
100

FIG.3

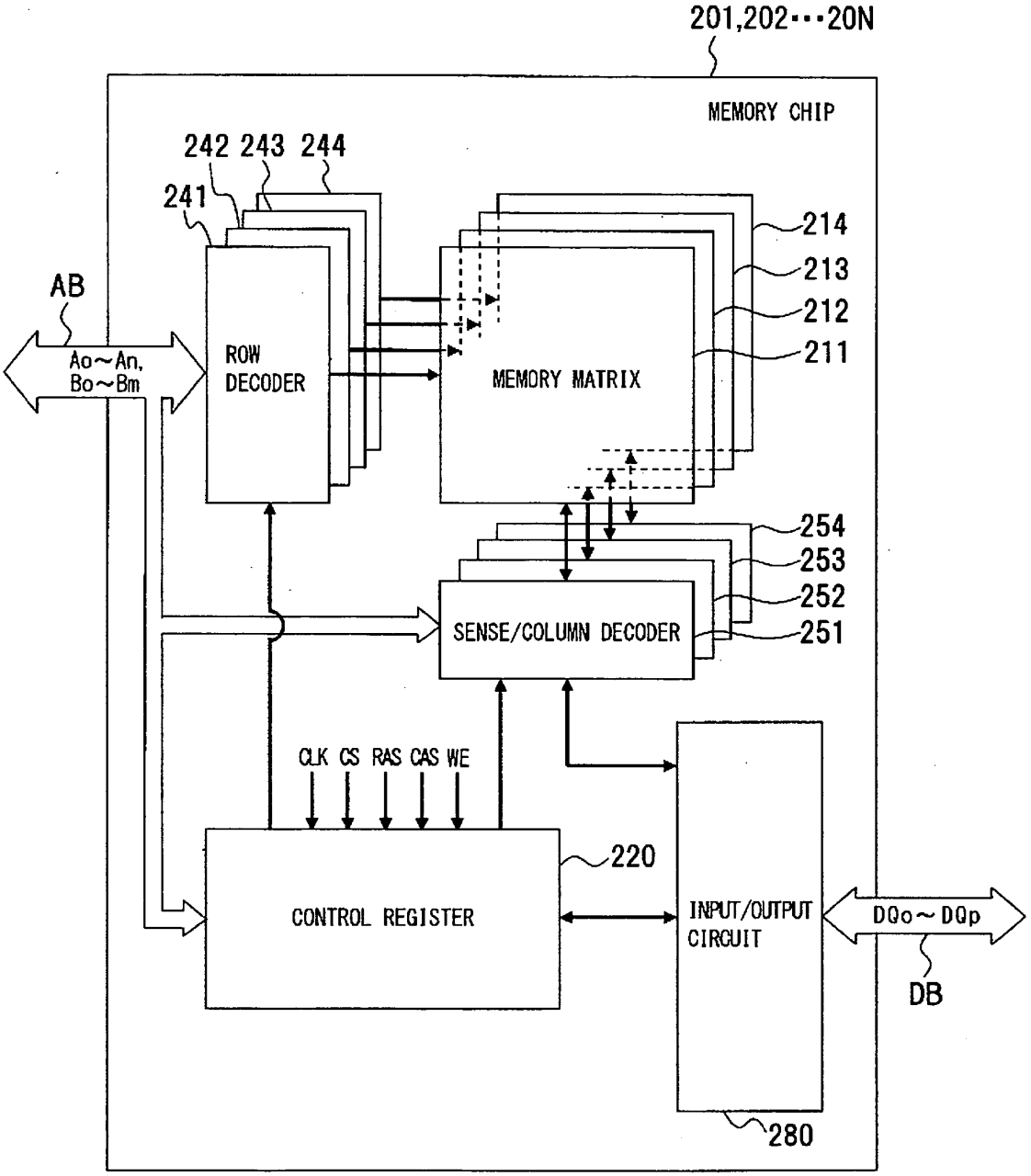

201,202···20N
MEMORY CHIP
242 243 244
241
AB
Ao~An,
Bo~Bm
ROW
DECODER
MEMORY MATRIX
214
213
212
211
254
253
252
251
SENSE/COLUMN DECODER
CLK CS RAS CAS WE
220
CONTROL REGISTER
INPUT/OUTPUT
CIRCUIT
DQo~DQp
DB
280

FIG.4

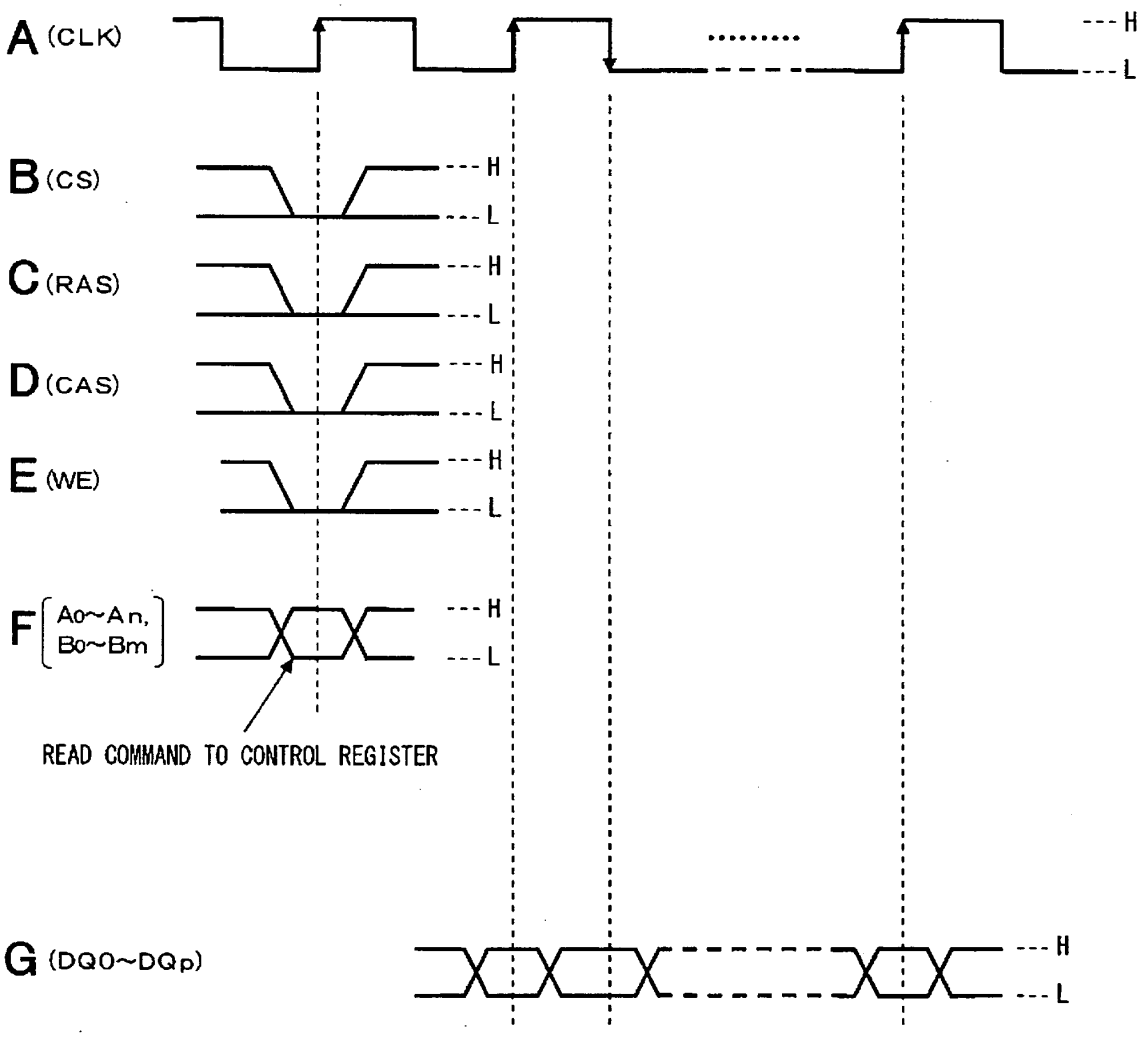

A (CLK)
H
L
B (CS)
C (RAS)
D (CAS)
E (WE)
F [A0~An, B0~Bm]
READ COMMAND TO CONTROL REGISTER
G (DQ0~DQp)

FIG.5

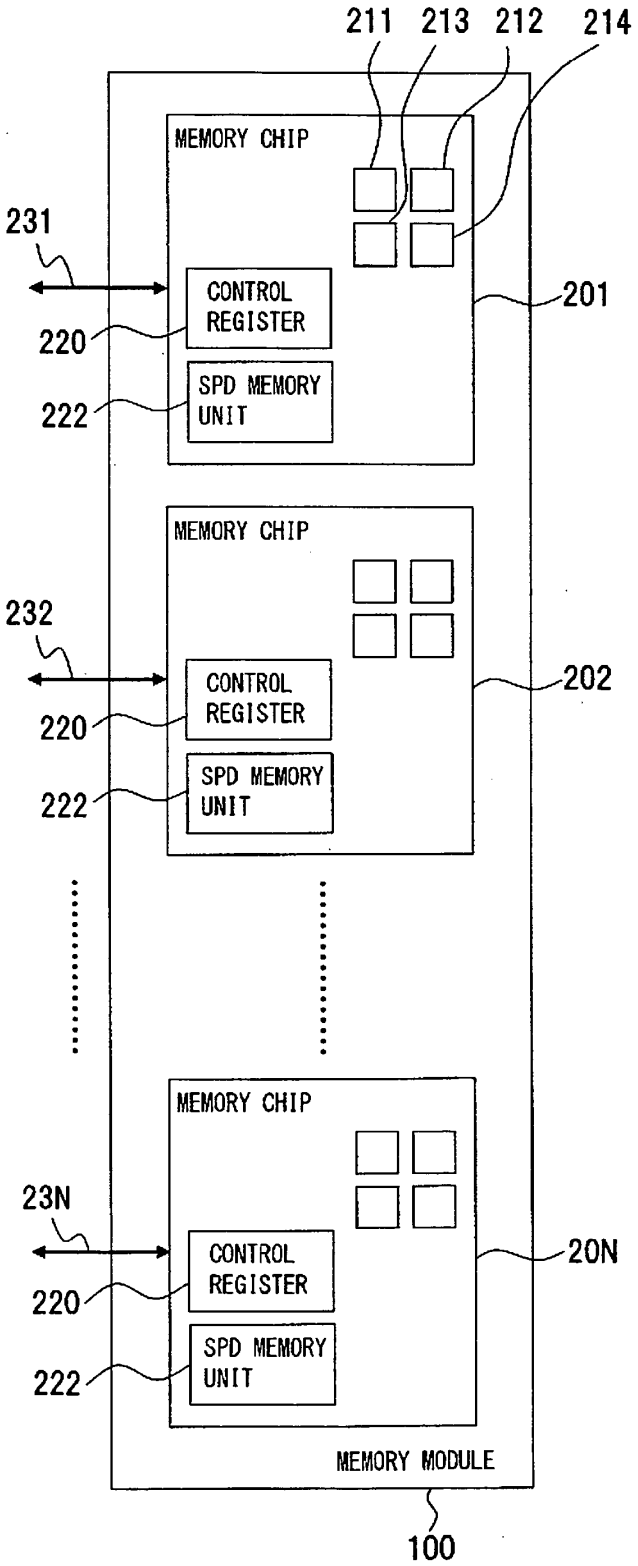

211
213
212
214
MEMORY CHIP
231
CONTROL REGISTER
220
SPD MEMORY UNIT
222
201
MEMORY CHIP
232
CONTROL REGISTER
220
SPD MEMORY UNIT
222
202
MEMORY CHIP
23N
CONTROL REGISTER
220
SPD MEMORY UNIT
222
20N
MEMORY MODULE
100

FIG.6

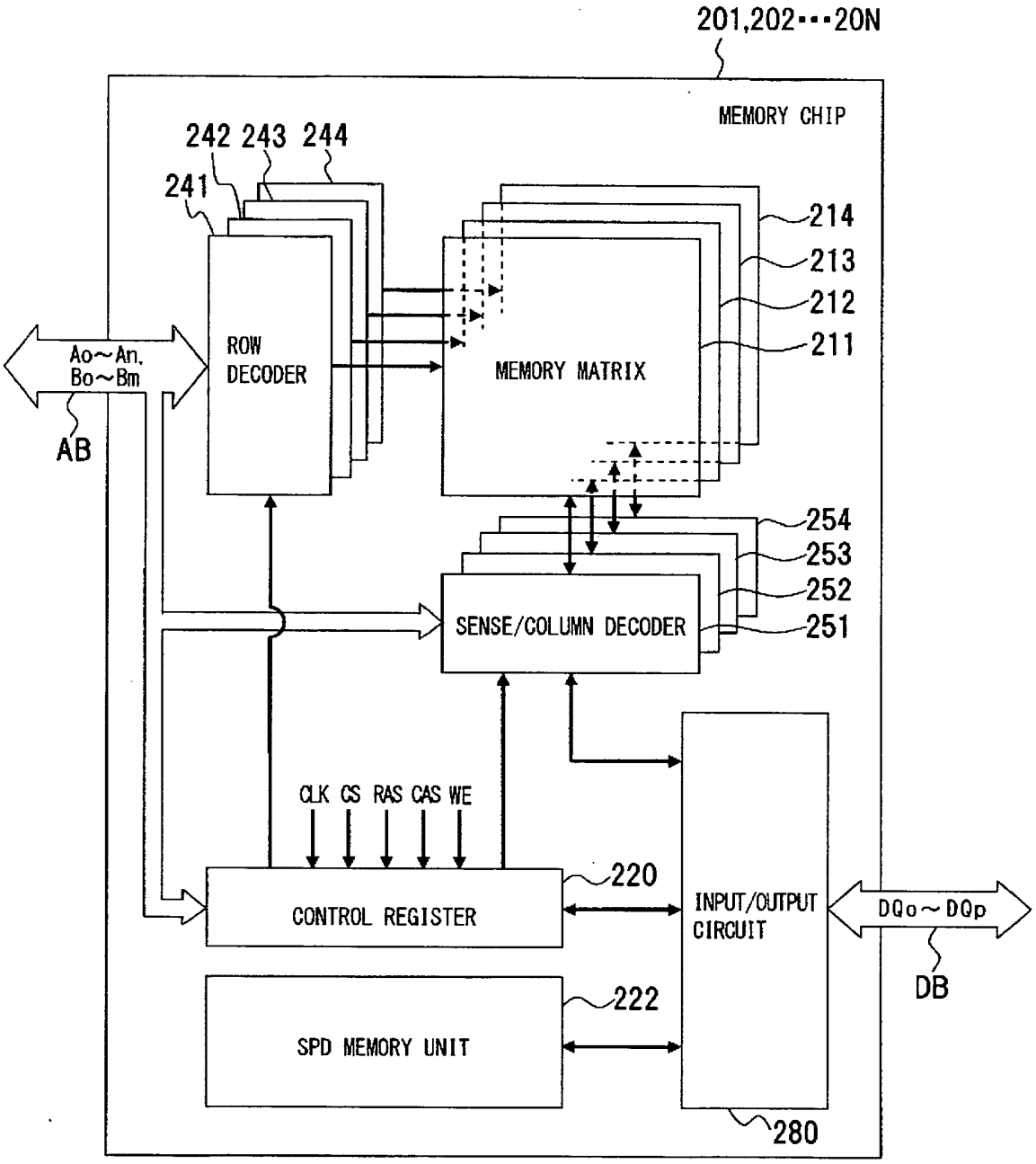

201,202···20N
MEMORY CHIP
242 243 244
241
214
213
212
211
ROW DECODER
MEMORY MATRIX
Ao~An,
Bo~Bm
AB
254
253
252
251
SENSE/COLUMN DECODER
CLK CS RAS CAS WE
220
CONTROL REGISTER
INPUT/OUTPUT CIRCUIT
DQo~DQp
DB
222
SPD MEMORY UNIT
280

FIG.7

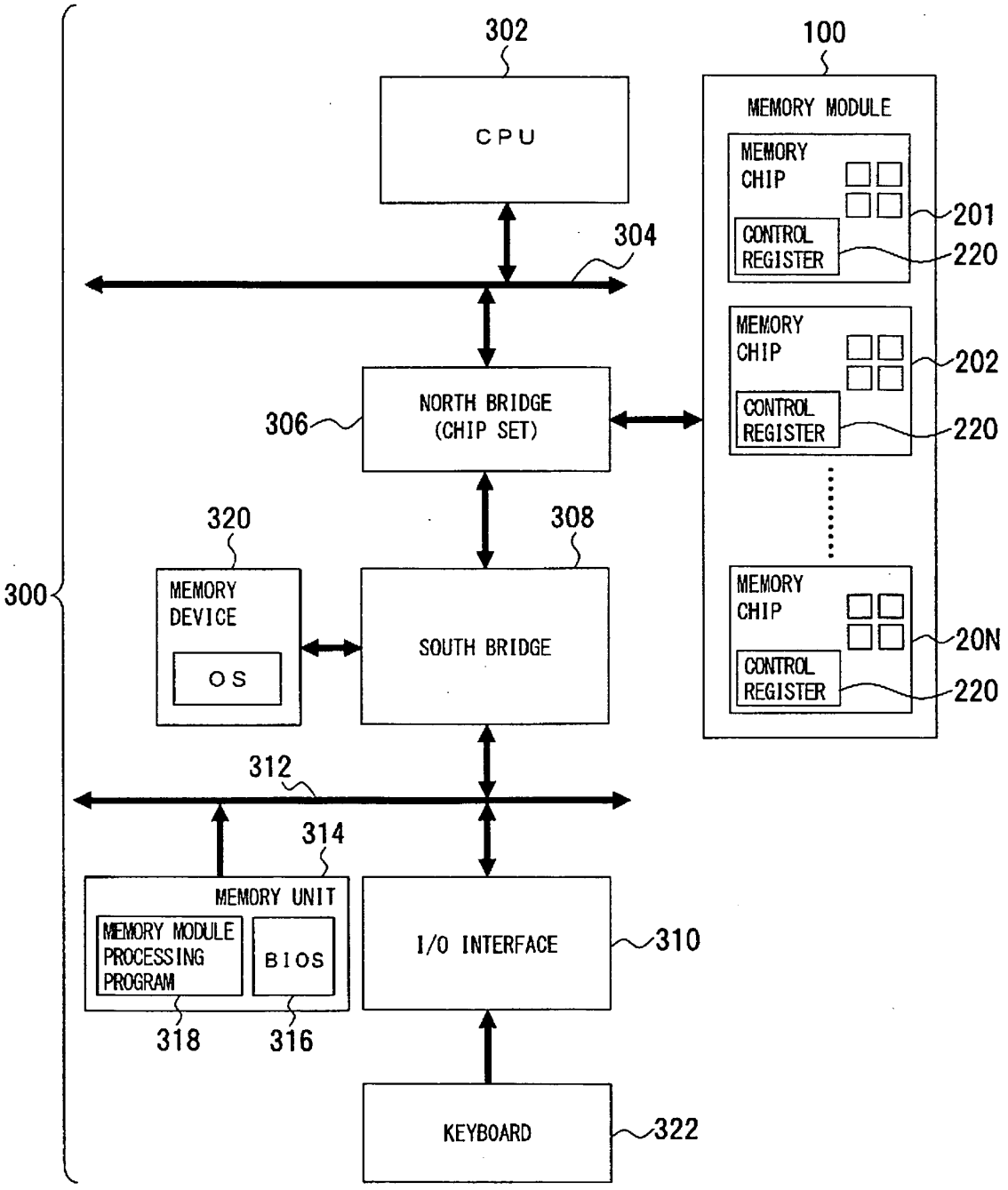

302
CPU
100
MEMORY MODULE
MEMORY CHIP
CONTROL REGISTER
201
220
304
MEMORY CHIP
CONTROL REGISTER
202
220
306
NORTH BRIDGE (CHIP SET)
320
308
MEMORY DEVICE
OS
SOUTH BRIDGE
MEMORY CHIP
CONTROL REGISTER
20N
220
300
312
314
MEMORY UNIT
MEMORY MODULE PROCESSING PROGRAM
BIOS
I/O INTERFACE
310
318
316
KEYBOARD
322

FIG.8

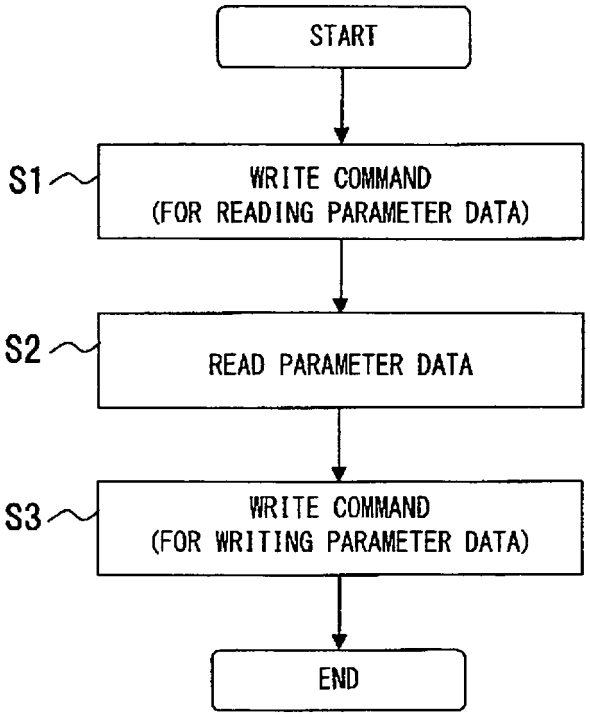

START
S1
WRITE COMMAND
(FOR READING PARAMETER DATA)
S2
READ PARAMETER DATA
S3
WRITE COMMAND
(FOR WRITING PARAMETER DATA)
END

FIG.9

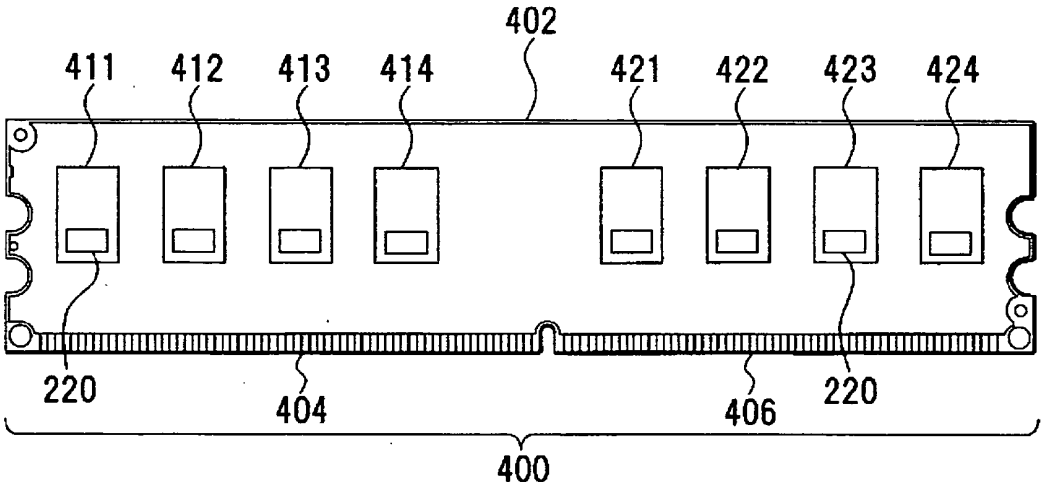
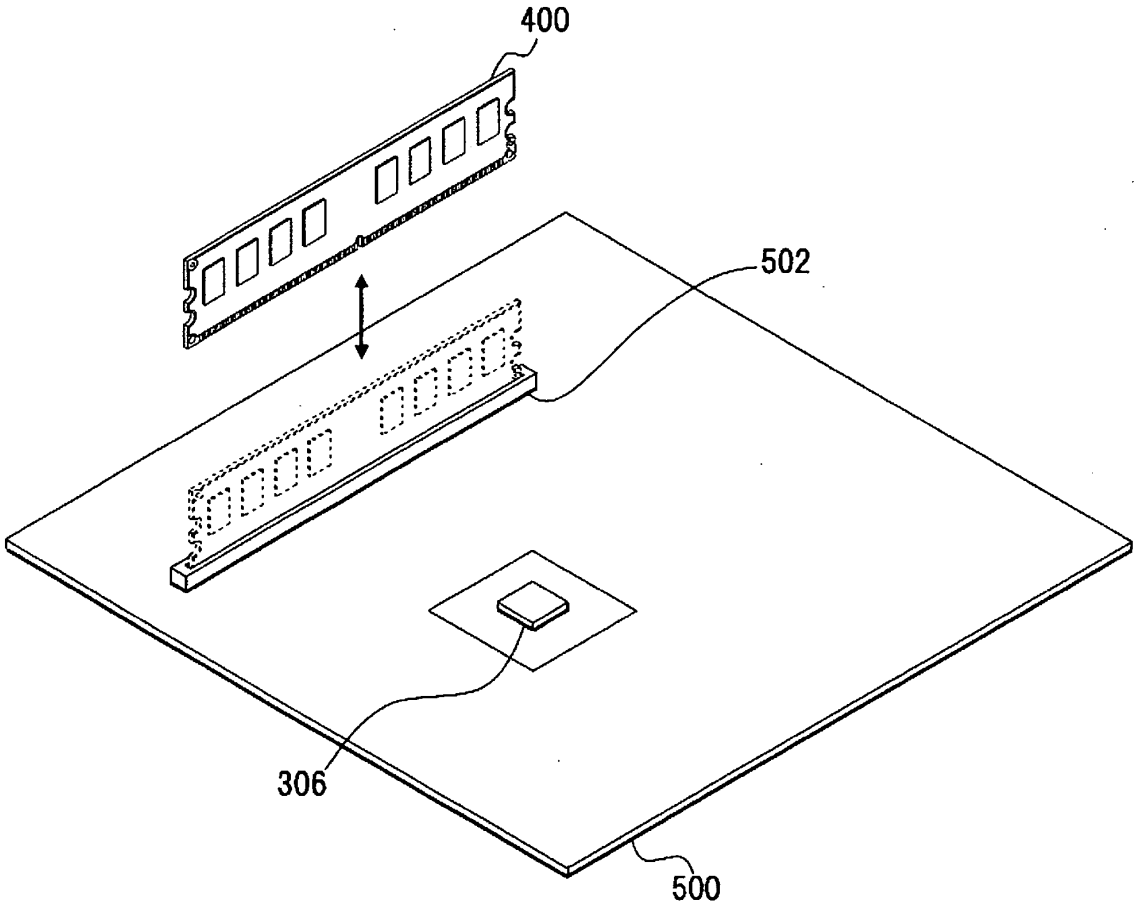


FIG.10



REFERENCES CITED IN THE DESCRIPTION

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