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(54) **PULL-DOWN CIRCUIT OF GATE DRIVING UNIT AND DISPLAY DEVICE**

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(57) **ABSTRACT**

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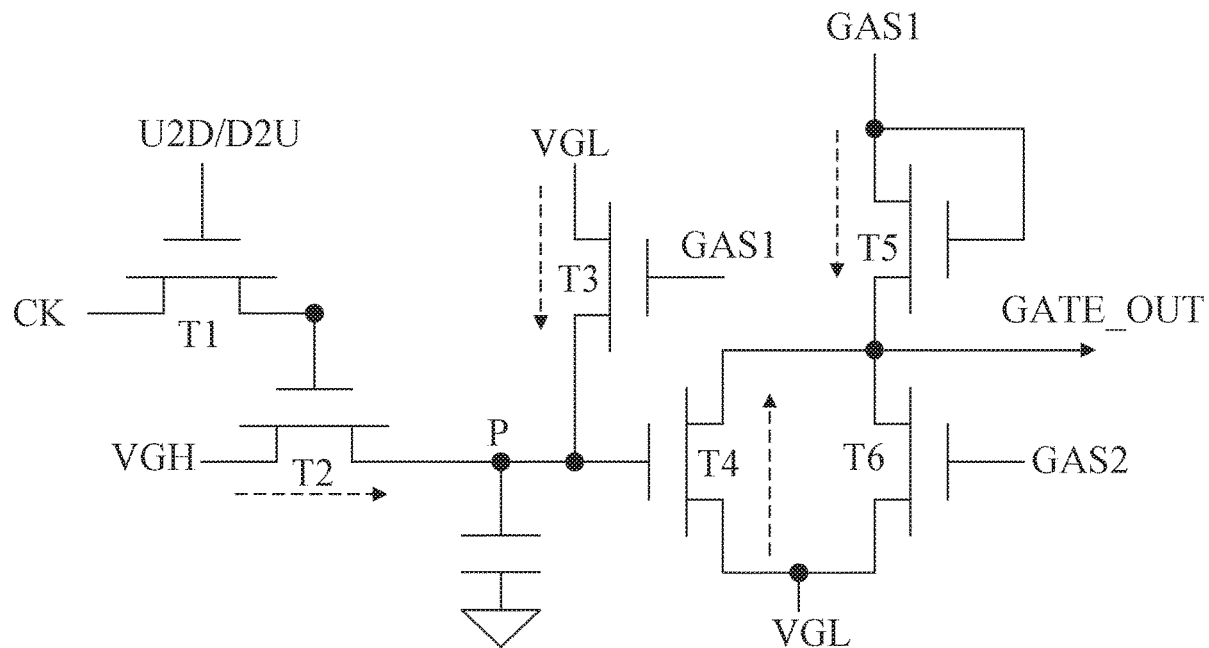
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A pull-down circuit of a gate driving unit includes: a first thin film transistor having a first gate to which a scan direction signal is inputted, a first source and a first drain to which a clock signal is inputted; a second thin film transistor having a second gate coupled to the first source, a second source coupled to a pull-down control node and a second drain to which a first direct-current voltage is inputted; a third thin film transistor having a third gate to which a first control signal is inputted, a third source coupled to the pull-down control node and a third drain coupled to a second direct-current voltage; and a fourth thin film transistor having a fourth gate coupled to the pull-down control node, a fourth source coupled to an output node and a fourth drain coupled to the second direct-current voltage.



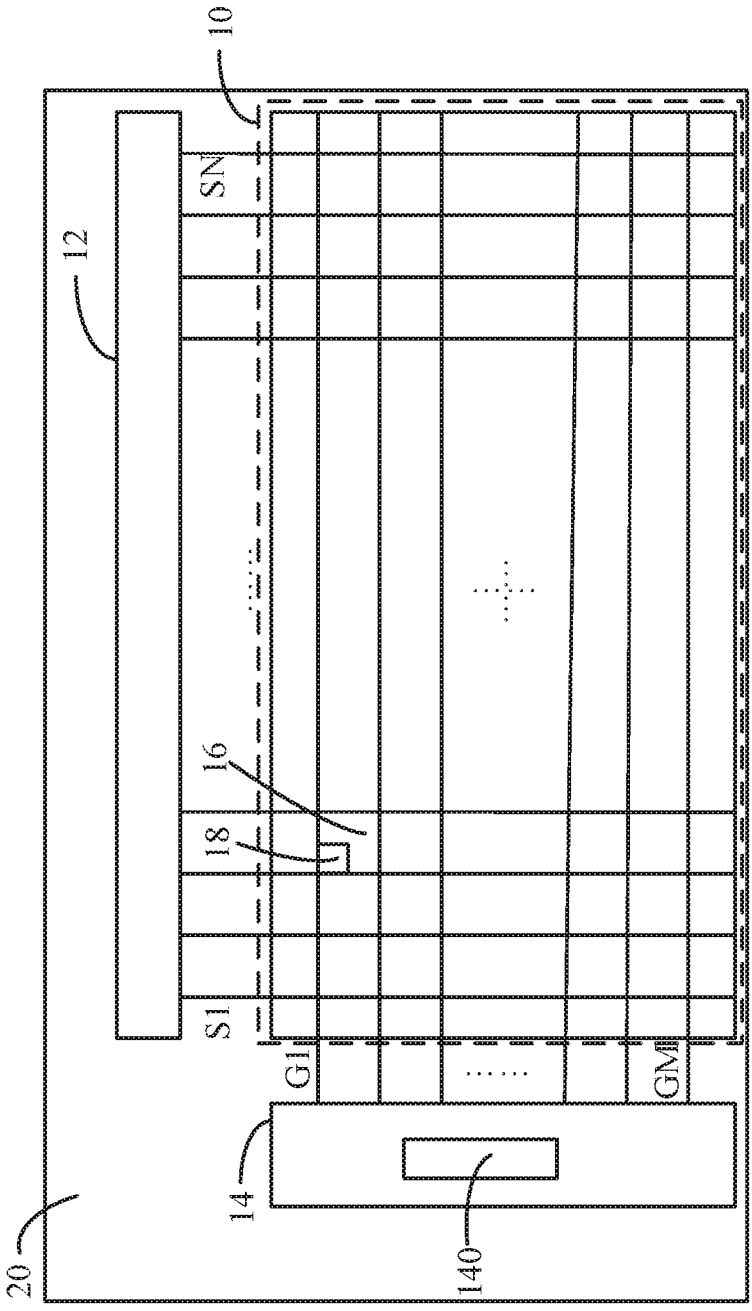


FIG. 1

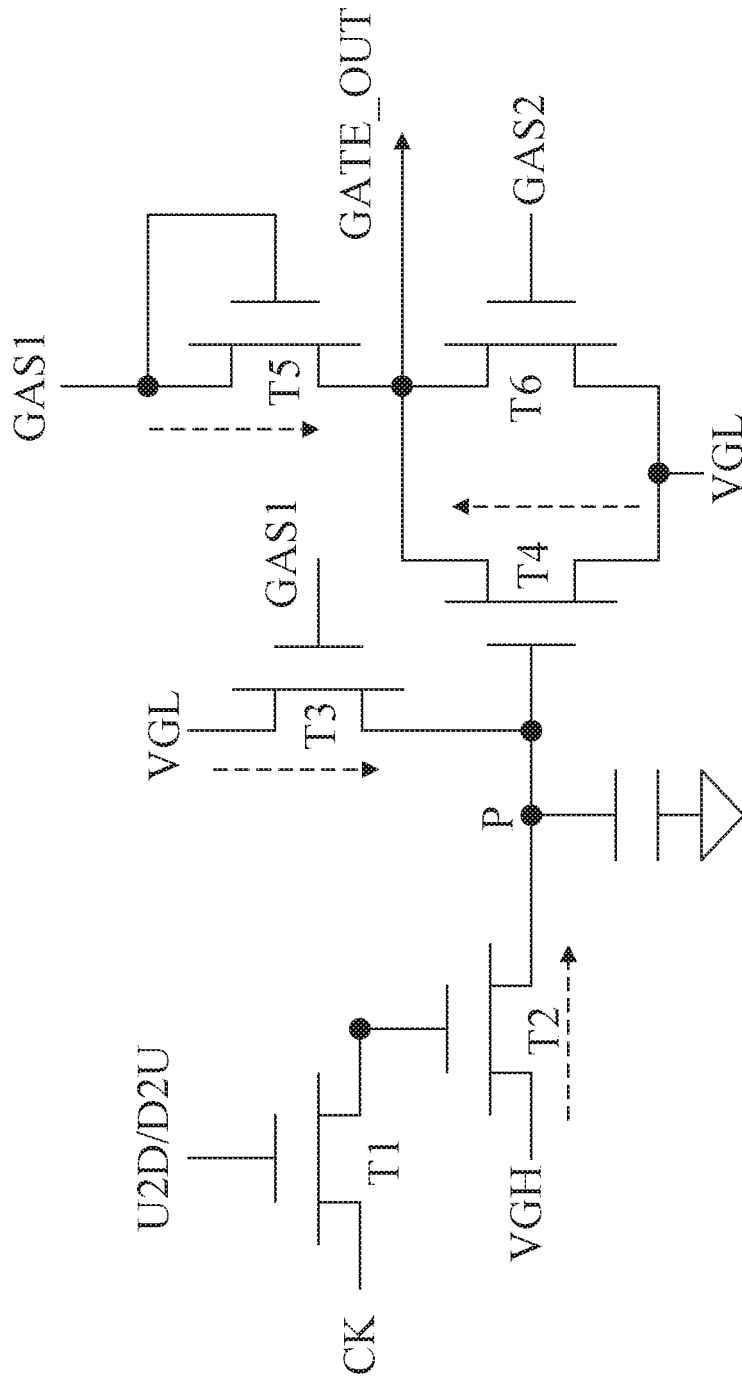


FIG. 2

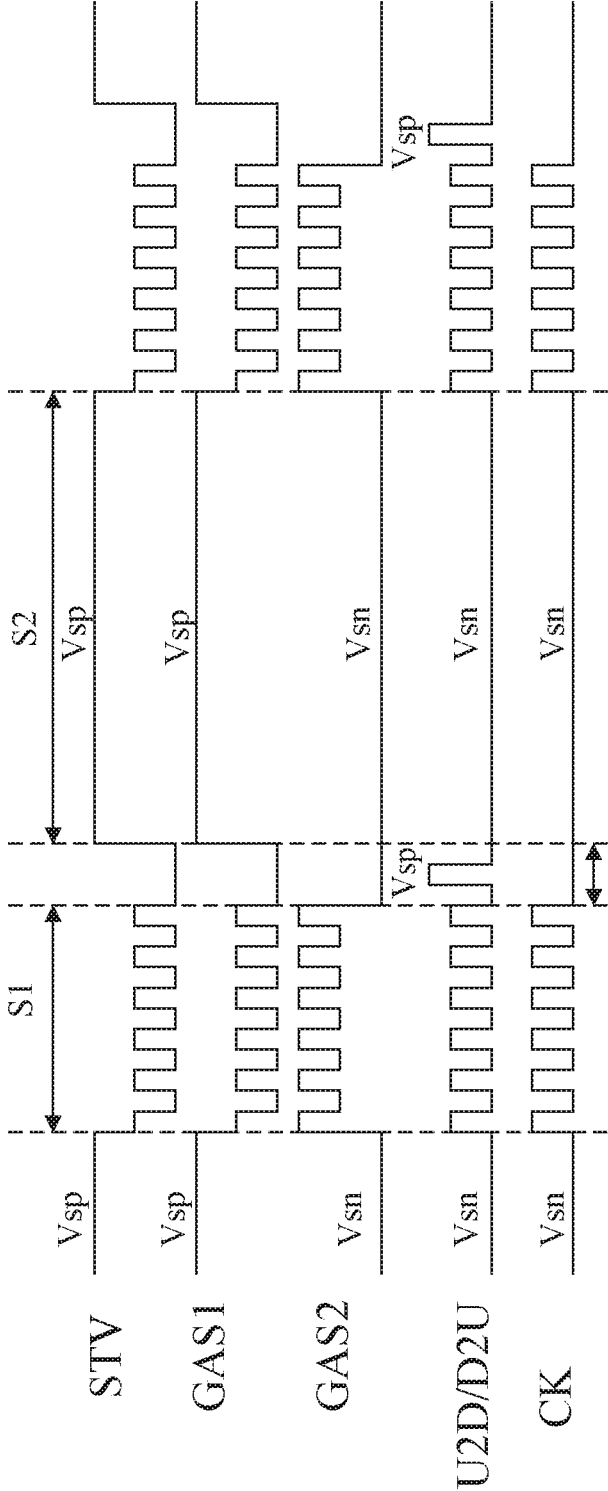


FIG. 3

PULL-DOWN CIRCUIT OF GATE DRIVING UNIT AND DISPLAY DEVICE

BACKGROUND

Field

[0001] The present disclosure relates to a display device, and more particularly to a pull-down circuit of a gate driving unit and a display device.

Background

[0002] Gate driver on array (GOA) technologies mean that gate driving circuits are manufactured on array substrate by a conventional array manufacturing process of thin film transistor liquid crystal displays (TFT-LCD) for implementing a driving manner of scanning gate lines row by row.

[0003] A low power wake-up gesture (LPWG) mode is a special function of smart phones. That is, sliding operations on screens are supported when the smart phones is in a standby (black screen) mode. Users can directly wake up some functions or corresponding software by preset gestures. In the LPWG mode, backlight sources of the smart phones are in a turned-off state, and all pixels store a common voltage (VCOM).

[0004] In the LPWG mode, gate lines are driven in two stages. In a first stage, scan signals are not provided for the gate lines, and screens of the smart phones can be configured to sense touch signals. In a second stage, the screens of the smart phones can be configured to display images. The first stage and the second stage are operated alternately.

[0005] However, when the first stage is switched to the second stage, micro-short circuit phenomenon occurs in elements of pull-down circuits of GOA modules due to influence of the above sensing signals. As such, power consumption of the screens is high in the LPWG mode.

[0006] Consequently, there is a need to solve the above-mentioned problems in the prior art.

SUMMARY OF THE DISCLOSURE

[0007] The micro-short circuit phenomenon occurs in the elements of the pull-down circuits of the GOA modules due to the influence of the above sensing signals. As such, the power consumption of the screens is high in the LPWG mode.

[0008] To solve the above problems, a pull-down circuit of a gate driving unit provided by the present disclosure is utilized for a display device and includes: a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain; a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain; a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the

second direct-current voltage, wherein the first thin film transistor, the second thin film transistor, the third thin film transistor, and the fourth thin film transistor are N-channel metal-oxide-semiconductor field-effect transistors.

[0009] In one embodiment, the pull-down circuit of the gate driving unit further includes: a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.

[0010] In one embodiment, the pull-down circuit of the gate driving unit further includes: a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.

[0011] In one embodiment, in a first stage, the display device is configured to sense at least one touch signal. In a second stage, the display device is configured to display an image.

[0012] In one embodiment, after the first stage ends and before the second stage starts, the scan direction signal is converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.

[0013] To solve the above problems, a pull-down circuit of a gate driving unit provided by the present disclosure is utilized for a display device and includes: a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain; a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain; a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the second direct-current voltage.

[0014] In one embodiment, the pull-down circuit of the gate driving unit further includes: a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.

[0015] In one embodiment, the pull-down circuit of the gate driving unit further includes: a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.

[0016] In one embodiment, in a first stage, the display device is configured to sense at least one touch signal. In a second stage, the display device is configured to display an image.

[0017] In one embodiment, after the first stage ends and before the second stage starts, the scan direction signal is converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.

[0018] To solve the above problems, a display device provided by the present disclosure has a display area and a non-display area. The display device includes: a plurality of source lines and a plurality of gate lines disposed on the display area; at least one source driving unit disposed on the non-display area and configured to provide data signals for the source lines; and at least one gate driving unit disposed on the non-display area and configured to provide scan signals for the gate lines. The gate driving unit at least includes a pull-down circuit. The pull-down circuit includes: a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain; a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain; a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the second direct-current voltage.

[0019] In one embodiment, the display device further includes: a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.

[0020] In one embodiment, the display device further includes: a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.

[0021] In one embodiment, in a first stage, the display device is configured to sense at least one touch signal. In a second stage, the display device is configured to display an image.

[0022] In one embodiment, after the first stage ends and before the second stage starts, the scan direction signal is converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.

[0023] Compared to the prior art, in the pull-down circuit and the display device of the present disclosure, the power consumption in the LPWG mode can be reduced by converting the scan direction signal to the second voltage level from the first voltage level for a predetermined time duration and then converting the second voltage level back to the first voltage level.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 illustrates a display device in accordance with an embodiment of the present disclosure.

[0025] FIG. 2 illustrates a circuit diagram of a pull-down circuit in accordance with an embodiment of the present disclosure.

[0026] FIG. 3 illustrates driving waves of the pull-down circuit in a low power wake-up gesture (LPWG) mode in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Hereinafter, exemplary embodiments of the present disclosure will be described with reference to the accompanying drawings for illustrating specific embodiments which can be carried out by the present disclosure.

[0028] Please refer to FIG. 1. FIG. 1 illustrates a display device in accordance with an embodiment of the present disclosure.

[0029] The display device has a display area **10** and a non-display area **12**. The display device includes a plurality of source lines **S1-SN**, a plurality of gate lines **G1-Gm**, at least one source driving unit **12** (one source driving unit **12** is shown in FIG. 1) and at least one gate driving unit **14** (one gate driving unit **14** is shown in FIG. 1).

[0030] The source lines **S1-SN** and the gate lines **G1-GM** are disposed on the display area **10**. In detail, the source lines **S1-SN** are disposed on the display area **10** and extend to the source driving unit **12**. The gate lines **G1-GM** are disposed on the display area **10** and extend to the gate driving unit **14**. The source lines **S1-SN** are formed in a first direction. The gate lines **G1-GM** are formed in a second direction. The first direction is perpendicular to the second direction. The source lines **S1-SN** and the gate lines **G1-GM** define a plurality of pixels **16**. Each of the pixels is electrically coupled to a thin film transistor **18**.

[0031] The source driving unit **12** is disposed on the non-display area **20**. The source driving unit **12** is electrically coupled to the source lines **S1-SN** and configured to provide data signals for the source lines **S1-SN**. The data signals are configured to be written into the pixels **16**.

[0032] The gate driving unit **14** is disposed on the non-display area **20**. That is, the gate driving unit **14** is a GOA circuit. The gate driving unit **14** is electrically coupled to the gate lines **G1-Gm** and configured to provide scan signals for the gate lines **G1-Gm**. The gate driving unit **14** at least includes a pull-down circuit **140**.

[0033] Please refer to FIG. 1 and FIG. 2. FIG. 2 illustrates a circuit diagram of the pull-down circuit **140** in accordance with an embodiment of the present disclosure.

[0034] The pull-down circuit **140** includes a first thin film transistor **T1**, a second thin film transistor **T2**, a third thin film transistor **T3**, a fourth thin film transistor **T4**, a fifth thin film transistor **T5** and a sixth thin film transistor **T6**.

[0035] The first thin film transistor **T1** has a first gate, a first source and a first drain. A scan direction signal **U2D/D2U** is inputted to the first gate. A clock signal is inputted to the first drain.

[0036] The second thin film transistor **T2** has a second gate, a second source and a second drain. The second gate is electrically coupled to the first source. The second source is electrically coupled to a pull-down control node **P**. A first direct-current voltage **VGH** is inputted to the second drain.

[0037] The third thin film transistor **T3** has a third gate, a third source and a third drain. A first control signal **GAS1** is inputted to the third gate. The third source is electrically coupled to the pull-down control node **P**. The third drain is electrically coupled to a second direct-current voltage **VGL**.

[0038] The fourth thin film transistor **T4** has a fourth gate, a fourth source and a fourth drain. The fourth gate is electrically coupled to the pull-down control node **P**. The fourth source is electrically coupled to an output node **GATE_OUT**. The fourth drain is electrically coupled to the second direct-current voltage **VGL**.

[0039] The fifth thin film transistor **T5** has a fifth gate, a fifth source and a fifth drain. The first control signal **GAS1** is inputted to the fifth gate and the fifth drain. The fifth source is electrically coupled to the output node **GATE_OUT**.

[0040] The sixth thin film transistor **T6** has a sixth gate, a sixth source and a sixth drain. A second control signal **GAS2** is inputted to the sixth gate. The sixth source is electrically coupled to the second direct-current voltage **VGL**. The sixth drain is electrically coupled to the output node **GATE_OUT**.

[0041] In the present embodiment, the first thin film transistor **T1**, the second thin film transistor **T2**, the third thin film transistor **T3**, the fourth thin film transistor **T4**, the fifth thin film transistor **T5** and the sixth thin film transistor **T6** may be N-channel metal-oxide-semiconductor field-effect transistors (N-MOSFETs).

[0042] Please refer to FIG. 1 to FIG. 3. FIG. 3 illustrates driving waves of the pull-down circuit **140** in a low power wake-up gesture (LPWG) mode in accordance with an embodiment of the present disclosure.

[0043] In the LPWG mode, the gate lines **G1-GM** are driven in two stages. In a first stage **S1**, scan signals are not provided for the gate lines **G1-GM** (all gates lines are off), and the display device can be configured to sense at least one touch signal. In a second stage **S2**, the scan signals are sequentially provided for the gate lines **G1-GM** (all gates lines are on), and the display device can be configured to display an image. The first stage and the second stage are operated alternately.

[0044] When the second stage **S2** is entered after the first stage **S1** ends, a competition relationship is formed by the second thin film transistor **T2** and the third thin film transistor **T3** because a touch pulse signal is high in the first stage **S1**. That is, a micro-short circuit path occurs between **Vsp** and **Vsn**. The first control signal **GAS1** does not have enough ability of pulling down a voltage of the pull-down control node **P** via the third thin film transistor **T3**. Accordingly, the pull-down control node **P** turns on the fourth thin film transistor **T4**. That is, a competition relationship is formed by the fourth thin film transistor **T4** and the fifth thin film transistor **T5**. A micro-short circuit path occurs between the first control signal **GAS1** (**Vsp**) and the second direct-current voltage **VGL** (**Vsn**).

[0045] As such, the power consumption is high due to the above competition relationships.

[0046] In the display device of the present disclosure, as shown in FIG. 3, after the first stage ends and before the second stage starts, the scan direction signal **U2D/D2U** is pulled up to the high voltage level **Vsp** from the low voltage level **Vsn** for a predetermined time duration and then pulled down back to the low voltage level **Vsn**. The predetermined time duration may be acquired according to characteristics of the display device (e.g., a frame rate). The scan direction signal **U2D/D2U** having the high voltage level **Vsp** clears the second gate of the second thin film transistor **T2** (i.e., pulls down to the low voltage level **Vsn**), so that the second gate of the second thin film transistor **T2** is turned off. As such, the competition path is not formed by the second thin film transistor **T2** and the third thin film transistor **T3**. The first control signal **GAS1** turns on the third thin film transistor **T3**. The pull-down control node **P** is pulled down to the low voltage level **Vsn**, and thus the fourth thin film transistor **T4** is turned off. As such, the competition path is not formed by the fourth thin film transistor **T4** and the fifth

thin film transistor **T5**. The output node **GATE_OUT** can output the high voltage level **Vsp**.

[0047] In another embodiment, the scan direction signal **U2D/D2U** may be converted to the low voltage level **Vsn** from the high voltage level **Vsp** for a predetermined time duration and then converted back to the high voltage level **Vsp**. That is, in the present disclosure, the scan direction signal **U2D/D2U** may be converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level. When the first voltage level is the low voltage level **Vsn**, the second voltage level is the high voltage level **Vsp**. When the first voltage level is the high voltage level **Vsp**, the second voltage level is the low voltage level **Vsn**.

[0048] In the pull-down circuit and the display device of the present disclosure, the power consumption in the LPWG mode can be reduced by converting the scan direction signal to the second voltage level from the first voltage level for a predetermined time duration and then converting the second voltage level back to the first voltage level.

[0049] In summary, although the present disclosure has been provided in the preferred embodiments described above, the foregoing preferred embodiments are not intended to limit the present disclosure. Those skilled in the art, without departing from the spirit and scope of the present disclosure, may make modifications and variations, so the scope of the protection of the present disclosure is defined by the claims.

What is claimed is:

1. A pull-down circuit of a gate driving unit, utilized for a display device, the pull-down circuit of the gate driving unit comprising:

- a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain;
- a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain;

- a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and
- a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the second direct-current voltage,

wherein the first thin film transistor, the second thin film transistor, the third thin film transistor, and the fourth thin film transistor are N-channel metal-oxide-semiconductor field-effect transistors.

2. The pull-down circuit of the gate driving unit of claim 1, further comprising:

- a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.

3. The pull-down circuit of the gate driving unit of claim 2, further comprising:

- a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.
4. The pull-down circuit of the gate driving unit of claim 1, wherein in a first stage, the display device is configured to sense at least one touch signal, in a second stage, the display device is configured to display an image.
5. The pull-down circuit of the gate driving unit of claim 4, wherein after the first stage ends and before the second stage starts, the scan direction signal is converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.
6. A pull-down circuit of a gate driving unit, utilized for a display device, the pull-down circuit of the gate driving unit comprising:
- a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain;
 - a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain;
 - a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and
 - a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the second direct-current voltage.
7. The pull-down circuit of the gate driving unit of claim 6, further comprising:
- a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.
8. The pull-down circuit of the gate driving unit of claim 7, further comprising:
- a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.
9. The pull-down circuit of the gate driving unit of claim 6, wherein in a first stage, the display device is configured to sense at least one touch signal, in a second stage, the display device is configured to display an image.
10. The pull-down circuit of the gate driving unit of claim 9, wherein after the first stage ends and before the second stage starts, the scan direction signal is converted up to a

second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.

11. A display device having a display area and a non-display area, the display device comprising:
- a plurality of source lines and a plurality of gate lines disposed on the display area;
 - at least one source driving unit disposed on the non-display area and configured to provide data signals for the source lines; and
 - at least one gate driving unit disposed on the non-display area and configured to provide scan signals for the gate lines,
- wherein the gate driving unit at least comprises a pull-down circuit, and the pull-down circuit comprises:
- a first thin film transistor having a first gate, a first source and a first drain, a scan direction signal inputted to the first gate, and a clock signal inputted to the first drain;
 - a second thin film transistor having a second gate, a second source and a second drain, the second gate electrically coupled to the first source, the second source electrically coupled to a pull-down control node, and a first direct-current voltage inputted to the second drain;
 - a third thin film transistor having a third gate, a third source and a third drain, a first control signal inputted to the third gate, the third source electrically coupled to the pull-down control node, and the third drain electrically coupled to a second direct-current voltage; and
 - a fourth thin film transistor having a fourth gate, a fourth source and a fourth drain, the fourth gate electrically coupled to the pull-down control node, the fourth source electrically coupled to an output node, and the fourth drain electrically coupled to the second direct-current voltage.
12. The display device of claim 11, further comprising:
- a fifth thin film transistor having a fifth gate, a fifth source and a fifth drain, the first control signal inputted to the fifth gate and the fifth drain, and the fifth source electrically coupled to the output node.
13. The display device of claim 12, further comprising:
- a sixth thin film transistor having a sixth gate, a sixth source and a sixth drain, a second control signal inputted to the sixth gate, the sixth source electrically coupled to the second direct-current voltage, and the sixth drain electrically coupled to the output node.
14. The display device of claim 11, wherein in a first stage, the display device is configured to sense at least one touch signal, in a second stage, the display device is configured to display an image.
15. The display device of claim 14, wherein after the first stage ends and before the second stage starts, the scan direction signal is converted up to a second voltage level from a first voltage level for a predetermined time duration and then converted back to the first voltage level.