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(54) **SINGLE-INDUCTOR MULTIPLE-OUTPUT (SIMO) CONVERTER AND CONTROL METHOD OF SIMO CONVERTER**

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(52) **U.S. Cl.**

CPC ***H02M 3/157*** (2013.01); *H02M 2001/009* (2013.01); ***H02M 1/00*** (2013.01)

(57) **ABSTRACT**

A single-inductor multiple-output (SIMO) converter includes a converter configured to provide respective voltages of a plurality of channels with a single inductor and a control logic configured to control switches of the converter based on clocks corresponding to the plurality of channels, wherein the control logic is configured to compare an output voltage of a selected channel of the plurality of channels that corresponds to a control target to a reference voltage of the selected channel based on a clock of the selected channel and operate in one of a first mode that adaptively adjusts a number of times that a pulse triggering a power transfer to the channel is generated, and a second mode that blocks a generation of the pulse.

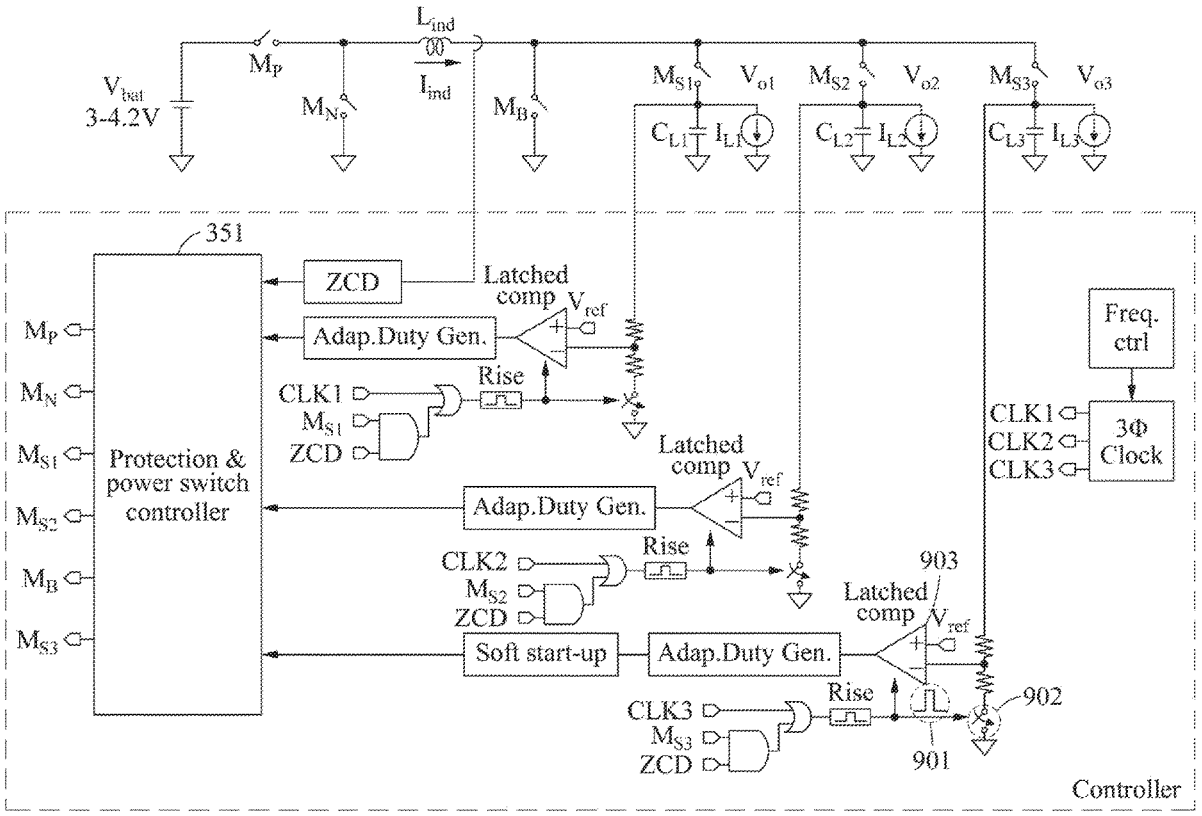
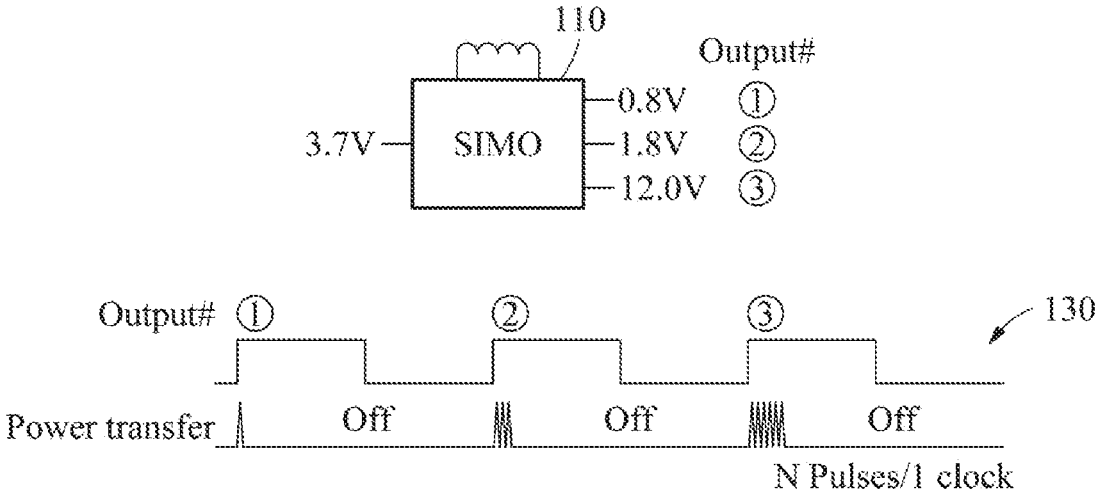


FIG. 1


110
Output#
3.7V
SIMO
0.8V ①
1.8V ②
12.0V ③
Output# ① ② ③
130
Power transfer
Off
Off
Off
N Pulses/1 clock

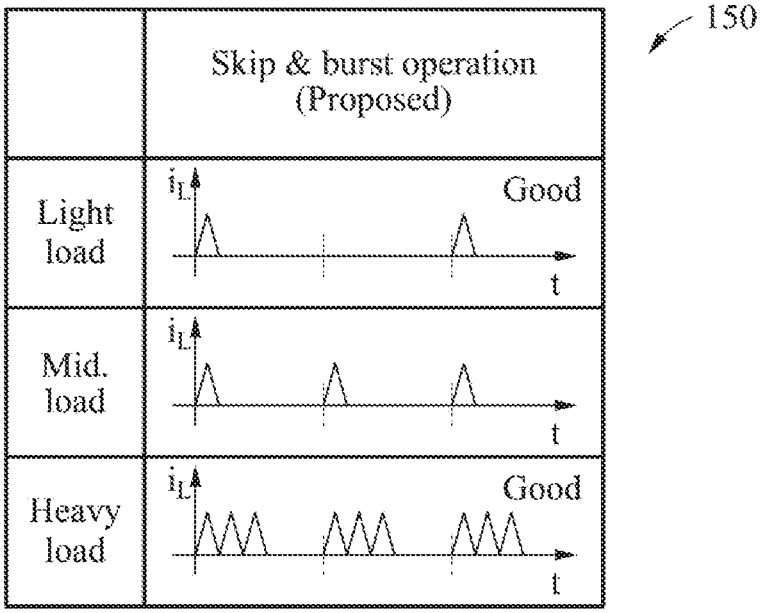

150
Skip & burst operation (Proposed)
Light load
Mid. load
Heavy load
Good
Good
i_L
t

FIG. 2

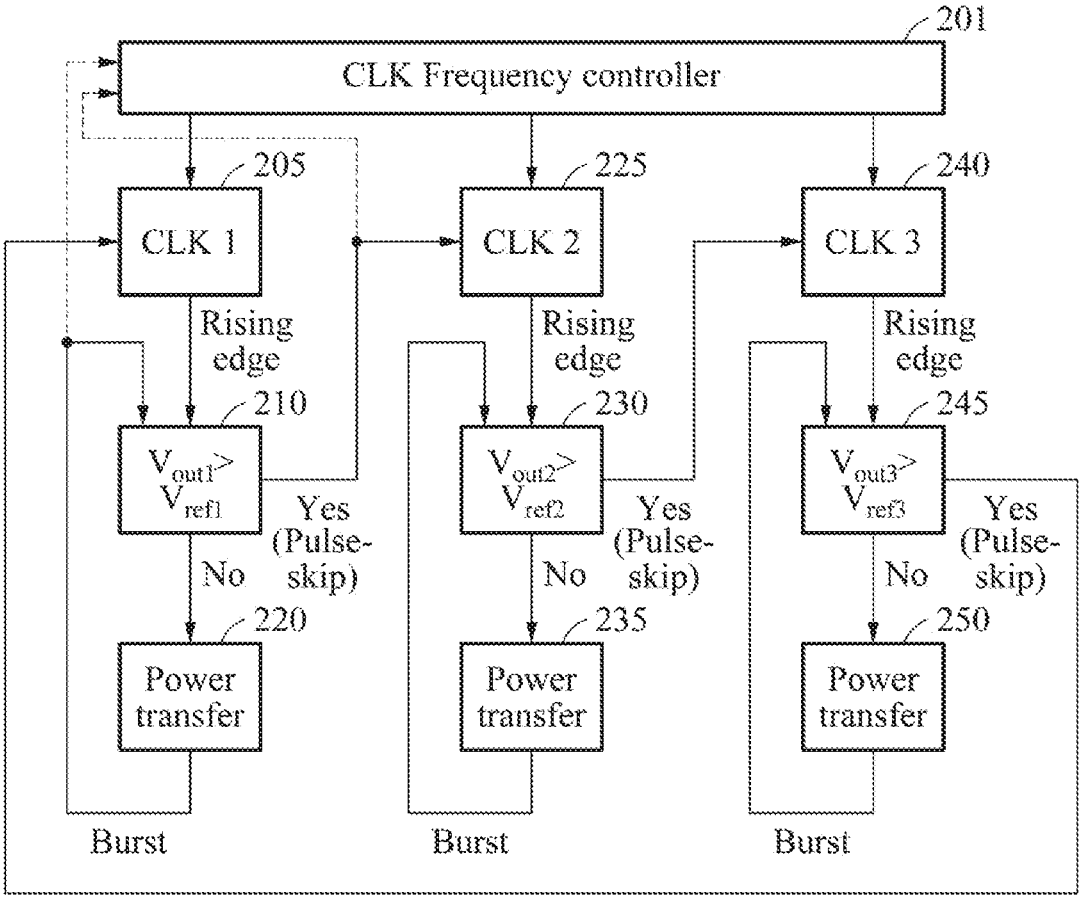

201
CLK Frequency controller
205
CLK 1
225
CLK 2
240
CLK 3
Rising edge
Rising edge
Rising edge
210
230
245
$V_{out1} > V_{ref1}$
$V_{out2} > V_{ref2}$
$V_{out3} > V_{ref3}$
Yes (Pulse-skip)
Yes (Pulse-skip)
Yes (Pulse-skip)
No
No
No
220
235
250
Power transfer
Power transfer
Power transfer
Burst
Burst
Burst

FIG. 3

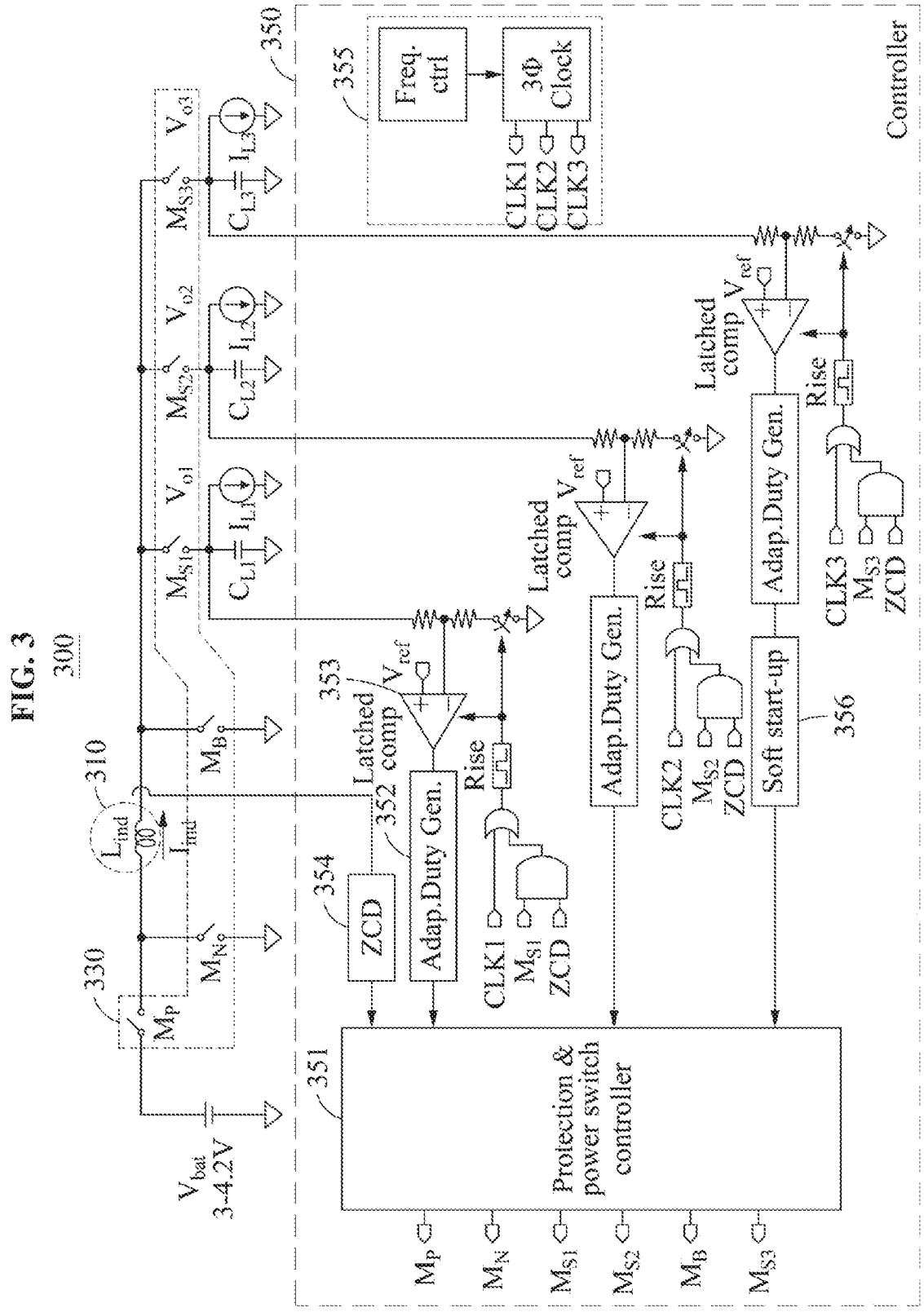

300
310
330
350
355
351
352
353
354
356
Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
Protection & power switch controller
Soft start-up
Adap.Duty Gen.
Latched comp
Rise
ZCD
V_{bat} 3-4.2V
L_{ind}
I_{ind}
M_P
M_N
M_B
M_{S1}
M_{S2}
M_{S3}
V_{o1}
V_{o2}
V_{o3}
I_{L1}
I_{L2}
I_{L3}
C_{L1}
C_{L2}
C_{L3}
V_{ref}

FIG. 4

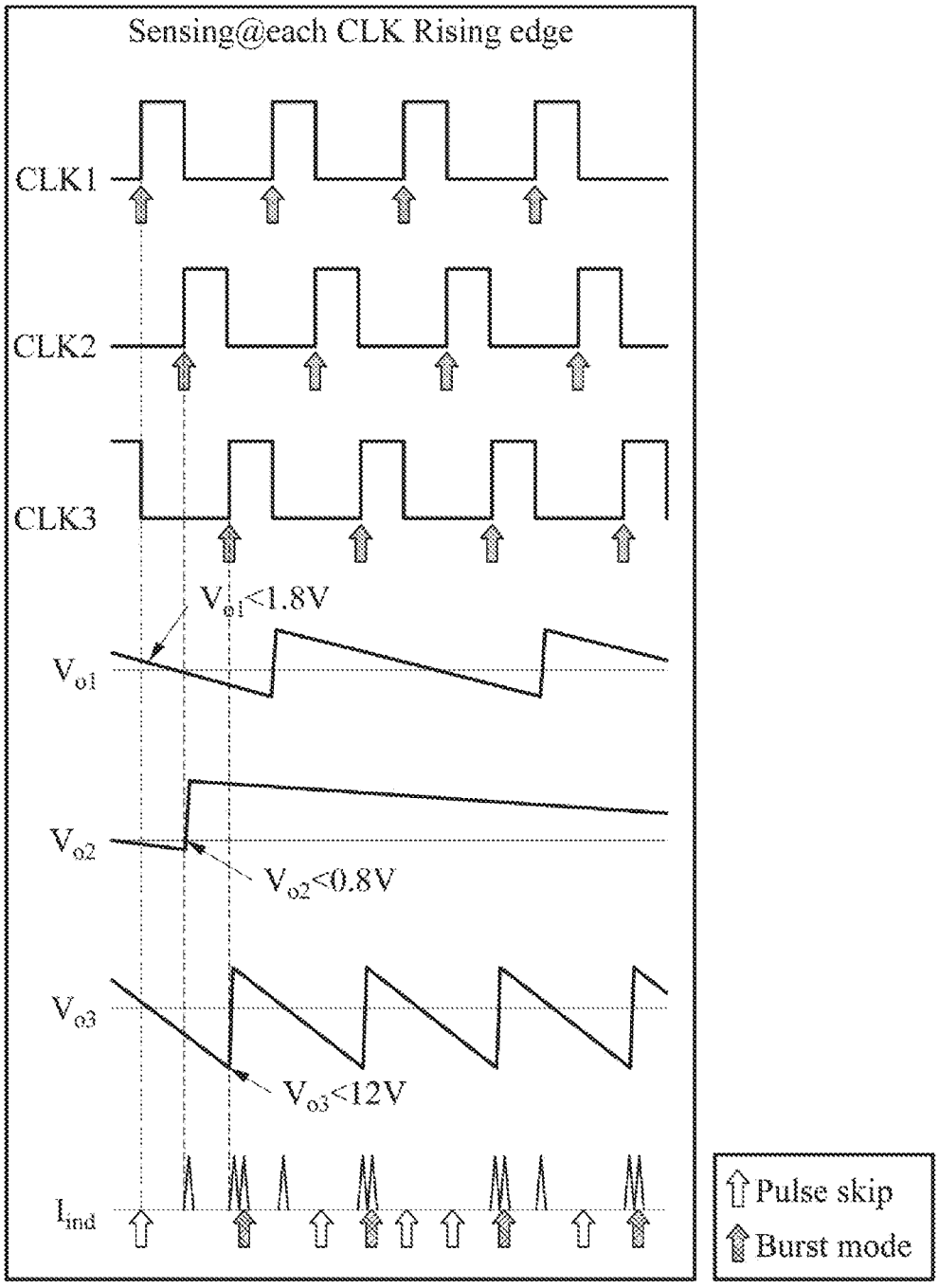

Sensing@each CLK Rising edge
CLK1
CLK2
CLK3
V_{o1}<1.8V
V_{o1}
V_{o2}
V_{o2}<0.8V
V_{o3}
V_{o3}<12V
I_{ind}
Pulse skip
Burst mode

FIG. 5A

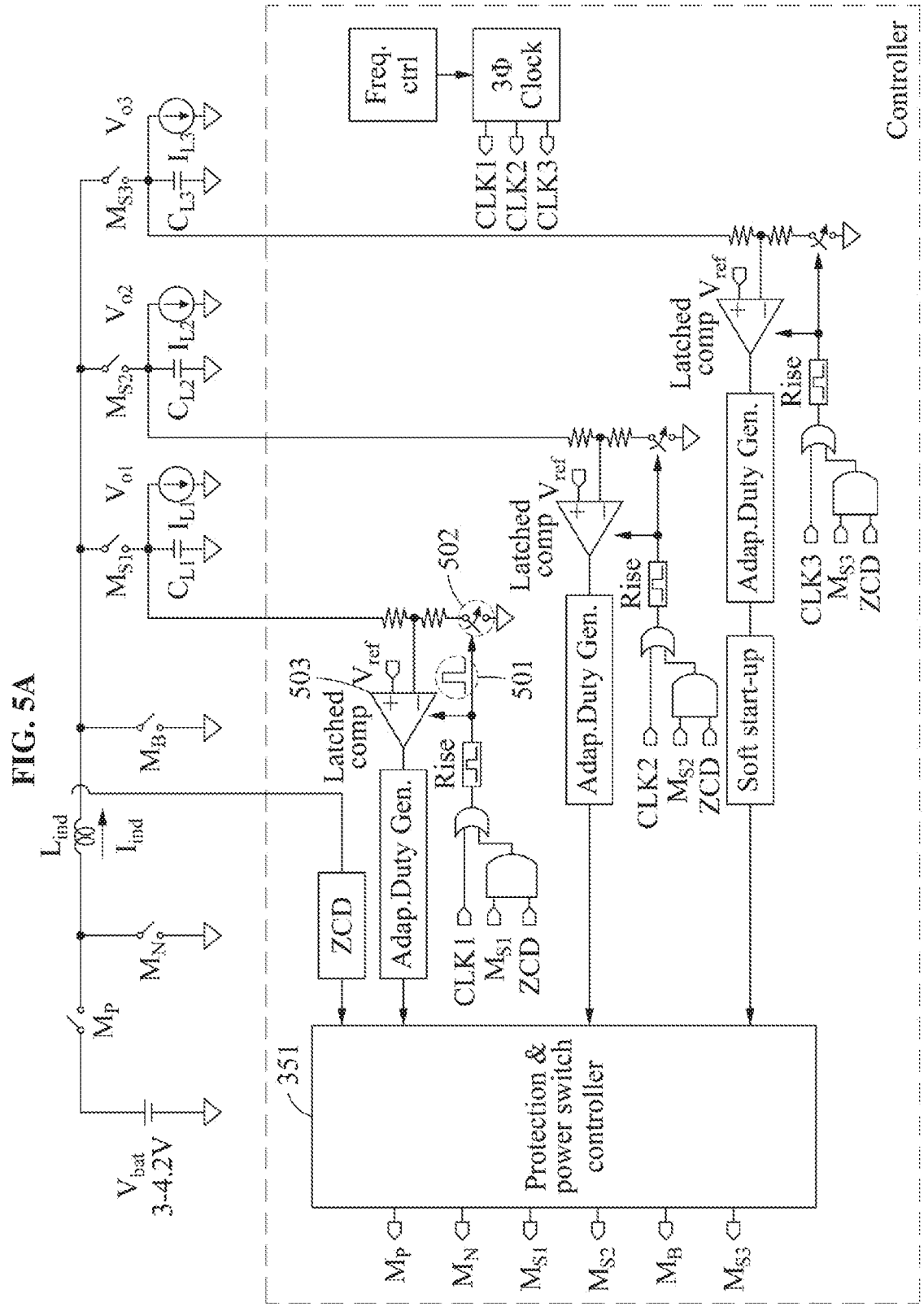

Controller
Freq. ctrl
3φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3}
C_{L3} I_{L3}
V_{o2}
M_{S2}
C_{L2} I_{L2}
V_{o1}
M_{S1}
C_{L1} I_{L1}
M_B
L_{ind}
I_{ind}
M_P
M_N
V_{bat}
3-4.2V
351
Protection & power switch controller
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
503
501
502
Rise
Soft start-up
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
CLK2
M_{S2}
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
CLK3
M_{S3}
ZCD
CLK1
M_{S1}
ZCD
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}

FIG. 5B

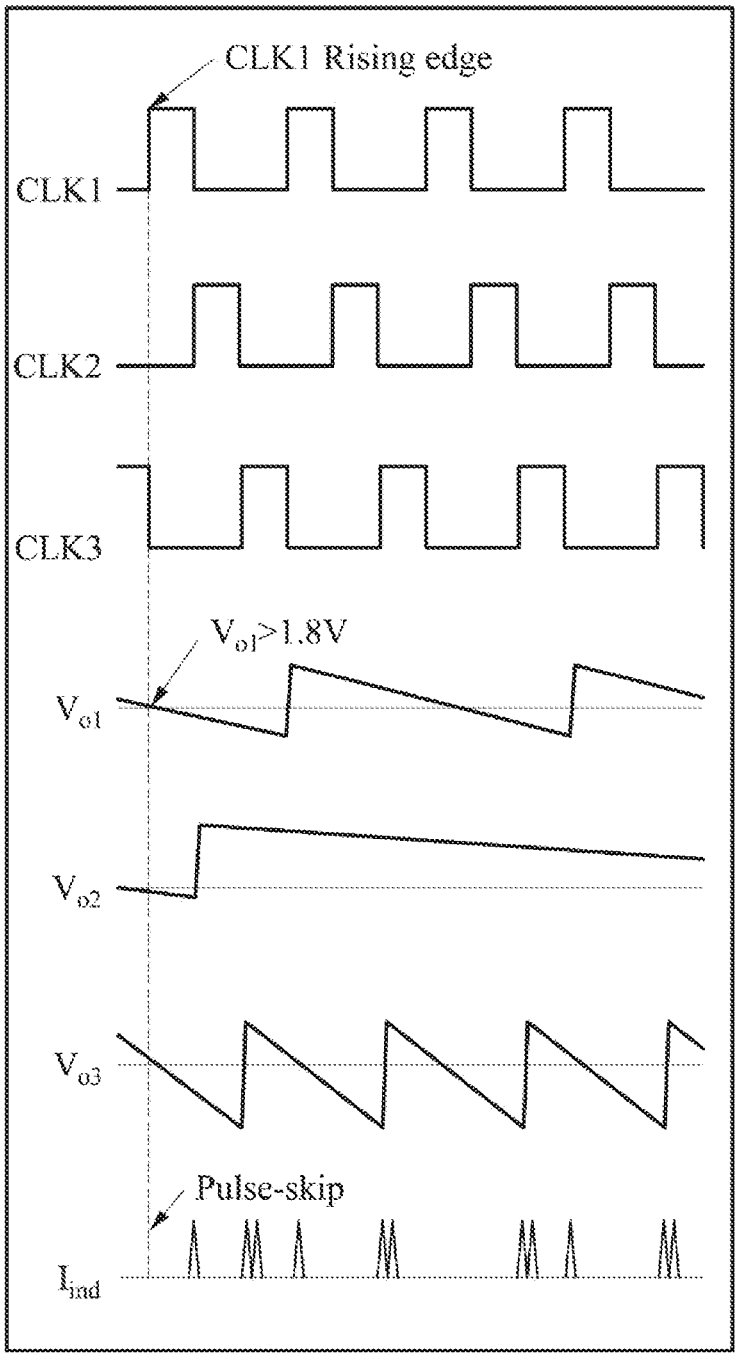

CLK1 Rising edge
CLK1
CLK2
CLK3
V_{o1}>1.8V
V_{o1}
V_{o2}
V_{o3}
Pulse-skip
I_{ind}

FIG. 6A

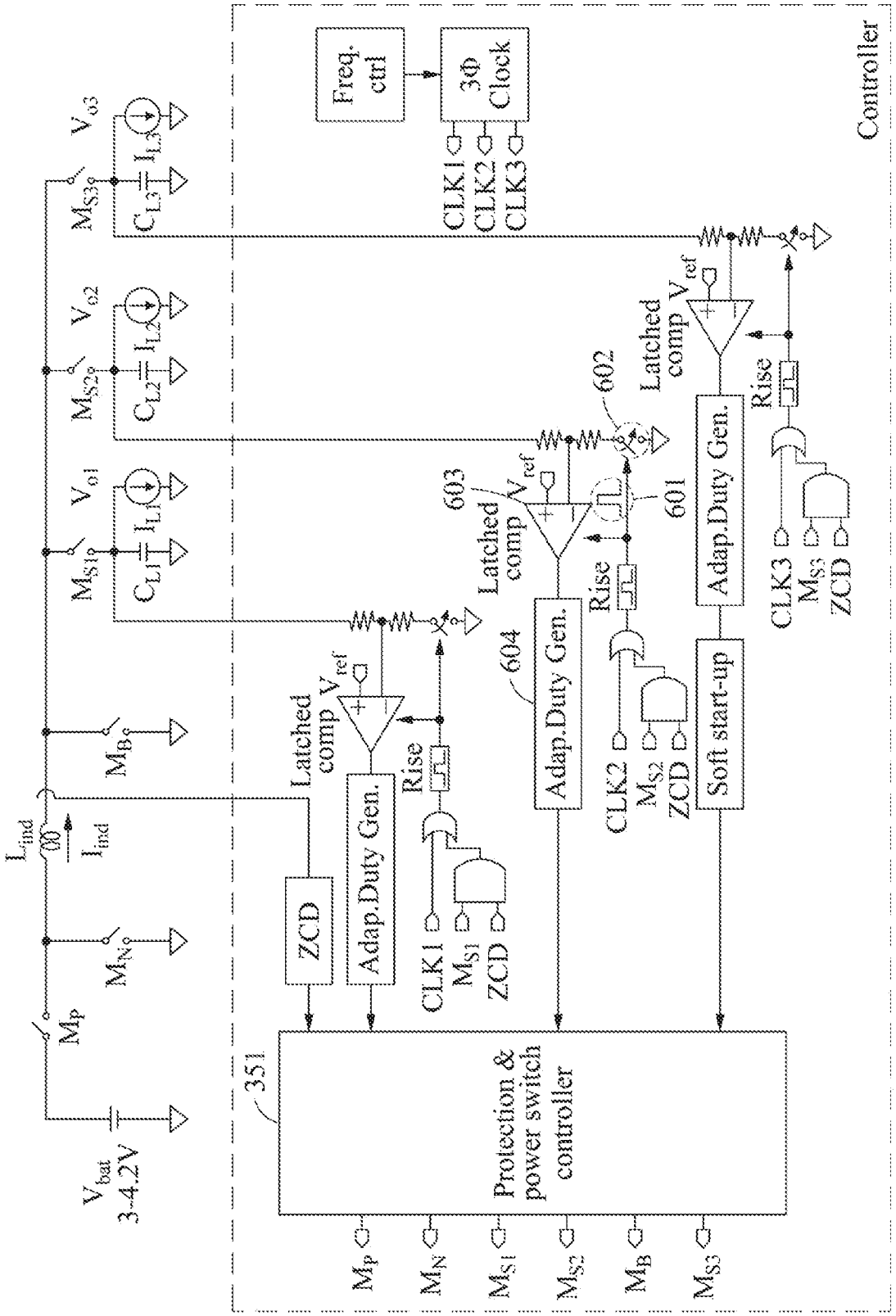

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3}
C_{L3}
I_{L3}
V_{o2}
M_{S2}
C_{L2}
I_{L2}
V_{o1}
M_{S1}
C_{L1}
I_{L1}
602
603
601
604
Latched comp
V_{ref}
Rise
Adap.Duty Gen.
Soft start-up
ZCD
L_{ind}
I_{ind}
M_P
M_N
M_B
V_{bat} 3-4.2V
351
Protection & power switch controller

FIG. 6B

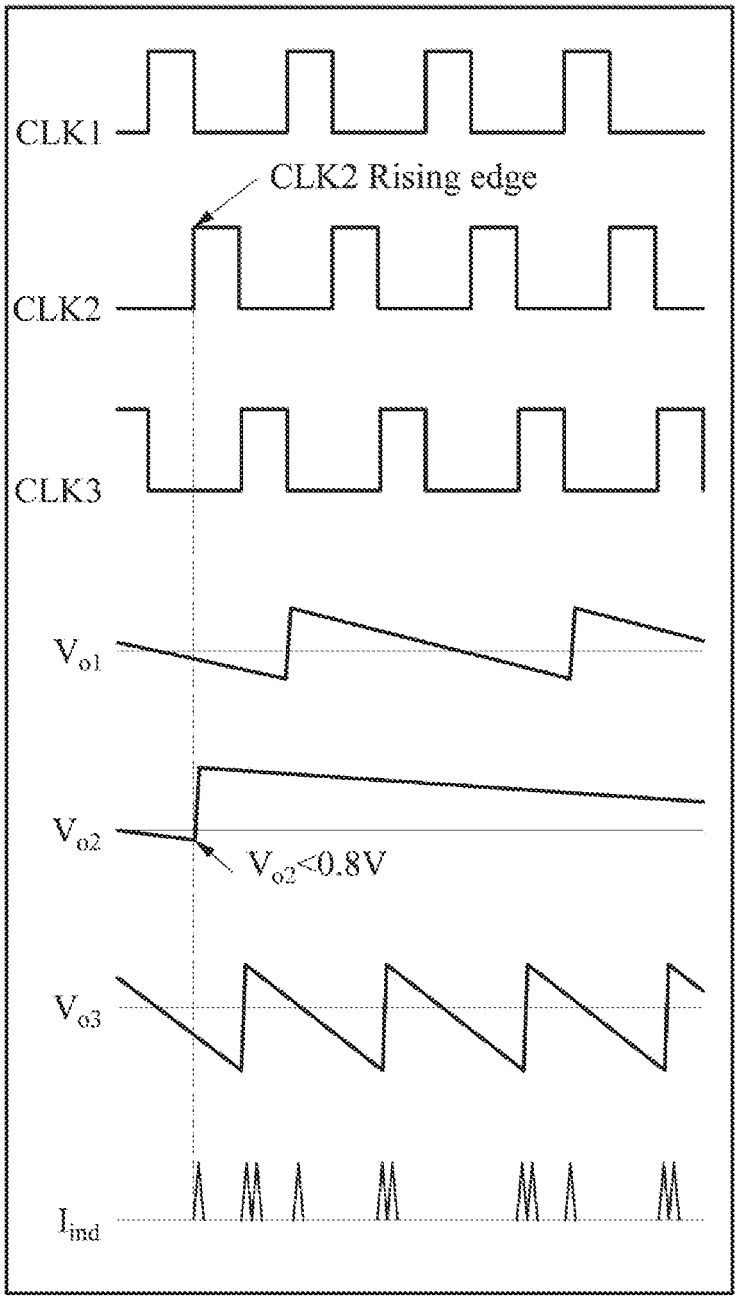


FIG. 7A

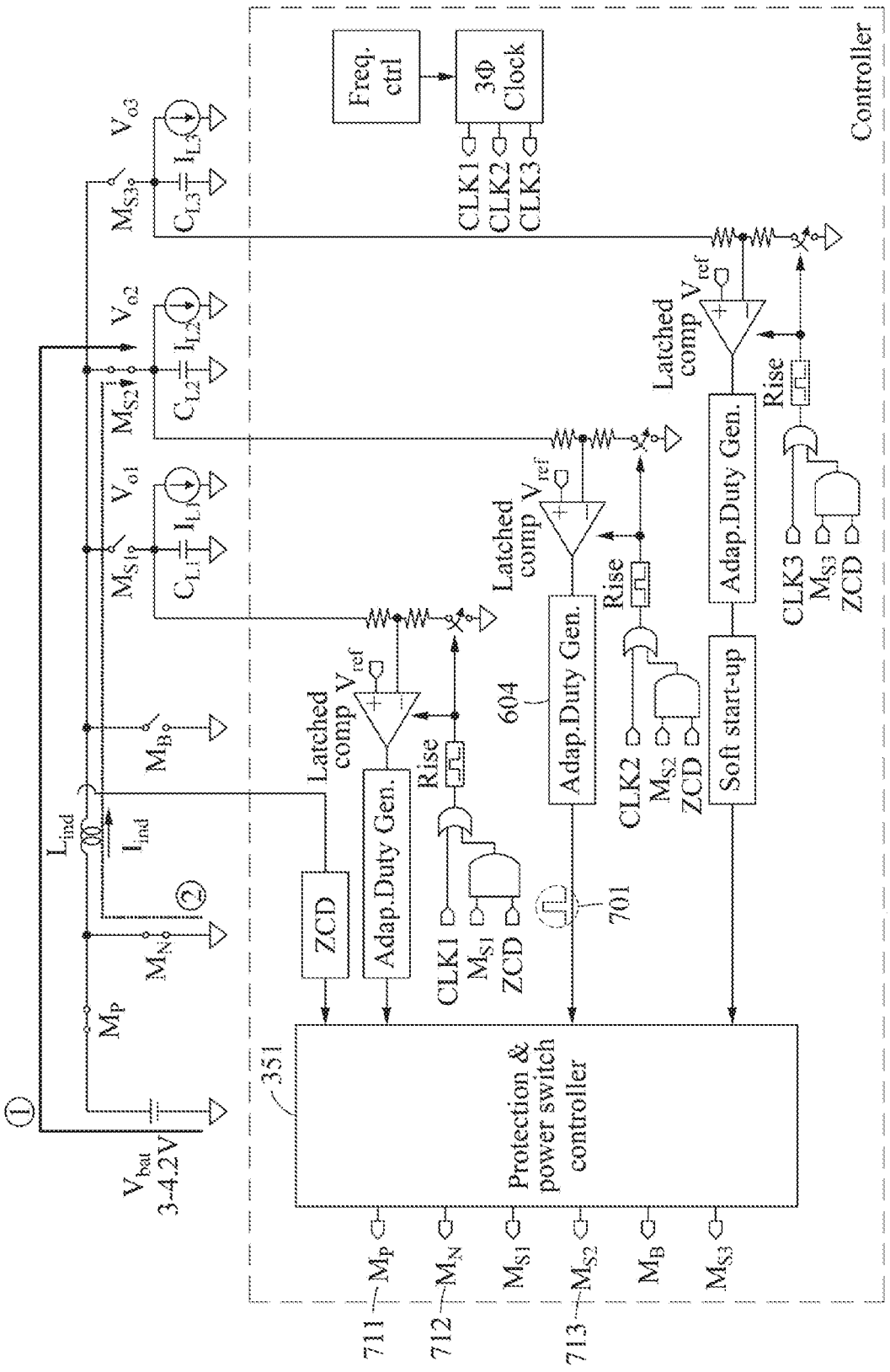

Controller
Freq. ctrl
3φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3}
C_{L3}
I_{L3}
V_{o2}
M_{S2}
C_{L2}
I_{L2}
V_{o1}
M_{S1}
C_{L1}
I_{L1}
M_B
L_{ind}
I_{ind}
M_P
M_N
V_{bat}
3-4.2V
Latched comp V_{ref}
Rise
ZCD
Adap.Duty Gen.
604
701
Soft start-up
Protection & power switch controller
351
711
712
713

FIG. 7B

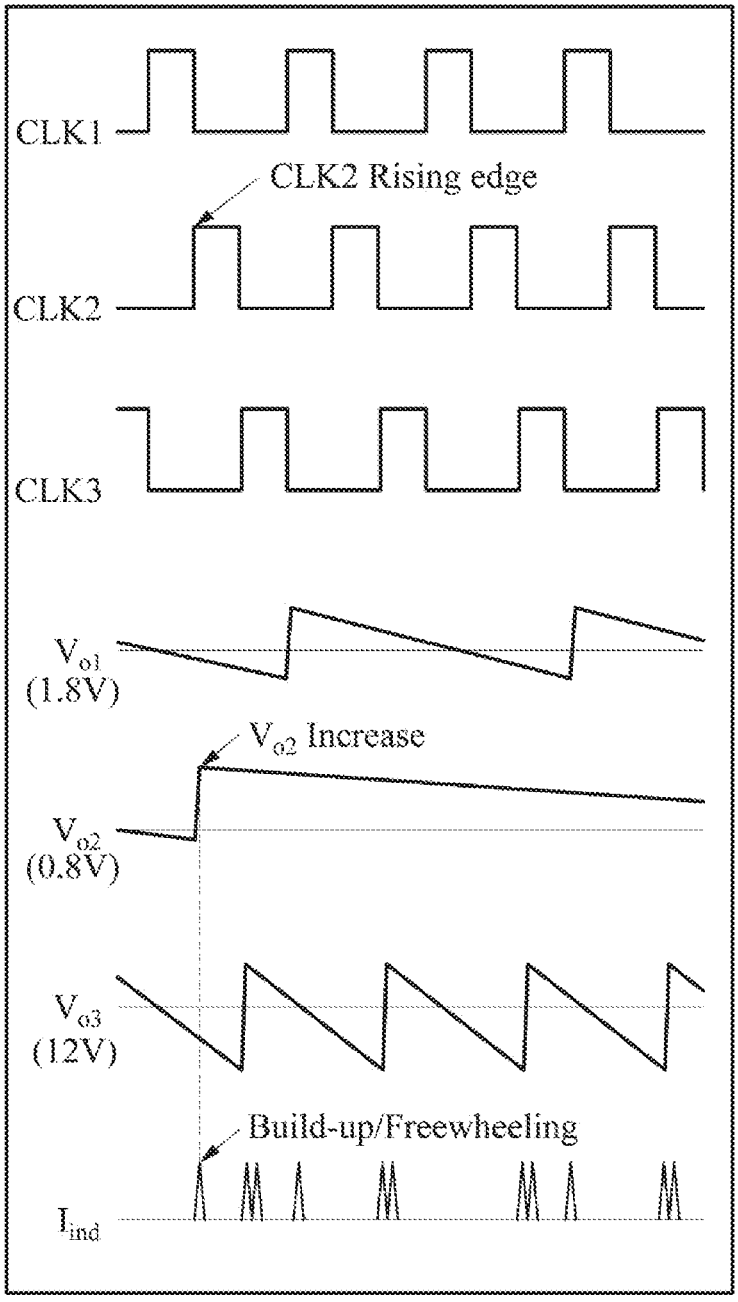

CLK1
CLK2 Rising edge
CLK2
CLK3
V_{o1}
(1.8V)
V_{o2} Increase
V_{o2}
(0.8V)
V_{o3}
(12V)
Build-up/Freewheeling
I_{ind}

FIG. 8A

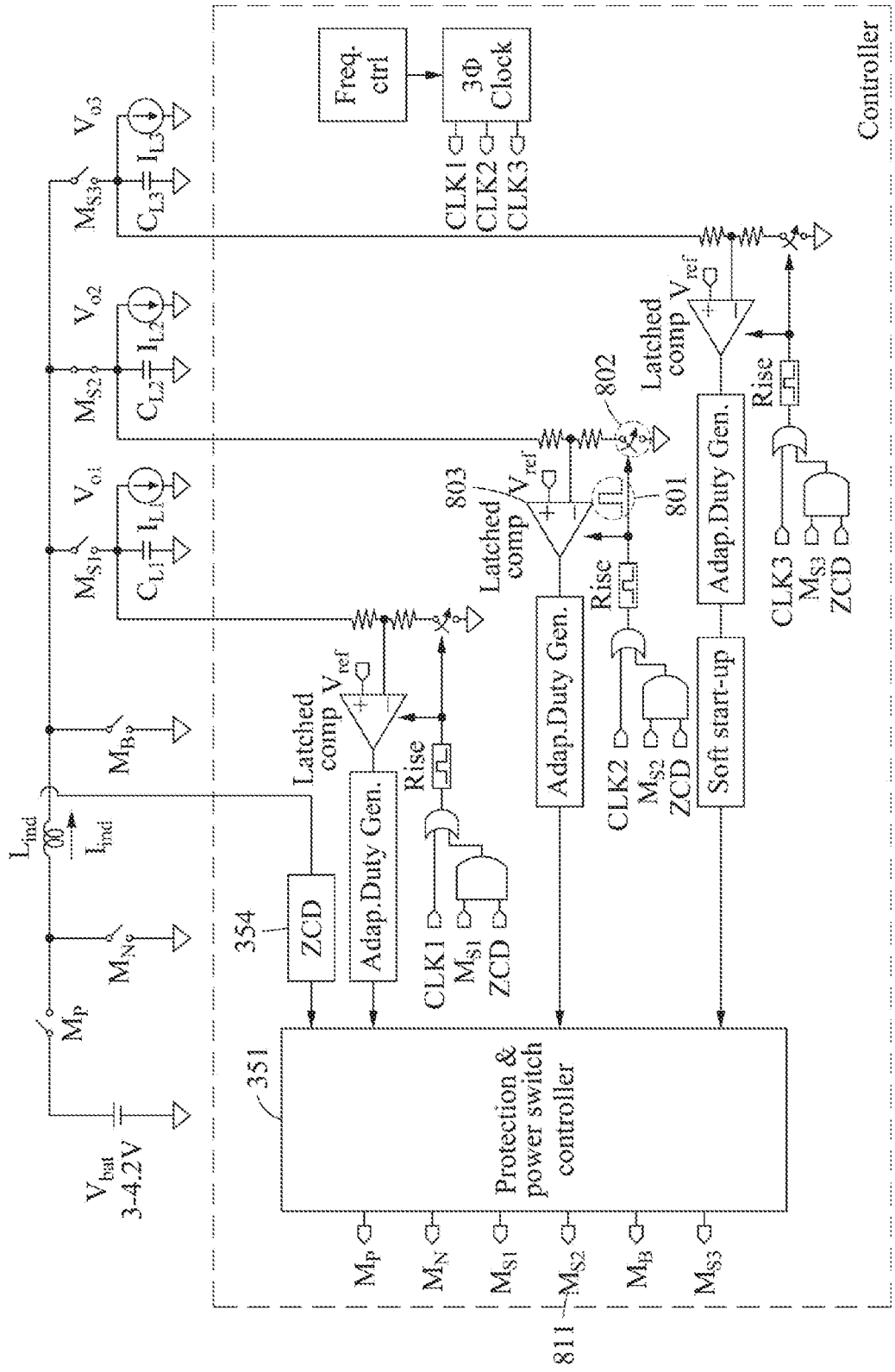

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
V_{o2}
V_{o1}
M_{S3p}
M_{S2p}
M_{S1p}
C_{L3} I_{L3}
C_{L2} I_{L2}
C_{L1} I_{L1}
802
803
801
Latched comp
V_{ref}
Rise
Adap.Duty Gen.
Soft start-up
CLK3
M_{S3}
ZCD
CLK2
M_{S2}
ZCD
CLK1
M_{S1}
ZCD
354
ZCD
351
Protection & power switch controller
M_{Bp}
M_{Np}
M_P
L_{ind}
I_{ind}
V_{bat}
3-4.2V
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}
811

FIG. 8B

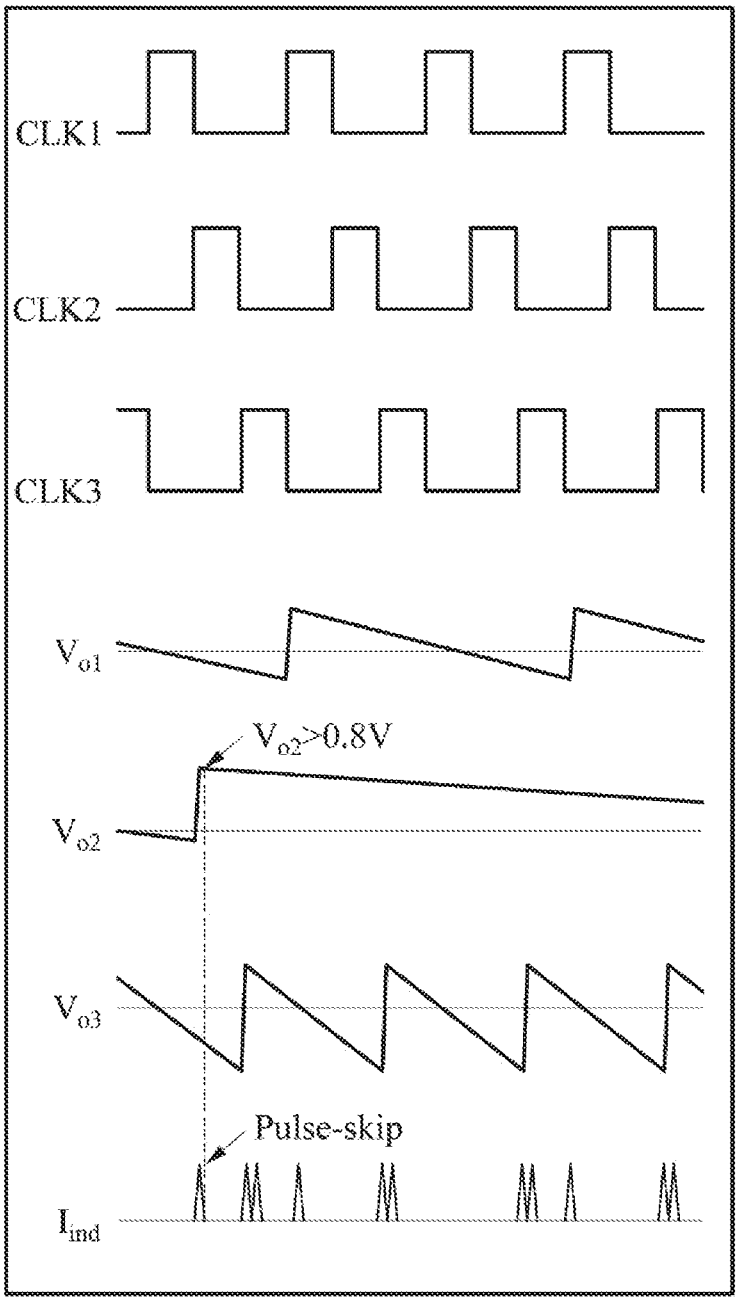


FIG. 9A

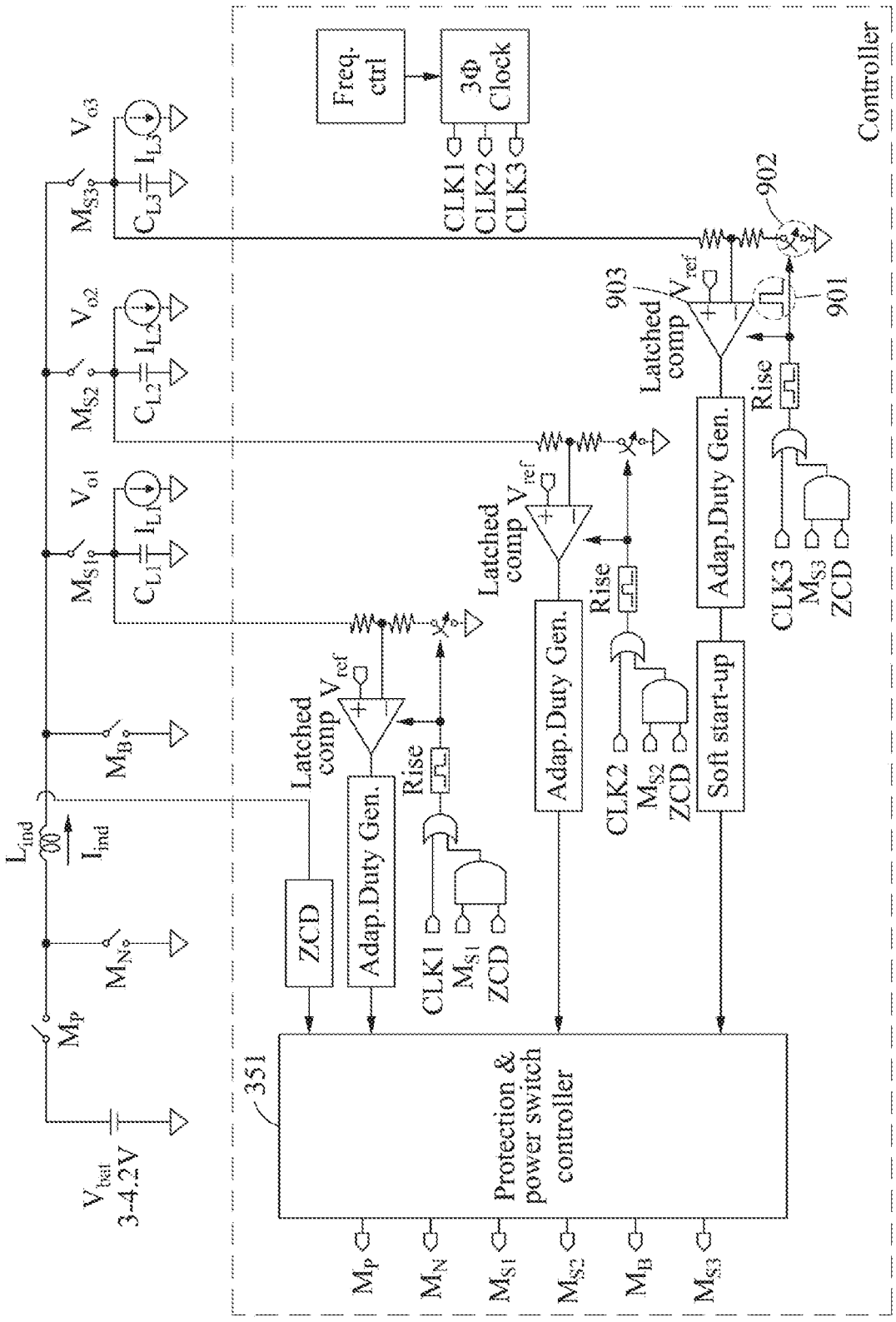

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
902
903
901
Latched comp
V_{ref}
Rise
Adap.Duty Gen.
Soft start-up
ZCD
M_{S3}
M_{S2}
M_{S1}
M_B
M_N
M_P
V_{o3}
V_{o2}
V_{o1}
I_{L3}
I_{L2}
I_{L1}
C_{L3}
C_{L2}
C_{L1}
L_{ind}
I_{ind}
V_{bat}
3-4.2V
351
Protection & power switch controller

FIG. 9B

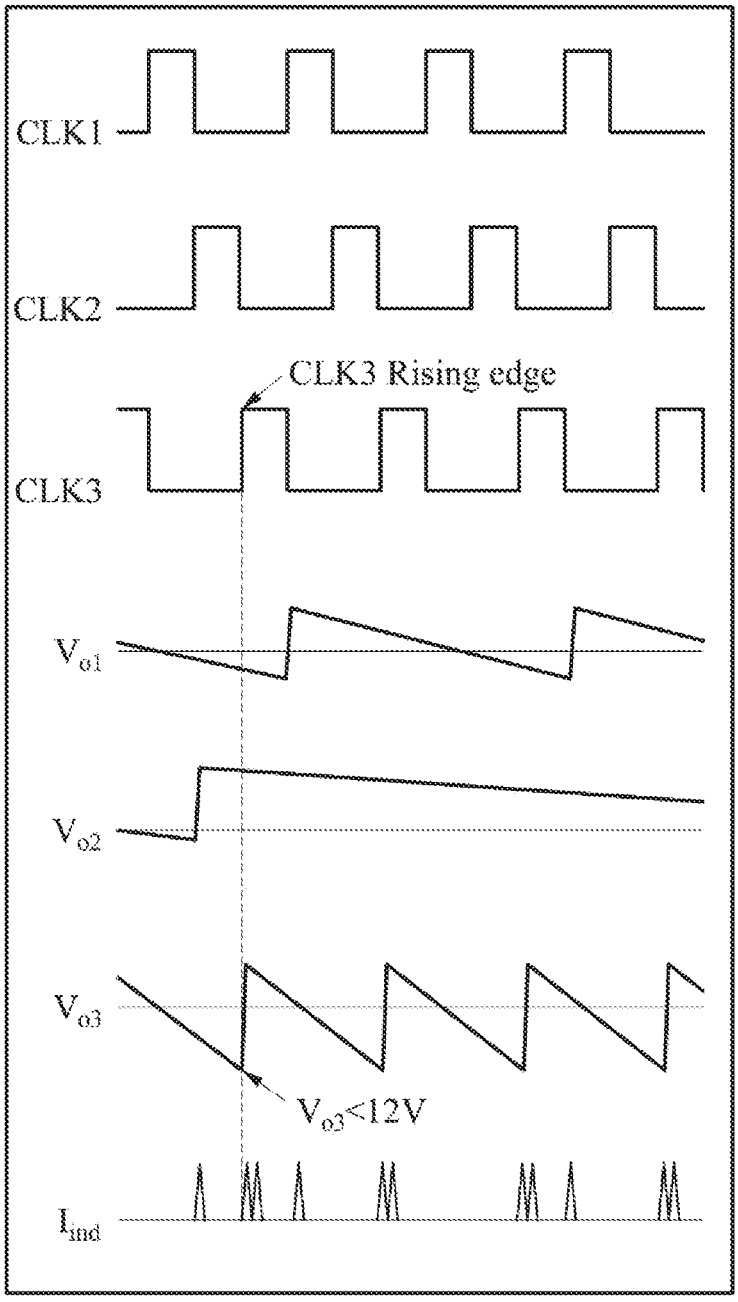


FIG. 10A

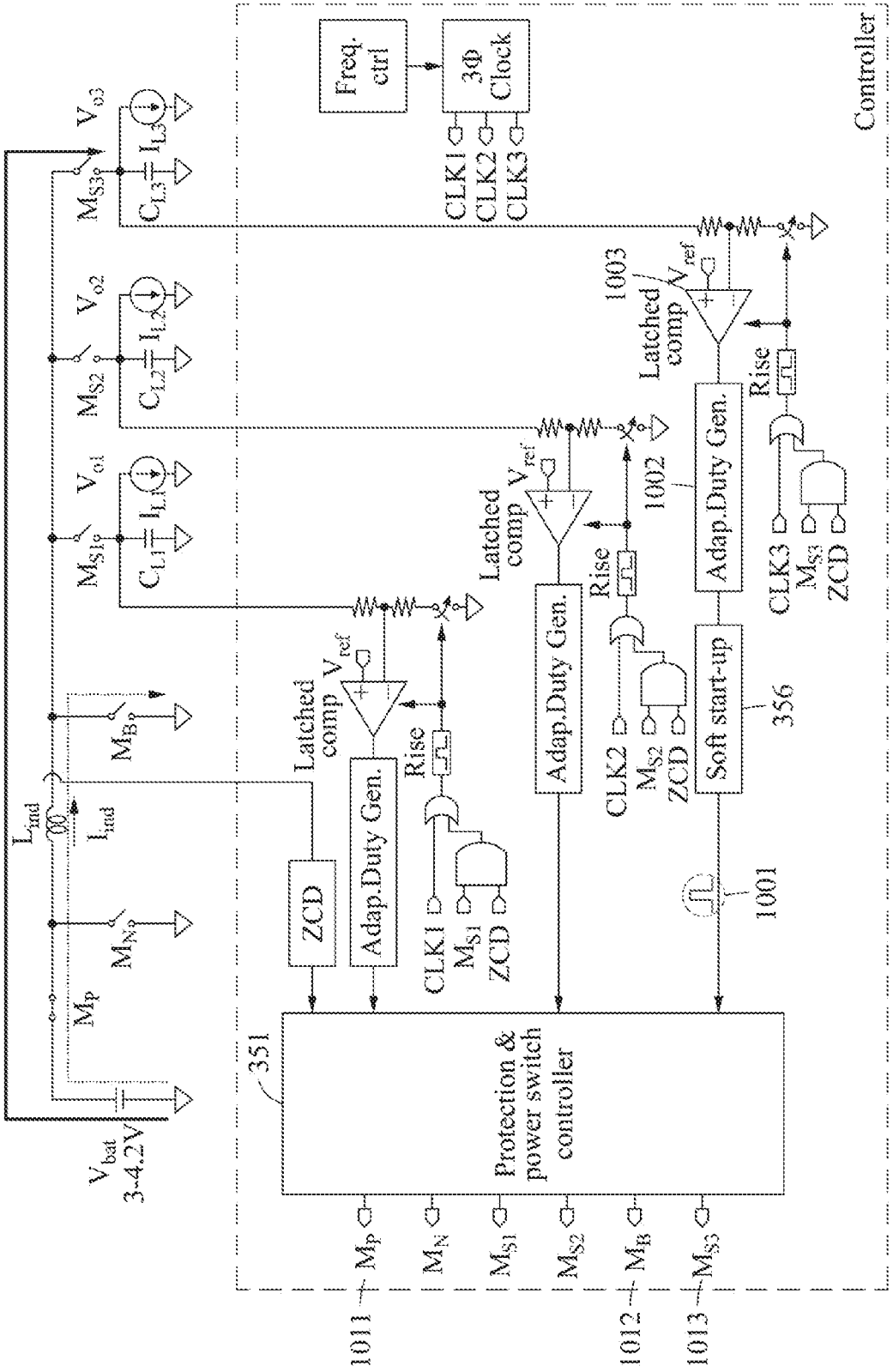

Controller
Freq. ctrl
3φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3P}
C_{L3} I_{L3}
V_{o2}
M_{S2P}
C_{L2} I_{L2}
V_{o1}
M_{S1P}
C_{L1} I_{L1}
M_{BP}
L_{ind}
I_{ind}
M_P
M_N
V_{bat} 3-4.2V
351
Protection & power switch controller
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
CLK1
M_{S1}
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
1002
CLK2
M_{S2}
ZCD
Soft start-up
356
1001
1003
Latched comp
V_{ref}
Rise
Adap.Duty Gen.
CLK3
M_{S3}
ZCD
1011
1012
1013
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}

FIG. 10B

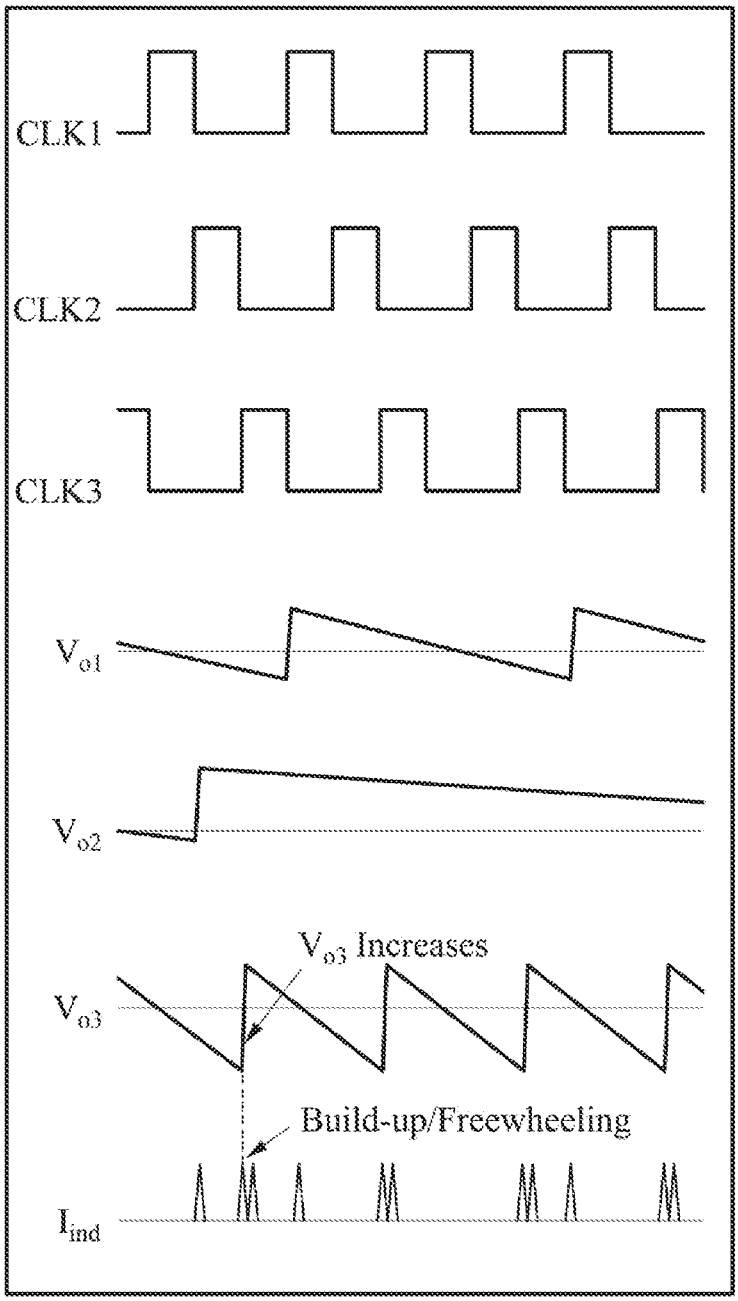

CLK1
CLK2
CLK3
V_{o1}
V_{o2}
V_{o3} Increases
V_{o3}
Build-up/Freewheeling
I_{ind}

FIG. 11A

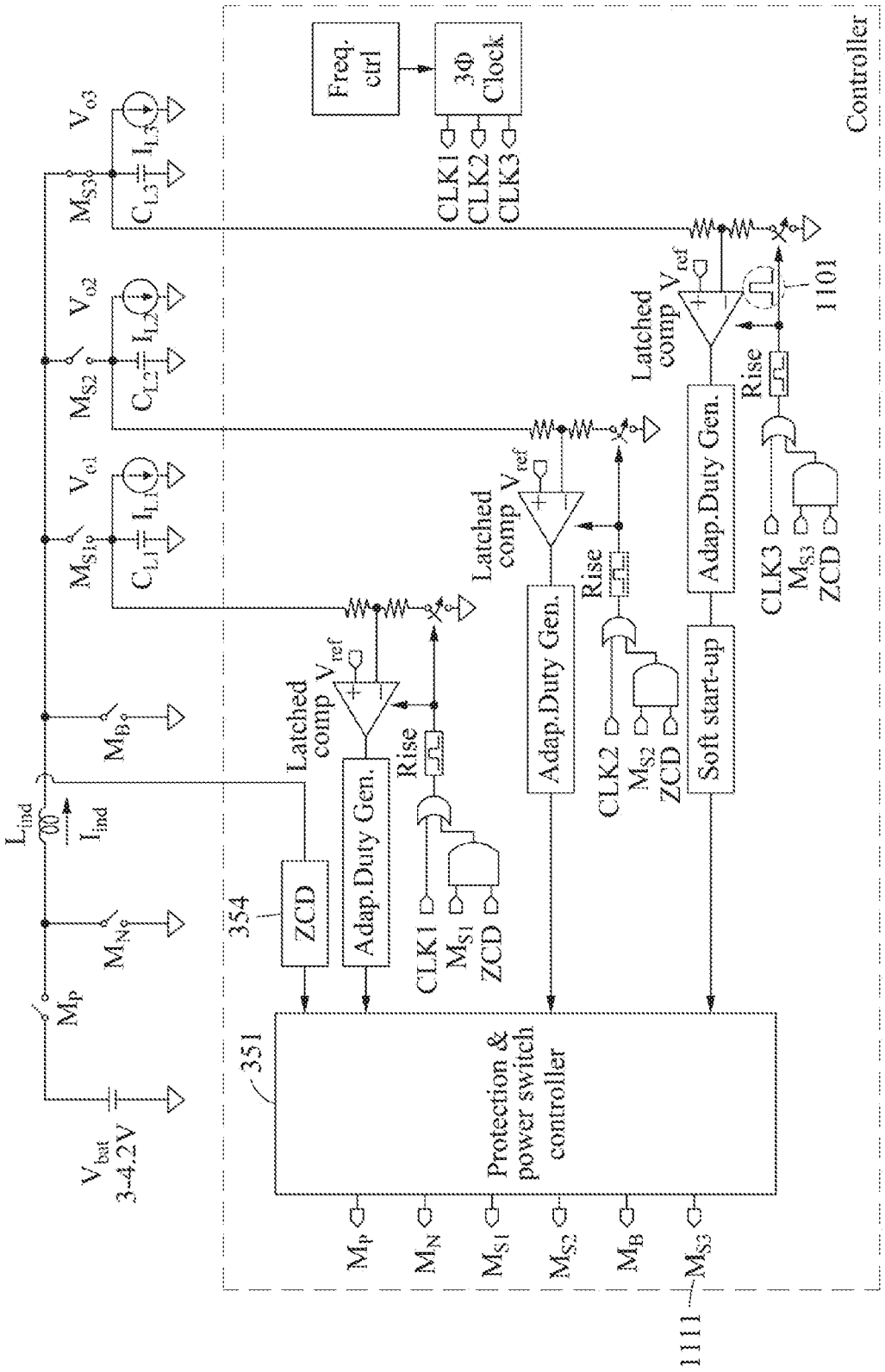

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3}
C_{L3}
I_{L3}
V_{o2}
M_{S2}
C_{L2}
I_{L2}
V_{o1}
M_{S1}
C_{L1}
I_{L1}
L_{ind}
I_{ind}
M_P
M_N
M_B
V_{bat}
3-4.2V
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
Soft start-up
1101
1111
351
354
Protection & power switch controller

FIG. 11B

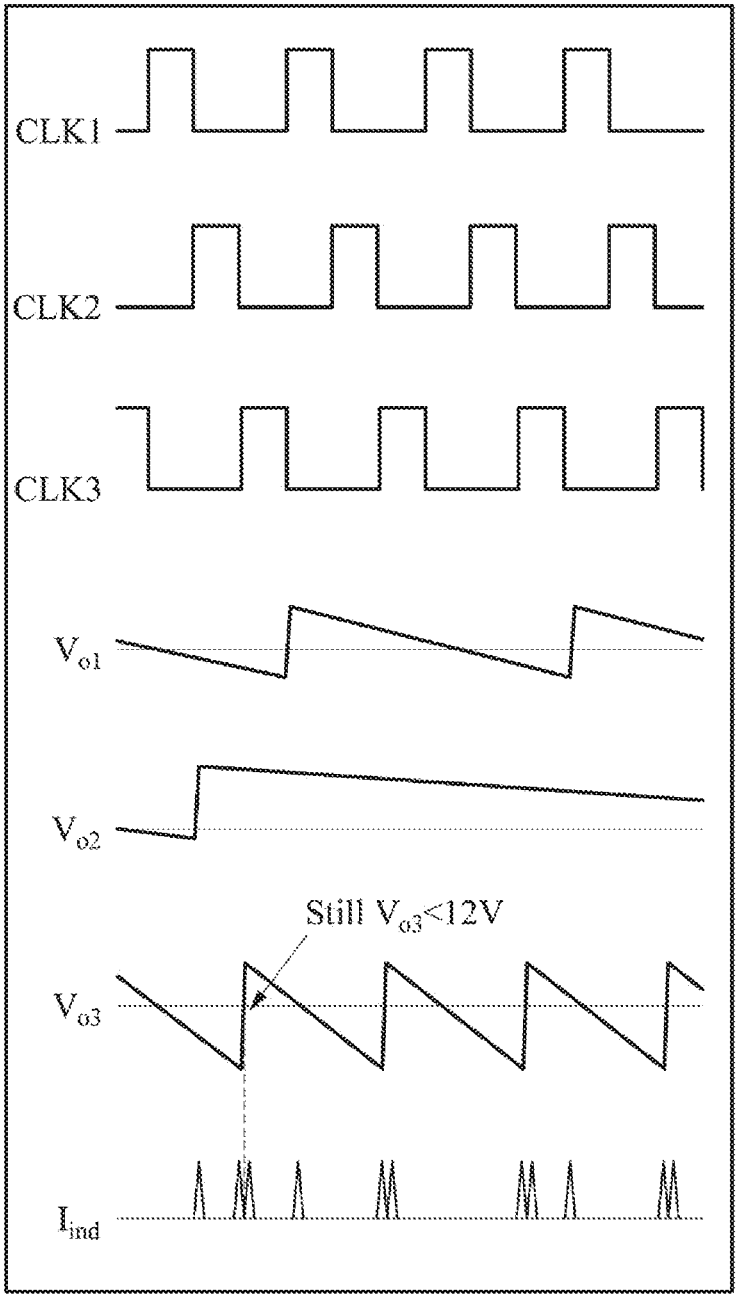


FIG. 12A

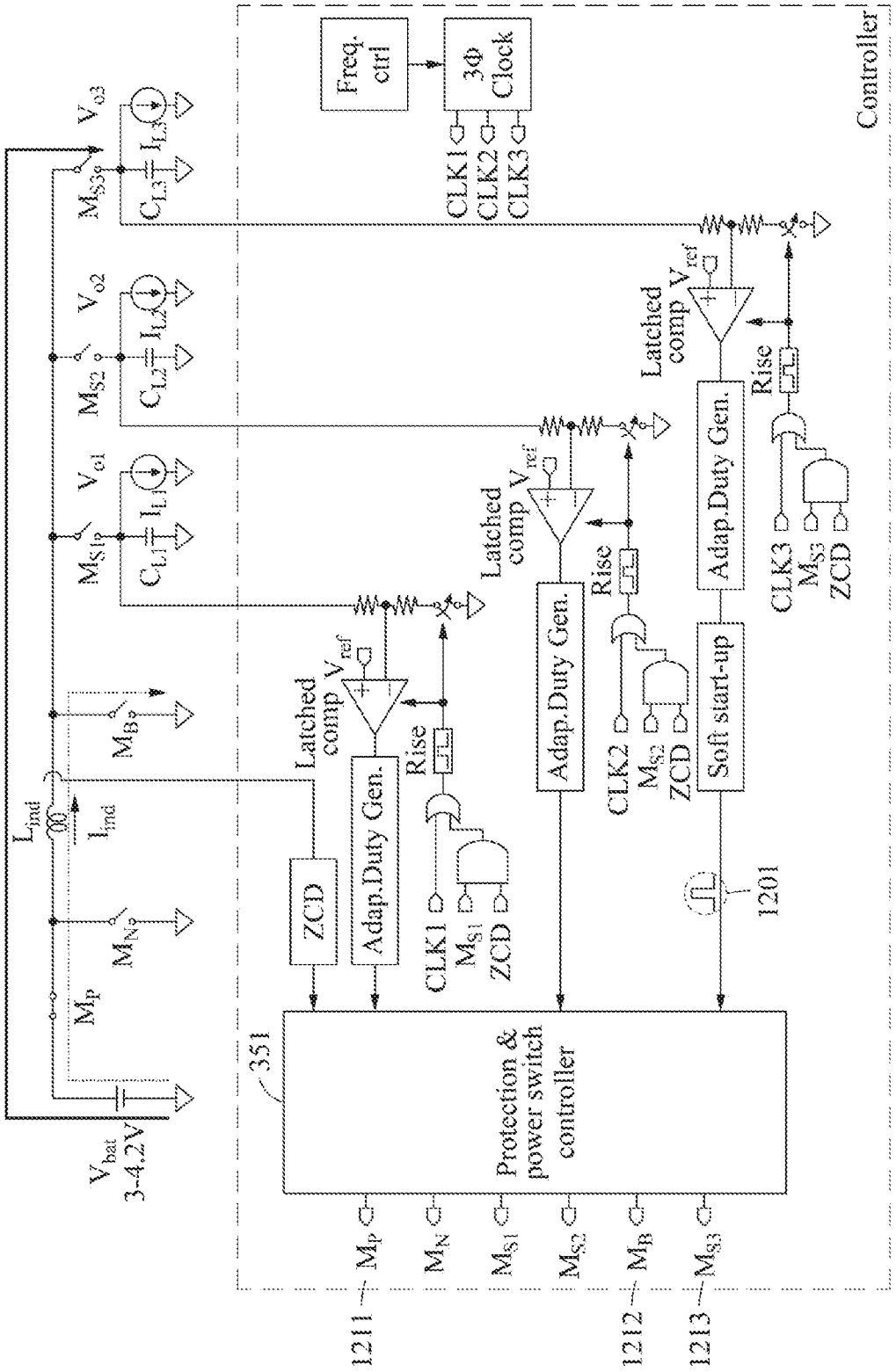

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3P}
C_{L3}
I_{L3}
V_{o2}
M_{S2}
C_{L2}
I_{L2}
V_{o1}
M_{S1P}
C_{L1}
I_{L1}
M_B
L_{ind}
I_{ind}
M_P
M_{NP}
V_{bat}
3-4.2V
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
CLK1
M_{S1}
ZCD
Adap.Duty Gen.
Latched comp V_{ref}
Rise
CLK2
M_{S2}
ZCD
Soft start-up
1201
Adap.Duty Gen.
Latched comp V_{ref}
Rise
CLK3
M_{S3}
ZCD
351
Protection & power switch controller
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}
1211
1212
1213

FIG. 12B

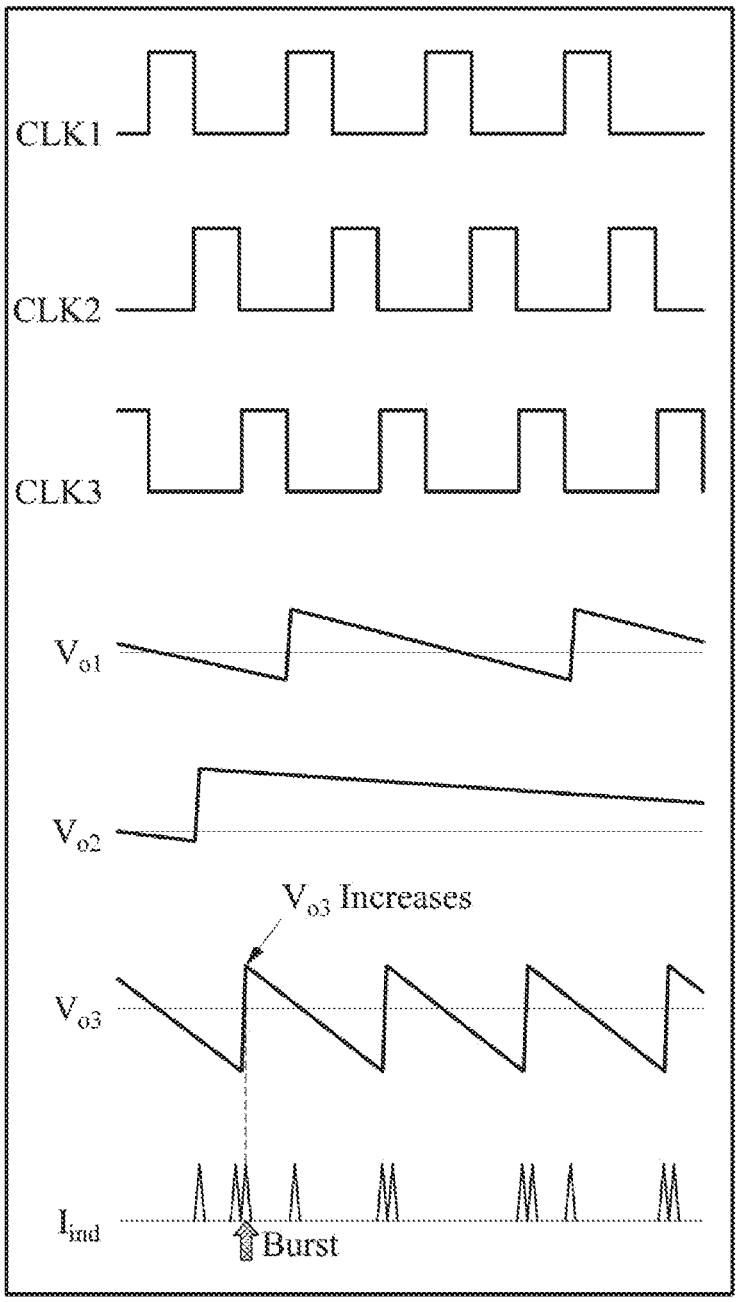


FIG. 13A

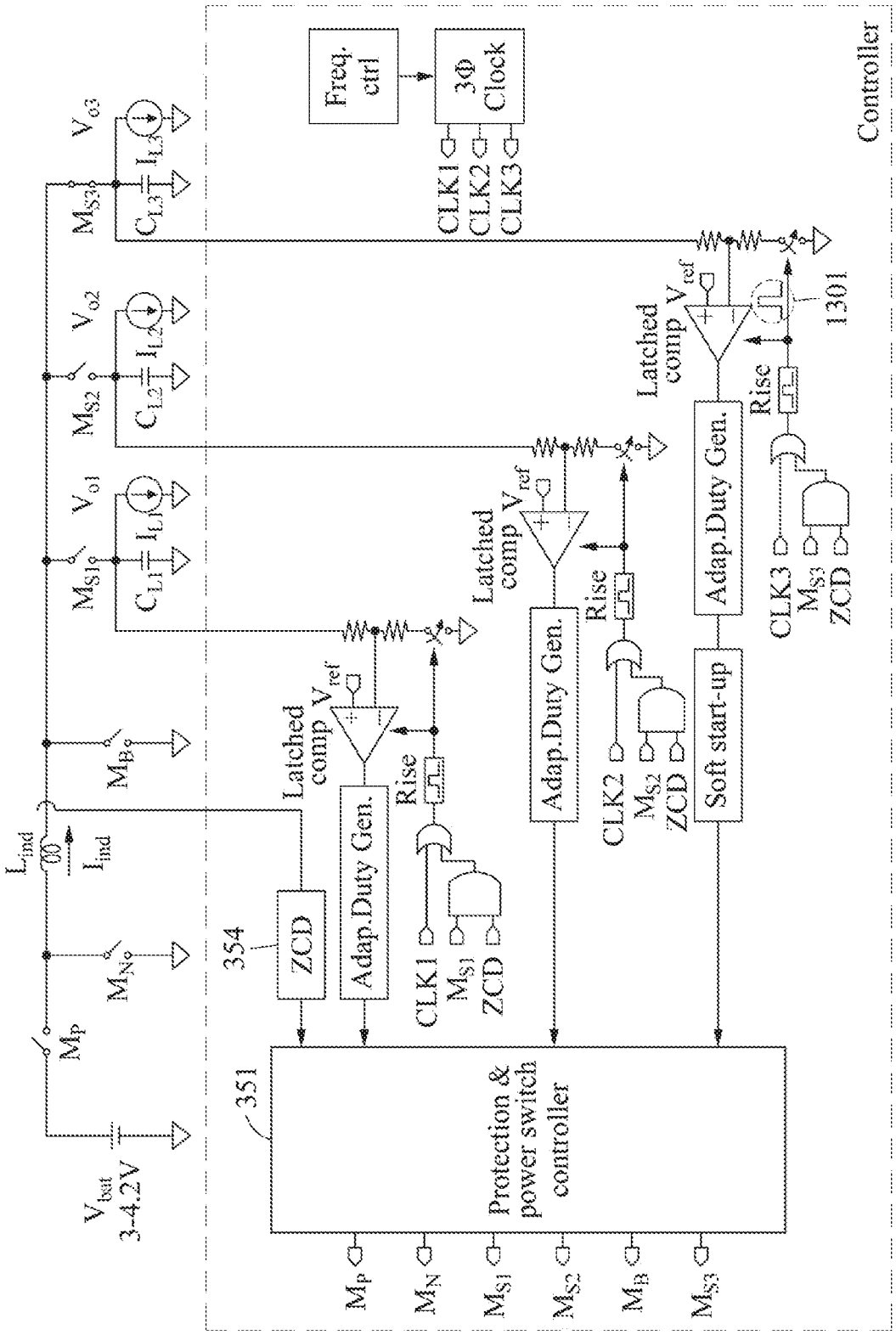

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
M_{S3}
C_{L3} I_{L3}
V_{o2}
M_{S2}
C_{L2} I_{L2}
V_{o1}
M_{S1}
C_{L1} I_{L1}
M_B
L_{ind}
I_{ind}
M_P
M_N
V_{batt} 3-4.2V
351
Protection & power switch controller
354
ZCD
Adap.Duty Gen.
Latched comp
V_{ref}
Rise
Soft start-up
1301
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}

FIG. 13B

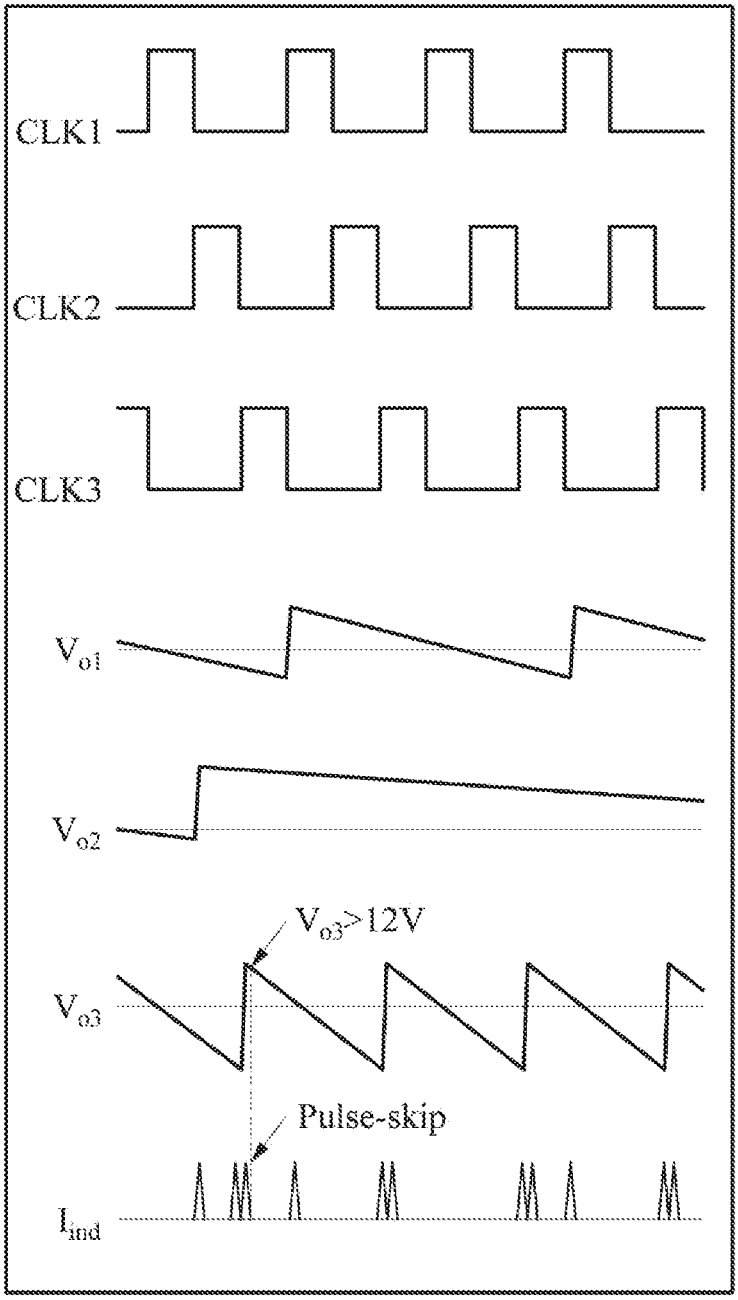


FIG. 14

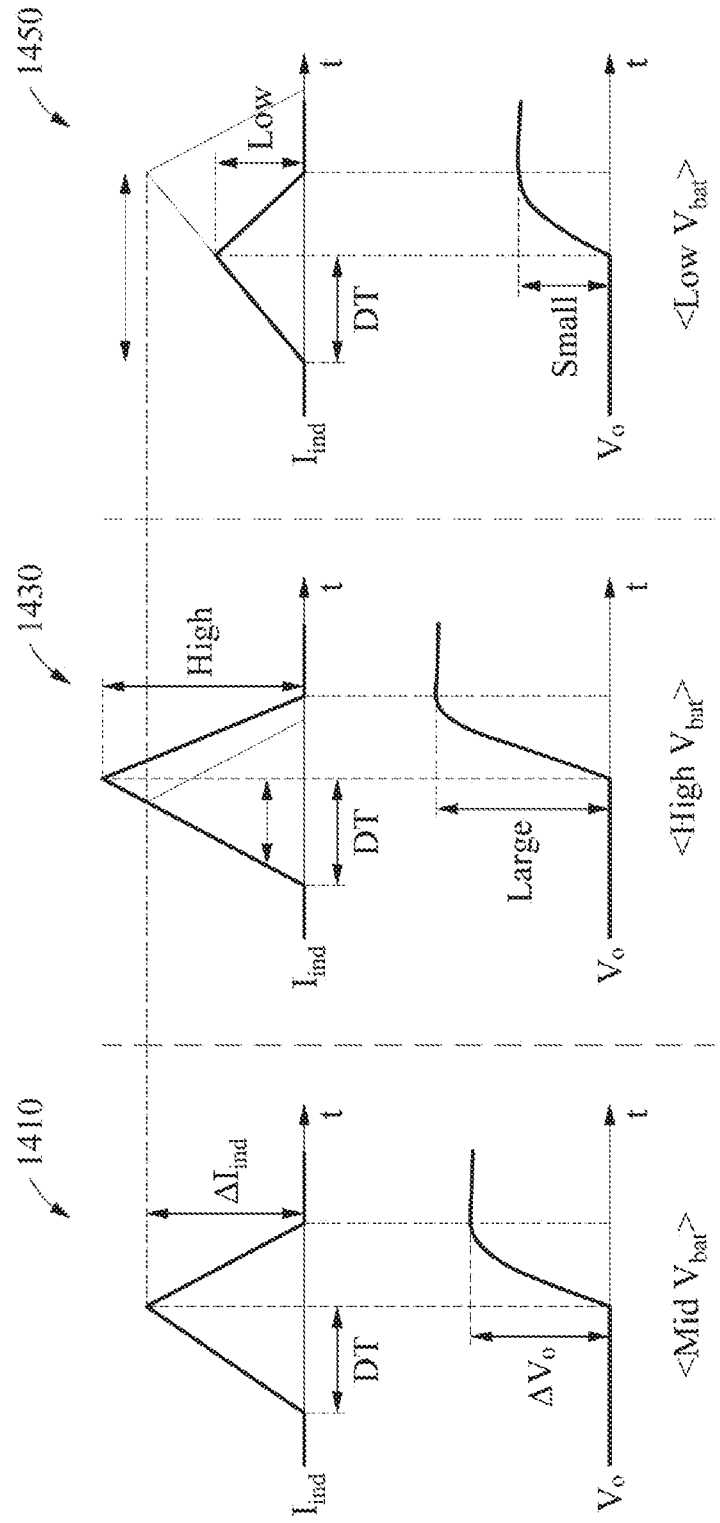

1450
1430
1410
Low
High
ΔI_{ind}
DT
I_{ind}
t
Small
Large
ΔV_o
V_o
<Low V_{bat}>
<High V_{bat}>
<Mid V_{bat}>

FIG. 15A

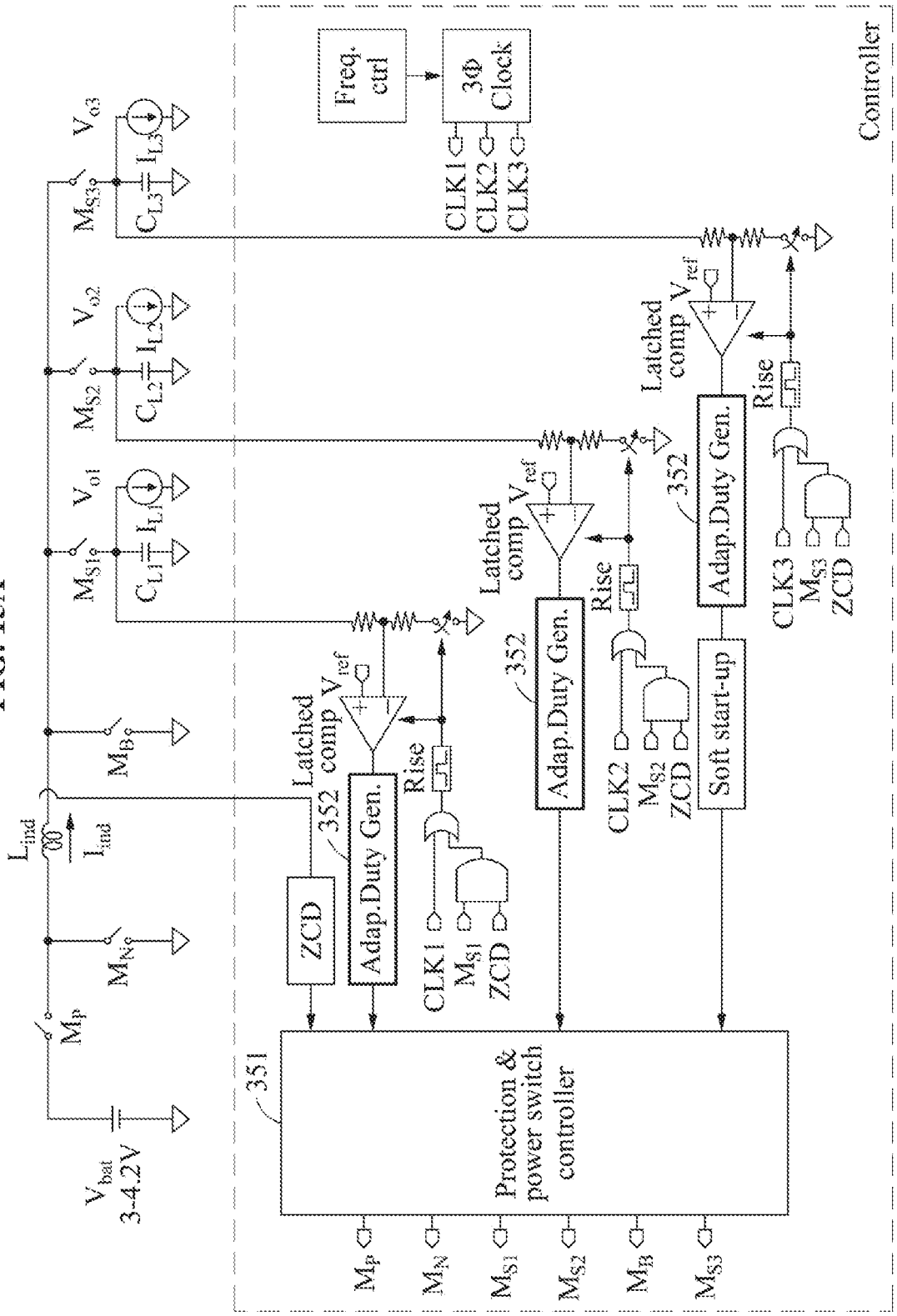

Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
I_{L3}
C_{L3}
M_{S3}
V_{o2}
I_{L2}
C_{L2}
M_{S2}
V_{o1}
I_{L1}
C_{L1}
M_{S1}
M_B
L_{ind}
I_{ind}
M_P
M_N
V_{bat}
3-4.2V
ZCD
Adap.Duty Gen.
352
Latched comp V_{ref}
Rise
CLK1
M_{S1}
ZCD
Adap.Duty Gen.
352
Latched comp V_{ref}
Rise
CLK2
M_{S2}
ZCD
Adap.Duty Gen.
352
Soft start-up
Latched comp V_{ref}
Rise
CLK3
M_{S3}
ZCD
351
Protection & power switch controller
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}

FIG. 15B

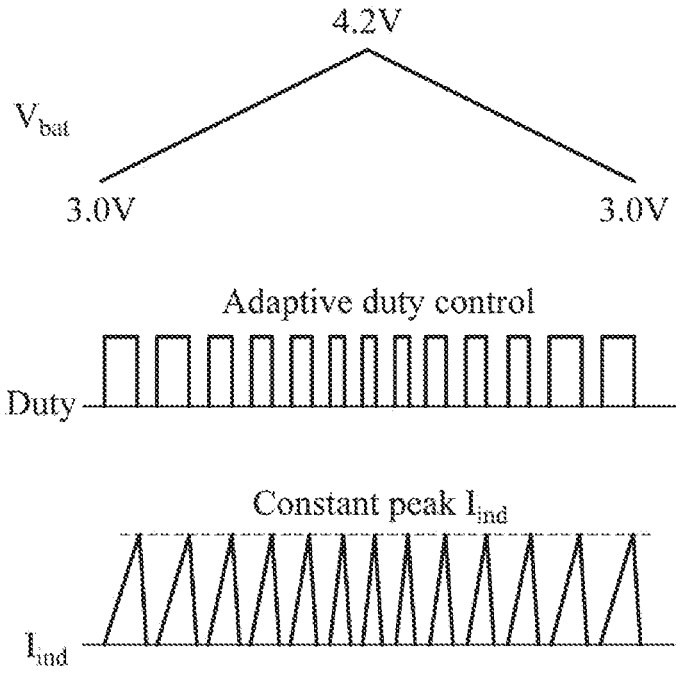

4.2V
V_{bat}
3.0V
3.0V
Adaptive duty control
Duty
Constant peak I_{ind}
I_{ind}

FIG. 16

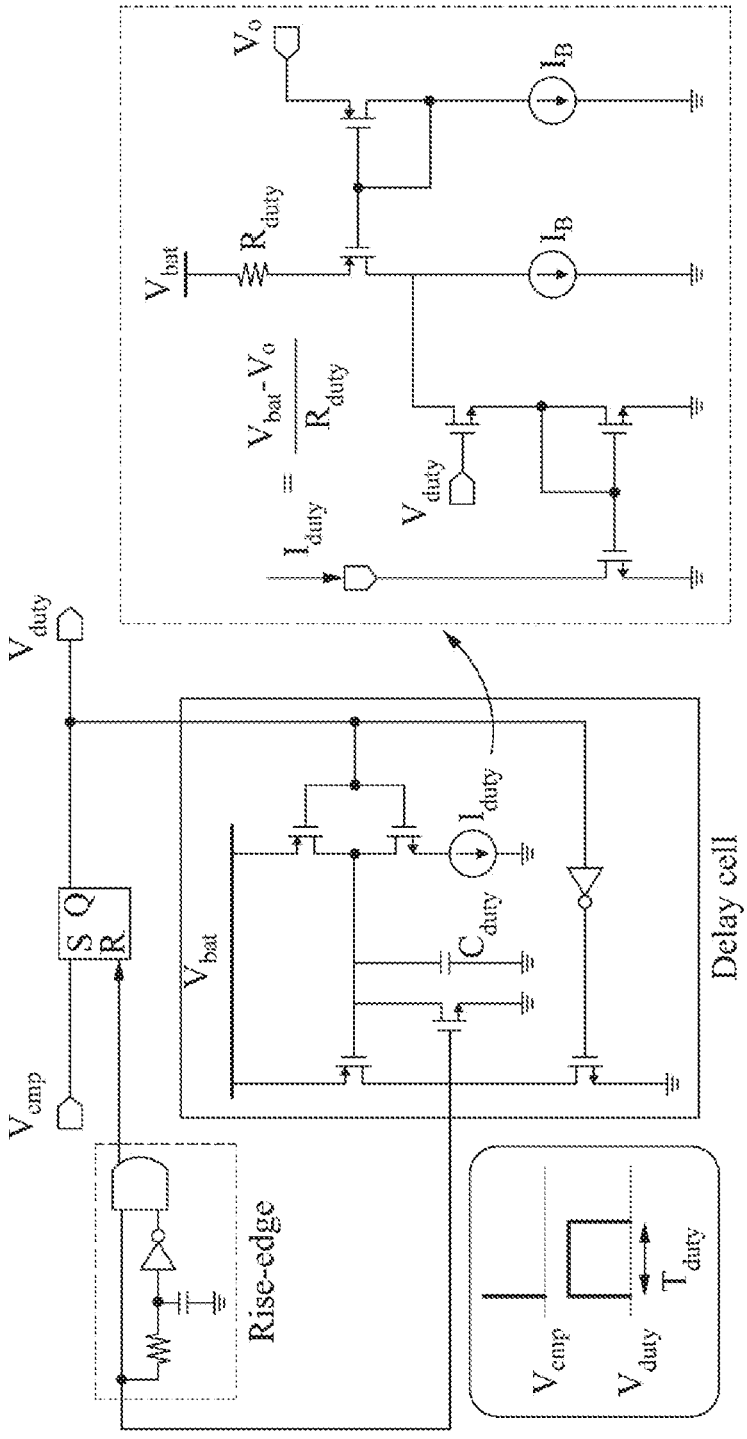

V_o
I_B
I_B
R_{duty}
V_{bat}
$\frac{V_{bat}-V_o}{R_{duty}} = I_{duty}$
V_{duty}
V_{duty}
S
Q
R
V_{bat}
I_{duty}
C_{duty}
Delay cell
V_{cmp}
Rise-edge
V_{cmp}
V_{duty}
T_{duty}

FIG. 17

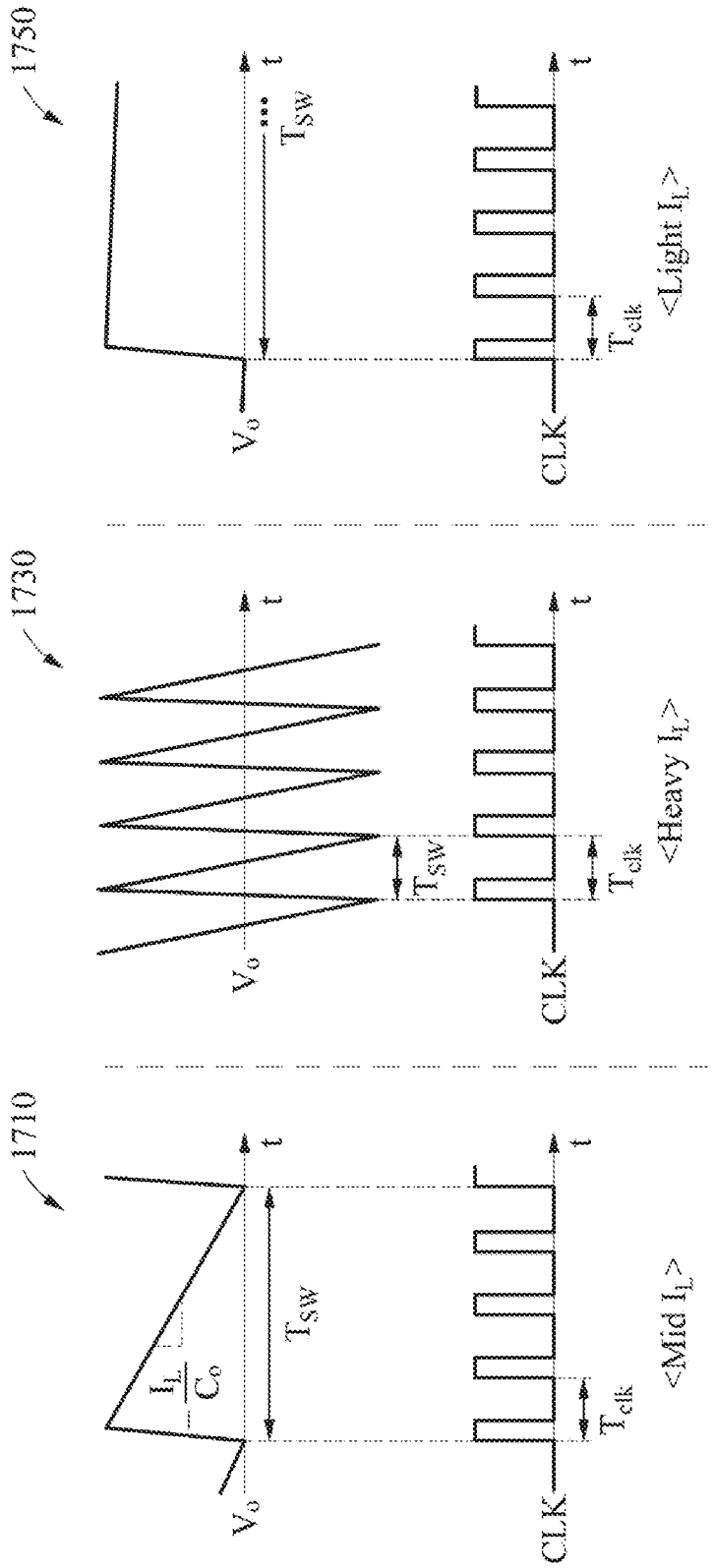

1750
t
T_{SW}
V_o
t
T_{clk}
CLK
<Light I_L>
1730
t
T_{SW}
V_o
t
T_{clk}
CLK
<Heavy I_L>
1710
t
$\frac{I_L}{C_o}$
T_{SW}
V_o
t
T_{clk}
CLK
<Mid I_L>

FIG. 18A

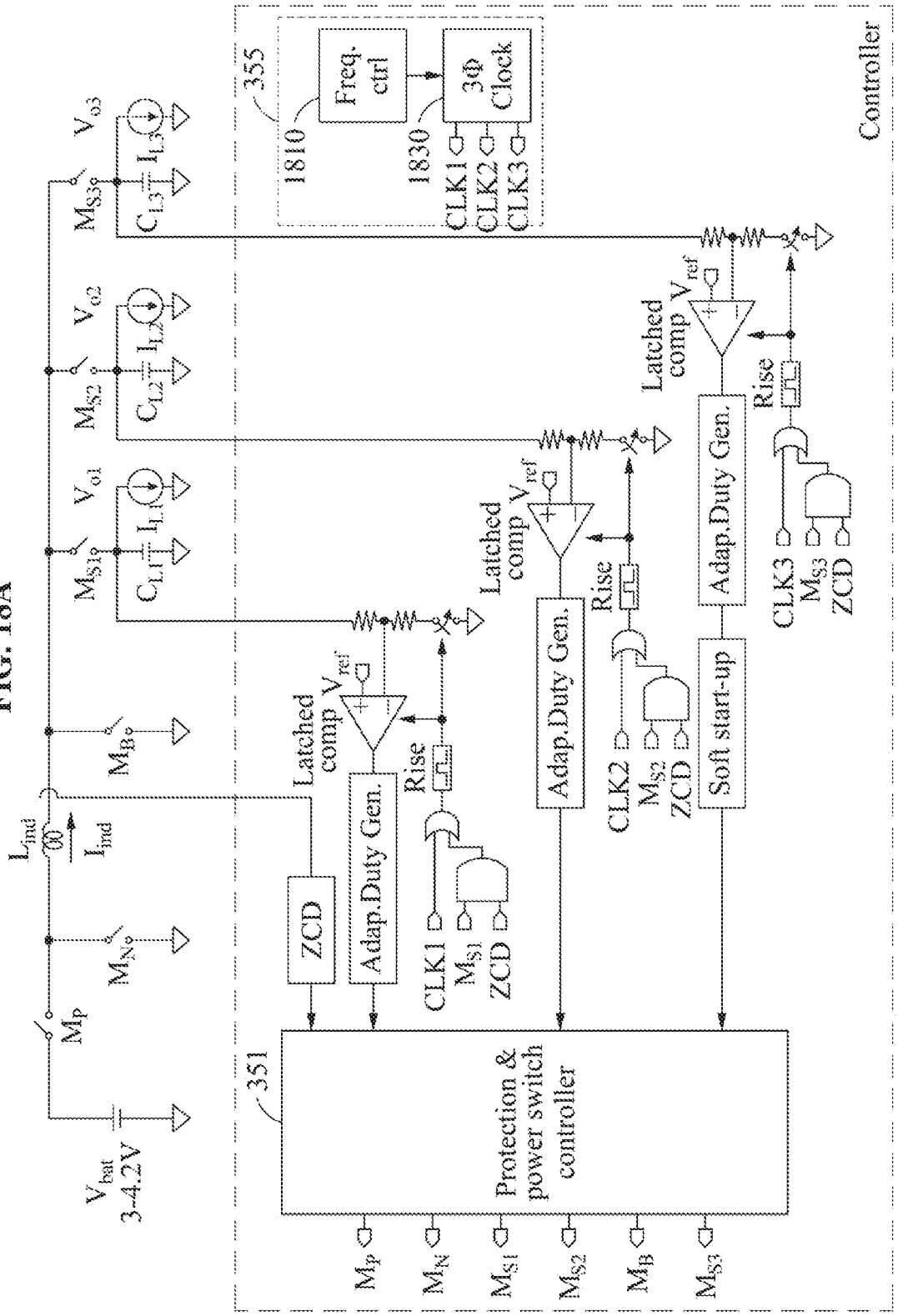

Controller
355
1810
Freq. ctrl
1830
3Φ Clock
CLK1
CLK2
CLK3
V_{o3}
I_{L3}
C_{L3}
M_{S3}
V_{o2}
I_{L2}
C_{L2}
M_{S2}
V_{o1}
I_{L1}
C_{L1}
M_{S1}
M_B
L_{ind}
I_{ind}
M_N
M_P
V_{bat}
3-4.2V
351
Protection & power switch controller
ZCD
Adap.Duty Gen.
Latched comp V_{ref}
Rise
CLK1
M_{S1}
ZCD
Adap.Duty Gen.
Latched comp V_{ref}
Rise
CLK2
M_{S2}
ZCD
Soft start-up
Adap.Duty Gen.
Latched comp V_{ref}
Rise
CLK3
M_{S3}
ZCD
M_P
M_N
M_{S1}
M_{S2}
M_B
M_{S3}

FIG. 18B

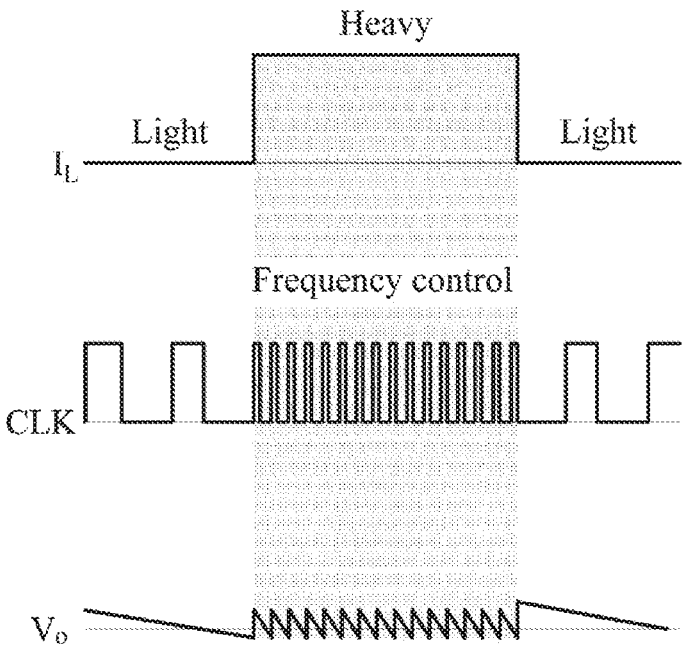


FIG. 19

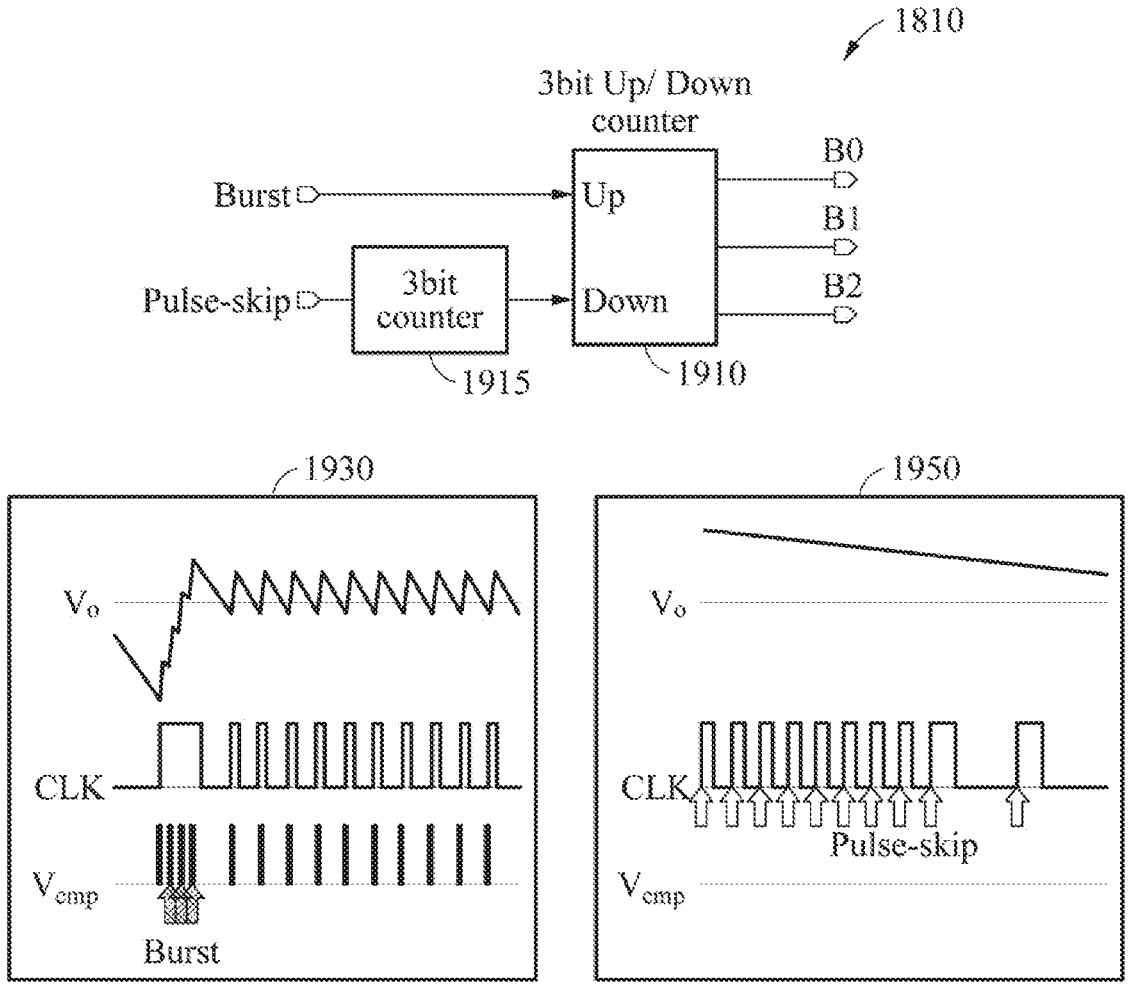

1810
3bit Up/ Down counter
Burst
Pulse-skip
3bit counter
Up
Down
B0
B1
B2
1915
1910
1930
V_o
CLK
V_{cmp}
Burst
1950
V_o
CLK
Pulse-skip
V_{cmp}

FIG. 20

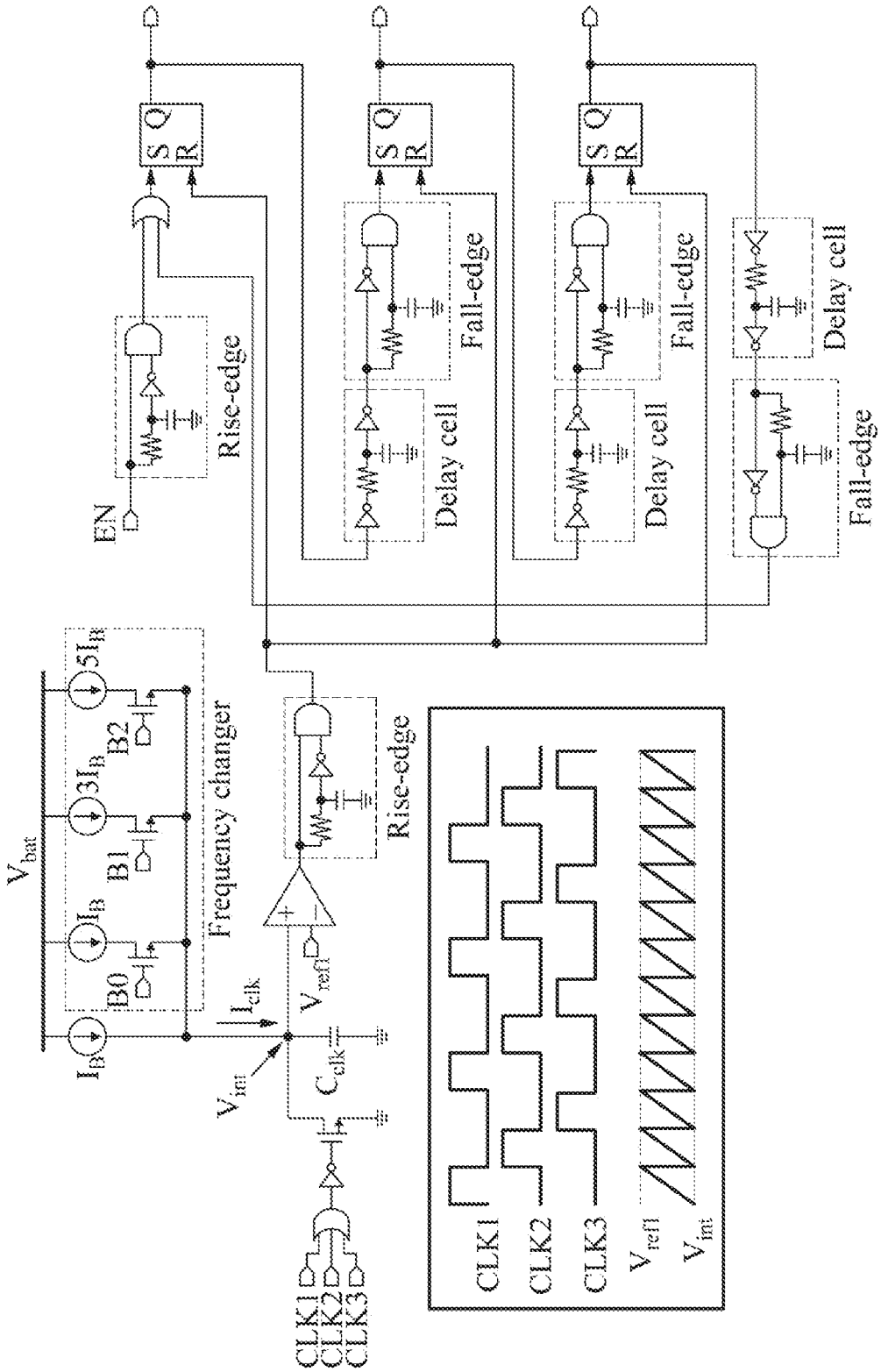

1830
EN
Rise-edge
Delay cell
Fall-edge
Delay cell
Fall-edge
Delay cell
Fall-edge
S
Q
R
V_{bat}
I_B
$3I_B$
$5I_B$
B0
B1
B2
Frequency changer
I_{clk}
V_{ref1}
V_{ini}
C_{clk}
Rise-edge
CLK1
CLK2
CLK3
V_{ref1}
V_{ini}

FIG. 21A

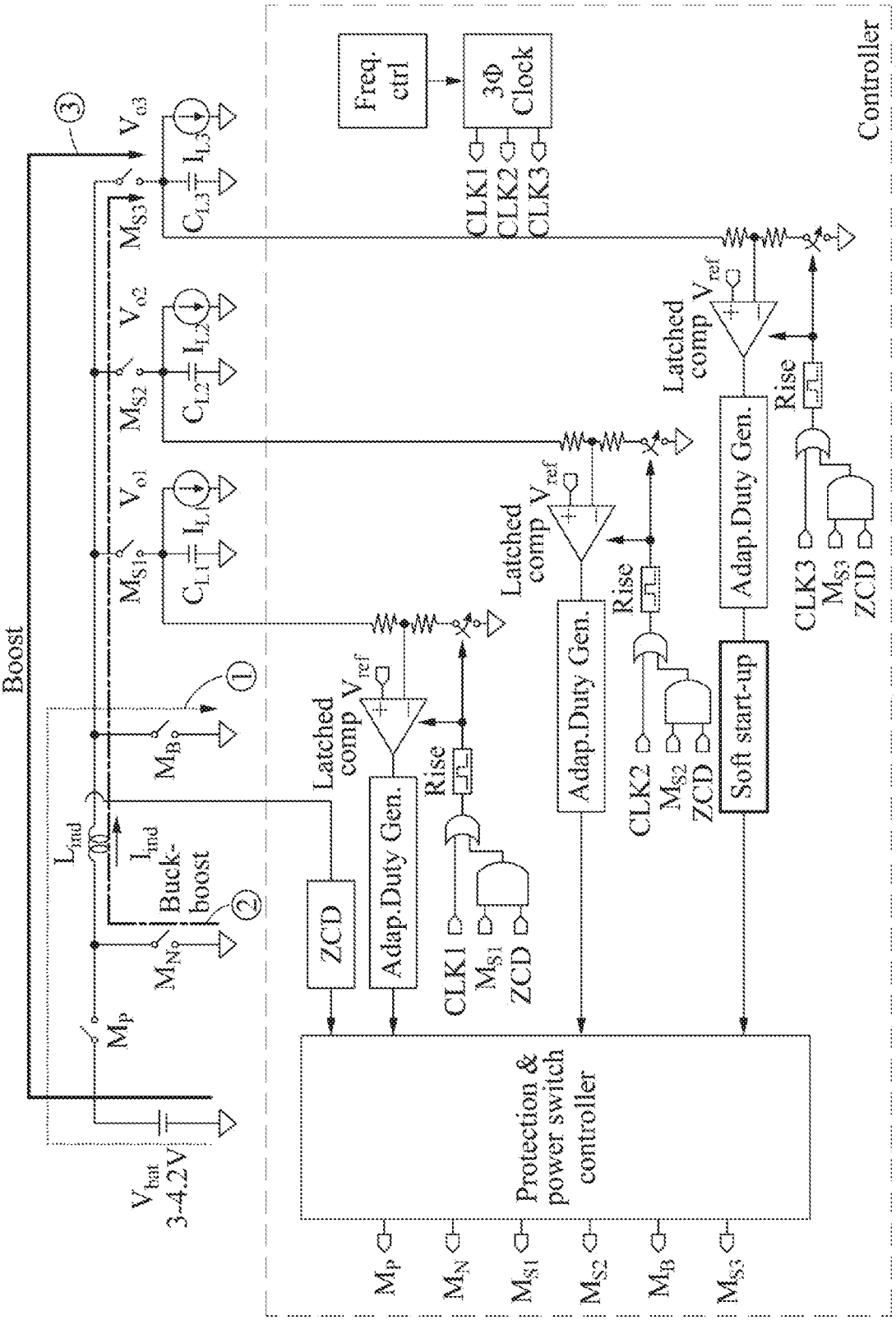

Boost
Buck-boost
Controller
Freq. ctrl
3Φ Clock
CLK1
CLK2
CLK3
Latched comp
Adap.Duty Gen.
Rise
ZCD
Soft start-up
Protection & power switch controller
V_{bat} 3-4.2V
L_{ind}
I_{ind}
M_P
M_N
M_B
M_{S1}
M_{S2}
M_{S3}
V_{o1}
V_{o2}
V_{o3}
V_{ref}
C_{L1} I_{L1}
C_{L2} I_{L2}
C_{L3} I_{L3}

FIG. 21B

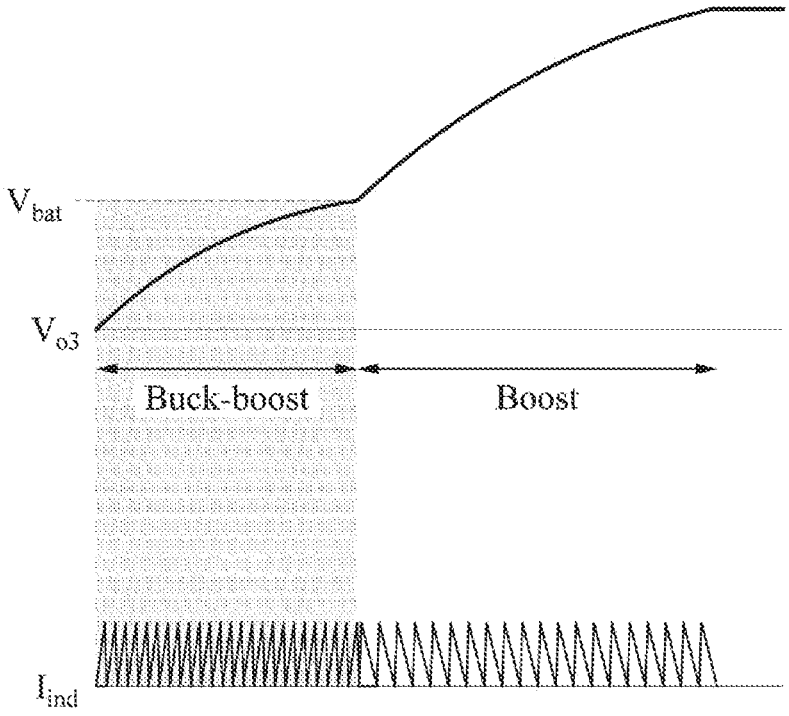
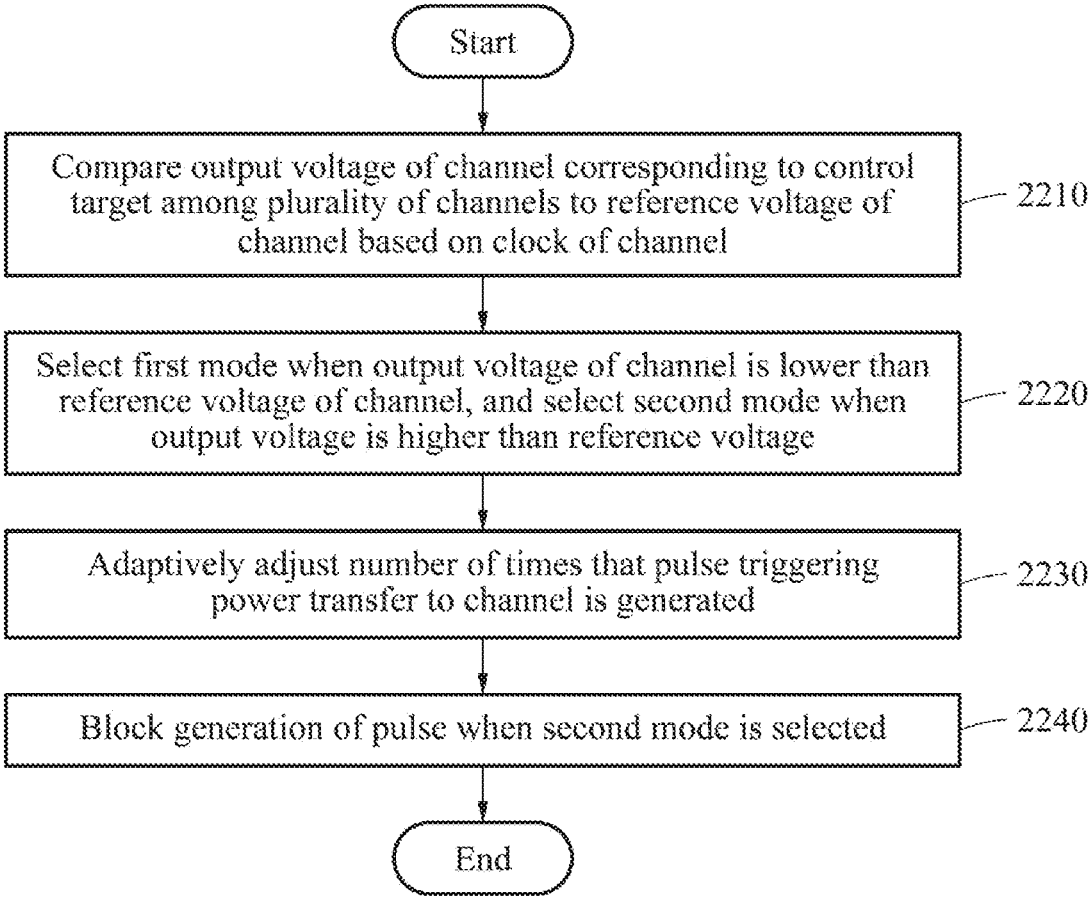


FIG. 22


Start
Compare output voltage of channel corresponding to control target among plurality of channels to reference voltage of channel based on clock of channel
2210
Select first mode when output voltage of channel is lower than reference voltage of channel, and select second mode when output voltage is higher than reference voltage
2220
Adaptively adjust number of times that pulse triggering power transfer to channel is generated
2230
Block generation of pulse when second mode is selected
2240
End

SINGLE-INDUCTOR MULTIPLE-OUTPUT (SIMO) CONVERTER AND CONTROL METHOD OF SIMO CONVERTER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application No. 62/724,196 filed on Aug. 29, 2018 in the U.S. Patent and Trademark Office and claims the benefit under 35 U.S.C. § 119(a) of Korean Patent Application No. 10-2019-0000545 filed on Jan. 3, 2019 in the Korean Intellectual Property Office, the entire disclosures of which are incorporated herein by reference for all purposes.

BACKGROUND

1. Field

[0002] This application relates to a single-inductor multiple-output (SIMO) converter and a control method of the SIMO converter.

2. Description of Related Art

[0003] A single-inductor multiple-output (SIMO) converter supplies energy needed by a plurality of output voltages using a single inductor. The SIMO converter recurrently selects the output voltages to supply the energy. In this instance, a method of controlling the SIMO converter such as a scheme for selecting the output voltages, an amount of energy to be supplied to correspond to the selected output voltage, and the like may be needed.

SUMMARY

[0004] This Summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

[0005] In a general aspect, a single-inductor multiple-output (SIMO) converter includes a converter configured to provide respective voltages of a plurality of channels with a single inductor, and a control logic configured to control switches of the converter based on clocks corresponding to the plurality of channels, wherein the control logic is configured to compare an output voltage of a selected channel of the plurality of channels that corresponds to a control target to a reference voltage of the selected channel based on a clock of the selected channel and operate in one of a first mode that adaptively adjusts a number of times that a pulse triggering a power transfer to the channel is generated, and a second mode that blocks a generation of the pulse.

[0006] The control logic may be further configured to repetitively generate the pulse in the first mode until the output voltage of the selected channel is higher than the reference voltage of the selected channel based on a determination that the output voltage of the channel is lower than the reference voltage of the channel.

[0007] The control logic may be further configured to block the generation of the pulse in the second mode based on a determination that the output voltage of the selected channel is higher than the reference voltage of the selected channel.

[0008] The control logic may be further configured to dynamically control a frequency of the clock corresponding to the selected channel based on a number of times that an operation is performed in the first mode and a number of times that an operation is performed in the second mode.

[0009] The converter may be further configured to provide the respective voltages of the plurality of channels based on the clocks having different phases based on a time multiplexing scheme.

[0010] In the first mode, the control logic may be further configured to adaptively adjust the number of times that the pulse is generated in a time interval initiated in response to an edge of the clock corresponding to the selected channel.

[0011] The converter may include the single inductor, and a switching unit comprising first switches configured to select the plurality of channels and second switches configured to control a flow of a current flowing in the single inductor.

[0012] The first switches may be configured to connect output ports of the plurality of channels and the single inductor in series.

[0013] The second switches may include a 2-1st switch, a 2-2nd switch, and a 2-3rd switch, the 2-1st switch may be configured to have a first end connected to an input port of the converter and a second end connected to a first end of the single inductor, the 2-2nd switch may be configured to have a first end connected to the first end of the single inductor, and a second end of the 2-2nd switch is grounded, and the 2-3rd switch may be configured to have a first end connected to a second end of the single inductor, and a second end of the 2-3rd switch is grounded.

[0014] The control logic may include a switch controller configured to select a first switch for the selected channel from among the first switches in response to the pulse being generated, and control the second switches based on a sequence for generating a desired voltage of the channel.

[0015] The control logic may be configured to dynamically control a duty-ratio of the second switches based on an input voltage of the converter.

[0016] The control logic may be further configured to reset a current of the single inductor after the power transfer is triggered due to the generation of the pulse.

[0017] The control logic may be further configured to dynamically control a frequency of the clock corresponding to the channel based on a load in the channel.

[0018] The control logic may include a comparator configured to latch the output voltage of the channel at an edge of the clock corresponding to the channel, and compare the latched output voltage to the reference voltage of the channel.

[0019] The control logic may be further configured to generate the clocks corresponding to the plurality of channels based on an importance level of the plurality of channels and control lengths of time intervals corresponding to phases of the clocks.

[0020] In a general aspect, a control method includes comparing, based on a clock of a selected channel corresponding to a control target among a plurality of channels, an output voltage of the selected channel to a reference voltage of the selected channel, selecting a first mode when the output voltage is lower than the reference voltage, and selecting a second mode when the output voltage is higher than the reference voltage, adaptively adjusting, when the first mode is selected, a number of times that a pulse

triggering a power transfer to the selected channel is generated, and blocking a generation of the pulse when the second mode is selected.

[0021] The adaptively adjusting the number of times that the pulse is generated may include repetitively generating the pulse until the output voltage of the selected channel is higher than the reference voltage of the selected channel based on the first mode.

[0022] The adaptively adjusting the number of times that the pulse is generated may include adaptively adjusting the number of times that the pulse is generated in a time interval initiated in response to an edge of the clock corresponding to the selected channel.

[0023] The method may further include counting a number of times that an operation is performed in the first mode and a number of times that an operation is performed in the second mode, and dynamically controlling a frequency of the clock corresponding to the selected channel based on a determination that the counted number of times corresponds to a preset number of times.

[0024] The dynamically controlling the frequency of the clock may include increasing the frequency of the clock corresponding to the selected channel when the number of times that an operation is performed in the first mode corresponds to the preset number of times.

[0025] The dynamically controlling the frequency of the clock may include reducing the frequency of the clock corresponding to the selected channel when the number of times that an operation is performed in the second mode corresponds to the preset number of times.

[0026] In a general aspect, a method includes comparing, in a single inductor multiple output (SIMO) converter, an output voltage of a selected channel among a plurality of channels to a reference voltage of the selected channel based on a clock of the selected channel, selecting a burst mode when the output voltage of the selected channel is less than or equal to the reference voltage, and selecting a pulse skip mode when the output voltage of the selected channel is greater than the reference voltage.

[0027] The method may further include adjusting a number of times a pulse triggering a power transfer to the selected channel is generated when the burst mode is selected, and blocking a generation of the pulse when the pulse skip mode is selected.

[0028] The SIMO converter may dynamically control a frequency of the clock corresponding to the selected channel by comparing a number of times that an operation is performed in the burst mode to a preset number of times, and comparing a number of times that an operation is performed in the pulse skip mode to the preset number of times.

[0029] Other features and aspects will be apparent from the following detailed description, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. **1** illustrates an example of an operation of a single-inductor multiple output (SIMO) converter, in accordance with one or more embodiments.

[0031] FIG. **2** illustrates an example of a control order of a SIMO converter, in accordance with one or more embodiments.

[0032] FIG. **3** is a circuit diagram illustrating an example of a SIMO converter, in accordance with one or more embodiments.

[0033] FIG. **4** illustrates an example of a method of operating a SIMO converter in a first mode or a second mode based on a clock, in accordance with one or more embodiments.

[0034] FIGS. **5**A and **5**B illustrate examples of an operation in an example in which a first clock CLK**1** corresponding to a first channel is applied in a SIMO converter, in accordance with one or more embodiments.

[0035] FIGS. **6**A through **8**B illustrate examples of an operation in an example in which a second clock CLK**2** corresponding to a second channel is applied in a SIMO converter, in accordance with one or more embodiments.

[0036] FIGS. **9**A through **13**B illustrate examples of an operation in an example in which a third clock CLK**3** corresponding to a third channel is applied in a SIMO converter, in accordance with one or more embodiments.

[0037] FIGS. **14** through **16** illustrate examples of a method of adaptively controlling a duty-ratio in an adaptive duty generator of a SIMO converter, in accordance with one or more embodiments.

[0038] FIGS. **17** through **19** illustrate examples of a method of dynamically controlling a frequency of a clock corresponding to each channel in a SIMO converter, in accordance with one or more embodiments.

[0039] FIG. **20** illustrate an example of a clock generator that generates clocks having different phases in a SIMO converter, in accordance with one or more embodiments.

[0040] FIGS. **21**A and **21**B illustrate examples of an operation of a soft start-up circuit of a SIMO converter.

[0041] FIG. **22** is flowchart illustrating an example of a control method of a SIMO converter.

[0042] Throughout the drawings and the detailed description, unless otherwise described or provided, the same drawing reference numerals will be understood to refer to the same elements, features, and structures. The drawings may not be to scale, and the relative size, proportions, and depiction of elements in the drawings may be exaggerated for clarity, illustration, and convenience.

DETAILED DESCRIPTION

[0043] The following detailed description is provided to assist the reader in gaining a comprehensive understanding of the methods, apparatuses, and/or systems described herein. However, various changes, modifications, and equivalents of the methods, apparatuses, and/or systems described herein will be apparent after an understanding of the disclosure of this application. For example, the sequences of operations described herein are merely examples, and are not limited to those set forth herein, but may be changed as will be apparent after an understanding of the disclosure of this application, with the exception of operations necessarily occurring in a certain order. Also, descriptions of features that are known in the art may be omitted for increased clarity and conciseness.

[0044] The features described herein may be embodied in different forms, and are not to be construed as being limited to the examples described herein. Rather, the examples described herein have been provided merely to illustrate some of the many possible ways of implementing the methods, apparatuses, and/or systems described herein that will be apparent after an understanding of the disclosure of this application.

[0045] The terminology used herein is for describing various examples only, and is not to be used to limit the

disclosure. The articles "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises," "includes," and "has" specify the presence of stated features, numbers, operations, members, elements, and/or combinations thereof, but do not preclude the presence or addition of one or more other features, numbers, operations, members, elements, and/or combinations thereof.

[0046] Unless otherwise defined, all terms, including technical and scientific terms, used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure pertains after an understanding of the present disclosure. Terms, such as those defined in commonly used dictionaries, are to be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and are not to be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0047] Additionally, in the description of examples, like reference numerals refer to like elements throughout the disclosure of this application, and repeated description related thereto is omitted. Further, detailed description of well-known related structures or functions will be omitted when it is deemed that such description will cause ambiguous interpretation of the present disclosure.

[0048] FIG. **1** illustrates an example of an operation of a single-inductor multiple output (SIMO) converter. Referring to FIG. **1**, a SIMO converter **110** provides desired voltages of a plurality of channels. The plurality of channels includes, for example, a first channel, a second channel, and a third channel. In an example, voltages of the first channel, the second channel, and the third channel are 0.8 volts (V), 1.8 V, and 12.0 V, respectively. In an example, the input voltage of the SIMO converter **110** is, for example, 3.7 V.

[0049] The SIMO converter **110** may operate based on a slow clock to reduce a standby power. Each of the channels of the SIMO converter **110** may operate based on a clock. An inductor current may operate in a discontinuous conduction mode (DCM) based on a clock such that the inductor current is reset for each clock. Herein, it is noted that use of the term 'may' with respect to an example or embodiment, e.g., as to what an example or embodiment may include or implement, means that at least one example or embodiment exists where such a feature is included or implemented while all examples and embodiments are not limited thereto.

[0050] The SIMO converter **110** may operate in a burst mode when an energy transfer to a channel is needed, and may operate in a pulse skip mode when an energy is sufficient. The SIMO converter **110** may compare an output voltage of a channel corresponding to a control target to a reference voltage, for example, a desired voltage of the channel based on a clock of the channel. The SIMO converter **110** operates in one of the burst mode and the pulse skip mode based on a voltage comparison result.

[0051] In this disclosure, the burst mode may be understood to be a mode in which a power is repetitively transferred through the inductor until the output voltage of the channel is higher than the reference voltage of the channel. The burst mode may also be referred to as a first mode. The pulse skip mode may be understood as a mode for blocking a generation of a pulse to the channel. The pulse skip mode may also be referred to as a second mode.

[0052] Hereinafter, the burst mode and the first mode are understood to have the same meaning and the pulse skip mode and the second mode are understood to have the same meaning.

[0053] When the energy is required in the channel, the SIMO converter **110** supplies the energy to the plurality of channels by adaptively adjusting a number of pulse generations per clock, for example, a number of pulse shots per clock. The SIMO converter **110** adaptively adjusts the number of pulse generations in a time interval initiated in response to an edge, for example, a rising edge corresponding to the channel. For example, when the energy is still inefficient after one shot of pulse is transferred in a time interval corresponding to one clock, the SIMO converter **110** may supply n shots of pulses until sufficient energy is supplied.

[0054] The SIMO converter **110** adaptively adjusts a number of times that a pulse triggering a power transfer to the channel is generated. For example, as shown in a table **150**, a light-load voltage may be desired in the first channel. In this example, as shown in a graph **130**, the SIMO converter **110** may generate a pulse once per clock such that the light-load voltage desired in the first channel is satisfied. Also, as shown in the table **150**, a high load of voltage may be desired in the third channel. In this example, as shown in the graph **130**, the SIMO converter **110** may generate a pulse N times per clock such that the high load of voltage desired in the third channel is satisfied.

[0055] When each of the channels has sufficient energy, the SIMO converter **110** operates in the second mode to block or skip a generation of a pulse.

[0056] The SIMO converter **110** operates based on a slow clock to reduce the standby power and rectify multiple output voltages constantly even when a load current changes.

[0057] For example, when the SIMO converter **110** operates in the first mode and the second mode based on the slow clock under a condition requiring a high-load voltage or a high-load current, a ripple may occur in the output voltage. In this example, a frequency of a clock may be adaptively varied to prevent an occurrence of a ripple voltage. The SIMO converter **110** may adjust the frequency of the clock to be decreased under a light-load condition requiring a light-load current and adjust the frequency of the clock to be increased under a high-load condition requiring a high-load current. The SIMO converter **110** may improve voltage regulation characteristics by adjusting the frequency of the clock to be increased in order to reduce an output ripple under the high-load condition.

[0058] The following description will be made based on an example in which a SIMO converter provides desired voltages of three channels as an example. However, a number of channels is not limited to the example. The number of channels may vary depending on an example.

[0059] FIG. **2** illustrates an example of a control order of a SIMO converter. As described above, a plurality of channels of a SIMO converter is sequentially controlled based on a first clock CLK **1**, a second clock CLK **2**, and a third clock CLK **3**. The SIMO converter operates in response to rising edges of the first clock CLK **1**, the second clock CLK **2**, and the third clock CLK **3**.

[0060] Referring to FIG. **2**, a clock frequency controller **201**, for example, a CLK frequency controller of a SIMO converter, supplies a clock corresponding to each channel.

When the first clock CLK **1** corresponding to a first channel is supplied from the clock frequency controller **201** in operation **205**, the SIMO converter compares a first output voltage V_{out1} corresponding to the first channel to a reference voltage V_{ref1} of the first channel, and determines if the first output voltage V_{out1} is higher than the reference voltage V_{ref1} of the first channel at the rising edge of the first clock in operation **210**.

[0061] When it is determined that the first output voltage V_{out1} is higher than the reference voltage V_{ref1} of the first channel in operation **210**, the SIMO converter blocks a pulse generation according to a pulse skip mode, thereby blocking an additional energy supply to the first output voltage V_{out1}. The SIMO converter transfers a pulse skip signal generated by the pulse skip mode to the second clock. Depending on an example, the pulse skip signal may be transferred to the clock frequency controller **201**.

[0062] When it is determined that the first output voltage V_{out1} is lower than or equal to the reference voltage V_{ref1} of the first channel, the SIMO converter transfers power through an inductor according to a burst mode in operation **220**. After transferring the power in operation **220**, the SIMO converter compares the first output voltage V_{out1} to the reference voltage V_{ref1} again in operation **210** and repeats a power transfer in operation **220** until the first output voltage V_{out1} is equal to the reference voltage V_{ref1}.

[0063] The SIMO converter dynamically controls a frequency of the first clock corresponding to the first channel by counting a number of times that an operation is performed in the burst mode and/or a number of times that an operation is performed in the pulse skip mode. When the burst mode occurs at least a preset number of times, the SIMO converter increases a speed (a frequency) of the first clock. When the pulse skip mode occurs at least a preset number of times, the SIMO converter reduces the speed (the frequency) of the first clock. The aforementioned operations may also be performed in the same manner in the second clock and/or the third clock in addition to the first clock depending on an example.

[0064] After the first clock is supplied, the second clock CLK **2** is supplied from the clock frequency controller **201** based on a time multiplexing scheme in operation **225**. In response to the second clock CLK **2** being supplied, the SIMO converter compares a second output voltage V_{out2} corresponding to the second channel to a reference voltage V_{ref2} of the second channel at the rising edge of the second clock in operation **230**.

[0065] When it is determined that the second output voltage V_{out2} is higher than the reference voltage V_{ref2} of the second channel in operation **230**, the SIMO converter blocks a pulse generation according to a pulse skip mode, thereby blocking an additional energy supply to the second output voltage V_{out2}.

[0066] When it is determined that the second output voltage V_{out2} is lower than or equal to the reference voltage V_{ref2} of the second channel in operation **230**, the SIMO converter transfers power through the inductor in operation **235**. After transferring the power, the SIMO converter compares the second output voltage V_{out2} to the reference voltage V_{ref2} again in operation **230** and repeats a power transfer in operation **235** until the second output voltage V_{out2} is equal to the reference voltage V_{ref2}.

[0067] After the second clock CLK **2** is supplied, the third clock CLK **3** is supplied from the clock frequency controller **201** based on a time multiplexing scheme in operation **240**. In response to the third clock CLK **3** being supplied, the SIMO converter compares a third output voltage V_{out3} corresponding to the third channel to a reference voltage V_{ref3} of the third channel at the rising edge of the third clock in operation **245**.

[0068] When it is determined that the third output voltage V_{out3} is higher than the reference voltage V_{ref3} of the third channel in operation **245**, the SIMO converter skips a pulse generation to block an additional energy supply. When it is determined that the third output voltage V_{out3} is lower than or equal to the reference voltage V_{ref3} of the third channel in operation **245**, the SIMO converter transfers power through the inductor in operation **250**. After transferring the power, the SIMO converter compares the third output voltage V_{out3} to the reference voltage V_{ref3} again in operation **245** and repeats a power transfer in operation **250** until the third output voltage V_{out3} is equal to the reference voltage V_{ref3}.

[0069] FIG. **3** is a circuit diagram illustrating an example of a SIMO converter in accordance with one or more embodiments. Referring to FIG. **3**, a SIMO converter **300** includes a single inductor **310**, for example, L_{ind}, a switching unit **330**, and a control logic **350**.

[0070] The single inductor **310** supplies voltages desired by a plurality of channels of a converter.

[0071] The switching unit **330** includes first switches M_{S1}, M_{S2}, and M_{S3} for selecting the plurality of channels, and second switches M_P, M_N, and M_B for controlling a flow of an inductor current I_{ind} flowing in the single inductor **310**, that is, an inductor current generated due to a power transfer through the single inductor. The first switches M_{S1}, M_{S2}, and M_{S3} connect output ports (for example, ports outputting output voltages V_{O1}, V_{O2}, and V_{O3}) of the plurality of channels and the single inductor **310** in series. Among the first switches M_{S1}, M_{S2}, and M_{S3}, a 1-1^{st} switch, for example, the first switch M_{S1} is a switch for selecting a first channel, a 1-2^{nd} switch, for example, the first switch M_{S2} is a switch for selecting a second channel, and a 1-3^{rd} switch, for example, the first switch M_{S3} is a switch for selecting a third channel.

[0072] The second switches M_P, M_N, M_B include a 2-1^{st} switch M_P, a 2-2^{nd} switch M_N, and a 2-3^{rd} switch M_B. One end of the 2-1^{st} switch M_P is connected to an input port (V_{bat}-side) of the SIMO converter **300** and the other end of the 2-1^{st} switch M_P is connected to one end of the single inductor **310**. One end of the 2-2^{nd} switch M_N is connected to the one end of the single inductor **310** and the other end of the 2-2^{nd} switch M_N is grounded, for example, connected to a ground GND. One end of the 2-3^{rd} switch M_B is connected to the other end of the single inductor **310** and the other end of the 2-3^{rd} switch M_B is grounded.

[0073] The SIMO converter **300** uses the single inductor **310**, for example, the inductor current I_{ind} of the single inductor **310** to provide the required voltages of the plurality of channels. The SIMO converter **300** provides the required voltages of the plurality of channels based on clocks having different phases using a time multiplexing scheme.

[0074] The control logic **350** compares an output voltage of a channel corresponding to a control target to a reference voltage of the channel based on a clock of the channel such that the SIMO converter **300** operates in one of the first mode and the second mode described above.

[0075] The control logic **350** controls switches, for example, the first switches M_P, M_N, and M_B and the second

switches M_{S1}, M_{S2}, M_{S3} of the switching unit **330** based on clocks, for example, CLK**1**, CLK**2**, and CLK**3** corresponding to the plurality of channels.

[0076] The control logic **350** includes a switch controller **351**, for example, a protection & power switch controller, adaptive duty generators **352**, comparators **353**, for example, latched comparators, a zero crossing detector (ZCD) **354**, a clock controller **355**, and a soft start-up circuit **356**.

[0077] The switch controller **351** selects a first switch for a corresponding channel from the first switches M_{S1}, M_{S2}, and M_{S3} in response to a pulse being generated and controls the second switches M_P, M_N, and M_B based on a sequence for generating a desired voltage of the channel. A method in which the switch controller **351** controls the switches M_P, M_N, M_B, M_{S1}, M_{S2}, and M_{S3} in response to a pulse being generated will be described in detail with reference to FIGS. **5**A through **13**B.

[0078] The adaptive duty generator **352** dynamically controls a duty-ratio of the second switches M_P, M_N, and M_B based on an input voltage of the SIMO converter **300**. An operation of the adaptive duty generator will be described in detail with reference to FIGS. **14** through **16**.

[0079] The comparator **353** latches the output voltage of the channel at an edge, for example, a rising edge of the clock corresponding to the channel. The comparator **353** compares the latched output voltage to the reference voltage of the channel.

[0080] The ZCD **354** resets the current I_{ind} of the single inductor **310** after the power transfer that is triggered due to the generation of the pulse.

[0081] The clock controller **355** supplies clocks having different phases to correspond to the plurality of channels based on a time multiplexing scheme. An operation of the clock controller **355** will be described in detail with reference to FIGS. **17** through **20**.

[0082] The soft start-up circuit **356** dynamically controls a frequency of the clock corresponding to the channel based on a load in the channel. An operation of the soft start-up circuit will be described in detail with reference to FIGS. **21**A and **21**B.

[0083] FIG. **4** illustrates an example of a method of operating a SIMO converter in a first mode or a second mode based on a clock. FIG. **4** illustrates a first clock CLK **1** of a first channel, a second clock CLK **2** of a second channel, and a third clock CLK **3** of a third channel. The first clock CLK **1**, the second clock CLK **2**, and the third clock CLK **3** are generated based on a common clock or a global clock. For example, a rising edge of the first clock CLK **1** is generated at a first rising edge of the common clock, a rising edge of the second clock CLK **2** is generated at a second rising edge of the common clock, and a rising edge of the third clock CLK **3** is generated at a third rising edge of the common clock. The common clock is divided in the aforementioned manner to generate the first clock CLK **1** though the third clock CLK **3**.

[0084] FIG. **4** illustrates an example in which an output voltage V_{O1} of the first channel is lower than a reference voltage, for example, 1.8 V of the first channel at the rising edge of the first clock CLK **1**, an example in which an output voltage V_{O2} of the second channel is lower than a reference voltage, for example, 0.8 V of the second channel at the rising edge of the second clock CLK **2**, and an example in which an output voltage V_{O3} of the third channel is lower than a reference voltage, for example, 12.0 V of the third channel at the rising edge of the third clock CLK **3**.

[0085] A SIMO converter compares the output voltage V_{O1} of the first channel to the reference voltage (for example, 1.8 V) of the first channel in response to the first clock CLK **1** of the first channel being supplied. For example, when the output voltage V_{O1} of the first channel is 1.9 V, the output voltage V_{O1} of the first channel is higher than the reference voltage (for example, 1.8 V). In this example, the SIMO converter blocks a generation of a pulse according to the second mode.

[0086] After the first clock CLK **1** is supplied, the second clock CLK is supplied based on a time multiplexing scheme. The SIMO converter compares the output voltage V_{O2} of the second channel to the reference voltage (for example, 0.8 V) of the channel. When the output voltage V_{O2} of the second channel is 0.7 V, the output voltage V_{O2} is lower than the reference voltage (for example, 0.8 V) of the second channel. In this example, the SIMO converter repetitively generates the pulse until the output voltage V_{O2} (0.7 V) of the second channel is higher than the reference voltage (for example, 0.8 V) of the second channel according to the first mode. For example, the output voltage V_{O2} (0.7 V) of the second channel may be increased to be higher than the reference voltage (for example, 0.8 V) through a pulse generation performed once. Thereafter, the SIMO converter blocks the pulse generation according to the second mode.

[0087] After the second clock CLK **2** is supplied, the third clock CLK **3** is supplied based on the time multiplexing scheme. The SIMO converter compares the output voltage V_{O3} of the third channel to the reference voltage (for example, 12.0 V) of the third channel at the rising edge of the third clock CLK **3**. When the output voltage V_{O3} of the third channel is 8.0 V, the output voltage V_{O3} of the third channel is lower than the reference voltage (for example, 12.0 V) of the third channel. In this example, the SIMO converter repetitively generates the pulse until the output voltage V_{O3} (8.0 V) of the third channel is higher than the reference voltage (for example, 12.0 V) according to the first mode. For example, the output voltage V_{O3} (8.0 V) of the third channel is increased to be higher than the reference voltage (for example, 12.0 V) through the pulse generation performed twice. Thereafter, the SIMO converter blocks the pulse generation according to the second mode.

[0088] An operation of a switching unit corresponding to each channel in an example in which sequential clocks are supplied to the channel based on the time multiplexing scheme will be described in detail with reference to FIGS. **5**A through **13**B.

[0089] FIGS. **5**A and **5**B illustrate examples of an operation in an example in which a first clock CLK**1** corresponding to a first channel is applied in a SIMO converter. Referring to FIG. **5**A, a signal **501** is generated in response to a rising edge of a first clock CLK **1** being detected. Referring to FIG. **5**B, an output voltage V_{O1} of the first channel is detected at a point in time in which the rising edge of the first clock CLK **1** corresponding to the first channel occurs.

[0090] When the signal **501** is generated in response to the rising edge of the first clock CLK **1** being detected, a switch **502** is turned on by the signal **501** such that the output voltage V_{O1} of the first channel is transferred to a first comparator **503**.

[0091] The first comparator **503** compares the output voltage V_{O1} of the first channel to a reference voltage (for example, 1.8 V) of the first channel. A circuit for comparing the output voltage V_{O1} of the first channel to the reference voltage of the first channel may be designed in various ways. A common reference voltage V_{ref} and a voltage divider may be used. For example, the output voltage V_{O1} of the first channel may be divided using a voltage divider of a ratio corresponding to the reference voltage (for example, 1.8 V) of the first channel. The voltage divider includes a plurality of sensing resistors. The first comparator **503** compares the common reference voltage V_{ref} and a voltage-divided output voltage, thereby comparing the output voltage V_{O1} of the first channel and the reference voltage (for example, 1.8 V) of the first channel.

[0092] The output voltage V_{O1} of the first channel is, for example, 1.9 V as illustrated in FIG. **5**B. In this example, since the output voltage V_{O1} (1.9 V) is higher than the reference voltage (1.8 V) of the first channel, the SIMO converter generates a pulse skip signal to block the pulse generation according to the second mode. In response to the pulse skip signal, the switch controller **351** does not generate a control signal for controlling a switching unit. In this example, a power transfer to a single inductor L_{ind} is blocked, so that an inductor current I_{ind} is not generated.

[0093] FIGS. **6**A through **8**B illustrate examples of an operation in an example in which a second clock CLK**2** corresponding to a second channel is applied in a SIMO converter. FIGS. **6**A through **8**B illustrate an operation performed in an example in which a second clock CLK **2** is supplied to a SIMO converter based on a time multiplexing scheme after a first clock CLK **1** is supplied similar to the example of FIGS. **5**A and **5**B.

[0094] Referring to FIG. **6**A, a signal **601** is generated in response to a rising edge of the second clock CLK **2** being detected. Referring to FIG. **6**B, an output voltage V_{O1} of the second channel is detected at a point in time in which the rising edge of the second clock CLK **2** corresponding to the second channel occurs.

[0095] When the signal **601** is generated in response to the rising edge of the second clock CLK **2** being detected, a switch **602** is turned on by the signal **601** such that the output voltage V_{O2} of the second channel is transferred to a second comparator **603**.

[0096] The second comparator **603** compares the output voltage V_{O2} of the second channel to a reference voltage (for example, 0.8 V) of the second channel. As an example, the output voltage V_{O2} of the second channel may be divided using a voltage divider of a ratio corresponding to the reference voltage (for example, 0.8 V) of the second channel. The second comparator **603** compares a common reference voltage V_{ref} and a voltage-divided output voltage, thereby comparing the output voltage V_{O2} of the second channel and the reference voltage (for example, 0.8 V) of the second channel.

[0097] The output voltage V_{O2} of the second channel is, for example, 0.7 V as illustrated in FIG. **6**B. In this example, since the output voltage V_{O2} (0.7 V) of the second channel is lower than the reference voltage (0.8 V), the SIMO converter generates a pulse according to a first mode to increase the output voltage V_{O2} of the second channel as illustrated in FIG. **6**B. The SIMO converter repetitively generates the pulse until the output voltage V_{O2} (0.7 V) of the second channel is higher than the reference voltage (for example, 0.8 V) according to the first mode.

[0098] When the output voltage V_{O2} (0.7V) of the second channel is lower than the reference voltage (for example, 0.8V) as illustrated in FIG. **6**B, the second comparator **603** transmits a signal to a second adaptive duty generator **604**.

[0099] The second adaptive duty generator **604** having received the signal transmitted from the second comparator **603** generates a signal **701** as illustrated in FIG. **7**A. The switch controller **351** dynamically controls a duty-ratio of second switches M_P, M_N, and M_B based on the signal **701** received from the second adaptive duty generator **604**. The signal **701** generated by the second adaptive duty generator **604** is used to dynamically control the duty-ratio of the second switches M_P, M_N, and M_B based on, for example, an input voltage V_{bat} of the SIMO converter such that the inductor current I_{ind} is built-up and freewheeled.

[0100] The switch controller **351** controls the switching unit **330** using the signal **701** as illustrated in FIG. **7**A. The switch controller **351** having received the signal **701** transmits a signal **711** for the second switch M_P and a signal **713** for a 1-2^{nd} switch M_{S2} corresponding to the second channel such that the second switch M_P and the 1-2^{nd} switch M_{S2} are turned on as indicated by an arrow ①. In this example remaining switches are off. Through this, the input voltage V_{bat} of the SIMO converter is supplied to the output voltage V_{O2} of the second channel through the 1-2^{nd} switch M_{S2}. Thereafter, the switch controller **351** transmits a signal **712** for a 2-2^{nd} switch, for example, the second switch M_N and a signal **713** for the 1-2^{nd} switch M_{S2} such that the 2-2^{nd} switch M_N and the 1-2^{nd} switch M_{S2} are turned on as indicated by an arrow ②. In this example remaining switches are off. Through this, a voltage obtained due to the inductor current I_{ind} may also be supplied to the output voltage V_{O2} of the second channel.

[0101] In response to the voltage being supplied to the output voltage V_{O2} of the second channel, the output voltage V_{O2} of the second channel is increased to be higher than or equal to the reference voltage (for example, 0.8 V) as illustrated in FIG. **7**B.

[0102] After power is transferred to the output voltage V_{O1} of the second channel based on the signal **701**, the SIMO converter resets a current L_{ind} of a single inductor using the ZCD **354** as illustrated in FIG. **8**A. The ZCD **354** allows the inductor current L_{ind} to be 0 and prevents a counter electromotive force being applied to a battery. The inductor current L_{ind} becomes zero by the ZCD **354** in the second mode as illustrated in FIG. **8**B.

[0103] Thereafter, as illustrated in FIG. **8**A, a signal **801** is generated by the output voltage V_{O2} of the second channel and the ZCD **354**. The switch controller **351** transmits a signal **811** for the 1-2^{nd} switch M_{S2} in response to the signal **801**. The 1-2^{nd} switch M_{S2} is turned on in response to the signal **811** such that the output voltage V_{O2} of the second channel is transferred to a second comparator **803**. As a comparison result of the second comparator **803**, the increased output voltage V_{O2} of the second channel is higher than the reference voltage (for example, 0.8 V) as illustrated in FIG. **8**B, the SIMO converter operates in the second mode.

[0104] FIGS. **9**A through **13**B illustrate examples of an operation in an example in which a third clock CLK**3** corresponding to a third channel is applied in a SIMO converter. FIGS. **9**A through **13**B illustrate an operation

performed in an example in which a third clock CLK **3** is supplied to a SIMO converter based on a time multiplexing scheme after a second clock CLK **2** is supplied.

[0105] Referring to FIG. **9**A, a signal **901** is generated in response to a rising edge of the third clock CLK **3** being detected. Referring to FIG. **9**B, an output voltage V_{O3} of the third channel is detected at a point in time in which the rising edge of the third clock CLK **3** corresponding to the third channel occurs.

[0106] When the signal **901** is generated in response to the rising edge of the third clock CLK **3** being detected, a switch **902** is turned on by the signal **901** such that the output voltage V_{O3} of the third channel is transferred to a third comparator **903**.

[0107] The third comparator **903** compares the output voltage V_{O3} of the third channel to a reference voltage (for example, 12 V) of the third channel. As an example, the output voltage V_{O3} of the third channel may be divided using a voltage divider of a ratio corresponding to the reference voltage (for example, 12 V) of the third channel. The third comparator **903** compares a common reference voltage V_{ref} and a voltage-divided output voltage, thereby comparing the output voltage V_{O3} of the third channel and the reference voltage (for example, 12 V) of the third channel.

[0108] For example, as illustrated in FIG. **9**B, the output voltage V_{O3} may be 8 V which is lower than the reference voltage of 12 V.

[0109] In this example, since the output voltage V_{O3} (8 V) of the third channel is lower than the reference voltage (for example, 12 V), the SIMO converter generates a signal **1001** according to a first mode to increase the output voltage V_{O3} of the third channel as illustrated in FIG. **10**A. The signal **1001** may be a signal generated through a third adaptive duty generator **1002** and the soft start-up circuit **356**.

[0110] A process of generating the signal **1001** is as follows, for example.

[0111] The SIMO converter repetitively generates a pulse to increase the output voltage V_{O3} (8 V) of the third channel until the output voltage V_{O3} is higher than the reference voltage (for example, 12 V) according to the first mode. When it is determined that the output voltage V_{O3} (8 V) of the third channel is lower than the reference voltage (for example, 12 V), a third comparator **1003** transfers a signal to the third adaptive duty generator **1002**. The signal may be generated as the signal **1001** via the third adaptive duty generator **1002** and the soft start-up circuit **356**. The soft start-up circuit **356** generates the signal **1001** and transfers the signal **1001** to the switch controller **351** to prevent an abrupt increase in current, for example, in rush current. The switch controller **351** having received the signal **1001** dynamically controls a duty-ratio of second switches, for example, a 2-1st switch M_P, a 2-2nd switch M_N, and a 2-3rd switch M_B.

[0112] The switch controller **351**, having received the signal **1001**, transmits a signal **1011** for the 2-1st switch M_P, a signal **1012** for the 2-3rd switch M_B, and a signal **1013** for a 1-3rd switch M_{S3}. The switches (the 2-1st switch M_P, the 2-3rd switch M_B, and the 1-3rd switch M_{S3}) having received the corresponding signals are turned on. An input voltage V_{bat} of the SIMO converter is grounded through the 2-3rd switch M_B, and only a voltage due to an inductor current I_{ind} is supplied to the output voltage V_{O3} of the third channel through the 1-3rd switch M_{S3}.

[0113] As such, the soft start-up circuit **356** increases the output voltage V_{O3} of the third channel to reach a level of the input voltage V_{bat} (for example, 3 V to 4.2 V) of the SIMO converter, and then increases the output voltage V_{O3} of the third channel to be equal to the reference voltage (for example, 12 V) through a boosting operation so as to prevent an occurrence of ripple current due to an abrupt increase in an amount of current. The soft start-up circuit **356** increases the output voltage V_{O3} of the third channel as illustrated in FIG. **10**B. An operation of the soft start-up circuit **356** will be further described with reference to FIGS. **21**A and **21**B.

[0114] After transferring a power to the output voltage V_{O3} of the third channel based on the signal **1001**, the SIMO converter transfers an inductor current of a single inductor to the ZCD **354**, thereby resetting the inductor current to be zero as illustrated in FIG. **11**A.

[0115] Thereafter, a signal **1101** is generated based on the ZCD **354** and the output voltage V_{O3} of the third channel. The switch controller **351**, having received the signal **1101**, transfers a signal **1111** for the 1-3rd switch M_{S3}. The 1-3rd switch M_{S3} is turned on in response to the signal **1111**. The output voltage V_{O3} of the third channel is transferred to the third comparator **1003**. As a comparison result of the third comparator **1003**, since the increased output voltage V_{O3} of the third channel is lower than the reference voltage (for example, 12 V) as illustrated in FIG. **11**B, the SIMO converter operates in the first mode.

[0116] As a comparison result of the third comparator **1003**, when it is determined that the output voltage V_{O3} (8 V) of the third channel is still lower than the reference voltage (for example, 12 V) as illustrated in FIG. **11**B, the SIMO converter generates a signal **1201** according to the first mode to increase the output voltage V_{O3} of the third channel as illustrated in FIG. **12**A. An inductor current generated in the first mode increases the output voltage V_{O3} of the third channel as illustrated in FIG. **12**B.

[0117] The switch controller **351** having received the signal **1201** transmits a signal **1211** for the 2-1st switch M_P, a signal **1212** for the 2-3rd switch M_B, and a signal **1213** for the 1-3rd switch M_{S3}. The switches (the 2-1st switch M_P, the 2-3rd switch M_B, and the 1-3rd switch M_{S3}) having received the corresponding signals are turned on and remaining switches are turned off. In this example, the input voltage V_{bat} of the SIMO converter is grounded through the 2-3rd switch M_B, and only a voltage due to the inductor current I_{ind} is supplied to the output voltage V_{O3} of the third channel through the 1-3rd switch M_{S3}.

[0118] After transferring a power to the output voltage V_{O3} of the third channel based on the signal **1201**, the SIMO converter transfers an inductor current of a single inductor to the ZCD **354**, thereby resetting the inductor current to be zero as illustrated in FIG. **13**A.

[0119] Thereafter, a signal **1301** is generated based on the ZCD **354** and the output voltage V_{O3} of the third channel. In this example, since the increased output voltage V_{O3} of the third channel is higher than the reference voltage (for example, 12 V) as illustrated in FIG. **13**B, the SIMO converter operates in the second mode.

[0120] FIGS. **14** through **16** illustrate examples of a method of adaptively controlling a duty-ratio in an adaptive duty generator of a SIMO converter. FIG. **14** illustrates situations in which a variation of an output voltage changes in response to a change in an input voltage V_{bat} of the SIMO converter when a duty-ratio of switches is fixed.

[0121] A variation ΔI_{ind} of an inductor current L_{ind} based on the input voltage V_{bat} of the SIMO converter is obtained using Equation 1 as shown below.

$$\Delta I_{ind} = \frac{V_{bat} - V_o}{L_{ind}} DT \quad \text{Equation 1}$$

[0122] In Equation 1, L_{ind} denotes an inductor current of the SIMO converter.

[0123] Also, a variation ΔV_o of the output voltage V_o of the SIMO converter corresponding to a variation of the inductor current is obtained using Equation 2 as shown below.

$$\Delta V_o = \sqrt{\frac{L_{ind}}{C_o}}\,\Delta I_{ind} = \frac{1}{\sqrt{C_o L_{ind}}}(V_{bat} - V_o)DT \quad \text{Equartion 2}$$

[0124] In Equation 2, C_o represents a capacitance value of a capacitor connected to an output port of the SIMO converter. Also, DT denotes a duty-ratio of switches of the SIMO converter. DT may have a fixed value.

[0125] For example, when the input voltage V_{bat} of the SIMO converter has an intermediate voltage Mid V_{bat}, the variation ΔI_{ind} of the inductor current and the variation ΔV_o of the output voltage may be as shown in section **1410** of FIG. **14**.

[0126] When the input voltage V_{bat} of the SIMO converter has a higher voltage High V_{bat} than the intermediate voltage Mid V_{bat}, and when DT has a fixed duty-ratio, a peak of the inductor current L_{ind} is increased to be higher than the intermediate voltage according to Equation 1 as shown in section **1430** of FIG. **14**. Accordingly, the output voltage V_o of the SIMO converter may also be increased to be higher than the intermediate voltage according to Equation 2.

[0127] When the input voltage V_{bat} of the SIMO converter has a lower voltage Low V_{bat} than the intermediate voltage Mid V_{bat}, and when DT has a fixed duty-ratio, a peak of the inductor current L_{ind} is reduced to be lower than the intermediate voltage according to Equation 1 as shown in section **1450** of FIG. **14**. Accordingly, the output voltage V_o of the SIMO converter may also be reduced to be lower than the intermediate voltage according to Equation 2.

[0128] As such, when the duty-ratio is fixed, a peak of the inductor current L_{ind} is changed in response to a change in the input voltage V_{bat} of the SIMO converter, which may result in a ripple in the output voltage V_o of the SIMO converter.

[0129] FIG. **15**A illustrates adaptive duty generators **352**. FIG. **15**B illustrates a graph representing a peak of an inductor current L_{ind} is constantly maintained by dynamically controlling a duty-ratio of second switches when an input voltage V_{bat} of the SIMO converter changes in a range between 3 V and 4.2 V.

[0130] The adaptive duty generators **352** of FIG. **15**A may prevent an occurrence of a ripple in the output voltage V_o of the SIMO converter by dynamically controlling a duty-ratio of the second switches M_P, M_N, and M_B based on the input voltage of the SIMO converter.

[0131] For example, as illustrated in FIG. **15**B, when the input voltage of the SIMO converter gradually increases from 3.0 V to 4.2 V, the adaptive duty generators **352** may gradually reduce the duty-ratio of the second switches M_P, M_N, and M_B. In response to the duty-ratio of the second switches M_P, M_N, and M_B being reduced, a peak value of the inductor current I_{ind} is also maintained at a predetermined level. As such, when the peak value of the inductor current is constantly maintained, the output voltage V_o is also constantly maintained to prevent the occurrence of the ripple.

[0132] FIG. **16** illustrates a circuit diagram of the adaptive duty generators **352**.

[0133] In the circuit diagram of FIG. **16**, a length of duty interval T_{duty} corresponding to a duty-ratio is obtained using Equation 3 as shown below.

$$T_{duty} = \frac{C_{duty}}{I_{duty}} V_{th} = \frac{C_{duty} R_{duty}}{V_{bat} - V_o} V_{th} \quad \text{Equation 3}$$

[0134] In Equation 3, C_{duty} denotes a predetermined capacitor value, R_{duty} denotes a predetermined resistor value (a constant value), V_{th} denotes a threshold of a transistor (PMOS), and V_o is a constant value. I_{duty} denotes a current generated based on a battery voltage V_{bat}.

[0135] I_{duty} is determined as, for example,

$$I_{duty} = \frac{V_{bat} - V_o}{R_{duty}}$$

based on the determined resistor value R_{duty}, the battery voltage V_{bat}, and the constant value V_o. I_{duty} flows through the predetermined capacitor C_{duty} so as to change a voltage of an upper terminal of C_{duty}. When the voltage changes and the voltage exceeds a threshold V_{th} of a rear-end transistor (PMOS), a status is transited so that a duty interval T_{duty} is determined. For example, the duty interval T_{duty} may be

$$T_{duty} = \frac{C_{duty}}{I_{duty}} V_{th}.$$

[0136] Also, when the duty-ratio is adaptively changed as illustrated in the circuit diagram of FIG. **16**. a variation ΔV_o of the output voltage of the SIMO converter may be obtained using Equation 4 as shown below.

$$\Delta V_o = \frac{1}{\sqrt{L_{ind} C_o}}(V_{bat} - V_o)T_{duty} = \frac{1}{\sqrt{L_{ind} C_o}} C_{duty} R_{duty} V_{th} \quad \text{Equation 4}$$

[0137] C_o corresponds to a capacitance value of a capacitor connected to an output port of the SIMO converter.

[0138] FIGS. **17** through **19** illustrate examples of a method of dynamically controlling a frequency of a clock corresponding to each channel in a SIMO converter. FIG. **17** illustrates output voltages corresponding to load currents I_L under a light load condition, an intermediate load condition, and a heavy load condition.

[0139] A relationship between the load current I_L and a clock frequency is expressed by Equation 5 as shown below.

$$T_{sw} = N \cdot T_{clk} = \frac{C_o V_o}{I_L} (N \geq 1) \quad \text{Equation 5}$$

[0140] In Equation 5, N denotes a number of clock occurrences and T_{clk} denotes a clock frequency. T_{sw} denotes a period of time in which switching occurs for actual power transfer, for example, a switching period.

[0141] In Equation 5, when the clock frequency T_{clk} is fixed, the switching period T_{sw} changes in response to a change in load current as follows.

[0142] When the load current of the SIMO converter is an intermediate load current Mid I_L as shown in section **1710** of FIG. **17**, power may be transferred by performing the switching once per 4 clocks. In addition, when the load current of the SIMO is a heavy load current Heavy I_L as shown in section **1730** of FIG. **17**, the power may be transferred by performing the switching for each clock. Also, when the load current of the SIMO converter is a light load current Light I_L as shown in section **1750** of FIG. **17**, no or few switching may be performed.

[0143] FIG. **18**A illustrates a clock controller **355** and FIG. **18**B illustrates a method of controlling a clock with the clock controller **355** based on an inductor current. The clock controller **355** dynamically controls a frequency of a clock corresponding to a channel based on a load in the channel. The clock controller **355** controls clocks to supply clock pulses having different frequencies corresponding to a plurality of channels in response to a change in inductor current. In this example, the clock controller **355** controls clocks to sequentially supply clock pulses with different frequencies corresponding to the plurality of channels based on a time multiplexing scheme. The clock controller **355** includes a frequency controller **1810** and a 3-phase (ϕ) clock generator **1830**. An operation of the frequency controller **1810**, for example, a Freq controller will be described in detail with reference to FIG. **19**. An operation of the 3-phase clock generator **1830** will be described in detail with reference to FIG. **20**.

[0144] For example, as illustrated in FIG. **18**B, when a load of a load current of the SIMO converter is light in a corresponding channel, no or few switching may be performed. Also, when the load of the load current is heavy, the power may be transferred by performing switching for each clock.

[0145] FIG. **19** illustrates a configuration and an operation of the frequency controller **1810** in accordance with one or more embodiments.

[0146] The frequency controller **1810** counts a number of times that the SIMO converter operates in a first mode and a number of times that the SIMO converter operates in a second mode using a 3-bit up/down counter **1910**. The frequency controller **1810** dynamically controls a frequency of a clock corresponding to a corresponding channel based on the counted number of times. When the counted number of times corresponds to a preset number of times, the frequency controller **1810** dynamically controls a frequency of a clock corresponding to a corresponding channel. In this example, a preset number of times corresponding to the first mode may be the same as or different from a preset number of times corresponding to the second mode. In an example, unlike a number of first mode occurrences, a number of second mode occurrences may be input to the 3-bit up/down counter **1910** via another 3-bit counter **1910**. In this example, the number of second mode occurrences may be transferred to the 3-bit up/down counter **1910** three times slower than the number of first mode occurrences.

[0147] For example, to increase the output voltage V_O, the SIMO converter may operate four times in the first mode (burst mode) as shown in a box **1930**, and the preset number of times corresponding to the first mode may be 4. Since the number of times that the SIMO converter operates in the first mode, which is 4, corresponds to the preset number of times (4), the frequency controller **1810** may adjust a clock frequency to be increased.

[0148] Also, when the output voltage V_o does not need to be increased, the SIMO may operate nine times in the second mode (pulse skip mode) as shown in a box **1950**, and, in a non-limiting example, the preset number of times corresponding to the second mode may be 9. Since the number of times that the SIMO converter operates in the second mode, which is 9, corresponds to the preset number of times, that is, 9, the frequency controller **1810** may adjust a clock frequency to be decreased.

[0149] In an example, a frequency of a common clock is dynamically controlled by monitoring modes of a single channel (for example, 1.8 V). Since a plurality of channels uses the frequency of the common clock by dividing the frequency, clock frequencies of the plurality channels may be dynamically controlled in response to the frequency of the common clock being dynamically controlled. For example, an output voltage V_o of FIG. **19** is an output voltage of a predetermined channel (1.8 V) and a clock CLK of FIG. **19** is a common clock.

[0150] In an example, a frequency of a common clock is dynamically controlled by monitoring modes of a plurality of channels. For example, the frequency of the common clock may be reduced by operating at least a preset number of times in the second mode (pulse skip mode) in one channel. Also, the frequency of the common clock may be increased by operating at least a preset number of times in the first mode (burst mode) in another channel. In this example, an output voltage V_o of FIG. **19** is an output voltage of a channel among the plurality of channels and a clock CLK of FIG. **19** is a common clock.

[0151] FIG. **20** illustrates an example of a clock generator that generates clocks having different phases in a SIMO converter. FIG. **20** illustrates a configuration and an operation of a 3-phase (ϕ) clock generator **1830**. The 3-phase clock generator **1830** generates clocks having three different phases in the SIMO converter. The 3-phase clock generator **1830** generates clocks having a frequency f_{clk} using Equation 6 as shown below.

$$f_{clk} = \frac{I_{clk}}{3C_{clk} \cdot V_{ref1}} \quad \text{Equation 6}$$

[0152] In Equation 6, C_{clk} denotes a capacitance value of a clock capacitor of a capacitor connected to an output power of a clock in parallel. V_{ref1} denotes a reference voltage of a channel (for example, a first channel) applied to a comparator. I_{clk} denotes a clock current applied from the frequency controller **1810** to the 3-phase clock generator **1830**.

[0153] The SIMO converter provides desired voltages of a plurality of channels using a time multiplexing scheme

based on the clocks having different phases generated by the 3-phase clock generator **1830** of FIG. **20**.

[0154] FIGS. **21**A and **21**B illustrate examples of an operation of a soft start-up circuit of a SIMO converter. FIG. **21**A illustrates a buck-boost operation and a boost operation for preventing an abrupt flow of a current using a soft start-up circuit. FIG. **21**B illustrates a change in an output voltage V_{O3} of a third channel during the buck-boost operation and the boost operation.

[0155] As described with reference to FIG. **10**, the soft start-up circuit may prevent an abrupt increase in inductor current, for example, in rush current.

[0156] For example, when a signal is transferred in the soft start-up circuit, the signal is transferred through the switch controller **351** such that each switch performs the buck-boost operation. The buck-boost operation is performed in an order indicated by arrows ① and ② in FIG. **21**A.

[0157] In the buck-boost operation, the switch controller **351** turns on a 2-1st switch M_P and a 2-3rd switch M_B as indicated by the arrow ① and turns off remaining switches. In this process, an input voltage V_{bat} of the SIMO converter may be grounded via the 2-3rd switch M_B. Thereafter, the switch controller **351** turns on a 2-2nd switch M_N and a 1-3rd switch M_{S3} as indicated by the arrow ② and turns off remaining switches. In this process, only a voltage due to an inductor current I_{ind} may be supplied to the output voltage V_{O3} of the third channel via the 1-3rd switch M_{S3}. The switch controller **351** performs the buck-boost operation until the output voltage V_{O3} of the third channel is equal to the input voltage V_{bat} of the SIMO converter. Referring to FIG. **21**B, it is shown that the output voltage V_{O3} of the third channel is moderately increased while the buck-boost operation is performed.

[0158] When the output voltage V_{O3} of the third channel is equal to the input voltage V_{bat} of the SIMO converter, the switch controller **351** performs the boost operation.

[0159] In the boost operation, the switch controller **351** turns on the 2-1st switch M_P and 1-3rd switch M_{S3} as indicated by an arrow ③ and turns off remaining switches. In this process, in addition to the voltage due to the inductor current I_{ind} of the inductor, the input voltage V_{bat} of the SIMO converter may also be supplied. In this case, the output voltage V_{O3} of the SIMO converter rises sharply from the input voltage V_{bat} as illustrated in FIG. **21**B.

[0160] As such, a soft start-up circuit slowly increases the output voltage V_{O3} of the third channel to reach a level of the input voltage V_{bat} (3 V to 4.2 V) of the SIMO converter through the buck-boost operation. After that, the soft start-up circuit quickly increases the output voltage V_{O3} of the third channel to reach the reference voltage (for example, 12 V) through the boost operation. Through this, the soft start-up circuit prevents an occurrence of a ripple current due to the abrupt increase in the amount of current.

[0161] FIG. **22** is flowchart illustrating an example of a control method of a SIMO converter. The operations in FIG. **22** may be performed in the sequence and manner as shown, although the order of some operations may be changed or some of the operations omitted without departing from the spirit and scope of the illustrative examples described. Many of the operations shown in FIG. **22** may be performed in parallel or concurrently. One or more blocks of FIG. **22**, and combinations of the blocks, can be implemented by special purpose hardware-based computer that perform the specified functions, or combinations of special purpose hardware and computer instructions. In addition to the description of FIG. **22** below, the descriptions of FIGS. **1-21** are also applicable to FIG. **22**, and are incorporated herein by reference. Thus, the above description may not be repeated here.

[0162] Referring to FIG. **22**, in operation **2210**, a SIMO converter compares an output voltage of a channel corresponding to a control target among a plurality of channels to a reference voltage of the channel based on a clock of the channel. In this example, the SIMO converter uses a single inductor to provide desired voltages of the plurality of channels.

[0163] In operation **2220**, the SIMO converter selects a first mode when the output voltage of the channel is lower than the reference voltage of the channel, and selects a second mode when the output voltage is higher than the reference voltage.

[0164] When the first mode is selected, in operation **2230**, the SIMO converter adaptively adjusts a number of times that a pulse triggering a power transfer to the channel is generated. The SIMO converter adaptively adjusts the number of times that the pulse is generated in a time interval initiated in response to an edge of the clock corresponding to the channel. For example, the SIMO converter repetitively generates the pulse until the output voltage of the channel is higher than the reference voltage of the channel according to the first mode.

[0165] In operation **2240**, the SIMO converter blocks a generation of the pulse when the second mode is selected.

[0166] The SIMO converter counts a number of times that an operation is performed in the first mode and a number of times that an operation is performed in the second mode. The SIMO converter dynamically controls a frequency of the clock corresponding to the channel based on a result obtained by determining whether the counted number of times (for example, the number of times that an operation is performed in the first mode and the number of times that an operation is performed in the second mode) corresponds to a preset number of times. When the number of times that an operation is performed in the first mode corresponds to the preset number of times, the SIMO converter increases the frequency of the clock corresponding to the channel. When the number of times that an operation is performed in the second mode corresponds to the preset number of times, the SIMO converter reduces the frequency of the clock corresponding to the channel.

[0167] The SIMO converter **110**, the clock frequency controller **201**, the SIMO converter **300**, the controller **350**, and other apparatuses, and devices, and other components described herein with respect to FIGS. **1-22** are, and are implemented by, hardware components. Examples of hardware components that may be used to perform the operations described in this application where appropriate include controllers, sensors, generators, drivers, memories, comparators, arithmetic logic units, adders, subtractors, multipliers, dividers, integrators, and any other electronic components configured to perform the operations described in this application. In other examples, one or more of the hardware components that perform the operations described in this application are implemented by computing hardware, for example, by one or more processors or computers. A processor or computer may be implemented by one or more processing elements, such as an array of logic gates, a controller and an arithmetic logic unit, a digital signal processor, a microcomputer, a programmable logic control-

ler, a field-programmable gate array, a programmable logic array, a microprocessor, or any other device or combination of devices that is configured to respond to and execute instructions in a defined manner to achieve a desired result. In one example, a processor or computer includes, or is connected to, one or more memories storing instructions or software that are executed by the processor or computer. Hardware components implemented by a processor or computer may execute instructions or software, such as an operating system (OS) and one or more software applications that run on the OS, to perform the operations described in this application. The hardware components may also access, manipulate, process, create, and store data in response to execution of the instructions or software. For simplicity, the singular term "processor" or "computer" may be used in the description of the examples described in this application, but in other examples multiple processors or computers may be used, or a processor or computer may include multiple processing elements, or multiple types of processing elements, or both. For example, a single hardware component or two or more hardware components may be implemented by a single processor, or two or more processors, or a processor and a controller. One or more hardware components may be implemented by one or more processors, or a processor and a controller, and one or more other hardware components may be implemented by one or more other processors, or another processor and another controller. One or more processors, or a processor and a controller, may implement a single hardware component, or two or more hardware components. A hardware component may have any one or more of different processing configurations, examples of which include a single processor, independent processors, parallel processors, single-instruction single-data (SISD) multiprocessing, single-instruction multiple-data (SIMD) multiprocessing, multiple-instruction single-data (MISD) multiprocessing, and multiple-instruction multiple-data (MIMD) multiprocessing.

[0168] The methods illustrated and discussed with respect to FIG. **1-22** that perform the operations described in this application are performed by computing hardware, for example, by one or more processors or computers, implemented as described above executing instructions or software to perform the operations described in this application that are performed by the methods. For example, a single operation or two or more operations may be performed by a single processor, or two or more processors, or a processor and a controller. One or more operations may be performed by one or more processors, or a processor and a controller, and one or more other operations may be performed by one or more other processors, or another processor and another controller. One or more processors, or a processor and a controller, may perform a single operation, or two or more operations.

[0169] Instructions or software to control computing hardware, for example, one or more processors or computers, to implement the hardware components and perform the methods as described above may be written as computer programs, code segments, instructions or any combination thereof, for individually or collectively instructing or configuring the one or more processors or computers to operate as a machine or special-purpose computer to perform the operations performed by the hardware components and the methods as described above. In one example, the instructions or software include machine code that is directly executed by the one or more processors or computers, such as machine code produced by a compiler. In another example, the instructions or software include higher-level code that is executed by the one or more processors or computers using an interpreter. The instructions or software may be written using any programming language based on the block diagrams and the flow charts illustrated in the drawings and the corresponding descriptions in the specification, which disclose algorithms for performing the operations performed by the hardware components and the methods as described above.

[0170] The instructions or software to control computing hardware, for example, one or more processors or computers, to implement the hardware components and perform the methods as described above, and any associated data, data files, and data structures, may be recorded, stored, or fixed in or on one or more non-transitory computer-readable storage media. Examples of a non-transitory computer-readable storage medium include read-only memory (ROM), random-access programmable read only memory (PROM), electrically erasable programmable read-only memory (EEPROM), random-access memory (RAM), dynamic random access memory (DRAM), static random access memory (SRAM), flash memory, non-volatile memory, CD-ROMs, CD-Rs, CD+Rs, CD-RWs, CD+RWs, DVD-ROMs, DVD-Rs, DVD+Rs, DVD-RWs, DVD+RWs, DVD-RAMs, BD-ROMs, BD-Rs, BD-R LTHs, BD-REs, as non-limiting blue-ray or optical disk storage examples, hard disk drive (HDD), solid state drive (SSD), flash memory, a card type memory such as multimedia card micro or a card (for example, secure digital (SD) or extreme digital (XD)), magnetic tapes, floppy disks, magneto-optical data storage devices, optical data storage devices, hard disks, solid-state disks, and any other device that is configured to store the instructions or software and any associated data, data files, and data structures in a non-transitory manner and provide the instructions or software and any associated data, data files, and data structures to one or more processors or computers so that the one or more processors or computers can execute the instructions. In one example, the instructions or software and any associated data, data files, and data structures are distributed over network-coupled computer systems so that the instructions and software and any associated data, data files, and data structures are stored, accessed, and executed in a distributed fashion by the one or more processors or computers.

[0171] While this disclosure includes specific examples, it will be apparent to one of ordinary skill in the art that various changes in form and details may be made in these examples without departing from the spirit and scope of the claims and their equivalents. The examples described herein are to be considered in a descriptive sense only, and not for purposes of limitation. Descriptions of features or aspects in each example are to be considered as being applicable to similar features or aspects in other examples. Suitable results may be achieved if the described techniques are performed in a different order, and/or if components in a described system, architecture, device, or circuit are combined in a different manner, and/or replaced or supplemented by other components or their equivalents. Therefore, the scope of the disclosure is defined not by the detailed description, but by the claims and their equivalents, and all variations within the scope of the claims and their equivalents are to be construed as being included in the disclosure.

What is claimed is:

1. A single-inductor multiple-output (SIMO) converter comprising:

a converter configured to provide respective voltages of a plurality of channels with a single inductor; and

a control logic configured to control switches of the converter based on clocks corresponding to the plurality of channels,

wherein the control logic is configured to compare an output voltage of a selected channel of the plurality of channels that corresponds to a control target to a reference voltage of the selected channel based on a clock of the selected channel and operate in one of a first mode that adaptively adjusts a number of times that a pulse triggering a power transfer to the channel is generated, and a second mode that blocks a generation of the pulse.

2. The SIMO converter of claim **1**, wherein the control logic is further configured to repetitively generate the pulse in the first mode until the output voltage of the selected channel is higher than the reference voltage of the selected channel based on a determination that the output voltage of the channel is lower than the reference voltage of the channel.

3. The SIMO converter of claim **1**, wherein the control logic is further configured to block the generation of the pulse in the second mode based on a determination that the output voltage of the selected channel is higher than the reference voltage of the selected channel.

4. The SIMO converter of claim **1**, wherein the control logic is further configured to dynamically control a frequency of the clock corresponding to the selected channel based on a number of times that an operation is performed in the first mode and a number of times that an operation is performed in the second mode.

5. The SIMO converter of claim **1**, wherein the converter is further configured to provide the respective voltages of the plurality of channels based on the clocks having different phases based on a time multiplexing scheme.

6. The SIMO converter of claim **1**, wherein, in the first mode, the control logic is further configured to adaptively adjust the number of times that the pulse is generated in a time interval initiated in response to an edge of the clock corresponding to the selected channel.

7. The SIMO converter of claim **1**, wherein the converter comprises:

the single inductor; and

a switching unit comprising first switches configured to select the plurality of channels and second switches configured to control a flow of a current flowing in the single inductor.

8. The SIMO converter of claim **7**, wherein the first switches are configured to connect output ports of the plurality of channels and the single inductor in series.

9. The SIMO converter of claim **7**, wherein the second switches comprise a 2-1st switch, a 2-2nd switch, and a 2-3rd switch,

the 2-1st switch is configured to have a first end connected to an input port of the converter and a second end connected to a first end of the single inductor,

the 2-2nd switch is configured to have a first end connected to the first end of the single inductor, and a second end of the 2-2nd switch is grounded, and

the 2-3rd switch is configured to have a first end connected to a second end of the single inductor, and a second end of the 2-3rd switch is grounded.

10. The SIMO converter of claim **7**, wherein the control logic comprises:

a switch controller configured to select a first switch for the selected channel from among the first switches in response to the pulse being generated, and control the second switches based on a sequence for generating a desired voltage of the channel.

11. The SIMO converter of claim **10**, wherein the control logic is configured to dynamically control a duty-ratio of the second switches based on an input voltage of the converter.

12. The SIMO converter of claim **1**, wherein the control logic is further configured to reset a current of the single inductor after the power transfer is triggered due to the generation of the pulse.

13. The SIMO converter of claim **1**, wherein the control logic is further configured to dynamically control a frequency of the clock corresponding to the channel based on a load in the channel.

14. The SIMO converter of claim **1**, wherein the control logic comprises:

a comparator configured to latch the output voltage of the channel at an edge of the clock corresponding to the channel, and compare the latched output voltage to the reference voltage of the channel.

15. The SIMO converter of claim **1**, wherein the control logic is further configured to generate the clocks corresponding to the plurality of channels based on an importance level of the plurality of channels and control lengths of time intervals corresponding to phases of the clocks.

16. A control method comprising:

comparing, based on a clock of a selected channel corresponding to a control target among a plurality of channels, an output voltage of the selected channel to a reference voltage of the selected channel;

selecting a first mode when the output voltage is lower than the reference voltage, and selecting a second mode when the output voltage is higher than the reference voltage;

adaptively adjusting, when the first mode is selected, a number of times that a pulse triggering a power transfer to the selected channel is generated; and

blocking a generation of the pulse when the second mode is selected.

17. The control method of claim **16**, wherein the adaptively adjusting the number of times that the pulse is generated comprises:

repetitively generating the pulse until the output voltage of the selected channel is higher than the reference voltage of the selected channel based on the first mode.

18. The control method of claim **16**, wherein the adaptively adjusting the number of times that the pulse is generated comprises:

adaptively adjusting the number of times that the pulse is generated in a time interval initiated in response to an edge of the clock corresponding to the selected channel.

19. The control method of claim **16**, further comprising:

counting a number of times that an operation is performed in the first mode and a number of times that an operation is performed in the second mode; and

dynamically controlling a frequency of the clock corresponding to the selected channel based on a determination that the counted number of times corresponds to a preset number of times.

20. The control method of claim **19**, wherein the dynamically controlling the frequency of the clock comprises:

increasing the frequency of the clock corresponding to the selected channel when the number of times that an operation is performed in the first mode corresponds to the preset number of times.

21. The control method of claim **19**, wherein the dynamically controlling the frequency of the clock comprises:

reducing the frequency of the clock corresponding to the selected channel when the number of times that an operation is performed in the second mode corresponds to the preset number of times.

22. A non-transitory computer-readable storage medium storing instructions that, when executed by a processor, cause the processor to perform the control method of claim **16**.

23. A method comprising:

comparing, in a single inductor multiple output (SIMO) converter, an output voltage of a selected channel among a plurality of channels to a reference voltage of the selected channel based on a clock of the selected channel;

selecting a burst mode when the output voltage of the selected channel is less than or equal to the reference voltage, and

selecting a pulse skip mode when the output voltage of the selected channel is greater than the reference voltage.

24. The method of claim **23**, further comprising adjusting a number of times a pulse triggering a power transfer to the selected channel is generated when the burst mode is selected, and blocking a generation of the pulse when the pulse skip mode is selected.

25. The method of claim **23**, wherein the SIMO converter dynamically controls a frequency of the clock corresponding to the selected channel by comparing a number of times that an operation is performed in the burst mode to a preset number of times, and comparing a number of times that an operation is performed in the pulse skip mode to the preset number of times.

26. The method of claim **25**, wherein the SIMO converter increases a frequency of the clock corresponding to the selected channel when the number of times that the operation is performed in the burst mode corresponds to the preset number of times.

27. The method of claim **25**, wherein the SIMO converter reduces the frequency of the clock corresponding to the selected channel when the number of times that an operation is performed in the pulse skip mode corresponds to the preset number of times.

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