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(54) **SEMICONDUCTOR DEVICE, METHOD OF FABRICATING THE SAME, AND PATTERNING METHOD**

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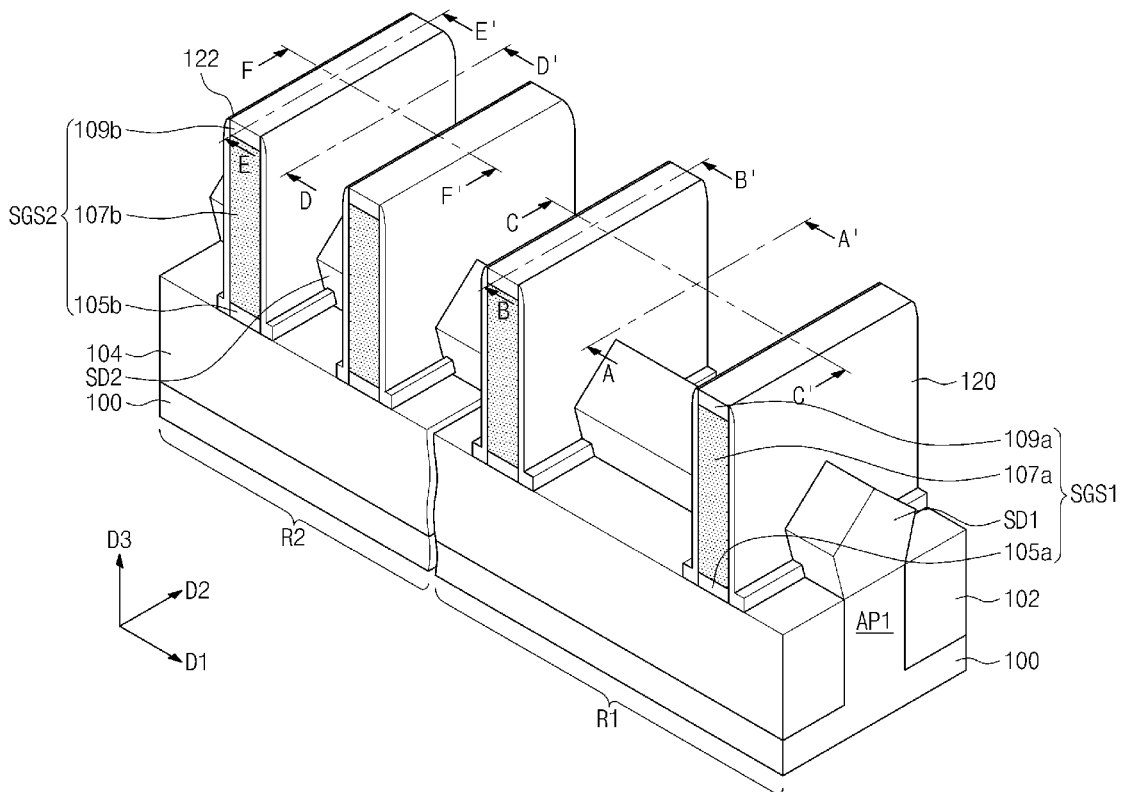
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(57) **ABSTRACT**

A method of fabricating a semiconductor device includes forming first and second active patterns on first and second regions, respectively, of a substrate, forming first and second gate structures on the first and second active patterns, respectively, forming a coating layer to cover the first and second gate structures and the first and second active patterns, and forming a first recess region in the first active pattern between the first gate structures and a second recess region in the second active pattern between the second gate structures.



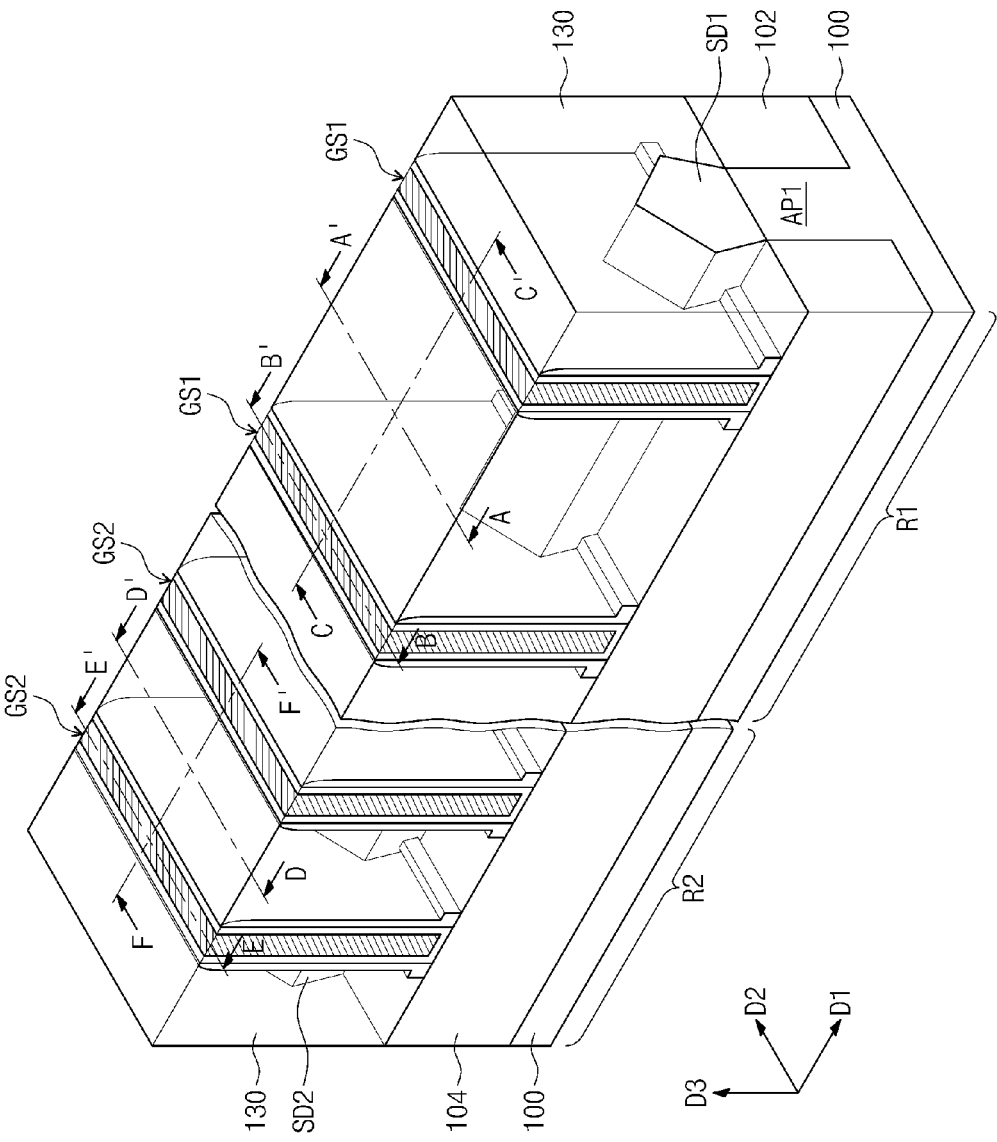


FIG. 1A

FIG. 2A

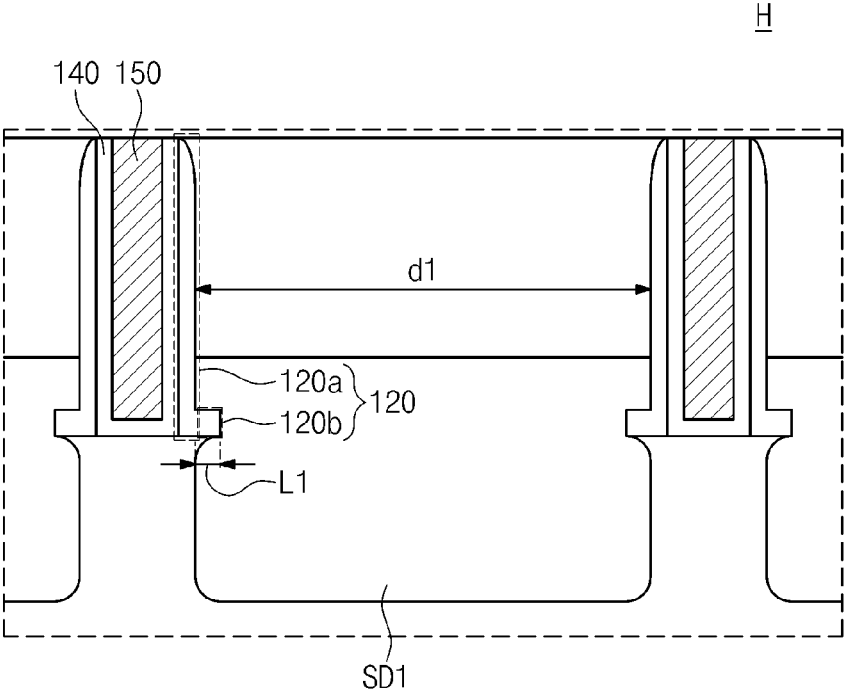


FIG. 2B

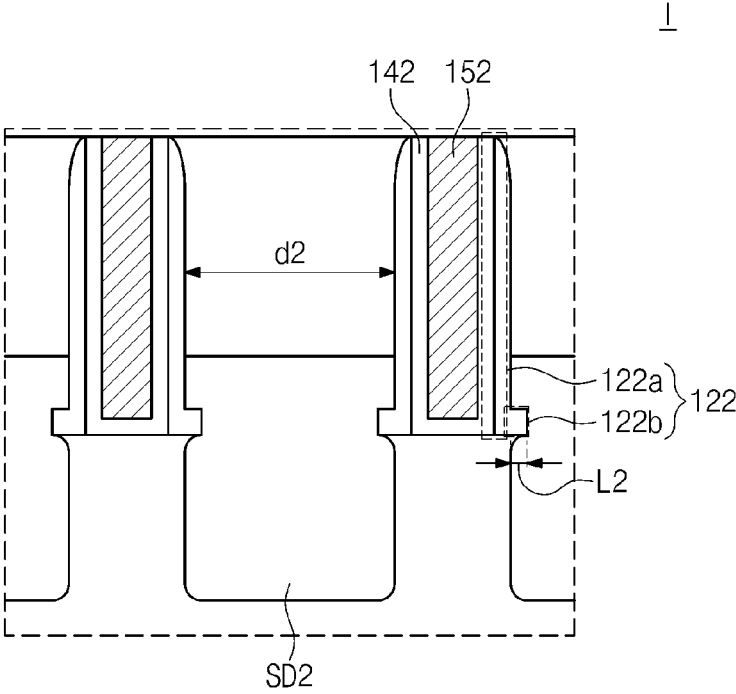


FIG. 3A

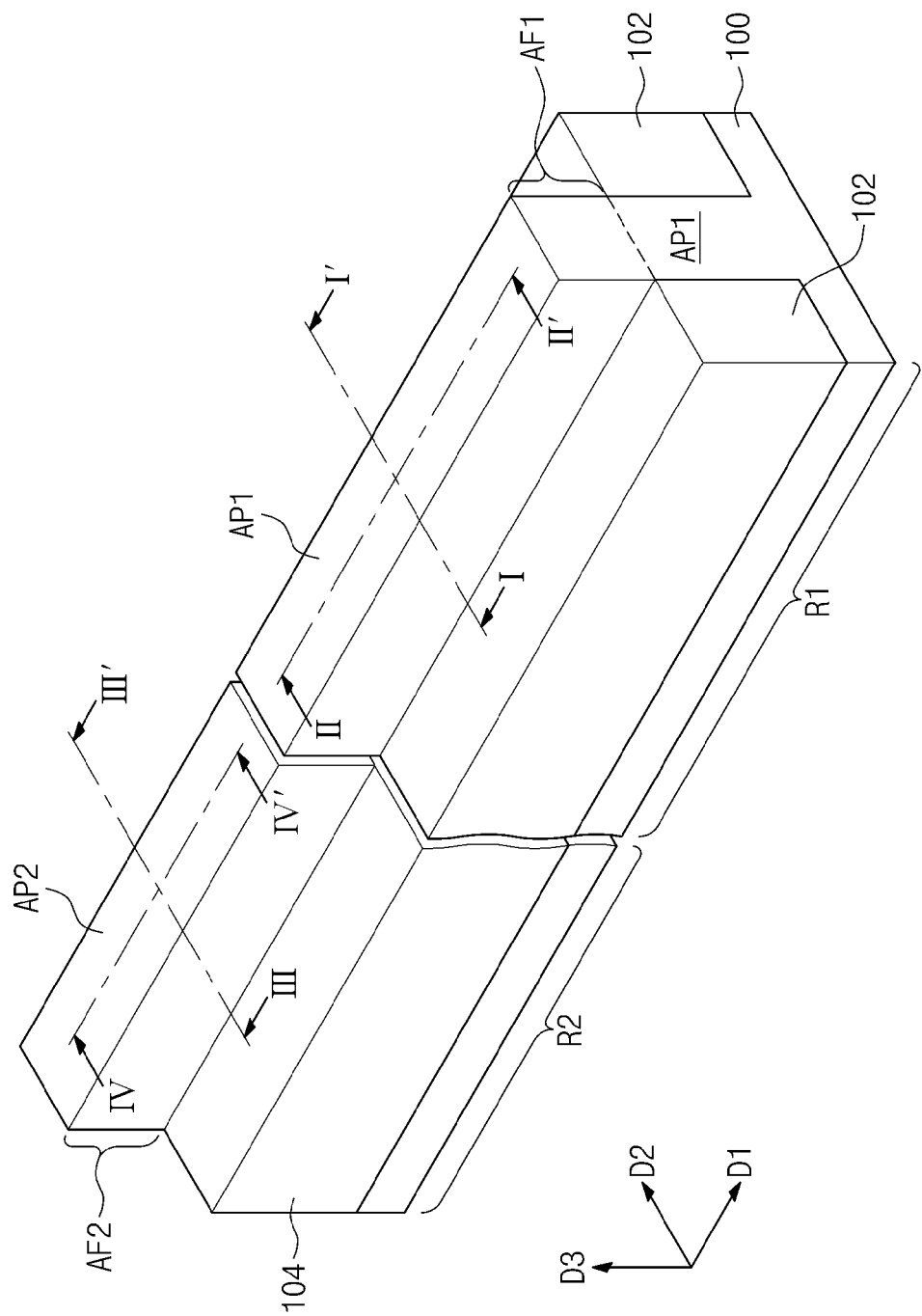


FIG. 3B

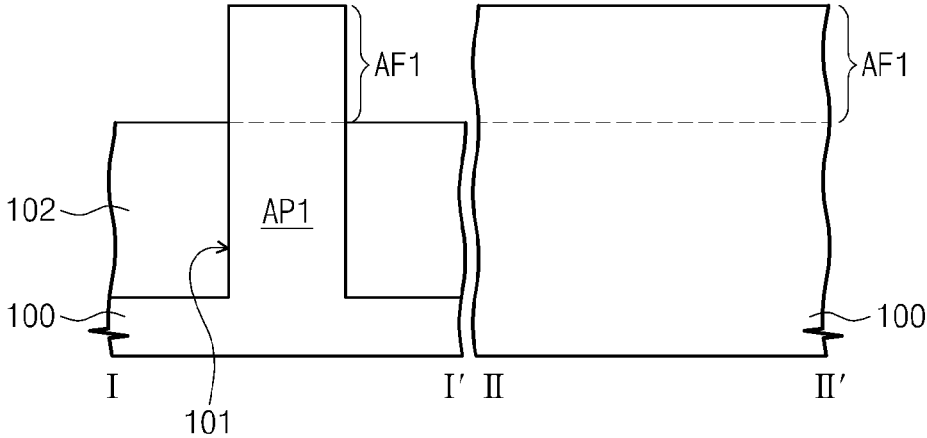


FIG. 3C

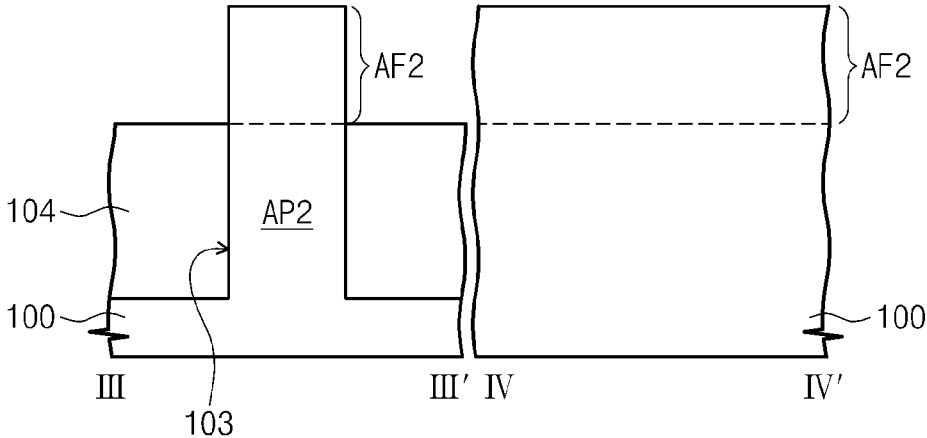


FIG. 4A

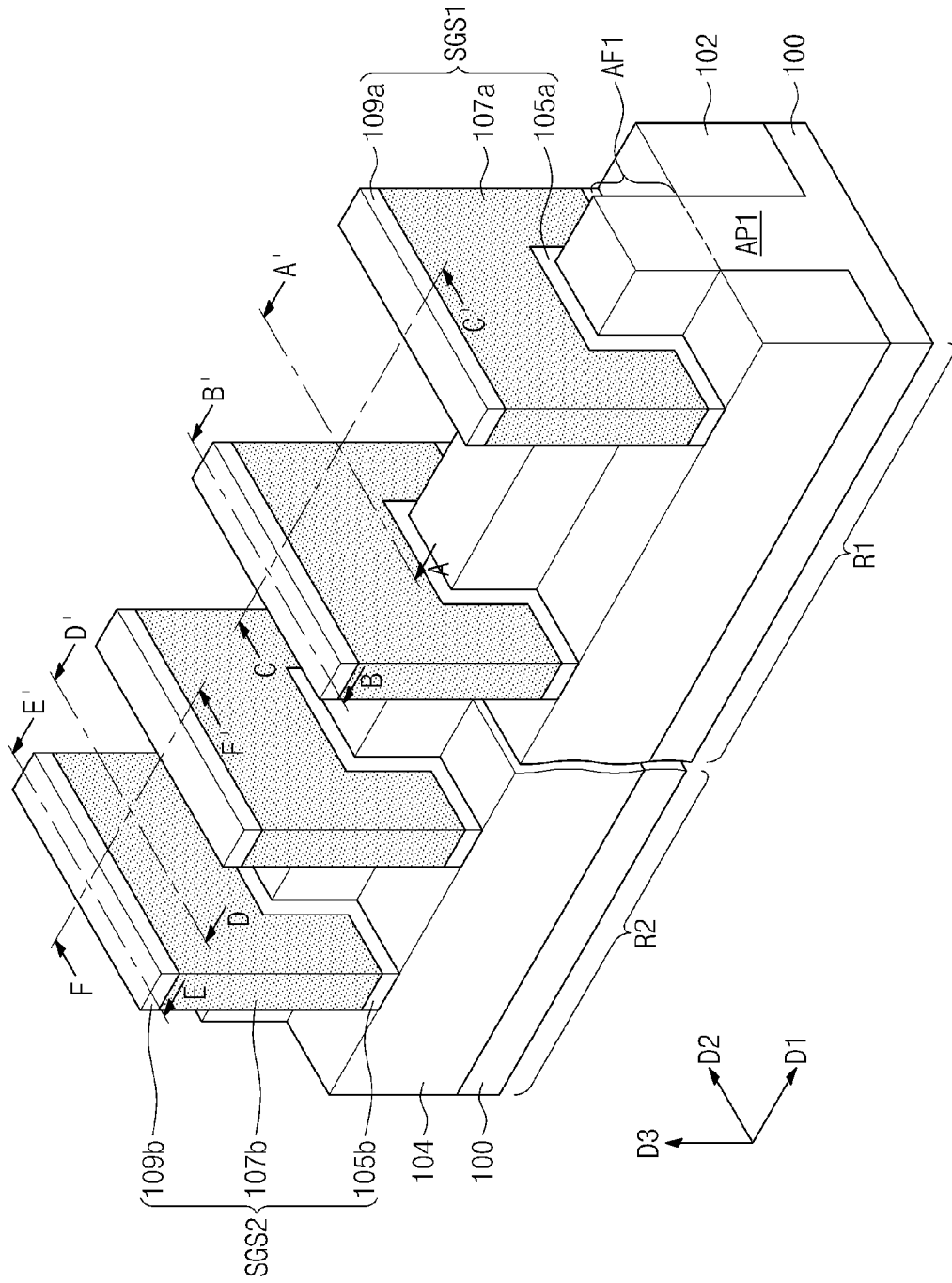


FIG. 4B

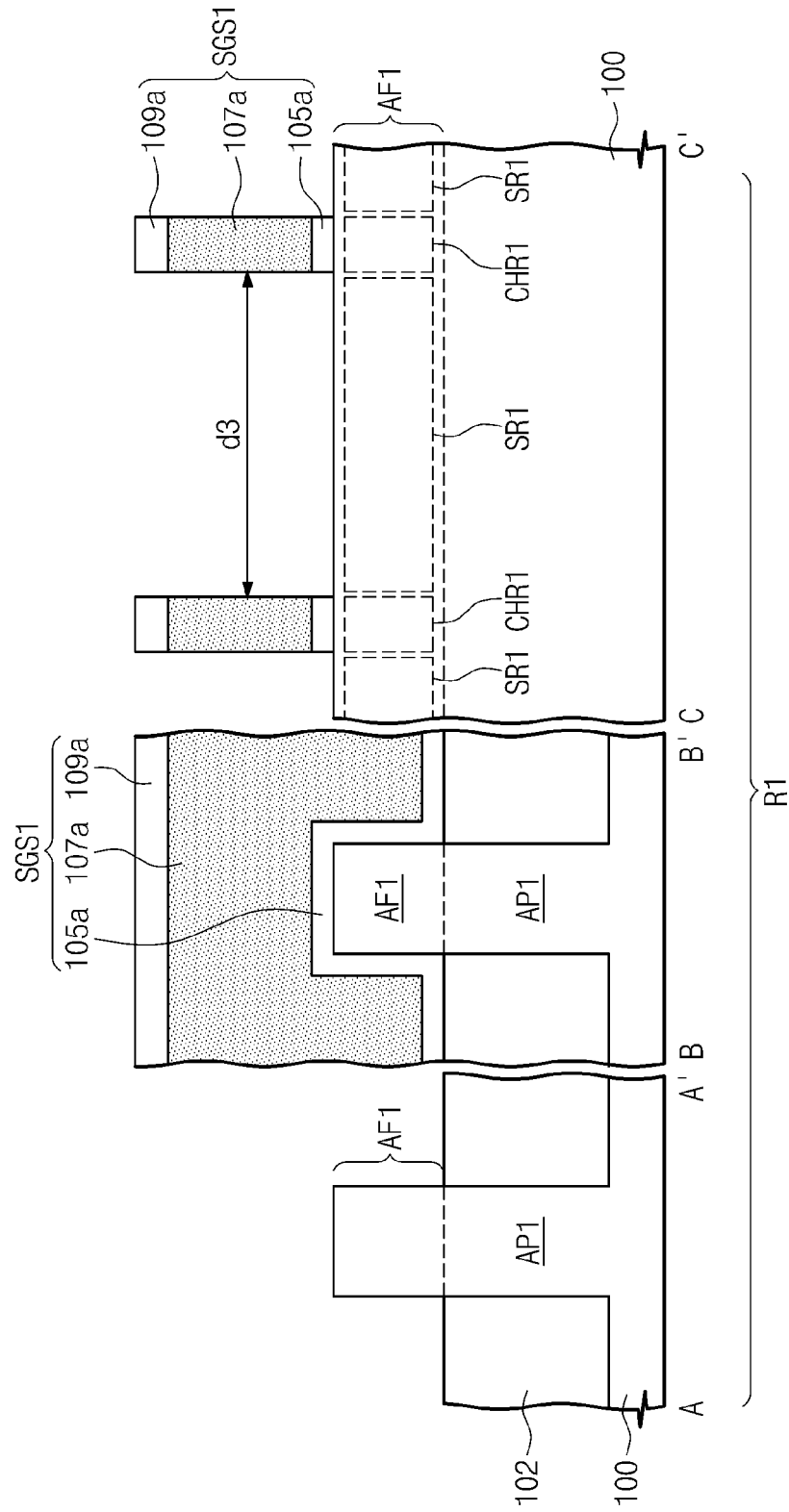


FIG. 5A

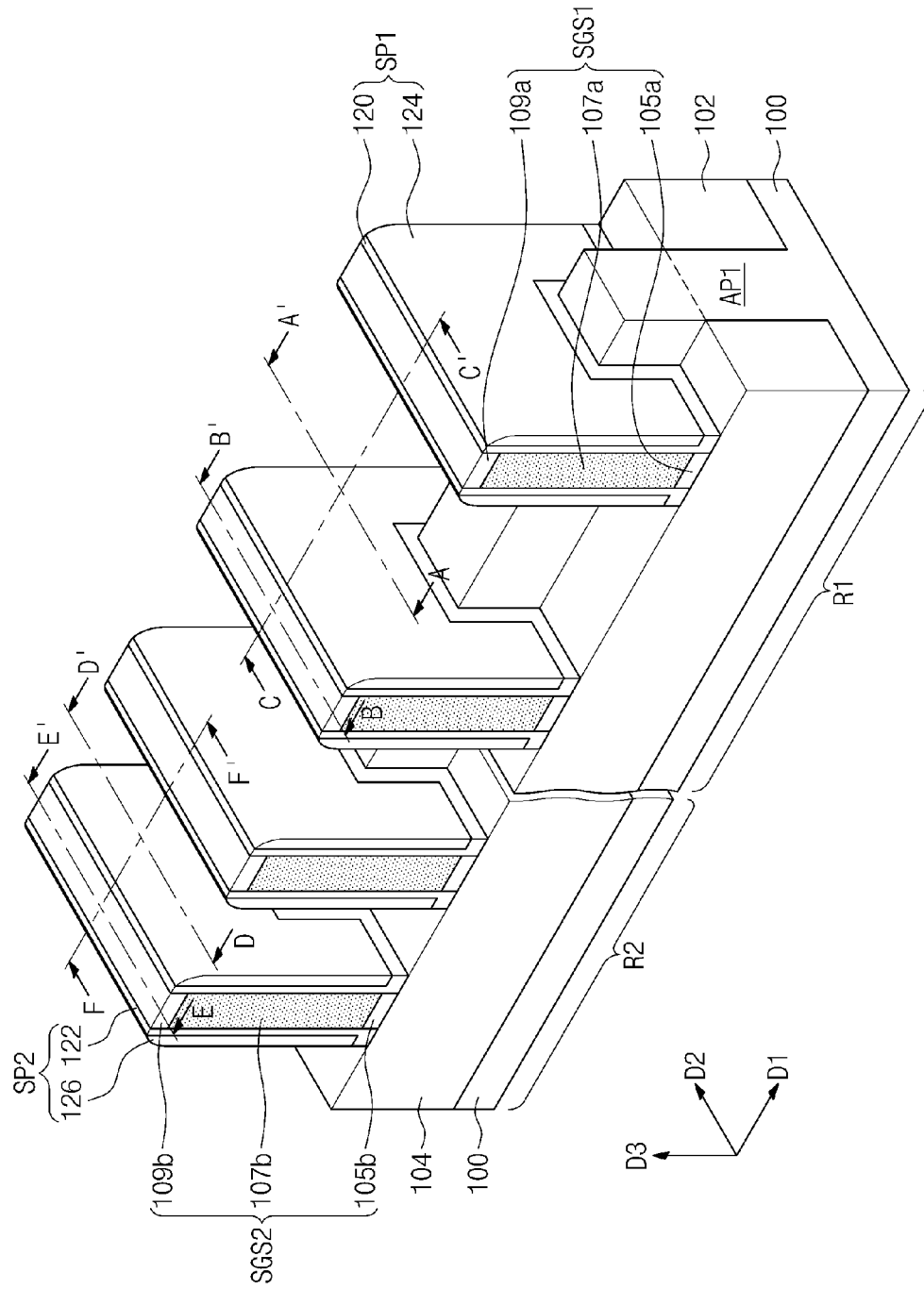


FIG. 5B

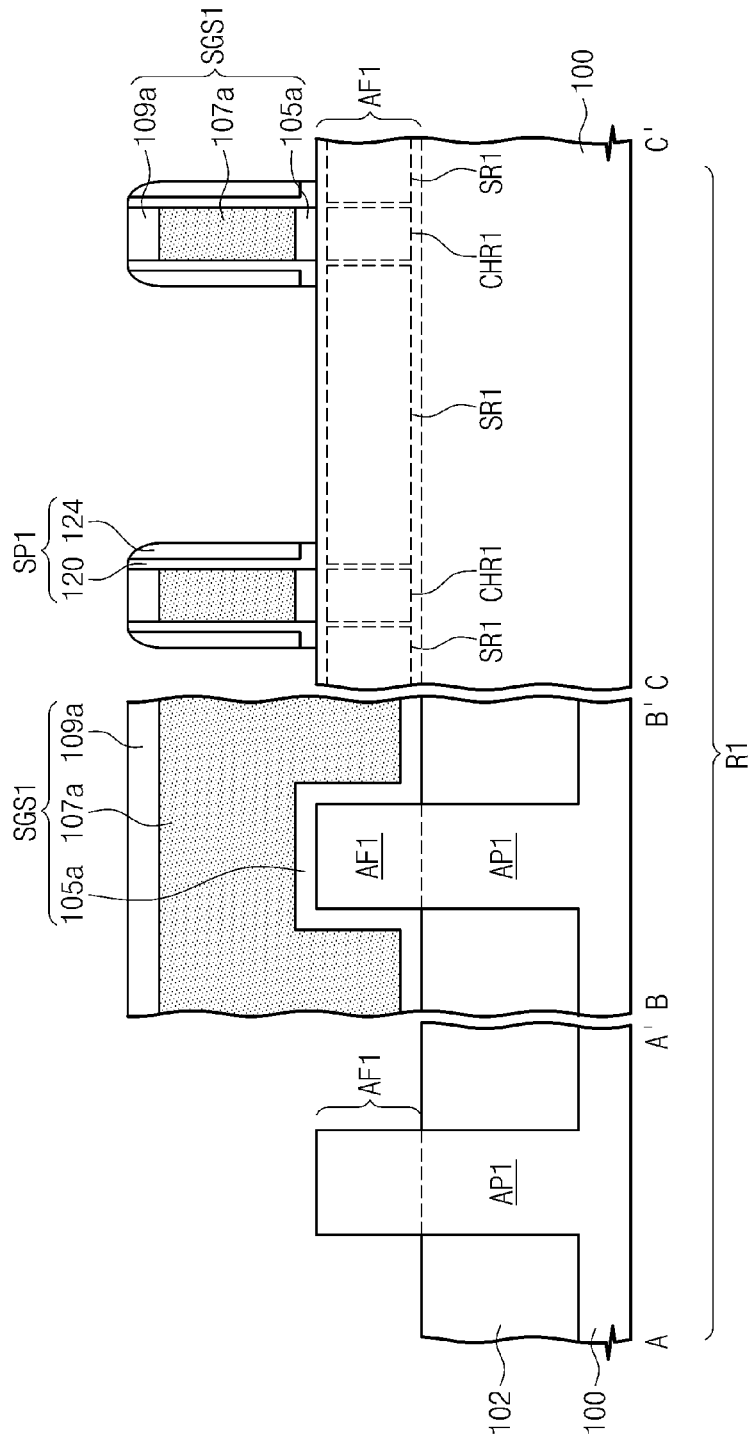


FIG. 6B

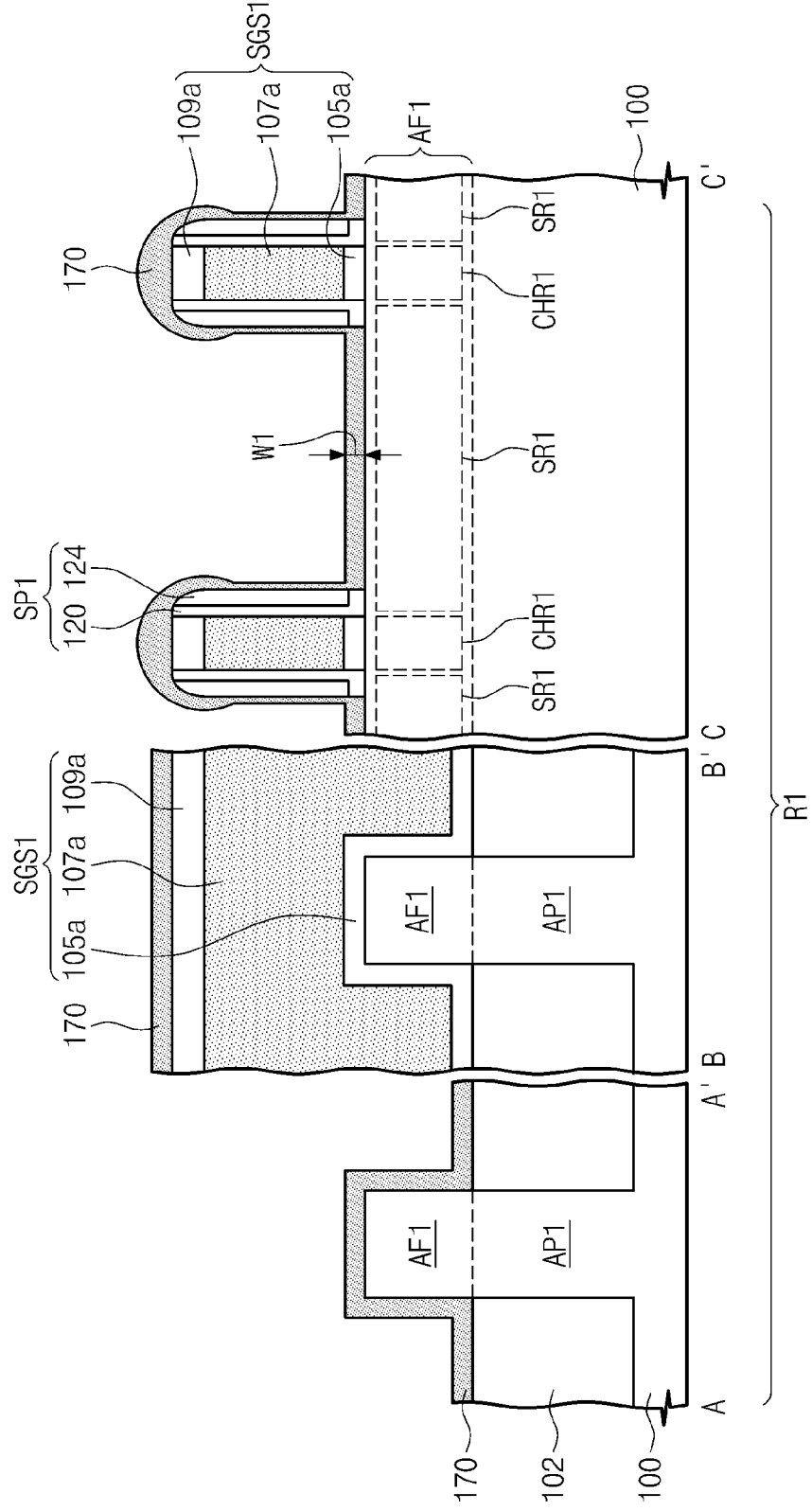


FIG. 6C

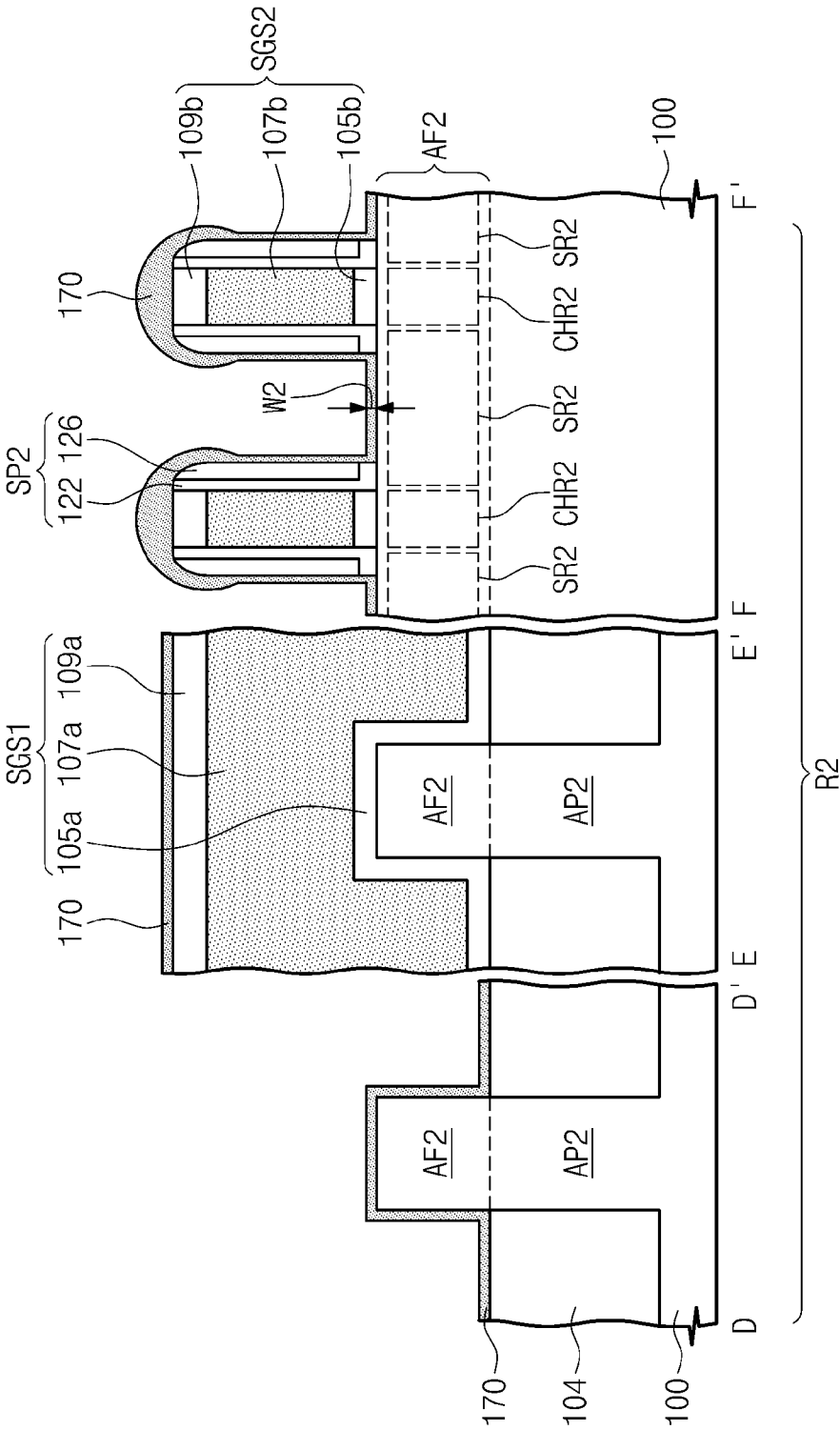


FIG. 7B

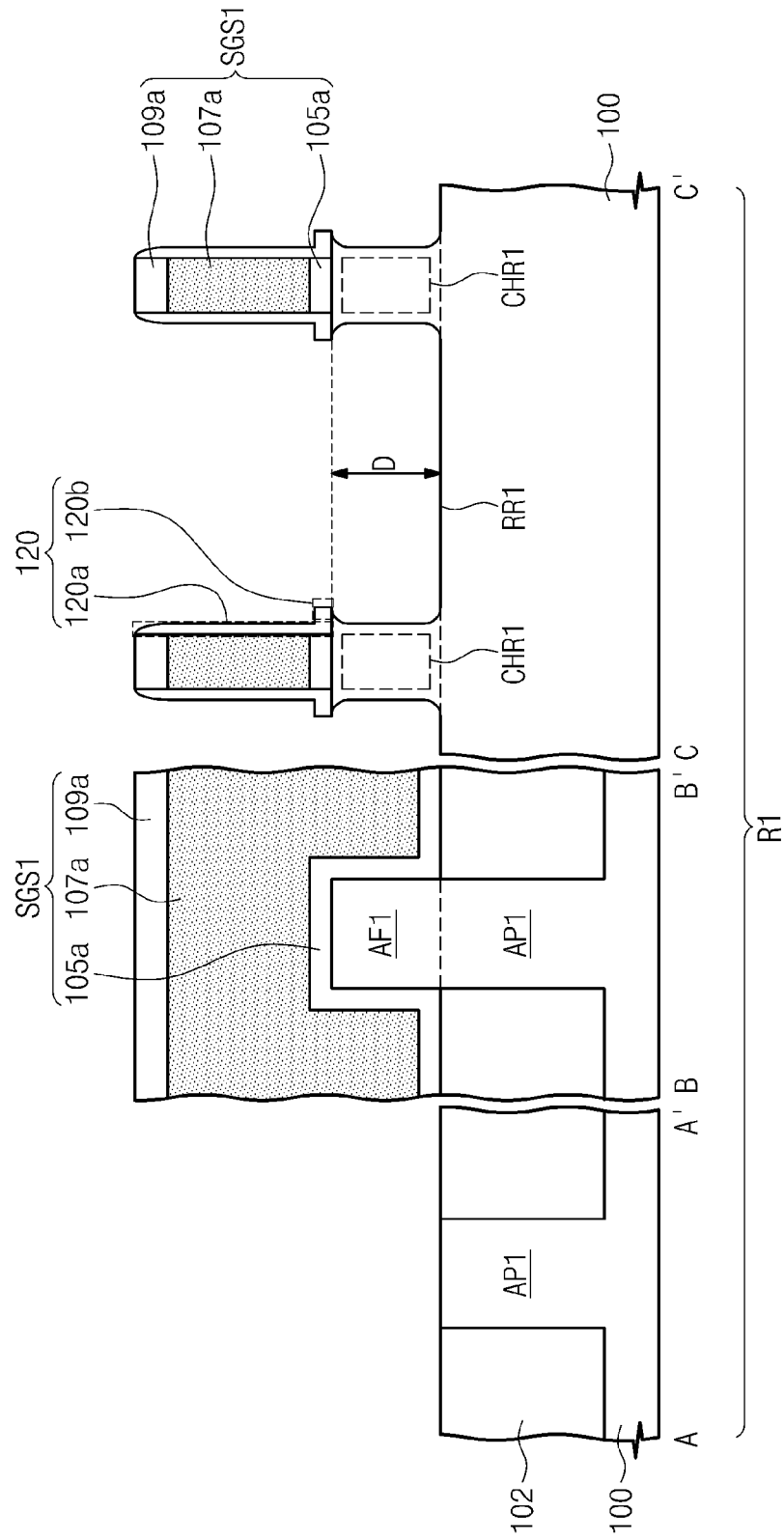


FIG. 8A

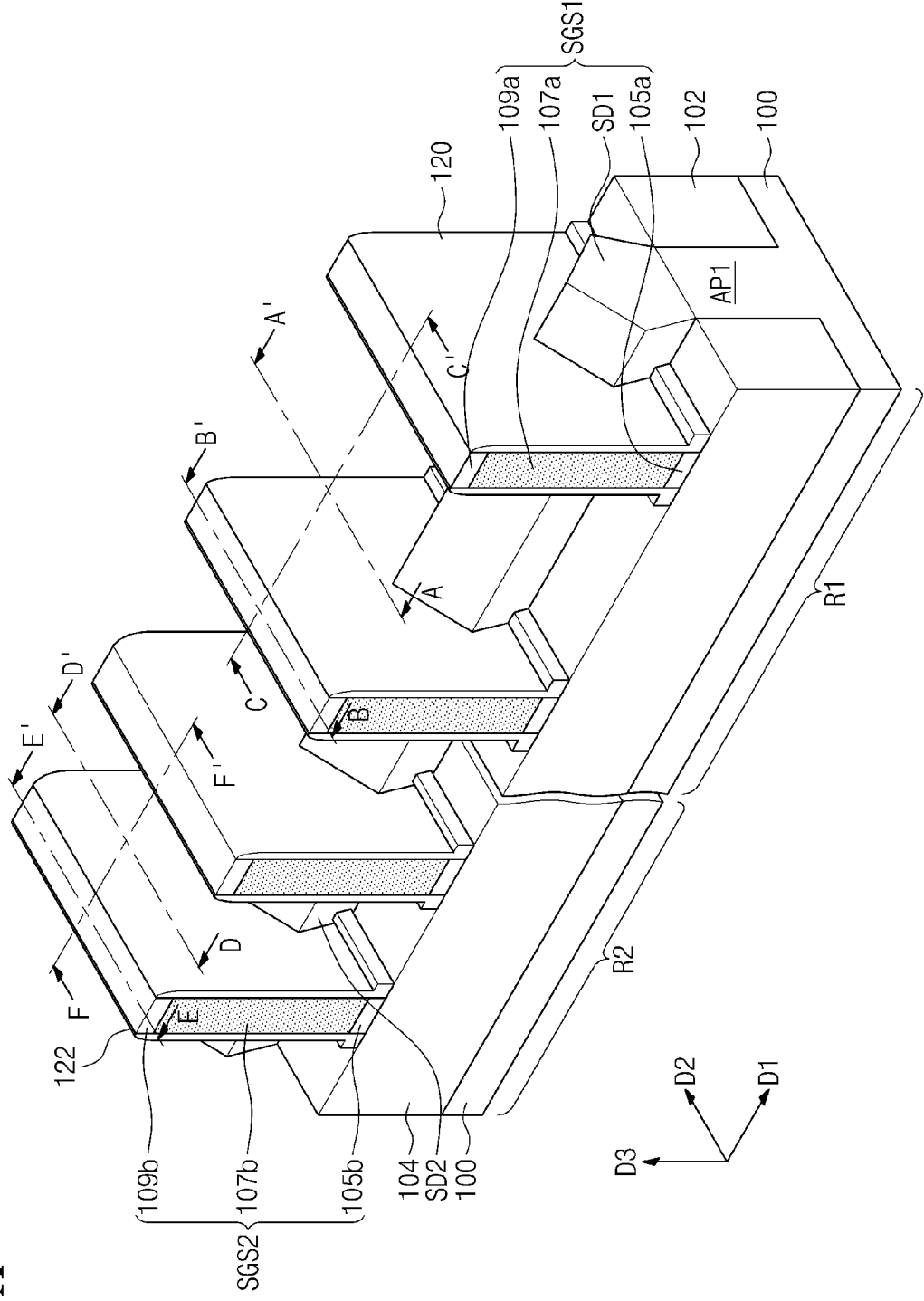
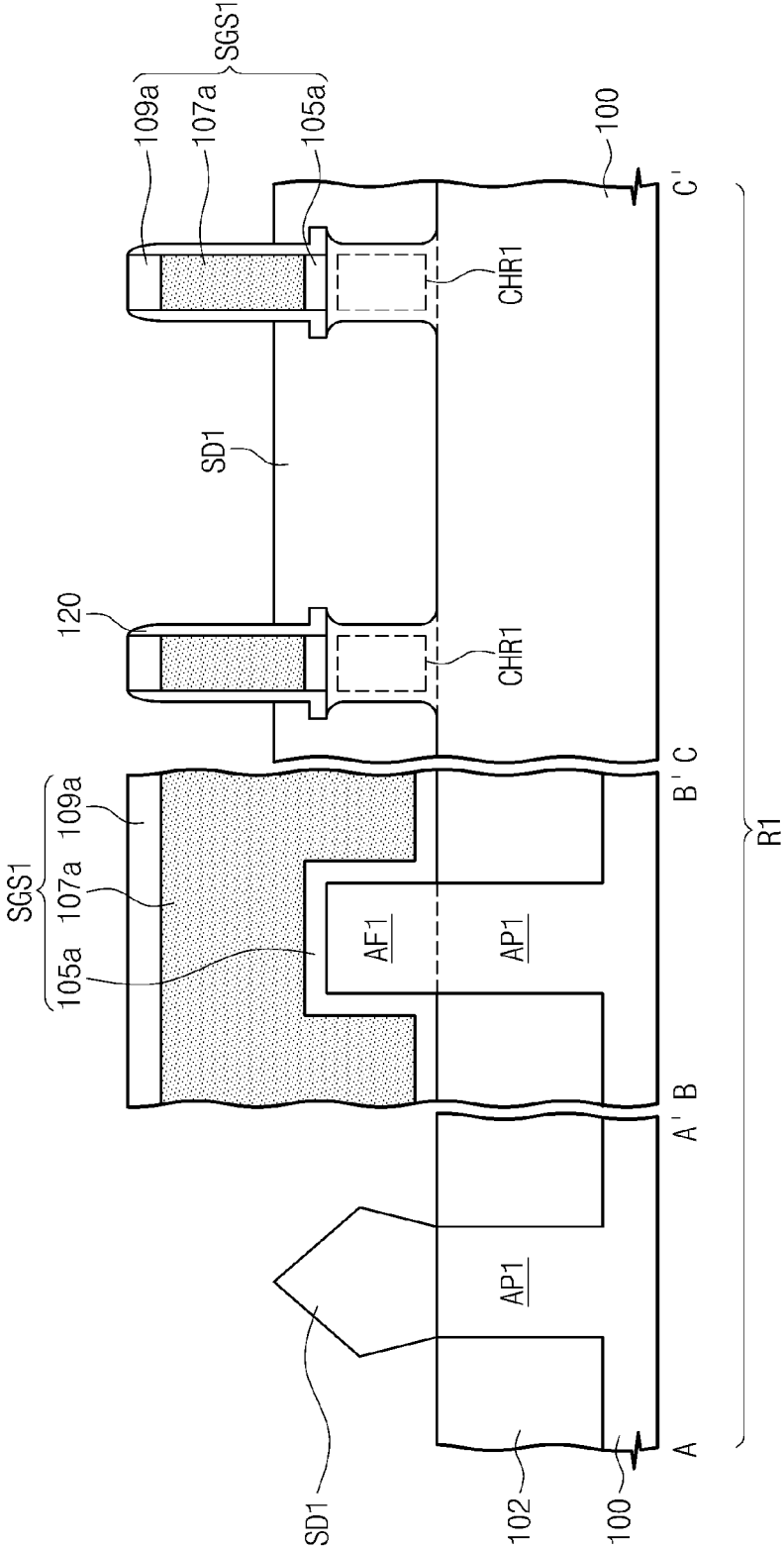


FIG. 8B



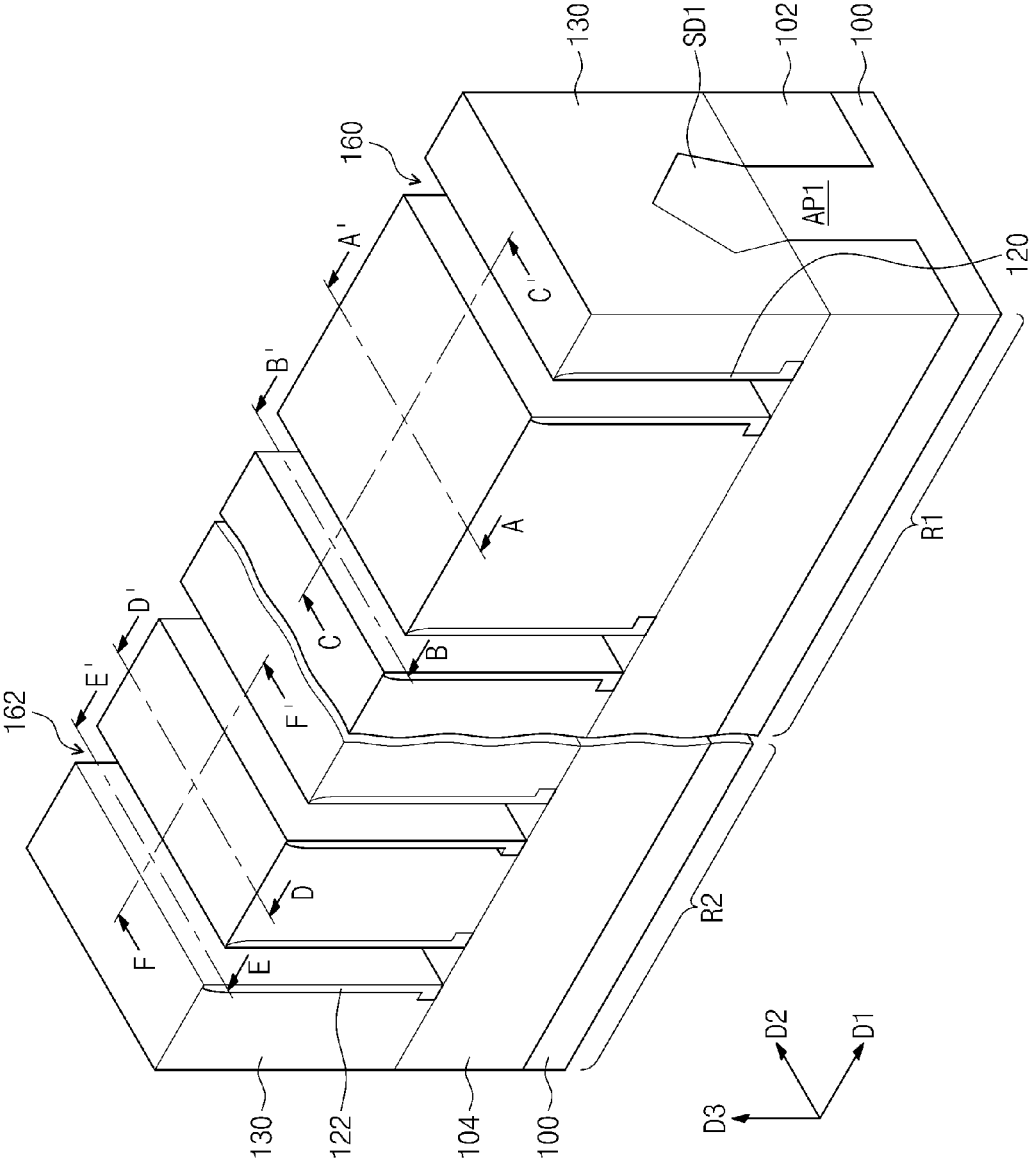


FIG. 9A

FIG. 9B

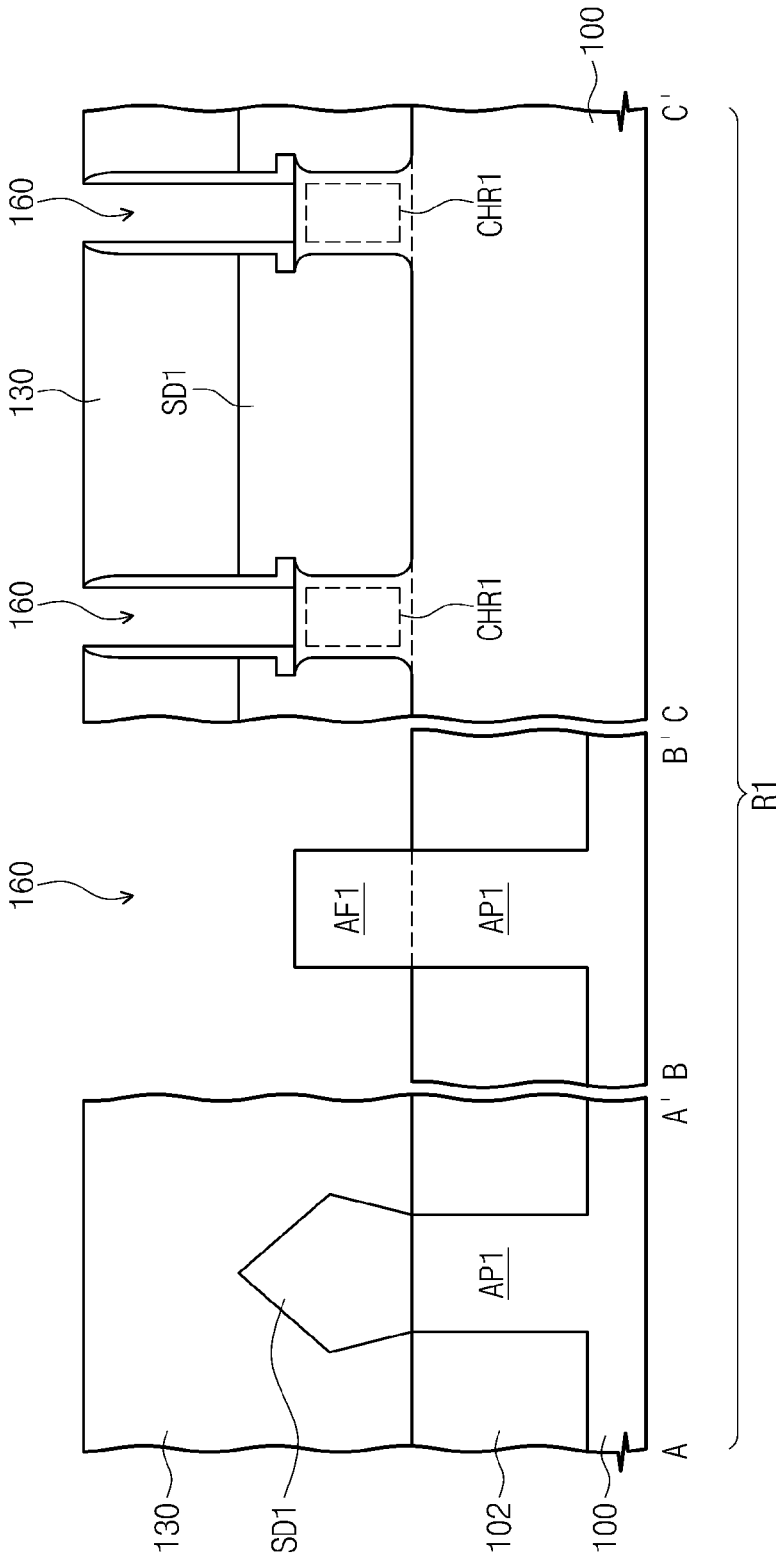
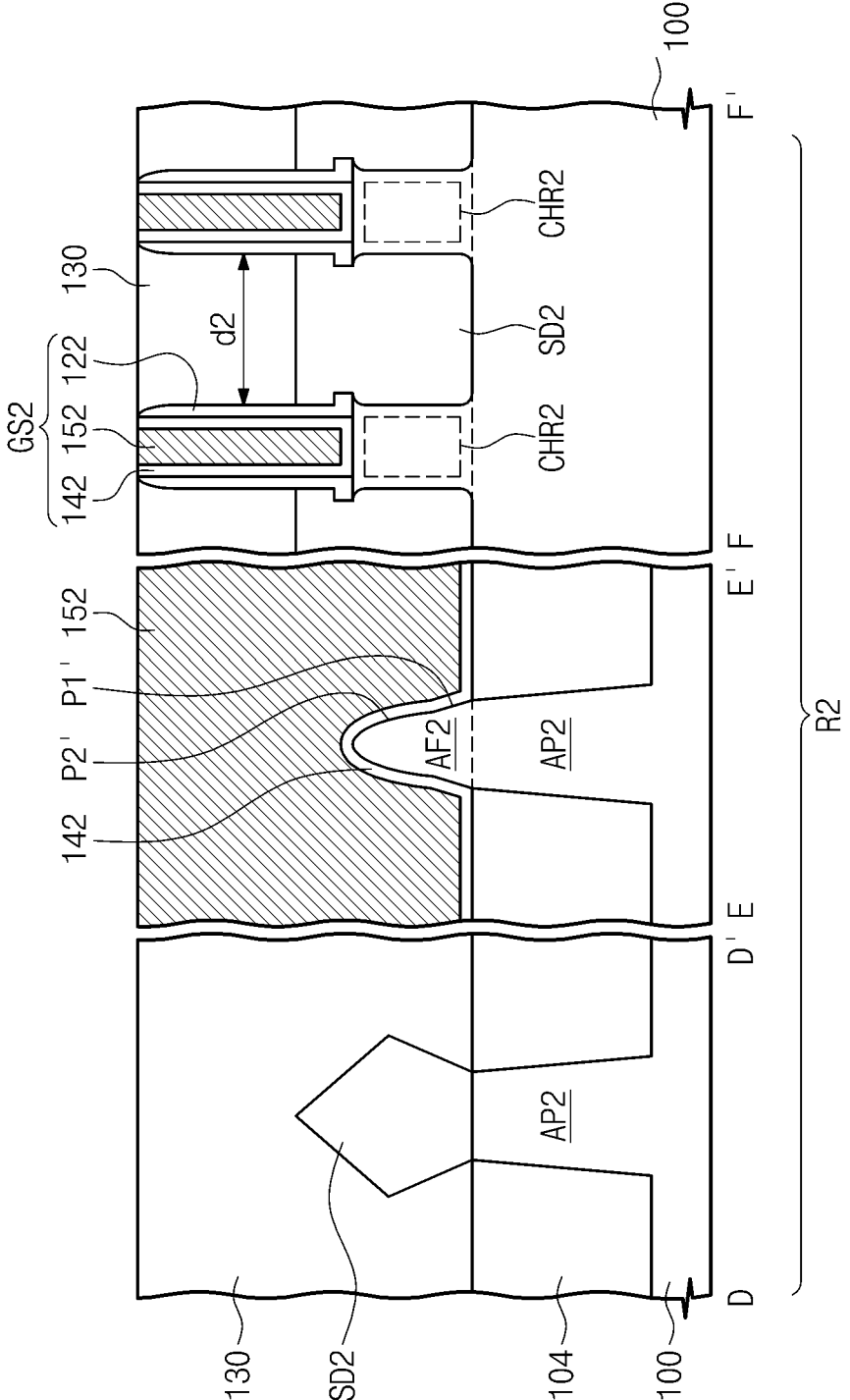


FIG. 10B



**SEMICONDUCTOR DEVICE, METHOD OF
FABRICATING THE SAME, AND
PATTERNING METHOD**

PRIORITY STATEMENT

[0001] This U.S. non-provisional patent application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2015-0134699, filed on September 23, 2015, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] The inventive concept relates to semiconductor devices, and in particular, to semiconductor devices having different series of patterns and the forming of recesses in regions where the different series of patterns are provided. For example, the inventive concept relates to semiconductor devices having metal-oxide-semiconductor field-effect transistors (MOS-FETs) and the forming of recesses in which source/drains of the MOS-FETs are epitaxially grown.

[0003] A semiconductor device may include integrated circuits (ICs) including metal-oxide-semiconductor field-effect transistors (MOS-FETs). As the size and design rule of such semiconductor devices decrease, the MOS-FETs are being increasingly scaled down. The reduction in size of the MOS-FET may lead to deterioration in operational properties of the semiconductor device. A variety of studies are being conducted to overcome technical limitations associated with the scaling-down of semiconductor devices and to realize high performance semiconductor devices.

SUMMARY

[0004] According to the inventive concept, there is provided a method of fabricating a semiconductor device including providing a substrate having a first region and a second region, forming first and second active patterns at the first and second regions, respectively, of the substrate, forming first gate structures across the first active pattern as spaced apart from each other by a first distance along the first active pattern, forming second gate structures across the second active pattern as spaced apart from each other by a second distance along the second active pattern, forming a coating layer to cover the first and second gate structures and the first and second active patterns, performing a recess process to form a first recess in the first active pattern between the first gate structures and a second recess in the second active pattern between the second gate structures, and forming a source/drain epitaxial layer in the first and second recesses. The coating layer is formed to a first thickness on a region of the first active pattern between the first gate structures and to have a second thickness different from the first thickness on a region of the second active pattern between the second gate structures.

[0005] According to the inventive concept, there is also provided a semiconductor device including a substrate with a first region and a second region, a first active pattern provided on the first region of the substrate, a second active pattern provided on the second region of the substrate, first gate structures spaced apart from each other by a first distance to cross the first active pattern, second gate structures spaced apart from each other by a second distance to cross the second active pattern, a first source/drain region provided on the first active pattern between the first gate

structures, and a second source/drain region provided on the second active pattern between the second gate structures. Each of the first gate structures may include a first gate pattern and a first gate spacer on an outer side surface of the first gate pattern, the first gate spacer including a first protrusion protruding from a lower portion of the first gate spacer by a first length in a direction parallel to the first active pattern, each of the second gate structures may include a second gate pattern and a second gate spacer on an outer side surface of the second gate pattern, the second gate spacer including a second protrusion protruding from a lower portion of the second gate spacer by a second length in a direction parallel to the second active pattern, and the first length may be different from the second length.

[0006] According to the inventive concept, there is also provided a patterning method including forming first and second patterns on first and second regions, respectively, of a substrate and in which the first and second patterns have first and second aspect ratios different from each other, and the first and second patterns are formed by forming a coating layer to first and second thicknesses on the first and second regions, respectively, and performing a recessing process to form first and second recesses to substantially the same depths in the first and second regions, respectively.

[0007] According to the inventive concept, there is also provided a semiconductor device including an active pattern on a substrate, a gate electrode provided to cross the active pattern, gate spacers provided on side surfaces of the gate electrode, and source/drain regions provided on the active pattern at both sides of the gate electrode. The gate spacer may include a first portion in contact with the side surfaces of the gate electrode, and a second portion protruding from a lower portion of the first portion in a direction parallel to the active pattern.

[0008] According to the inventive concept, there is also provided

[0009] a method of manufacturing a semiconductor device having first and second regions disposed beside one another so as to not overlap, and which includes forming a series of first features as spaced from each other along a first direction in the first region of the device at an upper surface of a substrate and forming a series of second features as spaced from each other along a second direction in the second region of the device at the upper surface of the substrate and such that the spacing between adjacent ones of the first features in the first direction is greater than the spacing between adjacent ones of the second features in the second direction, subsequently forming a coating on the upper surface of the substrate and which covers the first and second regions of the device and in which the thickness of the coating in the first region of the device at a location between the adjacent ones of the first features is greater than the thickness of the coating in the second region of the device at a locations between the adjacent ones of the second features, and performing an etching process that etches through the coating at respective locations in the first and second regions of the device and forms a first recess in the substrate in the first region of the device and a second recess in the substrate in the second region of the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The inventive concept will be more clearly understood from the following detailed description of examples thereof taken in conjunction with the accompanying draw-

ings. The accompanying drawings represent non-limiting examples as described hereinafter.

[0011] FIG. 1A is a perspective view illustrating a semiconductor device according to some examples of the inventive concept.

[0012] FIG. 1B is a sectional view illustrating sections taken along lines A-A', B-B', and C-C' of FIG. 1A.

[0013] FIG. 1C is a sectional view illustrating sections taken along lines D-D', E-E', and F-F' of FIG. 1A.

[0014] FIG. 2A is an enlarged view of a portion 'H' of FIG. 1B.

[0015] FIG. 2B is an enlarged view of a portion 'I' of FIG. 1C.

[0016] FIGS. 3A, 4A, 5A, 6A, 7A, 8A and 9A are perspective views illustrating a method of fabricating a semiconductor device, according to some examples of the inventive concept.

[0017] FIGS. 3B and 3C are sectional views illustrating sections taken along lines I-I', II-II' and IV-IV' of FIG. 3A.

[0018] FIGS. 4B, 5B, 6B, 7B, 8B and 9B are sectional views illustrating sections taken along lines A-A', B-B', and C-C' of FIGS. 4A to 9A, respectively.

[0019] FIGS. 4C, 5C, 6C, 7C, 8C and 9C are sectional views illustrating sections taken along lines D-D', E-E', and F-F' of FIGS. 4A to 9A, respectively.

[0020] FIGS. 10A and 10B are sectional views illustrating a semiconductor device according to some examples of the inventive concept.

[0021] It should be noted that these figures are intended to illustrate the general characteristics of methods, structure and/or materials utilized in certain examples and to supplement the written description provided below. These drawings are not, however, to scale and may not precisely reflect the precise structural or performance characteristics of any given example, and should not be interpreted as defining or limiting the range of values or properties encompassed by examples. For example, the relative thicknesses and positioning of molecules, layers, regions and/or structural elements may be reduced or exaggerated for clarity. The use of similar or identical reference numbers in the various drawings is intended to indicate the presence of a similar or identical element or feature.

DETAILED DESCRIPTION

[0022] The inventive concepts will now be described more fully hereinafter with reference to the accompanying drawings, in which examples of the inventive concepts are shown. The inventive concepts and methods of achieving them will be apparent from the following examples that will be described in more detail with reference to the accompanying drawings. The inventive concept may, however, be exemplified in different forms and should not be construed as limited to the examples set forth herein. Rather, these examples are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive concept to those skilled in the art.

[0023] As used herein, the singular terms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it may be directly connected or coupled to the other element or intervening elements may be present.

[0024] Similarly, it will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may be present. In contrast, the term "directly" means that there are no intervening elements. Additionally, the sectional views may be idealized views. Accordingly, shapes shown in the sectional views may differ from the actual shapes according to manufacturing techniques and/or allowable errors. Therefore, the inventive concepts are not limited to the specific shape illustrated in the exemplary views, but may include other shapes that may be created according to manufacturing processes.

[0025] Other terminology used herein for the purpose of describing particular examples of the inventive concept is to be taken in context. For example, the terms "comprises" or "comprising" when used in this specification specifies the presence of stated features or processes but does not preclude the presence or additional features or processes. The term "substrate" as used alone will be understood as referring basically to any underlying structure of one or more layers. The term "extending" will generally refer to the longest dimension of a particular feature, especially the lengthwise dimension or longitudinal direction in the case of a linear feature. The term "pattern" may refer to one feature in a series of similar features that have been formed by some patterning process. The term "about" as used with reference to parameters or conditions of a process will be understood as meaning equal to but is used encompass slight variations inherent in the particular process being described. The term "spacing" between features may be used synonymously with the term pitch and will generally refer to the average spacing between regularly spaced apart features in a linear array of the features.

[0026] Examples of aspects of the present inventive concepts explained and illustrated herein include their complementary counterparts. The same reference numerals or the same reference designators denote the same elements throughout the drawings.

[0027] FIG. 1A is a perspective view illustrating a semiconductor device according to some examples of the inventive concept. FIG. 1B is a sectional view illustrating sections taken along lines A-A', B-B', and C-C' of FIG. 1A, and FIG. 1C is a sectional view illustrating sections taken along lines D-D', E-E', and F-F' of FIG. 1A. FIG. 2A is an enlarged view of a portion 'H' of FIG. 1B, and FIG. 2B is an enlarged view of a portion 'I' of FIG. 1C.

[0028] Referring to FIGS. 1A to 1C, active patterns and gate structures crossing the active patterns may be provided on a substrate 100. The substrate 100 may be a semiconductor substrate. As an example, the substrate 100 may be a bulk silicon wafer or a silicon-on-insulator (SOI) wafer.

[0029] The substrate 100 (or device in general) may include a first region R1 and a second region R2. The active patterns may include a first active pattern AP1 on the first region R1 and a second active pattern AP2 on the second region R2. The gate structures may include a first gate structure GS1 crossing the first active pattern AP1 and a second gate structure GS2 crossing the second active pattern AP2.

[0030] When viewed in plan, each of the first and second active patterns AP1 and AP2 may be a line-shaped structure extending in a direction. The extension directions of the first and second active patterns AP1 and AP2 may be the same or different from each other. Hereinafter, for the sake of sim-

plicity, the description that follows will refer to an example in which each of the first and second active patterns AP1 and AP2 extends in a first direction D1.

[0031] Each of the first and second active patterns AP1 and AP2 may be provided to have a longitudinal axis parallel to the first direction D1 and a transverse axis parallel to a second direction D2 crossing the first direction D1. Each of the first and second active patterns AP1 and AP2 may be provided to have a structure upwardly protruding from the substrate 100. For example, each of the first and second active patterns AP1 and AP2 may protrude in a third direction D3 that is orthogonal to both of the first and second directions D1 and D2.

[0032] First device isolation patterns 102 may be provided at both sides of the first active pattern AP1, and second device isolation patterns 104 may be provided at both sides of the second active pattern AP2. The first and second device isolation patterns 102 and 104 may be formed of or include oxide, nitride, and/or oxynitride. Each of the first and second device isolation patterns 102 and 104 may be a line-shaped structure extending in the first direction D1. The first device isolation patterns 102 may be spaced apart from each other with the first active pattern AP1 interposed therebetween in the second direction D2, and the second device isolation patterns 104 may be spaced apart from each other with the second active pattern AP2 interposed therebetween in the second direction D2.

[0033] Each of the first device isolation patterns 102 may be provided to partially cover a side surface of the first active pattern AP1. For example, the first device isolation patterns 102 may be provided to expose an upper portion of the first active pattern AP1. The upper portion of the first active pattern AP1 exposed by the first device isolation patterns 102 will be referred to as a first active fin AF1. Each of the second device isolation patterns 104 may be provided to partially cover a side surface of the second active pattern AP2. For example, the second device isolation patterns 104 may be provided to expose an upper portion of the second active pattern AP2. The upper portion of the second active pattern AP2 exposed by the second device isolation patterns 104 will be referred to as a second active fin AF2.

[0034] In some examples, a plurality of the first gate structures GS1 may be provided to cross the first active pattern AP1. A plurality of the second gate structures GS2 may be provided to cross the second active pattern AP2. Each of the first gate structures GS1 may extend in the second direction D2 and may be spaced apart from each other in the first direction D1. Similarly, each of the second gate structures GS2 may extend in the second direction D2 and may be spaced apart from each other in the first direction D1. A first distance d1 between adjacent ones of the first gate structures GS1 may be greater than a second distance d2 between adjacent ones of the second gate structures GS2.

[0035] The first gate structure GS1 may cross the first active pattern AP1 and may cover a top surface and both side surfaces of the first active fin AF1. The first active fin AF1 may be locally provided below the first gate structure GS1. The first active fin AF1 may include a first channel region CHR1. The second gate structure GS2 may cross the second active pattern AP2 and may cover a top surface and both side surfaces of the second active fin AF2. The second active fin AF2 may be locally provided below the second gate structure GS2. The second active fin AF2 may include a second channel region CHR2.

[0036] Referring to FIGS. 1A, 1B, and 2A, the first gate structure GS1 may include a first gate electrode 150 crossing the first active pattern AP1, a first gate spacer 120 on both side surfaces of the first gate electrode 150, and a first gate dielectric pattern 140 between the first gate electrode 150 and the first gate spacer 120.

[0037] The first gate spacer 120 may include a first portion 120a and a first protrusion 120b. The first portion 120a of the first gate spacer 120 may be in contact with an outer side surface of the first gate electrode 150 and may extend parallel to the first gate electrode 150. The first protrusion 120b may be positioned at a lower portion of the first gate spacer 120 and may extend from the first portion 120a in a direction away from the first gate structure GS1. For example, the first protrusion 120b may protrude outward from the first gate electrode 150. As an example, the first protrusion 120b may extend in the first direction D1. The first protrusion 120b may protrude from the first portion 120a by a first length L1. In some examples, the portion of the first gate spacer 120 where the first protrusion 120b meets the first portion 120a may be concave, i.e., the outer surface of the first gate spacer 120 where the first protrusion 120b meets the first portion 120a may be rounded. In certain examples, a portion of the first active pattern AP1 positioned below the first protrusion 120b may be recessed in a direction toward the first gate electrode 150. In this example, the portion of the first active pattern AP1 positioned below the first protrusion 120b may be concave, i.e., the outer surface where the portion of the first active pattern AP1 meets the first protrusion 120b may be rounded.

[0038] The first gate dielectric pattern 140 may include a portion interposed between the first gate electrode 150 and the first active fin AF1. Furthermore, the first gate dielectric pattern 140 may extend horizontally to partially cover top surfaces of the first device isolation patterns 102. The first gate dielectric pattern 140 may extend along a bottom surface of the first gate electrode 150.

[0039] Referring to FIGS. 1A, 1C, and 2B, the second gate structure GS2 may include a second gate electrode 152 crossing the second active pattern AP2, a second gate spacer 122 on both side surfaces of the second gate electrode 152, and a second gate dielectric pattern 142 between the second gate electrode 152 and the second gate spacer 122.

[0040] The second gate spacer 122 may include a second portion 122a and a second protrusion 122b. The second portion 122a of the second gate spacer 122 may be in contact with an outer side surface of the second gate electrode 152 and may extend parallel to the second gate electrode 152. The second protrusion 122b may be positioned at a lower portion of the second gate spacer 122 and may extend from the second portion 122a in a direction away from the second gate structure GS2. The second protrusion 122b may protrude outward from the second gate electrode 152. As an example, the second protrusion 122b may extend in the first direction D1. The second protrusion 122b may protrude from the second portion 122a by a second length L2. Here, the second length L2 may be shorter than the first length L1. For example, the second length L2 may be shorter by about 5 Å to about 2 nm than the first length L1. In some examples, a portion of the second gate spacer 122 where the second protrusion 122b meets the second portion 122a may be concave, i.e., the outer surface of the second gate spacer 122 where the second protrusion 122b meets the second portion 122a may be rounded. In certain examples, a portion of the

second active pattern AP2 positioned below the second protrusion 122b may be recessed in a direction toward the second gate electrode 152. In this example, the portion of the second active pattern AP2 positioned below the second protrusion 122b where the second active pattern AP2 meets second protrusion 122b may be concave, i.e., the outer surface of the second active pattern AP2 where the second active pattern AP2 meets second protrusion 122b may be rounded.

[0041] The second gate dielectric pattern 142 may include a portion interposed between the second gate electrode 152 and the second active fin AF2. Furthermore, the second gate dielectric pattern 142 may extend horizontally to partially cover top surfaces of the second device isolation patterns 104. The second gate dielectric pattern 142 may extend along a bottom surface of the second gate electrode 152.

[0042] First source/drain regions SD1 may be provided on the first active pattern AP1 and at both sides, respectively, of the first gate structure GS1. The first source/drain regions SD1 may be epitaxial patterns that are epitaxially grown from the first active pattern AP1. The first source/drain regions SD1 may be formed of or include at least one of silicon germanium (SiGe), silicon (Si), and silicon carbide (SiC).

[0043] Second source/drain regions SD2 may be provided on the second active pattern AP2 and at both sides, respectively, of the second gate structure GS2. The second source/drain regions SD2 may be epitaxial patterns that are epitaxially grown from the second active pattern AP2. The second source/drain regions SD2 may be formed of or include at least one of silicon germanium (SiGe), silicon (Si), and silicon carbide (SiC).

[0044] The first and second gate electrodes 150 and 152 may be formed of or include at least one material selected from the group consisting of conductive metal nitrides (e.g., titanium nitride or tantalum nitride) and metals (e.g., aluminum or tungsten). The first and second gate spacers 120 and 122 may be formed of or include a nitride (e.g., silicon nitride). The first and second gate dielectric patterns 140 and 142 may include a high-k dielectric material. For example, the first and second gate dielectric patterns 140 and 142 may be formed of or include at least one of hafnium oxide, hafnium silicate, zirconium oxide, and zirconium silicate, but the inventive concept may not be limited thereto.

[0045] A lower interlayer insulating layer 130 may be provided on the substrate 100 to cover the first and second gate structures GS1 and GS2 and the first and second source/drain regions SD1 and SD2. The lower interlayer insulating layer 130 may have a top surface coplanar with those of the first and second gate structures GS1 and GS2 and may be formed of or include at least one of silicon oxide, silicon nitride, silicon oxynitride, and low-k dielectric materials.

[0046] Although not shown, an upper interlayer insulating layer may be further provided on the substrate 100 provided with the first and second gate structures GS1 and GS2. The upper interlayer insulating layer may be formed of or include at least one of, for example, oxides, nitrides, and oxynitrides. First and second contact holes may be formed to penetrate the upper interlayer insulating layer and the lower interlayer insulating layer 130. The first contact holes may be provided to expose the first source/drain regions SD1, and the second contact holes may be provided to expose the second source/drain regions SD2. Contact plugs

may be provided in the first and second contact holes, respectively. Interconnection lines may be provided on the upper interlayer insulating layer. The interconnection lines may be connected to at least one of the contact plugs. In some examples, each of the first and second source/drain regions SD1 and SD2 may be electrically connected to a corresponding one of the interconnection lines through the contact plug. The contact plugs and the interconnection lines may be formed of or include a conductive material.

[0047] FIGS. 3A to 9A are perspective views illustrating a method of fabricating a semiconductor device, according to some examples of the inventive concept. FIGS. 3B and 3C are sectional views illustrating sections taken along lines I-I', II-II', III-III', and IV-IV' of FIG. 3A, FIGS. 4B to 9B are sectional views illustrating sections taken along lines A-A', B-B, and C-C' of FIGS. 4A to 9A, respectively, and FIGS. 4C to 9C are sectional views illustrating sections taken along lines D-D', E-E', and F-F' of FIGS. 4A to 9A, respectively.

[0048] Referring to FIGS. 3A to 3C, the substrate 100 with the first and second regions R1 and R2 may be provided. The substrate 100 may be a bulk silicon wafer or a silicon-on-insulator (SOI) wafer. In the first region R1, the substrate 100 may be patterned to form first trenches 101 defining the first active pattern AP1. In the second region R2, the substrate 100 may be patterned to form second trenches 103 defining the second active pattern AP2. The first trenches 101 and the second trenches 103 may be formed simultaneously using the same process. The first trenches 101 may extend in the first direction D1 and may be spaced apart from each other in the second direction D2 crossing the first direction D1. Accordingly, the first active pattern AP1 may have a linear shape extending in the first direction D1. In addition, the second trenches 103 may extend in the first direction D1 and may be spaced apart from each other in the second direction D2. Accordingly, the second active pattern AP2 may have a linear shape extending in the first direction D1.

[0049] The forming of the first and second trenches 101 and 103 may include forming mask patterns on the substrate 100 and anisotropically etching the substrate 100 using mask patterns as an etch mask. Although not shown, each of the first and second trenches 101 and 103 may be formed to have a downwardly decreasing width, and thus, each of the first and second active patterns AP1 and AP2 may be formed to have an upwardly decreasing width.

[0050] The first device isolation patterns 102 may be formed to fill the first trenches 101 and the second device isolation patterns 104 may be formed to fill the second trenches 103. The forming of the first and second device isolation patterns 102 and 104 may include forming a device isolation layer on the substrate 100 to fill the first and second trenches 101 and 103 and planarizing the device isolation layer to expose the mask pattern.

[0051] Subsequently, the first and second device isolation patterns 102 and 104 may be vertically recessed to expose upper portions of the first and second active patterns AP1 and AP2. The vertical recessing of the first and second device isolation patterns 102 and 104 may be performed using, for example, a wet etching process having an etch selectivity with respect to the first and second active patterns AP1 and AP2. The upper portion of the first active pattern AP1 exposed by the first device isolation patterns 102 will be used as the first active fin AF1, and the upper portion of the second active pattern AP2 exposed by the second device

isolation patterns **104** will be used as the second active fin AF2. The vertical recessing of the first and second device isolation patterns **102** and **104** may be performed to remove the mask patterns and to thereby expose the top surfaces of the first and second active fins AF1 and AF2.

[0052] Referring to FIGS. 4A to 4C, the etch stop layer and the sacrificial gate layer may be sequentially formed on the substrate **100** to cover the first and second active fins AF1 and AF2. The etch stop layer may include, for example, a silicon oxide layer. The sacrificial gate layer may include material having an etch selectivity with respect to the etch stop layer. The sacrificial gate layer may be, for example, a polysilicon layer.

[0053] The sacrificial gate layer may be patterned to form a first sacrificial gate pattern **107a** and a second sacrificial gate pattern **107b** on the substrate **100**, and the first and second sacrificial gate patterns **107a** and **107b** may be formed to cross the first and second active fins AF1 and AF2, respectively. The forming of the first and second sacrificial gate patterns **107a** and **107b** may include forming a first gate mask pattern **109a** on the sacrificial gate layer of the first region R1, forming a second gate mask pattern **109b** on the sacrificial gate layer of the second region R2, and etching the sacrificial gate layer using the first and second gate mask patterns **109a** and **109b** as an etch mask. The first and second gate mask patterns **109a** and **109b** may be constituted by, for example, a silicon nitride layer. The etching of the sacrificial gate layer may be performed using an etching recipe having an etch selectivity with respect to the etch stop layer.

[0054] After the forming of the first and second sacrificial gate patterns **107a** and **107b**, the etch stop layer may be etched to form a first etch stop pattern **105a** below the first sacrificial gate pattern **107a** and a second etch stop pattern **105b** below the second sacrificial gate pattern **107b**. The first etch stop pattern **105a** may extend along a bottom surface of the first sacrificial gate pattern **107a** to partially cover the top surfaces of the first device isolation patterns **102**. The second etch stop pattern **105b** may extend along a bottom surface of the second sacrificial gate pattern **107b** to partially cover the top surfaces of the second device isolation patterns **104**.

[0055] Since the first sacrificial gate pattern **107a** is formed to cross the first active fin AF1, a first channel region CHR1 and first sacrificial regions SR1 may be defined in each of the first active fins AF1. The first channel region CHR1 may be a portion of the first active fin AF1 that is positioned below and overlapped by the first sacrificial gate pattern **107a**. The first sacrificial regions SR1 may be other portions of the first active fin AF1 that are positioned at both sides of the first sacrificial gate pattern **107a** and are horizontally separated from each other by the first channel region CHR1.

[0056] In addition, since the second sacrificial gate pattern **107b** is formed to cross the second active fin AF2, a second channel region CHR2 and second sacrificial regions SR2 may be defined in each of the second active fins AF2. The second channel region CHR2 may be a portion of the second active fin AF2 that is positioned below and overlapped by the second sacrificial gate pattern **107b**. The second sacrificial regions SR2 may be other portions of the second active fin AF2 that are positioned at both sides of the second sacrificial gate pattern **107b** and are horizontally separated from each other by the second channel region CHR2.

[0057] The first etch stop pattern **105a**, the first sacrificial gate pattern **107a**, and the first gate mask pattern **109a** may

constitute a first sacrificial gate structure SGS1, and the second etch stop pattern **105b**, the second sacrificial gate pattern **107b**, and the second gate mask pattern **109b** may constitute a second sacrificial gate structure SGS2.

[0058] In some examples, a plurality of first sacrificial gate structures SGS1 may be formed on the first region R1 of the substrate **100** to cross the first active pattern AP1, and a plurality of second sacrificial gate structures SGS2 may be formed on the second region R2 of the substrate **100** to cross the second active pattern AP2. A third distance d3 between adjacent ones of the first sacrificial gate structures SGS1 may be greater than a fourth distance d4 between adjacent ones of the second sacrificial gate structures SGS2. Accordingly, a length of the first active fin AF1 exposed by the adjacent ones of the first sacrificial gate structures SGS1 may be greater than a length of the second active fin AF2 exposed by the adjacent ones of the second sacrificial gate structures SGS2. Here, the length of the first active fin AF1 refers to the dimension of the exposed portion thereof in the longitudinal direction (e.g., the first direction D1) of the first active pattern AP1, and the length of each of the second sacrificial regions SR2 refers to the dimension of the exposed portion thereof in the longitudinal direction (e.g., the first direction D1) of the second active pattern AP2.

[0059] Referring to FIGS. 5A to 5C, a gate spacer layer and a spacer sacrificial layer may be formed on the substrate **100**. The gate spacer layer may be formed to conformally cover the first and second active patterns AP1 and AP2 and the first and second sacrificial gate structures SGS1 and SGS2. Subsequently, the spacer sacrificial layer may be conformally formed on the gate spacer layer. The gate spacer layer may include a silicon nitride layer, and the spacer sacrificial layer may include an oxide layer. The gate spacer layer and the spacer sacrificial layer may be formed by, for example, a chemical vapor deposition process.

[0060] The gate spacer layer and the spacer sacrificial layer may be patterned to form first and second spacer structures SP1 and SP2. For example, an anisotropic etching process may be performed to form the first and second spacer structures SP1 and SP2. The first spacer structure SP1 may include the first gate spacer **120** and a first sacrificial spacer **124**. The first gate spacer **120** and the first sacrificial spacer **124** may be formed on an outer side surface of the first sacrificial gate pattern **107a**. The second spacer structure SP2 may include the second gate spacer **122** and a second sacrificial spacer **126**. The second gate spacer **122** and the second sacrificial spacer **126** may be formed on an outer side surface of the second sacrificial gate pattern **107b**.

[0061] Referring to FIGS. 6A to 6C, a coating layer **170** may be formed on the substrate **100**. The coating layer **170** may be formed to conformally cover the first and second active patterns AP1 and AP2, the first and second sacrificial gate structures SGS1 and SGS2, and the first and second spacer structures SP1 and SP2. The coating layer **170** may include a silicon oxide layer. For example, the coating layer **170** may be a silicon oxide layer which may be deposited by a chemical reaction between silicon tetrachloride (SiCl₄) and oxygen (O₂). The coating layer **170** may be of the same material as the first and second sacrificial spacers **124** and **126**. In this case, the first and second sacrificial spacers **124** and **126** do not have to be formed thickly.

[0062] The coating layer **170** may be formed under a low pressure condition. For example, the coating layer **170** may be formed under a pressure condition of about 1 mTorr to

about 100 mTorr. Furthermore, in the case where a PECVD method is used to form the coating layer 170, the coating layer 170 may be formed under a bias power condition of about 100V or less. The coating layer 170 may be formed to have a first thickness w_1 on the first active pattern AP1 and first sacrificial region SR1 and a second thickness w_2 on the second active pattern AP2 and second sacrificial region SR2. The second thickness w_2 may be different from the first thickness w_1 . The second thickness w_2 may be smaller than the first thickness w_1 . In other words, in the case where the deposition process is performed under the process condition of low pressure and low power, a difference in geometry between topography on the first and second regions R1 and R2 may lead to a difference in thickness of the coating layer 170 (i.e., w_1 w_2). For example, the deposition process proceeds more easily or rapidly on the first region R1 than on the second region R2 because a distance between the first sacrificial gate structures SGS1 on the first region R1 is greater than that between the second sacrificial gate structures SGS2 on the second region R2. This may lead to a difference in thicknesses of the coating layer 170 between the first and second regions R1 and R2 (i.e., w_1 w_2). In addition, the coating layer 170 may be formed to have a relatively large thickness on the first and second sacrificial gate structures SGS1 and SGS2. As an example, the thickness of the coating layer 170 on the first and second sacrificial gate structures SGS1 and SGS2 may be larger than the second thickness w_2 .

[0063] Referring to FIGS. 7A to 7C, after the forming of the coating layer 170, a recess process may be performed to form first and second recess regions RR1 and RR2. The first recess region RR1 may be formed in the first active pattern AP1 between the first sacrificial gate structures SGS1. For example, the recess process may be performed to remove the first sacrificial regions SR1 of the first active fin AF1. The removal of the first sacrificial regions SR1 may be performed using a dry or wet etching process. The first recess region RR1 may define a recess of a predetermined depth D. The second recess region RR2 may be formed in the second active pattern AP2 between the second sacrificial gate structures SGS2. For example, the recess process may be performed to remove the second sacrificial regions SR2 of the second active fin AF2. The removal of the second sacrificial regions SR2 may be performed using a dry or wet etching process. The second recess region RR2 may also define a recess of the predetermined depth D. In some examples, the removal of the first and second sacrificial regions SR1 and SR2 may include etching the first and second sacrificial regions SR1 and SR2 using an etching process formulated to have a relatively high etch selectivity with respect to the gate spacer layer. Here, the upper portions of the first and second sacrificial regions SR1 and SR2 in contact with the first and second spacers 120 and 122 may be recessed along the bottom surfaces of the first and second spacers 120 and 122. As an example, the upper portions of the first and second sacrificial regions SR1 and SR2 in contact with the first and second spacers 120 and 122 may be rounded in a direction toward the first and second channel regions CHR1 and CHR2.

[0064] In the hypothetical case in which the recess process were to be performed on both of the first and second sacrificial regions SR1 and SR2 without the coating layer 170, the depth of the recess formed by etching the first sacrificial region SR1 would be greater than the depth of the

recess formed by etching the second sacrificial region SR2, because the exposed area of the first sacrificial region SR1 would be relatively large. However, according to some examples of the inventive concept, the coating layer 170 is formed to different thicknesses (i.e., w_1 and w_2) on the first and second regions R1 and R2, before the recess process is performed on the first and second sacrificial regions SR1 and SR2. This makes it possible to minimize or eliminate a difference depth of the recesses formed by etching the first and second sacrificial regions SR1 and SR2. In certain examples, the recess formed by etching the first sacrificial region SR1 may be shallower than that formed by etching the second sacrificial region SR2.

[0065] The process of forming the first and second recess regions RR1 and RR2 may include repeatedly performing a cycle including steps of coating and etching a layer. For example, a first cycle including steps of coating and etching a layer may be firstly performed, and then, a second cycle including steps of coating and etching a layer may be secondly performed. The cycle including steps of coating and etching a layer may be performed in an in-situ manner, and this may make it possible to change a process condition during the overall course of the process, without temporal and spatial limitations.

[0066] During the recess process, the first and second spacer structures SP1 and SP2 may be partially etched. As an example, side portions of the first and second spacer structures SP1 and SP2 may be etched during the recess process. Here, since the coating layer 170 is formed to be thicker on the first region R1 than on the second region R2, the amount of the first spacer structure SP1 removed by the etching process may be smaller than that of the second spacer structure SP2 removed by the etching process. Accordingly, in the case where the first and second sacrificial spacers 124 and 126 are removed through a cleaning process after the recess process, the amount of the first gate spacer 120 remaining after the cleaning process may be greater than that of the second gate spacer 122. In some examples, the cleaning process for removing the first and second sacrificial spacers 124 and 126 may be performed using hydrofluoric acid (HF).

[0067] Referring back to FIGS. 2A and 2B, the first protrusion 120b outwardly protruding from the first sacrificial gate pattern 107a may be formed at a lower portion of the first gate spacer 120. For example, the first protrusion 120b may be a lower portion of the first gate spacer 120 protruding in the first direction D1 with respect to the first portion 120a. The first protrusion 120b may protrude from the first portion 120a by the first length L1. The second protrusion 122b outwardly protruding from the second sacrificial gate pattern 107b may be formed at a lower portion of the second gate spacer 122. For example, the second protrusions 122b may be a lower portion of the second gate spacer 122 protruding in the first direction D1 with respect to the second portion 122a. The second protrusions 122b may protrude from the second portion 122a by the second length L2. Here, the second length L2 may be smaller than the first length L1. As an example, the second length L2 may be about 5Å to about 2nm smaller than the first length L1. For example, by controlling etching amounts of the first and second gate spacers 120 and 122, it is possible to make a difference in length between the first and second protrusions 120b and 122b. In certain examples, during the recess process, lower side portions of the first and second protrusions

sions **120b** and **122b** may be recessed toward the first and second sacrificial gate patterns **107a** and **107b**.

[0068] Furthermore, according to some examples of the inventive concept, the coating layer **170** may protect the first and second gate mask patterns **109a** and **109b** and the first and second gate spacer layers **120** and **122** from being etched. Otherwise, the first and second gate mask patterns **109a** and **109b** and the first and second gate spacer layers **120** and **122** could be partially removed during the anisotropic etching process for forming the recess regions RR1 and RR2.

[0069] Referring to FIGS. **8A** to **8C**, the first source/drain regions SD1 may be formed at both sides of the first sacrificial gate structure SGS1, and the second source/drain regions SD2 may be formed at both sides of the second sacrificial gate structure SGS2. The first and second source/drain regions SD1 and SD2 may be formed using the same process.

[0070] The forming of the first and second source/drain regions SD1 and SD2 may include performing a selective epitaxial growth process on the substrate **100**. For example, each of the first source/drain regions SD1 may be an epitaxial pattern grown using the first active pattern AP1 as a seed layer, and each of the second source/drain regions SD2 may be an epitaxial pattern grown using the second active pattern AP2 as a seed layer. The first and second source/drain regions SD1 and SD2 may include at least one of silicon germanium (SiGe), silicon (Si), and silicon carbide (SiC). In the case where the semiconductor device is a CMOS type of device, a first epitaxial layer may be formed to serve as source/drain electrodes of NMOSFETs, and a second epitaxial layer may be formed to serve as source/drain electrodes of PMOSFETs. The first epitaxial layer may be formed of a material capable of exerting a tensile stress on channel regions of the NMOSFETs, and the second epitaxial layer may be formed of a material capable of exerting a compressive stress on channel regions of the PMOSFETs. The first and second epitaxial layers may be formed of silicon carbide (SiC) and silicon germanium (SiGe), respectively, but the inventive concept may not be limited thereto. During or after the epitaxial process, the first and second source/drain regions SD1 and SD2 may be doped with impurities. Although not shown, each of the first and second source/drain regions SD1 and SD2 may include a plurality of epitaxial layers. As an example, each of the first and second source/drain regions SD1 and SD2 may include a first epitaxial layer (not shown), which serves as a buffer layer in contact with the first and second active patterns AP1 and AP2 and is formed of a lightly doped semiconductor material, a second epitaxial layer (not shown), which extends from the first epitaxial layer and is formed of a highly-doped semiconductor material, and a third epitaxial layer (not shown), which is provided on the second epitaxial layer (not shown) to serve as a capping layer.

[0071] Referring to FIGS. **9A** to **9C**, the lower interlayer insulating layer **130** may be formed on the substrate **100** provided with the first and second source/drain regions SD1 and SD2. The lower interlayer insulating layer **130** may be formed to cover the first and second source/drain regions SD1 and SD2 and the first and second sacrificial gate structures SGS1 and SGS2. The lower interlayer insulating layer **130** may be formed of or include at least one of a

silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, and a low-k dielectric layer.

[0072] The lower interlayer insulating layer **130** may be etched to expose the top surface of each of the first and second sacrificial gate patterns **107a** and **107b**. The etching process on the lower interlayer insulating layer **130** may be performed to remove the first and second gate mask patterns **109a** and **109b**. Subsequently, the first and second sacrificial gate patterns **107a** and **107b** may be removed. Accordingly, a first gap **160** may be formed between the first gate spacers **120** to expose the first channel region CHR1 of the first active fin AF1, and a second gap **162** may be formed between the second gate spacers **122** to expose the second channel region CHR2 of the second active fin AF2. The forming of the first and second gaps **160** and **162** may include performing an etching process having an etch selectivity with respect to the first and second gate spacers **120** and **122**, the lower interlayer insulating layer **130**, and the first and second etch stop patterns **105a** and **105b** to etch the first and second sacrificial gate patterns **107a** and **107b**. In addition, the forming of the first gap **160** may include removing the first etch stop pattern **105a** to expose the first channel region CHR1 of the first active fin AF1, and the forming of the second gap **162** may include removing the second etch stop pattern **105b** to expose the second channel region CHR2 of the second active fin AF2.

[0073] Referring back to FIGS. **1A** to **1C**, the first gate dielectric pattern **140** and the first gate electrode **150** may be formed to fill the first gap **160**. Also, the second gate dielectric pattern **142** and the second gate electrode **152** may be formed to fill the second gap **162**.

[0074] In some examples, a gate dielectric layer (not shown) may be formed on the substrate **100** to partially fill each of the first and second gaps **160** and **162**. The gate dielectric layer may be formed to cover the first and second channel regions CHR1 and CHR2. The gate dielectric layer may include at least one high-k dielectric layer. For example, the gate dielectric layer may be formed of or include at least one of hafnium oxide, hafnium silicate, zirconium oxide, and zirconium silicate, but the inventive concept may not be limited thereto. In addition, the gate dielectric layer may be formed by, for example, an atomic layer deposition process. A gate layer (not shown) may be formed on the gate dielectric layer to fill the remaining space of each of the first and second gaps **160** and **162**. The gate layer may be formed of or include at least one material selected from the group consisting of conductive metal nitrides (e.g., titanium nitride or tantalum nitride) and metals (e.g., aluminum or tungsten).

[0075] A planarization process may be performed on the gate dielectric layer and the gate layer, which are sequentially stacked on the substrate **100**, and thus, the first gate dielectric pattern **140**, the second gate dielectric pattern **142**, the first gate electrode **150**, and the second gate electrode **152** may be formed. For example, the planarization process may be performed to expose the top surface of the lower interlayer insulating layer **130** and the top surface of each of the first and second gate spacers **120** and **122**. Each of the first and second gate dielectric patterns **140** and **142** may extend along the bottom surface of each of the first and second gate electrodes **150** and **152**. The first gate dielectric pattern **140** may be formed on both side surfaces of the first gate electrode **150** and may be interposed between the first gate electrode **150** and the first gate spacer **120**. The second

gate dielectric pattern **142** may be formed on both side surfaces of the second gate electrode **152** and may be interposed between the second gate electrode **152** and the second gate spacer **122**.

[0076] The first channel region **CHR1** of the first active fin **AF1** disposed below the first gate electrode **150** may be interposed between the first source/drain regions **SD1**, and the second channel region **CHR2** of the second active fin **AF2** disposed below the second gate electrode **152** may be interposed between the second source/drain regions **SD2**. The first gate dielectric pattern **140**, the first gate electrode **150**, and the first gate spacer **120** may constitute the first gate structure **GS1**, and the second gate dielectric pattern **142**, the second gate electrode **152**, and the second gate spacer **122** may constitute the second gate structure **GS2**.

[0077] Although not shown, the upper interlayer insulating layer may be formed on the substrate **100** provided with the first and second gate structures **GS1** and **GS2**. The first contact hole and the second contact hole may be formed to penetrate the upper interlayer insulating layer and the lower interlayer insulating layer **130** and thereby to expose the first and second source/drain regions **SD1** and **SD2**, respectively, and the contact plugs may be formed to fill the first and second contact holes. The interconnection lines may be provided on the upper interlayer insulating layer and may be connected to at least one of the contact plugs. The interconnection lines may be connected to the first and second source/drain regions **SD1** and **SD2** through the contact plugs.

[0078] FIGS. **10A** and **10B** are sectional views illustrating a semiconductor device according to some examples of the inventive concept. For example, FIG. **10A** illustrates vertical sections taken along lines A-A', B-B', and C-C' of FIG. **1A**, and FIG. **10B** illustrate vertical sections taken along lines D-D', E-E', and F-F' of FIG. **1A**. In the following description, an element previously described with reference to FIGS. **1A** to **1C**, **2A**, and **2B** may be identified by a similar or identical reference number without repeating an overlapping description thereof, for the sake of brevity.

[0079] Referring to FIGS. **10A** and **10B**, each of the first and second active patterns **AP1** and **AP2** may be provided to have a structure upwardly protruding from the substrate **100**. For example, each of the first and second active patterns **AP1** and **AP2** may protrude in the third direction **D3** that is orthogonal to both of the first and second directions **D1** and **D2**. Here, each of the first and second active patterns **AP1** and **AP2** may have a width decreasing in a direction (the third direction **D3**) away from the substrate **100**.

[0080] Each of the first device isolation patterns **102** may cover a portion of the side surface of the first active pattern **AP1**, and the upper portion of the first active pattern **AP1** exposed by the first device isolation patterns **102** may be used as the first active fin **AF1**. Here, the first active fin **AF1** may include a first portion **P1** and a second portion **P2**. The first portion **P1** of the first active fin **AF1** may have side surface inclined inwardly in a direction away from the first active pattern **AP1**. The second portion **P2** of the first active fin **AF1** may be a protrusion extending upwardly from a top of the first portion **P1** and having a side surface inclined inwardly also in a direction away from the first active pattern **AP1** but to a different degree than the side surface of first portion **P1**. That is, in some examples, the first active fin **AF1** may be provided in such a way that the side surfaces of the first and second portions **P1** and **P2** have slopes different

from each other. In the illustrated example, the slope of the side of the first portion **P1** is greater than that of the side surface of the second portion **P2**. Features such as the widths, heights, and slopes of the side surfaces of the first and second portions **P1** and **P2** of the first active fin **AF1** may be established to specifications by implementing process conditions selected to produce the desired features.

[0081] Similarly, each of the second device isolation patterns **104** may cover a portion of the side surface of the second active pattern **AP2** and the upper portion of the second active pattern **AP2** exposed by the second device isolation patterns **104** may be used as the second active fin **AF2**. Here, the second active fin **AF2** may include a first portion **P1'** and a second portion **P2'**. The first portion **P1'** of the second active fin **AF2** may have a side surface inclined inwardly in a direction away from the second active pattern **AP2**. The second portion **P2'** of the second active fin **AF2** may be a protrusion upwardly extending from a top of the first portion **P1'** of the second active fin **AF2** and having a side surface inclined inwardly in the direction away from the second active pattern **AP2**. In some examples, the second active fin **AF2** may be provided in such a way that the side surfaces of the first and second portions **P1'** and **P2'** have slopes different from each other. Widths, heights, and angles of the first and second portions **P1'** and **P2'** of the second active fin **AF2** may be designed to specifications by implementing appropriate process conditions.

[0082] According to some examples of the inventive concept, the first gate structures **GS1** may be formed on the first region **R1** at a relatively large pitch or spacing (e.g., the first distance **d1**), and the second gate structures **GS2** may be formed on the second region **R2** at a relatively small pitch or spacing (e.g., the second distance **d2**). The coating layer **170** may be formed to different thicknesses (e.g., **w1** and **w2**) on the first and second regions **R1** and **R2**, and then, a recess process may be performed on the structure provided with the coating layer **170**. This may make it possible to control depths of recesses that are formed by the recess process. For example, it is possible to prevent a loading effect and consequently to mitigate several technical problems (e.g., differences in epitaxial growth rate, reduction in process margin of a contact forming process, or increase in resistance) which would otherwise be created in a subsequent process due to the loading effect. In addition, it is possible to control an amount of a recessed material. Since a hard mask pattern is protected by the coating layer **170**, it is possible to improve mask selectivity. The coating layer **170** may prevent the first and second spacer structures **SP1** and **SP2** from being etched or removed. The processes of depositing and etching the coating layer may be easily performed in an in-situ manner.

[0083] So far, the first and second gate structures **150** and **152** have been described as an example of spaced apart features to which the inventive concept is applied, but the inventive concept is not limited thereto. That is, the inventive concept may be applied to methods in which other features formed a substrate such as series of openings having different aspect ratios or series of protrusions having a difference in terms of their width and height. Also, each of the first and second gate spacers has been described as a single-layer structure, but the first and second gate spacers may be multi-layered structures. The distance between the gate structures on the first region has been described to be greater than that on the second region. Here, the first region

may include an input/output semiconductor device, and the second region may include a logic device. Furthermore, to reduce complexity in the drawings, the first and second gate structures have been illustrated to have the same width and the same height, but the first and second gate structures may have different widths and heights.

[0084] Finally, although examples of the inventive concepts have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made to these examples without departing from the spirit and scope of the attached claims.

1. A method of fabricating a semiconductor device, comprising:

providing a substrate having a first region and a second region;

forming first and second active patterns at the first and second regions, respectively, of the substrate;

forming first gate structures across the first active pattern as spaced apart from each other by a first distance along the first active pattern, and

forming second gate structures across the second active pattern as spaced apart from each other by a second distance along the second active pattern;

forming a coating layer to cover the first and second gate structures and the first and second active patterns;

performing a recess process to form a first recess in the first active pattern between the first gate structures and a second recess in the second active pattern between the second gate structures; and

forming a source/drain epitaxial layer in the first and second recesses,

wherein the coating layer is formed to a first thickness on a region of the first active pattern between the first gate structures and to a second thickness different from the first thickness on a region of the second active pattern between the second gate structures.

2. The method of claim 1, wherein the first distance is greater than the second distance and the first thickness is thicker than the second thickness.

3. The method of claim 1, wherein the coating layer comprises a silicon compound.

4. The method of claim 3, wherein the forming of the coating layer is performed under a pressure ranging from about 1 mTorr to about 100 mTorr.

5. The method of claim 1, wherein the forming of the coating layer and the recess process are alternately repeated.

6. The method of claim 1, wherein the first recess and the second recess are formed to substantially the same depth.

7. The method of claim 1, wherein the forming of the first and second gate structures comprises:

forming first sacrificial gate patterns crossing the first active pattern and second sacrificial gate patterns crossing the second active pattern; and

forming a first spacer structure on side surfaces of the first sacrificial gate pattern and a second spacer structure on side surfaces of the second sacrificial gate pattern,

wherein the forming of the first and second spacer structures comprises:

forming a gate spacer layer on outer side surfaces of the first and second sacrificial gate patterns; and

forming a spacer sacrificial layer on the gate spacer layer.

8. The method of claim 7, wherein the gate spacer layer comprises a nitride and the spacer sacrificial layer comprises an oxide.

9. The method of claim 7, further comprising removing the spacer sacrificial layer, after the first and second recesses have been formed.

10. The method of claim 7, wherein the forming of the first and second gate structures further comprises forming a hard mask layer on the first and second sacrificial gate patterns, before the spacer structure has been formed.

11. The method of claim 1, wherein the forming of the source/drain epitaxial layer comprises performing an epitaxial process, in which the first and second active patterns exposed by the first and second recess are used as a seed layer, to form the source/drain epitaxial layer.

12. The method of claim 1, wherein the first region comprises a logic semiconductor device, and the second region comprises an input/output semiconductor device.

13-17. (canceled)

18. A patterning method, comprising:

forming first and second patterns on first and second regions, respectively, of a substrate,

wherein the first and second patterns have first and second aspect ratios different from each other, and

the forming of the first and second patterns comprises:

forming a coating to first and second thicknesses on the first and second regions, respectively; and

performing a recessing process to form first and second recesses to substantially the same depths in the first and second regions, respectively.

19. The method of claim 18, wherein the first aspect ratio is greater than the second aspect ratio and the first thickness is thicker than the second thickness.

20-24. (canceled)

25. A method of manufacturing a semiconductor device having first and second regions disposed beside one another so as to not overlap, the method comprising:

forming, at an upper surface of a substrate, a series of first features as spaced from each other along a first direction in the first region of the device, and

forming, at the upper surface of the substrate, a series of second features as spaced from each other along a second direction in the second region of the device,

wherein the spacing between adjacent ones of the first features in the first direction is greater than the spacing between adjacent ones of the second features in the second direction;

subsequently forming, on the upper surface of the substrate, a coating covering the first and second regions of the device, wherein the thickness of the coating in the first region of the device at a location between the adjacent ones of the first features is greater than the thickness of the coating in the second region of the device at a locations between the adjacent ones of the second features; and

performing an etching process that etches through the coating at respective locations in the first and second regions of the device and forms a first recess in the substrate in the first region of the device and a second recess in the substrate in the second region of the device.

26. The method as claimed in claim 25, wherein the first and second directions coincide.

27. The method as claimed in claim 25, further comprising epitaxially growing layers in the first and second recesses.

28. The method of claim **25**, wherein the first recess and the second recess are formed to substantially the same depth relative to the upper surface of the substrate.

29. The method of claim **25**, wherein the forming of the coating and the etching process comprise performing several cycles of depositing material on the upper surface the substrate followed by an etch process.

30. The method of claim **25** wherein the features comprise gates protruding from the upper surface of the substrate, and the coating is formed over top and side surfaces of the gates such that the coating protects the gates as the recesses are formed in the substrate.

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