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(54) **METHOD FOR MAKING CONTACT WITH A COMPONENT EMBEDDED IN A PRINTED CIRCUIT BOARD**

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(57) **ABSTRACT**

The invention pertains to a method for the bonding of a component embedded into a printed circuit board exhibiting the following steps:

Provision of a core exhibiting at least one insulating layer and at least one conductor layer applied to the insulating layer,

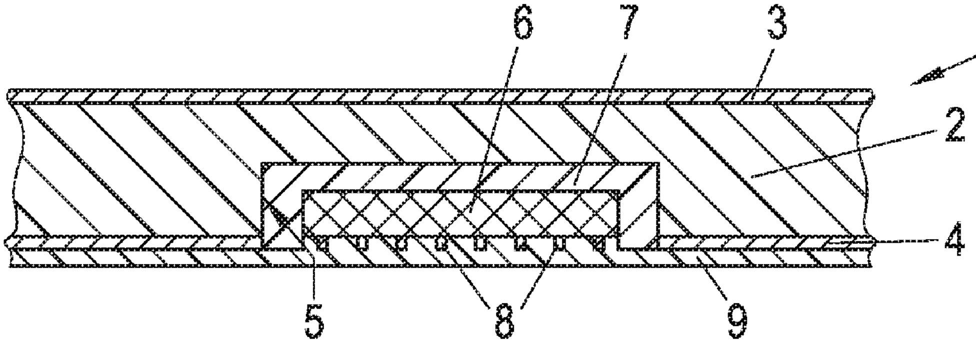
Embedding of at least one component into a recess of the insulating layer, wherein the contacts of the component are essentially situated in the plane of an outer surface of the core exhibiting the at least one conductor layer,

Application of a photoimageable resist onto the one outer surface of the core on which the component is arranged, while filling the spaces between the contacts of the component,

Clearing of end faces of the contacts and of the areas of the conductor layer covered by the photoimageable resist by exposing and developing the photoimageable resist,

by application of a semi-additive process, deposition of a layer of conductor material onto the cleared end faces of the contacts and the cleared areas of the conductor layer and formation of a conductor pattern on at least the one outer surface of the core on which the component is arranged, as well as the interconnecting paths between the contacts and the conductor pattern, and

Removal of the areas of the conductor layer not belonging to the conductor pattern.



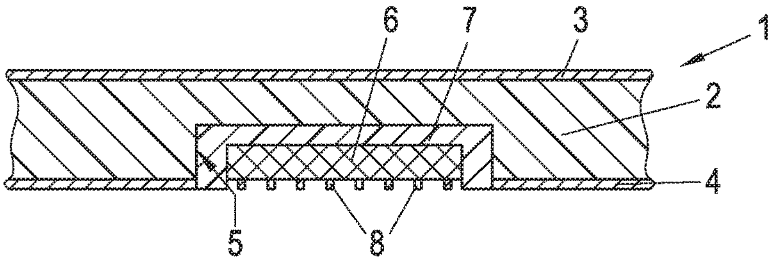


Fig. 1

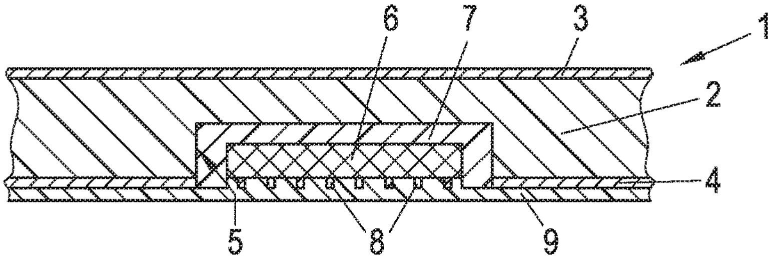


Fig. 2

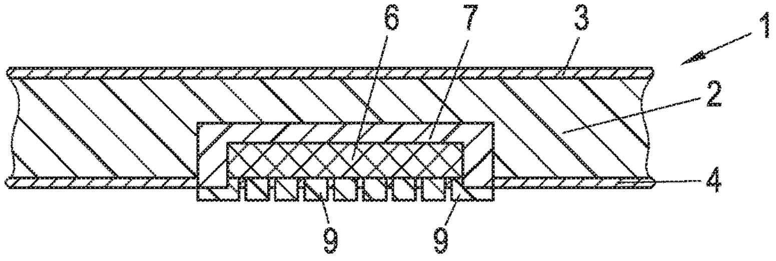


Fig. 3

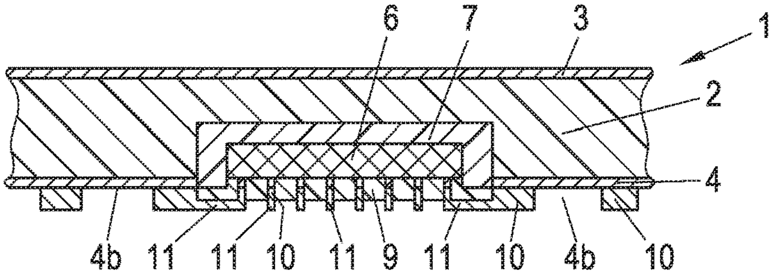


Fig. 4

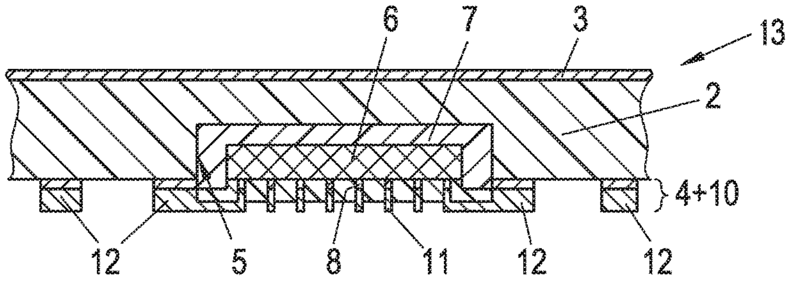


Fig. 5

METHOD FOR MAKING CONTACT WITH A COMPONENT EMBEDDED IN A PRINTED CIRCUIT BOARD

[0001] This application is a continuation in part of U.S. patent application Ser. No. 15/122,114, filed Aug. 26, 2016, which is a U.S. national stage of PCT Application No. PCT/AT2015/050052, filed Feb. 2, 2015, which claims priority to Austrian Application No. A50152/2014, filed Feb. 27, 2014, the disclosures of which are incorporated by reference herein in their entirety.

[0002] The invention pertains to a method for the bonding of a component embedded in a printed circuit board.

[0003] The invention furthermore pertains to a printed circuit board with at least one insulated layer and at least one structured conductor layer with conductor paths, with at least one component, which, by means of an adhesive layer, is embedded into a recess of the printed circuit board, with its contacts essentially being situated in the plane of an outer surface of the printed circuit board exhibiting the at least one conductor layer, and with conductive connections between the contacts of the components and the conductor paths of the conductor layer.

[0004] The embedding of components, in particular of semiconductor chips, in printed circuit board structures is familiar to the professional, wherein within the scope of the invention, structures are contemplated in which the contacts of the component are essentially situated within one plane at the outer surface of the printed circuit board, also called "surface embedded components". The electrical contacts of the component must be bonded with a conductor pattern, for which various methods have been applied.

[0005] DE 10 2006 009 723 A1, for example, describes a method of embedding a component in a circuit board and of its contacts, in which a first insulating layer with a conductor pattern is applied to a metallic substrate. This is followed by the creation of a window or cut-out for the chip in the first layer, into which the chip—while leaving a gap—is inserted and, using an adhesive, is fixated to the substrate. In doing so, the contacts of the chip are situated on a bonding side facing away from the substrate. Applied on top of this configuration is a photoimageable second insulating layer, which leaves the contact points of the chip cleared, followed by electrical bonding by means of galvanic deposition of a conductor material between the contacts of the chip and the conductor pattern on the first layer. The known method and the resulting product have the disadvantage that in the spacing area between the chip and the adjacent layers a cavity remains, which during the buildup of additional layers may lead to delamination issues.

[0006] One objective of this invention is to establish a method with the use of which a conductor pattern in the plane of the contacts, including the respective bondings, can be produced easily and cost-efficiently without the risk of detaching layers.

[0007] This objective is achieved with a method of the type referred to above, which according to the invention exhibits the following steps:

[0008] a) Provision of a core exhibiting at least one insulating layer and at least one conductor layer applied to the insulating layer,

[0009] b) Embedding of at least one component into a recess of the insulating layer, wherein the contacts of the component are essentially situated within the plane of an outer surface of the printed circuit board exhibiting the at least one conductor layer,

[0010] c) Application of a photoimageable lacquer on the one outer surface of the core on which the component is arranged while filling the spaces between the contacts of the component,

[0011] d) Clearing of end faces of the contacts and of the regions covered by the photoimageable lacquer of the conductor layer by means of exposing and developing the photoimageable lacquer,

[0012] e) using a semi-additive process, deposition of conductor material onto the cleared end faces of the contacts and the cleared regions of the conductor layer and forming of a conductor pattern at least on the one outer surface of the core on which the component is arranged, was well as the interconnecting paths between the contacts and the conductor pattern, and

[0013] f) Removal of the sections of the conductor layer not belonging to the conductor pattern.

[0014] Thanks to the invention, embedded components can be "wired" in the same position or plane as the embedding, such that the printed circuit boards can be designed to be thinner and the aforementioned problems of the risk of detachment do not arise.

[0015] In doing so, it is recommended for the removal of the sections of the conductor layer in step f) is carried out by flash-etching.

[0016] Regarding the additional function of the photoimageable lacquer as a part of the finished printed circuit board, it is advantageous for the photoimageable lacquer used in step c) to be epoxy-based lacquer.

[0017] In a particularly advantageous variation of the method according to the invention it may be provided that in step b) the component is embedded into an recess of the core using an adhesive layer, wherein the adhesive layer fully envelops all surfaces of the component—with the exception of those with the contacts—and essentially extends to the plane of the surface of the printed circuit board in which the end faces of the contacts are situated.

[0018] In a particularly expedient manner, the recess of the core extends through the conductor layer into the insulating layer.

[0019] The stated objectives will also be achieved with a printed circuit board of the above stated type, in which according to the present invention the connections and the conductor paths of the conductor layer are situated in one plane, where the adhesive layer completely envelops all surfaces of the component, except those with the contacts, where the spaces between the contacts of the component are filled with a cured, photoimageable lacquer, and an additional conductor layer is applied to the end faces of the contacts as well as to a conductor layer of the printed circuit board in the area of the conductor paths.

[0020] In a preferred embodiment, it is provided that the cured, photoimageable lacquer covers the cleared end faces of the adhesive layer between the outer wall of the component and the inner wall of the recess of the printed circuit board.

[0021] In one advanced embodiment of the invention, the printed circuit board again comprises a core exhibiting at least one insulating layer and at least one conductor layer having been applied to the insulating layer, wherein one outer surface of the core having been provided with at least one conductor layer exhibits a recess which extends through the conductor layer into the insulating layer, whereby the component is embedded into the recess of the core by means of an adhesive layer, and wherein the contacts of the component are essentially situated in the plane of the outer surface exhibiting the at least one conductor layer and the recess.

[0022] The invention and its further advantages is described in greater detail below based on a sample embodiment of the method and the circuit board, which is illustrated in the drawing. In this drawing show

[0023] FIG. **1** in a section through a partial section a core made in the first steps of the method with an embedded component,

[0024] FIG. **2** the structure of FIG. **1** after application of a photoimageable lacquer,

[0025] FIG. **3** the structure after exposure and development of the photoimageable lacquer,

[0026] FIG. **4** the structure after deposition of additional conductive material by application of a semi-additive process and

[0027] FIG. **5** the structure of the finished printed circuit board after part of the conductive coatings have been etched away.

[0028] The method according to the invention and the inventive printed circuit board will now be explained in reference to the figures. Therein, the term “core” used in the following in the context of the representational description shall be understood to mean a cured prepreg with a conductor layer (copper layer) on at least one surface.

[0029] FIG. **1** shows a section of a core **1** consisting of an insulating layer **2**, for example consisting of a prepreg material commonly used in the printed circuit board industry, like FR 4, and an upper conductor layer **3** as well as a lower conductor layer **4**. At this point it shall be noted that the terms “upper” and “lower” refer to the representation in the drawings only, and are being used for an easier description. Layer thicknesses, for example, are 100 microns for the insulating layer **2** and 1 to 5 microns, typically 2 microns, for upper and lower conductor layer **3** and **4** respectively.

[0030] In the core **1**, a recess **5** is formed, into which—using an adhesive layer **7**—a component **6** is embedded, whereby the layer thickness of this adhesive layer, for example, is 20 to 200 microns. The component **6**, a semiconductor chip, for example, carries on an outer surface contacts **8**, e.g. copper pads, whereby the adhesive layer **7** envelops all surfaces of the component **6** with the exception of those with the contacts **8**, and essentially extends to the plane of the surface of the core **1**, in which the end faces of the contacts **8** are situated, in this case, therefore the bottom surface. One possible adhesive, for example, is a solvent-free or low-solvent epoxy resin adhesive with a glass softening point of typically between 120° and 150° C., which will be pressed, filled or injected into the recess **5**. After placement of the component **6**, this adhesive will be hardened at temperatures of 110° to 150° C.

[0031] In a next step, an epoxy-based photoimageable resist **9** is applied at least to the outer surface of the core **1** with the end faces of the contacts **8**, with reference being made to FIG. **2**. Examples of products and materials suitable for this purpose are the XB7081 lacquer with the trade name Probelec® of the Huntsman Co. or the photoresist SU-8 from Microchem® Corp known from lithographic galvanoplasty (LIGA). As can be seen, the resist **9** is filling all spaces between the contacts **8** of the component **6**, and also extends across the lower conductor layer **4**.

[0032] Thereafter, a photolithographic process commonly used in printed circuit board manufacturing can be used to create the pattern (structuring), starting with exposure using film masking or LDI (Laser Direct Imaging). This is followed by development, obtainment of the patterns after washing-off with suitable chemicals, and the complete curing of the material. Curing is performed by means of conventional curing methods like thermal curing, UV- or IR-curing, application of laser radiation etc. The structuring and the exposure is performed in such manner that the contacts **8**, more specifically their end faces, will be cleared, for which purpose reference is made to FIG. **3**. This structuring/imaging process is performed such that the cured, photoimageable resist **9** covers the clear end faces of the adhesive layer **7** between the outer wall of the component **6** and the inner wall of the recess **5** of the core **1**, and that the lower conductor layer **4** is cleared again.

[0033] After this exposure and development, a semi-additive process for applying conductor material, among others, copper is applied according to the desired pattern. In doing so, a layer **10** of conductor material is applied in the desired areas, in particular for conductor paths, which is deposited also under formation of interconnecting paths **11** starting at the end faces **8** to the desired conductor pattern. The lower conductor layer **4**, on the other hand, is amplified in the area of the desired conductor paths or conductor pattern. This result is shown in FIG. **4**.

[0034] Since bridges **4***b* continue to exist between the thickened sections of the lower conductor layer **4** through layer **10**, which are to form the conductor paths, these bridges **4***b* and any other undesirable conductor material is removed in an additional step. This is preferably done using so-called “flash etching”, meaning the etching-off of the base copper foil and low-grade removal of the galvanically deposited copper layers. This etching process is performed, for example, with an acidic medium, e.g. HCl with the addition of H_2O_2 and of stabilizers, wherein the small crystallites of the base film are dissolved significantly faster than the electro-deposited layers, and selective etching is achieved. After this process of removing and etching, the surfaces and spaces between the contacts **9** are cleaned as well and the final conductor paths **12** have emerged and are completely formed, as referenced in FIG. **5**, which shows the finished printed circuit board **13** with the embedded and bonded component **6**.

[0035] In the example shown, only the structuring of the lower conductor layer **4** is described, but it should be clear that the upper conductor layer **3** may also be patterned in the same way. Also possible is the formation of vias (conductive feed-throughs) between the two conductor layers, just as additional insulating and conductor layers may be formed.

[0036] Finally, it should be understood that the representations in FIGS. **1** to **5** generally only show detail sections of a larger printed circuit board pattern, and that in practice, a plurality of components may be embedded and connected to conductor patterns at different locations on a printed circuit board.

What is claimed is:

1. A method of bonding of a component embedded into a printed circuit board, characterized by the following steps:

providing a core exhibiting at least one of at least one insulating layer and at least one conductive layer applied to the insulating layer and defining an outer layer of the core,

embedding at least one component into a recess of the insulating layer, the at least one component having a plurality of contacts separated by a plurality of spaces, each of the plurality of contacts having an end face distal from the at least one component,

depositing a layer of conductive material onto the end faces of the contacts and the conductive layer, and forming a conductor pattern on at least one outer surface of the core, and a plurality of interconnecting paths between the plurality of contacts and the conductor pattern.

2. The method according to claim **1**, wherein the plurality of contacts are configured to be positioned substantially perpendicular to a plane formed by the at least one outer surface of the core.

3. The method according to claim **1**, comprising the further steps of:

applying a resist onto the one outer surface of the core and/or the component such that the spaces between each of the plurality of contacts of the component are filled by the resist.

4. The method according to claim **3**, comprising the further step of:

clearing the resist from the end faces of the contacts and the conductive layer by exposing and developing the resist, wherein the layer of conductive material is deposited onto the cleared end faces of the contacts and the conductive layer.

5. The method according to claim **1**, wherein

the end face of each of the contacts is on a retracted position with respect to an outer surface of the component.

6. The method according to claim **1**, wherein

the conductor pattern and the plurality of interconnecting paths are formed by one of a subtractive process, an additive process and a semi-additive process.

7. The method according to claim **1**, further comprising a step of:

adding at least one further conductive layer onto the layer of conductive material.

8. The method according to claim **1**, comprising a step of removing portions of the conductive layer not incorporated into the conductor pattern.

9. The method according to claim **8**, wherein the removal of the areas of the conductive layer occurs by flash-etching.

10. The method according to claim **3**, wherein the applied resist comprises at least one of a photoimageable resist, an epoxy-based lacquer, a photoimageable resist, and polyimide.

11. The method according to claim **1**, wherein the embedding of the at least one component further comprises applying an adhesive layer into the recess of the core such that the adhesive layer fully encloses all surfaces of the component, except for the surface of the component from which the plurality of contacts extend, the adhesive layer extending substantially to the plane of the core.

12. The method according to claim **11**, wherein the recess of the core extends through the conductive layer into the insulating layer.

13. The method according to claim **11**, wherein

the adhesive layer comprises at least one of a solvent-free adhesive, a low-solvent adhesive and a prepreg adhesive.

14. The method according to claim **3**, wherein the resists covers a part of the component and a part of the at least one conductive layer.

15. The method according to claim **1**, wherein the contacts of the component are essentially situated in the plane of the at least one outer surface of the core exhibiting the at least one conductive layer.

16. The method according to claim **1**, wherein the recess is a through hole passing the core, wherein the embedding of the at least one component into the recess of the insulating layer is made by the following steps:

applying a temporary carrier onto the core below the recess,

placing the component into the recess and attaching the component to the temporary carrier so that the contacts of the component are located on that side of the component which is attached to the temporary carrier,

applying a first connecting layer onto the core on a side of the core opposite to the temporary carrier, wherein the first connecting layer enters the recess to adhere the at least one component in the recess, and

removing the temporary carrier from the core.

17. The method according to claim **16**, further comprising a step of:

applying a second connecting layer onto the core on a side of the core opposite to the first connecting layer.

18. The method according to claim **16**, wherein first connecting layer is a prepreg layer which is laminated onto the core.

19. A method of bonding of a component embedded into a printed circuit board, characterized by the following steps:

providing a core exhibiting at least one insulating layer,

embedding at least one component into a recess of the insulating layer, the at least one component having a plurality of contacts separated by a plurality of spaces, each of the plurality of contacts having an end face distal from the at least one component,

sputtering a conductive layer onto the insulating layer, the conductive layer defining an outer layer of the core, and

depositing at least one layer of conductive material onto the end faces of the contacts and the sputtered conductive layer, and forming a conductor pattern on at least one outer surface of the core, and a plurality of interconnecting paths between the plurality of contacts and the conductor pattern.

20. The method according to claim **19**, wherein the plurality of contacts are configured to be positioned substantially perpendicular to a plane formed by an outer surface of the core,

21. The method according to claim **19**, further comprising the steps of:

applying a resist onto the one outer surface of the core and/or the component such that the spaces between each of the plurality of contacts of the component are filled by the resist.

22. The method according to claim **21**, further comprising a step of:

clearing end faces of the contacts by exposing and developing the resist, wherein the layer of conductive material is deposited onto the cleared end faces of the contacts and the conductive layer.

23. The method according to claim **19**, comprising a step of removing portions of the conductive layer not incorporated into the conductor pattern.

24. The method according to claim **23**, wherein the removal of the areas of the conductive layer occurs by flash-etching.

25. The method according to claim **21**, wherein the applied resist comprises at least one of a photoimageable resist, an epoxy-based lacquer, a photoimageable resist, and polyimide.

26. The method according to claim **19**, wherein the embedding of the at least one component further comprises applying an adhesive layer into the recess of the core such that the adhesive layer fully encloses all surfaces of the component, except for the surface of the component from which the plurality of contacts extend, the adhesive layer extending substantially to the plane of the core.

27. The method according to claim **19**, wherein the recess of the core extends through the conductive layer into the insulating layer.

28. The method according to claim **19**, wherein the resists covers a part of the component and a part of the at least one conductive layer.

29. The method according to claim **19**, wherein the contacts of the component are essentially situated in the plane of an outer surface of the core exhibiting the at least one conductive layer.

30. The method according to claim **19**, wherein the recess is a through hole passing the core, wherein the embedding of the at least one component into the recess of the insulating layer is made by the following steps:

applying a temporary carrier onto the core below the recess,

placing the component into the recess and attaching the component to the temporary carrier so that the contacts of the component are located on that side of the component which is attached to the temporary carrier,

applying a first connecting layer onto the core on a side of the core opposite to the temporary carrier, wherein the first connecting layer enters the recess to adhere the at least one component in the recess, and

removing the temporary carrier from the core.

31. The method according to claim **30**, further comprising a step of:

applying a second connecting layer onto the core on a side of the core opposite to the first connecting layer.

32. The method according to claim **30**, wherein the first connecting layer is a prepreg layer which is laminated onto the core.

33. A Printed circuit board comprising:

at least one insulating layer and at least one patterned conductive layer with at least one conductor path disposed atop the at least one insulating layer,

at least one recess formed in at least one of the at least one insulating layer and the at least one patterned conductive layer,

wherein at least one of the at least one conductive layer and the at least one recess define an outer surface of a core of the printed circuit board,

at least one component comprising a plurality of contacts having spaces therebetween, that at least one component embedded in an adhesive layer disposed within the recess, and

further comprising a plurality of conductive connections interconnecting the contacts of the component and the at least one conductor path of the patterned conductive layer wherein:

the plurality of conductive connections and the at least one conductor path of the patterned conductive layer lie in a single plane,

the adhesive layer fully encloses all surfaces of the component except a surface from which the plurality of contacts extend,

the spaces between each of the plurality of contacts of the component are filled with a resist, and each of the plurality of contacts having an end face distal from the at least one component, and an additional conductive layer being applied onto the end faces of the plurality of contacts and to the at least one patterned conductive layer in the area of the at least one conductor path.

34. The printed circuit board according to claim **33**, wherein the plurality of contacts are configured to be positioned substantially perpendicular to a plane defined by the outer surface of the core.

35. The printed circuit board according to claim **33**, wherein the conductive connections extend at least partly onto the resist.

36. The printed circuit board according to claim **33**, wherein the resist covers the surfaces of the adhesive layer disposed between an outer wall of the component and an inner wall of the recess.

37. The printed circuit board according to claim **33**, wherein the resist comprises at least one of a photoimageable resist, an epoxy-based lacquer, a photoimageable resist, and polyimide.

38. The printed circuit board according to claim **33**, wherein the recess of the core extends through the conductive layer into the insulating layer.

39. The printed circuit board according to claim **33**, wherein the resists covers a part of the component and a part of the at least one conductive layer.

40. The printed circuit board according to claim **33**, wherein the contacts of the component are essentially situated in the plane of an outer surface of the core exhibiting the at least one conductive layer.

41. The printed circuit board according to claim **33**, wherein the adhesive layer comprises at least one of a solvent-free adhesive, a low-solvent adhesive and a prepreg adhesive.

42. The printed circuit board according to claim **33**, wherein each of the plurality of contacts is an elongated contact.

* * * * *