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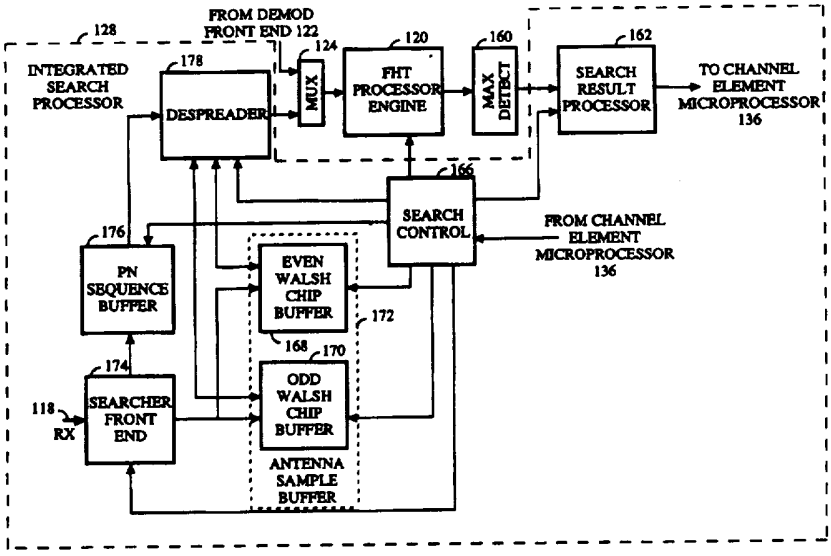

(57) Abstract

An integrated search processor (128) used in a modem for a spread spectrum communications system buffers receive samples and utilizes a time sliced transform processor operating on successive offsets from the buffer. The search processor (128) autonomously steps through a search as configured by a microprocessor (136) specified search parameter set, which can include the group of antennas (112) to search over, the starting offset and width of the search window to search over, and the number of Walsh symbols to accumulate results at each offset. The search processor (128) calculates the correlation energy at each offset, and presents a summary report of the best paths found in the search to use for demodulation element reassignment. This reduces the searching process related workload of the microprocessor (136) and also reduces the modem costs by allowing a complete channel element modem (110) circuit to be produced in a single IC.

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MULTIPATH SEARCH PROCESSOR FOR A SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

I. Field of the Invention

This invention relates generally to spread spectrum communication systems and, more particularly, to the signal processing in a cellular telephone communication system.

II. Description of the Related Art

In a wireless telephone communication system such as cellular telephone systems, personal communications systems and wireless local loop system, many users communicate over a wireless channel to connect to wireline telephone systems. Communication over the wireless channel can be one of a variety of multiple access techniques which facilitate a large number of users in a limited frequency spectrum. These multiple access techniques include time division multiple access (TDMA), frequency division multiple access (FDMA), and code division multiple access (CDMA). The CDMA technique has many advantages and an exemplary CDMA system is described in U.S. Patent No. 4,901,307 issued February 13, 1990 to K. Gilhousen et al., entitled "SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS," assigned to the assignee of the present invention and incorporated herein by reference.

In the just mentioned patent, a multiple access technique is disclosed where a large number of mobile telephone system users, each having a transceiver, communicate through satellite repeaters or terrestrial base stations using CDMA spread spectrum communication signals. In using CDMA communications, the frequency spectrum can be reused multiple times thus permitting an increase in system user capacity.

The CDMA modulation techniques disclosed in U.S. Patent No. 4,901,307 offer many advantages over narrow band modulation techniques used in communication systems using satellite or terrestrial channels. The terrestrial channel poses special problems to any communication system particularly with respect to multipath signals. The use of CDMA techniques permits the special problems of the terrestrial

channel to be overcome by mitigating the adverse effect of multipath, e.g. fading, while also exploiting the advantages thereof.

The CDMA techniques as disclosed in U.S. Patent No. 4,901,307 contemplate the use of coherent modulation and demodulation for both directions of the link in mobile-satellite communications. Accordingly, disclosed therein is the use of a pilot carrier signal as a coherent phase reference for the satellite-to-mobile unit link and the base station-to-mobile unit link. In the terrestrial cellular environment, however, the severity of multipath fading with the resulting phase disruption of the channel, as well as the power required to transmit a pilot carrier signal from the mobile unit, precludes usage of coherent demodulation techniques for the mobile unit-to-base station link. U.S. Patent No. 5,103,459 entitled "SYSTEM AND METHOD FOR GENERATING SIGNAL WAVEFORMS IN A CDMA CELLULAR TELEPHONE SYSTEM", issued June 25, 1990, assigned to the assignee of the present invention, the disclosure of which is incorporated by this reference, provides a means for overcoming the adverse effects of multipath in the mobile unit-to-base station link by using noncoherent modulation and demodulation techniques.

In a CDMA cellular telephone system, the same frequency band can be used for communication in all base stations. At the base station receiver, separable multipath, such as a line of site path and another one reflecting off of a building, can be diversity combined for enhanced modem performance. The CDMA waveform properties that provide processing gain are also used to discriminate between signals that occupy the same frequency band. Furthermore the high speed pseudonoise (PN) modulation allows many different propagation paths of the same signal to be separated, provided the difference in path delays exceeds the PN chip duration. If a PN chip rate of approximately 1 MHz is employed in a CDMA system, the full spread spectrum processing gain, equal to the ratio of the spread bandwidth to the system data rate, can be employed against paths having delays that differ by more than one microsecond. A one microsecond path delay differential corresponds to differential path distance of approximately 300 meters. The urban environment typically provides differential path delays in excess of one microsecond.

The multipath properties of the terrestrial channel produce at the receiver signals having traveled several distinct propagation paths. One characteristic of a multipath channel is the time spread introduced in a signal that is transmitted through the channel. For example, if an ideal impulse is transmitted over a multipath channel, the received signal

appears as a stream of pulses. Another characteristic of the multipath channel is that each path through the channel may cause a different attenuation factor. For example, if an ideal impulse is transmitted over a multipath channel, each pulse of the received stream of pulses generally has a different signal strength than other received pulses. Yet another characteristic of the multipath channel is that each path through the channel may cause a different phase on the signal. For example, if an ideal impulse is transmitted over a multipath channel, each pulse of the received stream of pulses generally has a different phase than other received pulses.

In the radio channel, the multipath is created by reflection of the signal from obstacles in the environment, such as buildings, trees, cars, and people. In general the radio channel is a time varying multipath channel due to the relative motion of the structures that create the multipath. For example, if an ideal impulse is transmitted over the time varying multipath channel, the received stream of pulses would change in time location, attenuation, and phase as a function of the time that the ideal impulse was transmitted.

The multipath characteristic of a channel can result in signal fading. Fading is the result of the phasing characteristics of the multipath channel. A fade occurs when multipath vectors are added destructively, yielding a received signal that is smaller than either individual vector. For example if a sine wave is transmitted through a multipath channel having two paths where the first path has an attenuation factor of X dB, a time delay of δ with a phase shift of Θ radians, and the second path has an attenuation factor of X dB, a time delay of δ with a phase shift of $\Theta + \pi$ radians, no signal would be received at the output of the channel.

In narrow band modulation systems such as the analog FM modulation employed by conventional radio telephone systems, the existence of multiple paths in the radio channel results in severe multipath fading. As noted above with a wideband CDMA, however, the different paths may be discriminated in the demodulation process. This discrimination not only greatly reduces the severity of multipath fading but provides an advantage to the CDMA system.

Diversity is one approach for mitigating the deleterious effects of fading. It is therefore desirable that some form of diversity be provided which permits a system to reduce fading. Three major types of diversity exist: time diversity, frequency diversity, and space/path diversity.

Time diversity can best be obtained by the use of repetition, time interleaving, and error correction and detection coding which introduce

redundancy. A system comprising the present invention may employ each of these techniques as a form of time diversity.

CDMA by its inherent wideband nature offers a form of frequency diversity by spreading the signal energy over a wide bandwidth. Therefore, frequency selective fading affects only a small part of the CDMA signal bandwidth.

Space and path diversity are obtained by providing multiple signal paths through simultaneous links from a mobile unit through two or more base stations and by employing two or more spaced apart antenna elements at a single base station. Furthermore, path diversity may be obtained by exploiting the multipath environment through spread spectrum processing by allowing a signal arriving with different propagation delays to be received and processed separately as discussed above. Examples of path diversity are illustrated in U.S. Patent No. 5,101,501 entitled "SOFT HANDOFF IN A CDMA CELLULAR TELEPHONE SYSTEM", issued March 21, 1992 and U.S. Patent No. 5,109,390 entitled "DIVERSITY RECEIVER IN A CDMA CELLULAR TELEPHONE SYSTEM", issued April 28, 1992, both assigned to the assignee of the present invention.

The deleterious effects of fading can be further controlled to a certain extent in a CDMA system by controlling transmitter power. A system for base station and mobile unit power control is disclosed in U.S. Patent No. 5,056,109 entitled "METHOD AND APPARATUS FOR CONTROLLING TRANSMISSION POWER IN A CDMA CELLULAR MOBILE TELEPHONE SYSTEM", issued October 8, 1991, also assigned to the assignee of the present invention.

The CDMA techniques as disclosed in the U.S. Patent No. 4,901,307 contemplate the use of relatively long PN sequences with each mobile unit user being assigned a different PN sequence. The cross-correlation between different PN sequences and the autocorrelation of a PN sequence, for all time shifts other than zero, both have a nearly zero average value which allows the different user signals to be discriminated upon reception. (Autocorrelation and cross-correlation requires logical "0" take on a value of "1" and logical "1" take on a value of "-1" or a similar mapping in order that a zero average value be obtained.)

However, such PN signals are not orthogonal. Although the cross-correlation essentially averages to zero over the entire sequence length, for a short time interval, such as an information bit time, the cross-correlation is a random variable with a binomial distribution. As such, the signals interfere with each other in much the same as they would if they were wide bandwidth

Gaussian noise at the same power spectral density. Thus the other user signals, or mutual interference noise, ultimately limits the achievable capacity.

It is well known in the art that a set of n orthogonal binary sequences, each of length n, for n any power of 2 can be constructed, see Digital Communications with Space Applications, S.W. Golomb et al., Prentice-Hall, Inc., 1964, pp. 45-64. In fact, orthogonal binary sequence sets are also known for most lengths which are multiples of four and less than two hundred. One class of such sequences that is easy to generate is called the Walsh function, also known as Hadamard matrices.

A Walsh function of order n can be defined recursively as follows:

$$W(n) = \begin{vmatrix} W(n/2) , W(n/2) \\ W(n/2) , W'(n/2) \end{vmatrix}$$

where W' denotes the logical complement of W, and $W(1) = \begin{vmatrix} 0 \end{vmatrix}$.

Thus,

$$W(2) = \begin{vmatrix} 0, 0 \\ 0, 1 \end{vmatrix},$$

$$W(4) = \begin{vmatrix} 0, 0, 0, 0 \\ 0, 1, 0, 1 \\ 0, 0, 1, 1 \\ 0, 1, 1, 0 \end{vmatrix}, \text{and}$$

$$W(8) = \begin{vmatrix} 0, 0, 0, 0, 0, 0, 0, 0 \\ 0, 1, 0, 1, 0, 1, 0, 1 \\ 0, 0, 1, 1, 0, 0, 1, 1 \\ 0, 1, 1, 0, 0, 1, 1, 0 \\ 0, 0, 0, 0, 1, 1, 1, 1 \\ 0, 1, 0, 1, 1, 0, 1, 0 \\ 0, 0, 1, 1, 1, 1, 0, 0 \\ 0, 1, 1, 0, 1, 0, 0, 1 \end{vmatrix}$$

A Walsh symbol, sequence or code is one of the rows of a Walsh function matrix. A Walsh function matrix of order n contains n sequences, each of length n Walsh chips. Each Walsh code has a corresponding Walsh index where the Walsh index refers to the number (1 though n) corresponding to the row in which a Walsh code is found. For example, for n=8 Walsh function matrix given above, the all zeros row corresponds to Walsh index 1 and the Walsh code 0, 0, 0, 0, 1, 1, 1, 1 corresponds to Walsh index 5.

A Walsh function matrix of order n (as well as other orthogonal functions of length n) has the property that over the interval of n bits, the cross-correlation between all the different sequences within the set is zero. This can be seen by noting that every sequence differs from every other sequence in exactly half of its bits. It should also be noted that there is always one sequence containing all zeroes and that all the other sequences contain half ones and half zeroes. The Walsh symbol which consists all logical zeros instead of half one's and zero's is called the Walsh zero symbol.

On the reverse link channel from the mobile unit to the base station, no pilot signal exists to provide a phase reference. Therefore a method is needed to provide a high-quality link on a fading channel having a low Eb/No (energy per bit/noise power density). Walsh function modulation on the reverse link is a simple method of obtaining 64-ary modulation with coherence over the set of six code symbols mapped into the 64 Walsh codes. The characteristics of the terrestrial channel are such that the rate of change of phase is relatively slow. Therefore, by selecting a Walsh code duration which is short compared to the rate of change of phase on the channel, coherent demodulation over the length of one Walsh code is possible.

On the reverse link channel, the Walsh code is determined by the information being transmitted from the mobile unit. For example a three bit information symbol could be mapped into the eight sequences of W(8) given above. An "unmapping" of the Walsh encoded symbols into an estimate of the original information symbols may be accomplished in the receiver by a Fast Hadamard Transform (FHT). A preferred "unmapping" or selection process produces soft decision data which can be provided to a decoder for maximum likelihood decoding.

An FHT is used to perform the "unmapping" process. An FHT correlates of the received sequence with each of the possible Walsh sequences. Selection circuitry is employed to select the most likely correlation value, which is scaled and provided as soft decision data.

A spread spectrum receiver of the diversity or "rake" receiver design comprises multiple data receivers to mitigate the effects of fading. Typically each data receiver is assigned to demodulate a signal which has traveled a different path, either through the use of multiple antennas or due to the multipath properties of the channel. In the demodulation of signals modulated according to an orthogonal signaling scheme, each data receiver correlates the received signal with each of the possible mapping values using an FHT. The FHT outputs of each data receiver are combined and selection

circuitry then selects the most likely correlation value based on the largest combined FHT output to produce a demodulated soft decision symbol.

In the system described in the above-referenced U.S. Patent No. 5,103,459, the call signal begins as a 9600 bit per second information source which is then converted by a rate 1/3 forward error correction encoder to a 28,800 symbols per second output stream. These symbols are grouped 6 at a time to form 4800 Walsh symbols per second, each Walsh symbol selecting one of sixty-four orthogonal Walsh functions that are sixty-four Walsh chips in duration. The Walsh chips are modulated with a user-specific PN sequence generator. The user-specific PN modulated data is then split into two signals, one of which is modulated with an in-phase (I) channel PN sequence and one of which is modulated with a quadrature-phase (Q) channel PN sequence. Both the I channel modulation and the Q channel modulation provide four PN chips per Walsh chip with a 1.2288 MHz PN spreading rate. The I and the Q modulated data are Offset Quadrature Phase Shift Keying (OQPSK) combined for transmission.

In the CDMA cellular system described in the above-referenced U.S. Patent No. 4,901,307, each base station provides coverage to a limited geographic area and links the mobile units in its coverage area through a cellular system switch to the public switched telephone network (PSTN). When a mobile unit moves to the coverage area of a new base station, the routing of that user's call is transferred to the new base station. The base station-to-mobile unit signal transmission path is referred to as the forward link and, as noted above, the mobile unit-to-base station signal transmission path is referred to as the reverse link.

As described above, the PN chip interval defines the minimum separation two paths must have in order to be combined. Before the distinct paths can be demodulated, the relative arrival times (or offsets) of the paths in the received signal must first be determined. The channel element modem performs this function by "searching" through a sequence of potential path offsets and measuring the energy received at each potential path offset. If the energy associated with a potential offset exceeds a certain threshold, a signal demodulation element may be assigned to that offset. The signal present at that path offset can then be combined with the contributions of other demodulation elements at their respective offsets. A method and apparatus of demodulation element assignment based on searcher demodulation element energy levels is disclosed in co-pending U.S. Patent Application Serial No. 08/144,902 entitled "DEMODULATION ELEMENT ASSIGNMENT IN A SYSTEM CAPABLE OF RECEIVING MULTIPLE SIGNALS," filed

October 28, 1993, assigned to the assignee of the present invention. Such a diversity or rake receiver provides for a robust digital link, because all paths have to fade together before the combined signal is degraded.

Figure 1 shows an exemplary set of signals from a single mobile unit arriving at the base station. The vertical axis represents the power received in decibels (dB). The horizontal axis represents the delay in the arrival time of a signal due to multipath delays. The axis (not shown) going into the page represents a segment of time. Each signal spike in the common plane of the page has arrived at a common time but has been transmitted by the mobile station at a different time. In a common plane, peaks to the right were transmitted at an earlier time by the remote unit than peaks to the left. For example, the left-most peak spike 2 corresponds to the most recently transmitted signal. Each signal spike 2-7 has traveled a different path and therefore exhibits a different time delay and a different amplitude response. The six different signal spikes represented by spikes 2-7 are representative of a severe multipath environment. Typical urban environments produces fewer usable paths. The noise floor of the system is represented by the peaks and dips having lower energy levels. The task of a searcher element is to identify in the delay as measured by the horizontal axis of signal spikes 2 - 7 for potential demodulation element assignment. The task of the demodulation elements is to demodulate a set of the multipath peaks for combination into a single output. It is also the task of the demodulation elements once assigned to a multipath peak to track that peak as it may move in time.

The horizontal axis can also be thought of as having units of PN offset. At any given time, the base station receives a variety of signals from a single mobile unit, each of which has traveled a different path and may have a different delay than the others. The mobile unit's signal is modulated by a PN sequence. A copy of the PN sequence is also generated at the base station. At the base station, each multipath signal is individually demodulated with a PN sequence code aligned to its timing. The horizontal axis coordinates can be thought of as corresponding to the PN sequence code offset which would be used to demodulate a signal at that coordinate.

Note that each of the multipath peaks varies in amplitude as a function of time as shown by the uneven ridge of each multipath peak. In the limited time shown, there are no major changes in the multipath peaks. Over a more extended time range, multipath peaks disappear and new paths are created as time progresses. The peaks can also slide to earlier or later offsets as the path distance change as the remote unit moves around in the coverage area of the base station. Each demodulation element tracks small variations in the signal

assigned to it. The task of the searching process is to generate a log of the current multipath environment as received by the base station.

In a typical wireless telephone communication system, the mobile unit transmitter may employ a vocoding system which encodes voice information in a variable rate format. For example, the data rate may be lowered due to pauses in the voice activity. The lower data rate reduces the level of interference to other users caused by the mobile unit transmitter. At the receiver, or otherwise associated with the receiver, a vocoding system is employed for reconstructing the voice information. In addition to voice information, non-voice information alone or a mixture of the two may be transmitted by the mobile unit.

A vocoder which is suited for application in this environment is described in copending U.S. patent application Ser. No. 07/713,661, entitled "VARIABLE RATE VOCODER," filed June 11, 1991 and assigned to the assignee of the present invention. This vocoder produces from digital samples of the voice information encoded data at four different rates, e.g. approximately 8,000 bits per second (bps), 4,000 bps, 2,000 bps and 1,000 bps, based on voice activity during a 20 millisecond (ms) frame. Each frame of vocoder data is formatted with overhead bits as 9,600 bps, 4,800 bps, 2,400 bps, and 1,200 bps data frames. The highest rate data frame which corresponds to a 9,600 bps frame is referred to as a "full rate" frame; a 4,800 bps data frame is referred to as a "half rate" frame; a 2,400 bps data frame is referred to as a "quarter rate" frame; and a 1,200 bps data frame is referred to as an "eighth rate" frame. In neither the encoding process nor the frame formatting process is rate information included in the data. When the mobile unit transmits data at less than full rate, the duty cycle of the mobile units transmitted signal is the same as the data rate. For example, at quarter rate a signal is transmitted from the mobile unit only one quarter of the time. During the other three quarters time, no signal is transmitted from the mobile unit. The mobile unit includes a data burst randomizer. Given the data rate of the signal to be transmitted, the data burst randomizer determines during which time slots the mobile unit transmits and during which time slots it does not. Further details on the data burst randomizer are described in copending U.S. patent application Serial No. 07/846,312, entitled "DATA BURST RANDOMIZER," filed March 5, 1992, and assigned to the assignee of the present invention.

At the base station, each individual remote unit signal must be identified from the ensemble of call signals received to be demodulated back into the original call signal of the mobile unit. A system and method for

demodulating a mobile unit signal received at a base station is described, for example, in U.S. Patent No. 5,103,459 . Figure 2 is a block diagram of the base station equipment described in U.S. Patent No. 5,103,459 for demodulating a reverse link mobile unit signal.

A typical prior art base station comprises multiple independent searcher and demodulation elements. The searcher and demodulation elements are controlled by a controller. In this exemplary embodiment, to maintain a high system capacity, each mobile station in the system does not continually transmit a pilot signal. The lack of a pilot signal on the reverse link increases the time needed to conduct a survey of all possible time offsets at which a mobile station signal may be received. Typically, a pilot signal is transmitted at a higher power than the traffic bearing signals thus increasing the signal to noise ratio of the received pilot signal as compared to the received traffic channel signals. In contrast, ideally each mobile unit transmits a reverse link signal which arrives with a signal level equal to the power level received from every other mobile unit therefore having a low signal to noise ratio. Also, a pilot channel transmits a known sequence of data. Without the pilot signal, the searching process must examine all possibilities of what data may have been transmitted.

For the system of Figure 2, each searcher contains one FHT processor capable of performing one FHT transform during a time period equal to the period of a Walsh symbol. The FHT processor is slaved to "real time" in the sense that every Walsh symbol interval one value is input and one value is output from the FHT. Therefore, to provide a rapid searching process, more than one searcher element must be used. The searcher elements continually scan in search of a particular mobile station's information signal as controlled by system controller. The searcher elements scan a set of time offsets around the nominal arrival of the signal in search of multipath signals that have developed. Each of searcher elements supplies back to the controller the results of the search it performs. The controller tabulates these results for use in the assignment of the demodulation elements to the incoming signals.

Figure 2 shows an exemplary embodiment of a prior art base station. The base station of Figure 2 has one or more antennas 12 receiving CDMA reverse link mobile unit signals 14. Typically, an urban base station's coverage area is split into three sub-regions called sectors. With two antennas per sector, a typical base station has a total of six receive antennas. The received signals are down-converted to baseband by an analog receiver 16 that quantizes the received signal I and Q channels and sends these digital values over signal lines 18 to channel element modems 20. Each channel element

modem supports a single user. The modem contains multiple digital data receivers, or demodulation elements, 22, 24 and multiple searcher receivers 26. Microprocessor 34 controls the operation of demodulation elements 22 and 24, and searchers 26. The user PN code in each demodulation element and searcher is set to that of the mobile unit assigned to that channel element. Microprocessor 34 steps searchers 26 through a set of offsets, called a search window, that is likely to contain multipath signal peak suitable for demodulation elements assignment. For each offset, searcher 26 reports the energy it found at that offset back to microprocessor 34. Demodulation elements 22 and 24 are then assigned by microprocessor 34 to the paths identified by searcher 26 (i.e. the timing reference of their PN generators is moved to align it to that of the found path). Once a demodulation element has locked onto the signal at its assigned offset, it then tracks that path on its own without microprocessor supervision, until the path fades away or until the demodulation element is assigned to a better path by the microprocessor.

In Figure 2, the internal structure of only one demodulation element 22 is shown, but should be understood to apply to demodulation element 24 and searchers 26 as well. Each demodulation element 22, 24 or searcher 26 of the channel element modem has a corresponding I PN and Q PN sequence generator 36, 38 and the user-specific PN sequence generator 40 that is used to select a particular mobile unit. User-specific PN sequence output 40 is XOR'd by XOR gates 42 and 44 with the output of I PN and Q PN sequence generators 36 and 38 to produce PN-I' and PN-Q' sequences that are provided to despreader 46. The timing reference of PN generators 36, 38, 40 is adjusted to the offset of the assigned signal, so that despreader 46 correlates the received I and Q channel antenna samples with the PN-I' and PN-Q' sequence consistent with the assigned signal offset. Four of the despreader outputs, corresponding to the four PN chips per Walsh chip, are summed to form a single Walsh chip by accumulators 48, 50. The accumulated Walsh chip is then input into Fast Hadamard Transform (FHT) processor 52. FHT processor 52 correlates a set of sixty-four received Walsh chips with each of the sixty-four possible transmitted Walsh functions and outputs a sixty-four entry matrix of soft decision data. FHT output of FHT processor 52 for each demodulation element is then combined with those of other demodulation elements by combiner 28. The output of combiner 28 is a "soft decision" demodulated symbol. Soft decision data is the chosen demodulated symbol weighted by the confidence that it correctly identifies the originally transmitted Walsh symbol. The soft decision is then passed to forward error correction decoder 29 for further processing to recover the original call signal.

This call signal is then sent through digital link 30 that routes the call to public switched telephone network (PSTN) 32.

Like each demodulation element 22, 24, each searcher 26 contains a complete demodulation data path. Searcher 26 only differs from demodulation element 22 in how its output is used and in that it does not provide time tracking. For each offset processed, each searcher 26 finds the correlation energy at that offset by despreading the antenna samples, accumulating them into Walsh chips that are input to the FHT transform, performing the FHT transform and summing the maximum FHT output energy for each of the Walsh symbols for which the searcher dwells at an offset. The final sum is reported back to microprocessor 34. Generally each searcher 26 is stepped through the search window with the others as a group by microprocessor 34, each separated from its neighbor by half of a PN chip. In this way enough correlation energy exists at each maximum possible offset error of a quarter chip to ensure that a path is not missed by chance just because the searcher did not correlate with the exact offset of the path. After sequencing searchers 26 through the search window, microprocessor 34 evaluates the results reported back, looking for strong paths for demodulation elements assignment as described in above mentioned co-pending U.S. Patent Application Serial No. 08/144,902.

The multipath environment is constantly changing as the mobile unit moves about in the base station coverage area. The number of searches that must be performed is set by the need to find multipath quickly enough so that the path may be put to good use by the demodulation elements. On the other hand, the number of demodulation elements required is a function of the number of paths generally found to be usable at any point in time. To meet these needs, the Figure 2 system has two searchers 26 and one demodulation element 24 for each of four demodulator integrated circuits (IC's) used, for a total of four demodulation elements and eight searchers per channel element modem. Each of these twelve processing elements contains a complete demodulation data path, including the FHT processor which takes a relatively large, costly amount of area to implement on an integrated circuit. In addition to the four demodulator IC's the channel element modem also has a modulator IC and a forward error correction decoder IC for a total of 6 IC chips. A powerful and expensive microprocessor is needed to manage and coordinate the demodulation elements and the searchers. As implemented in the modem of Figure 2, these circuits were completely independent and require the close guidance of microprocessor 34 to sequence through the correct offsets, and handle the FHT outputs. Every Walsh symbol

microprocessor 34 receives an interrupt to process the FHT outputs. This interrupt rate alone necessitates a high powered microprocessor.

It would be advantageous if the six IC's required for a modem could be reduced to a single IC needing less microprocessor support, thereby reducing the direct IC cost and board-level production cost of the modem, and allowing migration to a lower cost microprocessor (or alternately a single high powered microprocessor supporting several channel element modems at once). Just relying on shrinking feature sizes of the IC fabrication process and placing the six chips together on a single die is not enough; the fundamental architecture of the demodulator needs to be redesigned for an truly cost effective single chip modem. From the discussion above, it should be apparent that there is a need for a signal receiving and processing apparatus that can demodulate a spread spectrum call signal in a lower cost, and more architecturally efficient manner.

The present invention is a single, integrated search processor that can quickly evaluate large numbers of offsets that potentially contain multipath of a received call signal. For the system of Figure 2, each searcher contains one FHT processor capable of performing one FHT transform per Walsh symbol. To obtain extra searcher processing power in the Figure 2 approach, additional discrete searcher elements must added, each with its own FHT processor. A fundamental aspect of the invention is to decouple the sequencing of the FHT processor from real time, and instead to use a single time sliced FHT processor shared between the demodulation and the searching processes. To take full advantage of the rapid FHT processing requires that the FHT processor be supplied with a rapid stream of data. The present invention incorporates an efficient mechanism of supplying data to the FHT processor.

SUMMARY OF THE INVENTION

In accordance with the invention, a signal demodulator for a spread spectrum communication system uses a single, integrated search processor to quickly evaluate large numbers of offsets that potentially contain multipath of a received call signal. After completing an assigned search, the integrated search processor presents a summary of the best candidate paths for assignment of the demodulation elements.

Operation of the integrated search processor is based on a demodulation of the Walsh encoded antenna samples using a Fast Hadamard Transform (FHT) processor engine. The FHT processor engine can operate at many times the real time rate at which the data is received. For example in the preferred embodiment, the FHT processor engine can produce 32 Walsh

symbol correlation results in the time that the system receives one Walsh symbol worth of data.

To take advantage of the fast FHT processor engine, a system is needed to supply the FHT processor engine with data at a correspondingly high rate. In the preferred embodiment, the antenna samples are spread spectrum modulated and must be despread before being passed to the FHT processor engine.

Two buffers are needed to supply the despreader with input: a first buffer is needed to store the antenna data samples and a second buffer is needed to store PN sequence samples. Because there are more bits of data associated with the antenna samples than with the PN sequence, it is advantageous to limit the number of the antenna data samples that needs to be stored even if it means extending the number of the PN sequence data which must be stored. The antenna sample buffer in the preferred embodiment can store two Walsh symbols worth of data. It is written to and read from in a circular manner. The PN sequence buffer contains four Walsh symbols worth of data in the preferred embodiment.

To facilitate the circular manner of operation of the antenna sample buffer, the operation of the integrated search processor is broken down into groups of discrete searches. Each group of discrete searches is called a search rake. Each discrete search is called a rake element. Each rake element corresponds to one Walsh symbol worth of data and one FHT processor engine transform operation. The circular buffer operates such that each successive rake element in a search rake is offset from the preceding rake element by one half of a PN sequence chip and by one half offset in time. In this configuration, each rake element in a common search rake is correlated with the same PN sequence.

Groups of search rakes can be specified in a search windows. Groups of search windows can be specified as antenna search sets. An antenna search sets can be specified by a microprocessor by designating a few parameters. The integrated search processor then performs the designated searches and supplies the results back to the microprocessor with no further input from the microprocessor. In this manner the integrated search processor performs a plurality of searches quickly with minimum amount of processor interaction.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when

taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

Figure 1 represents an exemplary severe multipath signal condition;

Figure 2 is a block diagram of a prior art communications network demodulation system;

Figure 3 represents an exemplary CDMA telecommunications system constructed in accordance with the present invention;

Figure 4 is a block diagram of a channel element modem constructed in accordance with the present invention;

Figure 5 is a block diagram of the search processor;

Figure 6 illustrates the circular nature of the antenna sample buffer using a first offset;

Figure 7 illustrates the circular nature of the antenna sample buffer for a second accumulation at the first offset of Figure 6;

Figure 8 illustrates the circular nature of the antenna sample buffer for a second offset;

Figure 9 is a graph showing how the searcher processes the receiver input as a function of time;

Figure 10 is a block diagram of the searcher front end;

Figure 11 is a block diagram of the searcher despreader;

Figure 12 is a block diagram of the searcher result processor;

Figure 13 is a block diagram of the searcher sequencing control logic;

Figure 14 is a timing diagram showing the processing sequence depicted in Figure 5, showing the corresponding states of certain control logic elements presented in Figure 13; and

Figure 15 is an alternative block diagram of the search processor.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention can be implemented in a wide variety of data transmission applications and in the preferred embodiment illustrated in Figure 2 is implemented within a system 100 for voice and data transmission in which a system controller and switch, also referred to as mobile telephone switching office (MTSO) 102, performs interface and control functions to permit calls between mobile units 104 and base stations 106. MTSO 102 also controls the routing of calls between public switched telephone network (PSTN) 108 and the base stations 106 for transmission to and from the mobile units 104.

Figure 4 illustrates channel element modem 110 and other elements of the base station infrastructure operating in accordance with the CDMA

methods and data formats described in the above-referenced patents. A plurality of antennas 112 provides reverse link signal 114 to analog transmitter receiver 116. Analog transmitter receiver 116 down-converts the signal to baseband and samples the waveform at eight times the PN chip rate. Analog transmitter receiver 116 provides the digital samples to channel element modem 110 through base station RX backplane signal 118. When assigned to active call, demodulator front end 122 and integrated search processor 128 isolate a signal from a particular call from the plurality of call signals contained in reverse link signal by use of the PN sequences as described in the above referenced patents.

Channel element modem 110 of Figure 4 includes a single, integrated search processor 128 for identifying multipath signals within the received signal. Channel element modem 110 contains a single time shared Fast Hadamard Transform (FHT) processor engine 120 to service both integrated search processor 128 and demodulator front end 122. FHT processor engine 120 matches the input data to each of the possible Walsh symbols. In this exemplary embodiment there are 64 possible Walsh symbols. FHT processor engine 120 outputs an energy level corresponding to each of the 64 possible Walsh symbols where higher energy levels indicate higher probability that the corresponding Walsh symbol was the actual transmitted symbol. Max detect 160 determines the largest of the sixty-four outputs for each input to FHT processor engine 120. This maximum energy and the index of the Walsh symbol is then passed to integrated search processor 128 and pipelined demodulator processor 126. Pipelined demodulator processor 126 contains functionality contained in the prior art non-integrated demodulation elements which is not implemented in demodulator front end 122 that can be shared in the same time sliced manner as FHT processor engine 120. Pipelined demodulator processor 126 also time aligns and combines symbol data received at different offsets into a single demodulated "soft decision" symbol stream which is weighted for best performance of deinterleaver - forward error correction decoder 130. In addition, pipeline demodulator processor 126 calculates the power level of the signal being received. From the received power level a power control indication is created to command the mobile unit to raise or lower the mobile unit's transmit power. The power control indication is passed through modulator 140 which adds the indication to the base station transmitted signal for reception by the mobile unit. This power control loop operates under the method described in U.S. Patent 5,056,109 referenced above.

The soft decision symbol stream is output to deinterleaver - forward error correction decoder 130 where it is deinterleaved and decoded. Channel element microprocessor 136 supervises the entire demodulation procedure and obtains the recovered call signal from the deinterleaver - forward error correction decoder via microprocessor bus interface 134. The call signal is then routed through digital backhaul link 121 to MTSO 102 which connects the call through PSTN 108.

The forward link data path proceeds much as the inverse of the functions just presented for the reverse link. The signal is provided from PSTN 108 through MTSO 102 and to digital backhaul 121. Digital backhaul 121 provides input to encoder - interleaver 138 through channel element microprocessor 136. After encoding and interleaving the data, encoder - interleaver 138 passes the data to modulator 140 where it is modulated as disclosed in the above mentioned patents. The output of the modulator is passed to transmit summer 142 where it is added to the outputs of other channel element modems prior to being up-converted from baseband and amplified in analog transmitter receiver 116. A summing method is presented in a co-pending U.S. Patent Application Serial No. 08/316,156 entitled "SERIAL LINKED INTERCONNECT FOR THE SUMMATION OF MULTIPLE DIGITAL WAVEFORMS," filed September 30, 1994, and assigned to the assignee of the present application. As presented in the above referenced application, the transmit summer corresponding to each element 110 can be cascaded in a daisy-chain fashion eventually resulting in a final sum that is provided to the analog transceiver for broadcasting.

Figure 5 shows the elements comprising integrated search processor 128. The heart of the searching process is time sliced FHT processor engine 120, which, as mentioned above, is shared between integrated search processor 128 and demod front end 122 (not shown in Figure 5). Other than sharing FHT processor engine 120 and max detect 160 block, integrated search processor 128 is stand alone, self-controlled, and self-contained. In a manner described below, FHT processor engine 120 can perform Walsh symbol transforms at a rate 32 times faster than FHT processor 52 of Figure 2. This rapid transform capability empowers the time sliced performance of channel element modem 110.

In the preferred embodiment FHT processor engine 120 is constructed using a six stage butterfly network. Such butterfly networks architectures are well known in the art. They provide an efficient mechanism to perform an FHT both in terms of minimizing the number of gates and operations and in

terms of the number of and speed of clock cycles need to complete the transform.

A butterfly network can be used to create an inverse transform noting the symmetry which is used to create the Walsh symbols. A Walsh function of order n can be defined recursively as follows:

$$W(n) = \begin{vmatrix} W(n/2) , W(n/2) \\ W(n/2) , W'(n/2) \end{vmatrix}$$

where W' denotes the logical complement of W, and $W(1) = |0|$

In the preferred embodiment a Walsh sequence is generated where n = 6, therefore a 6-stage butterfly trellis is used to correlate the 64 input sample with each of the 64 possible Walsh functions. The butterfly trellis is a series of 6 parallel adders.

To reap the benefits of FHT processor engine 120 with thirty-two times the throughput of its real-time-slaved counterpart, FHT processor engine 120 must be provided with high rate input data to process. Antenna sample buffer 172 has been specifically tailored to meet this need. Antenna sample buffer 172 is written to and read from in a circular manner

The searching process is grouped in sets of single offset searches. The highest level of grouping is the antenna search set. Each antenna search set is made up of a plurality of search windows. Typically each search window in the antenna search set is an identically performed search group where each search window in the antenna search receives data from a different antenna. Each search window is made up of a series of search rakes. A search rake is a set of sequential search offsets that is performed in a time equivalent to the duration of a Walsh symbol. Each search rake is comprised of a set of rake elements. Each rake element represents a single search at a given offset.

At the beginning of the searching process, channel element microprocessor 136 sends parameters specifying a search window which may be part of an antenna search set. The width of the search window may be designated in PN chips. The number of search rakes needed to complete the search window varies depending on the number of PN chips specified in the search window. The number of rake elements per search rake can be specified by channel element microprocessor 136 or could be fixed to some constant.

Referring again to Figure 1 showing an exemplary set of signals arriving at the base station from a single mobile unit, the relationship of the search window, search rake, and rake element becomes more clear. The vertical axis in Figure 1 represents the power received in decibels (dB). The

horizontal axis represents the delay in the arrival time of a signal due to multipath delays. The axis (not shown) going into the page represents a segment of time. Each signal spike in the common plane of the page has arrived at the same time but has been transmitted by the mobile station at a different time.

The horizontal axis can be thought of as having units of PN chip offset. At any given time, the base station perceives a variety of signals from a single mobile unit, each of which has traveled a different path and may have a different delay than the others. The mobile unit's signal is modulated by a PN sequence. A copy of the PN sequence is also generated at the base station. At the base station, if each multipath signal were individually demodulated, a PN sequence code aligned to each signal's timing would be needed. Each of these aligned PN sequences would be delayed from the zero offset reference at the base station due to the delay. The number of PN chips that the aligned PN sequence is delayed from the zero offset base station reference could be mapped to the horizontal axis.

In Figure 1, time segment 10 represents a search window set of PN chip offsets to be processed. Time segment 10 is divided into five different search rakes such as search rake time segment 9. Each search rake is in turn made up of a number of rake elements which represent the actual offsets to be searched. For example, in Figure 1, each search rake is made up of 8 different rake elements such as the rake element indicated by arrow 8.

To process a single rake element as indicated by arrow 8, a set of samples over time at that offset are needed. For example, to process the rake element indicated by arrow 8, the despreading process needs the set of sample at the offset indicated by arrow 8 going back into the page over time. The despreading process also needs a corresponding PN sequence. The PN sequence can be determined by noting the time the samples arrived and the offset desired to be processed. The desired offset can be combined with the arrival time to determine the corresponding PN sequence to be correlated with the received samples.

As the rake element is despread the receive antenna samples and the PN sequence are run through a series of values over time. Note that the received antenna samples are the same for all offsets shown in Figure 1 and spikes 2-7 are showing exemplary multipath peaks which arrive simultaneously and are only discriminated by the despreading process.

In the preferred embodiment described below, each rake element is offset in time from the preceding rake element by one half PN chip in time. This means that if the rake element corresponding to arrow 8 was correlated

beginning from the sliced plane shown and moving forward in time (into the page as shown) then the rake element to the left of the one corresponding to arrow 8 would use samples starting one half chip in time back from the sliced plane shown. This progression in time allows each rake element in a common search rake to be correlated to the same PN sequence.

Each mobile unit receives the base station's transmitted signal delayed by some amount due to the path delay through the terrestrial environment. The same short and long code generation is also being performed in the mobile unit. The mobile unit generates a time reference based on the time reference it perceives from the base station. The mobile unit uses the time reference signal as an input to it's long and short code generators. The information signal received at the base station from the mobile unit is therefore delayed by the round trip delay of the signal path between the base station and the mobile unit. Therefore if the timing of PN generator 202, 204, and 206 used in the searching process is slaved to the zero offset timing reference at the base station, the output of the generators will always be available before the corresponding signal is received from the mobile unit.

In an OQPSK signal, the I channel data and the Q channel data are offset from each other by one half chip in time. Therefore OQPSK despreading used in the preferred embodiment requires data sampled at twice the chip rate. The searching process also operates optimally with data sampled at half the chip rate. Each rake element within a search rake is offset by one half chip from the previous rake element. The one half chip rake element resolution ensures that multipath peak signals are not skipped over without detection. For these reasons antenna sample buffer 172 stores data sampled at twice the PN chip rate.

One Walsh symbol worth of data is read from antenna sample buffer 172 to process a single rake element. Each successive rake element is read out of antenna sample buffer 172 half of a PN chip offset from the previous rake element. Each rake element is despread with the same PN sequence read from PN sequence buffer 176 by the despreader. Antenna sample buffer 172 is for each rake element in the search rake.

Antenna sample buffer 172 is two Walsh symbols deep and is repeatedly read from and written to throughout the searching process. Within each search rake, the rake element having the latest offset in time is processed first. The latest offset corresponds to the signal which has traveled the longest signal path from the mobile unit to the base station. The time at which the searcher starts to process a search rake is keyed to the Walsh symbol boundaries associated with the rake element having the latest offset in the

search rake. A time strobe, referred to as the offset Walsh symbol boundary, indicates the earliest time that the searching process can begin the first rake element in the search rake because all of the samples needed are available in antenna sample buffer 172.

The operation of antenna sample buffer 172 is most easily illustrated by noting its circular nature. Figure 6 shows an illustrative diagram of the operation of antenna sample buffer 172. In Figure 6 thick circle 400 can be thought of as antenna sample buffer 172 itself. Antenna sample buffer 172 contains memory locations for two Walsh symbols worth of data. Write pointer 406 circulates around antenna sample buffer 172 in the direction indicated in real time, meaning that write pointer 406 rotates around the two Walsh symbol deep antenna sample buffer 172 in the time that two Walsh symbols worth of samples are passed to searcher front end 174. As the samples are written into antenna sample buffer 172 according to the memory location indicated by write pointer 406, the previously stored values are overwritten. In the preferred embodiment, antenna sample buffer 172 contains 1024 antenna samples because each of the two Walsh symbols contains 64 Walsh chips, each Walsh chip contains 4 PN chips, and each PN chip is sampled twice.

The operation of the searching process is divided into discrete 'time slices.' In the preferred embodiment, a time slice is equal to 1/32 of the Walsh symbol duration. The choice of 32 time slices per Walsh symbol is derived from the available clocking frequency and number of clock cycles need to perform an FHT. 64 clock cycles are required to perform an FHT for one Walsh symbol. In the preferred embodiment, a clock running at eight times the PN chip frequency is available and provides the necessary performance level. Eight times the PN chip rate multiplied by the 64 required clocks is equivalent to the time it takes to receive two Walsh chips worth of data. Because there are 64 Walsh chips in each half of the buffer, 32 time slices are needed to read in a complete Walsh symbol.

In Figure 6, a set of concentric arcs on the outside of thick circle 400 represents read and write operation with antenna sample buffer 172. (The arcs within thick circle 400 are used to aid explanation and do not correspond to read or write operations.) Each arc represents a read or write operation during one time slice. The arc closest to the center of the circle occurs first in time and each successive arc represents an operation occurring in successively later time slices as indicated by time arrow 414. Each of the concentric arcs corresponds to a section of antenna sample buffer 172 as represented by thick circle 400. If one were to imagine radii drawn from the center of thick

circle 400 to the end points of each of the concentric arcs, the portion of thick circle 400 between the intersection of the radii and thick circle 400 would be representative of the memory locations accessed. For example, during the first time slice operation shown, 16 antenna samples are written to antenna sample buffer 172 represented by arc 402A.

In Figures 6, 7, and 8 the following search parameters for the illustrative search window are assumed:

Search window width = 24 PN chips
Search offset = 24 PN chips
Number of symbols to accumulate = 2
Number of rake elements per search rake =24.

Figure 6 also assumes that antenna sample buffer 172 contains nearly a full Walsh symbol worth of valid data before the write indicated by arc 402A. During subsequent time slices, a write corresponding to arc 402B and to arc 402C occurs. During the 32 time slices available during one Walsh symbol worth of time, the write operations continue from arc 402A to arc 402FF most of which are not shown.

The 32 time slices represented by arcs 402A to 402FF correspond to the time used to complete one search rake. Using the parameters given above, the search rake begins 24 PN chips offset from zero offset reference or 'real time' and contains 24 rake elements. The 24 PN chip offset corresponds to a rotation 16.875 degrees around thick circle 400 from the beginning of the first write indicated by arc 402A (calculated by dividing the 24 PN chip offset by the 256 total number of chips in half antenna sample buffer 172 and multiplying by 180 degrees.) The 16.875 degree arc is illustrated by arc 412. The 24 rake elements correspond to reads indicated by arcs 404A - 404X most of which are not shown. The first read corresponding to arc 404A begins at the offset some time after the write corresponding to 402C so that a contiguous set of data is available. Each successive read such as 404B is offset from the previous by a single memory location, corresponding to a 1/2 PN chip of time. During the search rake shown, the reads move toward earlier time offsets as shown by arcs 404A - 404X slanting counter clockwise with progressing time in the opposite rotation direction as write pointer indication 406. The 24 read represented by arcs 404A to 404X traverse the arc indicated by arc 418. The progression of the reads toward earlier samples has the advantage of providing seamless searching within a search window as each search rake is executed. This advantage is explained in detail subsequently herein.

Each of the reads corresponding to arcs 404A to 404X passes one Walsh symbol worth of data to despreader 178. The read therefore corresponds to traversing thick circle 400 by 180 degrees. Note that in the search rake shown of Figure 6, the last write corresponding to arc 402FF, and last read corresponding to arc 404X do not include any common memory locations to ensure contiguous valid data. However, hypothetically, if the pattern of read and writes were to continue they would in fact intersect and valid data would not be provided under this condition.

In most signaling conditions, the result of a rake element worth of data collected during one Walsh symbol worth of time is not sufficient to provide accurate information about the location of diverse signals. In these cases, a search rake may be repeated multiple times. The results of rate elements in successive search rakes at a common offset are accumulated by search result processor 162 as explained in detail subsequently herein. In this case the search parameters given above indicate that the number of symbols to accumulate at each offset is two. Figure 7 shows the search rake of Figure 6 repeated at the same offset for the next successive Walsh symbol worth of data. Note that antenna sample buffer 172 contains two Walsh symbols worth of data so that the data that is needed for processing during the search rake indicated on Figure 7 was written during the search rake shown on Figure 6. In this configuration, memory locations 180 degrees away from each other represent the same PN offset.

After completing the two accumulated search rakes in Figures 6 and 7, the searching process advances to the next offset in the search window. The amount of the advance is equal to the width of the search rake processed, in this case 12 PN chips. As specified in the search parameters, the search window width is 24 PN chips. The width of the window will determine how many search rake offsets are needed to complete the search window. In this case two different offsets are needed to cover the 24 PN chip window width. The window width is indicated on Figure 8 by arc 412. The second offset for this search window begins at the offset following the last offset of the previous search rake and continues around to the nominal zero offset point as set by the location of the beginning of the first write as indicated by arc 430A. Again there are 24 rake elements within the search rake as indicated by arcs 432A-432X most of which are not shown. Again the 32 writes are indicated by the arcs 430A - 430FF. Thus the last write, as indicated by arc 430FF, and the last read, as indicated by arc 432X, abut one another in antenna sample buffer 172 as indicated by reference arrow 434.

The search rake shown in Figure 8 is repeated on the opposite side of antenna sample buffer 172 much as the search rake in Figure 6 is repeated in Figure 7 because the search parameters designate that each symbol is accumulated twice. At the completion of the second accumulation of the second search rake, integrated search processor 128 is available to begin another search window. The subsequent search window could have a new offset or it could specify a new antenna or both.

In Figure 8, the location of the boundary between the read half and the write half of the buffer is marked with label 436. In Figure 6, the boundary is marked with label 410. The signal which indicates the point in time corresponding to label 436 is referred to as the offset Walsh symbol strobe and also indicates that a new Walsh symbol worth of samples is available. As the search rakes within a window advance to earlier offsets, the boundary between the read and write halves of the buffer slews in lock step counterclockwise as shown in Figure 8. If after the completion of the present search window, if a large change in the offset being processed is desired, the offset Walsh symbol strobe may be advanced a large portion of the circumference of the circle.

Figure 9 is a search timeline that provides further graphical illustration of the searcher processing. Time is plotted along the horizontal axis in units of Walsh symbols. Antenna sample buffer 172 address, and PN sequence buffer 176 addresses are shown along the vertical axis, also in units of Walsh symbols. Because antenna sample buffer 172 is two Walsh symbols deep, antenna sample buffer 172 addressing wraps on even Walsh symbol boundaries, but for illustrative purposes, Figure 9 shows the addresses before being folded on top of one another. Samples are written into antenna sample buffer 172 at an address taken directly from the time they were obtained, so write pointer 181 into antenna sample buffer 172 is a straight forty-five degree inclined line. The offset being processed maps into a base address in antenna sample buffer address 174 to start a read of a Walsh symbol of samples for a single rake element. The rake elements are illustrated in Figure 9 as nearly vertical read pointer line segments 192. Each rake element maps to a Walsh symbol in height as referred to the vertical axis.

The vertical gaps between the rake elements within a search rake are caused by demod front end 122 interrupting the search process to use FHT processor engine 120. Demod front end 122 operates in real time and has first priority use of FHT processor engine 120 whenever it has a current or queued set of data for processing. Therefore typically use of FHT processor engine 120 is given to demod front end 120 on each Walsh symbol boundary

corresponding to a PN offset that is being demodulated by demod front end 122.

Figure 9 shows the same search rakes shown in Figures 6, 7, and 8. For example, search rake 194 has its 24 rake elements each of which corresponds to one to the read arcs 404A - 404X on Figure 6. On Figure 9 for search rake 194, pointer 410 indicates the offset Walsh symbol strobe corresponds to the like pointer on Figure 6. To read the current samples, each rake element must be beneath write pointer 181. The downward slope of the rake elements with a search rake indicates the steps towards earlier samples. Search rake 195 corresponds to the search rake shown in Figure 7 and search rake 196 corresponds to the search rake shown in Figure 8.

In the search window defined by the parameters above, only 24 rake elements per search rake are specified even though the search rake has 32 available time slices. Each rake element can be processed in one time slice. However, it is not practically possible to increase the number of rake elements per search rake to 32 to match the number of time slices available during a search rake. Demod front end 122 uses some of the available time slices of the FHT processor time such as the four slices used for processing the signals in inset 178 in Figure 9. There is also a time delay associated with a rake advance as the read process must wait for the write process to fill the buffer with valid data at the advanced offset. Also some margin is needed to synchronize to a time slice processing boundary after observing the offset Walsh symbol strobe. All these factors practically limit the number of rake elements which can be processed in a single search rake. In some cases the number of rake elements per search rake could be increased such as if demod front end 122 has only one demodulation element assigned and only interrupts FHT processor engine 120 once per search rake. Therefore in the preferred embodiment, the number of rake elements per search rake is controllable by channel element microprocessor 136. In alternative embodiments, the number of rake elements per search rake could be a fixed constant.

There also can be significant overhead delay when switching between source antennas at the input to the sample buffer or changing the search window starting point or width between searches. If one rake needs a particular set of samples and the next rake for a different antenna needs to use an overlapping part of the buffer, the next rake must postpone processing until the next offset Walsh symbol boundary occurs, at which point a complete Walsh symbol of samples for the new antenna source are available. In Figure 9, search rake 198 is processing data from a different antenna than search rake 197. Horizontal line 188 indicates the memory location

corresponding to the new antenna input samples. Note that search rake 197 and 198 do not use any common memory locations.

For every time slice, two Walsh chips of samples must be written to the sample buffer and one full Walsh symbol of samples may be read from the sample buffer. In the preferred embodiment, there are 64 clock cycles during each time slice. A full Walsh chip of samples is comprised of four sets of samples: ontime I channel samples, late I channel samples, ontime Q channel samples and late Q channel samples. In the preferred embodiment, each sample is four bits. Therefore sixty four bits per clock are needed from antenna sample buffer 172. Using a single port RAM, the most straightforward buffer design doubles the word width to 128 bits, and splits the buffer into two 64 bit wide, 64 word, independently read/writeable even and odd Walsh chip buffers 168, 170. The much less frequent writes to the buffer are then multiplexed in between reads, which toggle between the two banks on successive clock cycles.

The Walsh chip of samples read from the even and odd Walsh chip buffers 168, 170 has an arbitrary alignment to the physical RAM word alignment. Therefore on the first read of a time slice, both halves are read into despreader 178 to form a two Walsh chip wide window from which the single Walsh chip with the current offset alignment is obtained. For even Walsh chip search offsets, the even and odd Walsh chip buffer address for the first read are the same. For odd Walsh chip offsets, the even address for the first read is advanced by one from the odd address to provide a consecutive Walsh chip starting from the odd half of the sample buffer. The additional Walsh chips needed by despreader 178 can be passed thereto by a read from a single Walsh chip buffer. Successive reads then ensure that there is always a refreshed two Walsh chip wide window from which to draw a Walsh chip of data aligned to the current offset being processed.

Referring again to Figure 5, for each rake element in a search rake processed, the same Walsh symbol of PN sequence data from the PN sequence buffer 176 is used in the despreading process. For every clock cycle of a time slice, four pairs of PN-I' and PN-Q' are needed. Using a single port RAM, the word width is doubled and read from half as often. The single write to PN sequence buffer 176 needed per time slice is then performed on a cycle not used for reading.

Because the searching process can specify searching PN offsets of up to two Walsh symbols delayed from the current time, four Walsh symbols worth of PN sequence data must be stored. In the preferred embodiment PN sequence buffer 176 is a one hundred and twenty eight word by sixteen bit

RAM. Four Walsh symbols are required because the starting offset can vary by 2 Walsh symbols and once the starting offset is chosen, one Walsh symbol worth of PN sequence is need for correlation meaning three Walsh symbols worth of data is need for the despreading process. Because the same PN sequence is repeatedly used, the data in PN sequence buffer 176 cannot be overwritten during the despreading process corresponding to a single search rake. Therefore an additional Walsh symbol worth of memory is needed to store the PN sequence data as it is generated.

The data that is written into both PN sequence buffer 176 and antenna sample buffer 172 is provided by searcher front end 174. A block diagram of searcher front end 174 is shown in Figure 10. Searcher front end 174 includes short code I and Q PN generators 202, 206 and the long code User PN generator 204. The values output by short code I and Q PN generators 202, 206 and the long code User PN generator 204 are determined by the time of day. Each base station has a universal timing standard such as GPS timing to create a timing signal. Each base station also transmits its timing signal over the air to the mobile units. At the base station, the timing reference is said to have zero offset because it is aligned to the universal reference.

The output of long code User PN generator 204 is logically XOR'd with the output of short code I and Q PN generators 202, 206 by XOR gates 208 and 210 respectively. (This same process is also performed in the mobile unit and the output is used to modulate the mobile unit's transmitted signal.) The output of XOR gates 208 and 210 is stored in serial to parallel shift register 212. Serial to parallel shift register 212 buffers the sequences up to the width of PN sequence buffer 176. The output of serial to parallel shift register 212 is then written into PN sequence buffer 176 at an address taken from the zero offset reference time. In this way, searcher front end 174 provides the PN sequence data to PN sequence buffer 176.

Searcher front end 174 also provides antenna samples to antenna sample buffer 172. Receive samples 118 are selected from one of a plurality of antennas via a MUX 216. The selected receive samples from MUX 216 are passed to latch 218 where they are decimated, meaning one quarter of the samples are selected for use in the searching process. Receive samples 118 have been sampled at eight times the PN chip rate by analog transmitter receiver 116 (of Figure 4). Processing within the searching algorithm is designed for samples taken at one half the chip rate. Therefore only one quarter of the received samples need be passed to antenna sample buffer 172.

The output of the latch 218 is fed to serial to parallel shift register 214, which buffers the samples up to the width of antenna sample buffer 172. The

samples are then written into even and odd Walsh chip buffers 168, 170 at addresses also taken from the zero offset reference time. In this way, despreader 178 can align the antenna sample data with a known offset with respect to the PN sequence.

Referring again to Figure 5, for each clock cycle in a time slice, despreader 178 takes a Walsh chip of antenna samples from antenna sample buffer 172 and a corresponding set of PN sequence values from PN sequence buffer 176 and outputs an I and Q channel Walsh chip to the FHT processor engine 120 through MUX 124.

Figure 11 shows a detailed block diagram of despreader 178. Even Walsh chip latch 220 and odd Walsh chip latch 222 latch the data from even Walsh chip buffer 168 and odd Walsh chip buffer 170 respectively. MUX bank 224 extracts the Walsh chip of samples to be used from the two Walsh chips worth of samples presented to by even and odd Walsh chip latches 220 and 222. MUX select logic 226 defines the boundary of the selected Walsh chip based on the offset of the rake element being processed. A Walsh chip is output to OQPSK despreader XOR bank 228.

The PN sequence values from PN sequence buffer 176 are latched by PN sequence latch 234. Barrel shifter 232 rotates the output of PN sequence latch 234 based on the offset of the rake element being processed and passes the PN sequence to OQPSK despreader XOR bank 228 which conditionally inverts the antenna samples based on the PN sequence. The XOR'd values are then summed through adder tree 230 which performs the sum operation in the OQPSK despread, and then sums four despread chip outputs together to form a Walsh chip for input to FHT processor engine 120.

Referring again to Figure 5, FHT processor engine 120 takes sixty-four received Walsh chips from despreader 178 through MUX 124, and using a 6-stage butterfly trellis, correlates these sixty-four input samples with each of the sixty-four Walsh functions in a sixty-four clock cycle time slice. Max detect 160 can be used to find the largest of the correlation energies output from FHT processor engine 120. The output of MAX detect 160 is passed on to search result processor 162 which is part of integrated search processor 128.

Search result processor 162 is detailed in Figure 12. Search result processor 162 also operates in a time sliced manner. The control signals provided to it are pipeline delayed to match the two time slice delay from the start of inputting Walsh chips to FHT processor engine 120 to obtaining the maximum energy output. As explained above, a set of search window parameters may designate that a number of Walsh symbols worth of data be accumulated before the results of the chosen offset are processed. In the

parameters used with the example of Figures 6, 7, 8, and 9, the number of symbols to accumulate is 2. Search result processor 162 performs the summing function along with other functions.

As search result processor 162 performs the sums over consecutive Walsh symbols, it must store a cumulative sum for each rake element in the search rake. These cumulative sums are stored in Walsh symbol accumulation RAM 240. The results of each search rake are input to summer 242 from max detect 160 for each rake element. Summer 242 sums the present result with the corresponding intermediate value available from Walsh symbol accumulation RAM 240. On the final Walsh symbol accumulation for each rake element, the intermediate result is read from Walsh symbol accumulation RAM 240 and summed by summer 242 with the final energy from that rake element to produce a final search result for that rake element offset. The search results are then compared with the best results found in the search up to this point as explained below.

In the above mentioned co-pending U.S. Patent Application Serial No. 08/144,902 entitled "DEMODULATION ELEMENT ASSIGNMENT IN A SYSTEM CAPABLE OF RECEIVING MULTIPLE SIGNALS," the preferred embodiment assigns the demodulation elements based on the best results from a search. In the present preferred embodiment, the eight best results are stored in best result register 250. (A lesser or greater number of results could be stored in other embodiments.) Intermediate result register 164 stores the peak values and their corresponding rank order. If the current search result energy exceeds at least one of the energy values in intermediate result register 164, search result processor control logic 254 discards the eighth best result in intermediate result register 164, and inserts the new result, along with its appropriate rank, the PN offset, and antenna corresponding to the rake element result. All lesser ranked results are "demoted" one ranking. There are a great number of methods well known in the art for providing such a sorting function. Any one of them could be used within the scope of this invention.

Search result processor 162 has a local peak filter basically comprised of comparator 244 and previous energy latch 246. The local peak filter, if enabled, prevents intermediate result register 164 from being updated even though a search result energy would otherwise qualify for inclusion, unless the search result represents a local multipath peak. In this way, the local peak filter prevents strong, broad "smeared" multipath from filling multiple entries in intermediate result register 164, leaving no room for weaker but distinct multipath that can make better candidates for demodulation.

The implementation of the local peak filter is straightforward. The energy value of the previous rake element summation is stored in previous energy latch 246. The present rake element summation is compared to the stored value by comparator 244. The output of comparator 244 indicates which of its two inputs is larger and is latched in search result processor control logic 254. If the previous sample represented a local maxima, search result processor control logic 254 compares the previous energy result with the data stored in intermediate result register 164 as described above. If the local peak filter is disabled by channel element microprocessor 136 then the comparison with intermediate result register 164 is always enabled. If either the leading or the last rake element at the search window boundary has a slope, then the slope latch is set so the boundary edge value can be considered as a peak as well.

The simple implementation of this local peak filter is aided by the progression of the reads toward earlier symbols within a search rake. As illustrated in Figure 6, 7, 8, and 9, within a search rake each rake element progress toward signals arriving earlier in time. This progression means that within a search window, the last rake element of a search rake and the first rake element of the subsequent search rake are contiguous in offset. Therefore, the local peak filter operation does not have to change and the output of comparator 244 is valid across search rake boundaries.

At the end of processing a search window, the values stored in intermediate result register 164 are transferred to best result register 250 readable by channel element microprocessor 136. Search result processor 162 has thus taken much of the workload from channel element microprocessor 136, which in the system of Figure 2 needed to handle each rake element result independently.

The preceding sections have focused on the processing data path of integrated search processor 128 and have detailed how raw antenna samples 118 are translated into a summary multipath report at the output of best result register 250. The following sections detail how the each of the elements in the search processing data path are controlled.

Search control block 166 of Figure 5 is detailed in Figure 13. As mentioned previously, channel element microprocessor 136 specifies a search parameter set including the group of antennas to search over as stored in antenna select buffer 348, the starting offset as stored in search offset buffer 308, the number of rake elements per search rake as stored in rake width buffer 312, the width of the search window as stored in search width buffer 314, the number of Walsh symbols to accumulate as stored in Walsh

symbol accumulation buffer 316, and a control word as stored in control word buffer 346.

The starting offset stored in search offset buffer 308 is specified with eighth chip resolution. The starting offset controls which samples are removed by decimation by latch 218 of Figure 10 in searcher front end 174. Due to the two Walsh symbol wide antenna sample buffer 172 in this embodiment, the largest value of the starting offset is half of a PN chip less than two full Walsh symbols.

Up until this point, the generic configuration to perform a search has been disclosed. In reality there are several classes of predefined searches. When a mobile unit initially attempts to access the system, it sends a beacon signal called a preamble using the Walsh zero symbol. Walsh zero symbol is the Walsh symbol which contains all logical zeros instead of half ones and zeroes as described above. When a preamble search is performed, the searcher looks for mobile units sending a Walsh zero symbol beacon signal on an access channel. The search result for a preamble search is the energy for the Walsh zero symbol. When an acquisition mode access channel search is performed, max detect 160 outputs the energy for Walsh zero symbol regardless of the maximum output energy detected. The control word stored in control word buffer 346 includes a preamble bit which indicates when a preamble search is being performed.

As discussed above, the power control mechanism of the preferred embodiment measures the signal level received from each mobile unit and creates a power control indication to command the mobile unit to raise or lower the mobile unit's transmit power. The power control mechanism operates over a set of Walsh symbols called a power control group during traffic channel operation. (Traffic channel operation follows access channel operation and implies operation during an active call.) All the Walsh symbols within a single power control group are transmitted using the same power control indication command at the mobile unit.

Also as described above, in the preferred embodiment of the present invention, the signal transmitted by the mobile unit is of a variable rate during traffic channel operation. The rate used by the remote unit to transmit the data is unknown at the base station during the searching process. As the consecutive symbols are accumulated, it is imperative that the transmitter is not gated off during the accumulation. Consecutive Walsh symbols in a power control group are gated as a group meaning that the 6 Walsh symbols comprising a power control group in the preferred embodiment are all gated on or all gated off.

Thus when the search parameter specifies that a plurality of Walsh symbols be accumulated during traffic channel operation, the searching process must align each search rake to begin and end within a single power control group. The control word stored in control word buffer 346 includes a power control group alignment bit. With the power control group alignment bit set to one indicating a traffic channel search, the searching process synchronizes to the next power control group boundary instead of just the next offset Walsh symbol boundary.

The control word stored in control word buffer 346 also includes the peak detection filter enable bit as discussed earlier in conjunction with Figure 8.

The searcher operates either in continuous or single step mode, according to the setting of the continuous/single step bit of the control word. In single step mode, after a search is performed, integrated search processor 128 returns to an idle state to await further instructions. In continuous mode, integrated search processor 128 is always searching, and by the time channel element microprocessor 136 is signaled that the results are available, integrated search processor 128 has started the next search.

Search control block 166 produces the timing signals used to control the searching process performed by integrated search processor 128. Search control block 166 sends the zero offset timing reference to short code I and Q PN generators 202, 206 and long code User PN generator 204, and the enable signal to decimator latch 218 and the select signal to MUX 216 in searcher front end 174. It provides the read and write addresses for PN sequence buffer 176 and even and odd Walsh chip buffers 168 and 170. It outputs the current offset to control the operation of despreader 178. It provides the intra-time slice timing reference for FHT processor engine 120, and determines whether the searching process or the demodulation process uses FHT processor engine 120 by controlling FHT input MUX 124. It provides several pipeline delayed versions of certain internal timing strobes to search result processor control logic 254 of Figure 12 to allow it to sum search results across a rake of offsets for a number of Walsh symbol accumulations. Search control block 166 provides best result register 250 with the pipelined offset and antenna information corresponding to accumulated energy in best result register 250.

In Figure 13, system time count 342 is slaved to the zero offset time reference. In the preferred embodiment as previously detailed, the system clock runs at eight times the PN chip rate. There are 256 PN chips in a Walsh symbol, and 6 Walsh symbols in a power control group for a total

of 6 X 256 X 8 = 12,288 system clocks per power control group. Therefore in the preferred embodiment, system time count 342 is comprised of a fourteen bit counter that counts the 12,288 system clocks. System time count 342 is slaved to zero offset time reference strobe for the base station. The input reference for short code I and Q PN generators 202, 206 and long code User PN generator 204 of Figure 10 in searcher front end 174 is taken from system time count 342. (Long code User PN generator 204 output is also based on a longer system wide reference which does not repeat for approximately 50 days. The longer system wide reference is not controlled by the searching process and acts as a preset value. The continuing operation based on the preset value is controlled by system time count 342.) The addresses for PN sequence buffer 176 and even and odd Walsh chip buffers 168 and 170 are taken from system time count 342. System time count 342 is latched by latch 328 at the beginning of each time slice. The output of latch 328 is selected via address Mux's 330, 332, and 334 which provide the write addresses corresponding to the current time slice when these buffers are written at some latter time within the time slice.

Offset accumulator 310 keeps track of the offset of the rake element currently being processed. The starting offset as stored in search offset buffer 308 is loaded into offset accumulator 310 at the beginning of each search window. Offset accumulator 310 is decremented with each rake element. At the end of each search rake that is to be repeated for further accumulations, the number of rake elements per search rake as stored in rake width buffer 312 is added back to the offset accumulator to reference it back to the first offset in the search rake. In this way, the searching process again sweeps across the same search rake for another Walsh symbol accumulation. If the searching process has swept across the current search rake on its final Walsh symbol accumulation then offset accumulator 310 is decremented by one by selection of the "-1" input of repeat rake MUX 304 which produces the offset of the first rake element in the next search rake.

The output of offset accumulator 310 always represents the offset of the current rake element being processed and thus is used to control data input to despreader 178. The output of offset accumulator 310 is added by adders 336 and 338 to the intra-time slice timing output of system time count 342 to generate the address sequence within a time slice corresponding to a rake element. The output of adders 336 and 338 is selected via address MUX's 330 and 332 to provide antenna sample buffer 172 read addresses.

The output of offset accumulator 310 is also compared by comparator 326 with the output of system time count 342 to form the offset

Walsh symbol strobe which indicates that antenna sample buffer 172 has sufficient valid data for the searching process to begin.

Search rake count 320 keeps track of the number of rake elements remaining to be processed in the current search rake. Search rake count 320 is loaded with the width of the search window as stored in search width buffer 314 at the beginning of a search window. Search rake count 320 is incremented after the processing of the final Walsh symbol accumulation of each search rake is complete. When it reaches its terminal count all offsets in the search window have been processed. To provide a indication that the end of the current search window is imminent, the output of search rake count 320 is summed by summer 324 with the output of rake width buffer 312. The end of the search window indication marks the time at which antenna sample buffer 172 may begin to be filled with data samples from an alternative antenna in preparation for the next search window without disrupting the contents needed for the current search window.

When channel element microprocessor 136 specifies a search window, it can specify that the search window be performed for a plurality of antennas. In such a case, the identical search window parameters are repeated using samples from a series of antennas. Such a group of search windows is called an antenna search set. If an antenna search set is specified by channel element microprocessor 136, the antenna set is programmed by the value stored in antenna select buffer 348. After the completion of an antenna search set, channel element microprocessor 136 is alerted.

Rake element count 318 contains the number of rake elements left to process in the current search rake. Rake element count 318 is incremented once for each rake element processed and is loaded with the output of rake width buffer 312 when the searcher is in the idle state or upon completion of a search rake.

Walsh symbol accumulation count 322 counts the number of Walsh symbols left to accumulate for the current search rake. The counter is loaded with the number of Walsh symbols to accumulate as stored in Walsh symbol accumulation buffer 316 when the searcher is in the idle state or after completing a search rake sweep on the final Walsh symbol accumulation. Otherwise the counter is incremented with the completion of each search rake.

Input valid count 302 is loaded whenever the input antenna or decimator alignment changes. It is loaded with the minimum number of samples the searcher needs to process a search rake based on the output of rake width buffer 312 (i.e. one Walsh symbol plus one rake width worth of

samples). Each time an antenna sample is written to antenna sample buffer 172, input valid count 302 is incremented. When it reaches its terminal count, it sends an enable signal that allows the searching process to begin. Input valid count 302 also provides the mechanism for holding off the search processing when the offsets of successive search windows do not allow continuous processing of data.

The searcher operates in either an idle state, a sync state, or an active state. Searcher sequencing control 350 maintains the current state. Integrated search processor 128 initializes to the idle state when a reset is applied to channel element modem 110. During the idle state, all counters and accumulators in search control block 166 load their associated search parameters as presented above. Once channel element microprocessor 136 commands the searching process to begin a continuous or a single step search via the control word, integrated search processor 128 moves to the sync state.

In the sync state, the searcher is always waiting for an offset Walsh symbol boundary. If the data in antenna sample buffer 172 isn't valid yet, or if the power control group alignment bit is set and the Walsh symbol is not a power control group boundary, then integrated search processor 128 remains in the sync state until the proper conditions are met on a subsequent offset Walsh symbol boundary. With a properly enabled offset Walsh symbol, the searcher can move to the active state.

Integrated search processor 128 stays in the active state until it has processed a search rake, at which time it normally returns to the sync state. If integrated search processor 128 is in single step mode, it can go from the active state to the idle state after completing the last rake element for the final Walsh symbol accumulation for the last search rake in the search window. Integrated search processor 128 then waits for channel element microprocessor 136 to initiate another search. If instead, integrated search processor 128 is in continuous mode then at this point it loads the new search parameter set and returns to the sync state to await the offset Walsh symbol at the initial offset to be processed in the new search. The active state is the only state in which the antenna data samples are processed. In the idle or sync states the searcher simply keeps track of time with system time count 342 and continues to write into the PN sequence buffer 176 and antenna sample buffer 172 so that when the searcher does move to the active state these buffers are ready to be used.

Figure 14 is an enlarged view of the first Walsh symbol accumulation of the second search rake in a search window such as search rake 196 shown in Figure 9. The third Walsh symbol as referenced to the zero offset reference

system time clock is shown divided into thirty-two time slices. Searcher state 372 changes from sync to active with the offset Walsh symbol boundary indication signals that antenna sample buffer 172 ready with valid samples to process at that offset. During the next available time slice, the first rake element of the search rake is processed. The searcher continues to use each time slice to process a rack element as indicated by an "S" in time slices 374 unless demod front end 122 uses the FHT processor engine **120** as indicated by an "D" in time slices 374. The searcher finishes processing every rake element in the rake and returns to the sync state before the next offset Walsh symbol boundary. Also shown is search rake count state 362 being incremented during the active state until it reaches the terminal state, indicating the complete search rake has been processed. Offset count state 364 is shown being incremented between each time slice corresponding to a rake element, so that it may be used to derive the sample buffer offset read address during the time slice. Offset count state 364 is pipelined delayed to produce offset count for Intermediate result register 164. The offset count 368 is incremented on the final Walsh symbol accumulation 370 pass.

Thus, a single integrated searcher processor, by buffering antenna samples and utilizing a time sliced transform processor, can independently sequence through a search as configured by a search parameter set, analyze the results and present a summary report of the best paths to use for demodulation element reassignment. This reduces the searcher related workload of the microprocessor so that a less expensive microprocessor can be used, and also reduces the direct IC costs by allowing a complete channel element modem on a single IC.

The general principles described herein can be used in systems using alternative transmission schemes. The discussion above was based on the reception of a reverse link signal where no pilot signal is available. On the forward link of the preferred embodiment, the base station transmits a pilot signal. The pilot signal is a signal having known data thus the FHT process used to determine which data was transmitted is not necessary. In order to embody the present invention, a integrated search processor for receiving a signal comprising a pilot signal would not contain the FHT processor or maximum detection function. For example FHT processor engine 120 and max detect 160 blocks of Figure 5 could be replaced with simple accumulator 125 as shown in Figure 15. The searching operation when a pilot signal is available is analogous to an acquisition mode access channel search operation as described above.

There are many configurations for spread spectrum multiple access communication systems not specifically described herein but with which the present invention is applicable. For example, other encoding and decoding means could be used instead of the Walsh encoding and FHT decoding.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WE CLAIM:

CLAIMS

1. An integrated search processor receiving a signal comprised of a group of spread spectrum modulated call signals sharing a common frequency band, said integrated search processor comprising:

a sample buffer for storing a limited number of data samples of said group of spread spectrum modulated call signals wherein each of said spread spectrum modulated call signals comprises a series of bits encoded in groups of a fixed length into a series of symbols having a transmission rate and wherein said data samples are stored at a rate corresponding to said transmission rate;

a PN sequence buffer for storing a limited number of PN sequence data chips wherein said PN sequence data chips correspond to a PN sequence used to modulate at least one call signal in said group of spread spectrum modulated call signals;

a despreader for correlating a portion of said data samples of said group of spread spectrum call signals stored in said sample buffer with a portion of said PN sequence data chips stored in said PN sequence buffer and for producing a correlated output corresponding to a single symbol; and

a transform engine for decoding said correlated output to produce an estimate of said series of bits wherein said transform engine decodes said correlated output at a rate higher than said transmission rate.

2. The integrated search processor of claim 1, wherein said sample buffer is capable of storing two symbols worth of said data samples and wherein said PN sequence buffer is capable of storing four symbols worth of said PN sequence data chips.

3. The integrated search processor of claim 1, wherein each symbol in said series of symbols is comprised of a series of code bits and wherein, in said at least one call signal, each of said code bits is modulated by a plurality of said PN sequence data chips and wherein said limited number of data samples stored in said sample buffer are stored such that two of said data samples are stored for each of said PN sequence data chips.

4. The integrated search processor of claim 1, wherein said estimate of said series of bits comprises a probability corresponding to each possible value of said groups of said fixed length, further comprising a maximum detector for receiving said estimate and providing a soft decision

output value indicative of a maximum energy level of said correlated output.

5. The integrated search processor of claim 1, wherein said rate at which said transform engine decodes said correlated output is 32 times higher than said transmission rate.

6. The integrated search processor of claim 1 further comprising a demodulation element for producing despread call data wherein said transform engine decodes said despread call data.

7. The integrated search processor of claim 1 wherein said series of bits are Walsh encoded in said groups of said fixed length.

8. The integrated search processor of claim 7 wherein said transform engine is a fast Hadamard transformer.

9. The integrated search processor of claim 4 further comprising an accumulator for summing successive ones of said soft decision output values.

10. The integrated search processor of claim 1 further comprising a search controller for providing signaling information.

11. The integrated search processor of claim 9 wherein a plurality of said series of symbols are grouped into a power control group wherein each symbol in said power control group has a common transmitted power level.

12. The integrated search processor of claim 11 wherein said accumulator sums said soft decision output values corresponding to symbols having a common power control group.

13. The integrated search processor of claim 1 wherein said despreader produces said correlated output at said rate higher than said transmission rate and wherein each of said correlated outputs corresponds to a time delay offset from a zero offset reference time

14. The integrated search processor of claim 10 wherein said sample buffer is comprised of an even and an odd sample buffer wherein if the previous data sample is stored in said even sample buffer then the subsequent data sample is stored in said odd sample buffer and if the previous data sample is stored in said odd sample buffer then the subsequent data sample is stored in said even sample buffer.

15. The integrated search processor of claim 1 wherein each symbol in said series of symbols is comprised of a series of code bits and wherein, in said at least one call signal, each of said code bits is modulated by four of said PN sequence data chips and wherein said limited number of data samples stored in said sample buffer are stored such that two of said data samples are stored for each of said PN sequence data chips, and wherein each sample is four bits.

16. A method of receiving a signal comprised of a group of spread spectrum call signals sharing a common frequency band in a modem operating under control of a modem microprocessor, and isolating one of said call signals from among said group to determine a call signal strength at a path delay time offset from a zero offset reference time, said method comprising the steps of:

storing PN sequence data bits in a PN sequence buffer;

storing a first received set of call signal samples in a sample buffer having a limited size;

despreading a first fixed length set of said call signal samples from said sample buffer corresponding to a first path delay time with a first set of PN sequence data bits from said PN sequence buffer to produce a first despread output;

storing a second received set of call signal samples in said sample buffer; and

despreading a second fixed length set of call signal samples from said sample buffer corresponding to a second path delay time with said first set of PN sequence data bits from said PN sequence buffer to produce a second despread output;

wherein said second fixed length set of call signal samples comprises a large number of the same call signal samples as said first fixed length set of call signal samples and wherein the length of said first and second received set of call signal samples is a fraction the fixed length of said first and second fixed length set of call signal samples.

17. The method of claim 16 for receiving and isolating one of said call signals from among said group of call signals wherein the step of despreading said first fixed length set of call signal samples from said sample buffer is conditioned upon there being a sufficient number of valid call signal samples available in said sample buffer to evaluate said signal strength at said first path delay time.

18. The method of claim 16 for receiving and isolating one of said call signals from among said group of call signals further comprising the step of selecting an antenna from a plurality of available antennas to supply said call signal samples.

19. The method of claim 16 for receiving and isolating one of said call signals from among said group of call signals further comprising the steps of:

storing a third received set of call signal samples in said sample buffer;

despreading a third fixed length set of call signal samples from said sample buffer corresponding to a third path delay time with a second set of PN sequence data bits from said PN sequence buffer to produce a third despread output;

storing a fourth received set of call signal samples in said sample buffer; and

despreading a fourth fixed length set of call signal samples from said sample buffer corresponding to a fourth path delay time with said second set of PN sequence data bits from said PN sequence buffer to produce a fourth despread output;

wherein said fourth fixed length set of call signal samples comprises a large number of the same call signal samples as said third fixed length set of call signal samples and wherein the length of said third and fourth received set of call signal samples is a fraction of the fixed length of said first and second fixed length set of call signal samples.

20. The method of claim 19 for receiving and isolating one of said call signals from among said group of call signals further comprising the steps of:

determining a first call signal strength corresponding to said first despread output;

determining a second call signal strength corresponding to said second despread output;

determining a third call signal strength corresponding to said third despread output; and

determining a fourth call signal strength corresponding to said fourth despread output.

21. The method of claim 20 for receiving and isolating one of said call signals from among said group of call signals further comprising the steps of:

summing said first call signal strength and said third call signal strength; and

summing said second call signal strength and said fourth call signal strength;

wherein said first path delay time is the same as said third path delay time and wherein said second path delay time is the same as said fourth path delay time.

22. The method of claim 21 for receiving and isolating one of said call signals from among said group of call signals further comprising the step of providing a largest summed result to said modem microprocessor.

23. The method of claim 20 for receiving and isolating one of said call signals from among said group of call signals wherein said step of determining said first call signal strength comprises the step of decoding said first despread output using a fast Hadamard transform to produce soft decision data.

24. The method of claim 16 for receiving and isolating one of said call signals from among said group of call signals wherein each of said spread spectrum modulated call signals comprises a series of bits encoded in groups of a fixed length into a series of symbols comprised of a series of code bits.

25. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein said series of bits is Walsh encoded and said series of symbols are Walsh symbols.

26. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein each of said code bits of said one isolated call signal are modulated by a plurality of said PN sequence data bits.

27. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein each of said code bits of said one isolated call signal are modulated by four of said PN sequence data bits.

28. The method of claim 27 for receiving and isolating one of said call signals from among said group of call signals wherein two call signal samples are stored in said sample buffer for each PN sequence data bits.

29. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein said limited size of said sample buffer corresponds to two symbols worth of data samples.

30. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein said PN sequence data buffer is capable of storing four symbols worth of PN sequence data bits.

31. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein first fixed length set of call signal samples corresponds to one symbols worth of data.

32. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein first receive set of call signal samples corresponds to 1/32 of a symbol.

33. The method of claim 16 for receiving and isolating one of said call signals from among said group of call signals wherein said in step of storing said first and second receive set of call signal samples, said first and second receive set of call signal samples are stored at the same rate at which call signal samples are transmitted.

34. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals wherein a series of said

symbols are grouped together in a power control group wherein each symbol in a common power control group is transmitted at a fixed power level.

35. The method of claim 24 for receiving and isolating one of said call signals from among said group of call signals further comprising the steps of:

despreading a third fixed length set of call signal samples from said sample buffer corresponding to a third path delay time with a second set of PN sequence data bits from said PN sequence buffer to produce a third despread output;

despreading a fourth fixed length set of call signal samples from said sample buffer corresponding to a fourth path delay time with said second set of PN sequence data bits from said PN sequence buffer to produce a fourth despread output;

wherein said fourth fixed length set of call signal samples comprises a large number of the same call signal samples as said third fixed length set of call signal samples;

determining a first call signal strength corresponding to said first despread output;

determining a second call signal strength corresponding to said second despread output;

determining a third call signal strength corresponding to said third despread output;

determining a fourth call signal strength corresponding to said fourth despread output.

summing said first call signal strength and said third call signal strength; and

summing said second call signal strength and said fourth call signal strength;

wherein said first path delay time is the same as said third path delay time and wherein said second path delay time is the same as said fourth path delay time and wherein said first fixed length set of call signal samples and third fixed length set of call signal samples correspond to a common power control group.

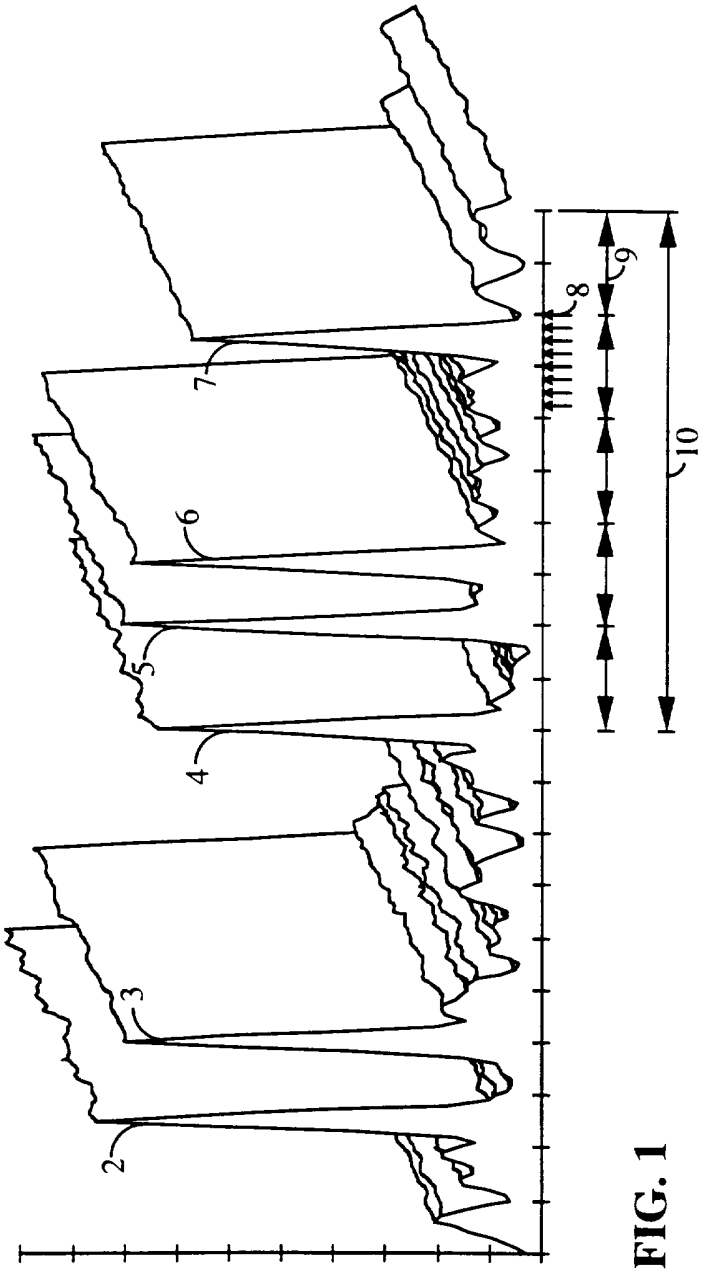

FIG. 1

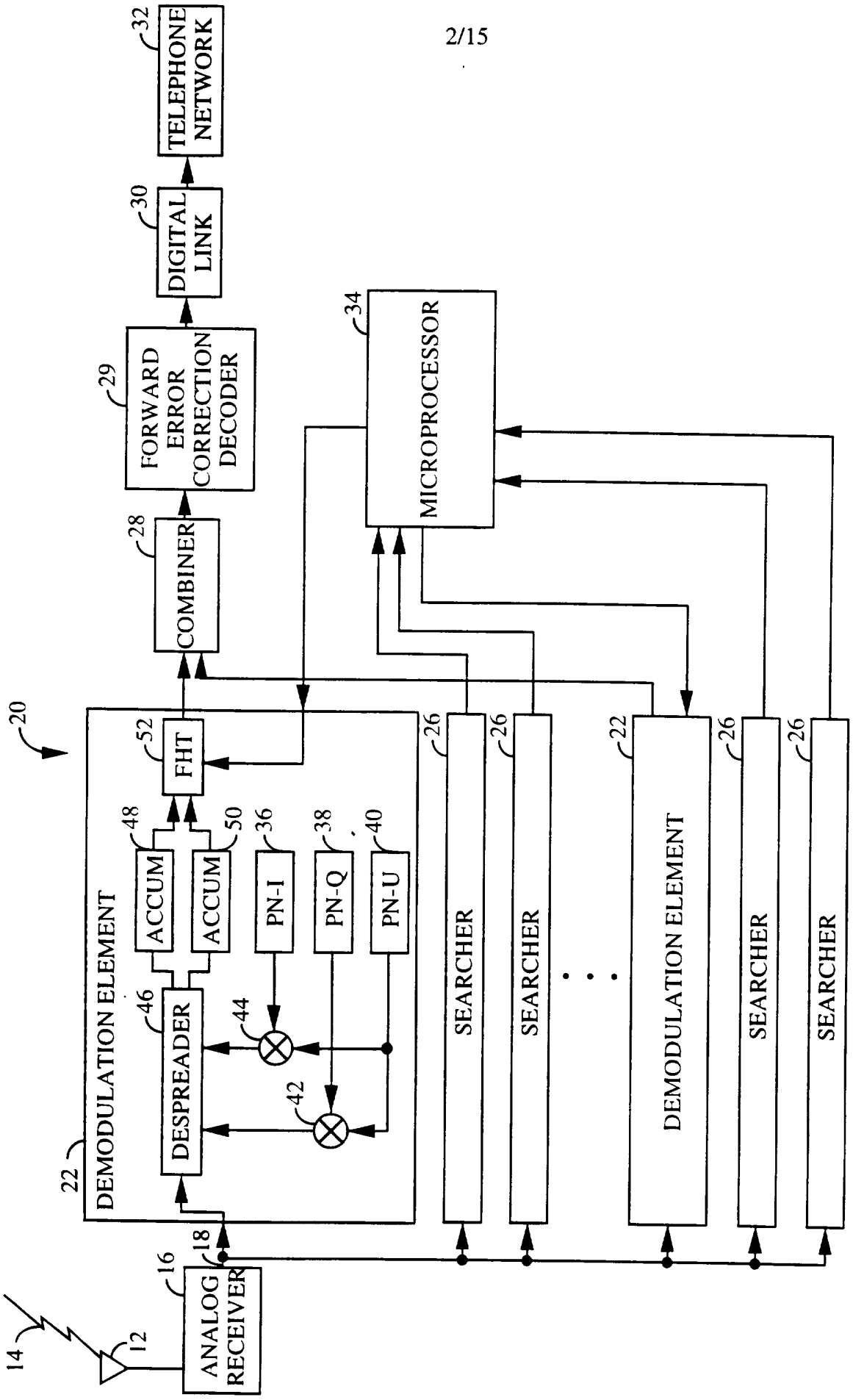
14
12
ANALOG RECEIVER
16
18
20
DEMODULATION ELEMENT
22
DESPREADER
46
ACCUM
48
ACCUM
50
FHT
52
PN-I
36
PN-Q
38
PN-U
40
44
42
SEARCHER
26
SEARCHER
26
DEMODULATION ELEMENT
22
SEARCHER
26
SEARCHER
26
COMBINER
28
FORWARD ERROR CORRECTION DECODER
29
DIGITAL LINK
30
TELEPHONE NETWORK
32
MICROPROCESSOR
34

FIG. 2

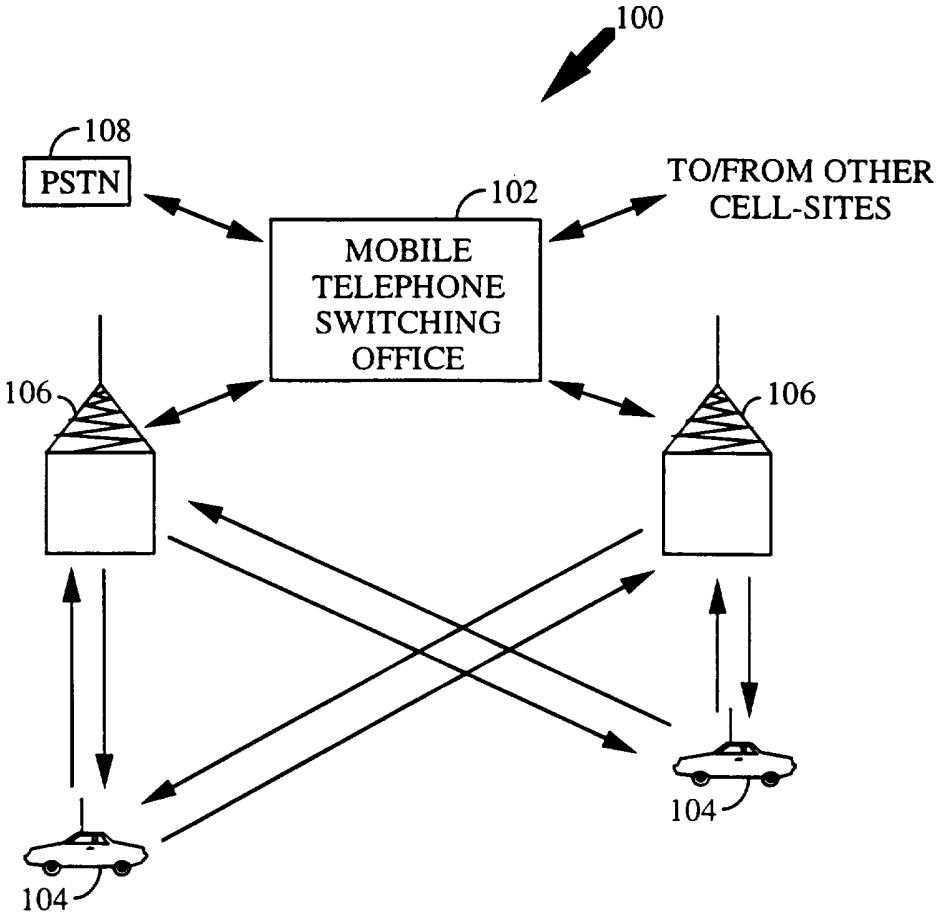
100
108
PSTN
102
TO/FROM OTHER
CELL-SITES
MOBILE
TELEPHONE
SWITCHING
OFFICE
106
106
104
104

FIG. 3

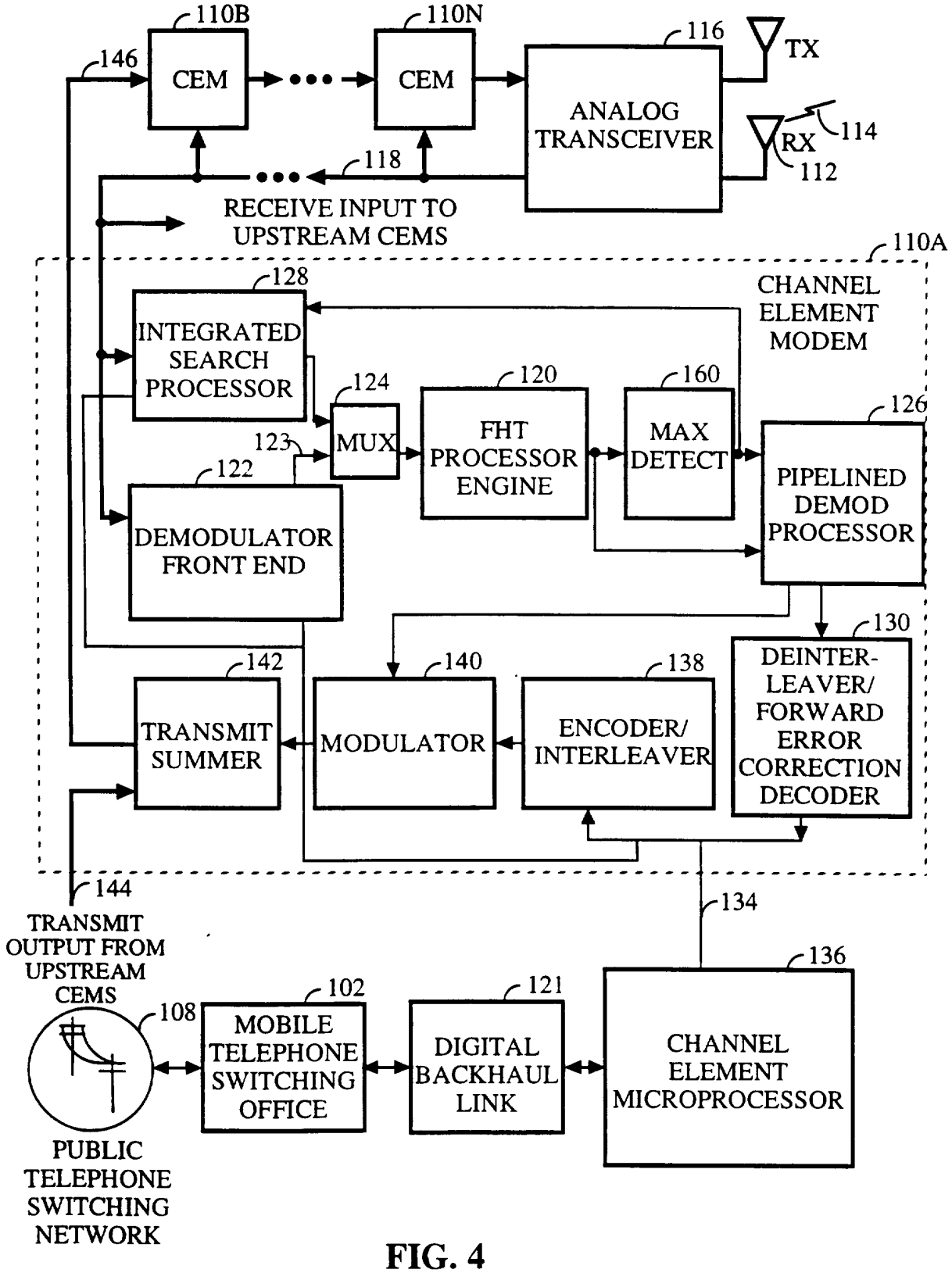
110B
110N
146
CEM
CEM
116
TX
ANALOG TRANSCEIVER
RX
114
112
118
RECEIVE INPUT TO UPSTREAM CEMS
110A
CHANNEL ELEMENT MODEM
128
INTEGRATED SEARCH PROCESSOR
124
120
160
126
123
MUX
FHT PROCESSOR ENGINE
MAX DETECT
PIPELINED DEMOD PROCESSOR
122
DEMODULATOR FRONT END
130
142
140
138
DEINTER-LEAVER/ FORWARD ERROR CORRECTION DECODER
TRANSMIT SUMMER
MODULATOR
ENCODER/ INTERLEAVER
144
134
TRANSMIT OUTPUT FROM UPSTREAM CEMS
136
102
121
108
MOBILE TELEPHONE SWITCHING OFFICE
DIGITAL BACKHAUL LINK
CHANNEL ELEMENT MICROPROCESSOR
PUBLIC TELEPHONE SWITCHING NETWORK

FIG. 4

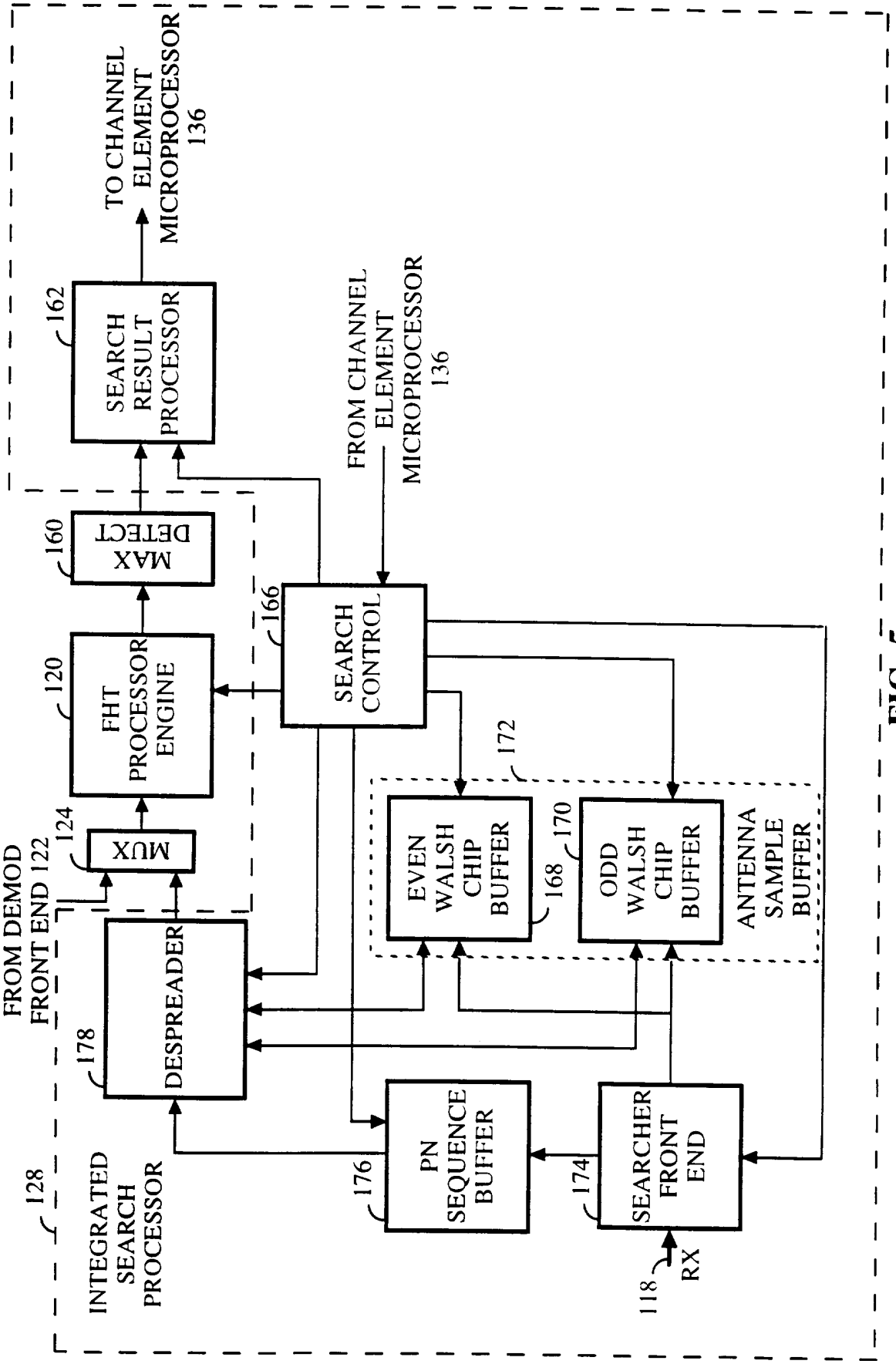
INTEGRATED SEARCH PROCESSOR
128
FROM DEMOD FRONT END
122
MUX
124
DESPREADER
178
FHT PROCESSOR ENGINE
120
MAX DETECT
160
SEARCH RESULT PROCESSOR
162
TO CHANNEL ELEMENT MICROPROCESSOR 136
FROM CHANNEL ELEMENT MICROPROCESSOR 136
SEARCH CONTROL
166
EVEN WALSH CHIP BUFFER
168
ODD WALSH CHIP BUFFER
170
ANTENNA SAMPLE BUFFER
172
PN SEQUENCE BUFFER
176
SEARCHER FRONT END
174
RX
118

FIG. 5

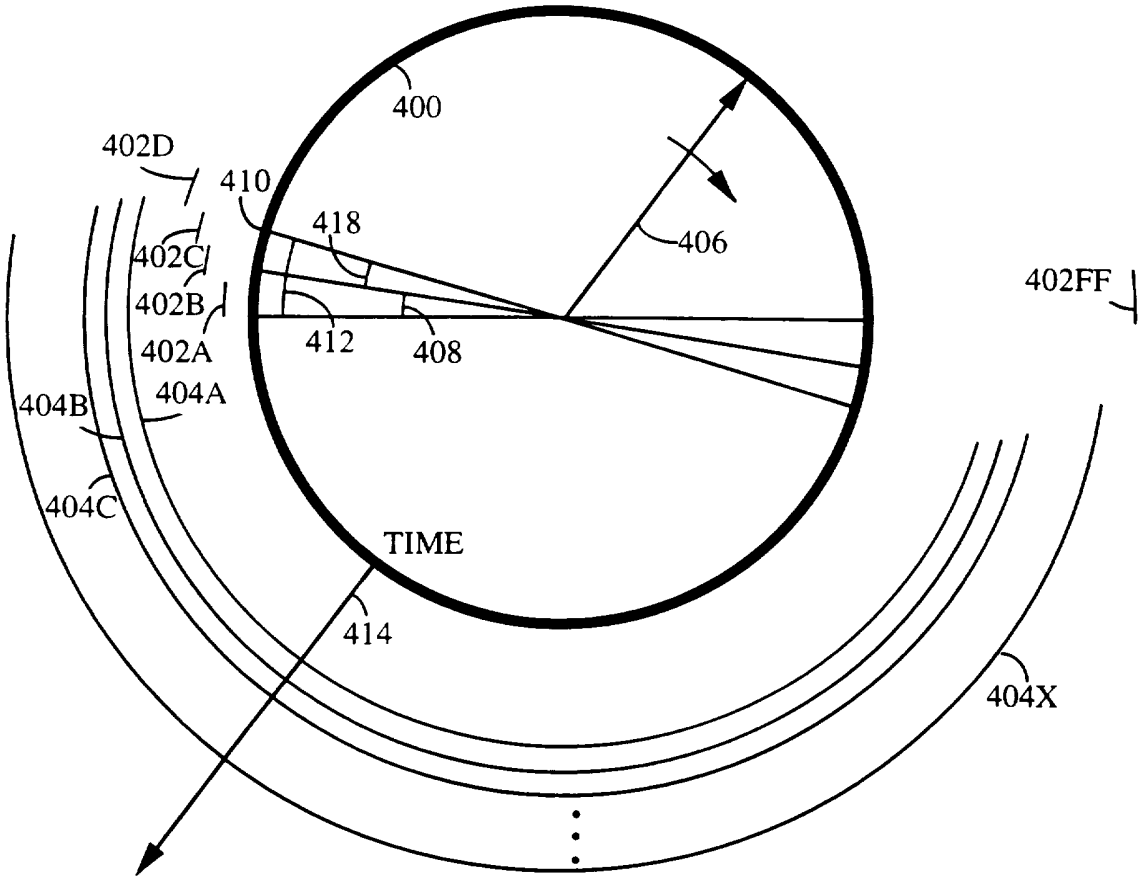
400
402D
410
418
406
402C
402B
402A
412
408
402FF
404B
404A
404C
TIME
414
404X

FIG. 6

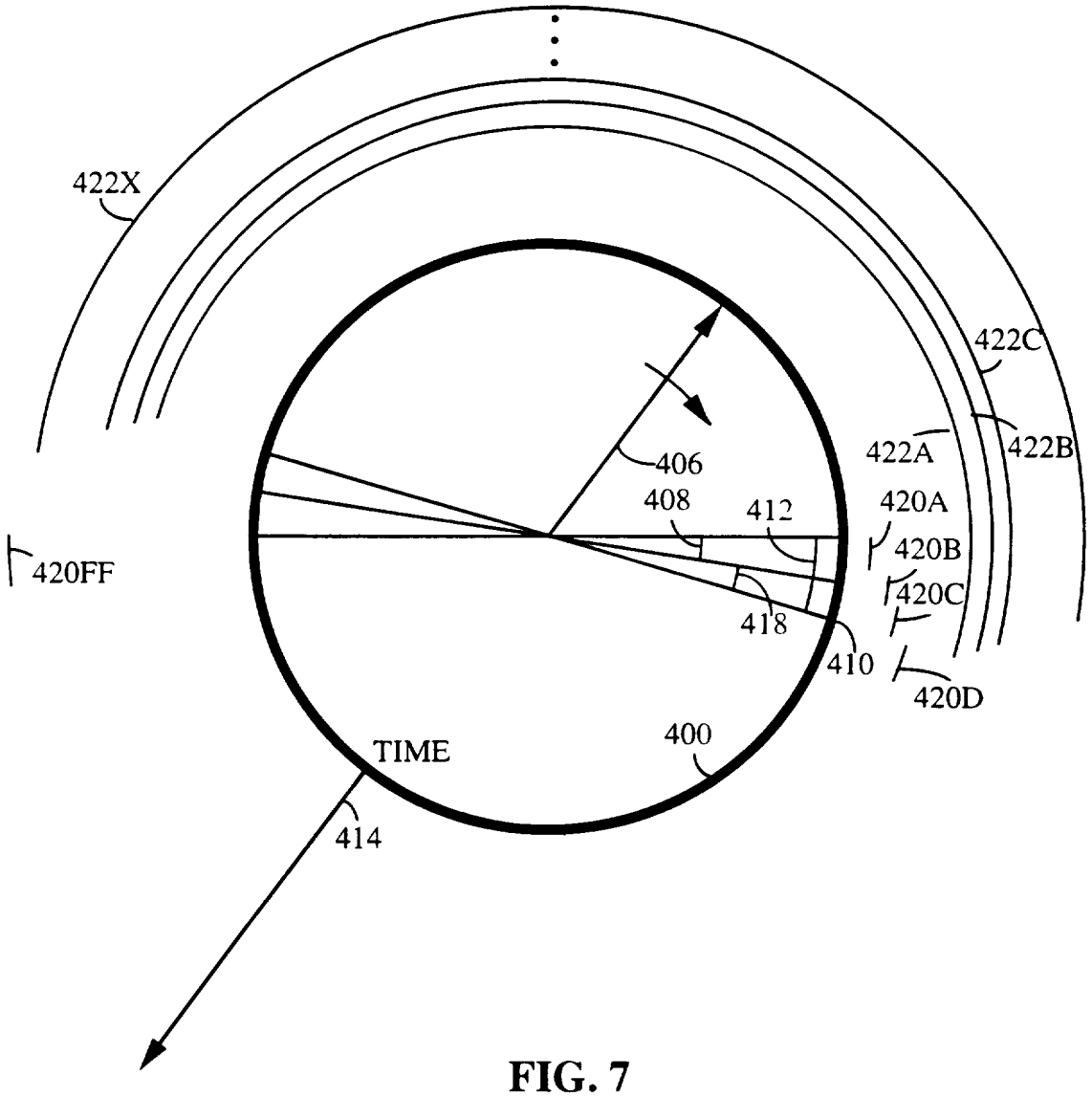
422X
422C
422A
422B
406
408
412
420A
420B
420C
420FF
418
410
420D
400
TIME
414

FIG. 7

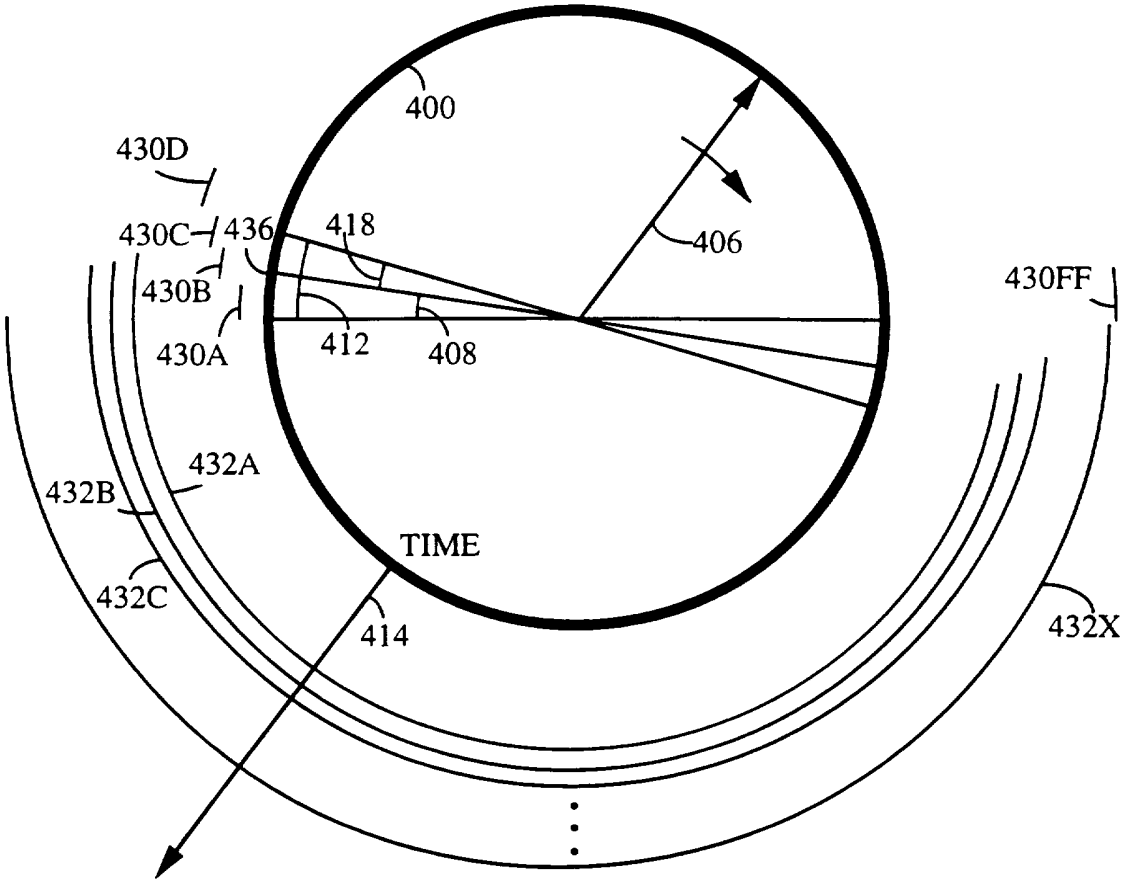
400
430D
430C
436
418
406
430B
430A
412
408
430FF
432A
432B
TIME
432C
414
432X

FIG. 8

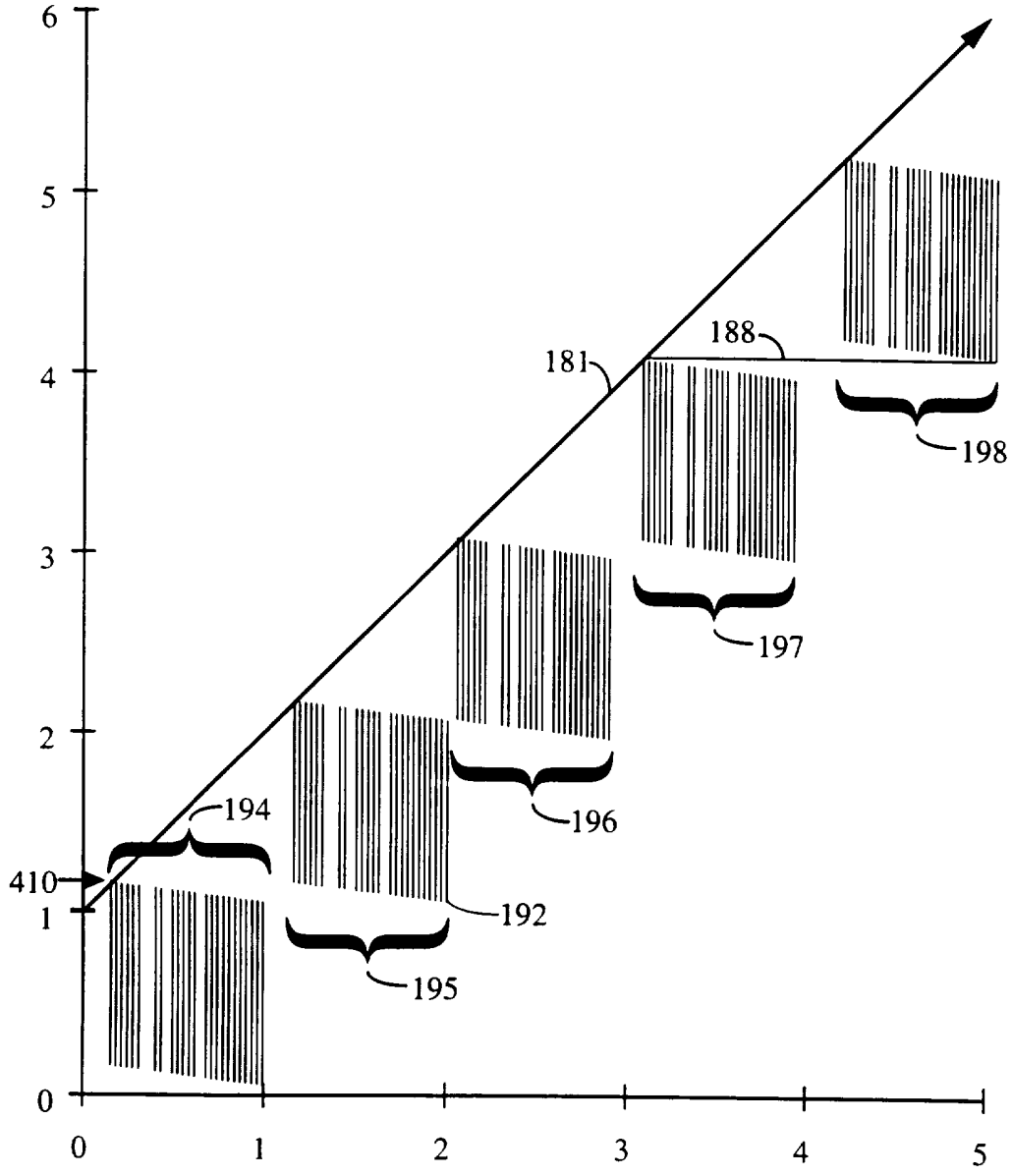

FIG. 9

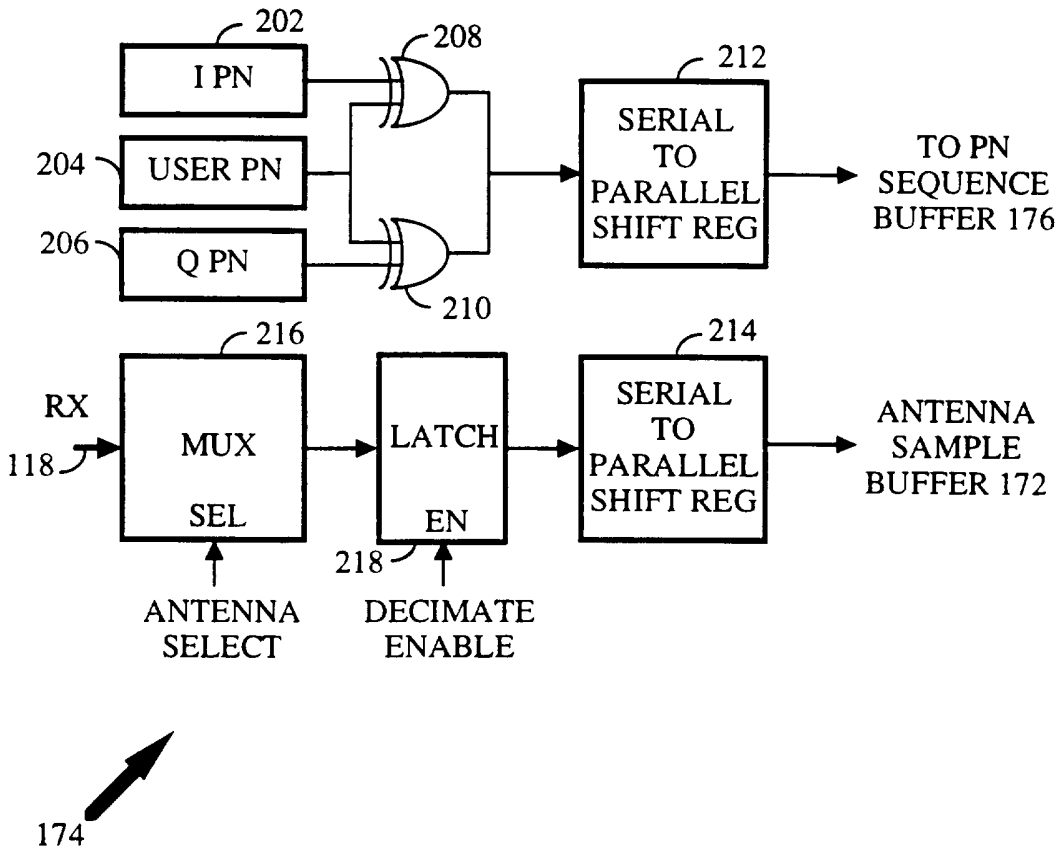
202
I PN
208
212
SERIAL TO PARALLEL SHIFT REG
TO PN SEQUENCE BUFFER 176
204
USER PN
206
Q PN
210
216
214
RX
118
MUX
SEL
LATCH
EN
SERIAL TO PARALLEL SHIFT REG
ANTENNA SAMPLE BUFFER 172
218
ANTENNA SELECT
DECIMATE ENABLE
174

FIG. 10

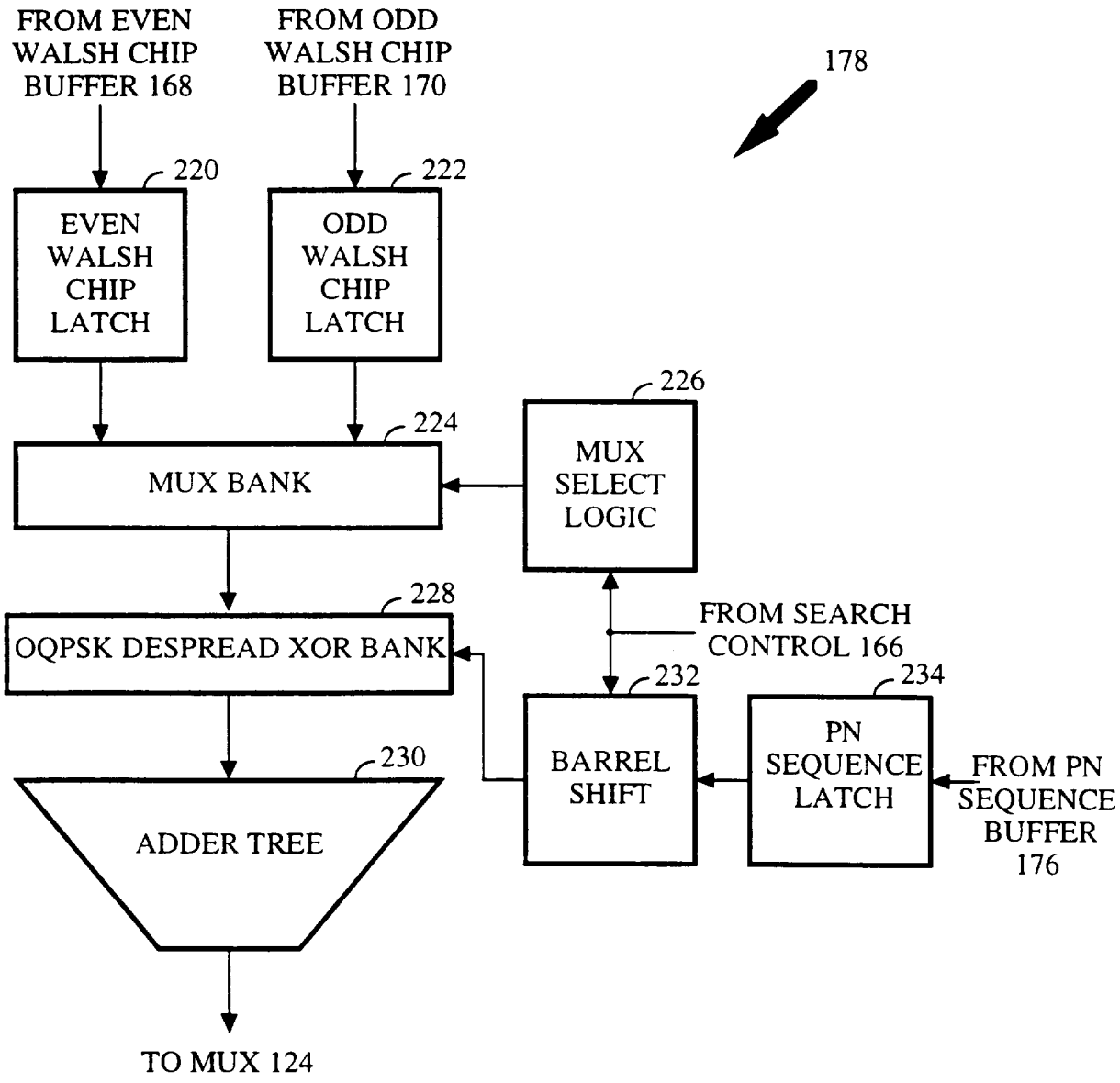
FROM EVEN WALSH CHIP BUFFER 168
FROM ODD WALSH CHIP BUFFER 170
178
220
222
EVEN WALSH CHIP LATCH
ODD WALSH CHIP LATCH
226
224
MUX BANK
MUX SELECT LOGIC
228
OQPSK DESPREAD XOR BANK
FROM SEARCH CONTROL 166
232
234
230
BARREL SHIFT
PN SEQUENCE LATCH
FROM PN SEQUENCE BUFFER 176
ADDER TREE
TO MUX 124

FIG. 11

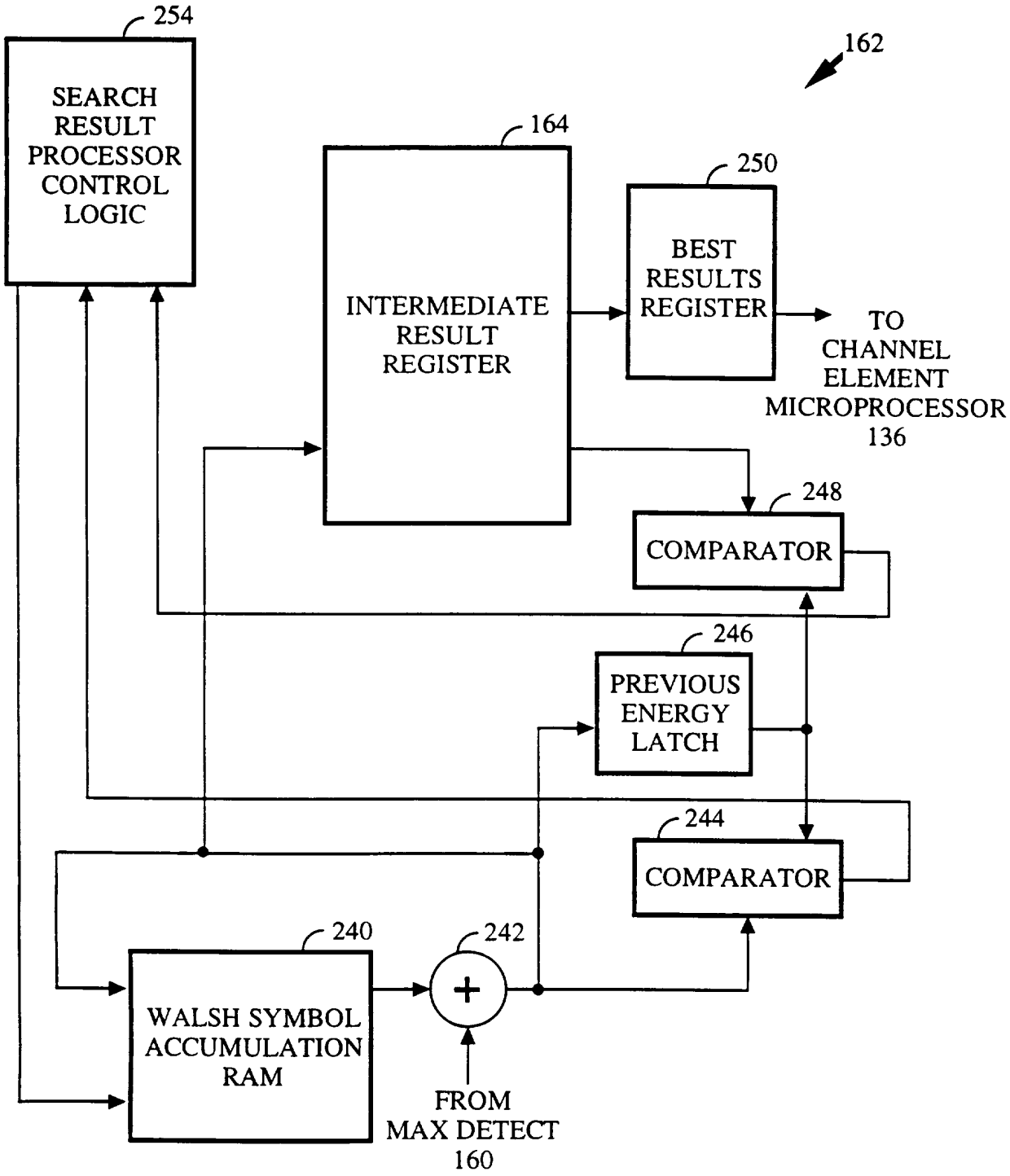
254
SEARCH RESULT PROCESSOR CONTROL LOGIC
162
164
INTERMEDIATE RESULT REGISTER
250
BEST RESULTS REGISTER
TO CHANNEL ELEMENT MICROPROCESSOR 136
248
COMPARATOR
246
PREVIOUS ENERGY LATCH
244
COMPARATOR
240
WALSH SYMBOL ACCUMULATION RAM
242
+
FROM MAX DETECT 160

FIG. 12

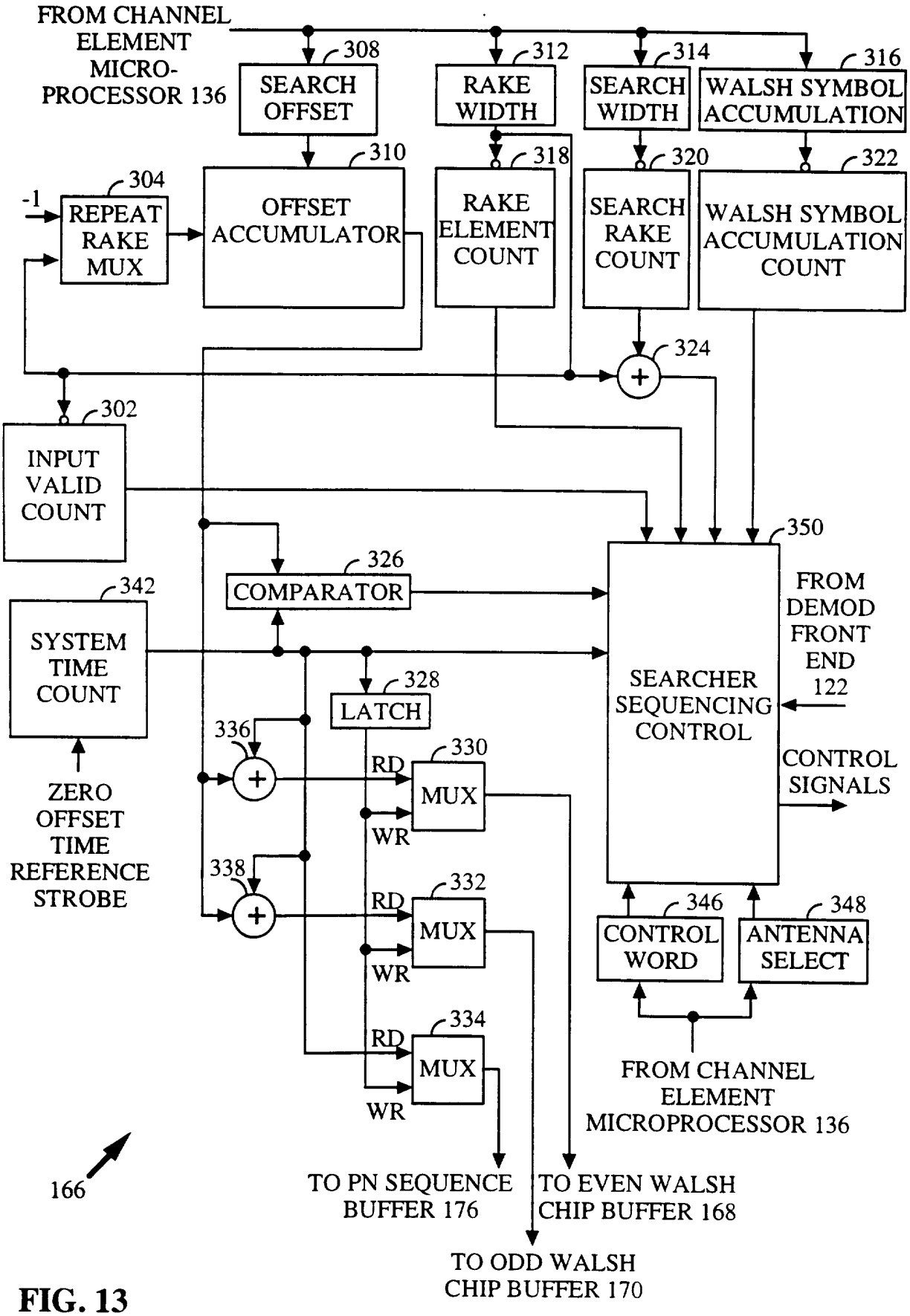
FROM CHANNEL ELEMENT MICRO-PROCESSOR 136
308
SEARCH OFFSET
312
RAKE WIDTH
314
SEARCH WIDTH
316
WALSH SYMBOL ACCUMULATION
310
318
320
322
304
-1
REPEAT RAKE MUX
OFFSET ACCUMULATOR
RAKE ELEMENT COUNT
SEARCH RAKE COUNT
WALSH SYMBOL ACCUMULATION COUNT
324
302
INPUT VALID COUNT
350
326
COMPARATOR
342
SYSTEM TIME COUNT
FROM DEMOD FRONT END 122
328
LATCH
SEARCHER SEQUENCING CONTROL
336
330
RD
MUX
WR
CONTROL SIGNALS
ZERO OFFSET TIME REFERENCE STROBE
338
332
RD
MUX
WR
346
348
CONTROL WORD
ANTENNA SELECT
334
RD
MUX
WR
FROM CHANNEL ELEMENT MICROPROCESSOR 136
166
TO PN SEQUENCE BUFFER 176
TO EVEN WALSH CHIP BUFFER 168
TO ODD WALSH CHIP BUFFER 170

FIG. 13

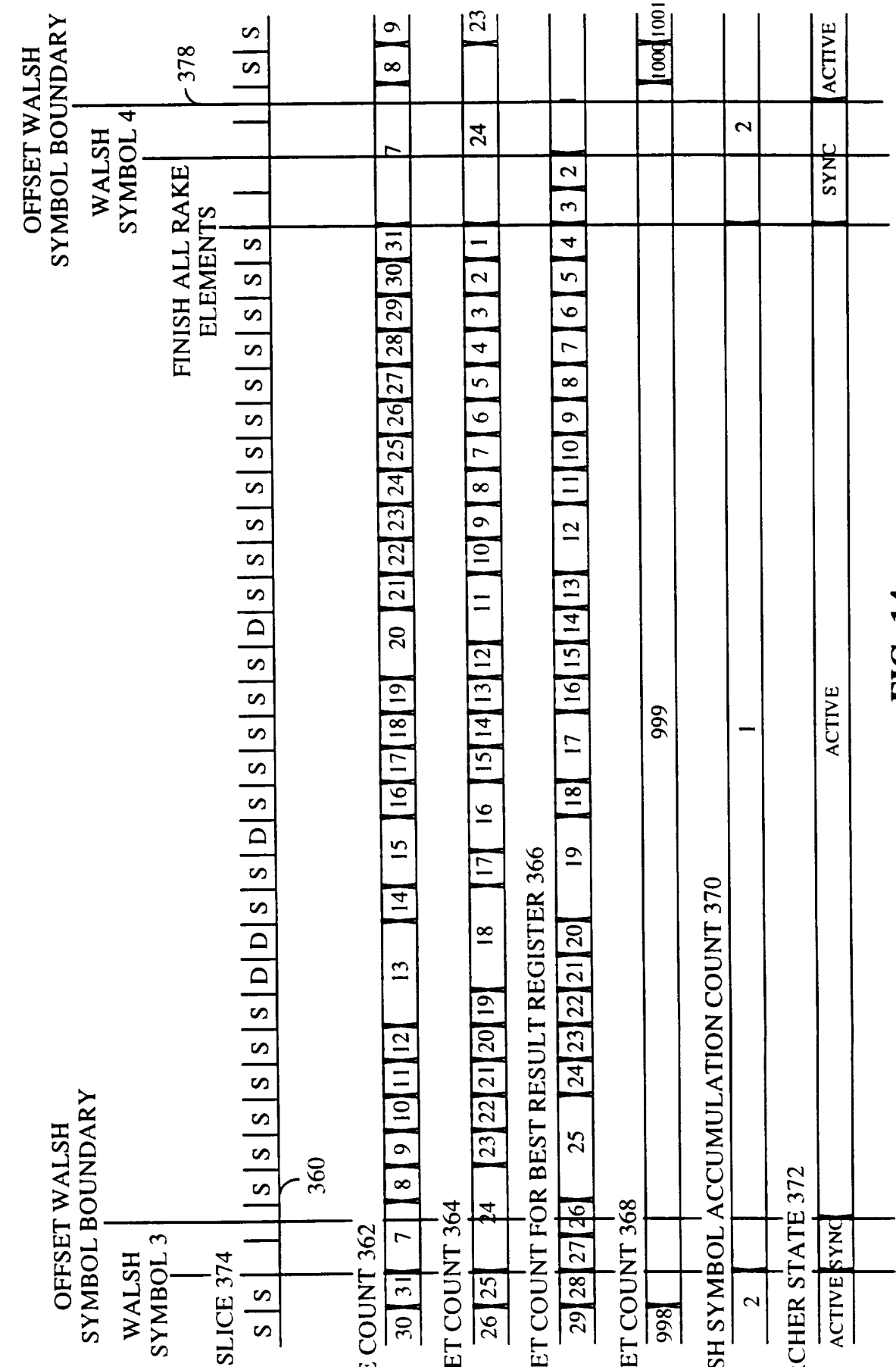
OFFSET WALSH SYMBOL BOUNDARY
WALSH SYMBOL 3
WALSH SYMBOL 4
FINISH ALL RAKE ELEMENTS
378
360
TIME SLICE 374
RAKE COUNT 362
OFFSET COUNT 364
OFFSET COUNT FOR BEST RESULT REGISTER 366
OFFSET COUNT 368
WALSH SYMBOL ACCUMULATION COUNT 370
SEARCHER STATE 372
ACTIVE
SYNC
ACTIVE

FIG. 14

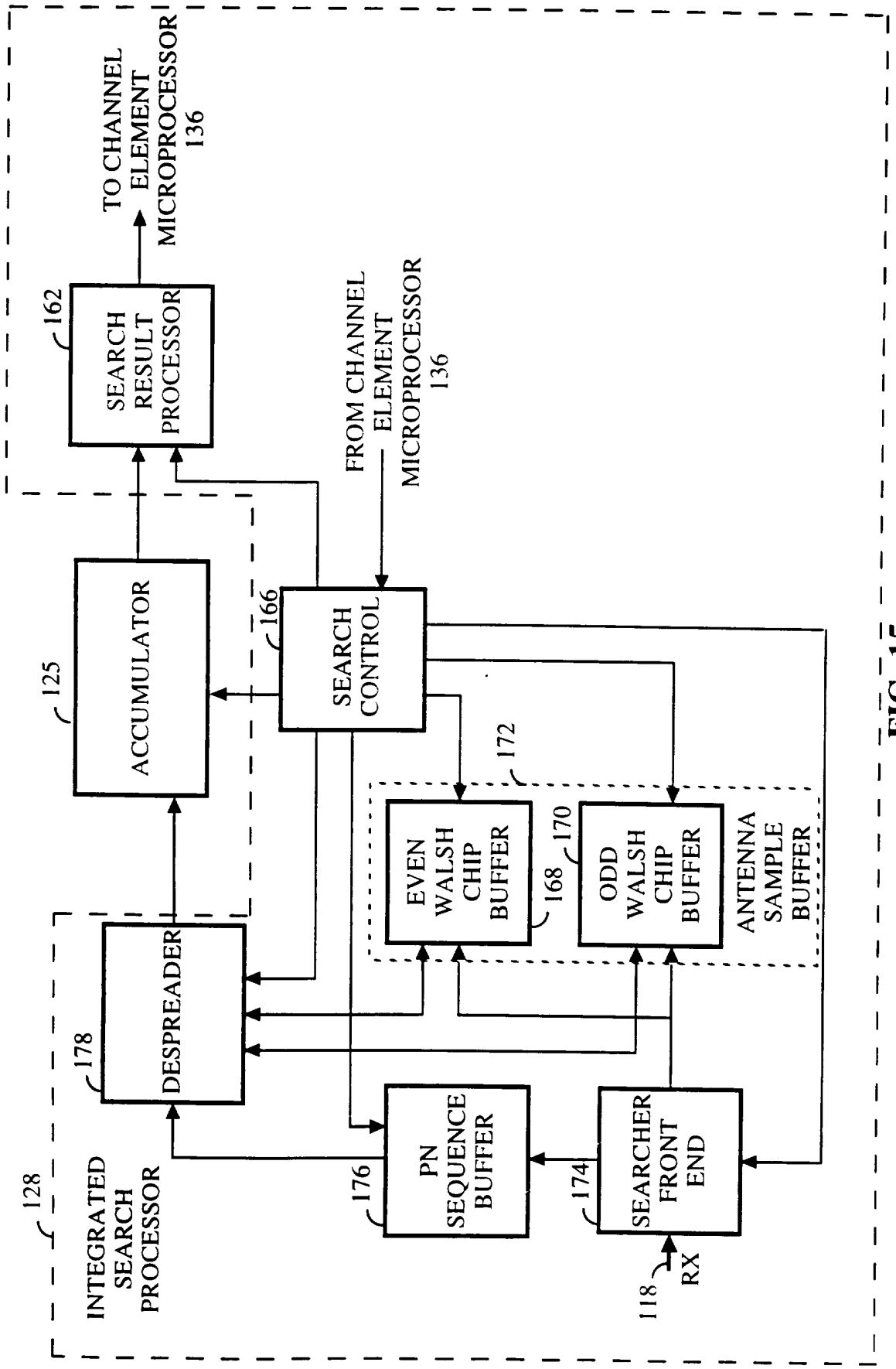
INTEGRATED SEARCH PROCESSOR
128
DESPREADER
178
ACCUMULATOR
125
SEARCH RESULT PROCESSOR
162
TO CHANNEL ELEMENT MICROPROCESSOR 136
FROM CHANNEL ELEMENT MICROPROCESSOR 136
SEARCH CONTROL
166
ANTENNA SAMPLE BUFFER
172
EVEN WALSH CHIP BUFFER
168
ODD WALSH CHIP BUFFER
170
PN SEQUENCE BUFFER
176
SEARCHER FRONT END
174
RX
118

FIG. 15

INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/US 95/12390

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04B H04J G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO,A,91 07036 (QUALCOMM INC) 16 May 1991 cited in the application see page 21, line 17 - page 23, line 33; figure 3 ---	1,7,8, 10,16, 18,23,25
A	US,A,5 329 549 (KAWASAKI KENICHIRO) 12 July 1994 see abstract see column 5, line 32 - line 37 see column 5, line 60 - column 7, line 19; figure 1 --- -/--	1,2,5, 16,29, 32,33

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 1996	08.03.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Bossen, M

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INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/US 95/12390

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 164 628 (REILLY ROBERT A ET AL) 14 August 1979 see column 2, line 4 - line 24 see column 3, line 64 - column 4, line 60; figure 3A -----	1,2,5, 16,29, 32,33

1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat Application No
PCT/US 95/12390

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-9107036	16-05-91	US-A-	5109390	28-04-92
		AU-B-	649987	09-06-94
		AU-B-	6874891	31-05-91
		CA-A-	2072876	08-05-91
		CN-A-	1061311	20-05-92
		EP-A-	0500761	02-09-92
		IL-A-	96220	12-04-94
		JP-T-	4502844	21-05-92
US-A-5329549	12-07-94	JP-A-	6059012	04-03-94
US-A-4164628	14-08-79	DE-A-	2824444	14-12-78
		GB-A-	1560474	06-02-80