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(54) **SEMICONDUCTOR MODULE MANUFACTURING METHOD, ELECTRONIC EQUIPMENT MANUFACTURING METHOD, SEMICONDUCTOR MODULE, AND ELECTRONIC EQUIPMENT**

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(57) **ABSTRACT**

A chip component including a first electrode and a second electrode, a semiconductor device including a first land and a second land, and a printed wiring board are prepared. A first solder paste and a second solder paste are supplied to the printed wiring board. The chip component is placed on the printed wiring board so that the first electrode is in contact with the first solder paste and the second electrode is in contact with the second solder paste. The semiconductor device is placed on the printed wiring board so that the first land faces the first electrode and the second land faces the second electrode. The solder paste is heated and melted, the first land and the first electrode are bonded to each other, and the second land and the second electrode are bonded to each other.

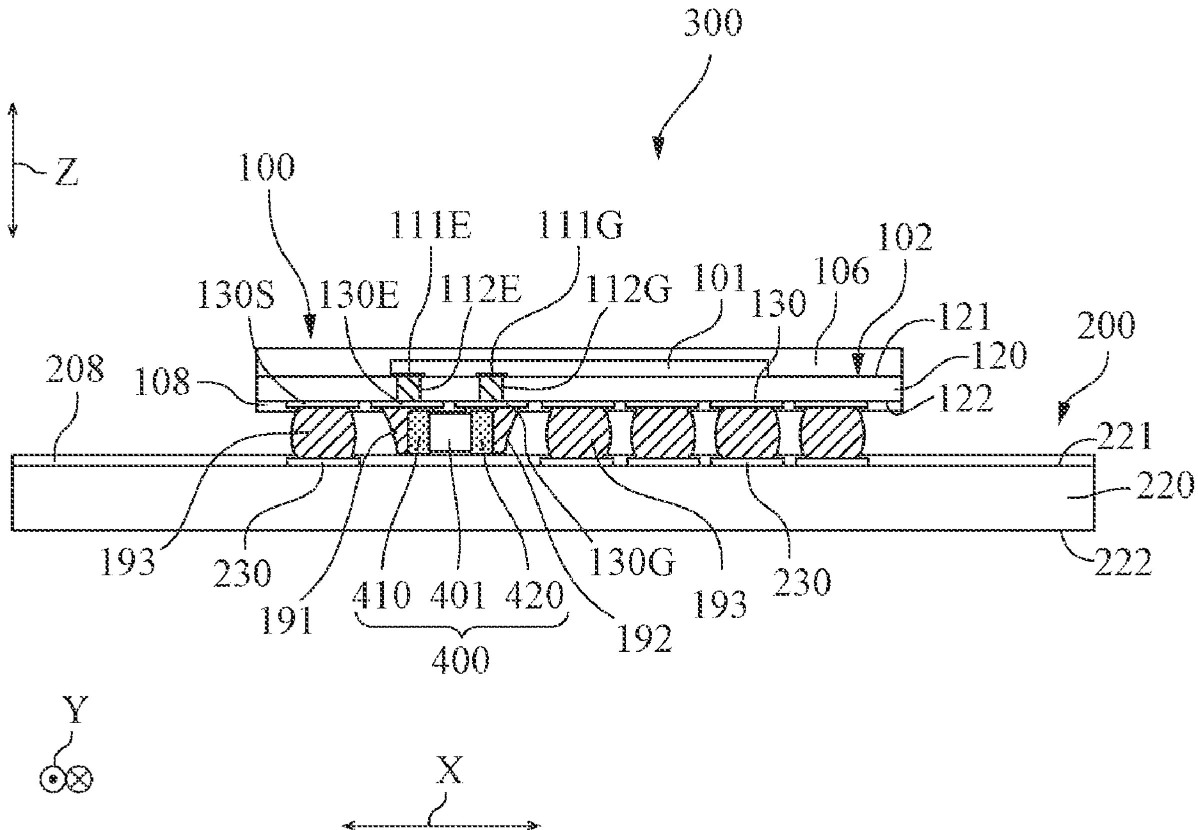


FIG.1

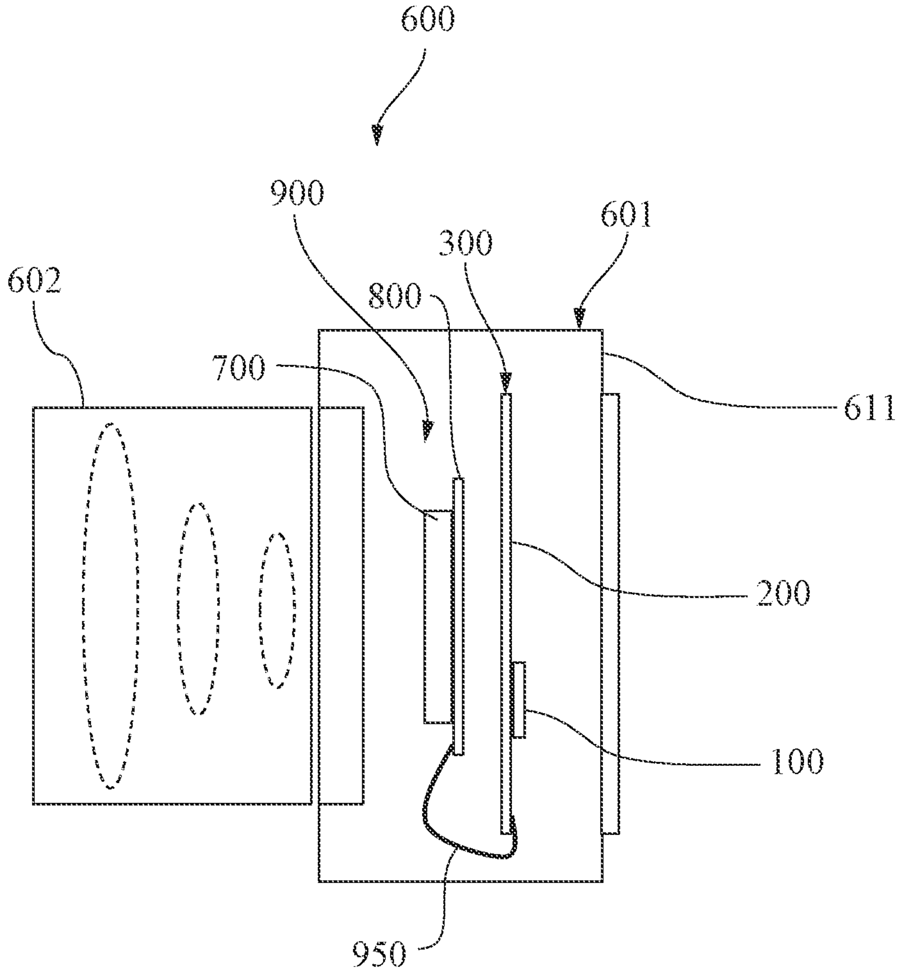


FIG.2A

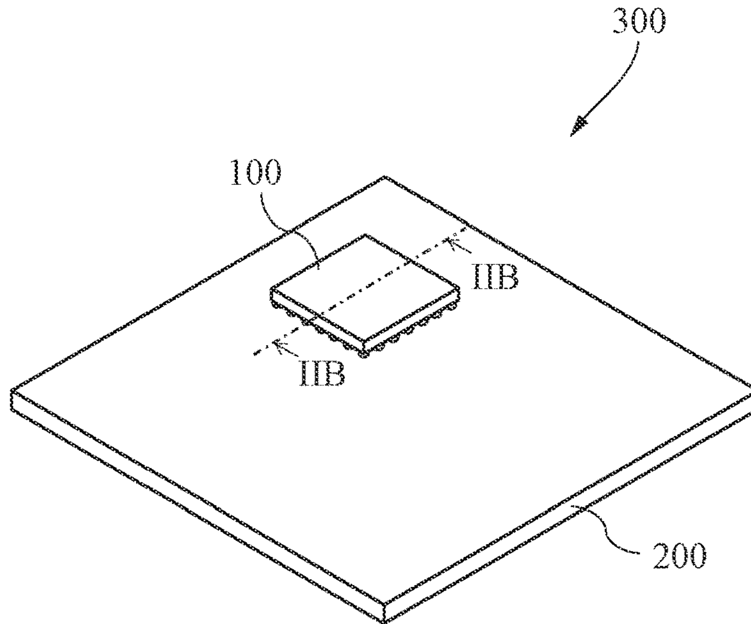


FIG.2B

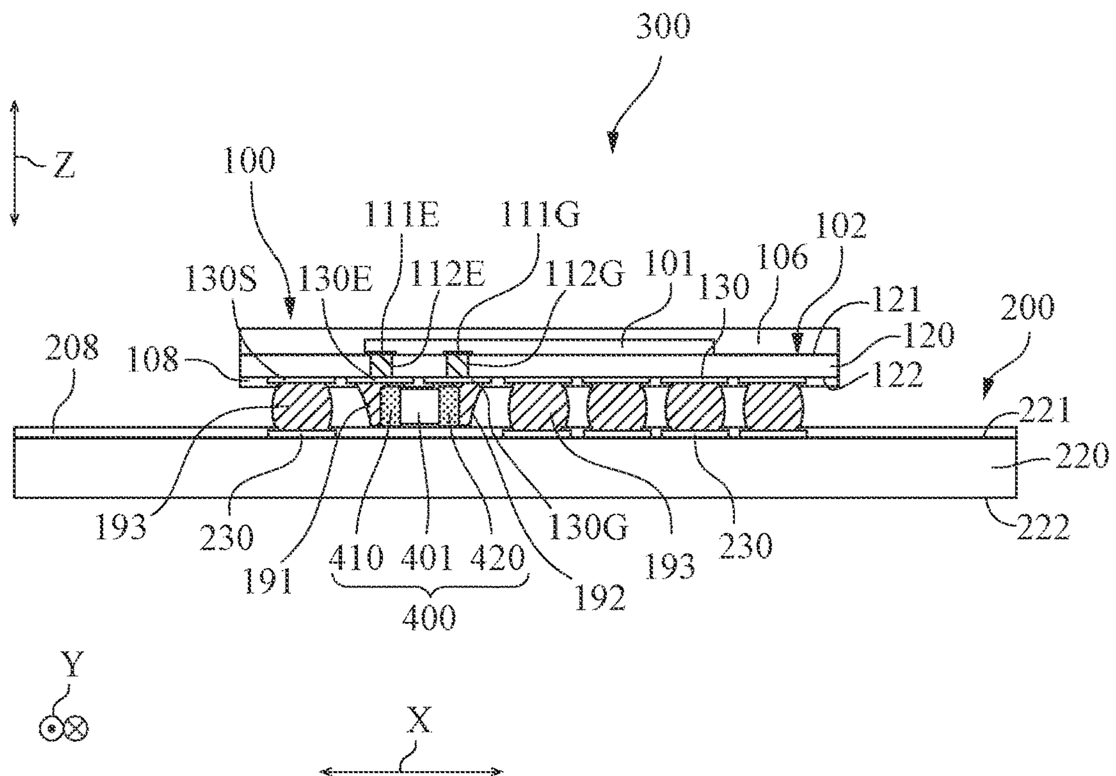


FIG.3

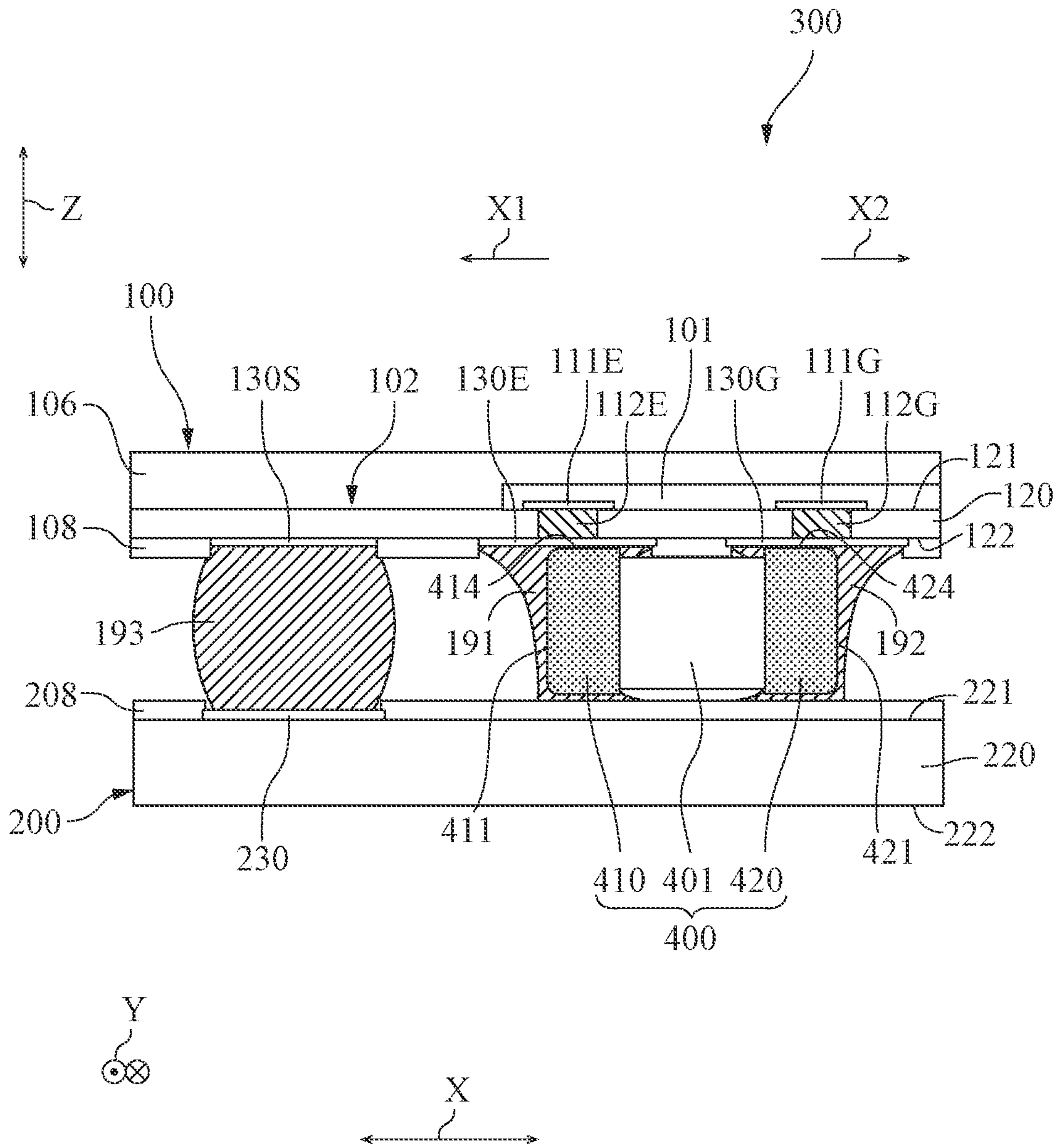


FIG.4A

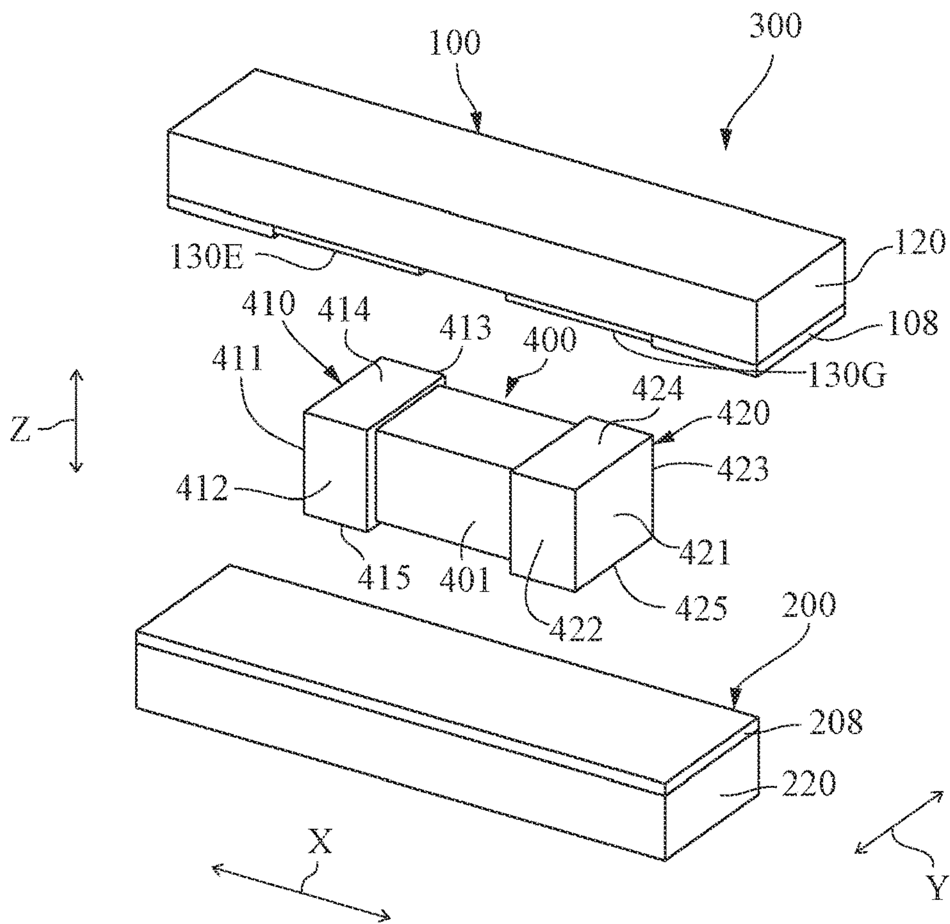


FIG.4B

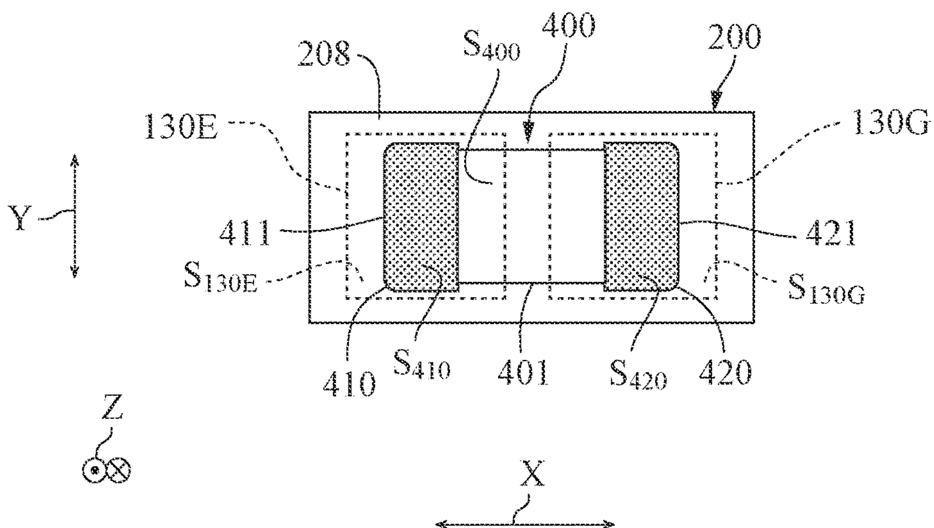


FIG.5A

FIG.5B

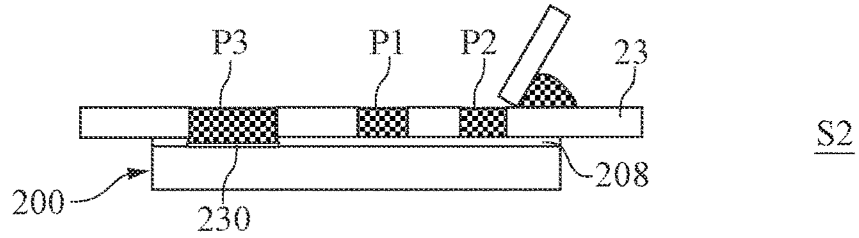


FIG.5C

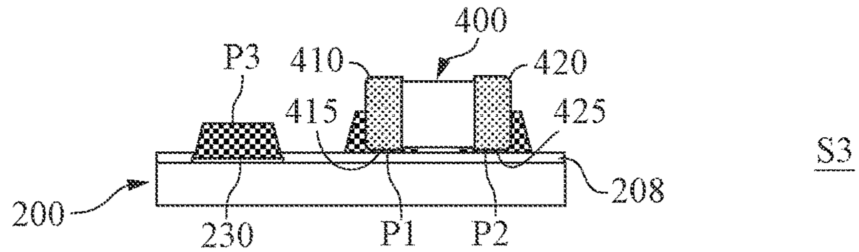


FIG.5D

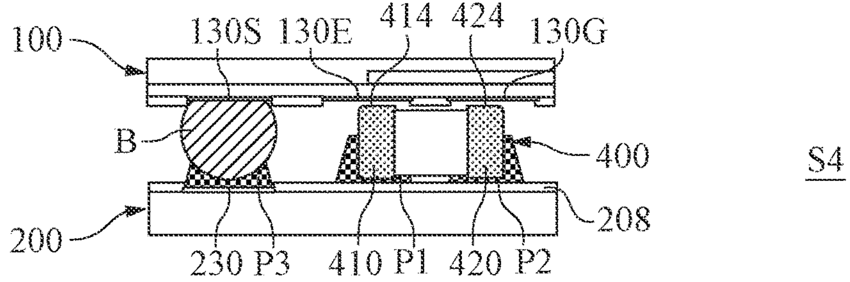


FIG.5E

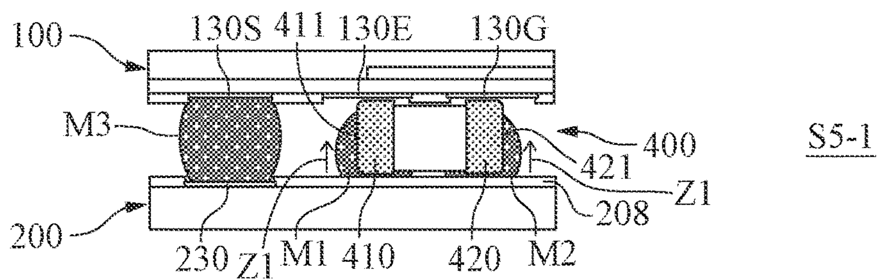


FIG.5F

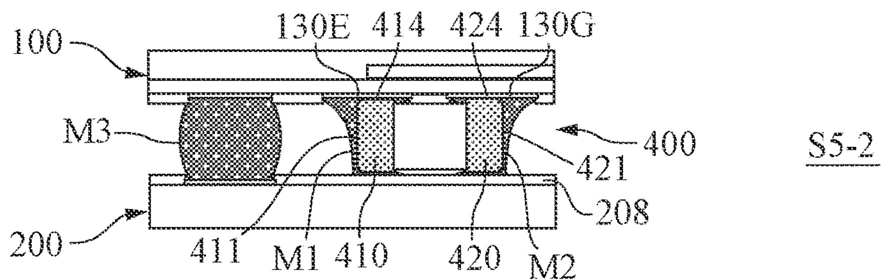


FIG.6

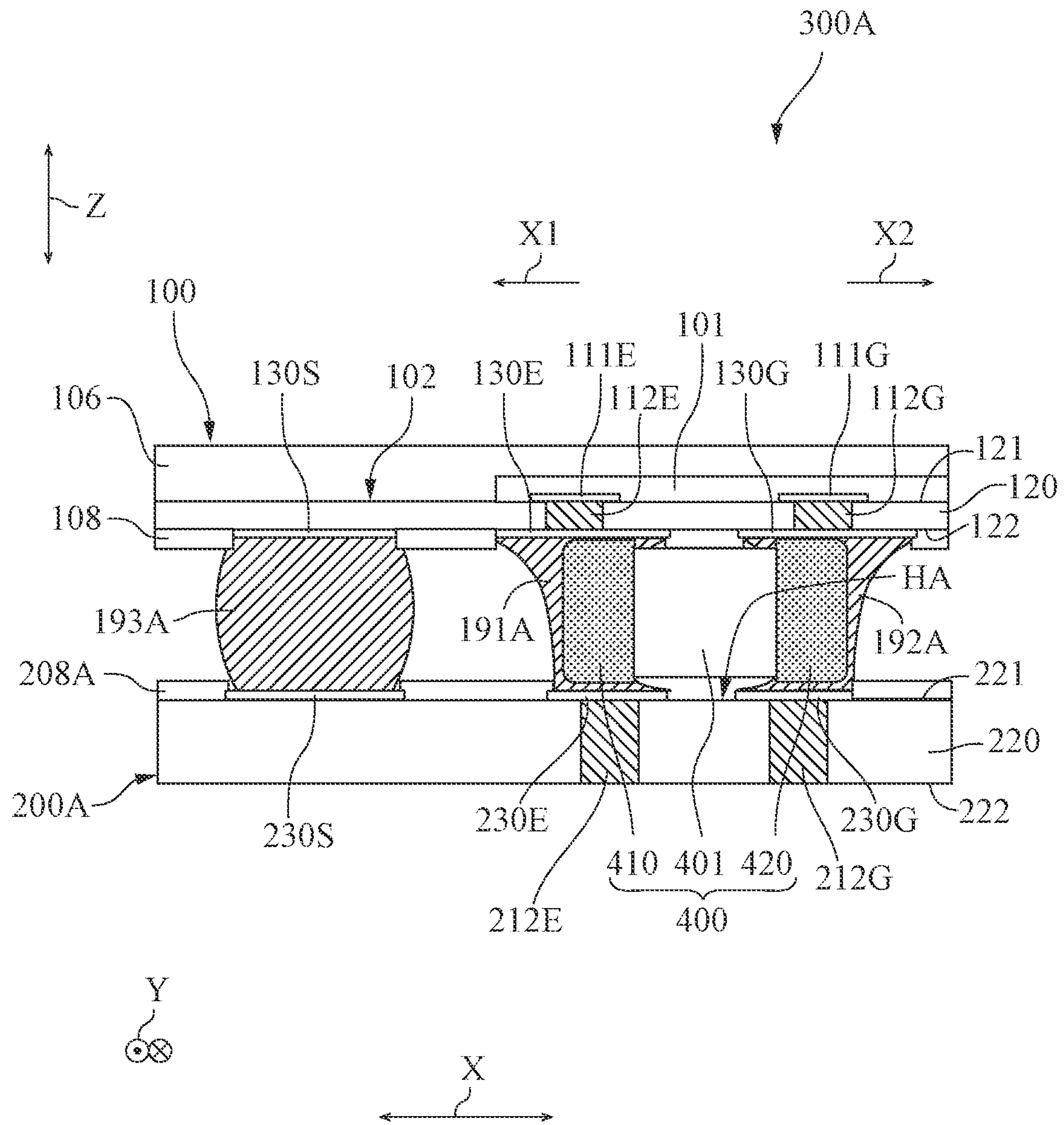


FIG.7A

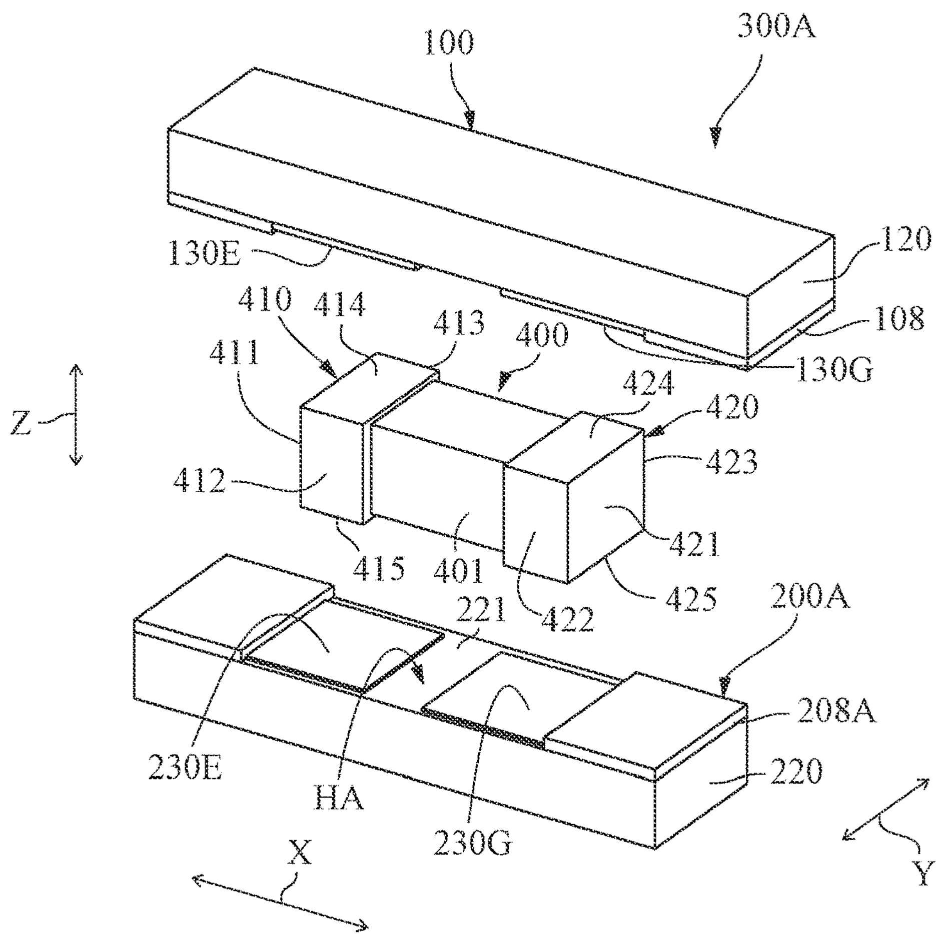


FIG.7B

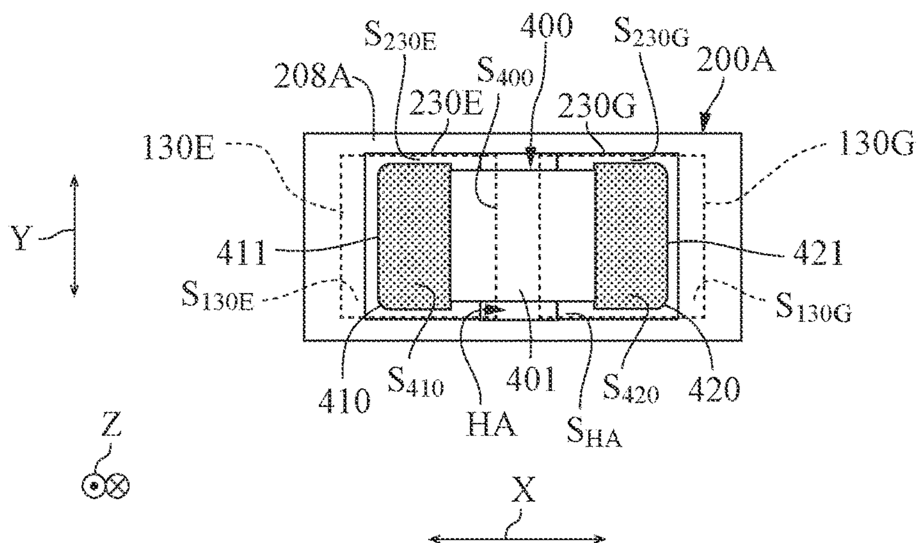


FIG.8A

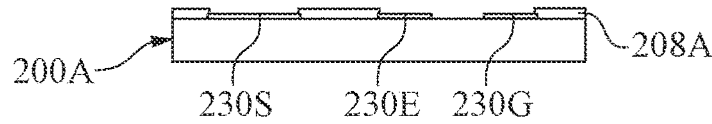


FIG.8B

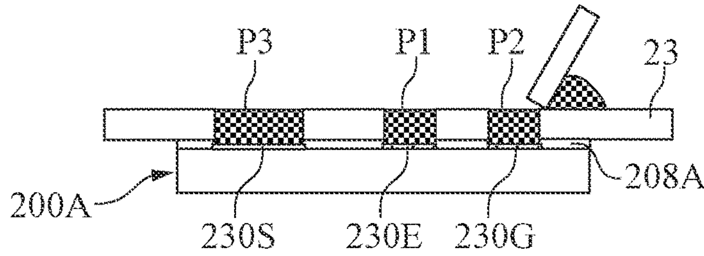


FIG.8C

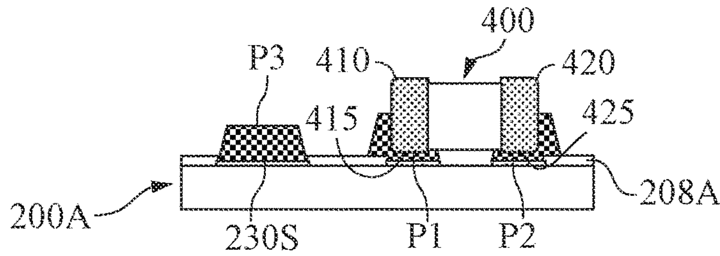


FIG.8D

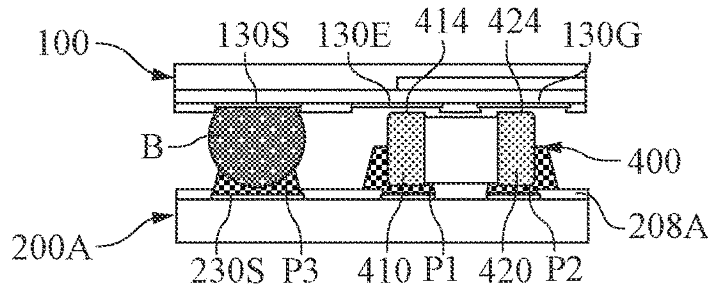


FIG.8E

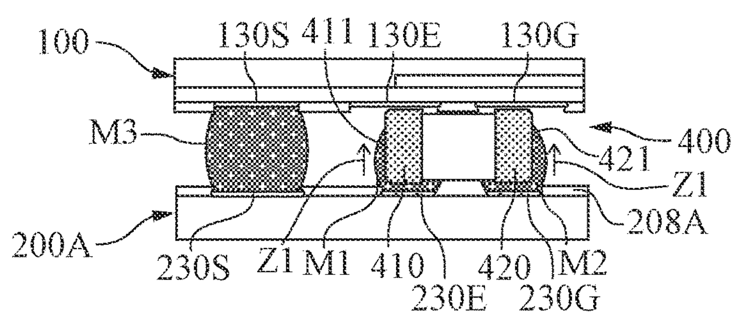


FIG.8F

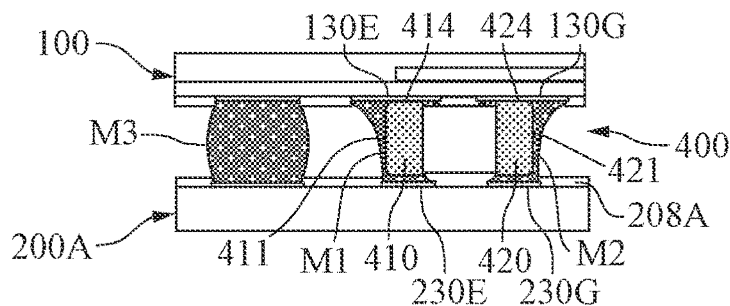


FIG.9

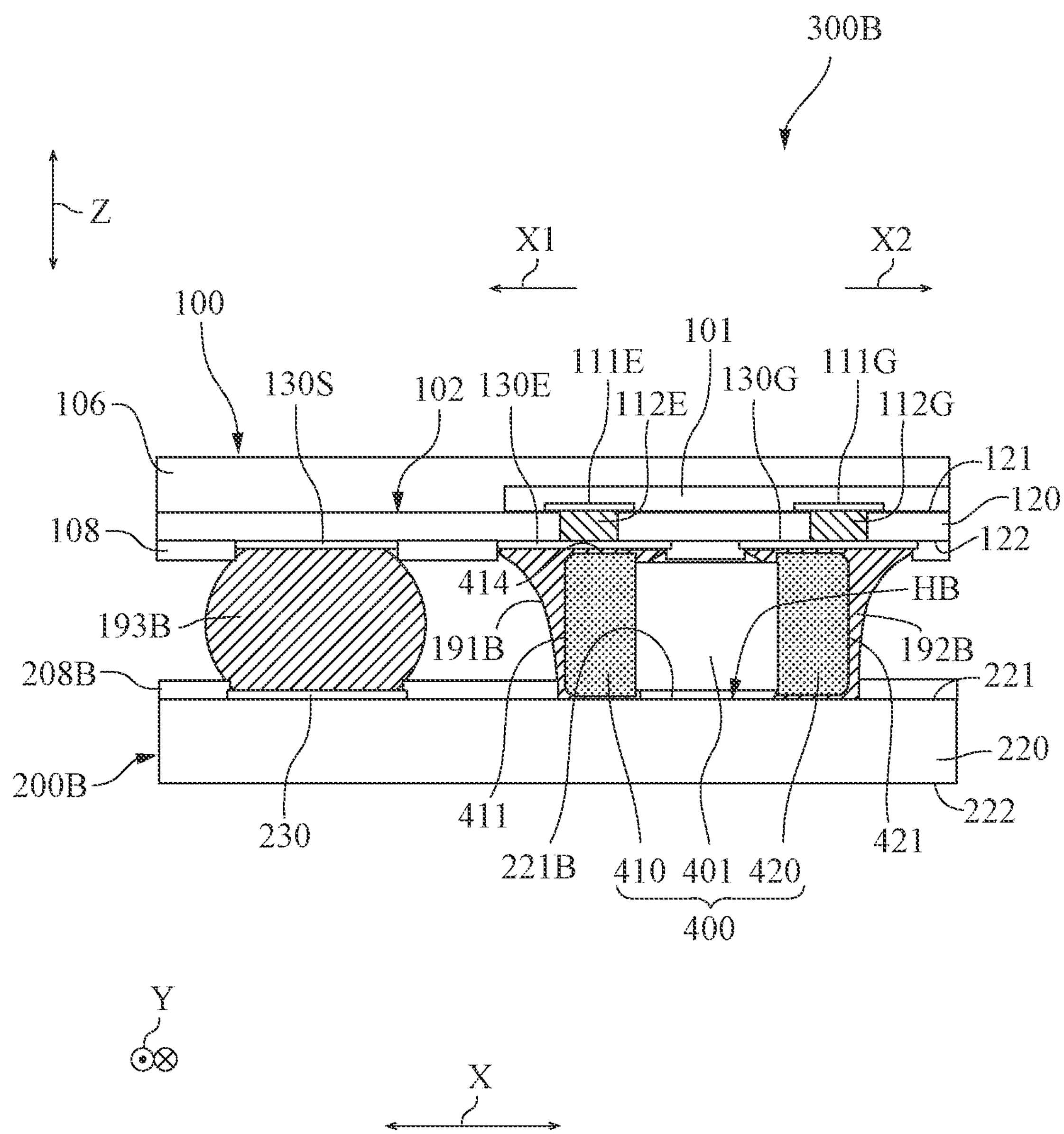


FIG.10A

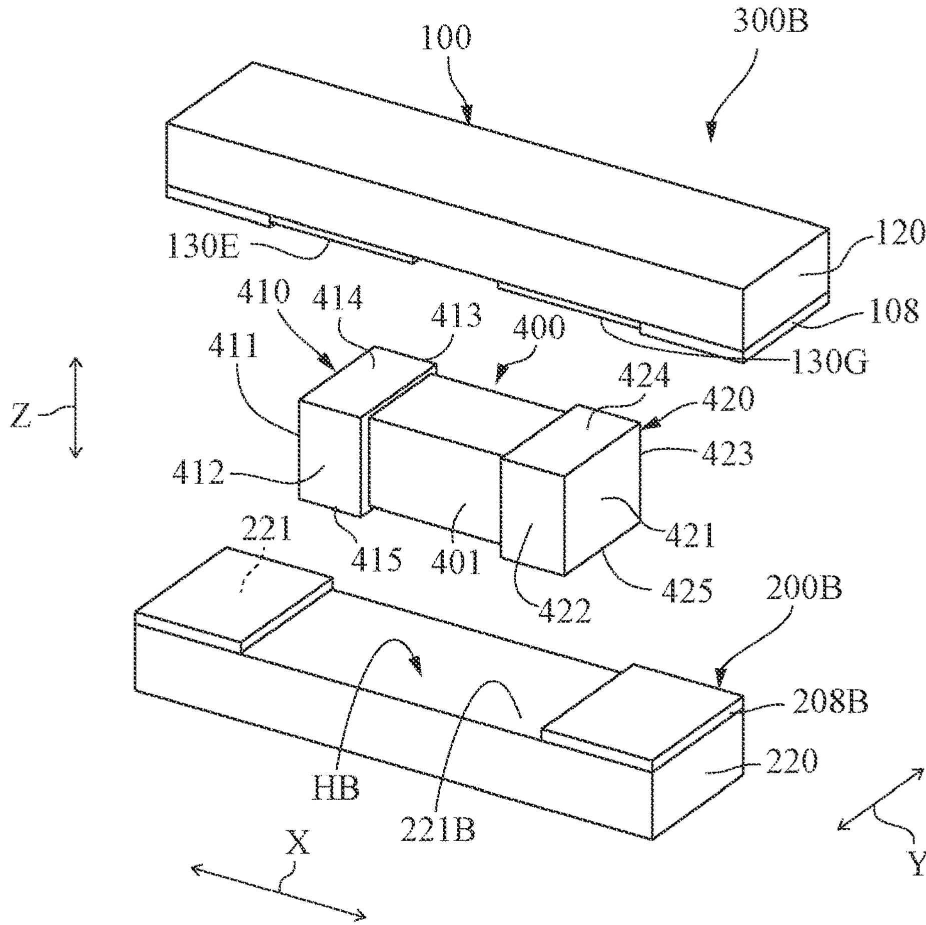


FIG.10B

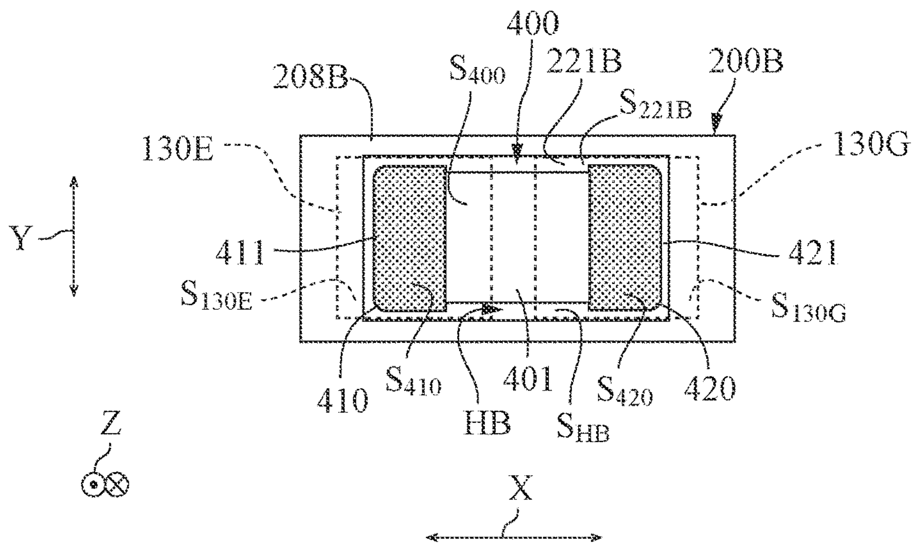


FIG.11A

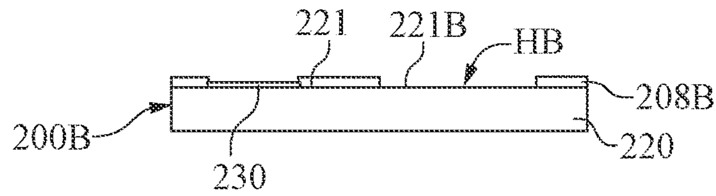


FIG.11B

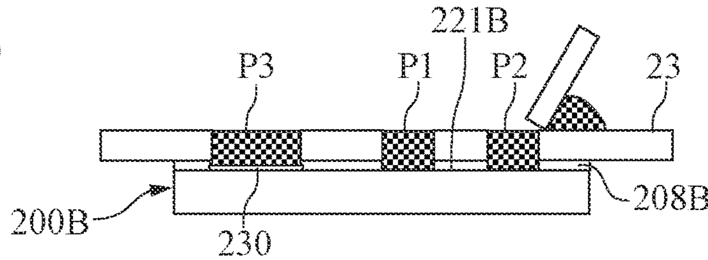


FIG.11C

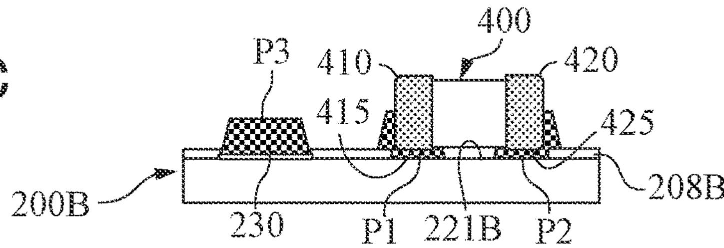


FIG.11D

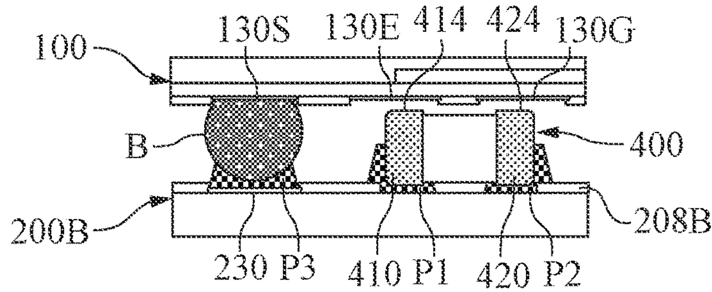


FIG.11E

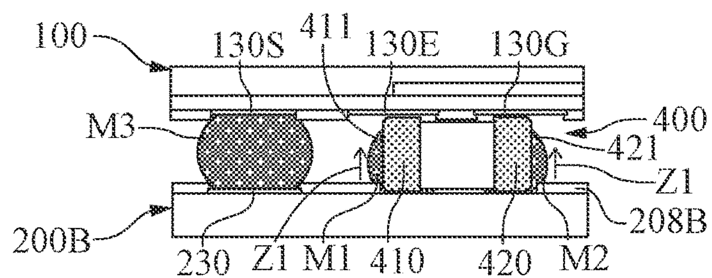


FIG.11F

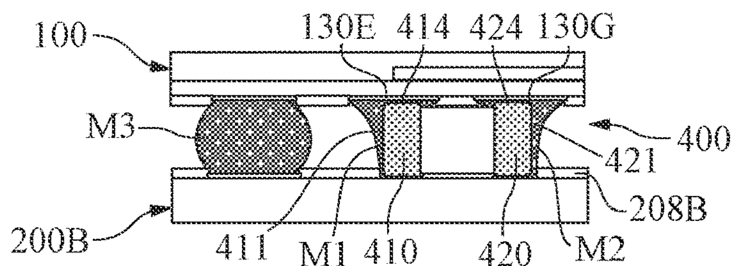


FIG.12A

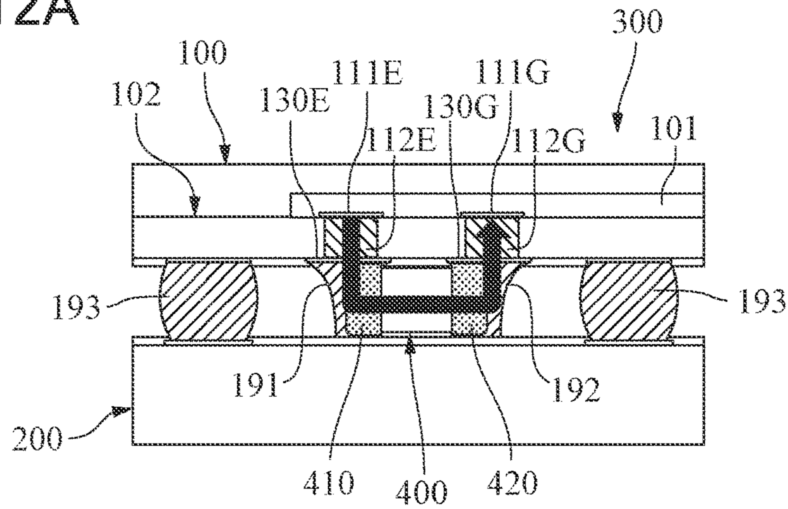


FIG.12B

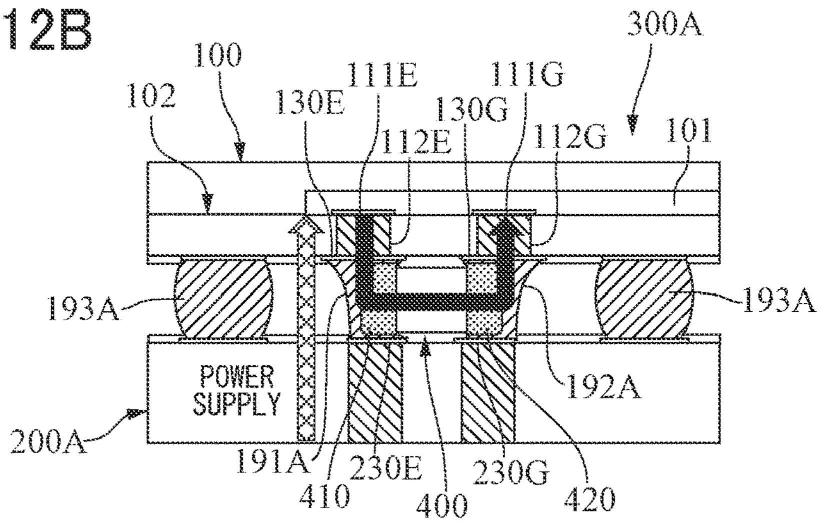


FIG.12C

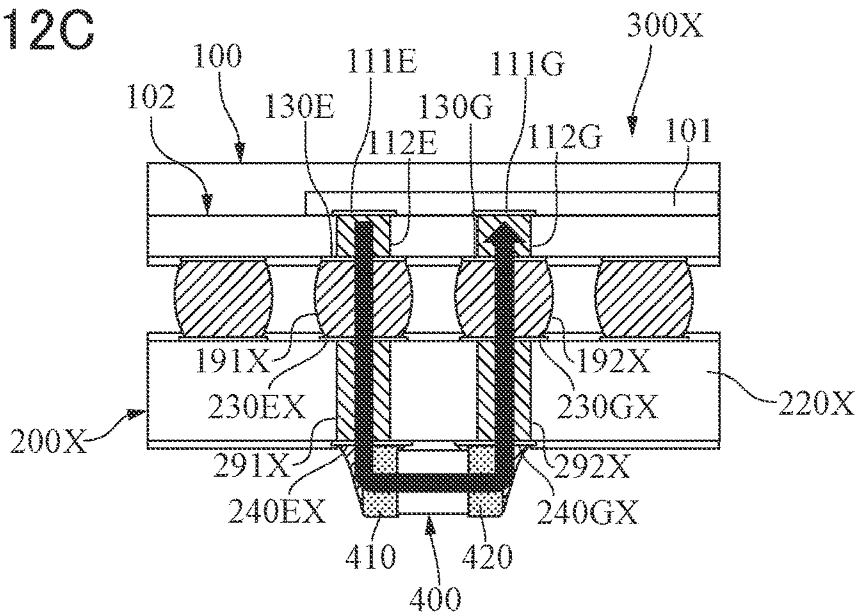
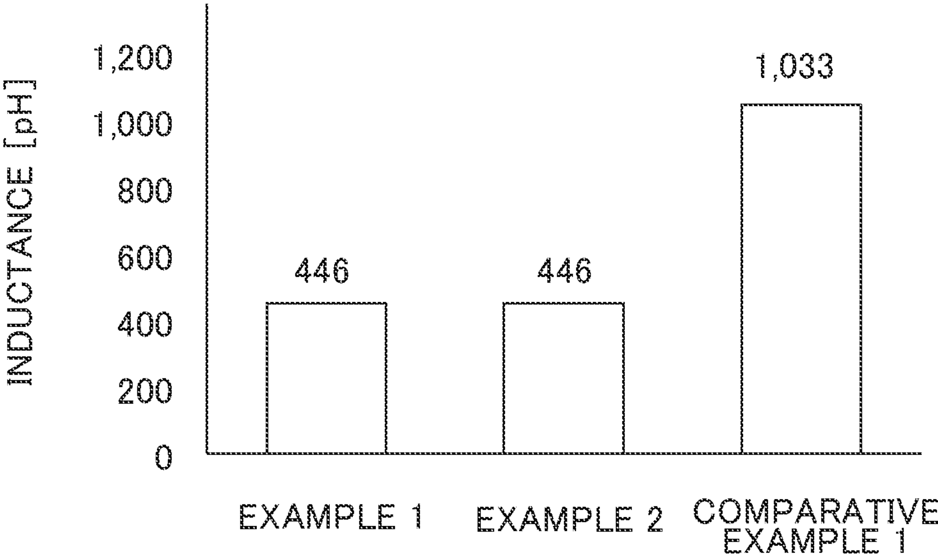


FIG.13



SEMICONDUCTOR MODULE MANUFACTURING METHOD, ELECTRONIC EQUIPMENT MANUFACTURING METHOD, SEMICONDUCTOR MODULE, AND ELECTRONIC EQUIPMENT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of International Patent Application No. PCT/JP2020/022914, filed Jun. 10, 2020, which claims the benefit of Japanese Patent Application No. 2019-110913, filed Jun. 14, 2019, and Japanese Patent Application No. 2020-088291, filed May 20, 2020 which are hereby incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a technology of a semiconductor module having a semiconductor device.

Description of the Related Art

[0003] Electronic equipment such as a mobile device includes a semiconductor module including a semiconductor device that communicates with another semiconductor device such as a memory and a printed wiring board on which the semiconductor device is mounted. A semiconductor device is a semiconductor package including a semiconductor element and a package substrate. An arrangement structure of terminals included in the semiconductor device is, for example, a ball grid array (BGA). In the electronic equipment, high-speed communication and low voltage communication of the semiconductor device have been advanced, and it is required to reduce noise generated in the semiconductor device. In addition, with downsizing and thinning of the electronic equipment, it is desired to narrow the pitch between adjacent terminals in the semiconductor device.

[0004] As one of means for reducing noise, it is considered to connect a bypass capacitor between a power terminal and a ground terminal of the semiconductor device. The bypass capacitor is generally mounted on a surface adjacent to the semiconductor device in the printed wiring board or on a surface opposite to a surface on which the semiconductor device is mounted in the printed wiring board by surface mount technology (SMT). However, in this method, it is necessary to form a wire that electrically connects the semiconductor device and the capacitor on the printed wiring board, and inductance of the wire contributes to generation of noise that hinders an increase in communication speed in the semiconductor device. Meanwhile, Japanese Patent Laid-Open No. 2006-173407 discloses a technology of directly attaching the bypass capacitor to a power supply pad and a ground pad of a BGA package with solder.

[0005] However, in the technology of Japanese Patent Laid-Open No. 2006-173407, it is necessary to form a solder ball on each of a pair of electrodes of the capacitor in advance before the semiconductor device is mounted on the printed wiring board. The capacitor is a compact electronic component. For this reason, it is difficult to form the solder balls on the electrodes of the capacitor in terms of manufacturing. In addition, since a process of forming the solder balls on the electrodes of the capacitor is required, the manufacturing process increases. Therefore, it has been required to improve productivity of the semiconductor module as compared with the related art. Such a problem also occurs when a small electronic component other than the capacitor, for example, an inductor or a resistor, is connected to the semiconductor device. Further, when these electronic components are connected to a semiconductor device, bonding strength is required.

[0006] Therefore, a technology for improving the productivity of the semiconductor module has been expected. In addition, it has been expected to increase the bonding strength of the electronic component connected to the semiconductor module.

SUMMARY OF THE INVENTION

[0007] According to a first aspect of the present invention, a semiconductor module manufacturing method includes preparing a chip component including a first electrode and a second electrode disposed at intervals in a predetermined direction, a semiconductor device including a first land and a second land, and a printed wiring board, supplying a first solder paste and a second solder paste to the printed wiring board at intervals, placing the chip component on the printed wiring board such that the first electrode is in contact with the first solder paste and the second electrode is in contact with the second solder paste, placing the semiconductor device on the printed wiring board such that the first land faces the first electrode and the second land faces the second electrode, heating and melting the first solder paste and the second solder paste, and bonding the first land and the first electrode to each other with solder and bonding the second land and the second electrode to each other with solder by cooling and solidifying wet-spread molten solder to each of the first land and the second land.

[0008] According to a second aspect of the present invention, a semiconductor module includes a printed wiring board, a semiconductor device including a first land and a second land, the semiconductor device being mounted on the printed wiring board, a chip component including a first electrode and a second electrode spaced apart from each other in a predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device, a first solder bonding portion that bonds the first electrode and the first land to each other, and a second solder bonding portion that bonds the second electrode and the second land to each other. The printed wiring board includes an insulating substrate and a solder resist disposed on a main surface of the insulating substrate. The chip component faces the solder resist. Each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode in a plan vie and extends outward in the predetermined direction from the chip component. The first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from the solder resist. The second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the solder resist.

[0009] According to a third aspect of the present invention, a semiconductor module includes a printed wiring

board, a semiconductor device including a first land and a second land, the semiconductor device being mounted on the printed wiring board, a chip component including a first electrode and a second electrode spaced apart from each other in a predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device, a first solder bonding portion that bonds the first electrode and the first land to each other, and a second solder bonding portion that bonds the second electrode and the second land to each other. The printed wiring board includes an insulating substrate, a third land disposed on a main surface of the insulating substrate and electrically connected to the first land by the first solder bonding portion, and a fourth land disposed on the main surface of the insulating substrate and electrically connected to the second land by the second solder bonding portion. In a plan view, each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode, overlaps at least a portion of each of the third land and the fourth land, and extends outward in the predetermined direction from the chip component. The first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from the third land. The second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the fourth land.

[0010] According to a fourth aspect of the present invention, a semiconductor module includes a printed wiring board, a semiconductor device comprising a first land and a second land, the semiconductor device being mounted on the printed wiring board, a chip component including a first electrode and a second electrode spaced apart from each other in a predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device, a first solder bonding portion that bonds the first electrode and the first land to each other, and a second solder bonding portion that bonds the second electrode and the second land to each other. The printed wiring board includes an insulating substrate and a solder resist disposed on a main surface of the insulating substrate. The solder resist has an opening portion into which a portion of the chip component is inserted. Each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode in a plan view and extends outward in the predetermined direction from the chip component. The first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from a portion of the main surface of the insulating substrate exposed by the opening portion of the solder resist. The second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the portion of the main surface of the insulating substrate exposed by the opening portion of the solder resist.

[0011] Further features of the present invention will become apparent from the following description of exemplary embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is an explanatory diagram of an example of electronic equipment according to a first embodiment.

[0013] FIG. **2**A is a perspective view of a processing module according to the first embodiment.

[0014] FIG. **2**B is a schematic cross-sectional view of the processing module according to the first embodiment.

[0015] FIG. **3** is a schematic cross-sectional view in which a portion of the processing module according to the first embodiment is enlarged.

[0016] FIG. **4**A is an exploded partial perspective view of the processing module according to the first embodiment.

[0017] FIG. **4**B is a schematic diagram for explaining an arrangement relationship among a semiconductor device, a capacitor, and a printed wiring board according to the first embodiment.

[0018] FIG. **5**A is a diagram for explaining one stage of a processing module manufacturing method according to the first embodiment.

[0019] FIG. **5**B is a diagram for explaining one stage of the processing module manufacturing method according to the first embodiment.

[0020] FIG. **5**C is a diagram for explaining one stage of the processing module manufacturing method according to the first embodiment.

[0021] FIG. **5**D is a diagram for explaining one stage of the processing module manufacturing method according to the first embodiment.

[0022] FIG. **5**E is a diagram for explaining one stage of the processing module manufacturing method according to the first embodiment.

[0023] FIG. **5**F is a diagram for explaining one stage of the processing module manufacturing method according to the first embodiment.

[0024] FIG. **6** is a schematic cross-sectional view in which a portion of a processing module according to a second embodiment is enlarged.

[0025] FIG. **7**A is an exploded partial perspective view of a processing module according to the second embodiment.

[0026] FIG. **7**B is a schematic diagram for explaining an arrangement relationship among a semiconductor device, a capacitor, and a printed wiring board according to the second embodiment.

[0027] FIG. **8**A is a diagram for explaining one stage of a processing module manufacturing method according to the second embodiment.

[0028] FIG. **8**B is a diagram for explaining one stage of the processing module manufacturing method according to the second embodiment.

[0029] FIG. **8**C is a diagram for explaining one stage of the processing module manufacturing method according to the second embodiment.

[0030] FIG. **8**D is a diagram for explaining one stage of the processing module manufacturing method according to the second embodiment.

[0031] FIG. **8**E is a diagram for explaining one stage of the processing module manufacturing method according to the second embodiment.

[0032] FIG. **8**F is a diagram for explaining one stage of the processing module manufacturing method according to the second embodiment.

[0033] FIG. **9** is a schematic cross-sectional view in which a portion of a processing module according to a third embodiment is enlarged.

[0034] FIG. **10**A is an exploded partial perspective view of the processing module according to the third embodiment.

[0035] FIG. **10**B is a schematic diagram for explaining an arrangement relationship among a semiconductor device, a capacitor, and a printed wiring board according to the third embodiment.

[0036] FIG. **11**A is a diagram for explaining one stage of a processing module manufacturing method according to the third embodiment.

[0037] FIG. **11**B is a diagram for explaining one stage of the processing module manufacturing method according to the third embodiment.

[0038] FIG. **11**C is a diagram for explaining one stage of the processing module manufacturing method according to the third embodiment.

[0039] FIG. **11**D is a diagram for explaining one stage of the processing module manufacturing method according to the third embodiment.

[0040] FIG. **11**E is a diagram for explaining one stage of the processing module manufacturing method according to the third embodiment.

[0041] FIG. **11**F is a diagram for explaining one stage of the processing module manufacturing method according to the third embodiment.

[0042] FIG. **12**A is a schematic cross-sectional view of a processing module of Example 1.

[0043] FIG. **12**B is a schematic cross-sectional view of a processing module of Example 2.

[0044] FIG. **12**C is a schematic cross-sectional view of a processing module of Comparative Example 1.

[0045] FIG. **13** is a graph illustrating calculation results of inductances in Example 1, Example 2, and Comparative Example 1.

DESCRIPTION OF THE EMBODIMENTS

[0046] Hereinafter, modes for carrying out the present invention will be described in detail with reference to the drawings.

First Embodiment

[0047] FIG. **1** is an explanatory diagram of a digital camera **600** which is an imaging device as an example of electronic equipment according to a first embodiment. The digital camera **600** as an imaging device is an interchangeable lens digital camera, and includes camera body **601**. A lens unit (lens barrel) **602** including a lens is detachable from the camera body **601**. The camera body **601** includes a casing **611**, and a processing module **300** and a sensor module **900**, which are printed circuit boards, disposed inside the casing **611**. The processing module **300** is an example of a semiconductor module. The processing module **300** and the sensor module **900** are electrically connected to each other by a cable **950**.

[0048] The sensor module **900** includes an image sensor **700** as an imaging element and a printed wiring board **800**. The image sensor **700** is mounted on the printed wiring board **800**. The image sensor **700** is, for example, a complementary metal oxide semiconductor (CMOS) image sensor or a charge coupled device (CCD) image sensor. The image sensor **700** has a function of converting light incident via the lens unit **602** into an electric signal.

[0049] The processing module **300** includes a semiconductor device **100** and a printed wiring board **200** which is a first wiring board. The semiconductor device **100** is mounted on the printed wiring board **200**. The printed wiring board **200** is a rigid substrate. The semiconductor device **100** is, for example, a digital signal processor, and has a function of acquiring an electric signal from the image sensor **700**, performing processing of correcting the acquired electric signal, and generating image data.

[0050] FIG. **2**A is a perspective view of the processing module **300** according to the first embodiment. FIG. **2**B is a schematic cross-sectional view of the processing module **300** taken along line IIB-IIB in FIG. **2**A. FIG. **3** is a schematic cross-sectional view in which a portion of the processing module **300** illustrated in FIG. **2**B is enlarged. Hereinafter, description will be given with reference to FIGS. **2**A, **2**B, and **3**.

[0051] The semiconductor device **100** is an area array semiconductor package, and is a BGA semiconductor package in the first embodiment. The semiconductor device **100** includes a semiconductor element **101** and a package substrate **102** which is a second wiring board. The package substrate **102** is a rigid substrate.

[0052] The semiconductor element **101** is mounted on the package substrate **102**. The package substrate **102** includes an insulating substrate **120**. The insulating substrate **120** has a main surface **121** and a main surface **122** opposite to the main surface **121**. A material of the insulating substrate **120** is, for example, ceramic such as alumina or an epoxy resin containing glass. The semiconductor element **101** is, for example, a semiconductor chip, and is mounted on the main surface **121** of the insulating substrate **120** in a face-up manner or a face-down manner, the face-down manner in the first embodiment. A sealing resin **106** for sealing the semiconductor element **101** is provided on the main surface **121** of the insulating substrate **120**. The package substrate **102** has a plurality of lands **130** disposed on the main surface **122** of the insulating substrate **120**. An arrangement pattern of the plurality of lands **130** may have a lattice shape, that is, a matrix shape, or a staggered shape. The land **130** is a terminal made of a conductive metal material such as copper or gold, and is, for example, a signal terminal, a power terminal, a ground terminal, or a dummy terminal. A solder resist **108** is provided on the main surface **122**. The solder resist **108** is a film made of a solder resist material. Each of the plurality of lands **130** is exposed through an opening portion formed in the solder resist **108**. The land **130** may be a land of either a solder mask defined (SMD) or a non-solder mask defined (NSMD), but is a land of SMD in the first embodiment. Although not illustrated, a heat sink may be disposed on the upper surface of the semiconductor element **101**.

[0053] The semiconductor element **101** includes a plurality of power terminals, a plurality of ground terminals, and a plurality of signal terminals, and each terminal is bonded to the package substrate **102** by wire bonding or flip chip bonding (not illustrated). FIGS. **2**B and **3** illustrate a power terminal **111**E, which is one of the plurality of power terminals, and illustrate a ground terminal **111**G, which is one of the plurality of ground terminals. That is, the semiconductor element **101** includes the power terminal **111**E and the ground terminal **111**G.

[0054] The printed wiring board **200** includes insulating substrate **220**. The insulating substrate **220** has a main surface **221** and a main surface **222** opposite to the main surface **221**. The printed wiring board **200** has a plurality of

lands **230** disposed on main surface **221** of the insulating substrate **220**. The land **230** is a terminal made of a conductive metal material such as copper or gold, and is, for example, a signal terminal, a power terminal, a ground terminal, or a dummy terminal. A material of the insulating substrate **220** is an insulating material such as an epoxy resin.

[0055] The printed wiring board **200** includes a solder resist **208**. The solder resist **208** is a film made of a solder resist material. The solder resist **208** is provided on the main surface **221**. Each of the plurality of lands **230** is exposed through an opening portion formed in the solder resist **208**. The land **230** may be either an SMD or an NSMD land, but is an SMD land in the first embodiment.

[0056] The plurality of lands **130** include a land **130**E serving as a power terminal and a land **130**G serving as a ground terminal. The plurality of lands **130** are arranged at intervals of 0.4 mm or less. The land **130**E is a first land, and the land **130**G is a second land. The land **130**E is electrically connected to the power terminal **111**E of the semiconductor element **101** via a via conductor **112**E formed on the insulating substrate **120**. The land **130**G is electrically connected to the ground terminal **111**G of the semiconductor element **101** via a via conductor **112**G formed on the insulating substrate **120**.

[0057] The plurality of lands **130** include a land **130**S other than the lands **130**E and **130**G. The land **130**S is a land serving as a signal terminal, a power terminal, a ground terminal, or a dummy terminal. In the first embodiment, each of the plurality of lands **130**S is a fifth land, and each of the plurality of lands **230** is a sixth land. The land **130**S and the land **230** are bonded to each other by solder bonding portion **193** that is a third solder bonding portion made of solder. A height of the solder bonding portion **193** is higher than a height of a capacitor **400** described later. Specifically, the height is 1.3 times or less the height of the capacitor. This is because warpage occurs from a center toward an outer peripheral edge of the semiconductor element **101** during a thermal bonding process.

[0058] The processing module **300** includes a capacitor **400** which is an example of a chip component. The capacitor **400** is a passive component and is a chip component. A size of the chip component in a plan view is preferably 0402 size or less, such as 0402 size of 0.4 mm×0.2 mm or 0201 size of 0.25 mm×0.125 mm. Notations such as 0402 size and 0201 size conform to the size notation method (mm standard) of electronic components in Japanese Industrial Standards.

[0059] The capacitor **400** includes an element body **401** having a substantially rectangular parallelepiped shape extending in a longitudinal direction as an example of a predetermined direction, and a pair of electrodes **410** and **420** provided on both sides of the element body **401** in the longitudinal direction. The pair of electrodes **410** and **420** is fixed to the element body **401** at intervals in the longitudinal direction. In FIGS. **2**B and **3**, the longitudinal direction of the capacitor **400**, that is, the element body **401** is an X direction. A short direction of the capacitor **400**, that is, the element body **401** is a Y direction. The Y direction is a width direction orthogonal to the X direction. A vertical direction of the capacitor **400**, that is, the element body **401** is a Z direction. The Z direction is a direction orthogonal to the X direction and the Y direction. The Z direction is also a direction perpendicular to the main surfaces **121**, **122**, **221**, and **222**.

[0060] One electrode **410** of the pair of electrodes **410** and **420** is a first electrode, and the other electrode **420** is a second electrode. Each of the electrodes **410** and **420** includes a base and an outer film covering the base. A material of the outer film of the electrode **410**,**420** is a conductive metal material such as tin.

[0061] The capacitor **400** is a bypass capacitor. The electrode **410** of the capacitor **400** is electrically connected to the land **130**E, and the electrode **420** of the capacitor **400** is electrically connected to the land **130**G.

[0062] A power supply noise is generated by an inductance of a wire between the electrode **410** of the capacitor **400** and the power terminal **111**E and an inductance of a wire between the electrode **420** of the capacitor **400** and the ground terminal **111**G. The power supply noise refers to a voltage fluctuation of a power supply line caused by the operation of the semiconductor device **100**. This voltage fluctuation occurs when a power supply current changes due to an inductance or a resistance parasitic in the power supply line. In order to reduce the power supply noise by reducing the inductance of the wire, the capacitor **400** is preferably disposed immediately below the semiconductor element **101** so that the wire between the capacitor **400** and the power terminal **111**E and the wire between the capacitor **400** and the ground terminal **111**G of the semiconductor device **100** are minimized. That is, it is preferable that the semiconductor element **101** and the capacitor **400** overlap in a plan view of the processing module **300** from the semiconductor device **100** side.

[0063] Therefore, in the first embodiment, the capacitor **400** is disposed on the main surface **221** side of the insulating substrate **220** of the printed wiring board **200**, that is, between the semiconductor device **100** and the printed wiring board **200**. The electrode **410** of the capacitor **400** is bonded to the land **130**E by a solder bonding portion **191** which is a first solder bonding portion formed of solder. The electrode **420** of capacitor **400** is bonded to the land **130**G by a solder bonding portion **192** which is a second solder bonding portion made of solder. Accordingly, the electrode **410** of the capacitor **400** is electrically connected directly to the land **130**E of the semiconductor device **100** by the solder bonding portion **191** without the printed wiring board **200** interposed therebetween. Therefore, the inductance of the wire between the electrode **410** of the capacitor **400** and the land **130**E can be reduced. Further, the electrode **420** of the capacitor **400** is electrically connected to the land **130**G of the semiconductor device **100** directly by the solder bonding portion **192** without the printed wiring board **200** interposed therebetween. Therefore, the inductance of the wire between the electrode **420** of the capacitor **400** and the land **130**G can be reduced. Since the inductance of the wire is reduced, the generated power supply noise is reduced, and a speed of communication in the semiconductor device **100** can be increased.

[0064] In the first embodiment, the solder bonding portions **191** and **192** are in contact with the solder resist **208**, but are not in contact with the land **230** of the printed wiring board **200**.

[0065] FIG. **4**A is an exploded partial perspective view of the processing module **300** according to the first embodiment. FIG. **4**B is a schematic diagram for explaining an

arrangement relationship of the semiconductor device **100**, capacitor **400**, and printed wiring board **200** when viewed in the Z direction. In FIGS. **4**A and **4**B, illustrations of solder bonding portions **191** and **192** are omitted. In FIG. **4**B, the lands **130**E and **130**G of the semiconductor device are indicated by broken lines.

[0066] As illustrated in FIG. **4**A, the electrode **410** has three side surfaces **411**, **412**, and **413**, an upper surface **414**, and a lower surface **415**, which are electrode surfaces. The side surfaces **411**, **412**, and **413**, the upper surface **414**, and the lower surface **415** have rectangular shapes when viewed from a direction perpendicular to each surface. Among the three side surfaces **411**, **412**, and **413**, the two side surfaces **412** and **413** face each other at an interval in the Y direction. The upper surface **414** and the lower surface **415** face each other at an interval in the Z direction. The side surface **411** is orthogonal to and adjacent to the side surfaces **412** and **413**, the upper surface **414**, and the lower surface **415**. The electrode **420** has three side surfaces **421**, **422**, and **423**, an upper surface **424**, and a lower surface **425** which are electrode surfaces. The side surfaces **421**, **422**, and **423**, the upper surface **424**, and the lower surface **425** have rectangular shapes when viewed from a direction perpendicular to each surface. Among the three side surfaces **421**, **422**, and **423**, the two side surfaces **422** and **423** face each other at an interval in the Y direction. The upper surface **424** and the lower surface **425** face each other at an interval in the Z direction. The side surface **421** is orthogonal to and adjacent to the side surfaces **422** and **423**, the upper surface **424**, and the lower surface **425**. The side surface **411** of the electrode **410** and the side surface **421** of the electrode **420** are arranged to face each other at an interval in the X direction. The upper surface **414** of the electrode **410** faces the land **130**E of the semiconductor device **100**, and the lower surface **415** of the electrode **410** faces the solder resist **208** of the printed wiring board **200**. The upper surface **424** of the electrode **420** faces the land **130**G of the semiconductor device **100**, and the lower surface **425** of the electrode **420** faces the solder resist **208** of the printed wiring board **200**.

[0067] As illustrated in FIG. **4**B, the land **130**E and the land **130**G are arranged at intervals in the X direction. The land **130**E overlaps at least a portion of the electrode **410** of the capacitor **400**, the entire electrodes **410** in the first embodiment in a plan view, that is, when viewed in the Z direction. The land **130**G overlaps at least a portion of the electrode **420** of the capacitor **400**, the entire electrode **420** in the first embodiment when viewed in the Z direction. In the first embodiment, an area S_{130E} of the land **130**E is larger than an area S_{410} of the electrode **410** as viewed in the Z direction. When viewed in the Z direction, an area S_{130G} of the land **130**G is larger than an area S_{420} of the electrode **420**. The land **130**E and the land **130**G extend outward in the X direction from the capacitor **400** when viewed in the Z direction.

[0068] As illustrated in FIG. **3**, each of the solder bonding portions **191** and **192** has a fillet shape in which the outer surface spreads away from the capacitor **400** from the solder resist **208** toward each of the lands **130**E and **130**G. More specifically, the solder bonding portion **191** has a fillet shape in which the solder bonding portion **191** expands outward in the X direction from the electrode **410**, that is, in the X1 direction, as the solder bonding portion **191** extends from the solder resist **208** toward the land **130**E. The solder bonding portion **192** has a fillet shape in which the solder bonding portion **192** expands outward in the X direction from the electrode **420**, that is, in the X2 direction, as the solder bonding portion **192** extends from the solder resist **208** toward the land **130**G. The X1 direction is a direction away from the electrode **410** in the X direction. The X2 direction is a direction opposite to the X1 direction in the X direction and is a direction away from the electrode **420**. As a result, the bonding strength between each of the lands **130**E and **130**G and each of the electrodes **410** and **420** increases. Further, as illustrated in FIG. **2**B, each of the solder bonding portions **191** and **192** is prevented from having a shape bulging in the X direction, and each of the solder bonding portions **191** and **192** is prevented from being short-circuited with the adjacent solder bonding portion **193**.

[0069] As illustrated in FIG. **4**B, each of the lands **130**E and **130**G has a rectangular shape when viewed in the Z direction, but is not limited thereto. For example, the lands **130**E and **130**G may have any shape such as a polygonal shape, a circular shape, or an elliptical shape when viewed in the Z direction.

[0070] Next, a method of manufacturing the processing module **300** will be described. FIGS. **5**A to **5**F are explanatory diagrams of the method of manufacturing the processing module **300** according to the first embodiment. As illustrated in FIG. **5**A, the printed wiring board **200** is prepared (Step S**1**). In Step S**1**, the semiconductor device **100** and the capacitor **400** are also prepared. Next, as illustrated in FIG. **5**B, a solder paste P**1** as a first solder paste, a solder paste P**2** as a second solder paste, and a solder paste P**3** as a third solder paste are supplied onto the printed wiring board **200** at intervals (Step S**2**). In the first embodiment, in Step S**2**, the solder paste P**1** and the solder paste P**2** are supplied onto the solder resist **208**. In Step S**2**, the solder paste P**3** is supplied onto the land **230** of the printed wiring board **200**.

[0071] The solder pastes P**1**, P**2**, and P**3** contain solder powder. The solder pastes P**1**, P**2**, and P**3** may further contain a flux component necessary for soldering. In the present embodiment, the solder pastes P**1**, P**2**, and P**3** are all the same material, but are not limited to the same material as long as the solder pastes P**1**, P**2**, and P**3** have close melting point. In Step S**2**, the solder pastes P**1**, P**2**, and P**3** are supplied to the printed wiring board **200** by screen printing using the metal mask **23**. The method for supplying the solder pastes P**1**, P**2**, and P**3** is not limited thereto. For example, the solder pastes P**1**, P**2**, and P**3** may be supplied to the printed wiring board **200** by a dispenser.

[0072] Next, as illustrated in FIG. **5**C, the capacitor **400** prepared in Step S**1** is placed on the printed wiring board **200** such that the electrode **410** is in contact with the solder paste P**1** and the electrode **420** is in contact with the solder paste P**2** (Step S**3**). As a result, the lower surface **415** of the electrode **410** comes into contact with the solder paste P**1**, and the lower surface **425** of the electrode **420** comes into contact with the solder paste P**2**. It is not necessary to attach solder balls to the electrodes **410** and **420** of the capacitor **400** in advance. In Step S**3**, the capacitor **400** is mounted on the printed wiring board **200** using a mounter (not illustrated). At this time, the capacitor **400** is positioned and placed on the printed wiring board such that the electrode **410** and the solder paste P**1** face each other and the electrode **420** and the solder paste P**2** face each other.

[0073] Next, as illustrated in FIG. **5**D, the semiconductor device **100** prepared in Step S**1** is mounted on the printed

wiring board **200** such that the land **130**E faces the electrode **410** and the land **130**G faces the electrode **420** (Step S**4**). In Step S**4**, the semiconductor device **100** is mounted on the printed wiring board **200** using a mounter (not illustrated). At this time, the semiconductor device **100** is aligned and placed on the printed wiring board such that the land **130**E faces the electrode **410**, the land **130**G faces the electrode **420**, and the land **130**S faces the land **230**. Here, the solder balls are not provided on the lands **130**E and **130**G of the semiconductor device **100** prepared in Step S**1**, and solder balls B as ball terminals are provided on the lands **130**S. Therefore, the semiconductor device **100** is placed on the printed wiring board **200** such that the center of the solder ball B coincides with the center of the land **230**. In Step S**4**, the semiconductor device **100** is placed on the printed wiring board **200** to bring the solder balls B formed on the lands **130**S into contact with the solder paste P**3**. In FIG. **5**D, the upper surface **414** of the electrode **410** and the land **130**E are not in contact with each other, and the upper surface **424** of the electrode **420** and the land **130**G are not in contact with each other, but these may be contacted with others.

[0074] In Step S**4**, a positional relationship among the printed wiring board **200**, the capacitor **400**, and the semiconductor device **100** when viewed from the Z direction is as illustrated in FIG. **4**B. When the capacitor **400** is placed on the printed wiring board **200**, each of the land **130**E and the land **130**G of the semiconductor device **100** overlaps at least a portion of each of the electrode **410** and the electrode **420** when viewed in the Z direction, and extends outward in the X direction from the capacitor **400**.

[0075] Next, in a state where the semiconductor device **100** and the capacitor **400** are placed on the printed wiring board **200**, the printed wiring board **200** is conveyed to a reflow furnace (not illustrated). Then, in Step S**5-1** illustrated in FIG. **5**E, a temperature of the atmosphere in the reflow furnace is adjusted to a temperature equal to or higher than the melting point of the solder, and the solder pastes P**1**, P**2**, and P**3** and the solder ball B of FIG. **5**D are melted as illustrated in FIG. **5**E. The solder paste P**1** is melted to form a flowable molten solder M**1**, and the solder paste P**2** is melted to form a flowable molten solder M**2**. When the solder paste P**3** and the solder ball B are melted, a flowable molten solder M**3** is obtained.

[0076] Subsequent to Step S**5-1**, in Step S**5-2** illustrated in FIG. **5**F, heating is continued to cause the molten solders M**1** and M**2** to flow. Since the electrode **410**,**420** has better wettability of the molten solder than the solder resist **208**, the molten solders M**1** and M**2** crawl up the side surfaces **411** and **421** in an upward direction indicated by an arrow Z**1** as illustrated in FIG. **5**E. Thereafter, the molten solders M**1** and M**2** move to the upper surfaces **414** and **424** as illustrated in FIG. **5**F due to the wet-spreading property. Although not illustrated in FIG. **5**E, the molten solders M**1** and M**2** also crawl up in the upward direction indicated by the arrow Z**1** on the side surfaces **412** and **413** of the electrode **410** and the side surfaces **422** and **423** of the electrode **420**.

[0077] In addition, the capacitor **400** is pushed upward toward the semiconductor device **100** by the molten solders M**1** and M**2**, the distance between the upper surface **414** of the electrode **410** and the land **130**E is narrowed, and the distance between the upper surface **424** of the electrode **420** and the land **130**G is narrowed. The molten solders M**1** and M**2** reaching the upper surfaces **414** and **424** come into contact with the lands **130**E and **130**G, wet-spread on the lands **130**E and **130**G, and have a fillet shape in which the skirt widens as it goes from the solder resist **208** toward the lands **130**E and **130**G.

[0078] Thereafter, the molten solders M**1** and M**2** wet-spread to every corner of the lands **130**E and **130**G are cooled and solidified. As a result, the molten solder M**1** is cooled and solidified in a fillet shape on the land **130**E. The molten solder M**2** is cooled and solidified in a fillet shape on the land **130**G. At the same time, the molten solder M**3** is also cooled and solidified. As a result, as illustrated in FIG. **3**, the solder bonding portion **191** in which the land **130**E and the electrode **410** are bonded by solder is formed, and the solder bonding portion **192** in which the land **130**G and the electrode **420** are bonded by solder is formed. In addition, the solder bonding portion **193** in which the land **130**S and the land **230** are bonded by solder is formed. As described above, the processing module **300** illustrated in FIG. **3** is manufactured.

[0079] Thereafter, the processing module **300** illustrated in FIG. **3** is housed in the casing **611** illustrated in FIG. **1**, whereby the camera body **601**, that is, the digital camera **600** is manufactured.

[0080] As described above, by melting the solder pastes P**1** and P**2** supplied to the printed wiring board **200**, the solder can be supplied to the lands **130**E and **130**G of the semiconductor device **100** via the electrodes **410** and **420** of the capacitor **400**. As a result, it is not necessary to form solder balls on the electrodes **410** and **420** of the capacitor **400** in advance, and the process of manufacturing the processing module **300** can be reduced. Therefore, since the processing module **300** can be easily manufactured, productivity of the processing module **300** is improved.

[0081] Here, when the solder wettability in the lands **130**E and **130**G of the semiconductor device **100** is F**1**, and the solder wettability in the electrodes **410** and **420** of the capacitor **400** is F**2**, a relationship of $F1 \geq F2$ is preferably satisfied. For example, by using gold as the material of the surface of the land **130**, that is, the material of the surfaces of the lands **130**E and **130**G, the relationship of $F1 \geq F2$ is established, and the molten solders M**1** and M**2** easily wet-spread in the lands **130**E and **130**G. As a result, the solder bonding portions **191** and **192** tends to have a fillet shape on the lands **130**E and **130**G. Therefore, even when the amount of solder in the solder bonding portions **191** and **192** is reduced, the lands **130**E and **130**G of the semiconductor device **100** and the electrodes **410** and **420** of the capacitor **400** can be reliably connected. Accordingly, even when the lands **130** of the semiconductor device **100** are arranged at a high density, it is possible to prevent a bonding failure from occurring.

Second Embodiment

[0082] A second embodiment will be described. FIG. **6** is a schematic cross-sectional view in which a portion of a processing module according to the second embodiment is enlarged. FIG. **6** schematically illustrates a cross section of a processing module **300**A according to the second embodiment. In the following description, the same components as those of the first embodiment are denoted by the same reference numerals, and detailed description thereof will be omitted.

[0083] The processing module **300**A according to the second embodiment includes the semiconductor device **100**

having the same configuration as that of the first embodiment and a printed wiring board **200**A. Similarly to the first embodiment, the land **130**E that is the first land, the land **130**G that is the second land, and the land **130**S that is the fifth land are arranged on the main surface **122** of the insulating substrate **120** included in the semiconductor device **100**.

[0084] The printed wiring board **200**A includes the insulating substrate **220** similar to that of the first embodiment. The insulating substrate **220** has a main surface **221** and a main surface **222** opposite to the main surface **221**. The printed wiring board **200**A includes a land **230**E that is a third land, a land **230**G that is a fourth land, and a land **230**S that is a sixth land, which are disposed on the main surface **221** of the insulating substrate **220**.

[0085] The lands **230**E, **230**G, and **230**S are terminals formed of a conductive metal material such as copper or gold. The land **230**E is a power terminal, and the land **230**G is a ground terminal. The land **230**S is a signal terminal, a power terminal, a ground terminal, or a dummy terminal. A via conductor **212**E formed on the insulating substrate **220** is connected to the land **230**E. The via conductor **212**G formed on the insulating substrate **220** is connected to the land **230**G.

[0086] The printed wiring board **200**A includes the solder resist **208**A. The solder resist **208**A is a film made of a solder resist material. The solder resist **208**A is provided on the main surface **221**. The land **230**S is exposed through an opening portion formed in the solder resist **208**A. The land **230**E and the land **230**G are exposed by one opening portion HA formed in the solder resist **208**A. Note that each of the land **230**E and the land **230**G may be exposed by each of two opening portions formed independently.

[0087] The land **130**E and land **230**E are bonded to each other by a solder bonding portion **191**A that is a first solder bonding portion made of solder. The land **130**G and land **230**G are bonded by a solder bonding portion **192**A that is a second solder bonding portion made of solder. The land **130**S and land **230**S are bonded to each other by a solder bonding portion **193**A that is a third solder bonding portion made of solder.

[0088] The processing module **300**A includes a capacitor **400** used as a bypass capacitor as in the first embodiment. The capacitor **400** is disposed on the main surface **221** side of the insulating substrate **220** of the printed wiring board **200**A, that is, between the semiconductor device **100** and the printed wiring board **200**A. The electrode **410** of the capacitor **400** is bonded to the land **130**E by the solder bonding portion **191**A. The electrode **420** of the capacitor **400** is bonded to the land **130**G by the solder bonding portion **192**A. Thus, the electrode **410** of the capacitor **400** is electrically connected directly to the land **130**E of the semiconductor device **100** by the solder bonding portion **191**A. Therefore, the inductance of the wire between the electrode **410** of the capacitor **400** and the land **130**E can be reduced. Further, the electrode **420** of the capacitor **400** is electrically connected directly to the land **130**G of the semiconductor device **100** by the solder bonding portion **192**A. Therefore, the inductance of the wire between the electrode **420** of the capacitor **400** and the land **130**G can be reduced. Since the inductance of the wire is reduced, the generated power supply noise is reduced, and a speed of communication in the semiconductor device **100** can be increased.

[0089] In the second embodiment, the land **230**E is electrically connected to the land **130**E by the solder bonding portion **191**A. The land **230**G is electrically connected to the land **130**E by the solder bonding portion **192**A. A power supply IC (not illustrated) electrically connected to the via conductors **212**E and **212**G illustrated in FIG. **6** is mounted on the printed wiring board **200**A. The power supply IC can supply power to the semiconductor element **101** of the semiconductor device **100** via the solder bonding portion **191**A and the solder bonding portion **192**A.

[0090] FIG. **7**A is an exploded partial perspective view of the processing module **300**A according to the second embodiment. FIG. **7**B is a schematic diagram for explaining an arrangement relationship of the semiconductor device **100**, the capacitor **400**, and the printed wiring board **200**A when viewed in the Z direction. In FIGS. **7**A and **7**B, illustrations of solder bonding portions **191**A and **192**A are omitted. In FIG. **7**B, the lands **130**E and **130**G of the semiconductor device are indicated by broken lines.

[0091] As illustrated in FIG. **7**A, the upper surface **414** of the electrode **410** faces the land **130**E of the semiconductor device **100**, and the lower surface **415** of the electrode **410** faces the land **230**E of the printed wiring board **200**A. The upper surface **424** of the electrode **420** faces the land **130**G of the semiconductor device **100**, and the lower surface **425** of the electrode **420** faces the land **230**G of the printed wiring board **200**A.

[0092] As illustrated in FIG. **7**B, the land **130**E and the land **130**G are arranged at intervals in the X direction. The land **130**E overlaps at least a portion of the electrode **410** of the capacitor **400**, the entire electrode **410** in the second embodiment when viewed in the Z direction. The land **130**G overlaps at least a portion of the electrode **420** of the capacitor **400**, the entire electrode **420** in the second embodiment when viewed in the Z direction. The land **230**E and the land **230**G are arranged at intervals in the X direction. The land **230**E overlaps at least a portion of the electrode **410** of the capacitor **400**, the entire electrode **410** in the second embodiment when viewed in the Z direction. The land **230**G overlaps at least a portion of the electrode **420** of the capacitor **400**, the entire electrode **420** in the second embodiment when viewed in the Z direction. In addition, the land **130**E overlaps at least a portion of the land **230**E, the entire land **230**E in the second embodiment when viewed in the Z direction. In addition, the land **130**G overlaps at least a portion of the land **230**G, the entire land **230**G in the second embodiment as viewed in the Z direction. In the second embodiment, the area S_{130E} of the land **130**E is larger than the area S_{410} of the electrode **410** as viewed in the Z direction. When viewed in the Z direction, an area S_{130G} of the land **130**G is larger than an area S_{420} of the electrode **420**. The land **130**E and the land **130**G extend outward in the X direction from the capacitor **400** when viewed in the Z direction.

[0093] In the second embodiment, as illustrated in FIG. **7**B, the area S_{130E} of the land **130**E is larger than the area S_{230E} of the land **230**E when viewed in the Z direction. When viewed in the Z direction, the area S_{130G} of the land **130**G is larger than the area S_{230G} of the land **230**G. Further, when viewed in the Z direction, an area S_{HA} of the opening portion HA is larger than an area S_{400} of the capacitor **400**.

[0094] As illustrated in FIG. **6**, each of the solder bonding portions **191**A and **192**A has a fillet shape in which the outer surface expands away from the capacitor **400** as each of the

solder bonding portions **191**A and **192**A extends from each of the lands **230**E and **230**G toward each of the lands **130**E and **130**G. More specifically, the solder bonding portion **191**A has a fillet shape that expands outward in the X direction from the electrode **410**, that is, in the X1 direction, as the solder bonding portion **191**A extends from the land **230**E toward the land **130**E. The solder bonding portion **192**A has a fillet shape that expands outward in the X direction from the electrode **410**, that is, in the X2 direction, as the solder bonding portion **192**A extends from the land **230**G toward the land **130**G. The X1 direction is a direction away from the electrode **410** in the X direction. The X2 direction is a direction opposite to the X1 direction in the X direction and is a direction away from the electrode **420**. As a result, the bonding strength between each of the lands **130**E and **130**G and each of the electrodes **410** and **420** increases. Further, each of the solder bonding portions **191**A and **192**A is prevented from having a shape bulging in the X direction, and each of the solder bonding portions **191**A and **192**A is prevented from being short-circuited with the adjacent solder bonding portion **193**A.

[0095] As illustrated in FIG. **7**B, each of the lands **230**E and **230**G has a rectangular shape when viewed in the Z direction, but is not limited thereto. For example, the lands **230**E and **230**G may have any shape such as a polygonal shape, a circular shape, or an elliptical shape when viewed in the Z direction.

[0096] Next, a method of manufacturing the processing module **300**A will be described. FIGS. **8**A to **8**F are explanatory diagrams of a method of manufacturing the processing module **300**A according to the second embodiment. As illustrated in FIG. **8**A, the printed wiring board **200**A is prepared (Step S**11**). In Step S**11**, the semiconductor device **100** and the capacitor **400** are also prepared. Next, as illustrated in FIG. **8**B, the solder paste P**1** which is the first solder paste, the solder paste P**2** which is the second solder paste, and the solder paste P**3** which is the third solder paste are supplied onto the printed wiring board **200**A at intervals (Step S**12**). In the second embodiment, in Step S**12**, the solder paste P**1** is supplied onto the land **230**E exposed by the opening portion HA formed in the solder resist **208**A. In addition, the solder paste P**2** is supplied onto the land **230**G exposed through the opening portion HA formed in the solder resist **208**A. In Step S**12**, the solder paste P**3** is supplied onto the land **230**S of the printed wiring board **200**A.

[0097] In Step S**12**, the solder pastes P**1**, P**2**, and P**3** are supplied to the printed wiring board **200**A by screen printing using the metal mask **23**. The method for supplying the solder pastes P**1**, P**2**, and P**3** is not limited thereto. For example, the solder pastes P**1**, P**2**, and P**3** may be supplied to the printed wiring board **200**A by a dispenser.

[0098] Next, as illustrated in FIG. **8**C, the capacitor **400** prepared in Step S**11** is placed on the printed wiring board **200**A such that electrode **410** is in contact with the solder paste P**1** and the electrode **420** is in contact with solder paste P**2** (Step S**13**). As a result, the lower surface **415** of the electrode **410** comes into contact with the solder paste P**1**, and the lower surface **425** of the electrode **420** comes into contact with the solder paste P**2**. It is not necessary to attach solder balls to the electrodes **410** and **420** of the capacitor **400** in advance.

[0099] Next, as illustrated in FIG. **8**D, the semiconductor device **100** prepared in Step S**11** is mounted on the printed wiring board **200**A such that the land **130**E faces the electrode **410** and the land **130**G faces the electrode **420** (Step S**14**). In Step S**14**, the semiconductor device **100** is placed on the printed wiring board **200**A to bring the solder balls B, which are ball terminals provided on the lands **130**S, into contact with the solder paste P**3**. In FIG. **8**D, the upper surface **414** of the electrode **410** and the land **130**E, and the upper surface **424** of the electrode **420** and land **130**G are not in contact with each other, but these may be contacted with other.

[0100] In Step S**14**, the positional relationship among the printed wiring board **200**A, the capacitor **400**, and the semiconductor device **100** when viewed from the Z direction is as illustrated in FIG. **7**B. When the capacitor **400** is placed on the printed wiring board **200**A, each of the land **130**E and the land **130**G of the semiconductor device **100** overlaps at least a portion of each of the electrode **410** and the electrode **420** when viewed in the Z direction, and extends outward in the X direction from the capacitor **400**.

[0101] Next, in a state where the semiconductor device **100** and the capacitor **400** are placed on the printed wiring board **200**A, the printed wiring board **200**A is conveyed to a reflow furnace (not illustrated). Then, in Step S**15-1** illustrated in FIG. **8**E, the temperature of the atmosphere in the reflow furnace is adjusted to a temperature equal to or higher than the melting point of the solder, and the solder pastes P**1**, P**2**, and P**3** and the solder ball B of FIG. **8**D are melted as illustrated in FIG. **8**E. The solder paste P**1** is melted to form a flowable molten solder M**1**, and the solder paste P**2** is melted to form a flowable molten solder M**2**. When the solder paste P**3** and the solder ball B are melted, a flowable molten solder M**3** is obtained.

[0102] Subsequent to Step S**15-1**, in Step S**15-2** illustrated in FIG. **8**F, heating is continued to cause the molten solders M**1** and M**2** to flow. As illustrated in FIG. **8**E, the molten solders M**1** and M**2** crawl up the side surfaces **411** and **421** in the upward direction indicated by the arrow Z**1**. Thereafter, the molten solders M**1** and M**2** move to the upper surfaces **414** and **424** as illustrated in FIG. **8**F. Although not illustrated in FIG. **8**E, the molten solders M**1** and M**2** also crawl up in the upward direction indicated by the arrow Z**1** on the side surfaces **412** and **413** of the electrode **410** and the side surfaces **422** and **423** of the electrode **420**.

[0103] In addition, the capacitor **400** is pushed upward toward the semiconductor device **100** by the molten solders M**1** and M**2**, the distance between the upper surface **414** of the electrode **410** and the land **130**E is narrowed, and the distance between the upper surface **424** of the electrode **420** and the land **130**G is narrowed. The molten solders M**1** and M**2** reaching the upper surfaces **414** and **424** come into contact with the lands **130**E and **130**G, wet-spread on the lands **130**E and **130**G, and have a fillet shape in which the skirt widens as it goes from the solder resist **208**A toward the lands **130**E and **130**G.

[0104] Thereafter, the molten solders M**1** and M**2** wet-spread to every corner of the lands **130**E and **130**G are cooled and solidified. As a result, the molten solder M**1** is cooled and solidified in a fillet shape on the land **130**E. The molten solder M**2** is cooled and solidified in a fillet shape on the land **130**G. At the same time, the molten solder M**3** is also cooled and solidified. As a result, the solder bonding portions **191**A, **192**A, and **193**A are formed as illustrated in FIG. **6**. As described above, the processing module **300**A illustrated in FIG. **6** is manufactured.

[0105] Thereafter, the processing module **300**A illustrated in FIG. **6** is housed in the casing **611** illustrated in FIG. **1**, thereby manufacturing a camera body of a digital camera which is an example of the electronic equipment.

[0106] As described above, by melting the solder pastes P**1** and P**2** supplied to the printed wiring board **200**A, the solder can be supplied to the lands **130**E and **130**G of the semiconductor device **100** via the electrodes **410** and **420** of the capacitor **400**. As a result, it is not necessary to form solder balls on the electrodes **410** and **420** of the capacitor **400** in advance, and the process of manufacturing the processing module **300**A can be reduced. Therefore, since the processing module **300**A can be easily manufactured, productivity of the processing module **300**A is improved.

[0107] In addition, the land **130**E and the land **230**E are electrically connected by the solder bonding portion **191**A, and the land **130**G and the land **230**G are electrically connected by the solder bonding portion **192**A. As a result, the solder bonding portions **191**A and **192**A for bonding the capacitor **400** to the semiconductor device **100** can be used as power supply lines for supplying power to the semiconductor element **101** of the semiconductor device **100**. This increases the degree of freedom of circuit design in the processing module **300**A.

[0108] In the second embodiment, as illustrated in FIG. **7**B, the areas S_{130E} and S_{130G} of the lands **130**E and **130**G are larger than the areas S_{230E} and S_{230G} of the lands **230**E and **230**G when viewed in the Z direction. Since the molten solders M**1** and M**2** are easily wet-spread in the lands **130**E and **130**G, it is possible to encourage more of the molten solders M**1** and M**2** to move to the lands **130**E and **130**G by utilizing this property. As a result, even if there is a variation in the supply amount of the solder pastes P**1** and P**2**, the allowable amount for the variation in the solder pastes P**1** and P**2** increases as the areas of the lands **130**E and **130**G are wider. Therefore, it is possible to prevent generation of side balls and the like in the solder bonding portions **191**A and **192**A, and as a result, it is possible to prevent short circuit defects in the solder bonding portions **191**A and **192**A.

Third Embodiment

[0109] A third embodiment will be described. FIG. **9** is a schematic cross-sectional view in which a portion of the processing module according to the third embodiment is enlarged. FIG. **9** schematically illustrates a cross section of a processing module **300**B according to the third embodiment. In the following description, the same components as those of the first embodiment are denoted by the same reference numerals, and detailed description thereof will be omitted.

[0110] The processing module **300**B according to the third embodiment includes the semiconductor device **100** having the same configuration as that of the first embodiment and a printed wiring board **200**B. Similarly to the first embodiment, the land **130**E that is the first land, the land **130**G that is the second land, and the land **130**S that is the fifth land are arranged on the main surface **122** of the insulating substrate **120** included in the semiconductor device **100**.

[0111] The printed wiring board **200**B has the insulating substrate **220** similar to that of the first embodiment. The insulating substrate **220** has a main surface **221** and a main surface **222** opposite to the main surface **221**. The land **230** is disposed on the main surface **221** of the insulating substrate **220** as in the first embodiment.

[0112] The printed wiring board **200**B includes a solder resist **208**B. The solder resist **208**B is a film made of a solder resist material. The solder resist **208**B is provided on the main surface **221**. The land **230** is exposed through an opening portion formed in the solder resist **208**B.

[0113] The processing module **300**B includes the capacitor **400** used as a bypass capacitor as in the first embodiment. The capacitor **400** is disposed on the main surface **221** side of the insulating substrate **220** of the printed wiring board **200**B, that is, between the semiconductor device **100** and the printed wiring board **200**B. The electrode **410** of the capacitor **400** is bonded to the land **130**E by a solder bonding portion **191**B that is a first solder bonding portion formed of solder. The electrode **420** of the capacitor **400** is bonded to the land **130**G by a solder bonding portion **192**B that is a second solder bonding portion made of solder. Thus, the electrode **410** of the capacitor **400** is electrically connected directly to the land **130**E of the semiconductor device **100** by the solder bonding portion **191**B. Therefore, the inductance of the wire between the electrode **410** of the capacitor **400** and the land **130**E can be reduced. The electrode **420** of the capacitor **400** is electrically connected directly to the land **130**G of the semiconductor device **100** by the solder bonding portion **192**B. Therefore, the inductance of the wire between the electrode **420** of the capacitor **400** and the land **130**G can be reduced. Since the inductance of the wire is reduced, the generated power supply noise is reduced, and a speed of communication in the semiconductor device **100** can be increased.

[0114] The land **130**S and land **230** are bonded to each other by a solder bonding portion **193**B that is a third solder bonding portion made of solder. In the third embodiment, the solder resist **208**B has an opening portion HB that exposes a portion **221**B of the main surface **221**.

[0115] FIG. **10**A is an exploded partial perspective view of the processing module **300**B according to the third embodiment. FIG. **10**B is a schematic diagram for explaining an arrangement relationship of the semiconductor device **100**, the capacitor **400**, and the printed wiring board **200**B when viewed in the Z direction. In FIGS. **10**A and **10**B, the solder bonding portions **191**B and **192**B are not illustrated. In FIG. **10**B, the lands **130**E and **130**G of the semiconductor device are indicated by broken lines.

[0116] As illustrated in FIG. **10**A, the upper surface **414** of the electrode **410** faces the land **130**E of the semiconductor device **100**, and the lower surface **415** of the electrode **410** faces the portion **221**B of the main surface **221** of the printed wiring board **200**B. The upper surface **424** of the electrode **420** faces the land **130**G of the semiconductor device **100**, and the lower surface **425** of the electrode **420** faces the portion **221**B of the printed wiring board **200**B.

[0117] As illustrated in FIG. **10**B, the land **130**E and the land **130**G are arranged at intervals in the X direction. The land **130**E overlaps at least a portion of the electrode **410** of the capacitor **400**, the entire electrode **410** in the third embodiment in a plan view, that is, viewed in the Z direction. When viewed in the Z direction, the land **130**G overlaps at least a portion of the electrode **420** of the capacitor **400**, and the entire electrode **420** in the third embodiment. In the third embodiment, the area S_{130E} of the land **130**E is larger than the area S_{410} of the electrode **410** as viewed in the Z direction. When viewed in the Z direction, an area S_{130G} of the land **130**G is larger than an area S_{420} of the electrode

420. The land **130**E and the land **130**G extend outward in the X direction from the capacitor **400** when viewed in the Z direction.

[0118] As illustrated in FIG. **9**, each of the solder bonding portions **191**B and **192**B has a fillet shape in which the outer surface expands away from the capacitor **400** as each of the solder bonding portions **191**B and **192**B extends from the portion **221**B exposed by the opening portion HB toward each of the lands **130**E and **130**G. More specifically, the solder bonding portion **191**B has a fillet shape expanding outward in the X direction from the electrode **410**, that is, in the X1 direction, as the solder bonding portion **191**B extends from the portion **221**B exposed by the opening portion HB toward the land **130**E. The solder bonding portion **192**B has a fillet shape that expands outward in the X direction from the electrode **420**, that is, in the X2 direction, as the solder bonding portion **192**B extends from the portion **221**B exposed by the opening portion HB toward the land **130**G. The X1 direction is a direction away from the electrode **410** in the X direction. The X2 direction is a direction opposite to the X1 direction in the X direction and is a direction away from the electrode **420**. As a result, the bonding strength between each of the lands **130**E and **130**G and each of the electrodes **410** and **420** increases. In addition, each of the solder bonding portions **191**B and **192**B is prevented from having a shape bulging in the X direction, and each of the solder bonding portions **191**B and **192**B is prevented from being short-circuited with the adjacent solder bonding portion **193**B.

[0119] In the third embodiment, as illustrated in FIG. **10**B, the area S_{HB} of the opening portion HB, that is, the area S_{221B} of the portion **221**B exposed by the opening portion HB is larger than the area S_{400} of the capacitor **400** as viewed in the Z direction. Therefore, as illustrated in FIG. **9**, a portion of the capacitor **400** in the Z direction is inserted into the opening portion HB, and the distance between the semiconductor device **100** and the printed wiring board **200**B is narrowed.

[0120] Next, a method of manufacturing the processing module **300**B will be described. FIGS. **11**A to **11**F are explanatory diagrams of the method of manufacturing the processing module **300**B according to the third embodiment. As illustrated in FIG. **11**A, the printed wiring board **200**B is prepared (Step S**21**). In Step S**21**, the semiconductor device **100** and the capacitor **400** are also prepared. Next, as illustrated in FIG. **11**B, the solder paste P**1** which is the first solder paste, the solder paste P**2** which is the second solder paste, and the solder paste P**3** which is the third solder paste are supplied onto printed wiring board **200**B at intervals (Step S**22**). In the third embodiment, in Step S**22**, the solder pastes P**1** and P**2** are supplied onto the portion **221**B exposed by the opening portion HB formed in the solder resist **208**B at intervals. In Step S**22**, the solder paste P**3** is supplied onto the land **230** of the printed wiring board **200**B.

[0121] In Step S**22**, the solder pastes P**1**, P**2**, and P**3** are supplied to the printed wiring board **200**B by screen printing using the metal mask **23**. The method for supplying the solder pastes P**1**, P**2**, and P**3** is not limited thereto. For example, the solder pastes P**1**, P**2**, and P**3** may be supplied to the printed wiring board **200**B by a dispenser.

[0122] Next, as illustrated in FIG. **11**C, the capacitor **400** prepared in Step S**21** is placed on printed wiring board **200**B such that the electrode **410** is in contact with the solder paste P**1** and the electrode **420** is in contact with the solder paste P**2** (Step S**23**). As a result, the lower surface **415** of the electrode **410** comes into contact with the solder paste P**1**, and the lower surface **425** of the electrode **420** comes into contact with the solder paste P**2**. It is not necessary to attach solder balls to the electrodes **410** and **420** of the capacitor **400** in advance.

[0123] Next, as illustrated in FIG. **11**D, the semiconductor device **100** prepared in Step S**21** is mounted on the printed wiring board **200**B such that the land **130**E faces the electrode **410** and the land **130**G faces the electrode **420** (Step S**24**). In Step S**24**, the semiconductor device **100** is placed on the printed wiring board **200**B to bring the solder balls B, which are ball terminals provided on the lands **130**S, into contact with the solder paste P**3**. In FIG. **11**D, the upper surface **414** of the electrode **410** and the land **130**E, and the upper surface **424** of the electrode **420** and the land **130**G are not in contact with each other, but these may be in contact with each other.

[0124] In Step S**24**, the positional relationship among the printed wiring board **200**B, the capacitor **400**, and the semiconductor device **100** as viewed from the Z direction is as illustrated in FIG. **10**B. When the capacitor **400** is placed on the printed wiring board **200**B, each of the land **130**E and the land **130**G of the semiconductor device **100** overlaps at least a portion of each of the electrode **410** and the electrode **420** when viewed in the Z direction, and extends outward in the X direction from the capacitor **400**.

[0125] Next, in a state where the semiconductor device **100** and the capacitor **400** are placed on the printed wiring board **200**B, the printed wiring board **200**B is conveyed to a reflow furnace (not illustrated). Then, in Step S**25-1** illustrated in FIG. **11**E, the temperature of the atmosphere in the reflow furnace is adjusted to a temperature equal to or higher than the melting point of the solder, and the solder pastes P**1**, P**2**, and P**3** and the solder ball B in FIG. **11**D are melted as illustrated in FIG. **11**E. The solder paste P**1** is melted to form a flowable molten solder M**1**, and the solder paste P**2** is melted to form a flowable molten solder M**2**. When the solder paste P**3** and the solder ball B are melted, a flowable molten solder M**3** is obtained.

[0126] Subsequent to Step S**25-1**, in Step S**25-2** illustrated in FIG. **11**F, heating is continued to cause the molten solders M**1** and M**2** to flow. As illustrated in FIG. **11**E, the molten solders M**1** and M**2** crawl up the side surfaces **411** and **421** in the upward direction indicated by the arrow Z**1**. Thereafter, the molten solders M**1** and M**2** move to the upper surfaces **414** and **424** as illustrated in FIG. **11**F. Although not illustrated in FIG. **11**, the molten solders M**1** and M**2** also crawl up in the upward direction indicated by the arrow Z**1** on the side surface **412**,**413** of the electrode **410** and the side surfaces **422** and **423** of the electrode **420**.

[0127] In addition, the capacitor **400** is pushed upward toward the semiconductor device **100** by the molten solders M**1** and M**2**, the distance between the upper surface **414** of the electrode **410** and the land **130**E is narrowed, and the distance between the upper surface **424** of the electrode **420** and the land **130**G is narrowed. The molten solders M**1** and M**2** reaching the upper surfaces **414** and **424** come into contact with the lands **130**E and **130**G, wet-spread on the lands **130**E and **130**G, and have a fillet shape in which the skirt widens as it goes from the solder resist **208**B toward the lands **130**E and **130**G.

[0128] Thereafter, the molten solders M**1** and M**2** wet-spread to the lands **130**E and **130**G are cooled and solidified.

As a result, the molten solder M1 is cooled and solidified in a fillet shape on the land 130E. The molten solder M2 is cooled and solidified in a fillet shape on the land 130G. At the same time, the molten solder M3 is also cooled and solidified. As a result, solder bonding portions 191B, 192B, and 193B are formed as illustrated in FIG. 9. As described above, the processing module 300B illustrated in FIG. 9 is manufactured.

[0129] Thereafter, the processing module 300B illustrated in FIG. 9 is housed in the casing 611 illustrated in FIG. 1, thereby manufacturing a camera body of a digital camera which is an example of the electronic equipment.

[0130] As described above, by melting the solder pastes P1 and P2 supplied to the printed wiring board 200B, the solder can be supplied to the lands 130E and 130G of the semiconductor device 100 via the electrode 410,420 of the capacitor 400. As a result, it is not necessary to form solder balls on the electrodes 410,420 of the capacitor 400 in advance, and the process of manufacturing the processing module 300B can be reduced. Therefore, since the processing module 300B can be easily manufactured, productivity of the processing module 300B is improved.

[0131] In the third embodiment, since a portion of the capacitor 400 is inserted into the opening portion HB, the height of the solder bonding portions 191B, 192B, and 193B in the Z direction, that is, the interval between the semiconductor device 100 and the printed wiring board 200B in the Z direction can be narrowed. Therefore, the amount of solder in the solder bonding portions 191B, 192B, and 193B can be reduced, and the manufacturing cost of the processing module 300B can be reduced.

Example 1

[0132] Example 1 corresponding to the first embodiment will be described. In the semiconductor device 100 illustrated in FIG. 3, a minimum pitch of the solder balls B (FIG. 5D), which are two adjacent unbonded ball terminals, was 0.4 [mm]. A material of the land 130 was Cu. A material of each of the solder bonding portion 191, 192, and 193 was Sn-3.0% Ag 0.5% Cu. The area S_{400} of the capacitor 400 as viewed from the Z direction illustrated in FIG. 4B was 0.4 [mm]×0.2 [mm]. That is, the capacitor 400 was a 0402 chip component.

[0133] A thickness of the metal mask 23 illustrated in FIG. 5B used in the manufacturing process of the processing module 300 was set to 0.08 [mm] from the minimum pitch of the solder balls B, which are the two adjacent ball terminals before bonding in the semiconductor device 100, and the size of the capacitor 400.

[0134] In Steps S5-1 and S5-2 illustrated in FIGS. 5E and 5F, the solder pastes P1, P2, and P3 were melted at a peak temperature of the atmosphere in the reflow furnace of 230° C. or higher. Thereafter, the molten solders M1, M2, and M3 were cooled and solidified. It was confirmed that the capacitor 400 was bonded to the semiconductor device 100 by the solder bonding portion 191,192. The solder bonding portion 191,192 had a fillet shape on the lands 130E and 130G.

[0135] The movement of the molten solders M1, M2, and M3 in Steps S5-1 and S5-2 was confirmed as follows by observation. First, the solder paste P3 and the solder ball B are integrally melted. At this time, the semiconductor device 100 moves toward the printed wiring board 200 by the molten solder M3 to be rounded. Meanwhile, since the molten solders M1 and M2 are not in contact with the land of the printed wiring board 200, the molten solders M1 and M2 move to the electrode 410,420 of the capacitor 400 and reach the upper surfaces 414 and 424 along the side surfaces 411 and 412. The capacitor 400 is raised with respect to the surface of the solder resist 208 by the molten solders M1 and M2. The raised amount depends on the amounts of the solder pastes P1 and P2, but was about 0.01 to 0.015 [mm] in Example 1. As a result, the upper surfaces 414 and 424 of the capacitor 400 are brought close to the lands 130E and 130G. The molten solders M1 and M2 reaching the upper surfaces 414 and 424 come into contact with the lands 130E and 130G, and wet-spread on the lands 130E and 130G. The movement of the molten solders M1, M2, and M3 as described above forms the solder bonding portion 191,192 having a fillet shape on the lands 130E and 130G.

Example 2

[0136] Example 2 corresponding to the second embodiment will be described. In the semiconductor device 100 illustrated in FIG. 6, a minimum pitch of the solder balls B (FIG. 8D), which are two adjacent unbonded ball terminals, was 0.4 [mm]. A material of the land 130 was Cu. The solder bonding portions 191A, 192A, and 193A were made of Sn-3.0% Ag 0.5% Cu. The area S_{400} of the capacitor 400 as viewed from the Z direction illustrated in FIG. 7B was 0.4 [mm]×0.2 [mm]. That is, the capacitor 400 was a 0402 chip component.

[0137] The sizes of the lands 130E and 130G in the semiconductor device 100 as viewed from the Z direction were set to 0.6 [mm]×0.22 [mm]. The sizes of the lands 230E and 230G in the printed wiring board 200A viewed from the Z direction were set to 0.5 [mm]×0.2 [mm]. The areas S_{130E} and S_{130G} of the lands 130E and 130G were 0.132 mm^2. The areas S_{230E} and S_{230G} of the lands 230E and 230G were 0.1 mm^2. As described above, the relationship between the areas S_{130E} and S_{130G} of the lands 130E and 130G and the areas S_{230E} and S_{230G} of the lands 230E and 230G is set as S_{230E} and $S_{230G}<S_{130E}$ and S_{130G}.

[0138] The amount of the solder pastes P1 and P2 was increased as compared with Example 1, and in order to confirm the fillet shape, the thickness of the metal mask 23 used in Step S12 illustrated in FIG. 8B was set to 0.10 [mm] thicker than 0.08 [mm].

[0139] Since the areas S_{130E} and S_{130G} of the lands 130E and 130G are larger than the areas S_{230E} and S_{230G} of the lands 230E and S 230G, the molten solders M1 and M2 wet-spread to the large areas of the lands 130E and 130G in Steps S15-1 and S15-2. Therefore, in Example 2, it was confirmed that generation of side balls and swelling of fillets were prevented in the solder bonding portions 191A and 192A, and short circuit defects were prevented.

Example 3

[0140] Next, a third example will be described. Example 3 corresponds to the first embodiment, but the materials of the lands 130E and 130G are different from those of Example 1.

[0141] The wettability of the molten solder in the lands 130E and 130G of the semiconductor device 100 is F1, and the wettability of the molten solder in the electrode 410,420 of the capacitor 400 is F2. In Example 3, the materials of the lands 130E and 130G of the semiconductor device 100 and the electrode 410,420 of the capacitor 400 were selected so

as to satisfy a relationship of F1≥F2. The wettability of the molten solder refers to ease of fitting of the molten solder.

[0142] In order for the molten solder to wet-spread on the surface of the electrode **410**,**420** of the capacitor **400** and the surfaces of the lands **130**E and **130**G of the semiconductor device **100**, it is important that the surfaces of the molten solder and the target metal are not contaminated. As the molten solder and the metal surface are cleaner, the interatomic distance therebetween becomes closer, and the molten solder wets and spreads on the metal surface so as to be in close contact with the metal surface. For this reason, the lands **130**E and **130**G of the semiconductor device **100** are subjected to Au plating which is hardly oxidized. In addition, the electrode **410**,**420** of the capacitor **400** is plated with Sn which is easily oxidized and has a low reduction rate.

[0143] The thickness of the metal mask **23** illustrated in FIG. **5**B was set to 0.05 [mm]. The supply amounts of the solder pastes P**1**, P**2**, and P**3** were smaller than those in Example 1. The sizes of the semiconductor device **100** and the capacitor **400** were the same as those in Example 1.

[0144] In Steps S**5**-**1** and S**5**-**2** in FIGS. **5**E and **5**F, it was confirmed that the molten solders M**1** and M**2** moved from the Sn-plated electrode **410**,**420** to the lands **130**E and **130**G on which the Au plating with high wettability was applied. As a result, it was confirmed that the capacitor **400** was favorably bonded to the semiconductor device **100** by the solder bonding portion **191**,**192**.

(Calculation of Inductance)

[0145] Next, the inductance of the wiring between the semiconductor element and the capacitor was calculated for Example 1, Example 2, and Comparative Example 1. FIG. **12**A is a schematic cross-sectional view of the processing module **300** of Example 1. FIG. **12**B is a schematic cross-sectional view of the processing module **300**A of Example 2. FIG. **12**C is a schematic cross-sectional view of a processing module **300**X of Comparative Example 1.

[0146] The processing module **300**X of Comparative Example 1 illustrated in FIG. **12**C includes the semiconductor device **100**, the capacitor **400**, and a printed wiring board **200**X. The semiconductor device **100** includes the semiconductor element **101** and the package substrate **102**. The semiconductor element **101** is mounted on the package substrate **102**. The package substrate **102** includes the land **130**E and a land **130**G.

[0147] The printed wiring board **200** includes an insulating substrate **220**X. The insulating substrate **220**X has one main surface and the other main surface opposite to the one main surface. Land **230**EX and land **230**GX are disposed on one main surface of the insulating substrate **220**X. Land **130**E and land **230**EX are bonded by a solder bonding portion **191**X. Land **130**G and land **230**GX are bonded by a solder bonding portion **192**X.

[0148] The capacitor **400** is disposed on the other main surface side of the insulating substrate **220**X of the printed wiring board **200**X. A land **240**EX bonded to the electrode **410** of the capacitor **400** by solder and a land **240**GX bonded to the electrode **420** of the capacitor **400** by solder are disposed on the other main surface of the insulating substrate **220**X. The land **230**EX and the land **240**EX are electrically connected by a via conductor **291**X formed on the insulating substrate **220**X. The land **230**GX and the land **240**GX are electrically connected by the via conductor **292**X formed on the insulating substrate **220**X.

[0149] Calculation conditions are illustrated below. In the semiconductor device **100** which is a BGA semiconductor package, the pitch between two adjacent ball terminals was set to 0.4 [mm]. The thickness of the package substrate **102** was set to 0.4 [mm]. Each of the solder bonding portions **193**, **193**A, **191**X, and **192**X had a height of 0.220 [mm] and a width of 0.250 [mm]. The capacitor **400** was a 0402 size chip capacitor. The thickness of each of the printed wiring boards **200**,**200**A, **200**X was set to 0.8 [mm]. For the calculation of the inductance, a calculation formula of the inductance in the parallel conducting wire was used.

[0150] A calculation result of Example 1 illustrated in FIG. **12**A will be described. The inductance value of each of the via conductors **112**E and **112**G in the package substrate **102** was 266 pH. Each of the inductance value between the electrode **410** of the capacitor **400** and the land **130**E and the inductance value between the electrode **420** of the capacitor **400** and the land **130**G was 180 pH. Therefore, each of the inductance value between the power terminal **111**E of the semiconductor element **101** and the electrode **410** of the capacitor **400** and the inductance value between the ground terminal **111**G of the semiconductor element **101** and the electrode **420** of the capacitor **400** was 466 pH. The calculation result of Example 2 illustrated in FIG. **12**B was similar to that of Example 1.

[0151] A calculation result of Comparative Example 1 illustrated in FIG. **12**C will be described. The inductance value of each of the via conductors **112**E and **112**G in the package substrate **102** was 266 pH. The inductance value of each of the solder bonding portions **191**X and **192**X was 42 pH. The inductance value of each of the via conductors **291**X and **292**X in the printed wiring board **200**X was 545 pH. Each of the inductance value between the electrode **410** of the capacitor **400** and the land **240**EX and the inductance value between the electrode **420** of the capacitor **400** and the land **240**GX was 180 pH. Therefore, each of the inductance value between the power terminal **111**E of the semiconductor element **101** and the electrode **410** of the capacitor **400** and the inductance value between the ground terminal **111**G of the semiconductor element **101** and the electrode **420** of the capacitor **400** was 1033 pH.

[0152] FIG. **13** illustrates calculation results of inductances in Example 1, Example 2, and Comparative Example 1. As illustrated in FIG. **13**, in Examples 1 and 2, the inductance value is smaller than that of Comparative Example 1. As a result, the generated power supply noise is reduced, and it is possible to realize high-speed communication in the semiconductor device **100**. In Example 2, as illustrated in FIG. **12**B, the semiconductor device **100** and the printed wiring board **200**A are connected by the solder bonding portions **191**A and **192**A via the capacitor **400**. As a result, power can be supplied to the semiconductor element **101** via the solder bonding portions **191**A and **192**A. Therefore, the land **130**S can be used for applications other than the power supply line, and the degree of freedom in circuit design is increased.

[0153] As described above, it is possible to manufacture a processing module that realizes high-speed communication without adding a manufacturing process.

[0154] Note that the present invention is not limited to the embodiments described above, and many modifications can be made within the technical idea of the present invention.

In addition, the effects described in the embodiments merely enumerate the most suitable effects resulting from the present invention, and the effects according to the present invention are not limited to those described in the embodiments.

[0155] In the above-described embodiments, the case where the electronic component is the capacitor **400** has been described, but the present invention is not limited thereto. The electronic component may be a passive component such as a resistor or an inductor.

[0156] In the above-described embodiments, the semiconductor device **100** in which the solder balls B are provided on the land **230**S is prepared in advance, but the present invention is not limited thereto. That is, in the step of preparing the semiconductor device **100**, the solder balls S may be provided on the land **230**S.

[0157] While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. A semiconductor module manufacturing method comprising:

preparing a chip component comprising a first electrode and a second electrode disposed at intervals in a predetermined direction, a semiconductor device comprising a first land and a second land, and a printed wiring board;

supplying a first solder paste and a second solder paste to the printed wiring board at intervals;

placing the chip component on the printed wiring board such that the first electrode is in contact with the first solder paste and the second electrode is in contact with the second solder paste;

placing the semiconductor device on the printed wiring board such that the first land faces the first electrode and the second land faces the second electrode;

heating and melting the first solder paste and the second solder paste; and

bonding the first land and the first electrode to each other with solder and bonding the second land and the second electrode to each other with solder by cooling and solidifying wet-spread molten solder to each of the first land and the second land.

2. The semiconductor module manufacturing method according to claim **1**,

wherein, in the placing the semiconductor device, each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode in a plan view, and extends outward in the predetermined direction from the chip component.

3. The semiconductor module manufacturing method according to claim **1**,

wherein, in the bonding, the wet-spread molten solder obtained by melting the first solder paste is cooled and solidified into a fillet shape on the first land, and the wet-spread molten solder obtained by melting the second solder paste is cooled and solidified into a fillet shape on the second land.

4. The semiconductor module manufacturing method according to claim **1**,

wherein the printed wiring board comprises an insulating substrate and a solder resist disposed on a main surface of the insulating substrate, and

the first solder paste and the second solder paste are supplied onto the solder resist.

5. The semiconductor module manufacturing method according to claim **1**,

wherein the printed wiring board comprises an insulating substrate, and a third land and a fourth land disposed on a main surface of the insulating substrate, and

in the supplying, the first solder paste is supplied onto the third land, and the second solder paste is supplied onto the fourth land.

6. The semiconductor module manufacturing method according to claim **5**,

wherein in a plan view, an area of the first land is larger than an area of the third land, and an area of the second land is larger than an area of the fourth land.

7. The semiconductor module manufacturing method according to claim **1**,

wherein the printed wiring board comprises an insulating substrate and a solder resist disposed on a main surface of the insulating substrate,

the solder resist has an opening portion that exposes a portion of the main surface of the insulating substrate, and

the first solder paste and the second solder paste are supplied to a portion exposed through the opening portion on the main surface of the insulating substrate.

8. The semiconductor module manufacturing method according to claim **1**,

wherein the semiconductor device comprises a fifth land provided with a solder ball, and the printed wiring board comprises a sixth land,

the method further comprising:

supplying a third solder paste onto the sixth land in a case of supplying the first solder paste and the second solder paste in the printed wiring board;

placing the semiconductor device on the printed wiring board to bring the solder ball into contact with the third solder paste;

heating and melting the third solder paste and the solder ball together with the first solder paste and the second solder paste; and

bonding the fifth land and the sixth land to each other with solder by cooling and solidifying the molten solder.

9. The semiconductor module manufacturing method according to claim **1**,

wherein the semiconductor device is a BGA semiconductor package.

10. An electronic equipment manufacturing method comprising:

manufacturing the semiconductor module by the manufacturing method according to claim **1**; and

disposing the semiconductor module inside a casing.

11. A semiconductor module comprising:

a printed wiring board;

a semiconductor device comprising a first land and a second land, the semiconductor device being mounted on the printed wiring board;

a chip component comprising a first electrode and a second electrode spaced apart from each other in a

predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device;
a first solder bonding portion that bonds the first electrode and the first land to each other; and
a second solder bonding portion that bonds the second electrode and the second land to each other,
wherein the printed wiring board comprises an insulating substrate and a solder resist disposed on a main surface of the insulating substrate,
the chip component faces the solder resist,
each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode in a plan vie and extends outward in the predetermined direction from the chip component,
the first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from the solder resist, and
the second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the solder resist.

12. A semiconductor module comprising:
a printed wiring board;
a semiconductor device comprising a first land and a second land, the semiconductor device being mounted on the printed wiring board;
a chip component comprising a first electrode and a second electrode spaced apart from each other in a predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device;
a first solder bonding portion that bonds the first electrode and the first land to each other; and
a second solder bonding portion that bonds the second electrode and the second land to each other,
wherein the printed wiring board comprises an insulating substrate, a third land disposed on a main surface of the insulating substrate and electrically connected to the first land by the first solder bonding portion, and a fourth land disposed on the main surface of the insulating substrate and electrically connected to the second land by the second solder bonding portion,
in a plan view, each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode, overlaps at least a portion of each of the third land and the fourth land, and extends outward in the predetermined direction from the chip component,
the first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from the third land, and
the second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the fourth land.

13. A semiconductor module comprising:
a printed wiring board;
a semiconductor device comprising a first land and a second land, the semiconductor device being mounted on the printed wiring board;
a chip component comprising a first electrode and a second electrode spaced apart from each other in a predetermined direction, the chip component being disposed between the printed wiring board and the semiconductor device;
a first solder bonding portion that bonds the first electrode and the first land to each other; and
a second solder bonding portion that bonds the second electrode and the second land to each other,
wherein the printed wiring board comprises an insulating substrate and a solder resist disposed on a main surface of the insulating substrate,
the solder resist has an opening portion into which a portion of the chip component is inserted,
each of the first land and the second land overlaps at least a portion of each of the first electrode and the second electrode in a plan view and extends outward in the predetermined direction from the chip component,
the first solder bonding portion has a fillet shape in which the first solder bonding portion spreads outward in the predetermined direction from the first electrode as the first solder bonding portion extends toward the first land from a portion of the main surface of the insulating substrate exposed by the opening portion of the solder resist, and
the second solder bonding portion has a fillet shape in which the second solder bonding portion spreads outward in the predetermined direction from the second electrode as the second solder bonding portion extends toward the second land from the portion of the main surface of the insulating substrate exposed by the opening portion of the solder resist.

14. The semiconductor module according to claim **11**,
wherein the first land is a power terminal, and the second land is a ground terminal.

15. The semiconductor module according to claim **11**,
wherein the chip component is a chip component of 0402 size or less.

16. The semiconductor module according to claim **11**,
wherein the chip component is a capacitor.

17. The semiconductor module according to claim **11**,
wherein the semiconductor device is a BGA semiconductor package in which an interval between lands is 0.4 mm or less.

18. The semiconductor module according to claim **11**,
wherein the semiconductor device comprises a semiconductor element, and
the semiconductor element and the chip component overlap each other in a plan view of the semiconductor module.

19. The semiconductor module according to claim **11**, further comprising, a third solder bonding portion that bonds a fifth land and a sixth land,
wherein the semiconductor device comprises the fifth land,
the printed wiring board comprises the sixth land on a main surface of the insulating substrate, and

a height of the third solder bonding portion is higher than a height of the chip component.

20. Electronic equipment comprising:

a casing; and

the semiconductor module according to claim **11** disposed inside the casing.

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