

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 December 2006 (21.12.2006)

PCT

(10) International Publication Number
WO 2006/133731 A1

(51) International Patent Classification:
H04L 25/02 (2006.01)

(21) International Application Number:
PCT/EP2005/008262

(22) International Filing Date: 17 June 2005 (17.06.2005)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US):
FREESCALE SEMICONDUCTOR, INC. [US/US];
6501 William Cannon Dr., Austin, TX 78735 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **HEMON, Erwan**
[FR/FR]; 21 Impasse des Palombes, F-31120 Goyrans
(FR).

(74) Agent: **WRAY, Antony, John**; Freescale Semiconductor,
Inc., Impetus IP Limited, Grove House, Lutyens Close,
Chineham Court, Basingstoke, Hampshire RG24 8AG
(GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

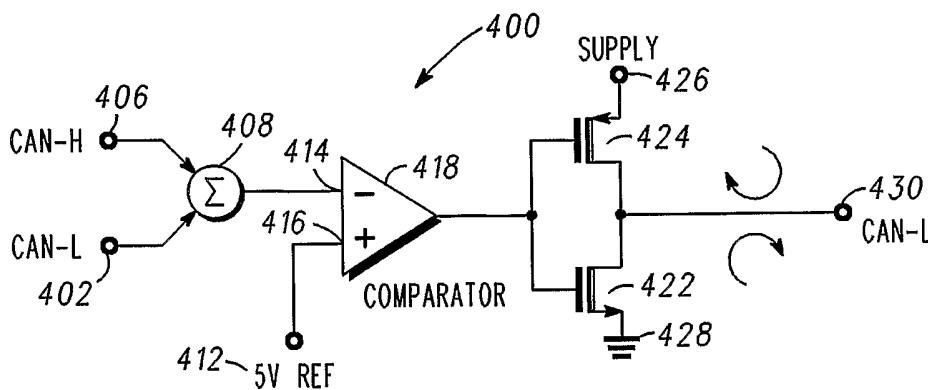
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- with amended claims and statement

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND METHOD THEREFOR



(57) Abstract: A communication system comprises a twisted pair communication link operably coupled to at least two driver stages for providing at least two independent input signals on the twisted pair communication link (400). The at least two independent input signals on the twisted pair communication link are summed and input to a comparator (418) arranged to compare the summed signal to a reference value. The output of the comparator (418) is input to the at least two driver stages. The outputs from the at least two driver stages are summed and fed back and summed with one or more of the independent input signals. In this manner, adverse effects due to non-ideal symmetry between components in a twisted pair communication link, such as a Controller Area Network (CAN) system, are reduced.

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TWISTED PAIR COMMUNICATION SYSTEM, APPARATUS AND
METHOD THEREFOR**Field of the Invention**

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The preferred embodiment of the present invention relates to reduction of emission level in a twisted pair communication system. The invention is applicable to, but not limited to, provision of a high speed two-wire
10 CAN network.

Background of the Invention

In the field of vehicle electronics, the use of a high
15 speed controller area network (CAN) is becoming ever more prevalent. In a typical automotive application, the CAN provides a two-wire multiplex communication link that can be routed around the vehicle. Thus, the CAN provides a simple mechanism for a vehicle processing unit to
20 communicate effectively with remote electrical/signal processing units, e.g. vehicle light modules, braking system, airbag modules, etc.

The CAN specifications for road vehicles are defined by
25 the International Standards Organisation (ISO), as described below.

- (i) ISO 11898-2: high speed physical layer - part 2;
- (ii) ISO 11898-3: low speed fault tolerant physical layer - part 3;
- 30 (iii) ISO 11898-4: time trigger CAN; and
- (iv) ISO 11898-5: high speed physical layer with low power mode and wake up.

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The CAN specifications support communication over, say, a ten metre length. However, in requiring the CAN bus to support communication over this length, the long wires act as an antenna and as such are effectively subject to
5 automotive electrical transients, as well as industrial transients, such as electro-magnetic interference (EMI) and electro-static discharge (ESD).

Furthermore, as the wires can be very long, the control
10 of the slew rate of signals routed by the wires is also known to be very critical to avoid any EMC emission. In addition, in order to operate the CAN bus successfully, in a problematic vehicle environment; a CAN transceiver must also be able to withstand high voltage transients.

15
Consequently, it is important to guarantee a good control and matching of the respective devices between the switching of the two CAN wires. To guarantee good matching of the slew rate between the respective wires,
20 the two wires (i.e. the high-side CAN (CAN-H) and the low-side CAN (CAN-L)) must be matched in performance and controlled equally.

A typical CAN driver circuit is illustrated in FIG. 1.
25 The CAN driver circuit comprises a digital transmit input signal 102 that is input to both the CAN-H driver 104 and a CAN-L driver 106. In order to achieve both high-speed and symmetry of operation, low-voltage matched components are generally used. The CAN-H driver utilizes, say, a
30 pnp transistor 130 as an active device operably coupled to Vcc 108, where as the CAN-L driver utilizes, say, a npn transistor 132 as an active device, operably coupled to ground 110.

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The respective outputs 118, 120 from the CAN-H and CAN-L drivers 104, 106 are input 114, 116 to a comparator 112. The output from the comparator 112 is a 'receive' digital output signal 122. Thus, as will be appreciated by a skilled artisan, the driver circuits that control the signals on the CAN-H wire 118 and CAN-L wire 120 need to be carefully matched, to ensure that the CAN-H driver 104 and CAN-L driver 106 are adjusted to switch between the CAN-H and CAN-L wires 118, 120 in phase. A key aspect to using such a twisted cable is to ensure the current contained in the wires (in both directions) is of equal amplitude and of opposite sign. In this manner, the magnetic field produced, which is proportional to the current, is substantially zero. Thus, electro-magnetic interference due to the current in the twisted pair of cables is minimized. Clearly, any asymmetry between the current in the two wires produces a magnetic field, which is highly undesirable.

20

In addition, it is known that the common-mode CAN-H bus wire and CAN-L bus wire must also be constant during the switching transition, i.e. when a signal appears on the CAN-H and CAN-L wires, and when it is taken off. Thus, the ΔI needs to be minimized during the transitions otherwise electro-magnetic interference is created. In effect, there are two types of common-mode configuration:

(i) Current: where the current value of both the CAN-H and CAN-L wires should be equal but of opposite sign; and

30

(ii) Voltage: which should be equal, given that the for high speed operation the bus impedance is specified as 60 ohms in the CAN standard.

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Furthermore, to avoid EMC emission, the slew rate applied to signals on the CAN-H bus wire 118 and the CAN-L bus wire 120 must be controlled and matched. The slew rate is a function of the temperature (delay) and of the load. Consequently, the slew rate is difficult to control accurately.

A graphical example of how difficult it is to achieve a good match between the high-side driver and the low-side driver is shown in FIG. 2. Here, the transmit waveform signal 202 is shown with a slight offset to the receive waveform signal 222. If the respective driver circuits are symmetrical, the CAN-H and CAN-L signals in waveform 218 are also symmetrical, resulting in the summation of CAN-H (nominally 3.5V) and CAN-L (nominally 1.5V) values to be flat, at approximately 5V. The summation of the CAN-H and CAN-L signals is often referred to as the 'common mode'. However, when the driver circuits are not completely matched, the symmetry between CAN-H and CAN-L during transitions is not met. This lack of matching results in a so-called common-mode glitch 230 (say a variation of the order of 120mV), which is noticeable upon the summation of the CAN-H and CAN-L values.

25

A solution to this problem is illustrated in the known prior art circuit 300 of FIG. 3, with the use of multiple drivers 316, 318, 320, 322 for the CAN-H and drivers 324, 326, 328 and 330 for CAN-L. A series of very fast switches 336, 338, 340, 342, 344, 346, 348 and 350 are operably coupled to respective serial resistances, where each driver operation is controlled by a fixed delay 304, 306, 308, 310, 312 and 314.

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In this regard, the slew rate is fixed by the delay elements 304, 306, 308, 310, 312 and 314, the series resistances and the load capacitance. Accurate selection
5 of these components ensures a good match.

However, with a high voltage range on the output, non symmetrical clamping is (due to the inherent nature of the components) introduced in series with resistance.
10 These high voltage components can be designed to be somewhat symmetrical at low frequencies. However, they will exhibit asymmetry at higher frequencies, say above 100 KHz. Thus, asymmetry of signals between the two wires will generate common-mode glitches at a frequency
15 of above 100 KHz. In effect, a new common-mode (i.e. the summation of the values of the CAN-H and CAN-L wires) exists at each frequency of operation.

European Patent EP 0955750, titled "Line driver with parallel driver stages" by Texas Instruments, as well as
20 European Patent EP0763917 titled "Line driver with pulse shaper" by Lucent Technologies Inc. US5194761 illustrates prior art CAN arrangements.

25 However, it is recognised that, in order to sustain higher and higher voltage levels during fault conditions, it is no longer possible to use low voltage components. Thus, instead, high voltage components are required to be used, particularly components that exhibit higher
30 parasitic effects. Notably, and problematically, the parasitic components exhibit different characteristics for the high side driver (CAN-H) and the low side driver (CAN-L) outputs. Consequently, the common-mode

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performance becomes degraded with those high voltage components.

Thus, a need exists for an improved twisted-pair based
5 communication system, apparatus and method therefor, particularly to drive CAN-H and CAN-L bus wires.

Statement of Invention

10 In accordance with preferred aspects of the present invention, there is provided a communication system, an apparatus and method therefor to reduce emission levels due to non-ideal symmetry between components in twisted pair paths, as defined in the appended Claims.

15

Brief Description of the Drawings

FIG. 1 illustrates a known CAN driver circuit;

20 FIG. 2 shows a graphical example illustrating the difficulty in achieving a good match between a CAN-H driver and a CAN-L driver in a CAN bus system; and

FIG. 3 illustrates a known multiple CAN driver circuit
25 that aims to provide a good match between a CAN-H driver and a CAN-L driver.

Exemplary embodiments of the present invention will now
be described, by way of example only, with reference to
30 the accompanying drawings, in which:

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FIG. 4 illustrates a CAN driver circuit in accordance with the preferred embodiment of the present invention; and

5 FIG. 5 illustrates graphically how the circuit of FIG. 4 provides a reduction in the common-mode error in accordance with the preferred embodiment of the present invention.

10 **Description of Preferred Embodiments**

Referring now to FIG. 4, a CAN driver circuit is illustrated in accordance with the preferred embodiment of the present invention. Notably, the CAN-H signal 406 and the CAN-L signal 402 are input to a summation function 408. It is envisaged that the summation function may be implemented in a variety of ways, such as a summing block, discrete logic gates, AC coupling capacitors, etc. The CAN-H signal 406 and the CAN-L signal 402 are thus summed and input 414 to a fast comparator 418 at, say, a negative input port 414.

A reference voltage level 412 is applied to the positive input port 416 of the comparator. The comparator 418 compares the summation of CAN-H and CAN-L signals with a reference voltage 412, which in the preferred embodiment is set at 5V. The comparator 418 outputs the comparison to both a CAN-H driver stage 424 and a CAN-L driver stage pair 422, 424. The CAN-H driver stage 424 is coupled to a supply voltage 426 and the CAN-L driver stage 422 is coupled to ground 428.

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Although the preferred embodiment of the present invention is described with respect to using NMOS and PMOS transistors 422, 424 at the output of the comparator 418 to generate a CAN-L feedback signal, it is envisaged that these devices may be replaced by equivalent functions, such as switches or current sources or current sources with resistors coupled thereto, etc.

Notably, the output from both the CAN-H driver stage 424 and the CAN-L driver stage 422 is summed and provided as a feedback signal to either the CAN-H or CAN-L (or indeed both) signal(s). In comparing the summation of 'CAN-H + CAN-L' to a reference voltage applied to the comparator, the output of the comparator flips as soon as the summation goes above or below the reference value. Thus, dependent upon the comparison of the common-mode (summation of CAN-H and CAN-L, nominally 5V) value to the reference value (of 5V), current is either drawn from the CAN-L or pushed into the CAN-L feedback path to compensate for the difference. In this manner, the value of 'CAN-H + CAN-L' is either decreased or increased via the feedback path.

The speed of the comparator defines the reaction time of this loop, and thus the difference between the summation of 'CAN-H + CAN-L' and the reference voltage.

Thus, in this manner, a mechanism to improve the performance of the CAN circuit 400 is described by summing the CAN-H signal 406 and CAN-L signal 402 and using a fast, continuously-operating comparator 418, e.g. one that provides sufficient speed and low offset between the two wires. Thereafter, the output from the

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comparator 418 is fed back to one or both of the CAN signals 406, 402. A typical (CMOS) comparator error of 10 mV will result in a common-mode glitch of 10 mV.

5 Furthermore, in this implementation, the current compensation is limited to, say, 10% of the total current, to avoid an adverse affect on the performance (e.g. slew rate, propagation time, etc.) when the compensation system is disturbed by EMC perturbation
10 (BCI, DPI, etc.).

In a CAN system, the transition rise time and fall time of the CAN-H and CAN-L signals has to be typically between 15 nsec and 35 nsec at a speed of 1M baud. Thus,
15 it is envisaged that if the two CAN wires cannot be accurately matched using a single driver stage, a series of respective driver stages may be used, where the series of small stages are located in parallel, as per the known system in FIG. 3.

20 In this regard, several stages may be sequentially triggered in parallel. For example, if 10 stages are located in series, for each of the parallel CAN-H and CAN-L paths, the comparator may need to switch between
25 the stages every 1.5 nsec to 3.5 nsec per transition. Hence, in this regard, a switching performance of the comparator of between 1nsec and 5nsec is likely to be acceptable.

30 Although, the preferred embodiment of the present invention is described with reference to a continuously-operating comparator, it is envisaged that the inventive concept is equally applicable to a 'time-discrete'

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comparator, as would be understood by a skilled artisan. In this context, a 'time-discrete' comparator would encompass a 'sample & hold' type of comparator, whereby values of the CAN-H and CAN-L signals are sampled and held and then compared in a time-discrete manner. Advantageously, a number of 'sample & hold' comparators offer an offset-cancellation technique. The use of an offset-cancellation technique allows the removal of any common-mode glitch that occurs due to the comparator offset.

It is also envisaged that known cancellation techniques may be applied to continuously-operating comparators such that they also can implement cancellations of common-mode glitches due to a comparator offset.

In an enhanced embodiment of the present invention, it is envisaged that the common-mode glitch problem is only applied during transition stages of the CAN system. In this regard, it is envisaged that the feedback circuitry is enabled at the start of a transition and disables after the transition has ended. Advantageously, employing such a time-multiplexed arrangement assists in minimising disturbances in the CAN system caused by the aforementioned circuitry.

The use of a fast comparator in this manner compensates for any real-time imbalance between the signal values on the CAN-H and CAN-L wires, thereby facilitating a dramatic reduction in emission level by limiting the common-mode glitch that occurs during transition on the bus lines.

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Advantageously, the current output capability of the CAN compensation circuit is limited to a certain (low) value, in contrast to the main CAN-L and CAN-H capabilities. Indeed the slew rate on (CAN-H or CAN-L) is directly proportional to the output current. Thus, by using a series of smaller MOSFETs, any variation of current in, say, the CAN-L line causes minimal modification to the slew rate. Consequently, it is an advantage to limit the current transition, particularly in vehicular applications, to minimise the effect of radiated emissions due to, say, mobile antenna(s) or portable TVs.

At each stage transition, the comparator 418 thus compensates the intrinsic error of common-mode 'CAN-H + CAN-L' by continuously adding or subtracting current in order to keep a common-mode value substantially equal to the reference value 412. By ensuring that the summation value of 'CAN-H + CAN-L' is made substantially equal to a predefined reference value, any electromagnetic emission resulting from using a twisted pair of wires (as per the CAN system) is effectively reduced, i.e. the magnetic fields generated by each wire are opposed in sign and therefore the resultant value of the summation is substantially 'zero'.

25

Referring now to FIG. 5, a graph illustrates how the circuit of FIG. 4 provides a reduction in the common-mode error in accordance with the preferred embodiment of the present invention. FIG. 5 illustrates a transition between CAN-H and CAN-L signals, and in particular the correction current that maintains a low glitch level.

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Although the preferred embodiment of the present invention has been described with reference to a CAN circuit, it is envisaged that, for alternative applications, the inventive concept may be applied to any communication system that employs twisted pair cabling, such as those used by Ethernet transceivers.

It will be understood that the communication system, apparatus and method for reducing emission levels in a two-wire communication system, such as a CAN system as described above, aims to provide at least one or more of the following advantages:

- (i) Improve the non-ideal symmetry on CAN-H, CAN-L drivers;
- (ii) Reduce the reliance on matched components within the device used between the two wires;
- (iii) The common-mode glitch problem associated with bus transitions is better controlled;
- (iv) The preferred embodiment is very robust to process variations, due to the introduction of the feedback loop;
- (v) The EMC emission is dramatically reduced; and
- (vi) The circuit of the preferred embodiment is such that it is very easy to reuse on other applications/ technologies; i.e. substantially no software/ hardware modifications are required.

In particular, it is envisaged that the aforementioned inventive concept can be applied by a semiconductor manufacturer to any device or integrated circuit for use in any communication system employing twisted cabling. It is further envisaged that, for example, a semiconductor manufacturer may employ the inventive

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concept in a design of a stand-alone device, such as an Ethernet transceiver, or an embedded module in an application-specific integrated circuit (ASIC) and/or any other sub-system element.

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Whilst the specific and preferred implementations of the embodiments of the present invention are described above, it is clear that one skilled in the art could readily apply variations and modifications of such an inventive

10

concept.

Thus, an improved twisted pair communication system, apparatus and method therefor; to reduce emission levels due to non-ideal symmetry between components in the
15 respective twisted pair paths have been described, wherein the aforementioned disadvantages with prior art arrangements have been substantially alleviated.

Claims (PCT)

1. A communication system comprising a twisted pair communication link operably coupled to at least two driver stages for providing at least two independent input signals on the twisted pair communication link (400), wherein the communication system is characterised in that the at least two independent input signals on the twisted pair communication link are summed and input to a comparator (418) arranged to compare the summed signal to a reference value, wherein the output of the comparator (418) is input to the at least two driver stages and the outputs from the at least two driver stages are summed and fed back and summed with one or more of the independent input signals.

2. A communication system according to Claim 1 further characterised in that the communication system supports a Controller Area Network (CAN) communication.

3. A communication system according to Claim 1 or Claim 2 further characterised in that the comparator (418) and at least two driver stages are arranged to compensate for common-mode error by adding or subtracting current (430) to be summed with the one or more of the independent input signals to substantially track the reference value (412).

4. A communication system according to any preceding Claim further characterised in that the comparator (418) is fast continuously-operating comparator or a 'time-discrete' comparator.

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5. A communication system according to any preceding Claim further characterised in that the communication system encompasses a plurality of output stages of the twisted pair communication link (400) arranged in parallel to produce one of a CAN-H output and/or one CAN-L output.

6. A communication system according to Claim 5 further characterised in that the plurality of stages are turned on in sequence.

7. Apparatus for a communication circuit (400) comprising a twisted pair communication link (402, 406) operably coupled to at least two driver stages (422, 424) for providing at least two independent input signals on the twisted pair communication link (402, 406), wherein the apparatus (400) is characterised in that the independent signals on the twisted pair communication link (402, 406) are summed and input to a comparator (418) that compares the summed signal to a reference value (412), wherein the output of the comparator (418) is input to the at least two driver stages (422, 424) and the output from the at least two driver stages (422, 424) is summed and fed back and summed with one or more of the independent input signals.

8. Apparatus for a communication circuit (400) according to Claim 7 further characterised in that the apparatus supports Controller Area Network (CAN) communication.

9. Apparatus according to Claim 7 or Claim 8 further characterised in that the comparator (418) and at least

two driver stages are arranged to compensate for common-mode error by adding or subtracting current (430) to be summed with the one or more of the independent input signals to substantially track the reference value (412).

5

10. Apparatus according to any of preceding Claims 7 to 9 further characterised in that the comparator (418) is fast continuously-operating comparator or a 'time-discrete' comparator.

10

11. Apparatus according to any of preceding Claims 7 to 10 further characterised in that the communication system encompasses a plurality of output stages of the twisted pair communication link (400) arranged in parallel to produce one of a CAN-H output and/or one CAN-L output.

15

12. Apparatus according to Claim 11 further characterised in that the plurality of stages are turned on in sequence.

20

13. A method of reducing common-mode error in a communication system comprising a twisted pair communication link comprising the steps of:

25 providing at least two independent input signals on the twisted pair communication link,

wherein the method is characterised by the steps of:

combining the at least two independent input signals on the twisted pair communication link (400);

30 comparing the summed signal to a reference value;

inputting the output of the comparator (418) to at least two driver stages;

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combining the outputs from the at least two driver stages; and

feeding back the summed output from the at least two driver stages to one or more of the independent input
5 signals.

AMENDED CLAIMS**received by the International Bureau on 27 April 2006 (27.04.06)****Claims (PCT)**

1. A communication system comprising a twisted pair communication link operably coupled to at least two driver stages (422, 424) for providing at least two independent input signals (402, 406) on the twisted pair communication link, wherein the communication system is characterised in that the at least two independent input signals (402, 406) on the twisted pair communication link are summed and input to a comparator (418) arranged to compare the summed signal to a reference value (412), wherein the output of the comparator (418) is input to the at least two driver stages (422, 424) and the outputs from the at least two driver stages (422, 424) are summed and fed back and summed with one or more of the independent input signals (402, 406).

2. A communication system according to Claim 1 further characterised in that the communication system supports a Controller Area Network (CAN) communication.

3. A communication system according to Claim 1 or Claim 2 further characterised in that the comparator (418) and at least two driver stages are arranged to compensate for common-mode error by adding or subtracting current (430) to be summed with the one or more of the independent input signals to substantially track the reference value (412).

4. A communication system according to any preceding Claim further characterised in that the comparator (418)

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is fast continuously-operating comparator or a 'time-discrete' comparator.

5 5. A communication system according to any preceding Claim further characterised in that the communication system encompasses a plurality of output stages of the twisted pair communication link (400) arranged in parallel to produce one of a CAN-H output and/or one CAN-L output.

10

6. A communication system according to Claim 5 further characterised in that the plurality of stages are turned on in sequence.

15 7. Apparatus for a communication circuit (400) comprising a twisted pair communication link operably coupled to at least two driver stages (422, 424) for providing at least two independent input signals (402, 406) on the twisted pair communication link, wherein the apparatus is characterised in that the independent
20 signals (402, 406) on the twisted pair communication link are summed and input to a comparator (418) that compares the summed signal to a reference value (412), wherein the output of the comparator (418) is input to the at least
25 two driver stages (422, 424) and the outputs from the at least two driver stages (422, 424) are summed and fed back and summed with one or more of the independent input signals (402, 406).

30 8. Apparatus for a communication circuit (400) according to Claim 7 further characterised in that the

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apparatus supports Controller Area Network (CAN) communication.

9. Apparatus according to Claim 7 or Claim 8 further
5 characterised in that the comparator (418) and at least
two driver stages are arranged to compensate for common-
mode error by adding or subtracting current (430) to be
summed with the one or more of the independent input
signals to substantially track the reference value (412).

10

10. Apparatus according to any of preceding Claims 7
to 9 further characterised in that the comparator (418)
is fast continuously-operating comparator or a 'time-
discrete' comparator.

15

11. Apparatus according to any of preceding Claims 7
to 10 further characterised in that the communication
system encompasses a plurality of output stages of the
twisted pair communication link (400) arranged in
20 parallel to produce one of a CAN-H output and/or one CAN-
L output.

12. Apparatus according to Claim 11 further
characterised in that the plurality of stages are turned
25 on in sequence.

13. A method of reducing common-mode error in a
communication system comprising a twisted pair
communication link comprising the steps of:

30 providing at least two independent input signals
(402, 406) on the twisted pair communication link,
wherein the method is characterised by the steps of:

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combining the at least two independent input signals (402, 406) on the twisted pair communication link;

comparing the summed signal to a reference value (412);

5 inputting the output of the comparator (418) to at least two driver stages (422, 424);

combining the outputs from the at least two driver stages (422, 424); and

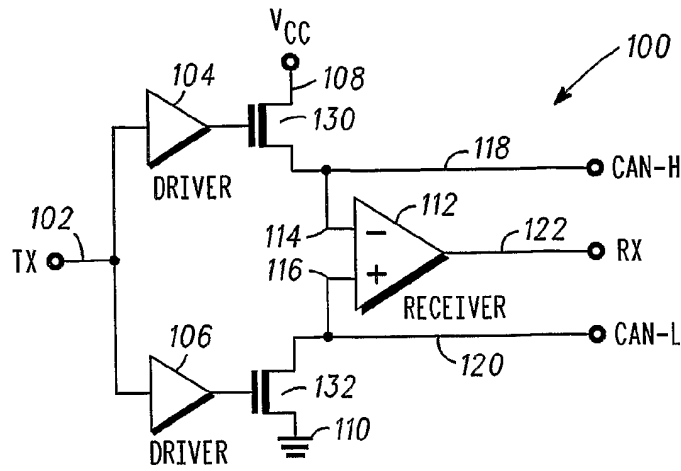
10 feeding back the summed output from the at least two driver stages (422, 424) to one or more of the independent input signals (402, 406).

STATEMENT UNDER ARTICLE 19 (1)

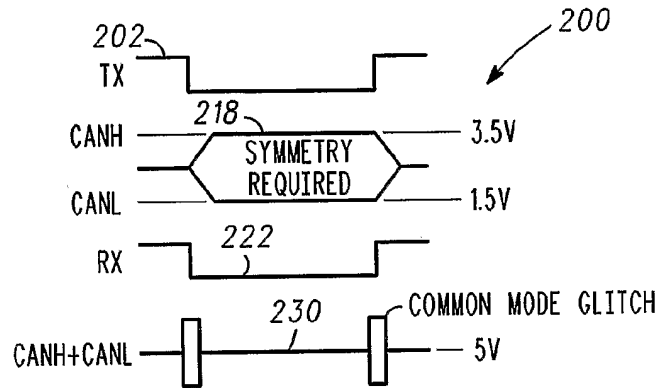
Re: Patent Application PCT/EP2005/008262 in the name of Freescale Semiconductor, Inc.

Amendments and support therefor:

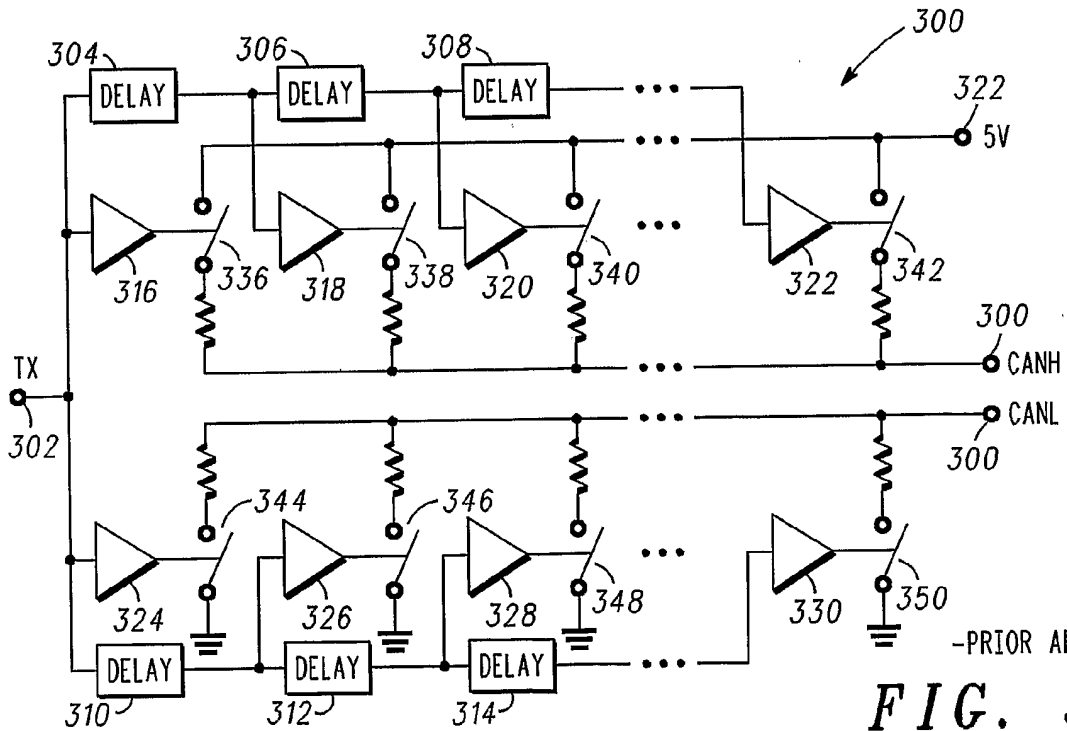
- (i) Claims 1, 7 and 13 have been amended to include reference numerals required by the examiner in order to bring consistency between the claims. Support for the inclusion of the reference numerals can be found in the independent claims as filed;
- (ii) Claim 7 has also been amended to recite that the outputs from the at least two driver stages are summed. Support for this feature that is the subject of this amendment can be found in Claims 1 and 13; and
- (iii) Dependent Claims 2 to 6, and 8 to 12 remain unchanged.



-PRIOR ART-
FIG. 1



-PRIOR ART-
FIG. 2



-PRIOR ART-
FIG. 3

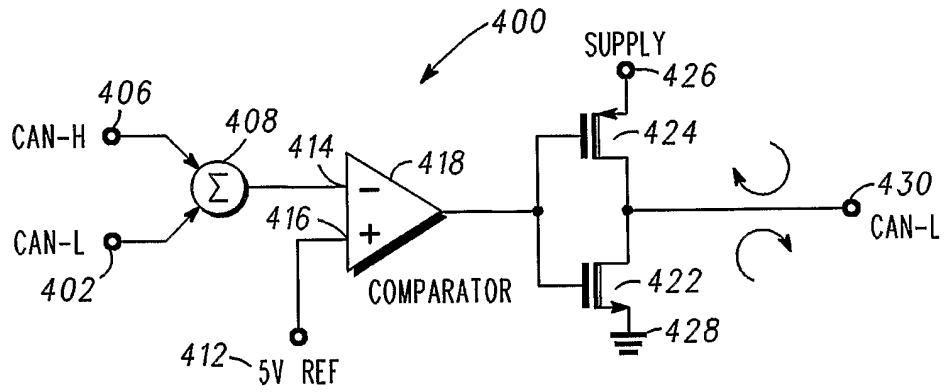


FIG. 4

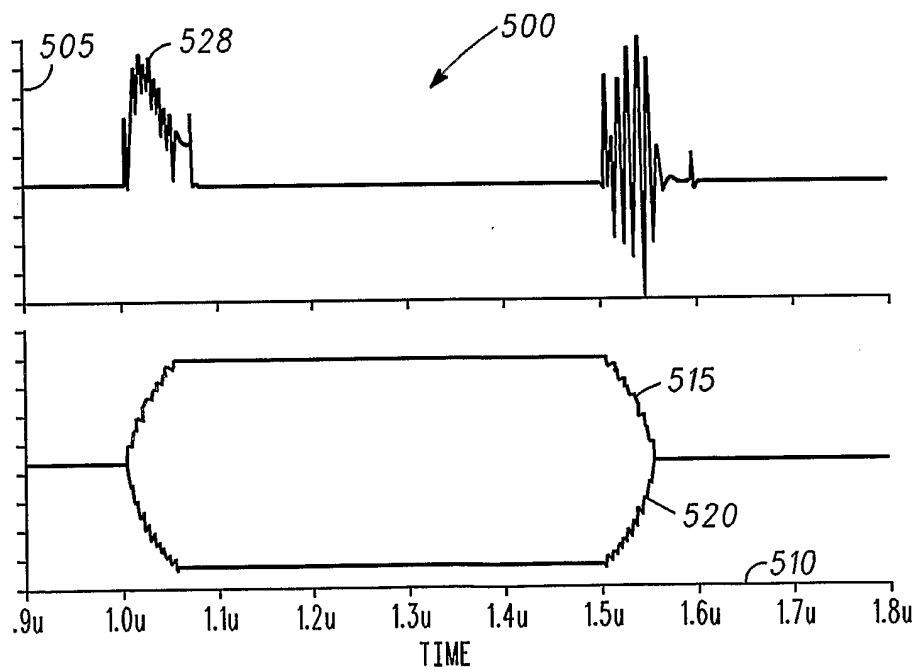


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
EP/EP2005/008262

| | | |
|---|---|---|
| A. CLASSIFICATION OF SUBJECT MATTER H04L25/02 | | |
| According to International Patent Classification (IPC) or to both national classification and IPC | | |
| B. FIELDS SEARCHED | | |
| Minimum documentation searched (classification system followed by classification symbols) H04L G06F | | |
| Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched | | |
| Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB | | |
| C. DOCUMENTS CONSIDERED TO BE RELEVANT | | |
| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| A | US 6 324 044 B1 (TEGGATZ ROSS E ET AL) 27 November 2001 (2001-11-27) column 1, line 32 - line 60 column 2, line 31 - line 57; figure 1 column 3, line 15 - line 38; figure 3 ----- | 1-13 |
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