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(54) **PIXEL DRIVING CIRCUIT, METHOD FOR DRIVING THE PIXEL DRIVING CIRCUIT, SILICON-BASED DISPLAY PANEL AND DISPLAY DEVICE**

(71) Applicant: **SEEYA OPTRONICS CO., LTD.**, Shanghai (CN)

(72) Inventors: **Ping-lin LIU**, Shanghai (CN); **Tong WU**, Shanghai (CN)

(73) Assignee: **SEEYA OPTRONICS CO., LTD.**, Shanghai (CN)

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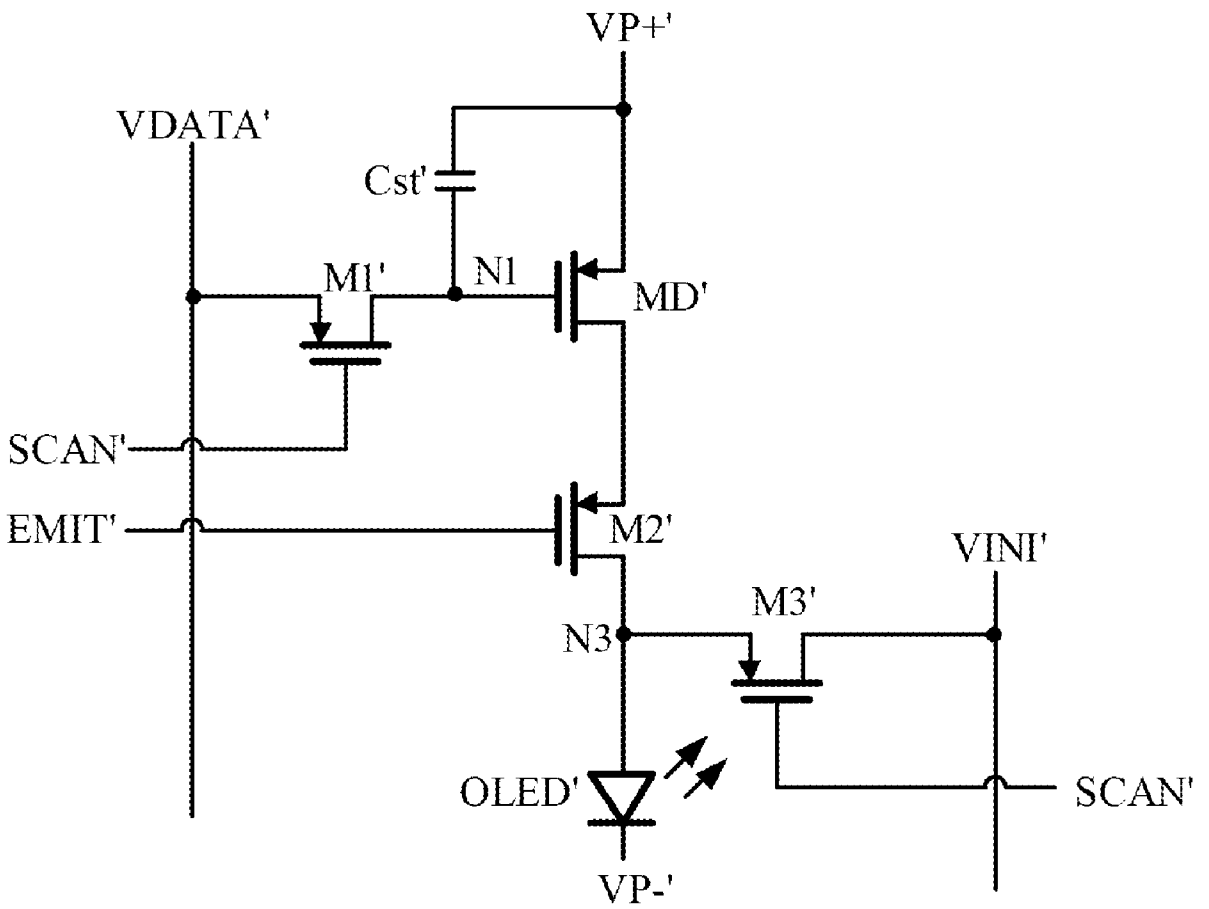
(57) **ABSTRACT**

Provided are a pixel driving circuit, a method for driving the pixel driving circuit, a silicon-based display panel and a display device. The pixel driving circuit is used for driving a light-emitting element to emit light. At an initial stage, a reset circuit provides a reset signal to a third node; a light emission control transistor is in a first on state to transmit the reset signal to a second node; a threshold compensation circuit transmits the reset signal to a first node; and a data write circuit transmits a non-enable level Vofs of a data signal to a second terminal of a first capacitor. At a threshold compensation stage, the threshold compensation circuit provides a threshold voltage of a drive transistor to the first node for compensation.



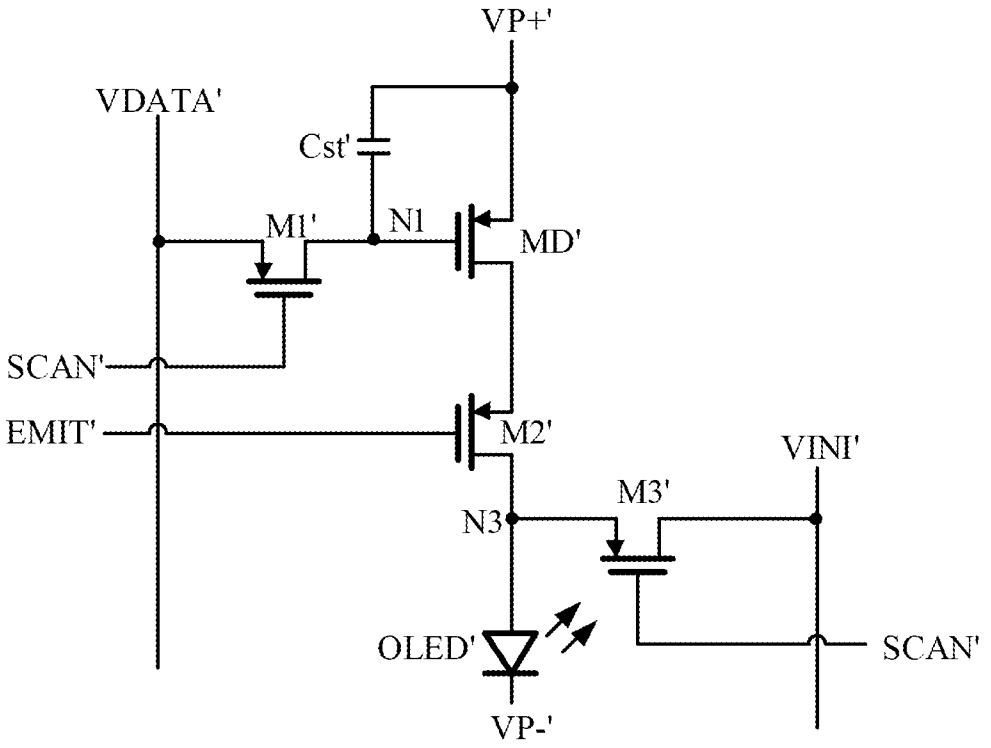

VP+'
VDATA'
Cst'
M1'
N1
MD'
SCAN'
EMIT'
M2'
VINI'
M3'
N3
OLED'
SCAN'
VP-'

FIG. 1

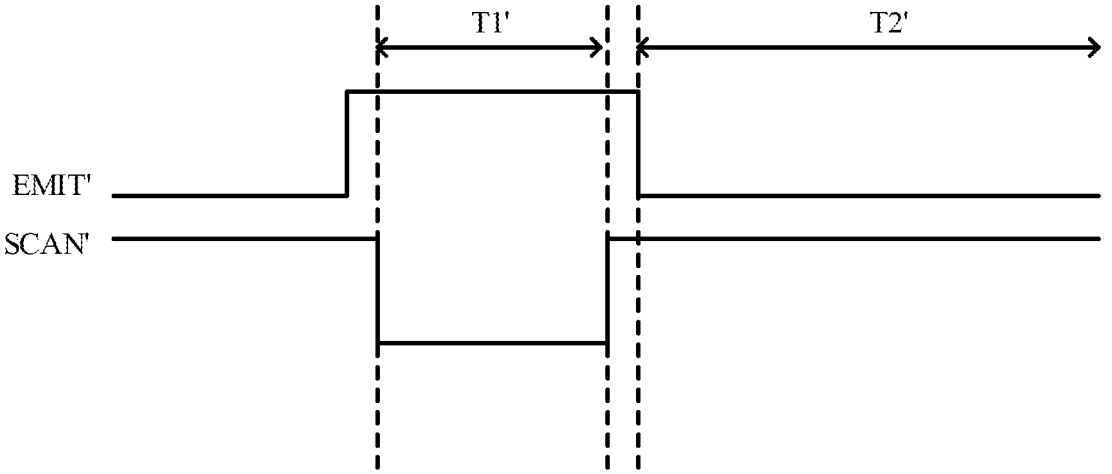

T1'
T2'
EMIT'
SCAN'

FIG. 2

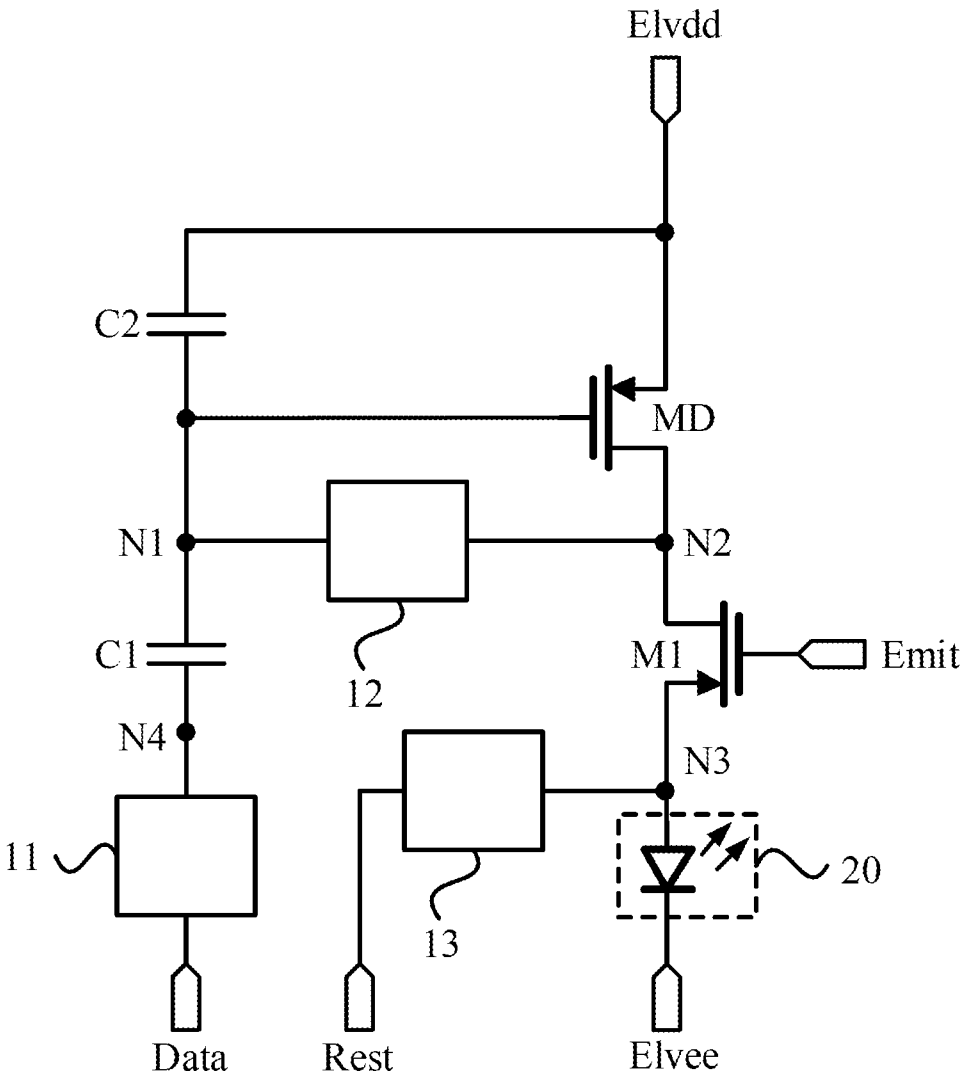

Elvdd
C2
MD
N1
N2
C1
12
M1
Emit
N4
N3
11
20
13
Data
Rest
Elvee

FIG. 3

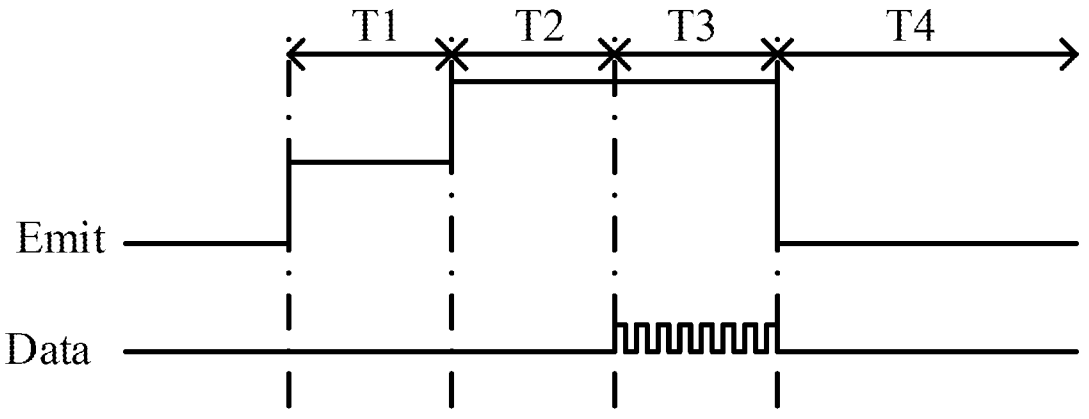

T1
T2
T3
T4
Emit
Data

FIG. 4

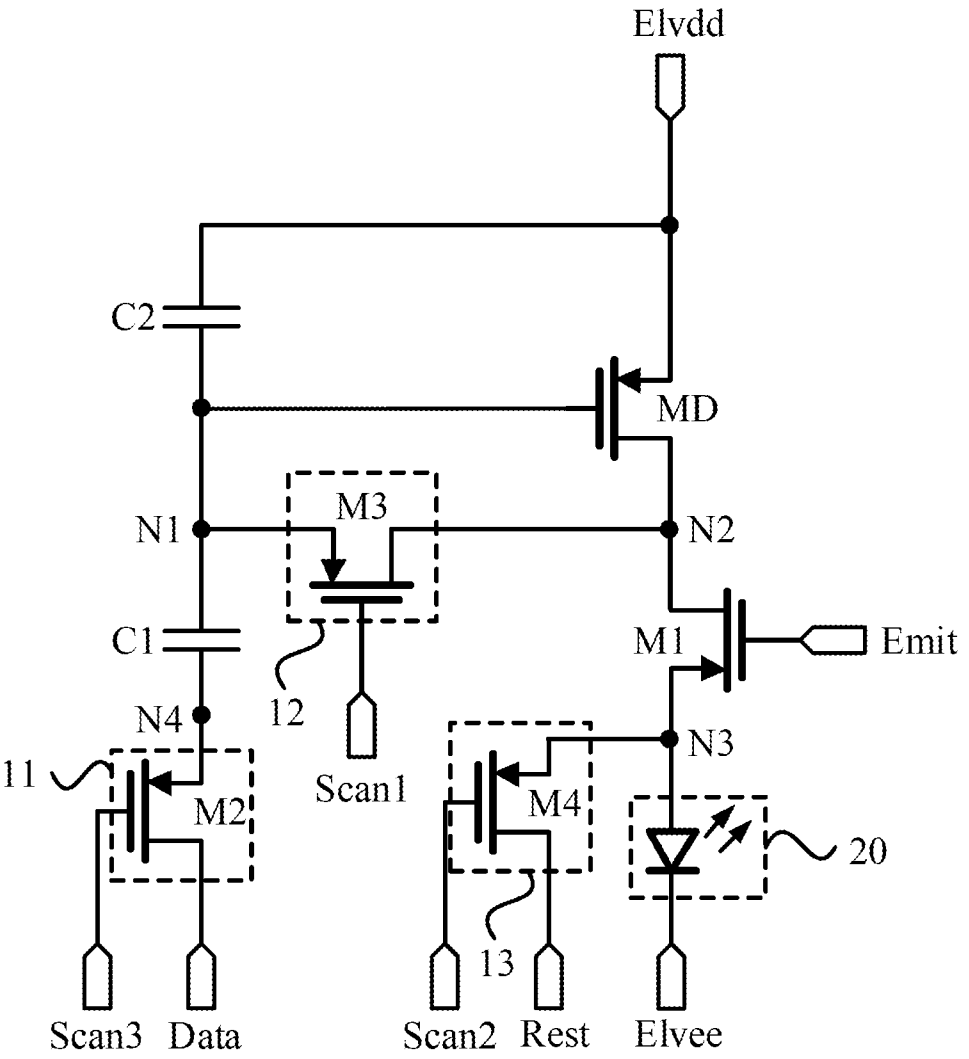

Elvdd
C2
MD
N1
M3
N2
C1
M1
Emit
12
N4
N3
11
Scan1
M2
M4
20
13
Scan3
Data
Scan2
Rest
Elvee

FIG. 5

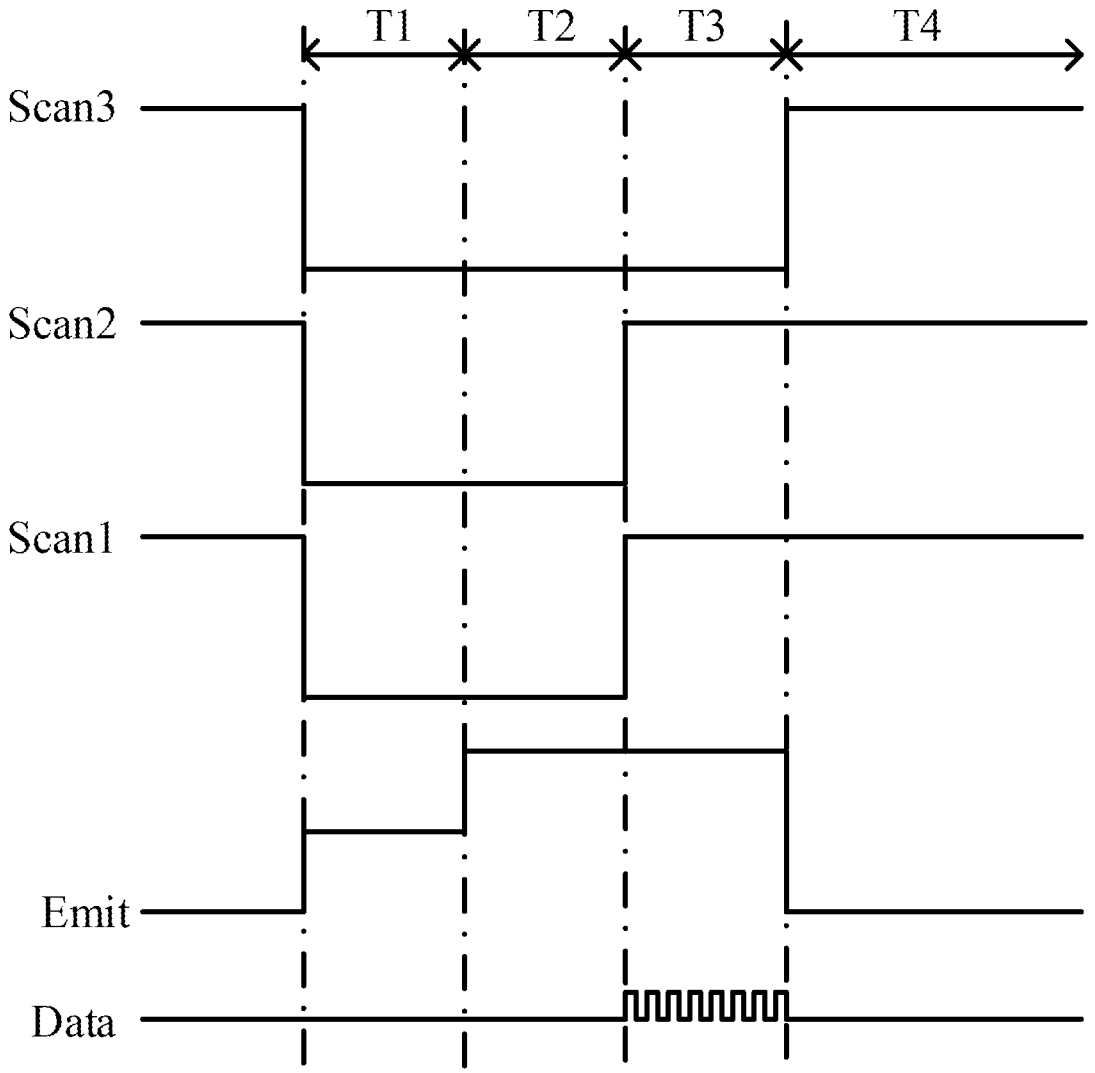


FIG. 6

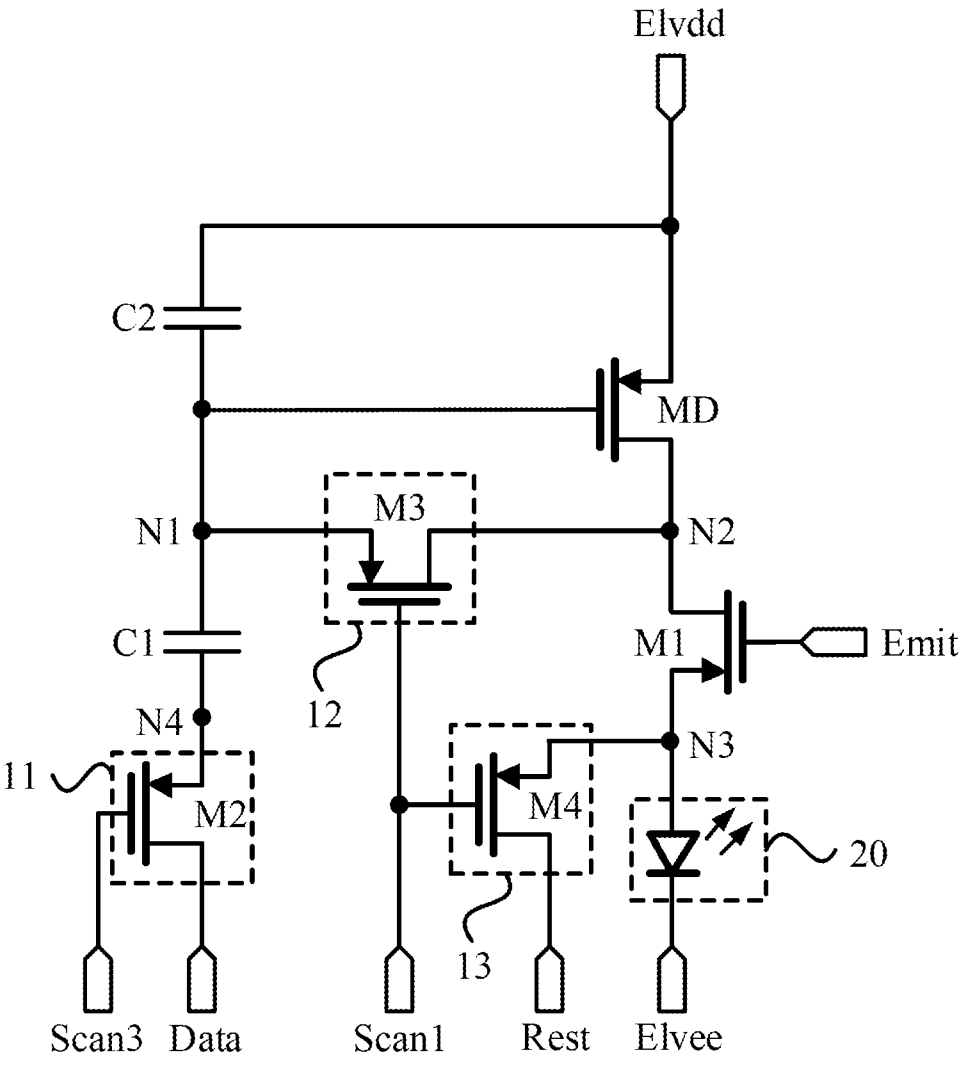

Elvdd
C2
MD
M3
N1
N2
C1
M1
Emit
12
N4
N3
11
M2
M4
20
13
Scan3
Data
Scan1
Rest
Elvee

FIG. 7

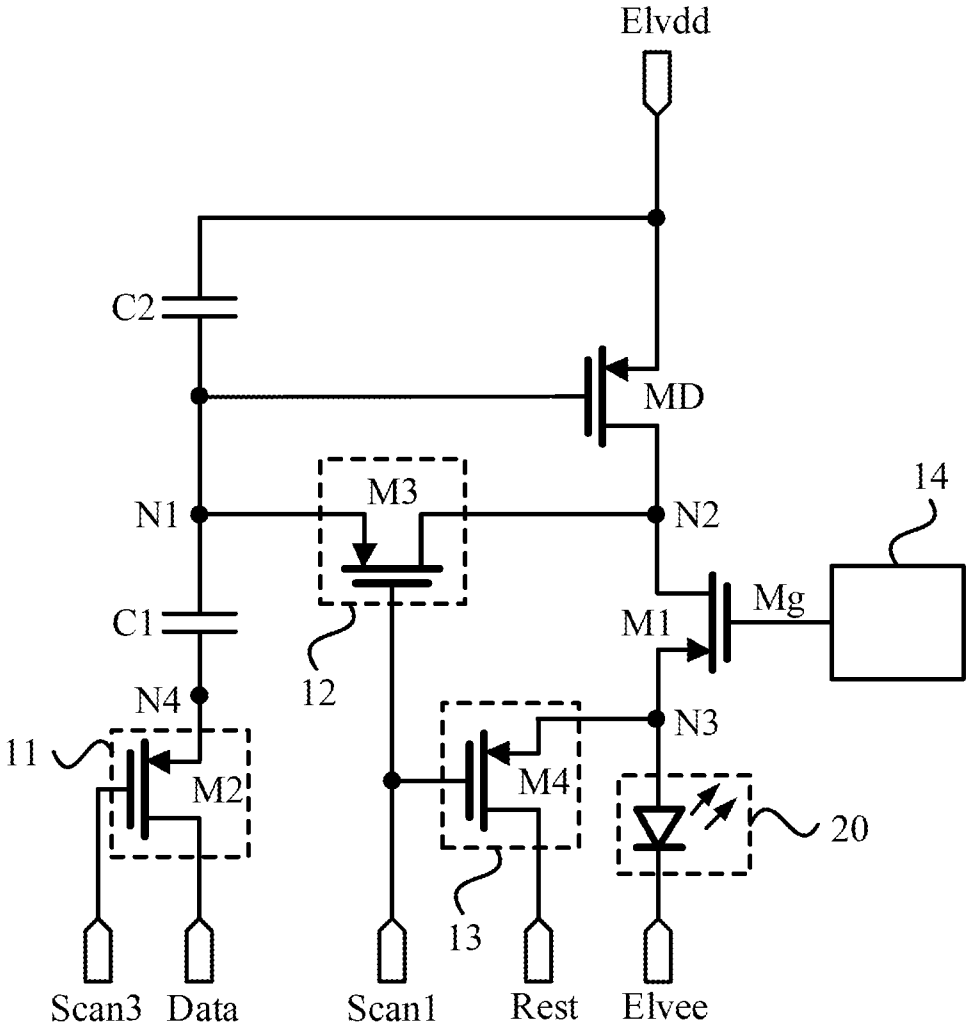

Elvdd
C2
MD
N1
M3
N2
14
C1
M1
Mg
12
N4
N3
11
M2
M4
20
13
Scan3
Data
Scan1
Rest
Elvee

FIG. 8

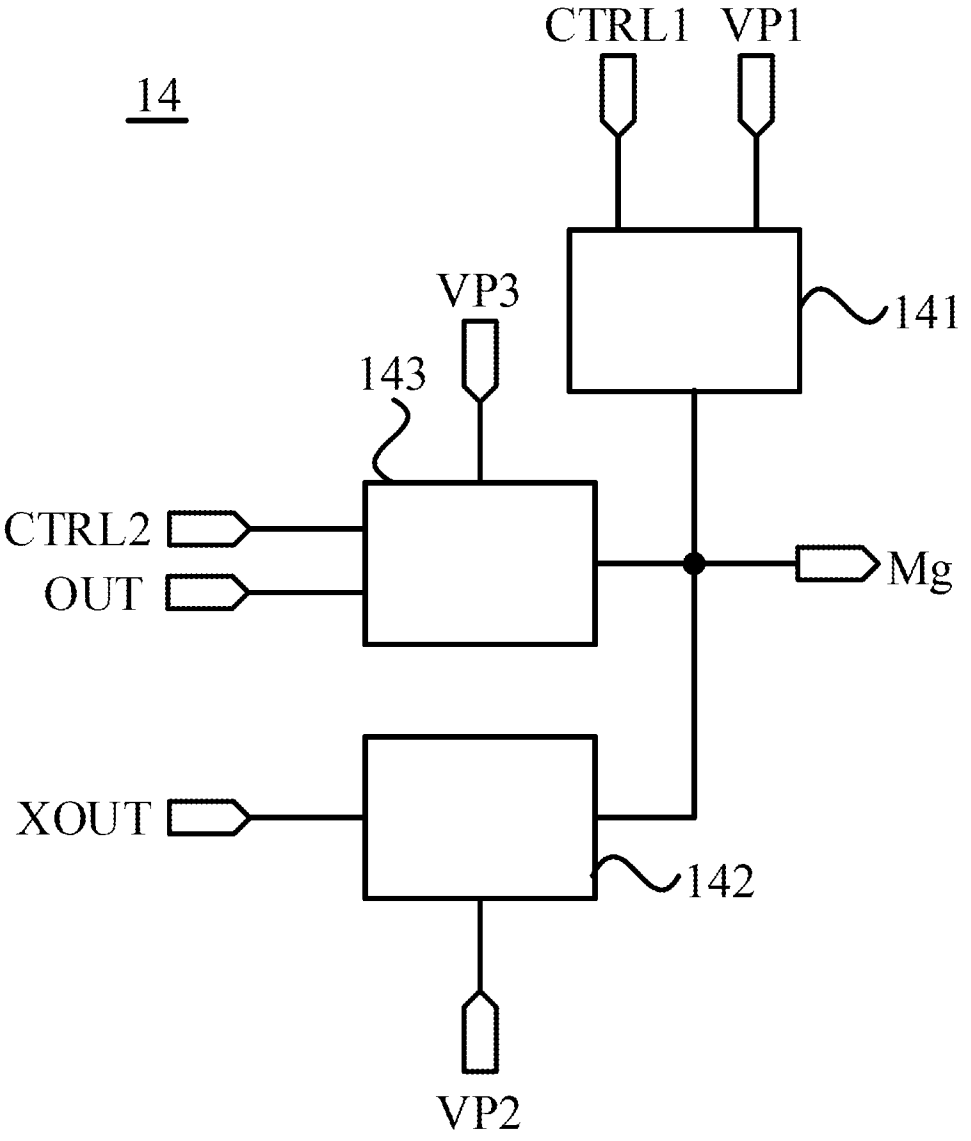


FIG. 9

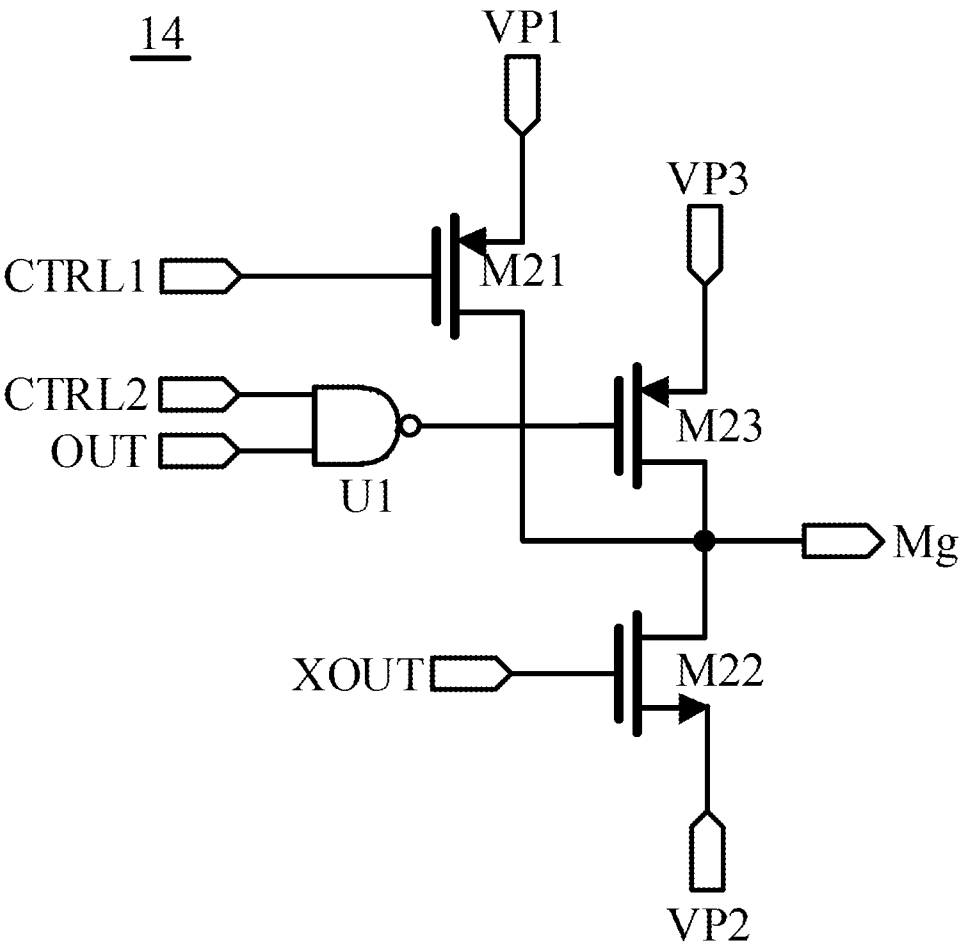


FIG. 10

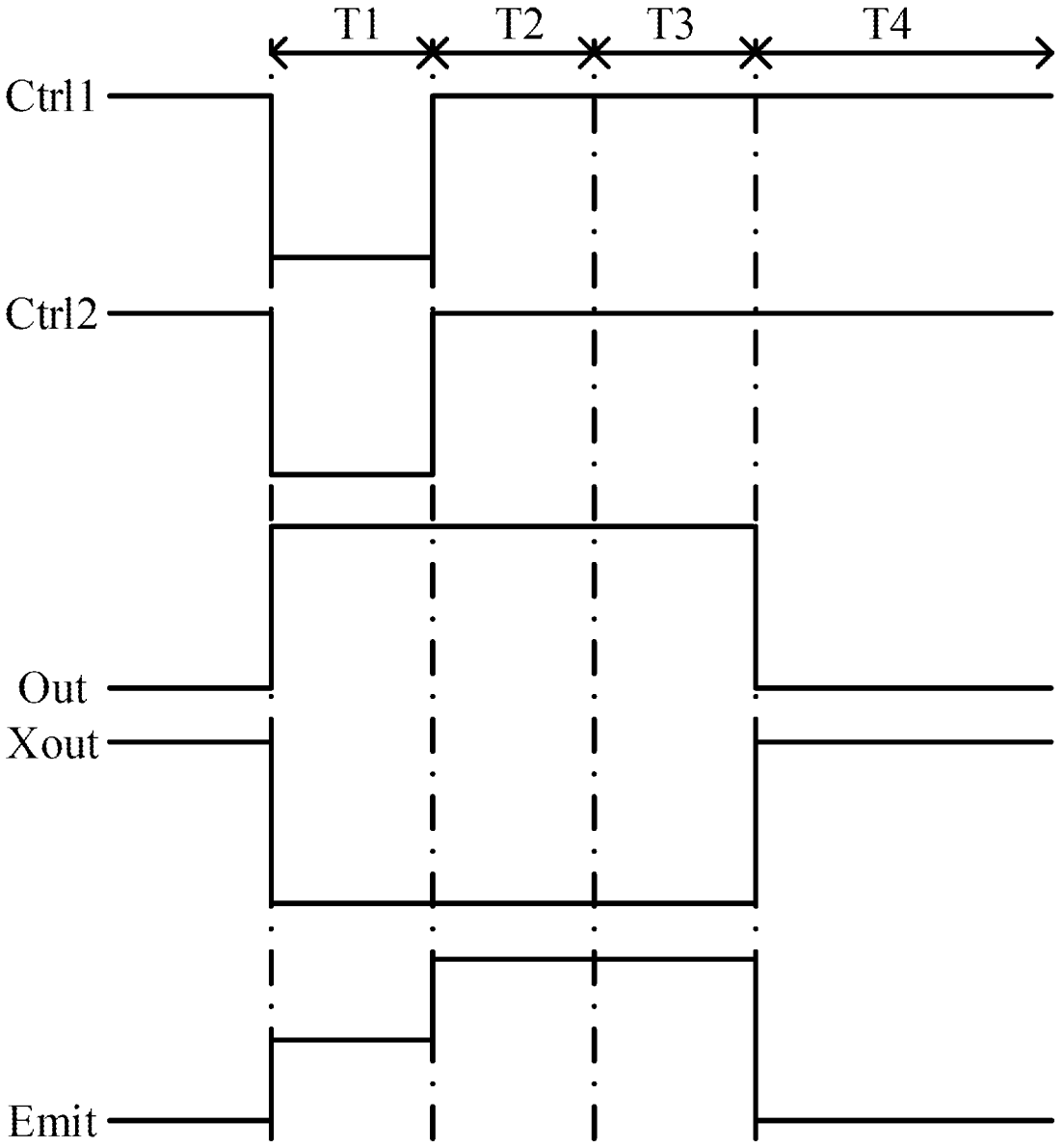


FIG. 11

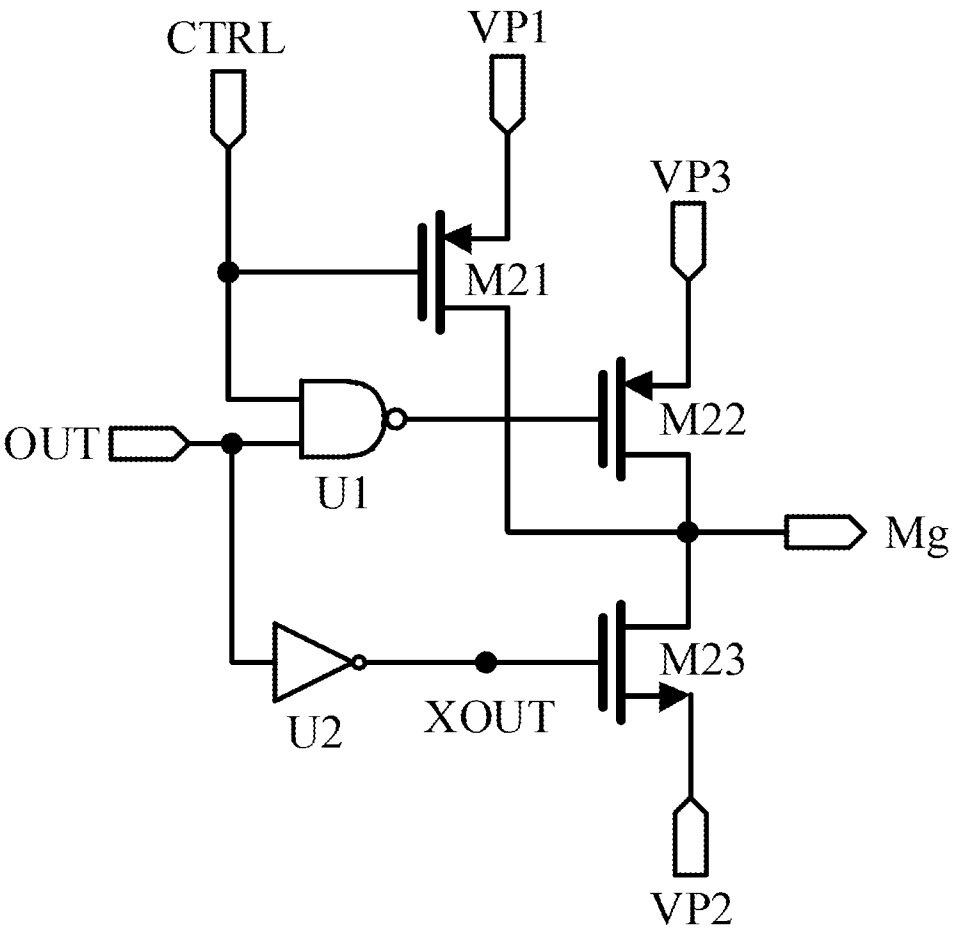


FIG. 12

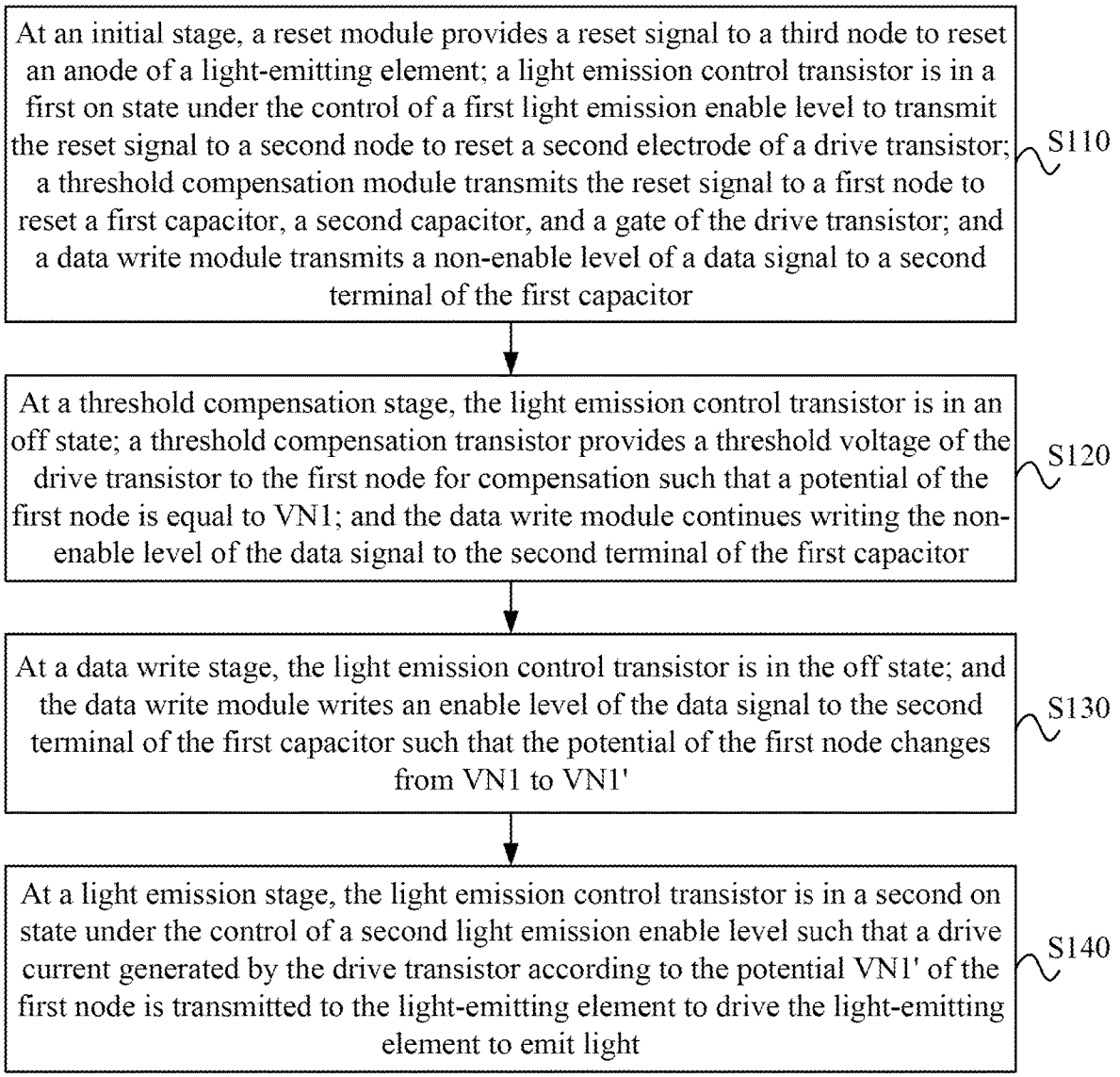

At an initial stage, a reset module provides a reset signal to a third node to reset an anode of a light-emitting element; a light emission control transistor is in a first on state under the control of a first light emission enable level to transmit the reset signal to a second node to reset a second electrode of a drive transistor; a threshold compensation module transmits the reset signal to a first node to reset a first capacitor, a second capacitor, and a gate of the drive transistor; and a data write module transmits a non-enable level of a data signal to a second terminal of the first capacitor
S110
At a threshold compensation stage, the light emission control transistor is in an off state; a threshold compensation transistor provides a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN1; and the data write module continues writing the non-enable level of the data signal to the second terminal of the first capacitor
S120
At a data write stage, the light emission control transistor is in the off state; and the data write module writes an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN1 to VN1'
S130
At a light emission stage, the light emission control transistor is in a second on state under the control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN1' of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light
S140

FIG. 13

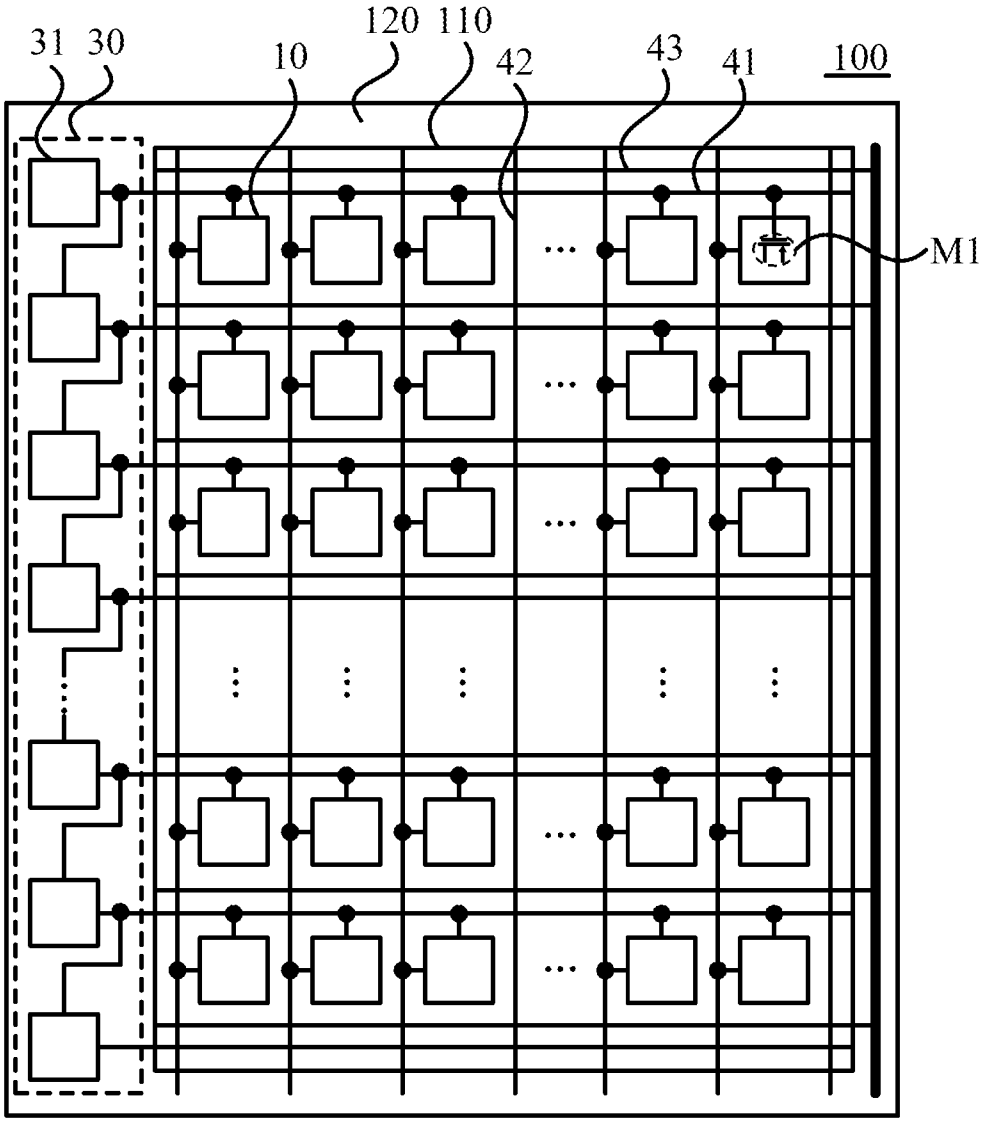


FIG. 14

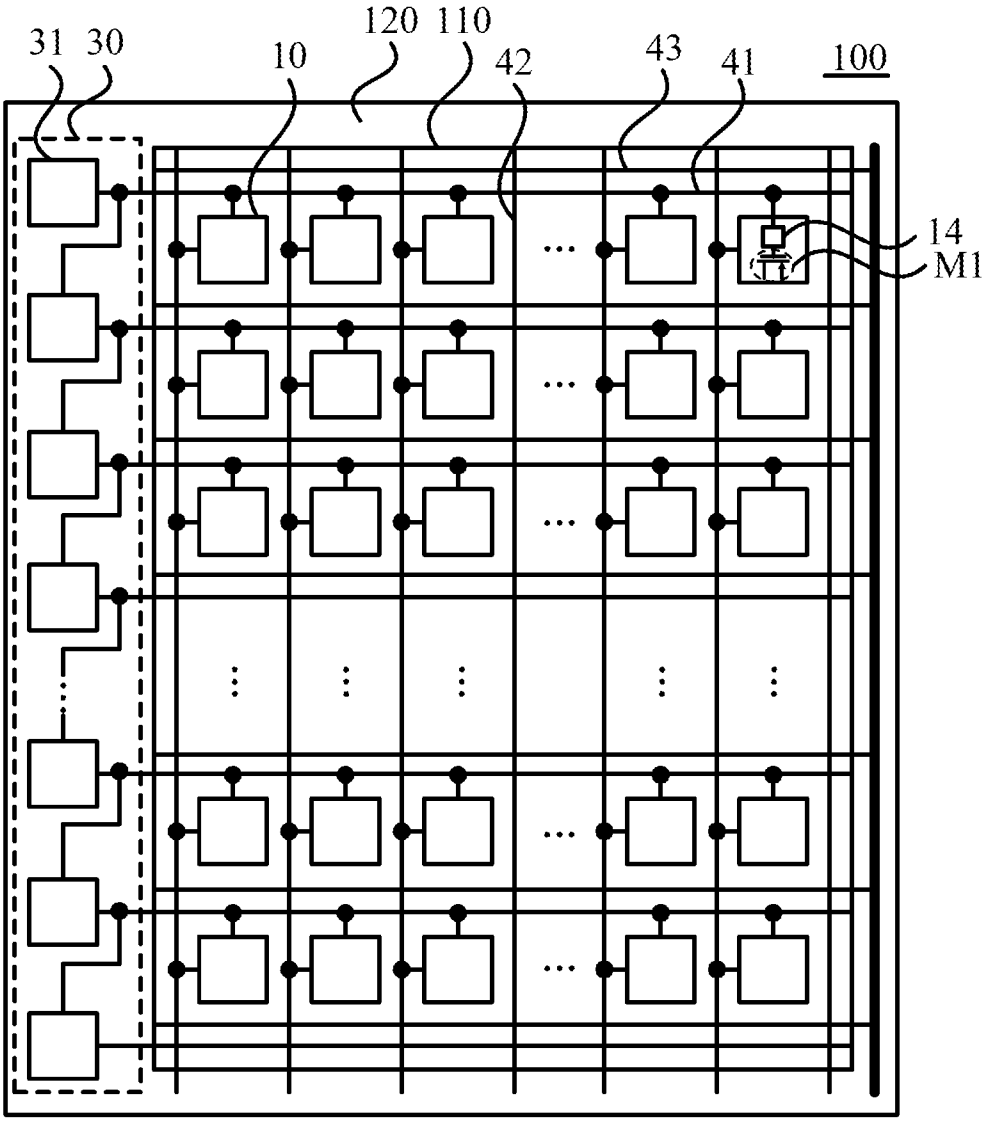


FIG. 15

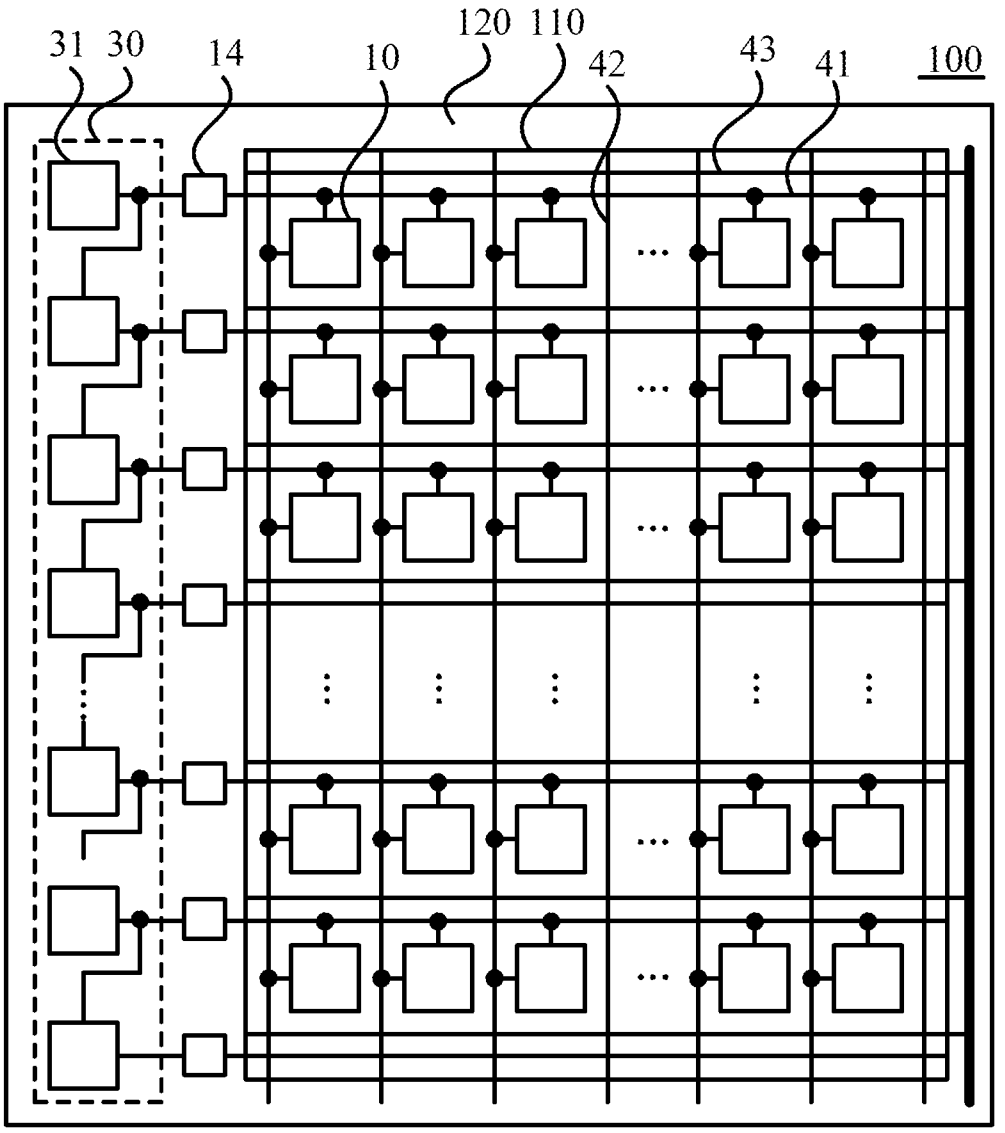


FIG. 16

PIXEL DRIVING CIRCUIT, METHOD FOR DRIVING THE PIXEL DRIVING CIRCUIT, SILICON-BASED DISPLAY PANEL AND DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to Chinese Patent Application No. 202111014624.5 filed Aug. 31, 2021, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of silicon-based display technology and, in particular, to a pixel driving circuit, a method for driving the pixel driving circuit, a silicon-based display panel and a display device.

BACKGROUND

[0003] A light-emitting element in a silicon-based display panel is typically an organic light-emitting diode (OLED) element which has the advantages of self-luminescence, a low drive voltage, high luminescence efficiency, a short response time and the like so that the silicon-based display panel becomes the most promising display panel in current wearable devices such as wristwatches, bracelets and virtual reality (VR) glasses.

[0004] Since the OLED element is a current-driven element, a corresponding pixel driving circuit needs to be configured to provide a drive current for the OLED element so that the OLED element can emit light. The pixel driving circuit in the silicon-based display panel typically includes a drive transistor, a switch transistor and a storage capacitor. Where the drive transistor can generate the drive current for driving the OLED element according to the voltage of its gate. However, for reasons such as the process of techniques and the aging of devices, a threshold voltage drift occurs in the drive transistor in the pixel driving circuit, resulting in display non-uniformity.

SUMMARY

[0005] In view of the preceding problems, embodiments of the present disclosure provide a pixel driving circuit, a method for driving the pixel driving circuit, a silicon-based display panel and a display device, so as to eliminate an effect of a threshold drift on display brightness, solve the problem of an afterimage, and improve a display effect.

[0006] In a first aspect, the embodiments of the present disclosure provide a pixel driving circuit for driving a light-emitting element to emit light. The pixel driving circuit includes a drive transistor, a light emission control transistor, a first capacitor, a second capacitor, a reset circuit, a data write circuit, and a threshold compensation circuit.

[0007] A gate of the drive transistor, a first terminal of the first capacitor, a second terminal of the second capacitor, and the threshold compensation circuit are electrically connected to a first node. A first terminal of the second capacitor is configured to receive a fixed voltage signal. A first electrode of the light emission control transistor, a second electrode of the drive transistor, and the threshold compensation circuit are electrically connected to a second node. A second electrode of the light emission control transistor, the reset circuit, and an anode of the light-emitting element are electrically connected to a third node.

[0008] At an initial stage, the reset circuit is configured to provide a reset signal to the third node to reset the anode of the light-emitting element; the light emission control transistor is configured to be in a first on state under the control of a first light emission enable level to transmit the reset signal to the second node to reset the second electrode of the drive transistor; the threshold compensation circuit is configured to transmit the reset signal to the first node to reset the first capacitor, the second capacitor, and the gate of the drive transistor; and the data write circuit is configured to transmit a non-enable level Vofs of a data signal to a second terminal of the first capacitor.

[0009] At a threshold compensation stage, the threshold compensation circuit is configured to provide a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit is configured to write the non-enable level Vofs of the data signal to the second terminal of the first capacitor.

[0010] At a data write stage, the data write circuit is configured to write an enable level Vdata of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1'**, where VN**1'**=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), where Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor.

[0011] At a light emission stage, the light emission control transistor is configured to be in a second on state under the control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1'** of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light.

[0012] A smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

[0013] In a second aspect, the embodiments of the present disclosure further provide a method for driving a pixel driving circuit. The method is used for driving the preceding pixel driving circuit. The method for driving a pixel driving circuit includes steps described below.

[0014] At an initial stage, a reset circuit provides a reset signal to a third node to reset an anode of a light-emitting element; a light emission control transistor is in a first on state under the control of a first light emission enable level to transmit the reset signal to a second node to reset a second electrode of a drive transistor; a threshold compensation circuit transmits the reset signal to a first node to reset a first capacitor, a second capacitor, and a gate of the drive transistor; and a data write circuit transmits a non-enable level Vofs of a data signal to a second terminal of the first capacitor.

[0015] At a threshold compensation stage, the light emission control transistor is in an off state; the threshold compensation circuit provides a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit continues writing the non-enable level Vofs of the data signal to the second terminal of the first capacitor.

[0016] At a data write stage, the light emission control transistor is in the off state; and the data write circuit writes an enable level Vdata of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1**'. Where VN**1**'=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), where Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor.

[0017] At a light emission stage, the light emission control transistor is in a second on state under the control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1**' of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light.

[0018] A smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

[0019] In a third aspect, the embodiments of the present disclosure further provide a silicon-based display panel. The silicon-based display panel includes a plurality of light-emitting elements and a plurality of pixel driving circuits described above. The plurality of pixel driving circuits are arranged in an array and configured to drive the plurality of light-emitting elements to emit light.

[0020] In a fourth aspect, the embodiments of the present disclosure further provide a display device including the preceding silicon-based display panel.

[0021] According to the pixel driving circuit, the method for driving the pixel driving circuit, the silicon-based display panel and the display device provided by the embodiments of the present disclosure, at the initial stage, the light emission control transistor is in the first on state under the control of the first light emission enable level so that a relatively small current flows through the light emission control transistor on the premise that the anode of the light-emitting element, the second electrode of the drive transistor, and the gate of the drive transistor can be reset in sequence. Therefore, the light emission control transistor has relatively small power consumption, facilitating the low power consumption of the pixel driving circuit. When the pixel driving circuit is applied to the display panel, the low power consumption of the silicon-based display panel can be facilitated and the application requirement of the silicon-based display panel for low power consumption can be satisfied. Moreover, at the light emission stage, the light emission control transistor is in the second on state under the control of the second light emission enable level so that a relatively large current can flow through the light emission control transistor, and the anode of the light-emitting element can be quickly charged by the drive current provided by the drive transistor, so as to prevent the silicon-based display panel including the pixel driving circuit from a color cast. Additionally, at the threshold compensation stage, the threshold voltage of the drive transistor is provided to the first node for compensation so that the drive current provided by the drive transistor at the light emission stage is independent of the threshold voltage of the drive transistor, so as to prevent a threshold drift of the drive transistor from affecting the display uniformity of the display panel and solve the problem of display non-uniformity of the display panel. Additionally, at the data write stage, the voltage of the first node N**1** is divided by the first capacitor and the second capacitor so that even if the enable level of the data signal written by the data write circuit to the second terminal of the first capacitor is a relatively large voltage, a voltage coupled to the second terminal of the first capacitor is proportional to a ratio of the capacitance value of the first capacitor to a sum of the capacitance values of the two capacitors (the first capacitor and the second capacitor). Therefore, by setting the capacitance values of the first capacitor and the second capacitor, the enable level of the data signal changes within a relatively large range and the potential of the first node changes within a relatively small range so that the brightness of the light-emitting element has different levels and can be adjusted with higher accuracy, improving the color richness of the image displayed by the display panel and the display quality of the display panel.

BRIEF DESCRIPTION OF DRAWINGS

[0022] FIG. **1** is a structure diagram of a pixel driving circuit in the related art;

[0023] FIG. **2** is a drive timing diagram of a pixel circuit corresponding to FIG. **1**;

[0024] FIG. **3** is a structure diagram of a pixel driving circuit according to an embodiment of the present disclosure;

[0025] FIG. **4** is a drive timing diagram of the pixel driving circuit in FIG. **3**;

[0026] FIG. **5** is a diagram showing specific circuit structures of a pixel driving circuit according to an embodiment of the present disclosure;

[0027] FIG. **6** is a drive timing diagram of the pixel driving circuit in FIG. **5**;

[0028] FIG. **7** is a diagram showing specific circuit structures of another pixel driving circuit according to an embodiment of the present disclosure;

[0029] FIG. **8** is a structure diagram of another pixel driving circuit according to an embodiment of the present disclosure;

[0030] FIG. **9** is a structure diagram of a signal conversion circuit according to an embodiment of the present disclosure;

[0031] FIG. **10** is a diagram showing specific circuit structures of a signal conversion circuit according to an embodiment of the present disclosure;

[0032] FIG. **11** is a drive timing diagram of the signal conversion circuit in FIG. **10**;

[0033] FIG. **12** is a diagram showing specific circuit structures of another signal conversion circuit according to an embodiment of the present disclosure;

[0034] FIG. **13** is a flowchart of a method for driving a pixel driving circuit according to an embodiment of the present disclosure;

[0035] FIG. **14** is a structure diagram of a silicon-based display panel according to an embodiment of the present disclosure;

[0036] FIG. **15** is a structure diagram of another silicon-based display panel according to an embodiment of the present disclosure; and

[0037] FIG. **16** is a structure diagram of another silicon-based display panel according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0038] The present disclosure is further described hereinafter in detail in conjunction with drawings and embodiments. It is to be understood that the embodiments described herein are merely intended to explain the present disclosure and not to limit the present disclosure. Additionally, it is to be noted that for ease of description, only part, not all, of the structures related to the present disclosure are illustrated in the drawings.

[0039] FIG. **1** is a structure diagram of a pixel driving circuit in the related art. FIG. **2** is a drive timing diagram of a pixel circuit corresponding to FIG. **1**. As shown in FIGS. **1** and **2**, the pixel driving circuit includes a drive transistor MD', a data write transistor M**1**', a light emission control transistor M**2**', a reset transistor M**3**', and a storage capacitor Cst', where the data write transistor M**1**' and the reset transistor M**3**' are turned on or off under the control of a scan signal SCAN', and the light emission control transistor M**2**' is turned on or off under the control of a light emission control signal EMIT'. At an initial stage T**1**', the scan signal SCAN' controls both the data write transistor M**1**' and the reset transistor M**3**' to be in an on state such that a data signal VDATA' is written to a gate of the drive transistor MD' through the data write transistor M**1**' that is on and stored in the storage capacitor Cst'; and at the same time, a reset signal VINI' is transmitted to an anode of a light-emitting element OLED' through the reset transistor M**3**' that is on to reset the anode of the light-emitting element OLED'. At a light emission stage T**2**', a light emission control signal EMIT' controls the light emission control transistor M**2**' to be in the on state such that a current path is formed between a positive power supply VP+' and a negative power supply VP−', and a drive current provided by the drive transistor MD' according to a potential of the gate of the drive transistor MD' is transmitted to the light-emitting element OLED' to drive the light-emitting element OLED' to emit light.

[0040] The drive transistor MD' works within a subthreshold region so that the drive current I_{MD}' provided by the drive transistor MD' at the light emission stage is expressed as follows:

$$I_{MD'} = \frac{Z}{L}\mu_p\left(\frac{kT}{q}\right)^2 C_D(\varphi_s)\exp\left[\frac{q}{kT}\left(\frac{V_{GS}-V_{th}}{n}\right)\right]*\left[1-\exp\left(-\frac{qV_{DS}}{kT}\right)\right];$$

[0041] where k denotes a Boltzmann constant, T denotes an absolute temperature, q denotes an amount of charge, L denotes a channel length of a metal-oxide-semiconductor (MOS) transistor, μ_p denotes a carrier mobility of a p-type MOS (PMOS) transistor, $C_D(\varphi_s)$ denotes a barrier capacitance of a channel depletion region, V_{GS} denotes a voltage difference between the gate and a source of the drive transistor MD', that is, VDATA'−VP+', V_{DS} denotes a voltage difference between a drain and the source of the drive transistor MD', and V_{th} denotes a threshold voltage of the drive transistor MD'. The drive current Imp' is sensitive to and exponentially related to the threshold voltage V_{th} of the drive transistor MD' so that when the threshold voltage V_{th} of the drive transistor MD' in the pixel driving circuit changes, the drive current Imp' exponentially changes with a variation ΔV_{th} of the threshold voltage V_{th}, and finally the brightness of the light-emitting element is uncontrollable, resulting in display non-uniformity and affecting a display effect. Moreover, since the drive transistor MD' is typically the PMOS transistor which has a relatively large mobility, the drive current is typically at a pA to nA level so that the data signal VDATA' has a very small voltage range and it is difficult to switch within a range of 0 to 255 grayscales, affecting the display quality of a displayed image.

[0042] To solve the preceding technical problems, embodiments of the present disclosure provide a pixel driving circuit for driving a light-emitting element to emit light. The pixel driving circuit includes a drive transistor, a light emission control transistor, a first capacitor, a second capacitor, a reset circuit, a data write circuit, and a threshold compensation circuit. A gate of the drive transistor, a first terminal of the first capacitor, a second terminal of the second capacitor, and the threshold compensation circuit are electrically connected to a first node. A first terminal of the second capacitor is configured to receive a fixed voltage signal. A first electrode of the light emission control transistor, a second electrode of the drive transistor, and the threshold compensation circuit are electrically connected to a second node. A second electrode of the light emission control transistor, the reset circuit, and an anode of the light-emitting element are electrically connected to a third node. At an initial stage, the reset circuit is configured to provide a reset signal to the third node to reset the anode of the light-emitting element; the light emission control transistor is configured to be in a first on state under the control of a first light emission enable level to transmit the reset signal to the second node to reset the second electrode of the drive transistor; the threshold compensation circuit is configured to transmit the reset signal to the first node to reset the first capacitor, the second capacitor, and the gate of the drive transistor; and the data write circuit is configured to transmit a non-enable level of a data signal to a second terminal of the first capacitor. At a threshold compensation stage, the threshold compensation circuit is configured to provide a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit is configured to continue writing the non-enable level of the data signal to the second terminal of the first capacitor. At a data write stage, the data write circuit is configured to write an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1**'. Where VN**1**'=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor. At a light emission stage, the light emission control transistor is configured to be in a second on state under the control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1**' of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light. A smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

[0043] According to the preceding technical solutions, on one hand, at the initial stage, the light emission control transistor is in the first on state under the control of the first light emission enable level so that a relatively small current flows through the light emission control transistor on the premise that the anode of the light-emitting element, the

second electrode of the drive transistor, and the gate of the drive transistor can be reset in sequence. Therefore, the light emission control transistor has relatively small power consumption, facilitating the low power consumption of the pixel driving circuit. When the pixel driving circuit is applied to a display panel, the low power consumption of a silicon-based display panel can be facilitated and the application requirement of the silicon-based display panel for low power consumption can be satisfied. On the other hand, at the light emission stage, the light emission control transistor is in the second on state under the control of the second light emission enable level so that a relatively large current can flow through the light emission control transistor, and the anode of the light-emitting element can be quickly charged by the drive current provided by the drive transistor, so as to prevent the silicon-based display panel including the pixel driving circuit from a color shift. Meanwhile, at the threshold compensation stage, the threshold voltage of the drive transistor is provided to the first node for compensation so that the drive current provided by the drive transistor at the light emission stage is independent of the threshold voltage of the drive transistor, so as to prevent a threshold drift of the drive transistor from affecting the display uniformity of the display panel and solve the problem of display non-uniformity of the display panel. Additionally, at the data write stage, the voltage of the first node N1 is divided by the first capacitor and the second capacitor so that even if the enable level of the data signal written by the data write circuit to the second terminal of the first capacitor is a relatively large voltage, a voltage coupled to the second terminal of the first capacitor is proportional to a ratio of the capacitance value of the first capacitor to a sum of the capacitance values of the two capacitors (the first capacitor and the second capacitor). Therefore, by setting the capacitance values of the first capacitor and the second capacitor, the enable level of the data signal changes within a relatively large range and the potential of the first node changes within a relatively small range so that the brightness of the light-emitting element has different levels and can be adjusted with higher accuracy, improving the color richness of the image displayed by the display panel and the display quality of the display panel.

[0044] The preceding is the core idea of the present disclosure. Based on the embodiments of the present disclosure, all other embodiments obtained by those of ordinary skill in the art without creative work are within the scope of the present disclosure. Hereinafter, the technical solutions in the embodiments of the present disclosure are described clearly and completely in conjunction with the drawings in the embodiments of the present disclosure.

[0045] FIG. **3** is a structure diagram of a pixel driving circuit according to an embodiment of the present disclosure. As shown in FIG. **3**, in the pixel driving circuit, a gate of a drive transistor MD, a first terminal of a first capacitor C**1**, a second terminal of a second capacitor C**2**, and a threshold compensation circuit **12** are electrically connected to a first node N**1**. A first terminal of the second capacitor C**2** receives a fixed voltage signal which may be a positive power supply Elvdd. A first electrode of a light emission control transistor M**1**, a second electrode of the drive transistor MD, and the threshold compensation circuit **12** are electrically connected to a second node N**2**. A second electrode of the light emission control transistor M**1**, a reset circuit **13**, and an anode of a light-emitting element **20** are electrically connected to a third node. A data write circuit **11** and a second terminal of the first capacitor C**1** may be electrically connected to a fourth node N**4**.

[0046] It is to be understood that in the pixel driving circuit, the drive transistor MD may be a PMOS or n-type MOS (NMOS) transistor. Considering mobility, the drive transistor MD is typically the PMOS transistor. Correspondingly, the light emission control transistor M**1** may also be a PMOS or NMOS transistor, which is not specifically limited in the embodiments of the present disclosure. When the light emission control transistor M**1** is the PMOS transistor, the light emission control transistor M**1** is turned on when a gate-source voltage difference of the light emission control transistor M**1** is lower than or equal to a threshold voltage of the light emission control transistor M**1**, that is, the light emission control transistor M**1** is turned on when a gate of the light emission control transistor M**1** receives a light emission control signal Emit at a relatively low level which is an enable level of the light emission control signal Emit. When the light emission control transistor M**1** is the NMOS transistor, the light emission control transistor M**1** is turned on when the gate-source voltage difference of the light emission control transistor M**1** is higher than or equal to the threshold voltage of the light emission control transistor M**1**, that is, the light emission control transistor M**1** is turned on when the gate of the light emission control transistor M**1** receives a light emission control signal Emit at a relatively high level which is the enable level of the light emission control signal Emit.

[0047] For ease of description, the technical solutions in the embodiments of the present disclosure are exemplarily described using an example in which the light emission control transistor M**1** is the PMOS transistor.

[0048] FIG. **4** is a drive timing diagram of the pixel driving circuit in FIG. **3**. As shown in FIGS. **3** and **4**, at an initial stage T**1**, the reset circuit **13** provides a reset signal Rest to the third node N**3** to reset the anode of the light-emitting element **20**. The light emission control transistor M**1** is in a first on state under the control of a first light emission enable level of the light emission control signal Emit to transmit the reset signal Rest from the third node N**3** to the second node N**2** to reset the second electrode of the drive transistor MD; the threshold compensation circuit **12** transmits the reset signal Rest from the second node N**2** to the first node N**1** to reset the first capacitor C**1**, the second capacitor C**2**, and the gate of the drive transistor MD; and the data write circuit **11** transmits a non-enable level Vofs of a data signal Data to the second terminal of the first capacitor C**1**. In this manner, at the initial stage T**1**, the light emission control transistor M**1** is in the first on state so that a relatively small current flows through the light emission control transistor M**1**. Therefore, on the premise that the second node N**2** and the first node N**1** can be reset, the light emission control transistor M**1** has relatively small power consumption, facilitating the low power consumption of the pixel driving circuit. When the pixel driving circuit is applied to a silicon-based display panel, the low power consumption of the silicon-based display panel is facilitated and the application requirement of the silicon-based display panel for low power consumption is satisfied. Moreover, when the initial stage T**1** ends, the gate and the second electrode of the drive transistor MD have been reset, and the drive transistor MD changes from a bias state in a previous drive cycle to an initial state, so as to prevent a hysteresis effect of the drive transistor MD from affecting the subsequent working state

of the drive transistor MD. Additionally, a voltage V across the first capacitor C1 is a voltage difference between the first node N1 and the fourth node N4. If a voltage drop caused by the reset circuit **13**, the light emission control transistor M1, the threshold compensation circuit **12**, and the data write circuit **11** is ignored, a voltage difference VC1 across the first capacitor C1 is equal to Rest−Vofs. That is, VC1=Rest−Vofs.

[0049] After the initial stage T1 ends, the pixel driving circuit enters a threshold compensation stage T2 at which a path is formed between the positive power supply Elvdd and the first node N1 so that a current signal passes through the drive transistor MD and the threshold compensation circuit **12** in sequence and charges the first node N1 until a potential VN1 of the first node N1 is Elvdd−Vth (that is, VN1=Elvdd−Vth), which is a critical point at which the drive transistor MD is turned off. Therefore, when the threshold compensation stage T2 ends, the potential of the first node N1 remains VN1. Vth denotes a threshold voltage of the drive transistor MD. In this manner, after the threshold compensation stage T2 ends, the potential of the first node N1 is related to the threshold voltage of the drive transistor MD so that the threshold compensation circuit **12** provides the threshold voltage of the drive transistor MD to the first node N1 for compensation. Meanwhile, at the threshold compensation stage T2, the data write circuit **11** keeps writing the non-enable level Vofs of the data signal Data to the second terminal of the first capacitor C1 so that the potential VN1 of the first node N1 is not coupled to the fourth node N4. Therefore, when the threshold compensation stage T2 ends, the voltage difference across the first capacitor C1 becomes to be equal to VN1−Vofs.

[0050] After the threshold compensation stage T2 ends, the pixel driving circuit enters a data write stage T3 at which the data write circuit **11** writes an enable level Vdata of the data signal Data to the second terminal of the first capacitor C1 so that a potential of the second terminal of the first capacitor C1 changes from Vofs to Vdata, that is, the potential of the second terminal of the first capacitor C1 changes by ΔV=Vdata−Vofs. Meanwhile, due to a coupling effect of the first capacitor C1, the potential of the first node N1 electrically connected to the first terminal of the first capacitor C1 changes accordingly. Since the first node N1 is electrically connected to the second capacitor C2, a variation of the potential of the first node N1 is related to a voltage division of the first node N1 across the first capacitor C1 so that the potential of the first node N1 changes from VN1 to VN1', where VN1'=VN1−(Vdata−Vofs)×(c1/(c1+c2)). That is, the potential VN1' of the first node N1 is Elvdd−Vth−(Vdata−Vofs)×(c1/(c1+c2)), where c1 denotes a capacitance value of the first capacitor C1, and c2 denotes a capacitance value of the second capacitor C2. In this manner, even if the enable level Vdata of the data signal Data written by the data write circuit **11** to the fourth node N4 is a relatively large voltage signal, a signal coupled to the first node N1 is proportional to a ratio of the capacitance value of the first capacitor C1 to a sum of the capacitance values of the two capacitors (the first capacitor C1 and the second capacitor C2) so that the voltage is divided by the first capacitor C1 and the second capacitor C2. Compared with the data signal Data written to the fourth node N4, the variation of the first node N1 is relatively small so that the data signal Data can have a relatively large range to be in a one-to-one correspondence to 0 to 255 grayscales. Therefore, when the data write stage T3 ends, the potential of the first node N1 can also be in a one-to-one correspondence to the 0 to 255 grayscales.

[0051] After the data write stage T3 ends, the pixel driving circuit enters a light emission stage T4. At the light emission stage T4, the light emission control transistor M1 is in a second on state under the control of a second light emission enable level of the light emission control signal Emit so that a drive current I_d generated by the drive transistor MD according to the potential VN1' of the first node N1 is transmitted to the light-emitting element **20** to drive the light-emitting element **20** to emit light. That is, the drive current I_d provided by the drive transistor MD is expressed as follows:

$$I_d = \frac{1}{2}\mu C_{OX}\frac{W_P}{L_P}(V_{SGP} - |V_{thp}|)^2 = \frac{1}{2}\mu C_{OX}\frac{W_P}{L_P}\left((V_{data} - V_{ofs}) * \left(\frac{c_1}{c_1 + c_2}\right)\right)^2.$$

Where μ denotes a carrier mobility of the drive transistor MD, C_{ox} denotes a parasitic capacitance of the gate and a channel region of the drive transistor MD, and W_p/L_p denotes a channel width-to-length ratio of the drive transistor MD. In this manner, at the light emission stage T4, the drive current I_d provided by the drive transistor MD is independent of the threshold voltage Vth of the drive transistor MD so that the current provided by the drive transistor MD is controllable, improving the display uniformity of the display panel including the pixel driving circuit. Meanwhile, at the light emission stage T4, the light emission control transistor M1 is in the second on state, and a relatively large current can flow through the light emission control transistor M1 to quickly charge the anode of the light-emitting element **20** so that a voltage difference between the anode and a cathode of the light-emitting element **20** reaches a light emission threshold Voled of the light-emitting element **20** as soon as possible, that is, a voltage difference between a potential VN3 of the third node N3 and a negative power supply Elvee is greater than or equal to the light emission threshold Voled of the light-emitting element **20**. In this manner, the time required for the light-emitting element **20** to reach stable brightness can be shortened, so as to avoid a significant color cast of the display panel due to a large difference between the times required for the light-emitting elements having different turn-on thresholds to be turned on and further improve the display effect of the display panel.

[0052] In the embodiments of the present disclosure, at the initial stage, the light emission control transistor is in the first on state under the control of the first light emission enable level so that a relatively small current flows through the light emission control transistor on the premise that the anode of the light-emitting element, the second electrode of the drive transistor, and the gate of the drive transistor can be reset in sequence. Therefore, the light emission control transistor has relatively small power consumption, facilitating the low power consumption of the pixel driving circuit. When the pixel driving circuit is applied to the display panel, the low power consumption of the silicon-based display panel can be facilitated and the application requirement of the silicon-based display panel for low power consumption can be satisfied. Moreover, at the light emission stage, the light emission control transistor is in the second on state under the control of the second light emission enable level so that a relatively large current can flow through the light

emission control transistor, and the anode of the light-emitting element can be quickly charged by the drive current provided by the drive transistor, so as to prevent the silicon-based display panel including the pixel driving circuit from the color cast. Additionally, at the threshold compensation stage, the threshold voltage of the drive transistor is provided to the first node for compensation so that the drive current provided by the drive transistor at the light emission stage is independent of the threshold voltage of the drive transistor, so as to prevent a threshold drift of the drive transistor from affecting the display uniformity of the display panel and solve the problem of display non-uniformity of the display panel. Additionally, at the data write stage, the voltage of the first node is divided by the first capacitor and the second capacitor so that even if the enable level of the data signal written by the data write circuit to the second terminal of the first capacitor is a relatively large voltage, a voltage coupled to the second terminal of the first capacitor is proportional to the ratio of the capacitance value of the first capacitor to the sum of the capacitance values of the two capacitors (the first capacitor and the second capacitor). Therefore, by setting the capacitance values of the first capacitor and the second capacitor, the enable level of the data signal changes within a relatively large range and the potential of the first node changes within a relatively small range so that the brightness of the light-emitting element has different levels and can be adjusted with higher accuracy, improving the color richness of the image displayed by the display panel and the display quality of the display panel.

[0053] Optionally, at the threshold compensation stage, the reset circuit continuously provides the reset signal to the third node. In this manner, the third node remains the voltage of the reset signal at the threshold compensation stage, that is, the third node remains a fixed voltage signal at the threshold compensation stage, and the fixed voltage signal is not sufficient to control the light-emitting element to emit light so that the third node is prevented from being charged by a leakage current generated by the light emission control transistor and from reaching the light emission voltage of the light-emitting element, preventing undesired light emission of a pixel.

[0054] It is to be noted that the threshold compensation circuit, the reset circuit, and the data write circuit in the embodiments of the present disclosure may be active elements and/or passive elements. The active element includes, for example, a transistor, and the passive element includes, for example, a resistor, a capacitor, an inductor, and the like. On the premise that the functions of the circuits can be implemented, the structures of the threshold compensation circuit, the reset circuit, and the data write circuit are not specifically limited in the embodiments of the present disclosure.

[0055] The technical solutions in the embodiments of the present disclosure are described below by way of typical examples.

[0056] Optionally, FIG. **5** is a diagram showing specific circuit structures of a pixel driving circuit according to an embodiment of the present disclosure. As shown in FIG. **5**, the reset circuit **13** includes a reset transistor M**4**, and the threshold compensation circuit **12** includes a threshold compensation transistor M**3**. Where the reset transistor M**4** has a first electrode for receiving the reset signal Rest, a second electrode electrically connected to the third node N**3**, and a gate for receiving a second scan signal Scan**2** and is configured to be turned on or off under the control of the second scan signal Scan**2**. The threshold compensation transistor M**3** has a gate for receiving a first scan signal Scan**1**, a first electrode electrically connected to the first node N**1**, and a second electrode electrically connected to the second node N**2** and is configured to be turned on or off under the control of the first scan signal Scan**1**.

[0057] Correspondingly, the data write circuit **11** may include a data write transistor M**2**. The data write transistor M**2** has a first electrode for receiving the data signal Data which includes the enable level Vdata and the non-enable level Vofs, a second electrode electrically connected to the fourth node N**4**, and a gate for receiving a third scan signal Scan**3** so that the data write transistor M**2** is turned on or off under the control of the third scan signal Scan**3**.

[0058] The reset transistor M**4**, the threshold compensation transistor M**3**, and the data write transistor M**2** may also be NMOS or PMOS transistors. The NMOS transistor is turned on when a scan signal received by a gate of the NMOS transistor is at a high level and is turned off when the scan signal is at a low level. The PMOS transistor is turned on when a scan signal received by a gate of the PMOS transistor is at a low level and is turned off when the scan signal is at a high level. The types of the reset transistor M**4**, the threshold compensation transistor M**3**, and the data write transistor M**2** are not specifically limited in the embodiments of the present disclosure. For ease of description, the technical solutions in the embodiments of the present disclosure are exemplarily described below using an example in which all transistors in the pixel driving circuit are PMOS transistors.

[0059] For example, FIG. **6** is a drive timing diagram of a pixel driving circuit in FIG. **5**. As shown in FIGS. **5** and **6**, at the initial stage T**1**, the threshold compensation transistor M**3** is turned on under the control of the first scan signal Scant, the reset transistor M**4** is turned on under the control of the second scan signal Scan**2**, the data write transistor M**2** is turned on under the control of the third scan signal Scan**3**, the light emission control transistor M**1** is turned on under the control of the first light emission enable level of the light emission control signal Emit, the non-enable level Vofs of the data signal Data is written to the fourth node N**4** through the data write transistor M**2** that is on, and the reset signal Rest is written to the anode of the light-emitting element **20** through the reset transistor M**4** that is on, transmitted to the second node N**2** through the light emission control transistor M**1** in the first on state, and written to the first node N**1** through the threshold compensation transistor M**3** that is on, so as to reset the anode of the light-emitting element **20**, the second electrode of the drive transistor, and the gate of the drive transistor, respectively.

[0060] At the threshold compensation stage T**2**, the threshold compensation transistor M**3** remains on under the control of the first scan signal Scant, the reset transistor M**4** remains on under the control of the second scan signal Scan**2**, the data write transistor M**2** remains on under the control of the third scan signal Scan**3**, the light emission control transistor M**1** is turned off under the control of the light emission non-enable level of the light emission control signal Emit, the third node N**3** remains the voltage of the reset signal Rest, and a current through the drive transistor MD and the threshold compensation transistor M**3** continuously charges the first node N**1** until the potential of the first node N**1** becomes VN**1**=Elvdd−Vth so that the threshold

voltage Vth of the drive transistor MD is provided to the first node N1 for compensation. Meanwhile, the fourth node N4 remains the non-enable level Vofs of the data signal Data.

[0061] At the data write stage T3, the threshold compensation transistor M3 is turned off under the control of the first scan signal Scant, the reset transistor M4 is turned off under the control of the second scan signal Scan2, the data write transistor M2 remains on under the control of the third scan signal Scan3, the light emission control transistor M1 remains off under the control of the light emission non-enable level of the light emission control signal Emit, the enable level Vdata of the data signal Data is written to the fourth node N4 through the data write transistor M2 that is on so that a potential of the fourth node N4 changes from the non-enable level Vofs of the data signal Data to the enable level Vdata of the data signal Data, and the potential of the first node N1 changes from VN1 to VN1' through the coupling effect of the first capacitor C1 and a voltage division effect of the second capacitor C2, so that the data signal is written.

[0062] At the light emission stage T4, the threshold compensation transistor M3 remains off under the control of the first scan signal Scant, the reset transistor M4 remains off under the control of the second scan signal Scan2, the data write transistor M2 is turned off under the control of the third scan signal Scan3, and the light emission control transistor M1 is in the second on state under the control of the second light emission enable level of the light emission control signal Emit so that a current path is formed between the positive power supply Elvdd and the negative power supply Elvee, and a relatively large current may flow through the light emission control transistor M1 to quickly drive the light-emitting element **20** to stably emit light.

[0063] As can be seen from the preceding analysis, the threshold compensation transistor and the reset transistor are on at the same stages so that when the reset transistor and the threshold compensation transistor are of the same channel type, the gates of the reset transistor and the threshold compensation transistor receive the same scan signal. In this case, as shown in FIG. **7**, the first scan signal Scan1 for controlling the reset transistor M4 to be turned on or off may also serve as the second scan signal for controlling the threshold compensation transistor M3 to be turned on or off, which can reduce the number of signals provided to the pixel driving circuit, reduce the number of ports for receiving signals in the pixel driving circuit, simplify the structure of the pixel driving circuit, and reduce the cost of the pixel driving circuit.

[0064] On the basis of the preceding embodiments, optionally, FIG. **8** is a structure diagram of another pixel driving circuit according to an embodiment of the present disclosure. As shown in FIG. **8**, the pixel driving circuit further includes a signal conversion circuit **14** electrically connected to the gate Mg of the light emission control transistor M1. The signal conversion circuit **14** is configured to provide, at the initial stage, the first light emission enable level to the gate Mg of the light emission control transistor M1 to control the light emission control transistor M1 to be in the first on state, provide, at the threshold compensation stage and the data write stage, the light emission non-enable level to the gate Mg of the light emission control transistor M1 to control the light emission control transistor M1 to be in an off state, and provide, at the light emission stage, the second light emission enable level to the gate Mg of the light emission control transistor M1 to control the light emission control transistor M1 to be in the second on state.

[0065] In this manner, the signal conversion circuit can provide different light emission control signals at different stages to control the light emission control transistor to be in different on states so that the drive transistor is reset and the light-emitting element is promoted to enter a stable light emission stage at the light emission stage, improving the light emission accuracy of the light-emitting element while ensuring that the pixel driving circuit has lower power consumption.

[0066] Optionally, FIG. **9** is a structure diagram of a signal conversion circuit according to an embodiment of the present disclosure. As shown in FIGS. **8** and **9**, the signal conversion circuit **14** includes a first enable level conversion circuit **141**, a second enable level conversion circuit **142**, and a third enable level conversion circuit **143**; where the first enable level conversion circuit **141** is electrically connected to a first level signal terminal VP1, a first logic control signal terminal CTRL1, and the gate Mg of the light emission control transistor M1 and configured to provide the first light emission enable level from the first level signal terminal VP1 to the gate Mg of the light emission control transistor M1 under the control of a first logic control signal Ctrl1 from the first logic control signal terminal CTRL1; the second enable level conversion circuit **142** is electrically connected to a first light emission control signal terminal XOUT, a second level signal terminal VP2, and the gate Mg of the light emission control transistor M1 and configured to provide the second light emission enable level from the second level signal terminal VP2 to the gate Mg of the light emission control transistor M1 under the control of a first light emission control signal outputted from the first light emission control signal terminal XOUT; and the third enable level conversion circuit **143** is electrically connected to a second logic control signal terminal CTRL2, a second light emission control signal terminal OUT, a third level signal terminal VP3, and the gate Mg of the light emission control transistor M1 and configured to provide the light emission non-enable level from the third level signal terminal VP3 to the gate Mg of the light emission control transistor M1 under the control of a second light emission control signal outputted from the second light emission control signal terminal OUT and a second logic control signal outputted from the second logic control signal terminal CTRL2.

[0067] Specifically, at the initial stage, the first enable level conversion circuit **141** transmits the first light emission enable level from the first level signal terminal VP1 to the gate Mg of the light emission control transistor M1 under the control of the first logic control signal Ctrl1 from the first logic control signal terminal CTRL1 so that the light emission control transistor M1 can be in the first on state and the reset signal of the third node N3 can be transmitted to the second node N2 and the first node N1 in sequence to reset the anode of the light-emitting element **20** and the gate and the second electrode of the drive transistor MD. At the threshold compensation stage and the data write stage, the third enable level conversion circuit **143** transmits the light emission non-enable level from the third level signal terminal VP3 to the gate Mg of the light emission control transistor M1 under the control of the second light emission control signal outputted from the second light emission control signal terminal OUT and the second logic control signal outputted from the second logic control signal termi-

nal CTRL2 so that the light emission control transistor M1 is in the off state, and the third node N3 is prevented from being charged by the corresponding electrical signal, so as to prevent the undesired light emission of the pixel. At the light emission stage, the second enable level conversion circuit **142** transmits the second light emission enable level from the second level signal terminal VP2 to the gate Mg of the light emission control transistor M1 under the control of the first light emission control signal outputted from the first light emission control signal terminal XOUT so that the light emission control transistor M1 is in the second on state, the drive current provided by the drive transistor MD can be quickly transmitted to the anode of the light-emitting element **20** to charge the anode of the light-emitting element **20**, and thus the light-emitting element **20** quickly enters the stable light emission stage.

[0068] The first enable level conversion circuit **141**, the second enable level conversion circuit **142**, and the third enable level conversion circuit **143** may be composed of various elements. The specific structures of the first enable level conversion circuit **141**, the second enable level conversion circuit **142**, and the third enable level conversion circuit **143** are not limited in the embodiments of the present disclosure.

[0069] For example, FIG. **10** is a diagram showing specific circuit structures of a signal conversion circuit according to an embodiment of the present disclosure. As shown in FIGS. **9** and **10**, the first enable level conversion circuit **141** includes a first transistor M21 which has a gate electrically connected to the first logic control signal terminal CTRL1, a first electrode electrically connected to the first level signal terminal VP1, and a second electrode electrically connected to the gate Mg of the light emission control transistor; the second enable level conversion circuit **142** includes a second transistor M22 which has a gate electrically connected to the first light emission control signal terminal XOUT, a first electrode electrically connected to the second level signal terminal VP2, and a second electrode electrically connected to the gate Mg of the light emission control transistor; and the third enable level conversion circuit **143** includes a NAND gate U1 and a third transistor M23, where the NAND gate U1 has a first input terminal electrically connected to the second logic control signal terminal CTRL2, a second input terminal electrically connected to the second light emission control signal terminal OUT, and an output terminal electrically connected to a gate of the third transistor M23; and the third transistor M23 further has a first electrode electrically connected to the third level signal terminal VP3 and a second electrode electrically connected to the gate Mg of the light emission control transistor.

[0070] It is to be noted that FIG. **10** is only an example drawing in the embodiments of the present disclosure and only shows the channel types of transistors for example. On the premise that the functions of the level conversion circuits can be implemented, the channel types of the transistors in the level conversion circuits are not specifically limited in the embodiments of the present disclosure.

[0071] For ease of description, the technical solutions in the embodiments of the present disclosure are exemplarily described below using an example in which the first transistor M21 and the third transistor M23 are PMOS transistors and the second transistor M22 is an NMOS transistor.

[0072] FIG. **11** is a drive timing diagram of a signal conversion circuit in FIG. **10**. As shown in FIGS. **10** and **11**, at the initial stage T1, the first logic control signal Ctrl1 from the first logic control signal terminal CTRL1 is at a low level so that the first transistor M21 is turned on, the first light emission enable level from the first level signal terminal VP1 is transmitted as the first light emission enable level of the light emission control signal Emit to the gate Mg of the light emission control transistor through the first transistor M21 that is on, and thus the light emission control transistor is in the first on state. Correspondingly, the second logic control signal Ctrl2 from the second logic control signal terminal CTRL2 is a low level, and the second light emission control signal Out from the second light emission control signal terminal OUT is at a high level so that the NAND gate U1 outputs a logic high level signal to control the third transistor M23 to be in the off state. Meanwhile, the first light emission control signal Xout from the first light emission control signal terminal XOUT is at a low level so that the second transistor M22 is also in the off state.

[0073] At the threshold compensation stage T2 and the data write stage T3, the first logic control signal Ctrl1 from the first logic control signal terminal CTRL1 is at a high level so that the first transistor M21 is in the off state; the second logic control signal Ctrl2 from the second logic control signal terminal CTRL2 is at a high level, and the second light emission control signal Out from the second light emission control signal terminal OUT is also at a high level so that the NAND gate U1 outputs a logic low level signal to control the third transistor M23 to be in an on state, the light emission non-enable level from the third level signal terminal VP3 is transmitted as the light emission control signal Emit to the gate Mg of the light emission control transistor through the third transistor M23 that is on, and the light emission control transistor is controlled to be in the off state; the first light emission control signal Xout from the first light emission control signal terminal XOUT is at a low level so that the second transistor M22 remains off.

[0074] At the light emission stage T4, the first logic control signal Ctrl1 from the first logic control signal terminal CTRL1 remains at the high level so that the first transistor M21 remains off the second logic control signal Ctrl2 from the second logic control signal terminal CTRL2 is at a high level, and the second light emission control signal Out from the second light emission control signal terminal OUT is at a low level so that the NAND gate U1 outputs a logic high level signal to control the third transistor M23 to be in the off state; the first light emission control signal Xout from the first light emission control signal terminal XOUT is at a high level so that the second transistor M22 is in the on state, the second light emission enable level from the second level signal terminal VP2 is transmitted as the light emission control signal Emit to the gate Mg of the light emission control transistor through the second transistor M22 that is on, and thus the light emission control transistor is in the second on state.

[0075] The first transistor M21 and the third transistor M23 are both the PMOS transistors, and the first logic control signal Ctrl1 from the first logic control signal terminal CTRL1 is the same as the second logic control signal Ctrl2 from the second logic control signal terminal CTRL2 so that the first logic control signal terminal CTRL1 may also serve as the second logic control signal terminal CTRL2. That is, when the first transistor M21 and the third transistor M23 are of the same channel type, the first logic

control signal terminal CTRL**1** may also serve as the second logic control signal terminal CTRL**2**, so as to reduce the number of signals provided to the signal conversion circuit.

[0076] Correspondingly, the second transistor M**22** is the NMOS transistor, the third transistor M**23** is the PMOS transistor, and the first light emission control signal Xout from the first light emission control signal terminal XOUT is reverse to the second light emission control signal Out from the second light emission control signal terminal OUT, that is, when the second transistor M**22** and the third transistor M**23** are of different channel types, the first light emission control signal Xout is reverse to the second light emission control signal Out.

[0077] Optionally, FIG. **12** is a diagram showing specific circuit structures of another signal conversion circuit according to an embodiment of the present disclosure. As shown in FIG. **12**, the signal conversion circuit may further include a first phase inverter U**2** which may be electrically connected between the first light emission control signal terminal XOUT and the second light emission control signal terminal OUT. In this manner, only the first light emission control signal Xout is provided to the first light emission control signal terminal XOUT of the signal conversion circuit, or only the second light emission control signal Out is provided to the second light emission control signal terminal OUT, so as to reduce the number of signals provided to the signal conversion circuit.

[0078] Based on the same inventive concept, the embodiments of the present disclosure further provide a method for driving a pixel driving circuit. The method is used for driving the pixel driving circuit provided by the embodiments of the present disclosure. FIG. **13** is a flowchart of a method for driving a pixel driving circuit according to an embodiment of the present disclosure. As shown in FIG. **13**, the method for driving a pixel driving circuit includes steps described below.

[0079] In S**110**, at an initial stage, a reset circuit provides a reset signal to a third node to reset an anode of a light-emitting element; a light emission control transistor is in a first on state under the control of a first light emission enable level to transmit the reset signal to a second node to reset a second electrode of a drive transistor; a threshold compensation circuit transmits the reset signal to a first node to reset a first capacitor, a second capacitor, and a gate of the drive transistor; and a data write circuit transmits a non-enable level of a data signal to a second terminal of the first capacitor.

[0080] In S**120**, at a threshold compensation stage, the light emission control transistor is in an off state; a threshold compensation transistor provides a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit continues writing the non-enable level of the data signal to the second terminal of the first capacitor.

[0081] In S**130**, at a data write stage, the light emission control transistor is in the off state; and the data write circuit writes an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1'**.

[0082] VN**1'**=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), where Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor.

[0083] In S**140**, at a light emission stage, the light emission control transistor is in a second on state under the control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1'** of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light.

[0084] A smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

[0085] In this manner, at the initial stage, the light emission control transistor is in the first on state under the control of the first light emission enable level so that a relatively small current flows through the light emission control transistor on the premise that the anode of the light-emitting element, the second electrode of the drive transistor, and the gate of the drive transistor can be reset in sequence. Therefore, the light emission control transistor has relatively small power consumption, facilitating the low power consumption of the pixel driving circuit. When the pixel driving circuit is applied to a display panel, the low power consumption of a silicon-based display panel can be facilitated and the application requirement of the silicon-based display panel for low power consumption can be satisfied. Moreover, at the light emission stage, the light emission control transistor is in the second on state under the control of the second light emission enable level so that a relatively large current can flow through the light emission control transistor, and the anode of the light-emitting element can be quickly charged by the drive current provided by the drive transistor, so as to prevent the silicon-based display panel including the pixel driving circuit from a color cast. Additionally, at the threshold compensation stage, the threshold voltage of the drive transistor is provided to the first node for compensation so that the drive current provided by the drive transistor at the light emission stage is independent of the threshold voltage of the drive transistor, so as to prevent a threshold drift of the drive transistor from affecting the display uniformity of the display panel and solve the problem of display non-uniformity of the display panel. Additionally, at the data write stage, the voltage of the first node is divided by the first capacitor and the second capacitor so that even if the enable level of the data signal written by the data write circuit to the second terminal of the first capacitor is a relatively large voltage, a voltage coupled to the second terminal of the first capacitor is proportional to a ratio of the capacitance value of the first capacitor to a sum of the capacitance values of the two capacitors (the first capacitor and the second capacitor). Therefore, by setting the capacitance values of the first capacitor and the second capacitor, the enable level of the data signal changes within a relatively large range and the potential of the first node changes within a relatively small range so that the brightness of the light-emitting element has different levels and can be adjusted with higher accuracy, improving the color richness of the image displayed by the display panel and the display quality of the display panel.

[0086] Optionally, at the threshold compensation stage, the reset circuit continuously provides the reset signal to the third node. In this manner, the third node remains the voltage of the reset signal at the threshold compensation stage, that is, the third node remains a fixed voltage signal at the threshold compensation stage, and the fixed voltage signal is not sufficient to control the light-emitting element to emit light so that the third node is prevented from being charged

by a leakage current generated by the light emission control transistor and from reaching the light emission voltage of the light-emitting element, preventing undesired light emission of a pixel.

[0087] Based on the same inventive concept, the embodiments of the present disclosure further provide a silicon-based display panel. The silicon-based display panel includes a plurality of light-emitting elements and a plurality of pixel driving circuits arranged in an array. The plurality of pixel driving circuits are configured to drive the plurality of light-emitting elements to emit light. The pixel driving circuit is provided by the embodiments of the present disclosure. Therefore, the silicon-based display panel provided by the embodiments of the present disclosure includes the technical features of the pixel driving circuit provided by the embodiments of the present disclosure and has the beneficial effects of the pixel driving circuit provided by the embodiments of the present disclosure. For the same content, reference may be made to the description of the pixel driving circuit provided by the embodiments of the present disclosure. The details are not repeated here.

[0088] The silicon-based display panel includes a silicon-based substrate, and the pixel driving circuits and the light-emitting elements in the silicon-based display panel are all formed on one side of the silicon-based substrate. That is, various devices of the silicon-based display panel may be formed on the silicon-based substrate using CMOS technology. Since a device formed directly on the silicon-based substrate has the physical characteristics of a micro device, the silicon-based display panel can display a high-quality image.

[0089] Optionally, FIG. **14** is a structure diagram of a silicon-based display panel according to an embodiment of the present disclosure. As shown in FIG. **14**, a silicon-based display panel **100** includes a display region **110** and a non-display region **120** surrounding the display region **110**, where the light-emitting elements are disposed in the display region **110**; the silicon-based display panel **100** further includes a light emission scan driving circuit **30** disposed in the non-display region **120**; the light emission scan driving circuit **30** includes a plurality of light emission scan drive units **31** cascaded; each of the plurality of light emission scan drive units **31** is electrically connected to gates of light emission control transistors M**1** in pixel driving circuits in one respective row. In this case, one pixel driving circuit and one light-emitting element may constitute one pixel **10**. Each of the plurality of light emission scan drive units **31** is configured to output, in sequence, a light emission control signal to the light emission control transistors M**1** in the pixel driving circuits in the one respective row. The light emission control signal includes a first light emission enable level, a second light emission enable level, or a light emission non-enable level. In this manner, at a reset stage, each light emission scan drive unit **31** may output, in sequence, the first light emission enable level of the light emission control signal to the gates of the light emission control transistors M**1** in one respective row of pixels **10** so that the light emission control transistors M**1** in each row of pixels **10** are in a first on state in sequence to reset drive transistors and light-emitting elements in the each row of pixels **10** in sequence. At a threshold compensation stage and a data write stage, each light emission scan drive unit **31** outputs the light emission non-enable level to the gates of the light emission control transistors M**1** in one respective row of pixels **10** so that the light emission control transistors M**1** in each row of pixels **10** are in an off state. At a light emission stage, each light emission scan drive unit **31** may output, in sequence, the second light emission enable level of the light emission control signal to the gates of the light emission control transistors M**1** in one respective row of pixels **10** so that the light emission control transistors M**1** in each row of pixels **10** are in a second on state in sequence, and drive currents provided by the drive transistors in the each row of pixels **10** are provided to the light-emitting elements in the each row of pixels **10** in sequence to drive the light-emitting elements in the each row of pixels **10** to emit light in sequence, thereby causing the silicon-based display panel **100** to display a corresponding image.

[0090] Additionally, the display region **110** of the silicon-based display panel **100** may further include light emission control signal lines **41**, a plurality of reset signal lines **43**, and a plurality of data signal lines **42**; where gates of light emission control transistors M**1** in at least part of pixel driving circuits in the same row are electrically connected to the same light emission control signal line **41** which is configured to transmit the light emission control signal; reset circuits in at least part of pixel driving circuits in the same row or the same column are electrically connected to the same reset signal line **43** which is configured to transmit a reset signal; data write circuits in at least part of pixel driving circuits in the same column are electrically connected to the same data signal line **42** which is configured to transmit a data signal; and each light emission scan drive unit **31** is electrically connected to gates of light emission control transistors M**1** in pixel driving circuits in one respective row through a respective one of the plurality of light emission control signal lines **41**. In this manner, the light emission control signal provided by the light emission scan drive unit **31** may be transmitted to light emission control transistors M**1** in corresponding pixels **10** through a corresponding light emission control signal line **41**, the reset signal is provided to reset circuits in each row of pixels **10** through a respective reset signal line **43**, and the data signal is transmitted to data write circuits in each column of pixels **10** through a respective data signal line **42**.

[0091] Optionally, FIG. **15** is a structure diagram of another silicon-based display panel according to an embodiment of the present disclosure. As shown in FIG. **15**, when the pixel driving circuit includes a signal conversion circuit **14**, the signal conversion circuit **14** may be electrically connected between the light emission control signal line **41** and the light emission control transistor M**1**. The signal conversion circuit **14** is configured to convert, at an initial stage, the light emission control signal transmitted through the light emission control signal line to the first light emission enable level to control the light emission control transistor M**1** to be in the first on state, convert, at the threshold compensation stage and the data write stage, the light emission control signal transmitted through the light emission control signal line to the light emission non-enable level to control the light emission control transistor M**1** to be in the off state, and convert, at the light emission stage, the light emission control signal transmitted through the light emission control signal line to the second light emission enable level to control the light emission control transistor M**1** to be in the second on state. In this manner, the signal conversion circuit **14** is provided in each pixel driving circuit to convert the light emission control signal outputted

from the light emission scan drive unit **31** to a corresponding level signal so that the on state of the light emission control transistor is controlled, which can ensure that the reset stage, the threshold compensation stage, the data write stage, and the light emission stage of the pixel driving circuit are steadily performed while reducing power consumption.

[0092] Optionally, FIG. **16** is a structure diagram of another silicon-based display panel according to an embodiment of the present disclosure. As shown in FIG. **16**, when the pixel driving circuit includes the signal conversion circuit **14**, pixel driving circuits electrically connected to the same light emission control signal line **41** share the signal conversion circuit **14**, that is, the signal conversion circuit **14** is electrically connected between the light emission scan drive unit **31** and the light emission control signal line **41**. Similarly, the signal conversion circuit **14** is configured to convert, at the initial stage, the light emission control signal outputted by the light emission scan drive unit to the first light emission enable level to control the light emission control transistors to be in the first on state, convert, at the threshold compensation stage and the data write stage, the light emission control signal outputted by the light emission scan drive unit to the light emission non-enable level to control the light emission control transistors to be in the off state, and convert, at the light emission stage, the light emission control signal outputted by the light emission scan drive unit to the second light emission enable level to control the light emission control transistors to be in the second on state. In this manner, the pixel driving circuits electrically connected to the same light emission control signal line share the signal conversion circuit, which can reduce the number of signal conversion circuits in the silicon-based display panel, simplify the structure of the pixel driving circuit in the silicon-based display panel, and improve the aperture ratio of the silicon-based display panel.

[0093] Based on the same inventive concept, the embodiments of the present disclosure further provide a display device. The display device includes the silicon-based display panel provided by the embodiments of the present disclosure. Therefore, the display device provided by the embodiments of the present disclosure includes the technical features of the silicon-based display panel provided by the embodiments of the present disclosure and can achieve the beneficial effects of the silicon-based display panel provided by the embodiments of the present disclosure. For the same, reference may be made to the description of the silicon-based display panel provided by the embodiments of the present disclosure. The details are not repeated here. The display device provided by the embodiments of the present disclosure may include, but is not limited to, a wearable device having a display function, such as a wristwatch, a bracelet, and VR glasses.

[0094] It is to be noted that the preceding are only preferred embodiments of the present disclosure and technical principles used therein. It is to be understood by those skilled in the art that the present disclosure is not limited to the embodiments described herein. Those skilled in the art can make various apparent modifications, adaptations, combinations, and substitutions without departing from the scope of the present disclosure. Therefore, while the present disclosure has been described in detail through the preceding embodiments, the present disclosure is not limited to the preceding embodiments and may include more other equivalent embodiments without departing from the concept of the present disclosure. The scope of the present disclosure is determined by the scope of the appended claims.

What is claimed is:

1. A pixel driving circuit for driving a light-emitting element to emit light, comprising: a drive transistor, a light emission control transistor, a first capacitor, a second capacitor, a reset circuit, a data write circuit, and a threshold compensation circuit; wherein

a gate of the drive transistor, a first terminal of the first capacitor, a second terminal of the second capacitor, and the threshold compensation circuit are electrically connected to a first node; a first terminal of the second capacitor is configured to receive a fixed voltage signal; a first electrode of the light emission control transistor, a second electrode of the drive transistor, and the threshold compensation circuit are electrically connected to a second node; a second electrode of the light emission control transistor, the reset circuit, and an anode of the light-emitting element are electrically connected to a third node;

at an initial stage, the reset circuit is configured to provide a reset signal to the third node to reset the anode of the light-emitting element; the light emission control transistor is configured to be in a first on state under control of a first light emission enable level to transmit the reset signal to the second node to reset the second electrode of the drive transistor; the threshold compensation circuit is configured to transmit the reset signal to the first node to reset the first capacitor, the second capacitor, and the gate of the drive transistor; and the data write circuit is configured to transmit a non-enable level of a data signal to a second terminal of the first capacitor;

at a threshold compensation stage, the threshold compensation circuit is configured to provide a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit is configured to continue writing the non-enable level of the data signal to the second terminal of the first capacitor;

at a data write stage, the data write circuit is configured to write an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1**', wherein VN**1**'=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor; and

at a light emission stage, the light emission control transistor is configured to be in a second on state under control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1**' of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light;

wherein a smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

2. The pixel driving circuit according to claim **1**, further comprising a signal conversion circuit electrically connected to a gate of the light emission control transistor; wherein

the signal conversion circuit is configured to: provide, at the initial stage, the first light emission enable level to

the gate of the light emission control transistor to control the light emission control transistor to be in the first on state, provide, at the threshold compensation stage and the data write stage, a light emission non-enable level to the gate of the light emission control transistor to control the light emission control transistor to be in an off state, and provide, at the light emission stage, the second light emission enable level to the gate of the light emission control transistor to control the light emission control transistor to be in the second on state.

3. The pixel driving circuit according to claim **2**, wherein the signal conversion circuit comprises a first enable level conversion circuit, a second enable level conversion circuit, and a third enable level conversion circuit; wherein

the first enable level conversion circuit is electrically connected to a first level signal terminal, a first logic control signal terminal, and the gate of the light emission control transistor and configured to provide the first light emission enable level from the first level signal terminal to the gate of the light emission control transistor under control of a first logic control signal outputted from the first logic control signal terminal;

the second enable level conversion circuit is electrically connected to a first light emission control signal terminal, a second level signal terminal, and the gate of the light emission control transistor and configured to provide the second light emission enable level from the second level signal terminal to the gate of the light emission control transistor under control of a first light emission control signal outputted from the first light emission control signal terminal; and

the third enable level conversion circuit is electrically connected to a second logic control signal terminal, a second light emission control signal terminal, a third level signal terminal, and the gate of the light emission control transistor and configured to provide the light emission non-enable level from the third level signal terminal to the gate of the light emission control transistor under control of a second light emission control signal outputted from the second light emission control signal terminal and a second logic control signal outputted from the second logic control signal terminal.

4. The pixel driving circuit according to claim **3**, wherein the first enable level conversion circuit comprises a first transistor, a gate of the first transistor is electrically connected to the first logic control signal terminal, a first electrode of the first transistor is electrically connected to the first level signal terminal, and a second electrode of the first transistor is electrically connected to the gate of the light emission control transistor;

wherein the second enable level conversion circuit comprises a second transistor, a gate of the second transistor is electrically connected to the first light emission control signal terminal, a first electrode of the second transistor is electrically connected to the second level signal terminal, and a second electrode of the second transistor is electrically connected to the gate of the light emission control transistor; and

wherein the third enable level conversion circuit comprises a NAND gate and a third transistor, wherein a first input terminal of the NAND gate is electrically connected to the second logic control signal terminal, a second input terminal of the NAND gate is electrically connected to the second light emission control signal terminal, and an output terminal of the NAND gate is electrically connected to a gate of the third transistor; and wherein a first electrode of the third transistor is electrically connected to the third level signal terminal and a second electrode of the third transistor is electrically connected to the gate of the light emission control transistor.

5. The pixel driving circuit according to claim **4**, wherein the first transistor and the third transistor are of a same channel type; and

the first logic control signal terminal serves as the second logic control signal terminal.

6. The pixel driving circuit according to claim **4**, wherein the second transistor and the third transistor are of different channel types; and

the first light emission control signal is reverse to the second light emission control signal.

7. The pixel driving circuit according to claim **6**, wherein the signal conversion circuit further comprises a first phase inverter; wherein

the first phase inverter is electrically connected between the first light emission control signal terminal and the second light emission control signal terminal.

8. The pixel driving circuit according to claim **1**, wherein at the threshold compensation stage, the reset circuit is further configured to continuously provide the reset signal to the third node.

9. The pixel driving circuit according to claim **8**, wherein the reset circuit comprises a reset transistor, and the threshold compensation circuit comprises a threshold compensation transistor; wherein

a first electrode of the reset transistor is configured for receiving the reset signal, a second electrode of the reset transistor is electrically connected to the third node, and a gate of the reset transistor is configured for receiving a second scan signal and is configured to be turned on or off under control of the second scan signal; and

a gate of the threshold compensation transistor is configured for receiving a first scan signal, a first electrode of the threshold compensation transistor is electrically connected to the first node, and a second electrode of the threshold compensation transistor is electrically connected to the second node and is configured to be turned on or off under control of the first scan signal.

10. The pixel driving circuit according to claim **9**, wherein the reset transistor and the threshold compensation transistor are of a same channel type; and

the first scan signal serves as the second scan signal.

11. A silicon-based display panel, comprising a plurality of light-emitting elements and a plurality of pixel driving circuits, wherein the plurality of pixel driving circuits are arranged in an array and configured to drive the plurality of light-emitting elements to emit light;

wherein each of the plurality of pixel driving circuits comprises:

a drive transistor, a light emission control transistor, a first capacitor, a second capacitor, a reset circuit, a data write circuit, and a threshold compensation circuit; wherein

a gate of the drive transistor, a first terminal of the first capacitor, a second terminal of the second capacitor, and the threshold compensation circuit are electrically connected to a first node;

a first terminal of the second capacitor is configured to receive a fixed voltage signal; a first electrode of the light emission control transistor, a second electrode of the drive transistor, and the threshold compensation circuit are electrically connected to a second node; a second electrode of the light emission control transistor, the reset circuit, and an anode of the light-emitting element are electrically connected to a third node;

at an initial stage, the reset circuit is configured to provide a reset signal to the third node to reset the anode of the light-emitting element; the light emission control transistor is configured to be in a first on state under control of a first light emission enable level to transmit the reset signal to the second node to reset the second electrode of the drive transistor; the threshold compensation circuit is configured to transmit the reset signal to the first node to reset the first capacitor, the second capacitor, and the gate of the drive transistor; and the data write circuit is configured to transmit a non-enable level of a data signal to a second terminal of the first capacitor;

at a threshold compensation stage, the threshold compensation circuit is configured to provide a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit is configured to continue writing the non-enable level of the data signal to the second terminal of the first capacitor;

at a data write stage, the data write circuit is configured to write an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1'**, wherein VN**1'**=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor; and

at a light emission stage, the light emission control transistor is configured to be in a second on state under control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1'** of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light;

wherein a smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

12. The silicon-based display panel according to claim **11**, comprising a display region and a non-display region surrounding the display region, wherein the plurality of light-emitting elements are disposed in the display region;

wherein the silicon-based display panel further comprises a light emission scan driving circuit disposed in the non-display region;

wherein the light emission scan driving circuit comprises a plurality of light emission scan drive units cascaded, each of the plurality of light emission scan drive units is electrically connected to gates of light emission control transistors in pixel driving circuits in one respective row, and each of the plurality of light emission scan drive units is configured to output, in sequence, a light emission control signal to the light emission control transistors in the pixel driving circuits in the one respective row;

wherein the light emission control signal comprises a first light emission enable level, a second light emission enable level, or a light emission non-enable level.

13. The silicon-based display panel according to claim **12**, wherein the display region further comprises a plurality of light emission control signal lines, a plurality of reset signal lines, and a plurality of data signal lines; wherein

gates of light emission control transistors in at least part of pixel driving circuits in a same row are electrically connected to a same light emission control signal line which is configured to transmit the light emission control signal;

reset circuits in at least part of pixel driving circuits in a same row or a same column are electrically connected to a same reset signal line which is configured to transmit a reset signal;

data write circuits in at least part of pixel driving circuits in a same column are electrically connected to a same data signal line which is configured to transmit a data signal; and

each of the plurality of light emission scan drive units is electrically connected to gates of light emission control transistors in pixel driving circuits in one respective row through a respective one of the plurality of light emission control signal lines.

14. The silicon-based display panel according to claim **13**, wherein each of the plurality of pixel driving circuits further comprises a signal conversion circuit electrically connected between the light emission control signal line and a light emission control transistor in the each of the plurality of pixel driving circuits;

wherein the signal conversion circuit is configured to convert, at an initial stage, the light emission control signal transmitted through the light emission control signal line to the first light emission enable level to control the light emission control transistor to be in a first on state, convert, at a threshold compensation stage and a data write stage, the light emission control signal transmitted through the light emission control signal line to the light emission non-enable level to control the light emission control transistor to be in an off state, and convert, at a light emission stage, the light emission control signal transmitted through the light emission control signal line to the second light emission enable level to control the light emission control transistor to be in a second on state.

15. The silicon-based display panel according to claim **13**, wherein each of the plurality of pixel driving circuits further comprises a signal conversion circuit, and pixel driving circuits electrically connected to the same light emission control signal line share the signal conversion circuit;

the signal conversion circuit is electrically connected between one of the plurality of light emission scan drive units and the light emission control signal line; and the signal conversion circuit is configured to: convert, at an initial stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the first light emission enable level to control the light emission control transistors to be in a first on state, convert, at a threshold

compensation stage and a data write stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the light emission non-enable level to control the light emission control transistors to be in an off state, and convert, at a light emission stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the second light emission enable level to control the light emission control transistors to be in a second on state.

16. A display device, comprising a silicon-based display panel, wherein the silicon-based display panel comprises a plurality of light-emitting elements and a plurality of pixel driving circuits, and the plurality of pixel driving circuits are arranged in an array and configured to drive the plurality of light-emitting elements to emit light;

wherein each of the plurality of pixel driving circuits comprises:

a drive transistor, a light emission control transistor, a first capacitor, a second capacitor, a reset circuit, a data write circuit, and a threshold compensation circuit; wherein

a gate of the drive transistor, a first terminal of the first capacitor, a second terminal of the second capacitor, and the threshold compensation circuit are electrically connected to a first node; a first terminal of the second capacitor is configured to receive a fixed voltage signal; a first electrode of the light emission control transistor, a second electrode of the drive transistor, and the threshold compensation circuit are electrically connected to a second node; a second electrode of the light emission control transistor, the reset circuit, and an anode of the light-emitting element are electrically connected to a third node;

at an initial stage, the reset circuit is configured to provide a reset signal to the third node to reset the anode of the light-emitting element; the light emission control transistor is configured to be in a first on state under control of a first light emission enable level to transmit the reset signal to the second node to reset the second electrode of the drive transistor; the threshold compensation circuit is configured to transmit the reset signal to the first node to reset the first capacitor, the second capacitor, and the gate of the drive transistor; and the data write circuit is configured to transmit a non-enable level of a data signal to a second terminal of the first capacitor;

at a threshold compensation stage, the threshold compensation circuit is configured to provide a threshold voltage of the drive transistor to the first node for compensation such that a potential of the first node is equal to VN**1**; and the data write circuit is configured to continue writing the non-enable level of the data signal to the second terminal of the first capacitor;

at a data write stage, the data write circuit is configured to write an enable level of the data signal to the second terminal of the first capacitor such that the potential of the first node changes from VN**1** to VN**1**', wherein VN**1**'=VN**1**−(Vdata−Vofs)×(c**1**/(c**1**+c**2**)), Vdata denotes the enable level of the data signal, Vofs denotes the non-enable level of the data signal, c**1** denotes a capacitance value of the first capacitor, and c**2** denotes a capacitance value of the second capacitor; and

at a light emission stage, the light emission control transistor is configured to be in a second on state under control of a second light emission enable level such that a drive current generated by the drive transistor according to the potential VN**1**' of the first node is transmitted to the light-emitting element to drive the light-emitting element to emit light;

wherein a smaller current flows through the light emission control transistor in the first on state than the light emission control transistor in the second on state.

17. The display device according to claim **16**, comprising a display region and a non-display region surrounding the display region, wherein the plurality of light-emitting elements are disposed in the display region;

wherein the silicon-based display panel further comprises a light emission scan driving circuit disposed in the non-display region;

wherein the light emission scan driving circuit comprises a plurality of light emission scan drive units cascaded, each of the plurality of light emission scan drive units is electrically connected to gates of light emission control transistors in pixel driving circuits in one respective row, and each of the plurality of light emission scan drive units is configured to output, in sequence, a light emission control signal to the light emission control transistors in the pixel driving circuits in the one respective row;

wherein the light emission control signal comprises a first light emission enable level, a second light emission enable level, or a light emission non-enable level.

18. The display device according to claim **17**, wherein the display region further comprises a plurality of light emission control signal lines, a plurality of reset signal lines, and a plurality of data signal lines; wherein

gates of light emission control transistors in at least part of pixel driving circuits in a same row are electrically connected to a same light emission control signal line which is configured to transmit the light emission control signal;

reset circuits in at least part of pixel driving circuits in a same row or a same column are electrically connected to a same reset signal line which is configured to transmit a reset signal;

data write circuits in at least part of pixel driving circuits in a same column are electrically connected to a same data signal line which is configured to transmit a data signal; and

each of the plurality of light emission scan drive units is electrically connected to gates of light emission control transistors in pixel driving circuits in one respective row through a respective one of the plurality of light emission control signal lines.

19. The display device according to claim **18**, wherein each of the plurality of pixel driving circuits further comprises a signal conversion circuit electrically connected between the light emission control signal line and a light emission control transistor in the each of the plurality of pixel driving circuits;

wherein the signal conversion circuit is configured to convert, at an initial stage, the light emission control signal transmitted through the light emission control signal line to the first light emission enable level to control the light emission control transistor to be in a first on state, convert, at a threshold compensation stage

and a data write stage, the light emission control signal transmitted through the light emission control signal line to the light emission non-enable level to control the light emission control transistor to be in an off state, and convert, at a light emission stage, the light emission control signal transmitted through the light emission control signal line to the second light emission enable level to control the light emission control transistor to be in a second on state.

20. The display device according to claim **18**, wherein each of the plurality of pixel driving circuits further comprises a signal conversion circuit, and pixel driving circuits electrically connected to the same light emission control signal line share the signal conversion circuit;

the signal conversion circuit is electrically connected between one of the plurality of light emission scan drive units and the light emission control signal line; and the signal conversion circuit is configured to: convert, at an initial stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the first light emission enable level to control the light emission control transistors to be in a first on state, convert, at a threshold compensation stage and a data write stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the light emission non-enable level to control the light emission control transistors to be in an off state, and convert, at a light emission stage, the light emission control signal outputted by the one of the plurality of light emission scan drive units to the second light emission enable level to control the light emission control transistors to be in a second on state.

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