(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 935 021 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
15.01.2020 Bulletin 2020/03

(21) Application number: **06813638.1**

(22) Date of filing: **23.08.2006**

(51) Int Cl.:
H01L 27/146 *(2006.01)*

(86) International application number:
PCT/US2006/032770

(87) International publication number:
WO 2007/024855 (01.03.2007 Gazette 2007/09)

(54) **IMPLANTED ISOLATION REGION FOR IMAGER PIXELS**

IMPLANTIERTE ISOLATIONSREGION FÜR BILDGEBER-PIXEL

REGION D'ISOLATION IMPLANTEE POUR PIXELS D'IMAGEUR

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

(30) Priority: **26.08.2005 US 211651**

(43) Date of publication of application:
25.06.2008 Bulletin 2008/26

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EP 1 935 021 B1

Printed by Jouve, 75001 PARIS (FR)

Description

FIELD OF THE INVENTION

[0001] The present invention relates generally to digital image sensors and in particular to isolating pixel cells in an imager array.

BACKGROUND OF THE INVENTION

[0002] Typically, a digital imager array includes a focal plane array of pixel cells, each one of the cells including a photosensor, e.g. a photogate, photoconductor, or a photodiode. In a CMOS imager a readout circuit is connected to each pixel cell which typically includes a source follower output transistor. The photosensor converts photons to electrons which are typically transferred to a storage region, e.g., a floating diffusion region, which is connected to the gate of the source follower output transistor. A charge transfer device (e.g., transistor) can be included for transferring charge from the photosensor to the floating diffusion region. In addition, such imager cells typically have a transistor for resetting the floating diffusion region to a predetermined charge level prior to charge transference. The output of the source follower transistor is gated as a pixel output signal by a row select transistor.

[0003] Exemplary CMOS imaging circuits, processing steps thereof, and detailed descriptions of the functions of various CMOS elements of an imaging circuit are described, for example, in U.S. Patent No. 6,140,630, U.S. Patent No. 6,376,868, U.S. Patent No. 6,310,366, U.S. Patent No. 6,326,652, U.S. Patent No. 6,204,524, and U.S. Patent No. 6,333,205, each assigned to Micron Technology, Inc.

[0004] EP A2 0 501 316, US 2004/094784 A1, EP A 1 427 023, JP 11 274461 A, US 2005/087781, EP A 0 862 219, EP 1 566 842 A2, EP 1 376 701 A2, EP 1 244 149 A2, EP 1 017 106 A2 disclose imagers having active pixel sensors.

[0005] With reference to FIGS. 1 and 2, which respectively illustrate a top-down and a cross-sectional view of a conventional CMOS pixel sensor cell 100, when incident light 187 strikes the surface of a photodiode photosensor 120, electron/hole pairs are generated in the silicon. The generated electrons (photo-charges) are collected in the n-type accumulation region 122 just below the p+ surface layer 123 of the photodiode photosensor 120. The photo-charges move from the initial charge accumulation region 122 to a floating diffusion region 110 via a transfer transistor 106. The charge at the floating diffusion region 110 is typically converted to a pixel output voltage by a source follower transistor 108 and subsequently output on a column output line 111 via a row select transistor 109.

[0006] Conventional CMOS images, such as that shown in FIG. 1, typically achieve approximately a fifty percent fill factor or less, meaning that less than half of the pixel 100 is utilized as the photosensor for converting light to charge carriers. As shown in FIG. 1, only a small portion of the cell 100 comprises a photosensitive element (i.e., photosensor 120). The remainder of the pixel cell 100 includes isolation regions 102 (FIG. 2), shown as shallow trench isolation (STI) or local oxidation on silicon (LOCOS) regions in a substrate 101, the floating diffusion region 110 coupled to a transfer gate 106' of the transfer transistor 106, and source/drain regions 115 for reset 107, source follower 108, and row select 109 transistors having respective gates 107', 108', and 109'. Moreover, as the total pixel area continues to decrease (due to desired scaling), it becomes increasingly important to create high sensitivity photosensors that utilize a minimum amount of surface area and/or to develop more efficient layouts of the pixel array for the non-photosensitive components of the cells to provide an increased size for the photosensitive areas.

[0007] As briefly mentioned above, shallow trench isolation (STI) is one technique that can be used to isolate pixels from one another in a pixel array, or other integrated structures from one another. As depicted in FIG. 2, an STI region 102 is typically formed as an isolation trench 117 formed in the substrate 101 to isolate the active areas of one pixel from other pixel cells. In a typical STI isolation structure 102, a trench 117 is etched into the substrate 101 and filled with one or more layers of dielectric material 125 to provide a physical and electrical barrier between adjacent active areas within a substrate. For example, an STI structure 102 can be formed by etching a trench 117 and then filling it with a dielectric 125 such as a chemical vapor deposited (CVD) or high density plasma (HDP) silicon oxide or silicon dioxide (SiO_2). The filled trench is then planarized by a chemical mechanical planarization (CMP) or etch-back process so that the dielectric 125 remains only in the trench 117 and its top surface remains level with that of the silicon substrate 101. To enhance the isolation further, ions may be implanted into the silicon substrate 101 in the area 140 directly beneath the trench 117.

[0008] Further, although deeper STI regions 102 may provide better isolation, there is a limit as to how deep the STI region 102 can be made. If the STI region 102 is too deep, filling the trench 117 with oxide layers 125 may produce voids or cracks 116 in the filled trench 117. In addition, creating an isolation trench 117 that is too wide takes away area of the pixel cell 100 that could otherwise be photosensitive, thereby decreasing the pixel's 100 fill factor.

[0009] A pixel array having sufficient pixel isolation and having an increased fill factor is therefore desired.

BRIEF SUMMARY OF THE INVENTION

[0010] The present invention, in the various exemplary embodiments, provides a pixel cell array architecture as disclosed in claim 1.

[0011] In accordance with the invention, to further im-

prove the photosensor fill factor, the neighboring pixel cells share pixel components, including parts operative for reading out signals from the pixels. In addition, angled transfer gates are used.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention, in which:

FIG. 1 is a top-down view of a conventional CMOS pixel cell;
FIG. 2 is a cross-sectional view of the pixel cell of FIG. 1, taken along line 1-1';
FIG. 3 is a cross-sectional view of a portion of two adjacent pixel cells, constructed in accordance with a first exemplary embodiment of the invention;
FIG. 4 is a top-down view of a portion of a pixel array constructed in accordance with a second exemplary embodiment of the invention;
FIG. 5 is a top-down view of a portion of a pixel array constructed in accordance with a third exemplary embodiment of the invention;
FIG. 6 is a top-down view of a portion of a pixel array constructed in accordance with a fourth exemplary embodiment of the invention;
FIG. 7 is a block diagram of a CMOS imager chip having an array of pixel cells constructed in accordance with the invention; and
FIG. 8 is a schematic diagram of a processing system employing a CMOS imager constructed in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the scope of the present invention. The progression of processing steps described is exemplary of embodiments of the invention; however, the sequence of steps is not limited to that set forth herein and may be changed as is known in the art, with the exception of steps necessarily occurring in a certain order.

[0014] The terms "wafer" and "substrate," as used herein, are to be understood as including silicon, epitaxial silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous processing steps may have been utilized to form regions, junctions, or material layers in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, gallium arsenide or other semiconductors.

[0015] The term "pixel," as used herein, refers to a photo-element unit cell containing a photosensor and associated transistors for converting photons to an electrical signal. For purposes of illustration, representative pixels are illustrated in the figures and their formation is described herein; however, typically fabrication of a plurality of like pixels proceeds simultaneously. Accordingly, the following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

[0016] The terms "at an angle," "angled," and "slanted," as used herein are to be interpreted as meaning at any angle, with respect to some stated reference point, that is not exactly parallel or exactly perpendicular. Accordingly, when a part of an object and some reference point meet to form an angle that is not 0°, 90°, or 180°, the object is considered "angled," "at an angle," or "slanted" with respect to the reference point.

[0017] Now turning to the figures, where like numerals represent like elements, FIG. 3 depicts a cross-sectional view of two adjacent pixel cells 301, 302 having photosensors 303, 304 separated by an isolation region 222, constructed in accordance with the invention. Specifically, the isolation region 222 consists of at least one p-well ion implant 250 formed between two n-type charge accumulation regions 313, 314 in a p-type epitaxial layer 300 above a p+ substrate. The illustrated isolation region 222 begins at a top surface of the epitaxial layer 300 and ends at a depth in the epitaxial layer 300 that is deeper than that of the adjacent charge accumulation regions 313, 314.

[0018] In accordance with the invention the isolation region 222 is formed of several p-well ion implants 250 that effectively form a solid p-well isolation region 222. Each ion-implant region 250 is formed by implanting an appropriate ion, such as boron, into a pre-determined area of the p-type epitaxial layer 300. The doping concentration of the implants 250 may be in the range of approximately $1e^{11}$ to $1e^{15}$ atoms per cm^3. Photosensor 303 has a top p+ enhancement layer 323, and similarly photosensor 304 has a p+ enhancement layer 324, each located just below a top surface of the epitaxial layer 300. Similarly, the ion-implant isolation region 222 has a p+ enhancement layer 251 near the surface of the epitaxial layer 300. It should be understood that the p+ enhancement layers, although designated with different numerals 323, 324 and 251, may be formed as one or more blanket enhancement deposition layers. In addition, the p+ enhancement layer 251 has a higher concentration of ions than the implant regions 250.

[0019] Each pixel cell 301, 302 has a photosensor 303, 304 for generating photo-charges in response to incident

light. The photosensors 303, 304 are illustratively a p-/n-/p+ photodiode, although it should be understood that the invention is not limited to a photodiode photosensor or to a photodiode having specific n or p-type concentrations. The photo-charges accumulate in the n-type accumulation regions 313, 314, and are transferred respectively by a transfer transistor 315, 316, to an associated floating diffusion region 309, 310. Other pixel circuitry (not shown) is connected to each floating diffusion region 309, 310 for generating and reading out a signal representing the amount of charge transferred to the floating diffusion regions 309, 310. This readout circuitry may include a source follower transistor and row select transistor, as described above with reference to FIG. 1 and other known four transistor (4T) pixel cell circuits described, for example, in the above-referenced patents.

[0020] In accordance with this exemplary embodiment, the ion-implant isolation region 222 of the invention has several advantages over the conventional STI region 102 (FIG. 2) discussed above. First, the formation of the implanted isolation region 222 mitigates the stress and silicon dislocations associated with the STI trench in addition to reducing the cracks and/or voids that are associated with the deposition of oxide layers in an STI trench. In fact, the isolation region 222 can be formed deeper in the epitaxial layer 300 than a conventional STI region (102 in FIG. 2), thereby preventing unwanted charge flow beneath the isolation region 222.

[0021] Next, although conventional STI regions are often a site for electron generation/reaction, which leads to dark current, replacing the STI region with the ion-implant isolation region 222 eliminates this component of dark current from hot pixel defects. Because neither dark current nor electron generation is a major concern with the ion-implant isolation region 222, the active area (i.e., n-type accumulation region 313, 314) of each photosensor 303, 304 for adjacent cells 301, 302, can be located closer to one another and to the sidewall of the isolation region 222 than would be true if a conventional isolation trench was used. The spacing necessary between the isolation region 222 and each n-type accumulation region 313, 314 may therefore be cut in half, which advantageously increases the fill factor for pixel cells 301, 302, as more of a pixel's surface area can be photosensitive.

[0022] In addition, it should be understood that other isolation techniques, including but not limited to STI, can be used in conjunction with the present invention for providing isolation in other areas of the pixel arrays. For example, although the implant isolation region 222 is preferably used to isolate the neighboring photosensors 303, 304 from one another, other pixel components, like transistors, may be separated by other isolation techniques, including, but not limited to, STI or LOCOS regions.

[0023] FIG. 4 represents a top-down view of a portion of a pixel array 198 constructed in accordance with a second exemplary embodiment of the invention. As shown in FIG. 4, two neighboring pixel cells 201, 202 each have an associated photosensor 203, 204, respectively. The active areas of the photosensors 203, 204, which are depicted as dashed lines because they would not be visible in a top-down perspective of the cells, may comprise accumulation regions of a photodiode, for example. The photosensors 203, 204 are separated by an isolation region 320, which is preferably an STI isolation region.

[0024] Extending into the isolation region 320 is a trunk region 340 which is associated with a pixel pair in an adjacent row of the pixel array 198. The trunk region 340 may include active areas for transistors and a floating diffusion region for the pixels similar to those shared by the pixels 201, 202.

[0025] On either side of the photosensors 203, 204 opposite the isolation region 320 is an ion-implant isolation region 222 in accordance with the invention. The ion-implant isolation region 222 is used to isolate the photosensors 203, 204 from respective photosensor areas on adjacent pixels in the same column of the array 198. The ion-implant isolation region 222 may comprise a p-well region having a p+ enhancement layer on top of the p-well, when the active area of the photosensors 203, 204 are n-type accumulation regions. Thus, the implant isolation region 222 may be the same as the isolation region 222 discussed above with reference to FIG. 3.

[0026] In the FIG. 4 embodiment, each pixel cell 201, 202 has a transfer gate 215, 216 for a respective pair of transfer transistors; at least one edge 229 of the transfer gate is preferably angled with respect to the photosensors 203, 204 for improving the fill factor of pixel cells 211, 212. The transfer transistors, located at a corner of the photosensors 203, 204 transfer photo-charges generated by the photosensors 203, 204 through the transfer gates 215, 216 to a shared floating diffusion region 210, which serves as a common storage node for the pixels 201, 202. Other shared pixel components in this embodiment include a reset transistor 206 having a gate 206', which is located on a side of the floating diffusion region 210 opposite the photosensors 203, 204. A source/drain region 217 is located on a second side of the reset transistor gate 206' and is capable of receiving a supply voltage $V_{aa\text{-}pix}$. The floating diffusion region 210 is also electrically connected to the gate 207' of a source follower transistor 207, which has a drain coupled to $V_{aa\text{-}pix}$. The source follower transistor 207 creates a voltage output signal based on stored charge at the floating diffusion region 210. A row select transistor 208 having a gate 208' has a drain connected to the source of the source follower transistor 207, for selectively reading out the pixel signals to a column line 220.

[0027] A third exemplary embodiment of the invention is shown in top-down view in FIG. 5. It should be understood that while it is possible a cross-section of this third embodiment could be drawn as illustrated in FIG. 3, the third embodiment includes a unique layout of the remaining pixel components that are not shown in FIG. 3. The

third exemplary embodiment includes two neighboring pixel cells 211, 212 having associated photosensors 213, 214, respectively. The photosensors 213, 214 are separated by an isolation region 320, which may be an STI region. As discussed above with respect to FIG. 4, a trunk region 340 for pixels in an adjacent row may extend into the isolation region 320.

[0028] Each pixel cell 211, 212 has an associated transfer gate 215, 216, respectively. In a preferred embodiment, the transfer gates 215, 216 are angled with respect to the associated photosensors 213, 214. The remaining pixel cell components are shared between the two pixel cells 211, 212. The FIG. 5 embodiment also shows the shared pixel components in a "split trunk" architecture, meaning that a first trunk that includes a first active region 227, where the transfer transistors, shared floating diffusion region 210 and reset transistor 206 are located, is physically separated from, but electrically connected to, a second trunk including a second active region 228. The second trunk includes gates for a source follower 207 and row select 208 transistors. The second trunk 228 can be located in an isolation region 320, located adjacent a photosensor 213 on pixel 211. A connector 290, that electrically connects the two trunks, may take the form of a buried interconnect near the surface of the substrate or a metallization wiring layer above the substrate.

[0029] Turning to FIG. 6, a fourth exemplary embodiment of the invention is now described. FIG. 6 shows a top-down view of a portion of the pixel array 550. The pixel array 550 architecture includes 4-way sharing of pixel components among individual pixel cells having respective photosensors 601, 602, 603, 604. These four pixels have a shared architecture shown by dotted lines area 710 in FIG. 6. The shared architecture includes a linearly- extending trunk located within the area between the pair of photosensors 601, 603 and the pair of photosensors 602, and 604. Isolation regions 222 in accordance with the invention are located between each two adjacent photosensors. For example, between photosensor pairs 601 and 521 and between 522 and 523. Other types of isolation regions 320 may also be used, for instance, to isolate the capacitors 518 or other parts of the circuitry. These isolation regions 320 may be STI or LOCOS regions.

[0030] Each pixel cell has an associated transfer transistor gate 605, 606, 607, 608 for transferring charges from the photosensors 601, 602, 603, 604. At least a portion, such as an edge 692, of each transfer gate 605, 606, 607, 608 is preferably at an angle 692 with respect to the photosensors 601, 602, 603, 604 as shown in FIG. 6. It should also be noted that the transfer transistor gates 605, 606, 607, 608 of this embodiment are being shared, each among two adjacent pixels in a column. For example, column adjacent pixel photosensors 601 and 521 each share the transfer gate 605. The two illustrated pixels (having associated photosensors 601, 521) that share a transfer transistor gate (605), however, do not share a floating diffusion region or readout circuit. Rather, this embodiment has two row adjacent pixels having photosensors 601 and 602 sharing a first floating diffusion region 610, and two row adjacent photosensors and 603, 604 sharing a second floating diffusion region 620.

[0031] The two floating diffusion regions 610, 620 are electrically connected to one another and to one electrode of an associated capacitor 518 and the source follower transistor 514 through a first metallization layer formed above the surface of the pixel array 550. As shown in FIG. 6, each capacitor 518 is connected at another side to a contact receiving a source voltage, e.g., $V_{aa\text{-}pix}$, at source/drain region 513 through a second metallization layer.

[0032] One reset transistor having a gate 512 is utilized for resetting the charges at both floating diffusion regions 610, 620 and the associated capacitor 518. To one side of the reset gate 512 is a source/drain region 513 that is capable of receiving a supply voltage $V_{aa\text{-}pix}$. The four pixel cells having associated photosensors 601, 602, 603, 604 share a common readout circuit that includes a source follower transistor having a gate 514 and a row select transistor having a gate 516. The four pixels also share the optional capacitor 518 which can increase the storage capacity of the two associated floating diffusion regions 510, 520.

[0033] The four-way shared pixel layout described herein illustratively has four pixels with respective photosensors 601, 602, 603, 604 sharing one set of readout circuitry 710. Photosensors 601 and 602 are adjacent within the same row. Photosensors 603 and 604 are adjacent within the same row directly above or below photosensors 601 and 602. Photosensors 601, 603 are column adjacent to photosensors 602, 604. Thus, a column output line V_{out} is only necessary, in accordance with this exemplary embodiment, for every other column in the array.

[0034] The illustrated, 4-way shared pixel array configuration has at least two distinct advantages: it allows for larger pitch circuits in the periphery in the column direction and it reduces the metallization layers needed in the layers above the surface of the pixel array 550 while increasing the photosensitive area and thus quantum efficiency over the conventional pixel array. In addition, each capacitor 518 is efficiently located at the corners of four photosensors, such as shown at the clipped edges 711 of photosensors 602, 604. This location allows for a maximized capacitor area without sacrificing photosensitive area, or thereby decreasing the fill factor of the pixels array 550.

[0035] FIG. 7 illustrates a block diagram of an exemplary CMOS imager 500 having a pixel array 400 with pixels constructed in accordance with the embodiments described above. Pixel array 400 comprises a plurality of pixels arranged in a predetermined number of columns and rows (not shown). Attached to the array 400 is signal processing circuitry, as described herein. The pixels of each row in array 400 are all turned on at the same time

by a row select line, and the pixels of each column are selectively output by respective column select lines. A plurality of row and column lines are provided for the entire array 400. The row lines are selectively activated by a row driver 410 in response to row address decoder 420. The column select lines are selectively activated by a column driver 460 in response to column address decoder 470. Thus, a row and column address is provided for each pixel.

[0036] The CMOS imager 500 is operated by the timing and control circuit 450, which controls address decoders 420, 470 for selecting the appropriate row and column lines for pixel imaging and readout. The control circuit 450 also controls the row and column driver circuitry 410, 460 such that these apply driving voltages to the drive transistors of the selected row and column lines. The pixel column signals, which typically include a pixel reset signal (V_{rst}) and a pixel image signal (V_{sig}), are read by a sample and hold circuit 465 associated with the column driver 460. A differential signal (V_{rst} - V_{sig}) is produced by differential amplifier 467 for each pixel, which is digitized by analog-to-digital converter 475 (ADC). The analog-to-digital converter 475 supplies the digitized pixel signals to an image processor 480, which forms and outputs a digital image.

[0037] FIG. 8 shows a processor system 508, which includes an imaging device 500 constructed in accordance with an embodiment of the invention. The processor system 508 may be part of a digital camera, computer or other imaging or processing system. The imaging device 500 may receive control or other data from system 508. System 508 includes a processor 502 such as a central processing unit (CPU) for image processing, or other processing operations. The processor 502 communicates with various devices over a bus 504. Some of the devices connected to the bus 504 provide communication into and out of the system 508; an input/output (I/O) device 506 and imaging device 500 are such communication devices. Other devices connected to the bus 504 provide memory, for instance, a random access memory (RAM) 510 or a removable memory 515.

[0038] The processes and devices described above illustrate preferred methods and typical devices of many that could be used and produced. The above description and drawings illustrate embodiments, which achieve the objects, features, and advantages of the present invention. However, it is not intended that the present invention be strictly limited to the above-described and illustrated embodiments. For example, although the implant isolation region is shown only in context with CMOS pixel imager cells, it should be understood that the invention may have a broader scope of application, being useful as an isolation technique for isolating pixels or photosensors in any solid state imaging device. In addition, it should be understood that other isolation techniques may be useful in conjunction with the present invention, as mentioned above with respect to FIG. 3.

Claims

1. A pixel cell array comprising:

a first pixel cell and a second pixel cell adjacent to the first pixel cell,
the first pixel cell comprising:

a material layer (300) having a first conductivity type (p);
a photosensor (303, 304) formed in the material layer, the photosensor comprising: an active charge accumulation area (313, 314) of a second conductivity type (n) being opposite to the first conductivity type (p); and
a first doped surface layer (323, 324) located over the active charge accumulation area and doped to the first conductivity type (p); and
an isolation region (222) located adjacent one side of the photosensor and serving as an isolation region between a portion of the photosensor of the first pixel cell and a portion of a photosensor of the second pixel cell, the isolation region comprising:

a doped region (250) doped to the first conductivity type (p) and to a first concentration; and
a second doped surface layer (251) located just below the surface of the material layer in an area over the doped region, the second doped surface layer (251) being doped to the first conductivity type and to a second concentration that is greater than the first concentration,
wherein the doped region comprises a plurality of p-well ion-doped regions (250), and
wherein the first and second doped surface layers are p+ doped surface layers,
the first and second pixel cells each further comprising a transfer transistor (315, 316) having a transfer gate (215, 216) that is located on a side of the active charge accumulation area opposite the isolation region,
wherein the photosensor (203) of the first pixel cell and a photosensor (204) of the second pixel cell each have four edges defining an essentially rectangular shape of the respective photosensor, **characterized in that** the transfer transistor gates are provided at a non-zero angle with respect to the edges of the photosensor of the respective pixel

cell,
wherein the transfer gates (215) are located at adjacent corners of the photosensors of the first and second pixel cells,
wherein the transfer transistors are configured to transfer photo charges generated by the photosensors (203, 204) through the transfer gates (215, 216) to a shared floating diffusion region (210), which serves as a common storage node for the first and second pixel cells.

2. The pixel cell array of claim 1, wherein the transfer transistors and the shared floating diffusion region (210) are part of a first active region (227) of the pixel cells and wherein a second active region (228) of the pixel cells, physically separated from, but electrically connected to, the first active region, comprises at least one source follower transistor (207) for generating a signal from the pixel cells.

3. The pixel cell array of claim 2, wherein the first and second active regions are electrically connected by a conductive interconnect (290).

4. The pixel cell array of claim 3, wherein the conductive interconnect (290) comprises a buried conductor.

5. The pixel cell array of claim 3, wherein the conductive interconnect comprises a metallization wiring layer.

6. The pixel cell array of one of the preceding claims, wherein a shallow trench isolation region (320) is formed between the first and second pixel cells (211, 212) to isolate areas other than the active charge accumulation areas.

7. A processing system (508) comprising:

a processor (502); and
an imaging device (500) electrically coupled to said processor, said imaging device comprising the pixel cell array of one of the preceding claims.

8. A method of forming a pixel cell array of one of claims 1 to 6 having a first pixel cell and a second pixel cell adjacent to the first pixel cell, the method comprising:

forming a photosensor (313) in a material layer (300) of a first conductivity type (p), the photosensor including an active charge accumulation area (313) doped to a second conductivity type (n) being opposite to the first conductivity type (p), and a first doped surface layer (323) doped to the first conductivity type (p), wherein the first doped surface layer is located over the active charge accumulation area;
performing first ion-implants to form a plurality of first implant regions (250) doped to the first conductivity type (p) and to a first concentration, wherein the first implant regions (250) are adjacent to a first side of the active charge accumulation area; and
performing a second ion-implant above the first implant regions (250) and just below the surface of the material layer (300) to form a second doped surface layer (251), the second ion-implant doped to the first conductivity type (p) and to a second concentration that is greater than the first concentration,
wherein the first implant regions (250) are formed as p-well ion-doped regions and the second doped surface layer (251) is formed as a p+ doped surface layer above the first implant regions (250).

9. The method of claim 8, wherein the transfer transistors and the shared floating diffusion region (210) are part of a first active region (227) of the pixel cells and wherein a second active region (228) of the pixel cells, physically separated from, but electrically connected to, the first active region, comprises at least one source follower transistor (207) for generating a signal from the pixel cells.

10. The method of claim 8 or 9, wherein the act of forming the first doped surface layer (324) comprises performing a blank deposition of boron ions above the second doped surface layer (251) and the active charge accumulation area (314).

11. The method of claim 9, further comprising forming a shallow trench isolation region (320) between the first and second pixel cells (211,212) to isolate areas other than the charge accumulation areas.

12. An imager device comprising:
the pixel cell array of one of claims 1 to 6 and further comprising a plurality of pixel cells in rows and columns, an wherein the adjacent pixel cells are formed in a substrate.

13. The imager device of claim 12, wherein the imager is a CMOS imager and the pixel cells are CMOS pixels.

14. The imager device of claim 12, further comprising a second pair of adjacent pixel cells, wherein the isolation region is formed in an area between at least a portion of each of the first and the second pair of adjacent pixel cells.

15. The imager device of claim 14, wherein the first and

the second pairs of pixel cells include column adjacent pixel cells.

Patentansprüche

1. Pixelzellenfeld, umfassend:
eine erste Pixelzelle und eine zweite Pixelzelle, die an die erste Pixelzelle angrenzt, wobei die erste Pixelzelle umfasst:

eine Materialschicht (300) mit einem ersten Leitfähigkeitstyp (p);
einen in der Materialschicht ausgebildeten Photosensor (303, 304), wobei der Photosensor umfasst:

einen aktiven Ladungsakkumulationsbereich (313, 314) eines zweiten Leitfähigkeitstyps (n), der dem ersten Leitfähigkeitstyp (p) entgegengesetzt ist; und
eine erste dotierte Oberflächenschicht (323, 324), die über dem aktiven Ladungsakkumulationsbereich angeordnet und auf den ersten Leitfähigkeitstyp (p) dotiert ist; und
ein Isolationsgebiet (222), das angrenzend an eine Seite des Photosensors angeordnet ist und als Isolationsgebiet zwischen einem Abschnitt des Photosensors der ersten Pixelzelle und einem Abschnitt eines Photosensors der zweiten Pixelzelle dient, wobei das Isolationsgebiet umfasst:

ein dotiertes Gebiet (250), das auf den ersten Leitfähigkeitstyp (p) und auf eine erste Konzentration dotiert ist; und
eine zweite dotierte Oberflächenschicht (251), die sich direkt unterhalb der Oberfläche der Materialschicht in einem Bereich über dem dotierten Gebiet befindet, wobei die zweite dotierte Oberflächenschicht (251) auf den ersten Leitfähigkeitstyp und auf eine zweite Konzentration dotiert ist, die größer als die erste Konzentration ist,
wobei das dotierte Gebiet eine Vielzahl von ionendotierten p-Wannengebieten (250) umfasst, und
wobei die ersten und zweiten dotierten Oberflächenschichten auf p+ dotierte Oberflächenschichten sind,
wobei die ersten und zweiten Pixelzellen ferner jeweils einen Übertragungstransistor (315, 316) mit einem Übertragungs-Gate (215, 216) umfassen, das sich auf einer Seite des aktiven Ladungsakkumulationsbereichs gegenüber dem Isolationsgebiet befindet,
wobei der Photosensor (203) der ersten Pixelzelle und ein Photosensor (204) der zweiten Pixelzelle jeweils vier Kanten aufweisen, die eine im Wesentlichen rechteckige Form des jeweiligen Photosensors definieren,
dadurch gekennzeichnet, dass die Gates der Übertragungstransistoren in einem Winkel ungleich Null in Bezug auf die Kanten des Photosensors der jeweiligen Pixelzelle bereitgestellt sind,
wobei die Übertragungs-Gates (215) an aneinander angrenzenden Ecken der Photosensoren der ersten und zweiten Pixelzellen angeordnet sind,
wobei die Übertragungstransistoren konfiguriert sind, um von den Photosensoren (203, 204) erzeugte Photoladungen durch die Übertragungs-Gates (215, 216) zu einem gemeinsamen potentialfreien Diffusionsgebiet (210) zu übertragen, das als gemeinsamer Speicherknoten für die ersten und zweiten Pixelzellen dient.

2. Pixelzellenfeld nach Anspruch 1, wobei die Übertragungstransistoren und das gemeinsame potentialfreie Diffusionsgebiet (210) Teil eines ersten aktiven Gebiets (227) der Pixelzellen sind und wobei ein zweites aktives Gebiet (228) der Pixelzellen, das physikalisch von dem ersten aktiven Gebiet getrennt, aber elektrisch mit diesem verbunden ist, mindestens einen Quellfolgertransistor (207) zum Erzeugen eines Signals aus den Pixelzellen umfasst.

3. Pixelzellenfeld nach Anspruch 2, wobei das erste und zweite aktive Gebiet durch eine leitende Verbindung (290) elektrisch verbunden sind.

4. Pixelzellenfeld nach Anspruch 3, wobei die leitende Verbindung (290) einen vergrabenen Leiter umfasst.

5. Pixelzellenfeld nach Anspruch 3, wobei die leitende Verbindung eine Metallverdrahtungsschicht umfasst.

6. Pixelzellenfeld nach einem der vorhergehenden Ansprüche, wobei ein Isolationsgebiet (320) mit einem flachen Graben zwischen den ersten und zweiten Pixelzellen (211, 212) ausgebildet ist, um andere Bereiche als die aktiven Ladungsakkumulationsbereiche zu isolieren.

7. Verarbeitungssystem (508), umfassend:

einen Prozessor (502); und
eine Bildaufnahmevorrichtung (500), die elek-

trisch mit dem Prozessor gekoppelt ist, wobei die Bildaufnahmevorrichtung das Pixelzellenfeld nach einem der vorherigen Ansprüche umfasst.

8. Verfahren zum Bilden eines Pixelzellenfelds nach einem der Ansprüche 1 bis 6 mit einer ersten Pixelzelle und einer zweiten Pixelzelle, die an die erste Pixelzelle angrenzt, wobei das Verfahren umfasst:

Bilden eines Photosensors (313) in einer Materialschicht (300) mit einem ersten Leitfähigkeitstyp (p), wobei der Photosensor einen aktiven Ladungsakkumulationsbereich (313), der auf einen zweiten Leitfähigkeitstyp (n) dotiert ist, der zu dem ersten Leitfähigkeitstyp (p) entgegengesetzt ist, und eine erste dotierte Oberflächenschicht (323), die auf den ersten Leitfähigkeitstyp (p) dotiert ist, beinhaltet, wobei die erste dotierte Oberflächenschicht über dem aktiven Ladungsakkumulationsbereich angeordnet ist;
Durchführen erster Ionenimplantierungen, um eine Vielzahl von ersten Implantatgebieten (250) auszubilden, die auf den ersten Leitfähigkeitstyp (p) und auf eine erste Konzentration dotiert werden, wobei die ersten Implantatgebiete (250) an eine erste Seite des aktiven Ladungsakkumulationsbereichs angrenzen; und
Durchführen einer zweiten Ionenimplantierung über den ersten Implantatgebieten (250) und direkt unter der Oberfläche der Materialschicht (300), um eine zweite dotierte Oberflächenschicht (251) auszubilden, wobei das zweite Ionenimplantat auf den ersten Leitfähigkeitstyp (p) und auf eine zweite Konzentration dotiert wird, die größer als die erste Konzentration ist,
wobei die ersten Implantatgebiete (250) als ionendotierte p-Wannengebiete ausgebildet werden und die zweite dotierte Oberflächenschicht (251) als p+ dotierte Oberflächenschicht über den ersten Implantatgebieten (250) ausgebildet wird.

9. Verfahren nach Anspruch 8, wobei die Übertragungstransistoren und das gemeinsame potentialfreie Diffusionsgebiet (210) Teil eines ersten aktiven Gebiets (227) der Pixelzellen sind und wobei ein zweites aktives Gebiet (228) der Pixelzellen, das physikalisch von dem ersten aktiven Gebiet getrennt, aber elektrisch mit diesem verbunden ist, mindestens einen Quellfolgertransistor (207) zum Erzeugen eines Signals aus den Pixelzellen umfasst.

10. Verfahren nach Anspruch 8 oder 9, wobei der Akt des Ausbildens der ersten dotierten Oberflächenschicht (324) das Durchführen einer Leerabscheidung von Borionen über der zweiten dotierten Oberflächenschicht (251) und dem aktiven Ladungsakkumulationsbereich (314) umfasst.

11. Verfahren nach Anspruch 9, ferner umfassend das Ausbilden eines Isolationsgebiets (320) mit einem flachen Graben zwischen den ersten und zweiten Pixelzellen (211, 212), um andere Bereiche als die Ladungsakkumulationsbereiche zu isolieren.

12. Bildaufnahmevorrichtung, umfassend:
das Pixelzellenfeld nach einem der Ansprüche 1 bis 6, und ferner umfassend eine Vielzahl von Pixelzellen in Zeilen und Spalten, und wobei die aneinander angrenzenden Pixelzellen in einem Substrat ausgebildet sind.

13. Bildaufnahmevorrichtung nach Anspruch 12, wobei der Bildaufnehmer ein CMOS-Bildaufnehmer ist und die Pixelzellen CMOS-Pixel sind.

14. Bildaufnahmevorrichtung nach Anspruch 12, die ferner ein zweites Paar aneinander angrenzender Pixelzellen umfasst, wobei das Isolationsgebiet in einem Bereich zwischen mindestens einem Teil von jedem des ersten und des zweiten Paars aneinander angrenzender Pixelzellen ausgebildet ist.

15. Bildaufnahmevorrichtung nach Anspruch 14, wobei die ersten und die zweiten Paare von Pixelzellen an Spalten angrenzende Pixelzellen beinhalten.

Revendications

1. Réseau de cellules de pixel comprenant :
une première cellule de pixel et une seconde cellule de pixel adjacente à la première cellule de pixel, la première cellule de pixel comprenant :

une couche de matériau (300) ayant un premier type de conductivité (p) ;
un photodétecteur (303, 304) formé dans la couche de matériau, le photodétecteur comprenant : une zone active d'accumulation de charges (313, 314) d'un second type de conductivité (n) opposé au premier type de conductivité (p) ; et
une première couche de surface dopée (323, 324) située au-dessus de la zone active d'accumulation de charges et dopée au premier type de conductivité (p) ; et
une région d'isolation (222) située adjacente à un côté du photodétecteur et servant de région d'isolation entre une partie du photodétecteur de la première cellule de pixel et une partie d'un photodétecteur de la seconde cellule de pixel, la région d'isolation comprenant :

une région dopée (250) dopée au premier

type de conductivité (p) et à une première concentration ; et
une seconde couche de surface dopée (251) située juste au-dessous de la surface de la couche de matériau dans une zone au-dessus de la région dopée, la seconde couche de surface dopée (251) étant dopée au premier type de conductivité et à une seconde concentration qui est supérieure à la première concentration,
dans lequel la région dopée comprend une pluralité de régions de puits p dopées aux ions (250) et
dans lequel les première et seconde couches de surface dopées sont des couches de surface dopées p+,
les première et seconde cellules de pixel comprenant chacune en outre un transistor de transfert (315, 316) ayant une grille de transfert (215, 216) qui est située d'un côté de la zone active d'accumulation de charges opposé à la région d'isolation,
dans lequel le photodétecteur (203) de la première cellule de pixel et un photodétecteur (204) de la seconde cellule de pixel présentent chacun quatre bords définissant une forme essentiellement rectangulaire du photodétecteur respectif,
caractérisé en ce que les grilles de transistor de transfert sont prévues à un angle non nul par rapport aux bords du photodétecteur de la cellule de pixel respective,
les grilles de transfert (215) étant situées à des coins adjacents des photodétecteurs des première et seconde cellules de pixel,
les transistors de transfert étant configurés pour transférer les photocharges générées par les photodétecteurs (203, 204) via les grilles de transfert (215, 216) vers une zone de diffusion flottante partagée (210) qui sert de nœud de stockage commun pour les première et seconde cellules de pixel.

2. Réseau de cellules de pixel selon la revendication 1, dans lequel les transistors de transfert et la région de diffusion flottante partagée (210) font partie d'une première région active (227) des cellules de pixel et dans lequel une seconde région active (228) des cellules de pixel, séparée physiquement de la première région active mais connectée électriquement à celle-ci, comprend au moins un transistor suiveur de source (207) pour générer un signal à partir des cellules de pixel.

3. Réseau de cellules de pixel selon la revendication 2, dans lequel les première et seconde régions actives sont connectées électriquement par une interconnexion conductrice (290).

4. Réseau de cellules de pixel selon la revendication 3, dans lequel l'interconnexion conductrice (290) comprend un conducteur enterré.

5. Réseau de cellules de pixel selon la revendication 3, dans lequel l'interconnexion conductrice comprend une couche de câblage de métallisation.

6. Réseau de cellules de pixel selon l'une des revendications précédentes, dans lequel une région d'isolation par tranchée peu profonde (320) est formée entre les première et seconde cellules de pixel (211, 212) pour isoler des zones autres que les zones actives d'accumulation de charges.

7. Système de traitement (508) comprenant :

un processeur (502) ; et
un dispositif d'imagerie (500) couplé électriquement audit processeur, ledit dispositif d'imagerie comprenant le réseau de cellules de pixel selon l'une des revendications précédentes.

8. Procédé de formation d'un réseau de cellules de pixel selon l'une des revendications 1 à 6 ayant une première cellule de pixel et une seconde cellule de pixel adjacente à la première cellule de pixel, le procédé comprenant les étapes consistant à :

former un photodétecteur (313) dans une couche de matériau (300) d'un premier type de conductivité (p), le photodétecteur incluant une zone active d'accumulation de charges (313) dopée à un second type de conductivité (n) opposé au premier type de conductivité (p) et une première couche de surface dopée (323) dopée au premier type de conductivité (p), la première couche de surface dopée étant située au-dessus de la zone active d'accumulation de charges ;
effectuer de premières implantations ioniques pour former une pluralité de premières régions d'implantation (250) dopées au premier type de conductivité (p) et à une première concentration, les premières régions d'implantation (250) étant adjacentes à un premier côté de la zone active d'accumulation de charges ; et
effectuer une seconde implantation ionique au-dessus des premières régions d'implantation (250) et juste au-dessous de la surface de la couche de matériau (300) pour former une seconde couche de surface dopée (251), la seconde implantation ionique étant dopée au premier type de conductivité (p) et à une seconde concentration qui est supérieure à la première concentration,
dans lequel les premières régions d'implantation (250) sont formées en tant que régions de

puits p dopées aux ions et la seconde couche de surface dopée (251) est formée en tant que couche de surface dopée p+ au-dessus des premières régions d'implantation (250).

9. Procédé selon la revendication 8, dans lequel les transistors de transfert et la région de diffusion flottante partagée (210) font partie d'une première région active (227) des cellules de pixel et dans lequel une seconde région active (228) des cellules de pixel, séparée physiquement de la première région active mais connectée électriquement à celle-ci, comprend au moins un transistor suiveur de source (207) pour générer un signal à partir des cellules de pixel.

10. Procédé selon la revendication 8 ou 9, dans lequel l'acte consistant à former la première couche de surface dopée (324) consiste à effectuer un dépôt à blanc d'ions bore au-dessus de la seconde couche de surface dopée (251) et de la zone active d'accumulation de charges (314).

11. Procédé selon la revendication 9, comprenant en outre l'étape consistant à former une zone d'isolation par tranchée peu profonde (320) entre les première et seconde cellules de pixel (211, 212) pour isoler des zones autres que les zones d'accumulation de charges.

12. Dispositif imageur comprenant :
le réseau de cellules de pixel selon l'une des revendications 1 à 6 et comprenant en outre une pluralité de cellules de pixel en rangées et colonnes, et dans lequel les cellules de pixel adjacentes sont formées dans un substrat.

13. Dispositif imageur selon la revendication 12, dans lequel l'imageur est un imageur CMOS et les cellules de pixel sont des pixels CMOS.

14. Dispositif imageur selon la revendication 12, comprenant en outre une seconde paire de cellules de pixel adjacentes, dans lequel la région d'isolation est formée dans une zone comprise entre au moins une partie de chacune des première et seconde paires de cellules de pixel adjacentes.

15. Dispositif imageur selon la revendication 14, dans lequel les première et seconde paires de cellules de pixel incluent des cellules de pixel adjacentes dans une colonne.

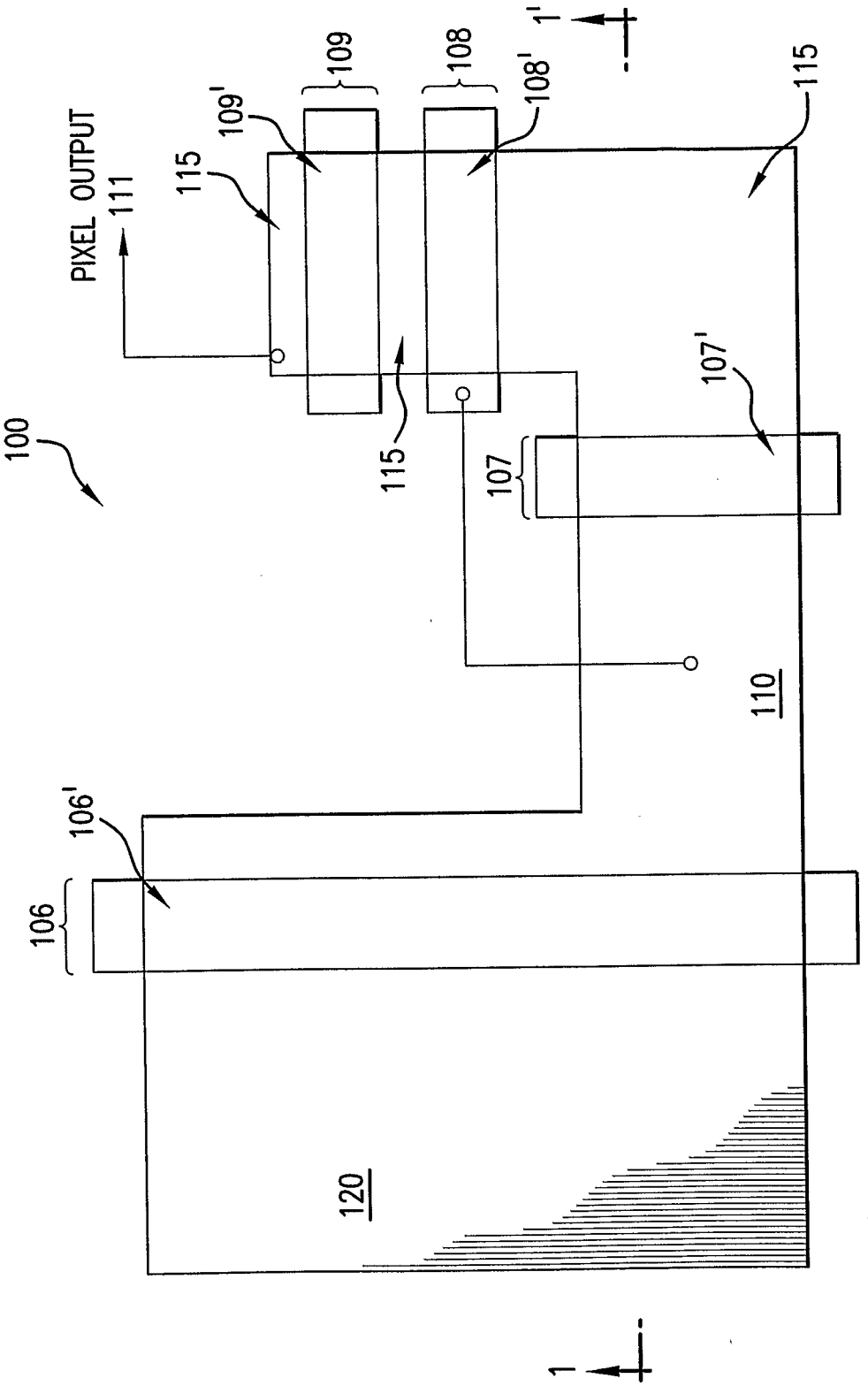

FIG. 1
(PRIOR ART)

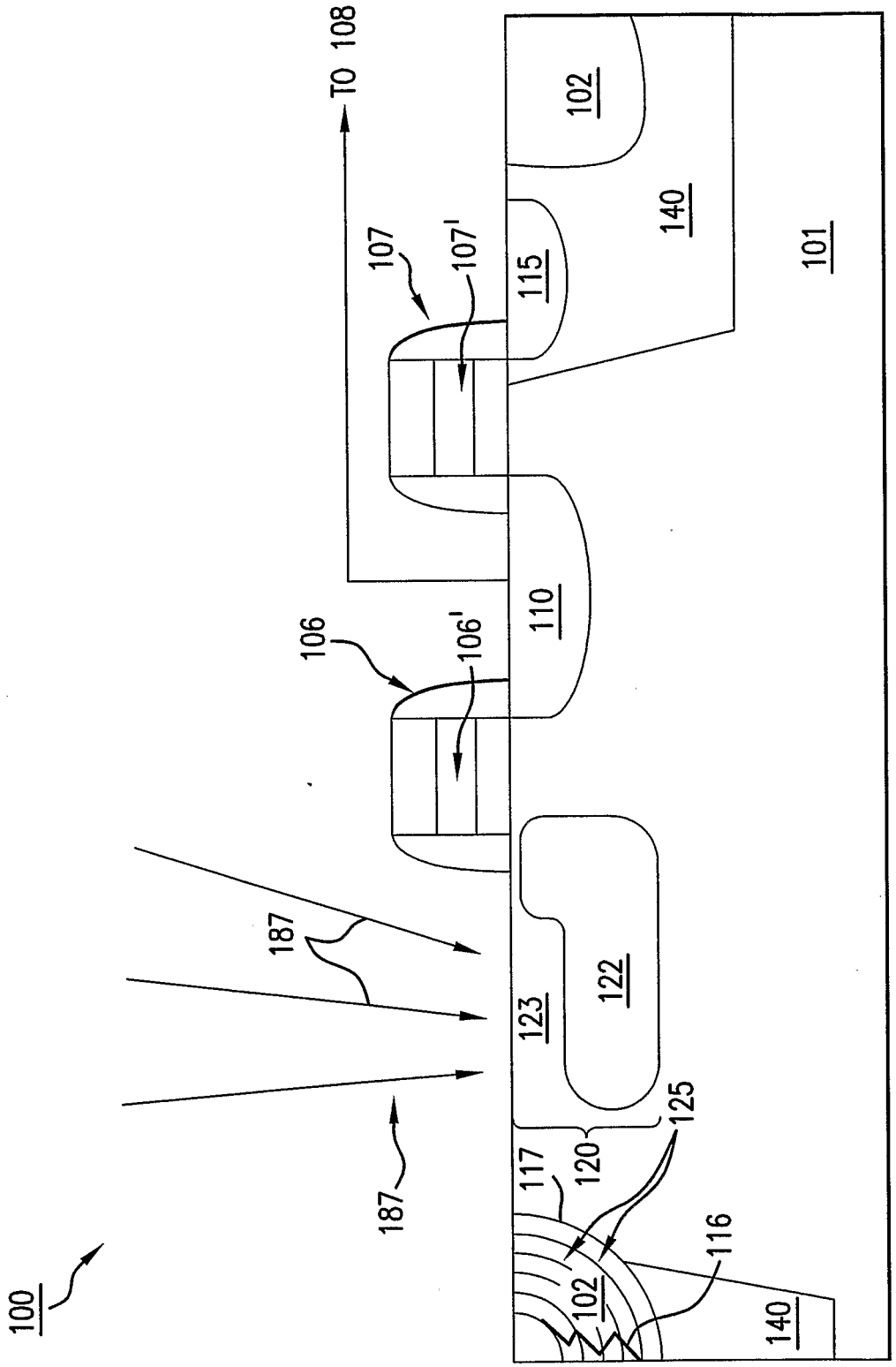

FIG.2
(PRIOR ART)

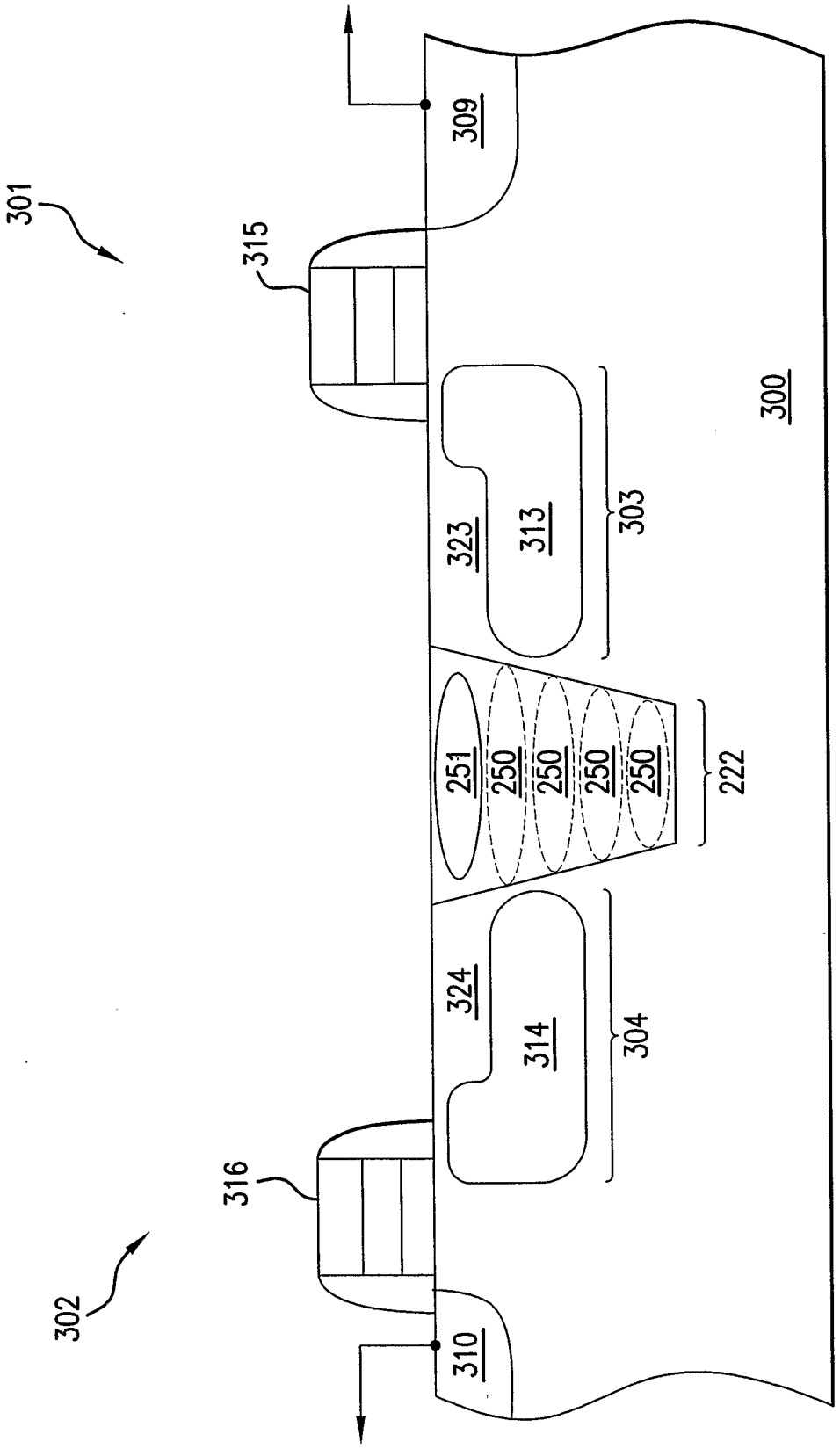
301
315
309
300
323
313
303
251
250
250
250
250
222
324
314
304
316
302
310

FIG.3

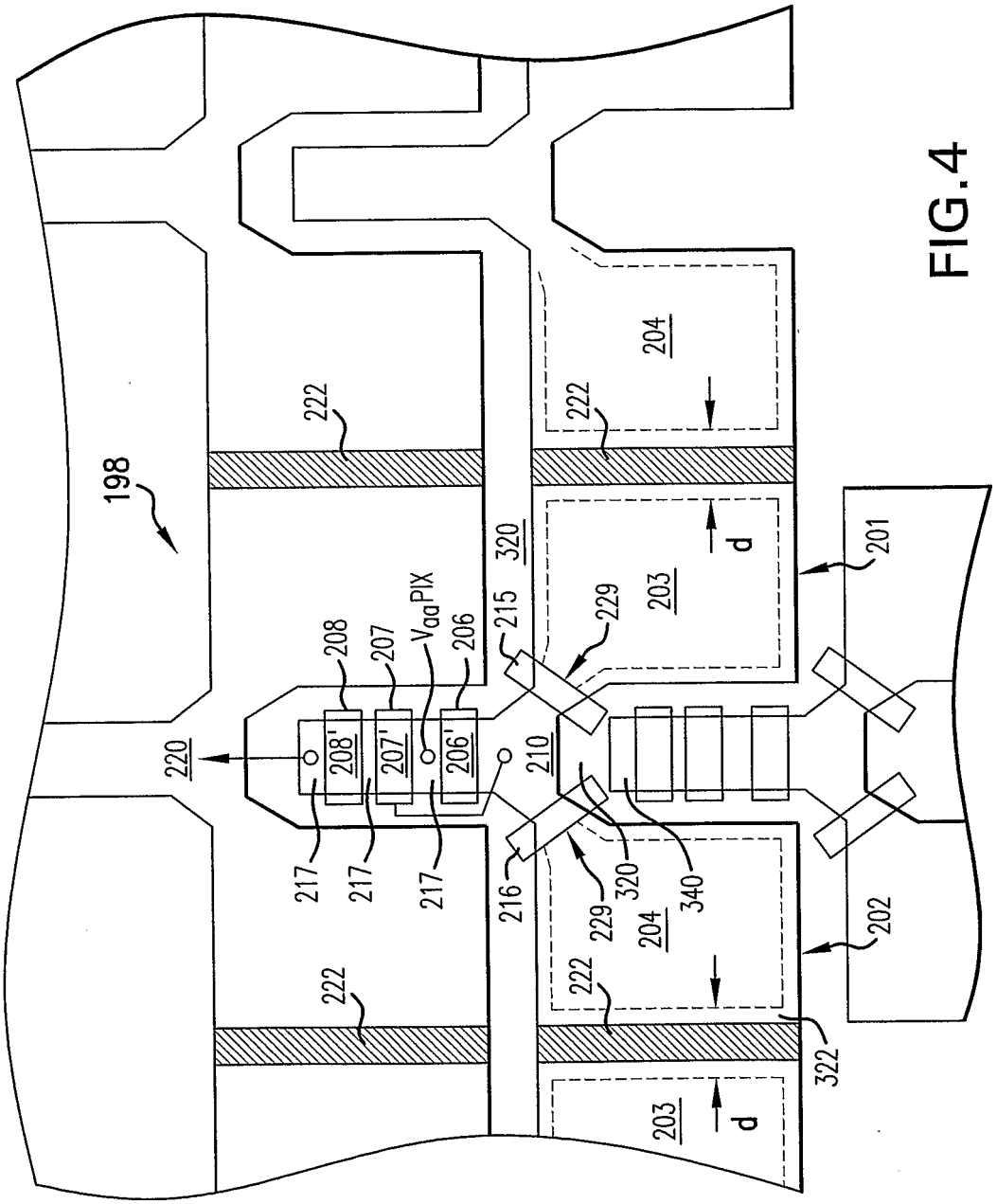
198
222
222
204
320
215
229
203
d
201
208
207
V_{aa}PIX
206
220
208'
207'
206'
210
217
217
217
216
229
320
340
204
202
222
222
322
203
d

FIG.4

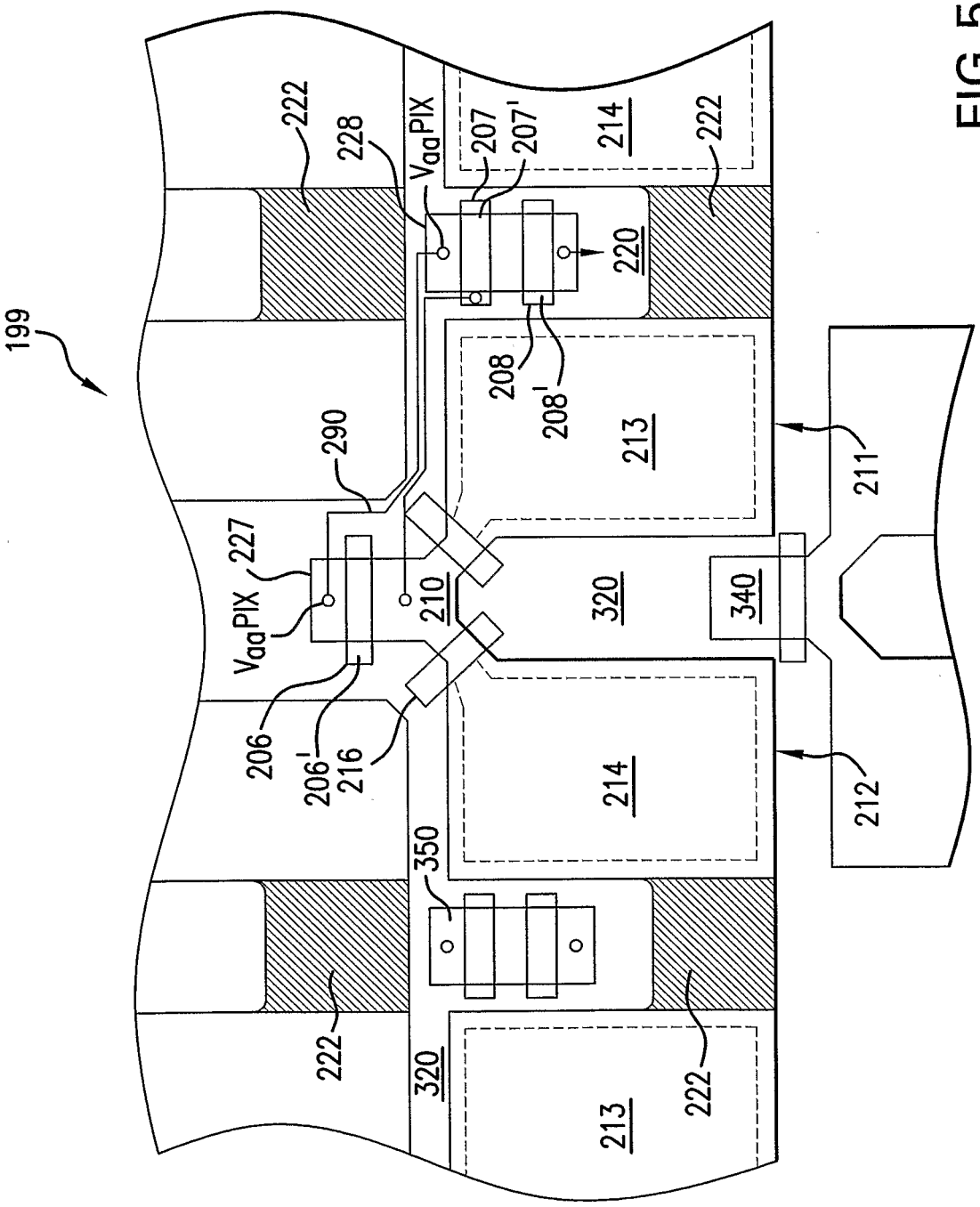
199
222
228
$V_{aa}PIX$
207
207'
214
222
220
208
208'
213
290
211
227
$V_{aa}PIX$
210
320
340
206
206'
216
214
212
350
222
320
213
222

FIG.5

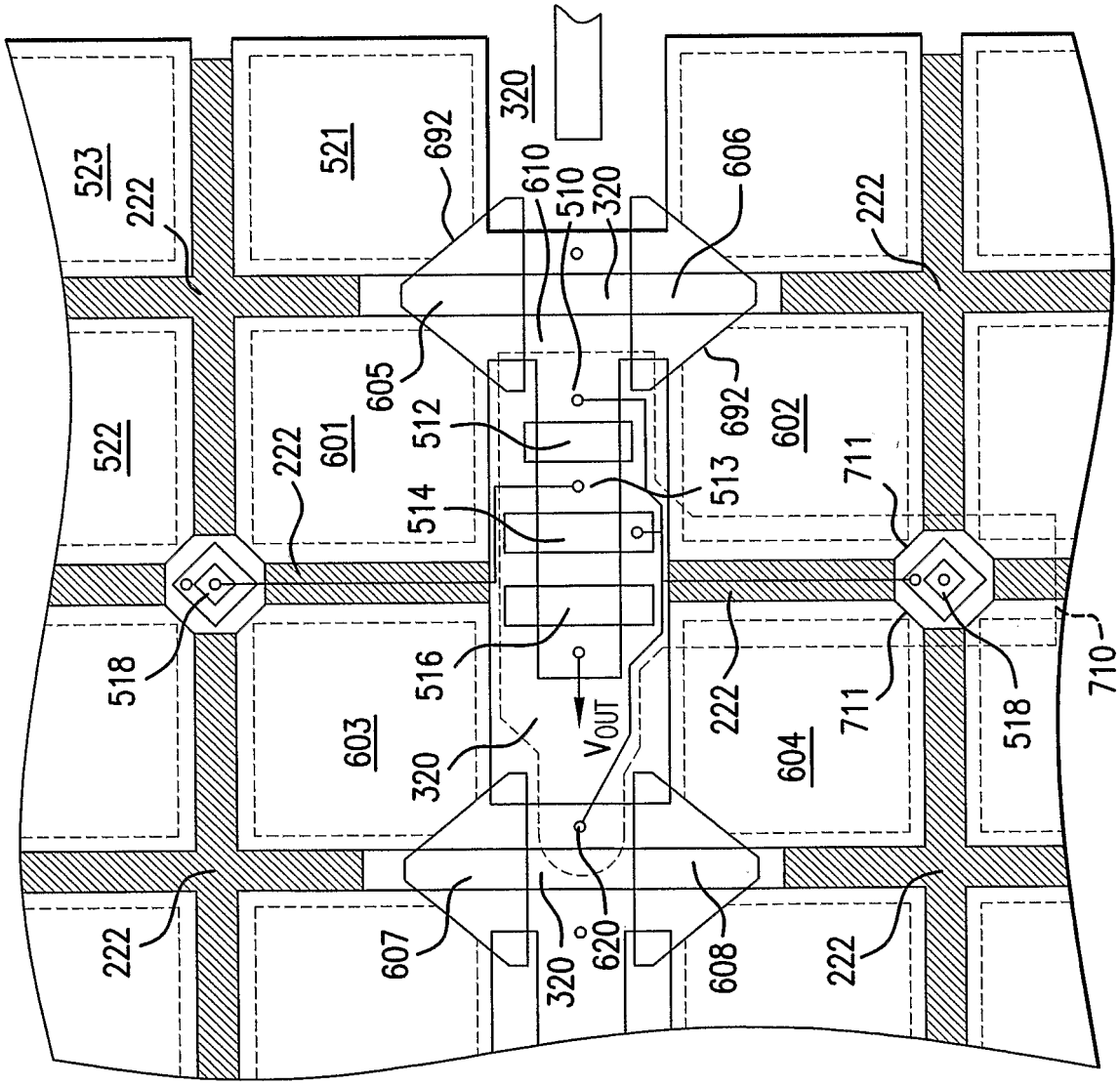
550
523
222
521
692
320
610
510
320
606
222
605
522
222
601
512
692
602
513
711
514
518
516
603
320
V_{OUT}
222
604
711
518
710
222
607
320
620
608
222

FIG.6

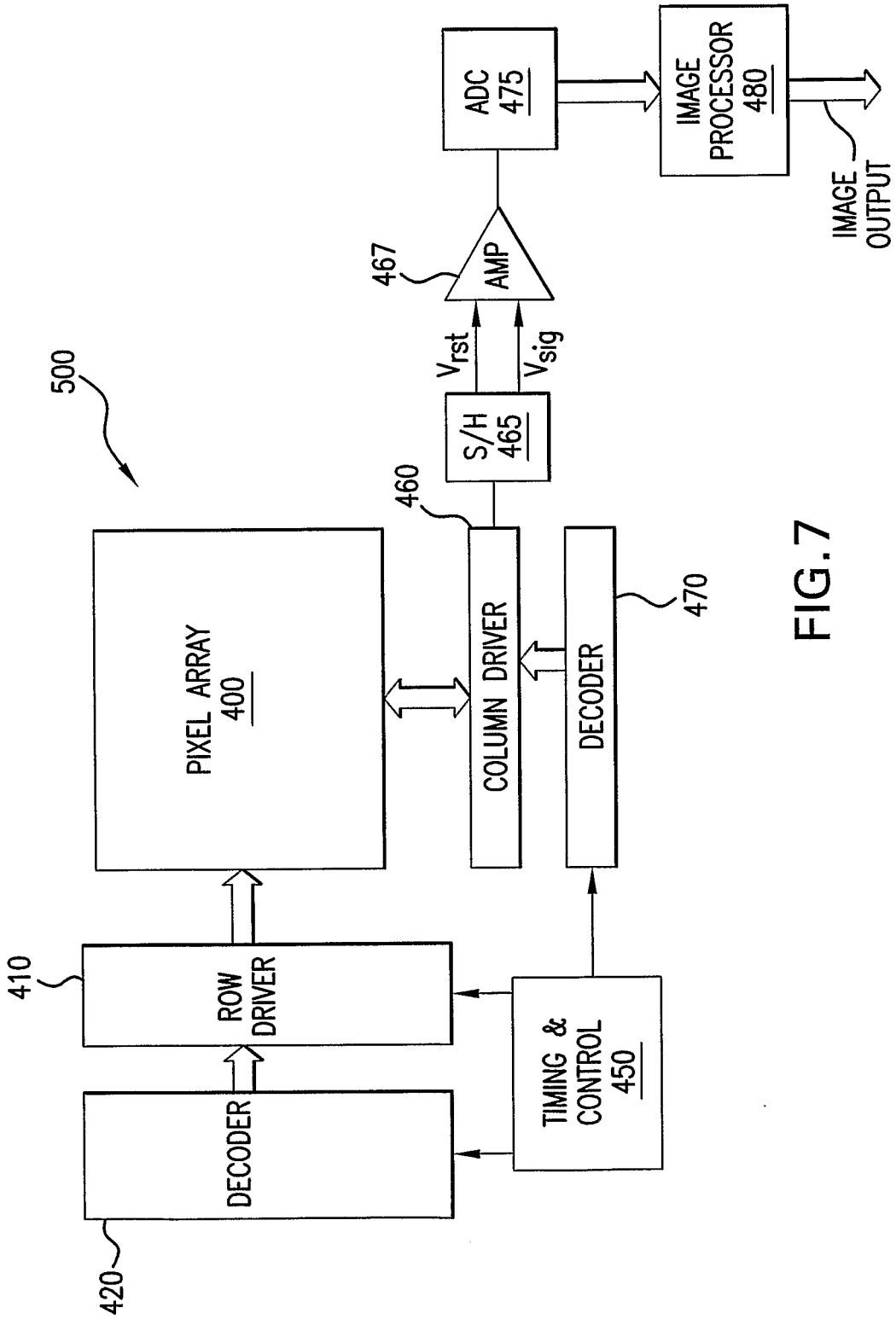
500
PIXEL ARRAY
400
410
ROW
DRIVER
DECODER
420
460
COLUMN DRIVER
DECODER
470
S/H
465
V_{rst}
V_{sig}
467
AMP
ADC
475
IMAGE
PROCESSOR
480
IMAGE
OUTPUT
TIMING &
CONTROL
450

FIG. 7

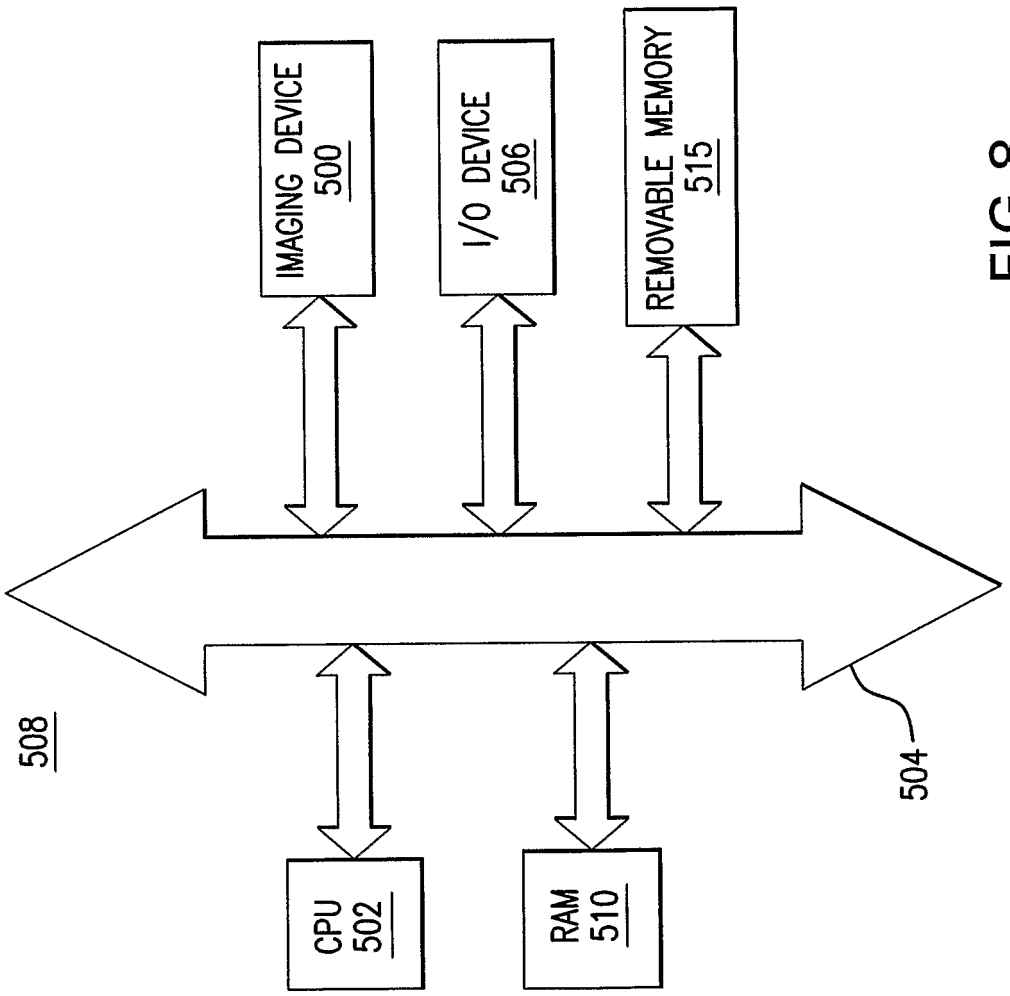
IMAGING DEVICE
500
I/O DEVICE
506
REMOVABLE MEMORY
515
508
504
CPU
502
RAM
510

FIG.8

REFERENCES CITED IN THE DESCRIPTION

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