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(54) **WAFER LEVEL CHIP SCALE PACKAGE STRUCTURE**

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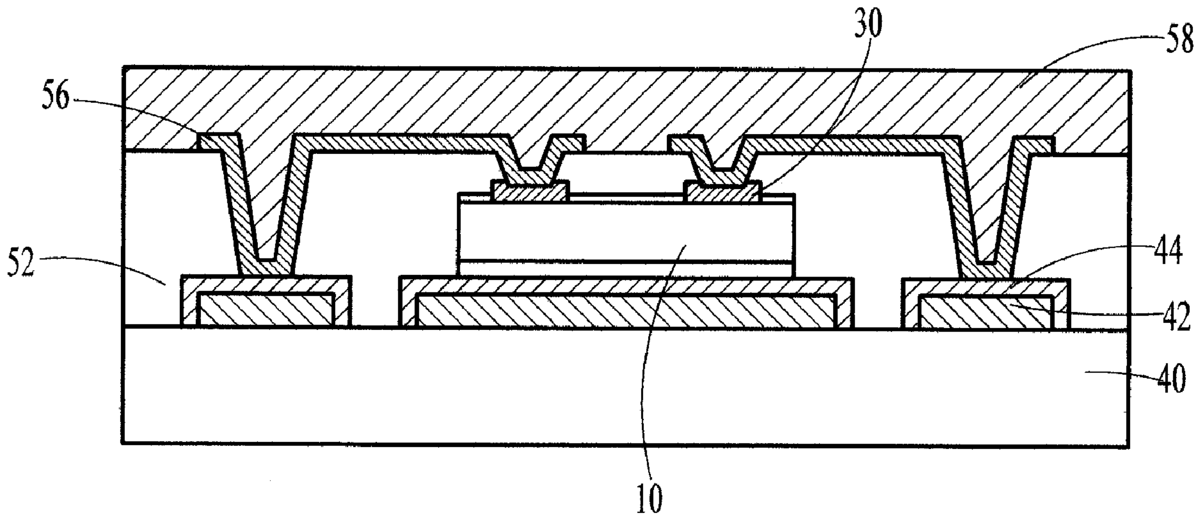
(57) **ABSTRACT**

At least one redistribution layer (RDL) is provided on a silicon die. A passivation layer is deposited on the RDL. First openings having a first diameter are etched in the passivation layer where copper posts are to be formed. A seed layer is deposited over the passivation layer and within the openings. A photoresist layer is coated on the seed layer and patterned to form second openings having a second diameter over the first openings larger than the first diameter. Copper is plated on the seed layer to form copper posts filling the second openings. The silicon die is die attached to a metal substrate. A lamination layer is coated over the silicon die and the copper posts. Third openings are formed through the lamination layer to the copper posts and to metal pads on the metal substrate. Metal vias are formed in the third openings.



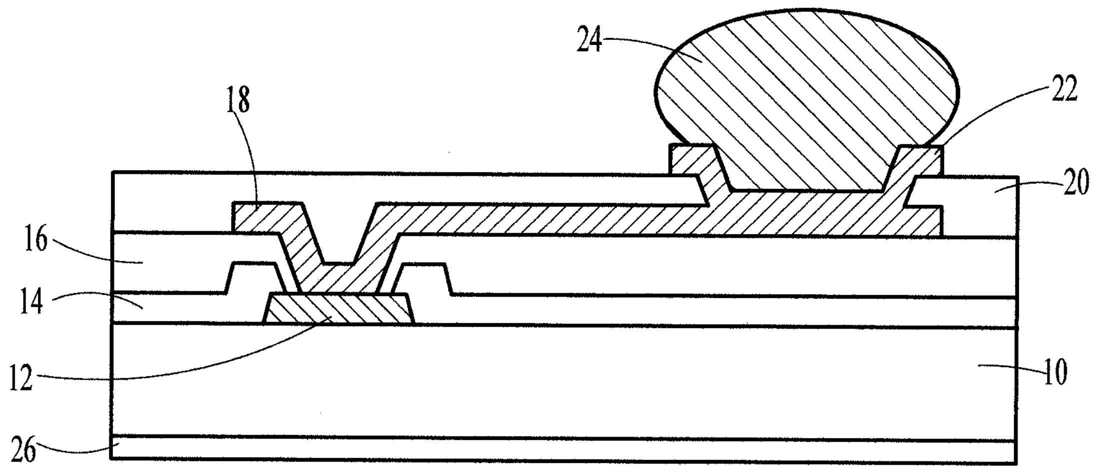


Figure 1 Prior Art

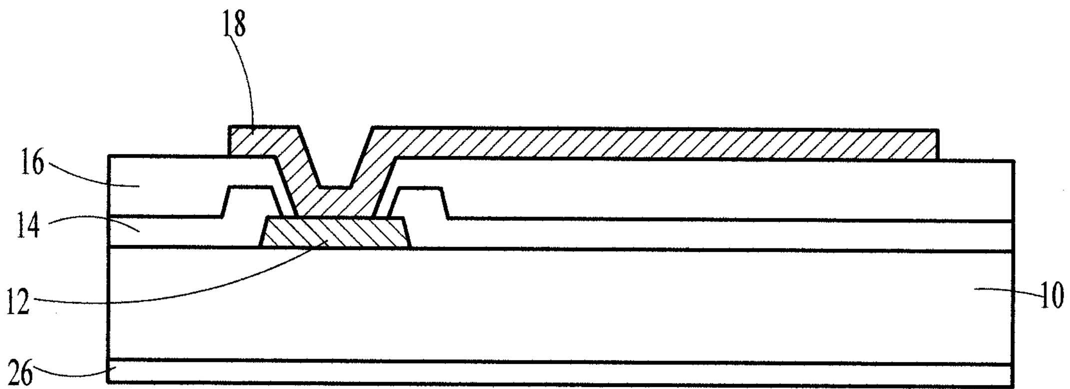


Figure 2

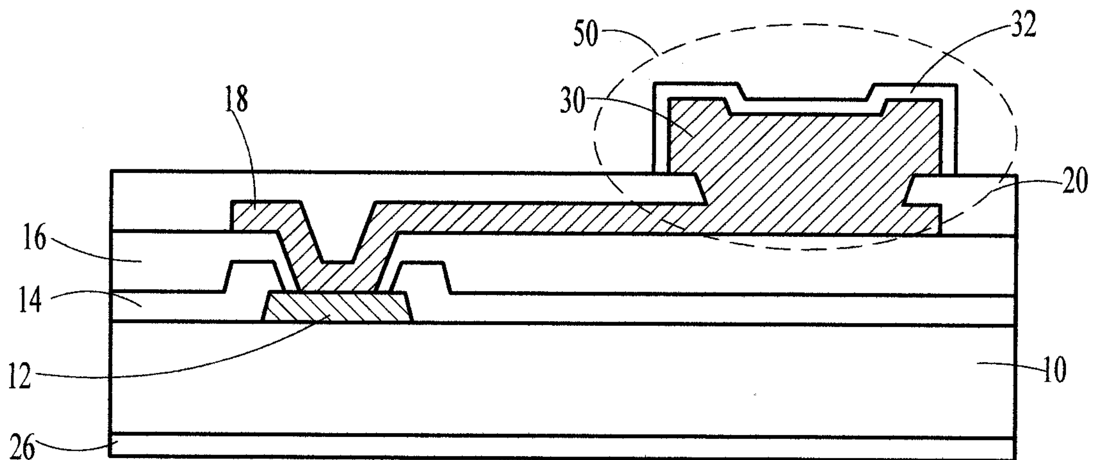


Figure 3

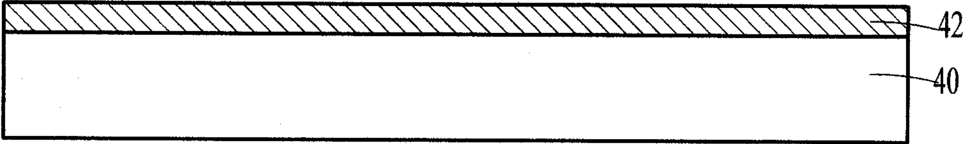


Figure 4

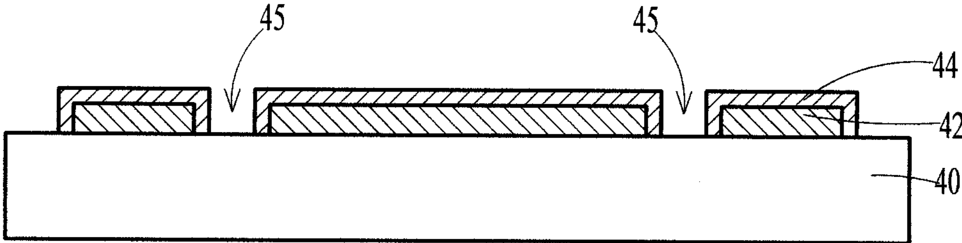


Figure 5

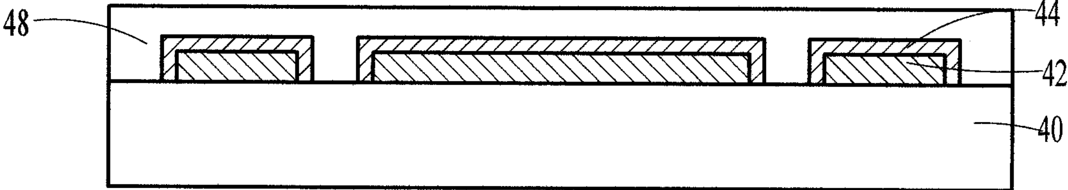


Figure 6

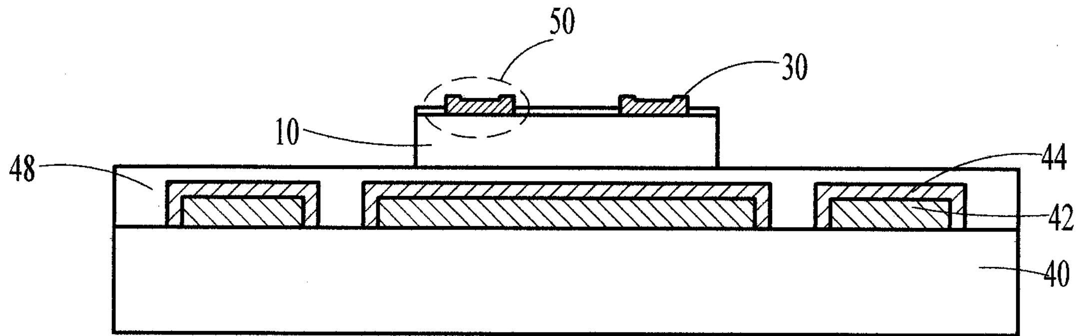


Figure 7

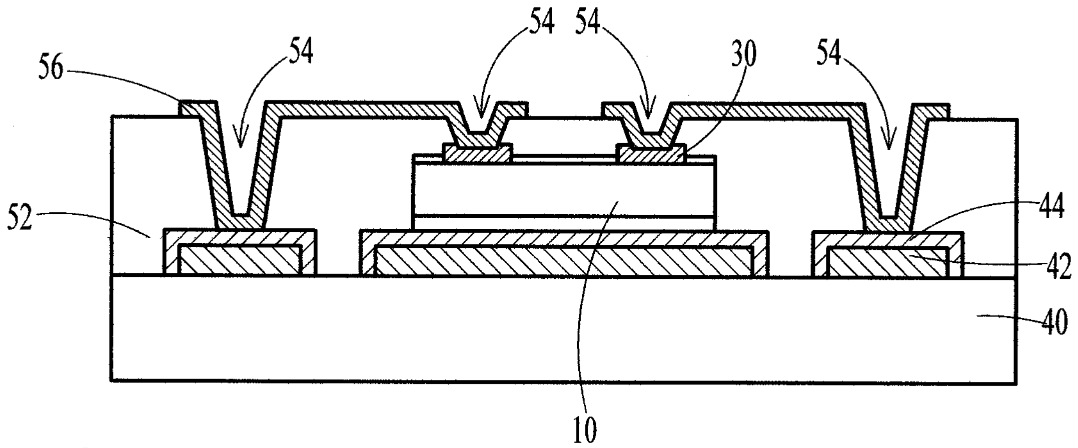


Figure 8

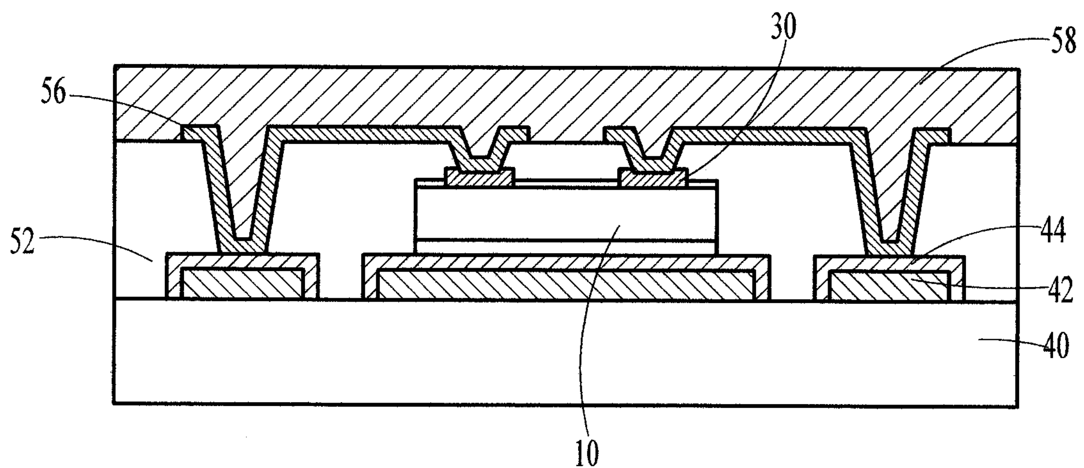


Figure 9

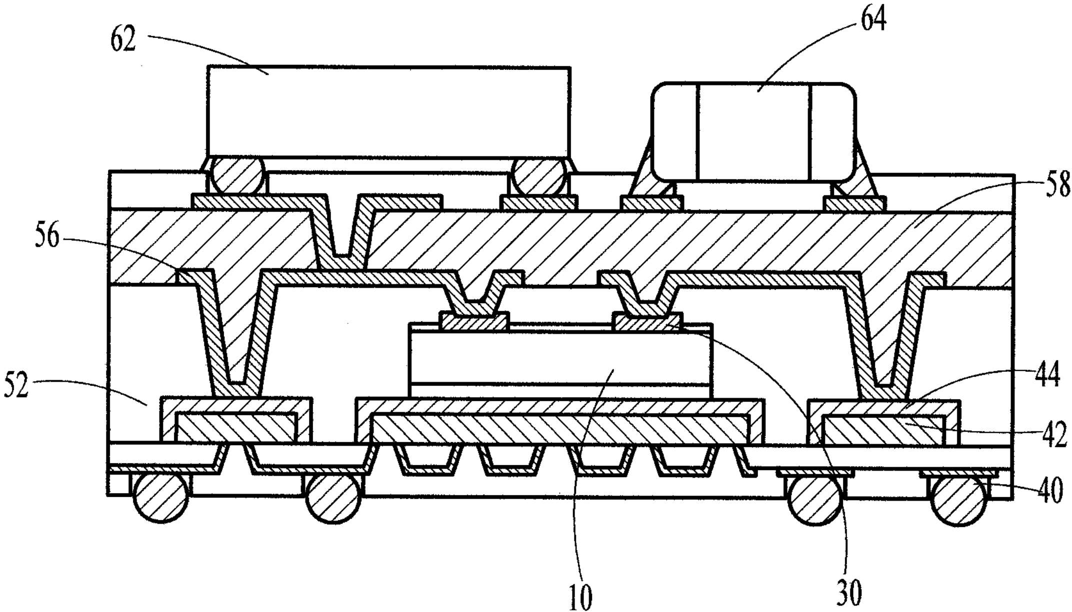


Figure 10

WAFER LEVEL CHIP SCALE PACKAGE STRUCTURE

TECHNICAL FIELD

[0001] This disclosure is related to wafer packaging technologies, and more particularly, to improved wafer level chip scale packaging.

BACKGROUND

[0002] The IOT (internet of things) is the new reality and the connection of billions of mobile devices to the cloud with infinite data sharing possibilities can be expected in the future. Each of these devices will require, at a minimum, a microcontroller to add intelligence to the device, one or more sensors to allow for data collection, one or more chips to allow for connectivity and data transmission, and a memory component. Semiconductor device manufacturers are constantly confronted with device integration challenges as consumers want electronics to be smaller, more portable, and more multi-functional than ever.

[0003] The current WLCSP (Wafer Level Chip Scale Package) structure cannot be directly embedded into a substrate without removing solder balls because solder material will melt after reflow and further cause reliability issues. It is desired to embed a WLCSP into a substrate and to replace solder balls with copper posts.

[0004] U.S. Pat. No. 9,520,342 (Michael et al), U.S. Pat. No. 9,312,198 (Meyer et al), U.S. Pat. No. 8,686,556 (Clark et al), and U.S. Pat. No. 9,559,029 (Shim et al) show various types of packages. All of these references are different from the present disclosure.

SUMMARY

[0005] It is the primary objective of the present disclosure to provide a wafer level chip scale package embedded in a substrate.

[0006] It is another objective of the disclosure to provide an improved wafer level chip scale package having copper post instead of solder ball interconnections and being embedded in a substrate.

[0007] It is a further objective of the disclosure to provide a process for fabricating a wafer level chip scale package having copper post instead of solder ball interconnections and being embedded in a substrate.

[0008] Yet another objective is to provide a process for fabricating a wafer level chip scale package embedded in a substrate having high current carrying capacity and electromagnetic shielding.

[0009] In accordance with the objectives of the present disclosure, a wafer level chip scale package is achieved comprising a silicon die on a metal substrate and metal vias through a lamination layer over the silicon die, the metal vias providing connections to at least one copper post on the silicon die and to at least one metal pad on the metal substrate.

[0010] Also in accordance with the objectives of the present disclosure, a method of fabricating a wafer level chip scale package is achieved. At least one redistribution layer (RDL) is provided on a silicon die. A passivation layer is deposited on the RDL. First openings having a first diameter are etched in the passivation layer where copper posts are to be formed. A seed layer is deposited over the passivation layer and within the openings. A photoresist layer is coated on the seed layer and patterned to form second openings having a second diameter over the first openings wherein the second diameter is larger than the first diameter. Copper is plated on the seed layer in the first and second openings to form copper posts filling the second openings. The silicon die is die attached to a metal substrate. A lamination layer is coated over the silicon die and the copper posts. Third openings are formed through the lamination layer to the copper posts and to metal pads on the metal substrate. Metal vias are formed in the third openings. The metal vias are covered with a solder mask to complete the wafer level chip scale package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] In the accompanying drawings forming a material part of this description, there is shown:

[0012] FIG. **1** is a cross-sectional representation of a silicon die of the prior art.

[0013] FIGS. **2-3** are cross-sectional representations of a silicon die of the present disclosure.

[0014] FIGS. **4-9** are cross-sectional representations of a wafer level chip scale package of the present disclosure.

[0015] FIG. **10** is a cross-sectional representation of one example of a completed wafer level chip scale package of the present disclosure.

DETAILED DESCRIPTION

[0016] The present disclosure describes a structure and a process in which a wafer level chip scale package (WLCSP) can be embedded into a substrate having high current carrying capacity. Other chips and passive components are further integrated in the same substrate. Only copper (Cu) posts are required in this structure to connect the circuit embedded in the substrate, rather than solder balls that are used in the prior art. The Cu post thickness can be adjusted through an electroplating process from about 1 μm to 20 μm based on the substrate lamination material thickness and required electrical performance.

[0017] The process of the present disclosure will provide higher electrical performance. Other advantages of the WLCSP of the present disclosure include:

[0018] 1. Enabling the current WLCSP structure to be embedded into a substrate with high current carrying capability.

[0019] 2. Better heat dissipation in the substrate structure.

[0020] 3. No solder balls exist in this structure, thus minor cost savings can be expected.

[0021] FIG. **1** illustrates a traditional WLCSP in the production stage. An opening is made to the aluminum pad **12** on the die **10** through the die passivation layer **14**. First dielectric layer **16** is deposited, then patterned to provide an opening for the RDL layer **18**. Second dielectric layer **20** is deposited over the patterned RDL. Dielectric layer **20** is patterned to form an opening for the UBM **22** which is also patterned. Solder ball **24** is placed onto the UBM. Backside film **26** protects the silicon die **10** from chipping.

[0022] Referring now to FIGS. **2-8**, the process of fabricating a WLCSP of the present disclosure will be described in detail. As illustrated in FIG. **2**, the package of the present disclosure is fabricated similarly to the traditional package. An opening is made to the aluminum pad **12** on the die **10** through the die passivation layer **14**. First dielectric layer **16** is deposited, then patterned to provide an opening for the

RDL layer **18**. RDL layer **18** is plated to the desired thickness and patterned as shown in FIG. **2**.

[0023] Referring now to FIG. **3**, a second dielectric layer **20** is deposited over the patterned RDL layer **18**. Preferably the second dielectric layer **20** is a passivation material such as polybenzoxazole (PBO) or polyimide (PI). The passivation layer is patterned using a photolithography process to provide openings where copper posts will be formed. Copper (Cu) posts **30** are formed on the RDL layer **18**. A seed layer, not shown, is deposited over the passivation layer **20** and patterned RDL layer **18** by a physical vapor deposition (PVD) process, such as evaporation or a sputtering process under vacuum conditions, or a chemical vapor deposition (CVD) process, such as metal-organic CVD (MOCVD) or metal-organic Vapor-Phase Epitaxy (MOVPE). Preferably, the seed layer will be titanium or copper.

[0024] A photoresist mask is formed with openings where copper posts are to be placed and to define the Cu post diameter size which is larger than the passivation layer **20** opening size. Copper posts **30** are plated onto the seed layer in the openings to the desired Cu post height. The Cu post thickness can be from about 1 μm to 20 μm based on the substrate lamination material thickness and required electrical performance. The photoresist material and the seed layer not covered by the copper posts are chemically removed.

[0025] After Cu post preparation, an extra organic solderability preservative (OSP) material **32** can be prepared to further protect the Cu posts from oxidation. Later, this OSP material **32** will be removed by physical plasma or chemical etching before the via plating process. After the OSP process, the wafer can be further thinned down to the desired thickness, tested, have its backside ground, and singulated into package form.

[0026] Next, a substrate is prepared. FIG. **4** illustrates a resin coated copper (RCC) substrate. Solder mask material **40** is shown coated with a copper layer **42**. Referring now to FIG. **5**, alignment patterns **45** for the die attach process will be defined by a photolithography process and generated by a further developing and etching process in the copper side of the RCC. An extra metal plating **44** may be made on the copper layer **42** after the alignment patterns **45** have been generated. The extra metal plating **44** may also be copper or a nickel-plated material. It will be added in case the coated copper **42** from the RCC substrate is not thick enough for the high current application required for the semiconductor die **10**. The copper layer **42** is preferably 5-10 μm thick. The copper substrate provides electromagnetic shielding capability as well as high current carrying capacity.

[0027] The die bonder can identify the alignment patterns **45** on the substrate side and the die side to do the die attachment process. An extra lamination layer **48** can be deposited or laminated over the RCC substrate **40**, as shown in FIG. **6**, as a stop layer to stop copper from layers **42/44** from penetrating into the die substrate **10**. The layer **48** may be Ajinomoto Build-up Film (ABF) or pre-impregnated composite fiber (PP) materials, for example. Preferably, the layer **48** may have a thickness of between about 5-30 μm.

[0028] Now, as illustrated in FIG. **7**, the die **10** of FIG. **3** is attached to the top layer of the substrate **40** by a die attach process. Copper post **30** is shown in the circle **50** in both FIGS. **3** and **7**.

[0029] One example of further manufacturing flow is shown in FIGS. **8** and **9**. Lamination material **52** is coated over the substrate and the die, as shown in FIG. **8**. The lamination material **52** may be ABF, PP, or a thick resin as in the RCC substrate. The lamination material may be 50-250 μm in thickness. The Cu posts **30** are covered by the lamination material. Now, openings are to be made through the lamination material to the Cu posts **30** and to copper pads **42** on the substrate outside of the die **10**.

[0030] Laser drilling is preferred to create via openings **54** through the lamination layer **52**. A certain laser type can be selected which will not damage the copper surface or generate too much heat. Laser drilling is more cost effective in this process than a photolithography process and provides high accuracy, high etch rate, and high anisotropy. A photoresist material rather than the lamination material can be considered, but the overall cost to prepare the substrate will be higher. Thinner lamination material might be 30-50 μm in thickness, and it depends on the final thickness requirement. The second passivation layer **20** helps avoid damage from laser drilling.

[0031] After the laser drilling process, the OSP **32** layer covering the copper posts (shown in FIG. **3**) needs to be removed within the laser drilled via openings. This is done by a physical plasma, chemical etching, or reflow process. Next, copper plating **56** is performed within the via openings to form connections as desired in the package and as shown in FIGS. **8** and **9**. Finally, a solder mask **58** is laminated over the copper connections to complete the WLCSP, as shown in FIG. **9**. FIG. **10** shows an option where other chips and passive devices **62** and **64** are connected to the WLCSP.

[0032] Compared with the traditional WLCSP structures, the WLSCP structures of the present disclosure have no solder balls placed onto the Cu post structure. If solder balls were placed onto the Cu posts, this would increase the height and difficulty to force the lamination material **50** to fill in underneath the solder balls. Normally solder is used for interconnection with a substrate, but this is not necessary for the die embedded in the substrate in the present disclosure.

[0033] Furthermore, the process of the present disclosure does not require a backside lamination film on the silicon die back side. The purpose of a backside lamination film is to protect the silicon backside from chipping and light radiation. However, as seen in FIG. **9**, the backside of the die is embedded into the substrate material which will further protect it. The absence of the backside lamination film also saves cost.

[0034] The Cu posts on the die may have a height of between 1 and 20 μm, and optionally up to 100 μm. If the Cu post thickness is too thin, the RDL Cu pad might be damaged by the laser via opening process after the die attach which may impact electrical performance of the package. If the Cu post thickness is too thick, a thicker lamination material will be required and voids might form in the thick lamination layer.

[0035] The WLCSP of the present disclosure comprises a silicon die embedded in a substrate having high current carrying capacity and electromagnetic shielding. The die on the substrate is laminated and laser drilled via openings are made to copper posts on the die and metal pads on the substrate for further interconnection.

[0036] Although the preferred embodiment of the present disclosure has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the disclosure or from the scope of the appended claims.

What is claimed is:

1. A wafer level chip scale package comprising:
a silicon die, comprising:
at least one redistribution layer (RDL) on an upper surface of said silicon die;
a passivation layer on said RDL; and
at least one copper post contacting said at least one RDL through an opening in said passivation layer wherein said at least one copper post is wider than said opening;
wherein said silicon die is attached on top of a metal substrate comprising:
a resin coated copper;
a copper or nickel-plated layer on said resin coated copper; and
a stopper layer on said copper or nickel-plated layer comprising Ajinomoto Build-up Film (ABF) or pre-impregnated composite fiber (PP) materials; and
metal vias through a lamination layer over said silicon die and said metal substrate, said metal vias providing connections to said at least one copper post on said silicon die and to at least one metal pad on said metal substrate.

2-4. (canceled)

5. The package according to claim **1** wherein said lamination layer comprises Ajinomoto Build-up Film (ABF), pre-impregnated composite fiber (PP) materials, or resin.

6. The package according to claim **1** further comprising a solder mask over said metal vias.

7. A method of fabricating a wafer level chip scale package comprising:
providing at least one redistribution layer (RDL) on a silicon die;
depositing a passivation layer on said RDL;
etching first openings having a first diameter in said passivation layer where copper posts are to be formed;
depositing a seed layer over said passivation layer and within said openings;
coating a photoresist layer on said seed layer and patterning said photoresist layer to form second openings having a second diameter over said first openings wherein said second diameter is larger than said first diameter;
plating copper on said seed layer in said first and second openings to form said copper posts filling said second openings;
thereafter die attaching said silicon die to a metal substrate;
coating a lamination layer over said metal substrate, said silicon die, and said copper posts;
forming third openings through said lamination layer to said copper posts and to metal pads on said metal substrate;
forming metal vias in said third openings; and
covering said metal vias with a solder mask to complete said wafer level chip scale package.

8. The method according to claim **7** wherein said passivation layer comprises polybenzoxazole (PBO) or polyimide (PI).

9. The method according to claim **7** wherein said copper posts have a thickness of between about 1 μm and 100 μm, and preferably about 1 μm and 20 μm.

10. The method according to claim **7** further comprising:
depositing an organic solderability preservative (OSP) layer onto said copper posts prior to said die attaching step; and
removing said OSP layer in said third openings prior to forming said metal vias.

11. The method according to claim **7** wherein said metal substrate comprises:
a resin coated copper;
a copper or nickel-plated layer deposited on said resin coated copper; and
a stopper layer on said copper or nickel-plated layer comprising Ajinomoto Build-up Film (ABF) or pre-impregnated composite fiber (PP) materials.

12. The method according to claim **7** wherein said lamination layer comprises Ajinomoto Build-up Film (ABF), pre-impregnated composite fiber (PP) materials, or resin.

13. A method of fabricating a wafer level chip scale package comprising:
providing at least one redistribution layer (RDL) on a silicon die;
depositing a passivation layer on said RDL;
etching first openings having a first diameter in said passivation layer where copper posts are to be formed;
depositing a seed layer over said passivation layer and within said openings;
coating a photoresist layer on said seed layer and patterning said photoresist layer to form second openings having a second diameter over said first openings wherein said second diameter is larger than said first diameter;
plating copper on said seed layer in said first and second openings to form said copper posts filling said second openings;
providing a metal substrate comprising:
coating a resin on a copper substrate forming a resin-coated copper substrate;
depositing a copper or nickel-plated layer on said resin coated copper; and
forming a stopper layer on said copper or nickel-plated layer comprising
Ajinomoto Build-up Film (ABF) or pre-impregnated composite fiber (PP) materials;
thereafter die attaching said silicon die to said metal substrate;
coating a lamination layer over said metal substrate, said silicon die, and said copper posts;
forming third openings through said lamination layer to said copper posts and to metal pads on said metal substrate;
forming metal vias in said third openings; and
covering said metal vias with a solder mask to complete said wafer level chip scale package.

14. The method according to claim **13** wherein said passivation layer comprises polybenzoxazole (PBO) or polyimide (PI).

15. The method according to claim **13** wherein said copper posts have a thickness of between about 1 μm and 100 μm, and preferably about 1 μm and 20 μm .

16. The method according to claim **13** further comprising:
depositing an organic solderability preservative (OSP) layer onto said copper posts prior to said die attaching step; and

removing said OSP layer in said third openings prior to forming said metal vias.

17. The method according to claim **13** wherein said lamination layer comprises Ajinomoto Build-up Film (ABF), pre-impregnated composite fiber (PP) materials, or resin.

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