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(54) **Title:** ENHANCEMENT MODE III-NITRIDE SEMICONDUCTOR DEVICE WITH REDUCED ELECTRIC FIELD BETWEEN THE GATE AND THE DRAIN

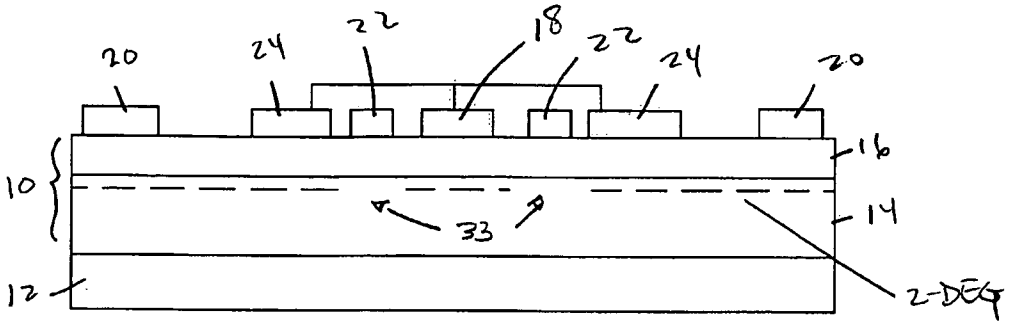

FIG. 1

(57) **Abstract:** An enhancement mode III-nitride heterojunction device that includes a region between the gate and the drain electrode thereof that is at the same potential as the source electrode thereof when the device is operating.

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ENHANCEMENT MODE III-NITRIDE SEMICONDUCTOR DEVICE WITH REDUCED ELECTRIC FIELD BETWEEN THE GATE AND THE DRAIN

RELATED APPLICATION

[0001] This application is based on and claims priority to United States Provisional Application Serial No. 60/973,935, filed on September 20, 2007, entitled Enhancement Mode III-Nitride Semiconductor Device with Reduced Electric Field Between the Gate and the Drain, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

FIELD OF INVENTION

[0002] The present application relates to semiconductor devices and methods of fabrication of semiconductor devices.

DEFINITION

[0003] As referred to herein III-nitride refers to a semiconductor alloy from the InAlGaN system, including, but not limited to, GaN, AlGaN, AlN, InGaN, InAlGaN, and the like.

BACKGROUND AND SUMMARY OF THE INVENTION

[0004] Depletion mode devices are normally ON, while enhancement mode devices are normally OFF. Depletion mode III-nitride heterojunction power semiconductor devices such as III-nitride high electron mobility transistors (HEMTs) are well known.

[0005] For various reasons, e.g. efficiency and simplicity of operation, enhancement mode III-nitride power semiconductor devices are desirable. To obtain an enhancement mode III-nitride heterojunction type power semiconductor device, the carrier-rich region (referred to as the two-dimensional electron gas or 2-DEG) under the gate must be interrupted, whereby the device is rendered normally OFF when no voltage is applied to the gate electrode.

[0006] In Control of Threshold Voltage of AlGaN/GaN HEMT by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode, Yong Cai, Yugang Zhou, Kei May Lau and Kevin Chen, IEEE Transactions on Electron Devices, Vol. 53, No. 9, September 2006 (Cai et al.) it is taught that using a CF_4 process fluoride ions can be embedded in the barrier region of a depletion mode device in order to render the same normally OFF.

[0007] In practice, however, a depletion mode III-nitride HEMT which has been turned into an enhancement mode device using the CF_4 process is unstable. Specifically, after a period of operation, the threshold voltage of such a device tends to shift back to negative. That is, the device reverts back to depletion mode operation.

[0008] It is believed that the electric field between the gate electrode and the drain electrode of a III-nitride power semiconductor device is responsible for the shift of the threshold voltage.

[0009] To overcome the drawbacks discussed above, according to one aspect of the present invention, the voltage between the gate and the drain is reduced, whereby a stable enhancement mode III-nitride device, which has been fabricated for example, by using the CF_4 process is obtained.

[0010] According to one embodiment of the present invention, an enhancement mode III-nitride power device fabricated using the CF_4 process is provided with a field plate over the heterojunction which is shorted to the source electrode of the

device. As a result, the gate to drain voltage "seen" by the gate electrode is reduced, whereby the device is rendered more stable.

[0011] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0012] Fig. 1 schematically illustrates a cross-sectional view of two adjacent active cells of a device according to the present invention.

[0013] Fig. 2 schematically illustrates a cross-sectional view of two adjacent active cells of a device according to the second embodiment of the present invention.

[0014] Fig. 3 schematically illustrates a cross-sectional view of two adjacent active cells of a device according to the third embodiment of the present invention.

[0015] Fig. 4 schematically illustrates a cross-sectional view of two adjacent active cells of a device according to the fourth embodiment of the present invention.

[0016] Fig. 5A schematically illustrates a region under the gate of a device according to one configuration.

[0017] Fig. 5B schematically illustrates a region under the gate of a device according to another configuration.

[0018] Fig. 5C schematically illustrates a region under the gate of a device according to yet another configuration.

DETAILED DESCRIPTION

[0019] Referring to Fig. 1, a device according to the preferred embodiment of the present invention includes a III-nitride heterojunction 10 formed over a support body 12. Heterojunction 10 includes a first III-nitride body 14 formed over support body 12, and second III-nitride body 16 formed over first III-nitride body 14. The

thickness and composition of first and second III-nitride bodies 14, 16 are selected to generate a two-dimensional electron gas (2-DEG) at (near) the heterojunction thereof either inside first semiconductor body 14 or inside second semiconductor body 16, as is well known in the art.

[0020] In the preferred embodiment, first III-nitride body 14 serves as the channel layer and may be composed of GaN, and second III-nitride body 16 serves as the barrier layer and may be composed of AlGaN. Support body 12 may be a substrate that is compatible with first III-nitride body 14, e.g. GaN, or may be a substrate (e.g. silicon, SiC or sapphire) that includes a transition layer (e.g. AlN) to allow for the growth thereon of first III-nitride body 14.

[0021] A device according to the present invention further includes in each active cell thereof, first power electrode 18 (e.g. source electrode), second power electrode 20 (e.g. drain electrode), and a gate electrode 22 disposed between first power electrode 18 and second power electrode 20. In the preferred embodiment, and as illustrated by Fig. 1, gate electrode 22 makes a schottky contact with second III-nitride body 16. However, it should be understood that a gate electrode 22 may be capacitively coupled to second III-nitride body 16 (e.g. through a gate dielectric) without deviating form the scope and the spirit of the present invention.

[0022] In one preferred embodiment of the present invention, second III-nitride body (barrier layer) 16 is processed using the CF_4 process (or any other plasma based process) as set forth, for example, in Cai et al. to obtain a negatively charged region directly under the gate which causes the interruption of the 2-DEG directly under the gate in order to render the device normally OFF when no voltage is applied to the gate. Thus, for example, second III-nitride body 16 includes negative charges, e.g. negative Fluorine ions or chlorine ions, under the gate in order to render the device normally OFF when no voltage is applied to gate electrode 22.

[0023] According to an aspect of the present invention, a field plate 24 is disposed over second III-nitride body 16 and between a gate electrode 22 and drain electrode 20. Field plate 24 is electrically shorted to source electrode 18 to reduce the voltage between gate electrode 22 and drain electrode 20. Thus, the gate will experience the potential between the gate and the source which may be in the order of 6-7 volts typically. As a result, a stable enhancement mode III-nitride heterojunction power device is obtained. Field plate 24 may be shorted to source electrode 18 through a conductive bus residing on the device, or field plate 24 and source electrode 18 may be shorted outside the device, e.g. through electrically connected pads of a lead frame or a circuit board. Thus, field plate 24 and source electrode 18 would be at the same potential when the device is operating.

[0024] Note that field plate 24 may be a metallic body that is schottky coupled to second III-nitride body 16, or may be a conductive semiconductor body such as a highly conductive III-nitride body (e.g. N+ GaN or N+AlGaN) as illustrated by Fig. 1.

[0025] Referring to Fig. 2, in which like numerals identify like features, in a III-nitride heterojunction power device according to the second embodiment of the present invention, a gate dielectric 32 (e.g. $Si0_2$ or Si_3N_4) may be disposed between the gate electrode 18 and body 16. Furthermore, a dielectric body 34 (e.g. $Si0_2$ or Si_3N_4) may be disposed between field plate 24 and second III-nitride body 16.

[0026] Referring now to Fig. 3, in which like numerals identify like features, in a III-nitride heterojunction power device according to the third embodiment, gate electrode 22 is schottky coupled to second III-nitride body 16, while field plate 24 is capacitively coupled to second III-nitride body 16 though dielectric body 34.

[0027] Referring to Fig. 4, in which like numerals identify like features, in a III-nitride heterojunction power device according to the fourth embodiment, gate electrode 22 is capacitively coupled to second III-nitride body 16 through a

respective gate dielectric 32, while field plate 24 is schottky coupled to second III-nitride body 16.

[0028] Referring now to Figs. 5A-5C, to obtain an interrupted region 33 in the 2-DEG in each embodiment, negatively charged region 35, which may include implanted negative ions such as Fluorine ions or Chlorine ions, may be formed directly under the gate G inside second III-nitride body 16 (Fig. 5A), or inside first III-nitride body 14 (Fig. 5B), or inside both first III-nitride body 14 and second III-nitride body 16. The charge in each negatively charged region 35 should be selected to interrupt a portion of the 2-DEG under the gate G when no voltage is applied to the same.

[0029] A device according to any of the embodiments of the present invention is suited for power applications, and particularly large current high frequency applications.

[0030] One suitable application for devices according to the present invention are in driver circuits, e.g. MOSgate drivers or the like applications.

[0031] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A power semiconductor device comprising:

a III-nitride heterojunction that includes one III-nitride body over another III-nitride body, said one III-nitride body and said another III-nitride body having different bandgaps, whereby a two-dimensional electron gas is generated inside said III-nitride heterojunction;

a source electrode and a drain electrode both disposed over and coupled to said III-nitride heterojunction;

a gate electrode coupled to said III-nitride heterojunction;

a negatively charged region formed in said III-nitride heterojunction directly under said gate electrode; and

a field plate coupled to said III-nitride heterojunction and disposed between said gate electrode and said drain electrode, wherein said field plate is electrically coupled to said source electrode, whereby said field plate is at the same potential as said source electrode when said device is operating.

2. The power semiconductor device of claim 1, wherein said negatively charged region includes negatively charged ions.

3. The power semiconductor device of claim 1, wherein said negatively charged region includes fluorine ions.

4. The power semiconductor device of claim 1, wherein said negatively charged region includes chlorine ions.

5. The power semiconductor device of claim 1, wherein said field plate is schottky coupled to said III-nitride heterojunction.

6. The power semiconductor device of claim 1, wherein said field plate is capacitively coupled to said III-nitride heterojunction through a dielectric body.

7. The power semiconductor device of claim 1, wherein said gate electrode is schottky coupled to said III-nitride heterojunction.

8. The power semiconductor device of claim 1, wherein said gate electrode is capacitively coupled to said III-nitride heterojunction through a gate dielectric body.

9. The power semiconductor device of claim 1, wherein said one III-nitride body is comprised of AlGaN and said another III-nitride body is comprised of GaN.

10. A driver circuit that includes a III-nitride power semiconductor device, said III-nitride power semiconductor device comprising:

a III-nitride heterojunction that includes one III-nitride body over another III-nitride body, said one III-nitride body and said another III-nitride body having different bandgaps, whereby a two-dimensional electron gas is generated inside said III-nitride heterojunction;

a source electrode and a drain electrode both disposed over and coupled to said III-nitride heterojunction;

a gate electrode coupled to said III-nitride heterojunction;

a negatively charged region formed in said III-nitride heterojunction directly under said gate electrode; and

a field plate coupled to said III-nitride heterojunction and disposed between said gate electrode and said drain electrode, wherein said field plate is

electrically coupled to said source electrode, whereby said field plate is at the same potential as said source electrode when said device is operating.

11. The power semiconductor device of claim 10, wherein said negatively charged region includes negatively charged ions.

12. The power semiconductor device of claim 10, wherein said negatively charged region includes fluorine ions.

13. The power semiconductor device of claim 10, wherein said negatively charged region includes chlorine ions.

14. The power semiconductor device of claim 10, wherein said field plate is schottky coupled to said III-nitride heterojunction.

15. The power semiconductor device of claim 10, wherein said field plate is capacitively coupled to said III-nitride heterojunction through a dielectric body.

16. The power semiconductor device of claim 10, wherein said gate electrode is schottky coupled to said III-nitride heterojunction.

17. The power semiconductor device of claim 10, wherein said gate electrode is capacitively coupled to said III-nitride heterojunction through a gate dielectric body.

18. The power semiconductor device of claim 10, wherein said one III-nitride body is comprised of AlGaN and said another III-nitride body is comprised of GaN.

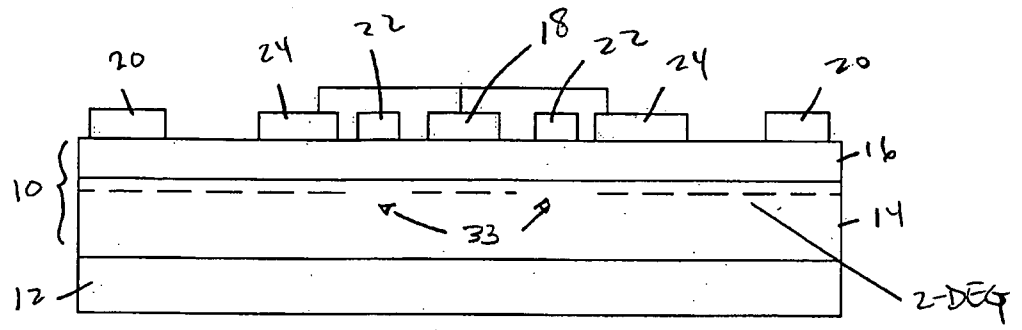

FIG. 1

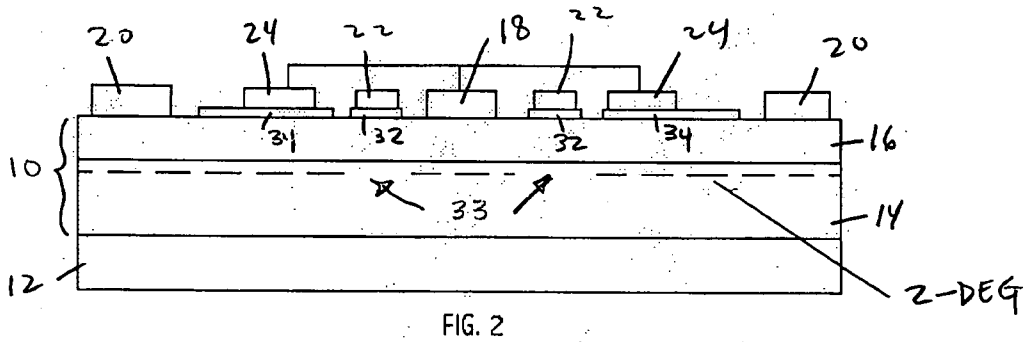

FIG. 2

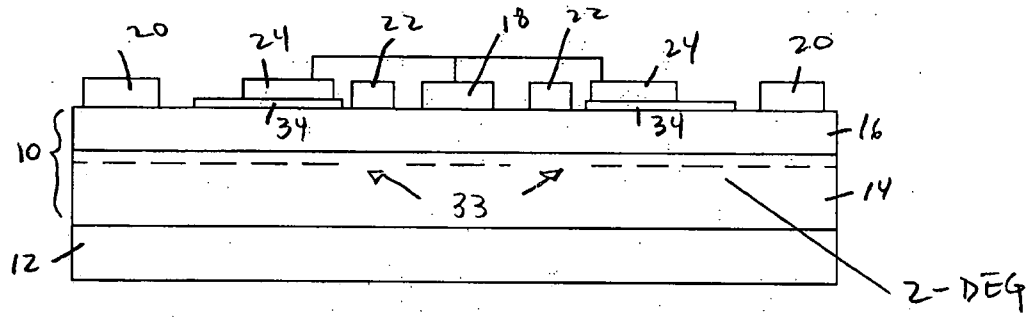

FIG. 3

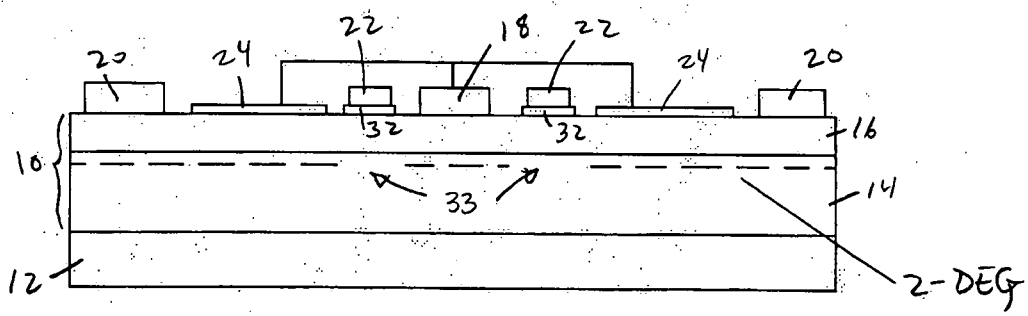

FIG. 4

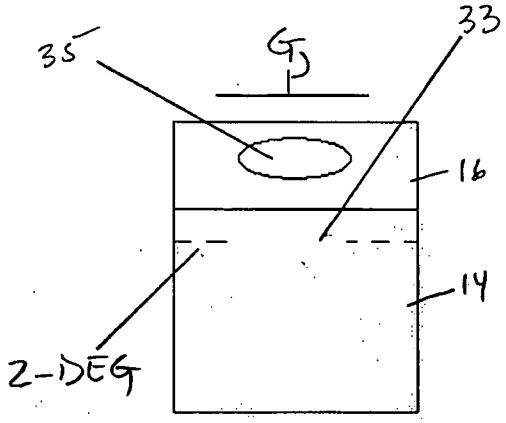

FIG. 5A

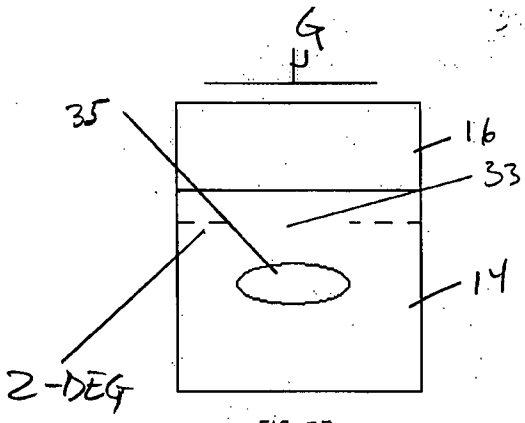

FIG. 5B

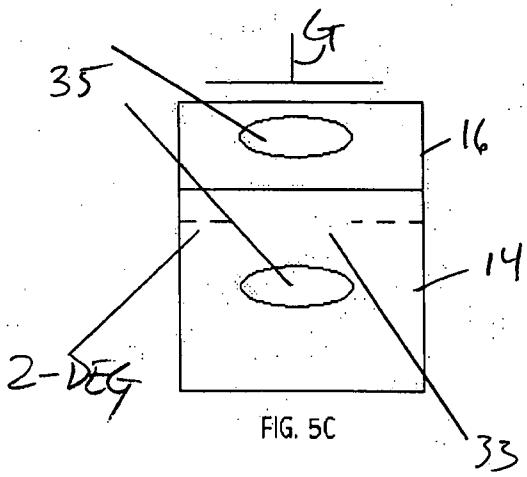

FIG. 5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/10986

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/12 (2008.04)
USPC - 257/189
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 29/12 (2008.04)
USPC - 257/189

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 257/11,12,183

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO WEST (USPT, PGPUB, EPAB, JPAB); INSPEC; Google Scholar
Search Terms: HFET, HEMT, JFET, heterojunction, transistor, enhancement mode, field plate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2007/0114569 A1 (Wu et al.) 24 May 2007 (24.05.2007), para [0006], [0025], [0026], [0033], [0034], [0035], [0037], [0038], [0049]; Fig 2, 3	1-4, 6, 7, 9-13, 15, 16, 18 --- 5, 8, 14, 17
Y	US 2007/0066020 A1 (Beach) 22 March 2007 (22.03.2007), para [0067], [0081]; Fig 4, 7	5, 8, 14, 17

☐ Further documents are listed in the continuation of Box C. ☐

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Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2008 (13.11.2008)	26 NOV 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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