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(54) **ASYMMETRIC-CHANNEL MEMORY SYSTEM**

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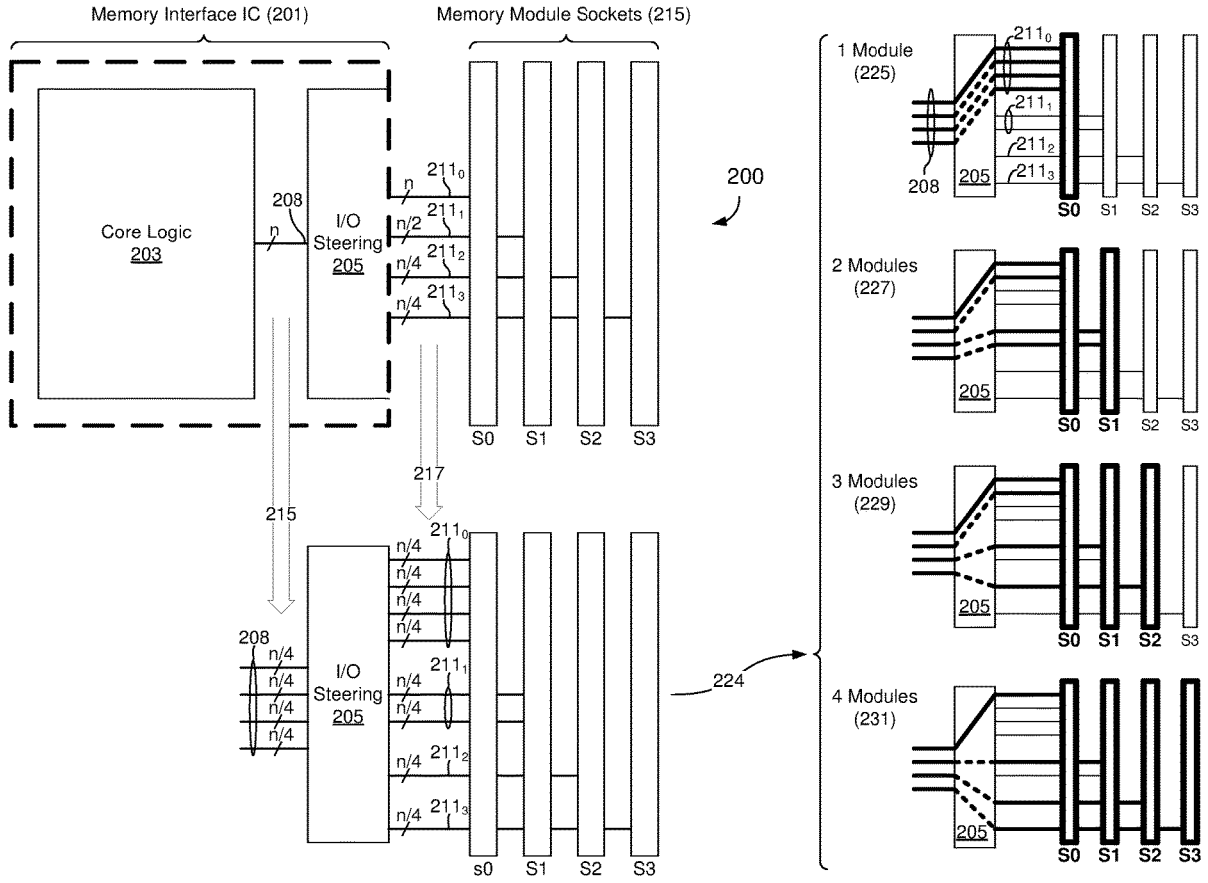
(52) **U.S. Cl.**

CPC ***G06F 13/1678*** (2013.01); ***G06F 13/4022*** (2013.01); ***G06F 13/1673*** (2013.01)

(57) **ABSTRACT**

An expandable memory system that enables a fixed signaling bandwidth to be configurably re-allocated among dedicated memory channels. Memory channels having progressively reduced widths are dedicated to respective memory sockets, thus enabling point-to-point signaling with respect to each memory socket without signal-compromising traversal of unloaded sockets or costly replication of a full-width memory channel for each socket.



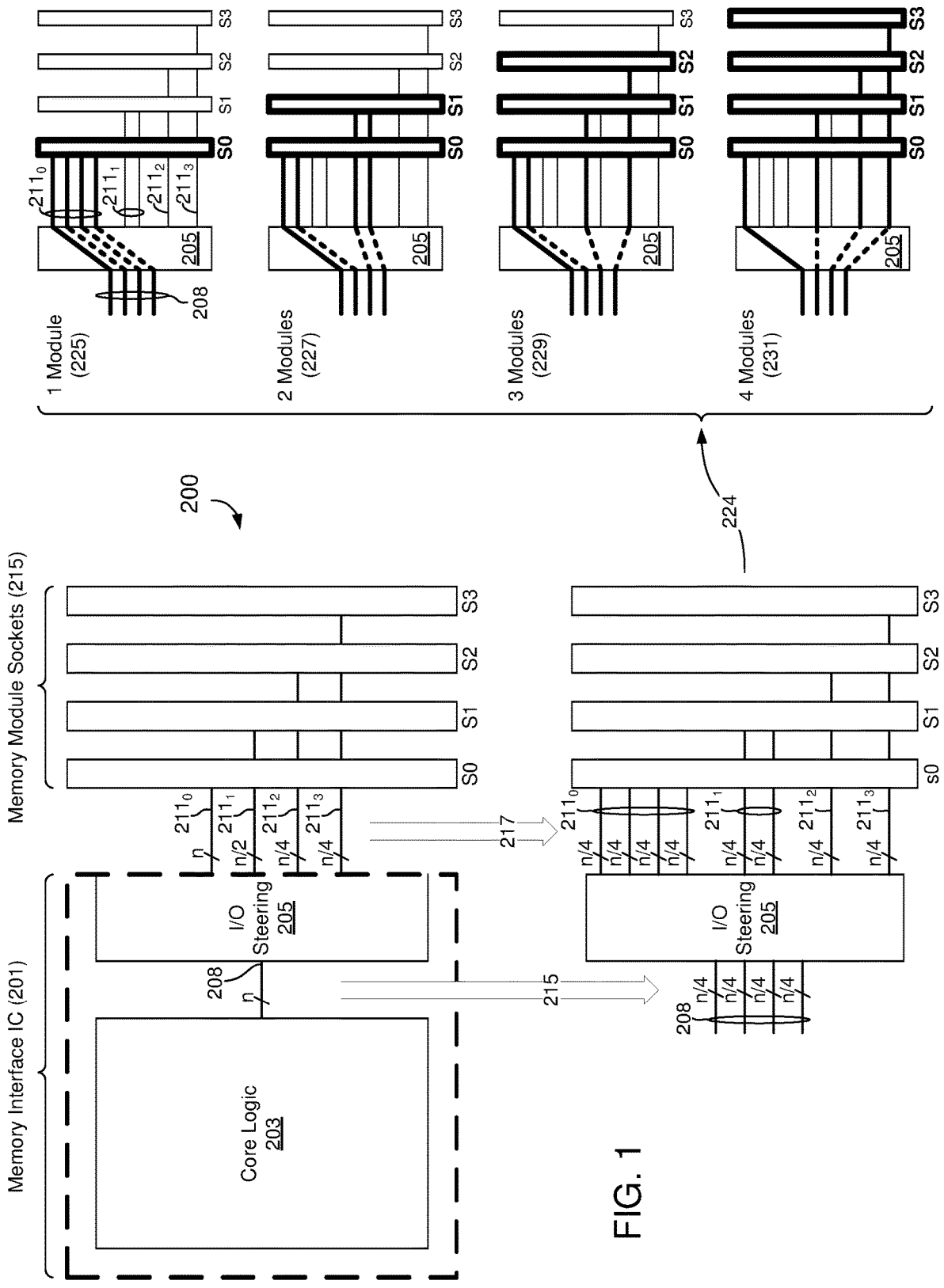

1 Module (225)
2 Modules (227)
3 Modules (229)
4 Modules (231)
S3
S2
S1
S0
205
208
200
224
Memory Module Sockets (215)
Memory Interface IC (201)
Core Logic 203
I/O Steering 205
217
215
n
n/2
n/4

FIG. 1

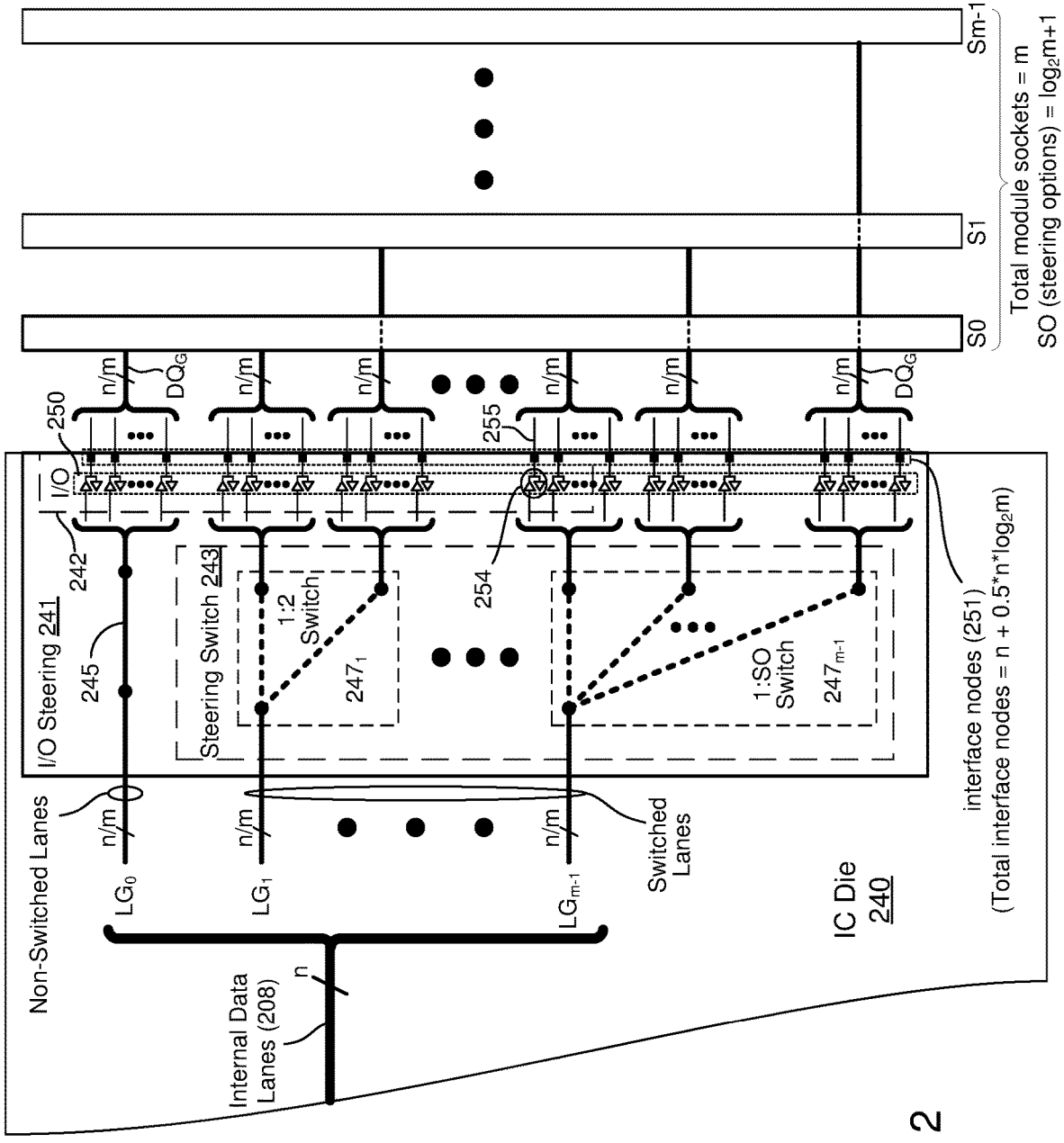

Sm-1
S1
S0
Total module sockets = m
SO (steering options) = log2m+1
DQG
n/m
250
I/O
242
I/O Steering 241
245
Steering Switch 243
1:2 Switch
2471
254
255
1:SO Switch
247m-1
interface nodes (251)
(Total interface nodes = n + 0.5*n*log2m)
Non-Switched Lanes
LG0
LG1
LGm-1
Switched Lanes
IC Die
240
Internal Data Lanes (208)
n

FIG. 2

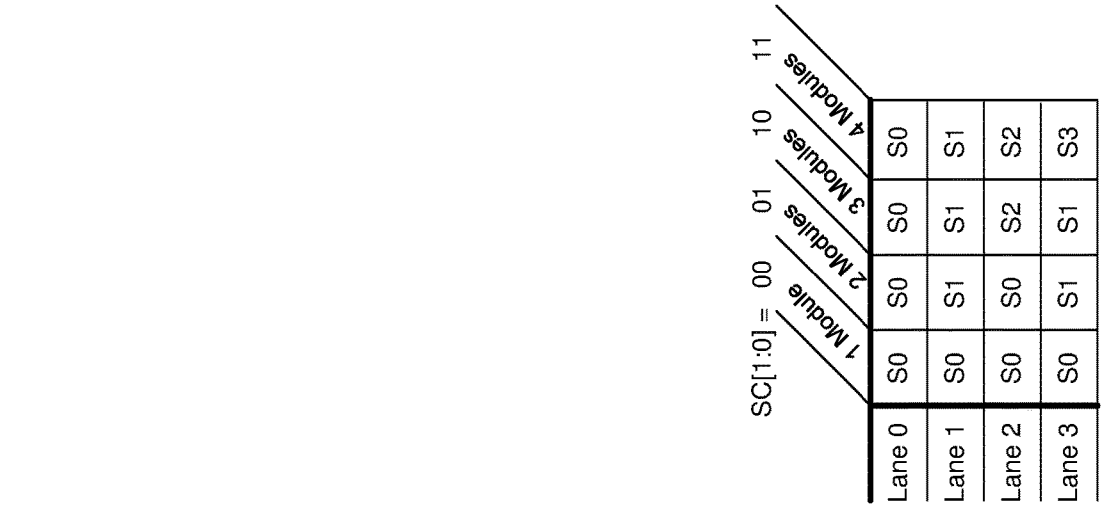

SC[1:0] = 00
01
10
11
1 Module
2 Modules
3 Modules
4 Modules
Lane 0
Lane 1
Lane 2
Lane 3
S0
S1
S2
S3

FIG. 3B

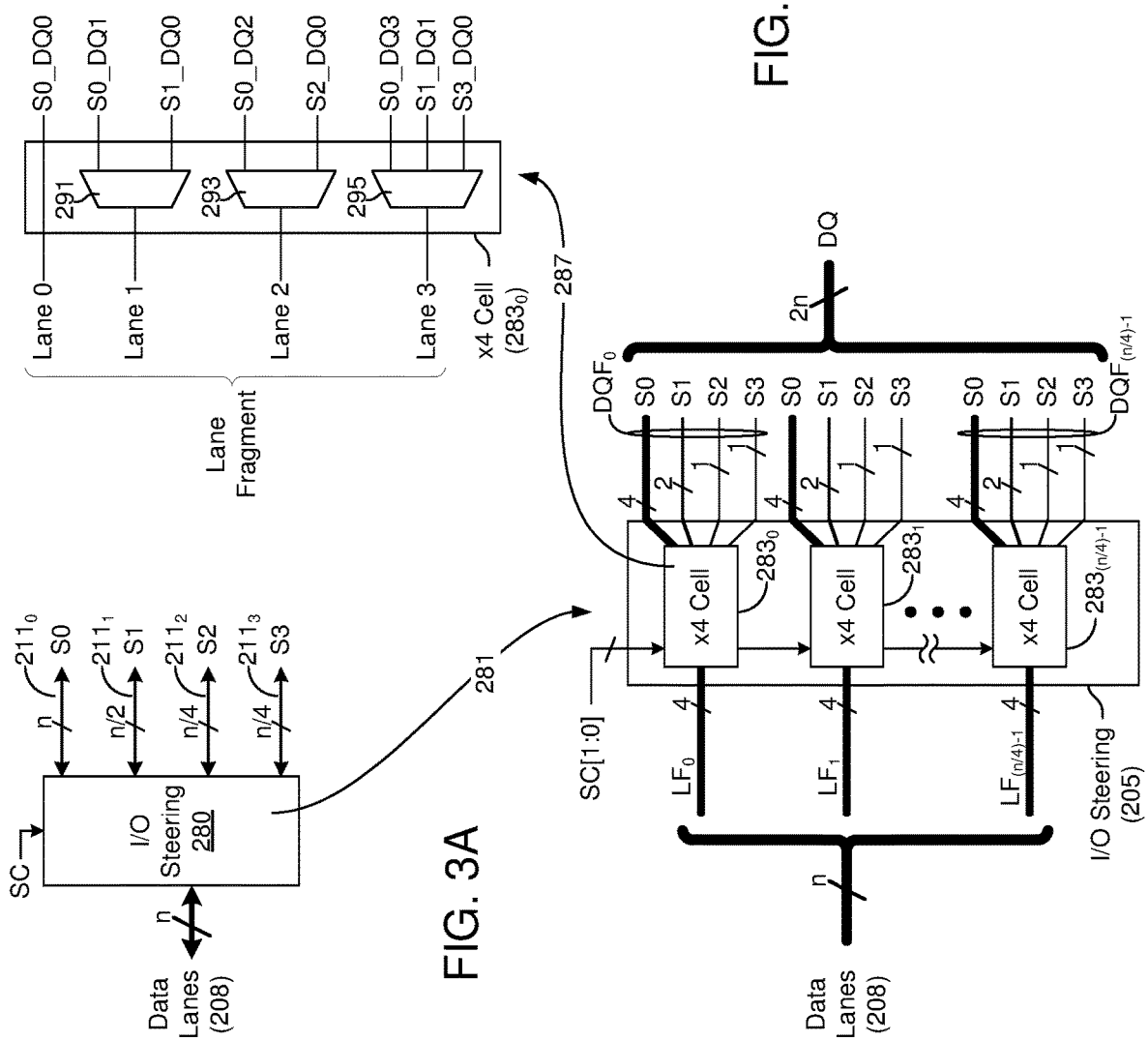

SC
I/O Steering 280
n
Data Lanes (208)
211_0
211_1
211_2
211_3
n
n/2
n/4
n/4
S0
S1
S2
S3
281
287
Lane 0
Lane 1
Lane 2
Lane 3
S0_DQ0
S0_DQ1
S1_DQ0
S0_DQ2
S2_DQ0
S0_DQ3
S1_DQ1
S3_DQ0
291
293
295
x4 Cell (283_0)
Lane Fragment
SC[1:0]
LF_0
LF_1
$LF_{(n/4)-1}$
4
x4 Cell
283_0
283_1
$283_{(n/4)-1}$
DQF_0
$DQF_{(n/4)-1}$
2n
DQ
I/O Steering (205)
Data Lanes (208)

FIG. 3A

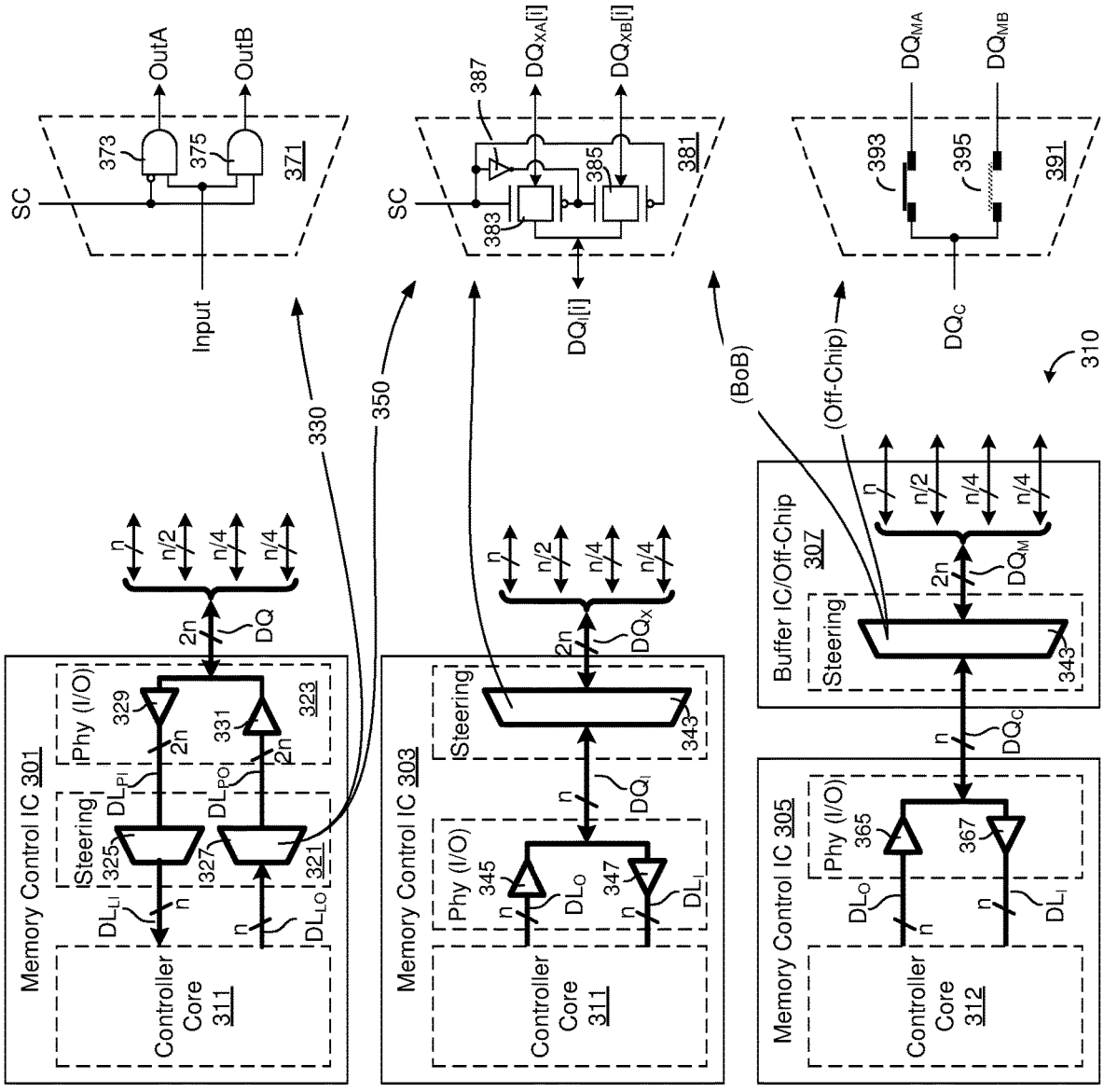
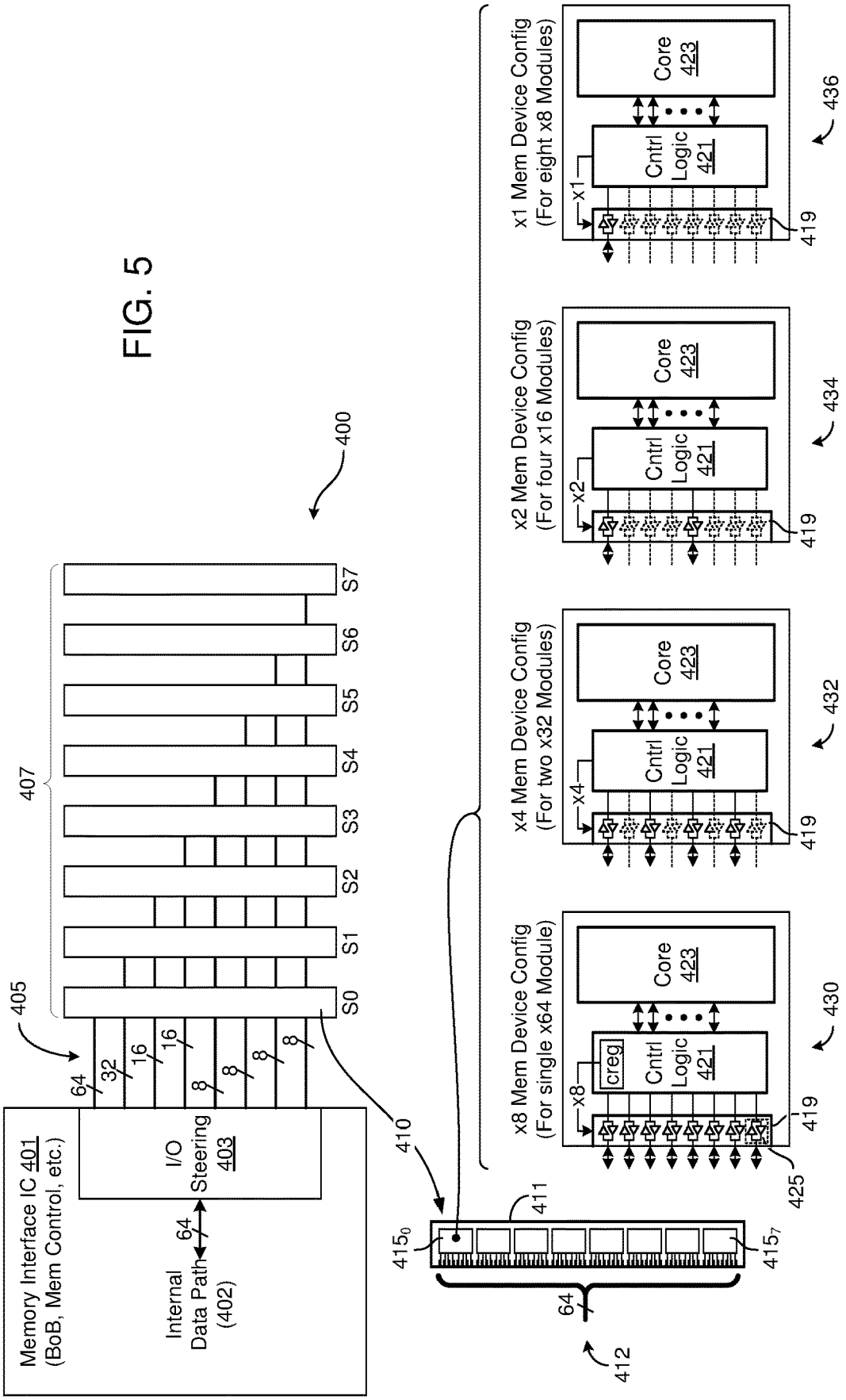

Memory Control IC 301
Memory Control IC 303
Memory Control IC 305
Buffer IC/Off-Chip 307
Controller Core 311
Controller Core 312
Phy (I/O)
Steering
SC
OutA
OutB
Input
DQ
DQ[i]
DQXA[i]
DQXB[i]
DQC
DQMA
DQMB
(BoB)
(Off-Chip)
330
350
310
371
373
375
381
383
385
387
391
393
395
321
323
325
327
329
331
343
345
347
365
367

FIG. 4

FIG. 5


400
407
405
S0
S1
S2
S3
S4
S5
S6
S7
64
32
16
16
8
8
8
8
Memory Interface IC 401
(BoB, Mem Control, etc.)
I/O Steering 403
64
Internal Data Path (402)
410
411
415_0
415_7
64
412
x8 Mem Device Config
(For single x64 Module)
x4 Mem Device Config
(For two x32 Modules)
x2 Mem Device Config
(For four x16 Modules)
x1 Mem Device Config
(For eight x8 Modules)
x8
x4
x2
x1
creg
Cntrl Logic 421
Core 423
419
425
430
432
434
436

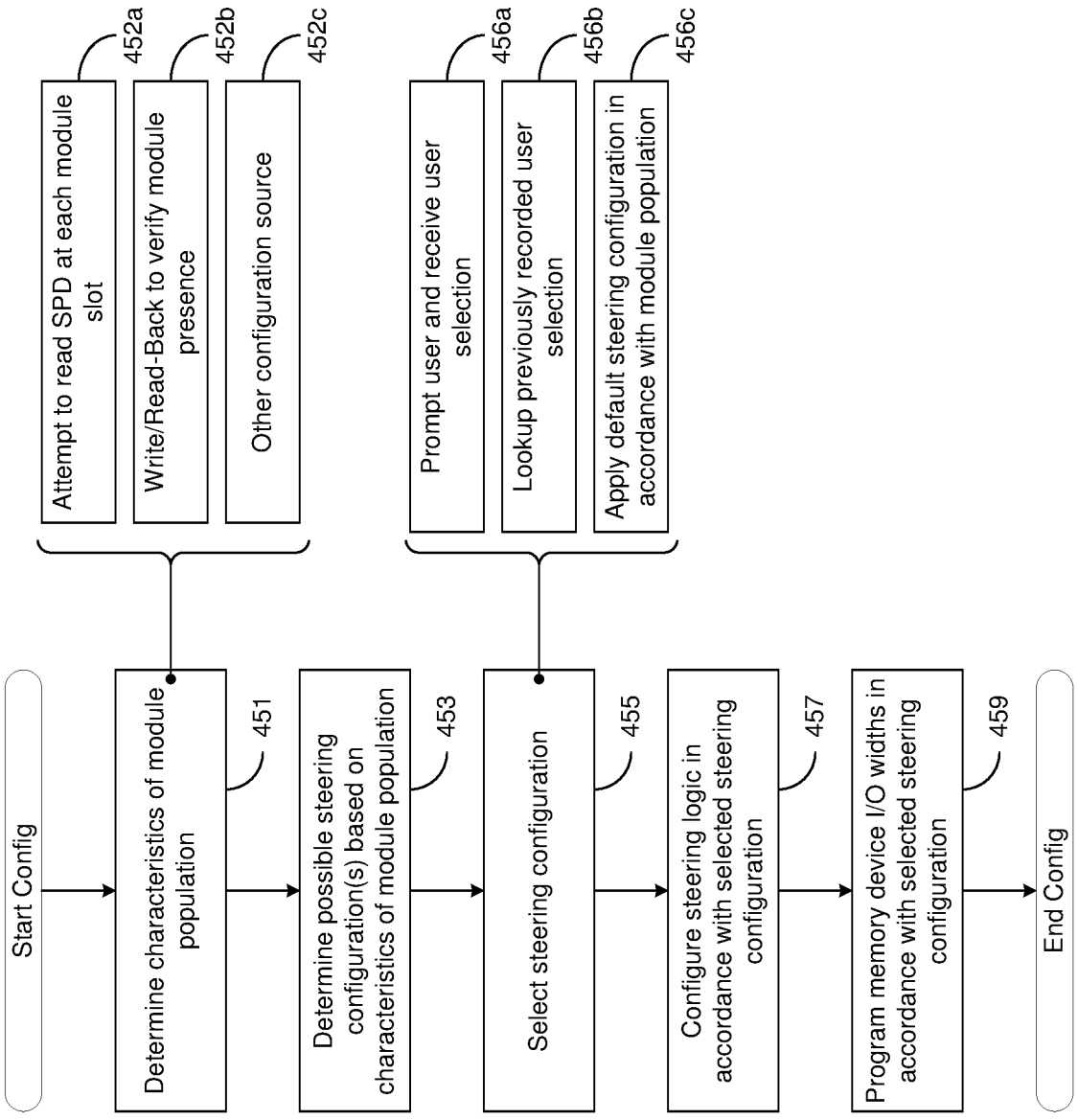

Start Config
Determine characteristics of module population
451
Determine possible steering configuration(s) based on characteristics of module population
453
Select steering configuration
455
Configure steering logic in accordance with selected steering configuration
457
Program memory device I/O widths in accordance with selected steering configuration
459
End Config
Attempt to read SPD at each module slot
452a
Write/Read-Back to verify module presence
452b
Other configuration source
452c
Prompt user and receive user selection
456a
Lookup previously recorded user selection
456b
Apply default steering configuration in accordance with module population
456c

FIG. 6

ASYMMETRIC-CHANNEL MEMORY SYSTEM

[0001] This application is a continuation of U.S. patent application Ser. No. 16/828,570 filed Mar. 24, 2020 (now U.S. Pat. No. 11,200,181), which is a continuation of U.S. patent application Ser. No. 15/992,112 filed May 29, 2018 (now U.S. Pat. No. 10,621,120), which is a continuation of U.S. patent application Ser. No. 15/458,166 filed Mar. 14, 2017 (now U.S. Pat. No. 9,996,485), which is a continuation of U.S. patent application Ser. No. 14/874,324 filed Oct. 2, 2015 (now U.S. Pat. No. 9,632,956), which is a continuation of U.S. patent application Ser. No. 13/499,029 filed Mar. 29, 2012 (now U.S. Pat. No. 9,183,166), which is a 35 U.S.C. § 371 U.S. National Stage of International Patent Application No. PCT/US2010/051318 filed Oct. 4, 2010, which claims priority to U.S. Provisional Patent Application No. 61/286,371 filed Dec. 14, 2009. Each of the above-identified patent applications is hereby incorporated by reference in its entirety.

[0002] Reflecting on the bandwidth allocation options of Table 1, each of the switched lane groups is switched between as few as two and at least as many as $\log_2 m+1$ different steering options. Lane group LG**1**, for example, is switchably coupled to either socket S**0** or socket S**1** (two steering options) and thus may be steered by a 1:2 switch element **247**$_1$ as shown. By contrast, lane group LG**7** is switchably coupled to one of four different sockets (i.e., $\log_2 8+1$=four steering options) so that, in the 8-socket example of Table 1, switch element **247**$_{m-1}$ may be implemented by a 1:4 switch), including socket S**0** in the single-module (x**1**) configuration, socket S**1** in the x**2** configuration, socket S**3** in the x**3**-x**6** configurations and socket S**7** in the x**7** and x**8** configurations. Thus, steering switch may be formed by m−1 switching elements (one for each of the switched lane groups), including switches having as few as two steering options (switch selections) per data lane, and switches having at least as many as $\log_2 m+1$ steering options. Also, because the number of required interface nodes increases by half the base number (n) for each doubling of the number of module sockets, the total number of interface nodes is given by $n+0.5*n*\log_2 m$ (or $n+½*n*(SO-1)$), where "*" denotes multiplication. That is, the number of interface nodes is proportional to the log of the socket count (not the socket count itself as in the replicated-channel system discussed above). Further, the number of interface nodes required per memory socket (and thus the memory channel width and maximum allocable fraction of the system bandwidth for that socket) halves with each doubling of the number of memory sockets, with the sockets in the last-to-be-loaded half of the system having half the minimum number of interface nodes provided to the sockets in the first-to-be-loaded half of the system. Analytically, the number of interface nodes per socket in such an embodiment may be expressed as: n/(2*^roundup($\log_2$X)), where '*^' denotes exponentiation, 'X' is the socket number (an integer between 1 and m that corresponds to the order in which the socket is loaded, with socket number 1 being loaded first), and "roundup( )" is a function that rounds its argument up to the nearest integer. For example, in an eight-socket system in accordance with the foregoing, the number of interface nodes per socket may be as follows (more or fewer sockets may be provided in alternative embodiments):

TABLE 2

Socket Position	Socket No.	Interface Nodes (memory channel width)
S0	1	n
S1	2	n/2
S2	3	n/4
S3	4	n/4
S4	5	n/8
S5	6	n/8
S6	7	n/8
S7	8	n/8

[0003] Detail view **350** illustrates an example of a switching element **381** that may be replicated as necessary within steering circuit **343** (or within steering circuits **325** and/or **327**) to provide a bidirectional 1:2 (and 2:1) or unidirectional signal steering function. As shown, an internal signal link, DQ_I is switchably coupled to each of two external signaling links DQ_{XA} and DQ_{XB} via respective pass gates **383** and **385**. Each of the pass gates is implemented by a pair of parallel-coupled transistors that is switched on in response to opposite polarity gate voltages (e.g., PMOS and NMOS transistors in the example shown). A switch control signal is provided to the gate terminals of each pass-gate **383** and **385** in a reverse polarity orientation such that one of the pass gates is switched to a conducting state (i.e., switched on) and the other to a substantially non-conducting state (i.e., switched off), depending on the state of the switch control signal. More specifically, in the embodiment shown, a logic high switch control signal switches on pass gate **383** (through application of the logic high voltage to the NMOS transistor and a logic low voltage, generated by inverted **387**, to the PMOS transistor) and switches off pass gate **385** to switchably couple the internal data link, DQ_I[i] exclusively and bidirectionally to external link DQ_{XA}[i]. Conversely, a logic low switch-control signal switches on pass gate **385** (logic low signal applied to PMOS transistor and logic high signal, generated by inverter **387**, applied to NMOS transistor) and switches off pass gate **383** to switchably couple DQ_I[i] exclusively and bidirectionally to external link DQ_{XB}[i]. Analog switching element **381** may be used as a building block (or the number of pass gates therein increased) to provide a generalized 1:N or N:1 steering function.

[0004] As mentioned, the steering circuitry may also be disposed in a buffer IC **307**, thus enabling use of a memory control IC that lacks an internal steering function (e.g., the buffer IC may provide for capacity expansion while maintaining a compatible system integration with legacy systems that utilize memory controllers lacking an internal steering function). In the embodiment shown, for example, buffer IC **307** is coupled between a set of asymmetric memory channels (shown as four channels having widths n, n/2, n/4 and n/4) and a memory control IC **305** having controller core logic **313** and physical I/O circuitry (drivers **365** and receivers **367**), but lacking the above-described signal steering function. More specifically, the buffer IC **307** includes a steering circuit **361** and memory-side interface (indicated conceptually by links DQ_M) to the asymmetric memory channels, as well as a controller-side interface (indicated by links DQ_C) to the memory control IC **305**. The buffer IC may be mounted to a motherboard or other substrate (thus forming a buffer-on-board) or together with the memory control IC and/or other IC's in an integrated circuit package

(e.g., a system-in-package). With regard to internal organization, the steering circuit **361** may be disposed on either side of the physical memory-side signaling interface (e.g., as in memory IC **301** or memory IC **303**) and thus implemented using either of the multiplexing or switching elements **371** and **381**.

1-20. (canceled)

21. An integrated circuit (IC) component comprising:

a controller-side data interface, N-bits wide, to be coupled to a memory control component;

a first memory-side data interface, N-bits wide, to be coupled to a first memory module socket;

a second memory-side data interface, M-bits wide, to be coupled to a second memory module socket, M being not more than N divided by two; and

interconnect circuitry coupled between the controller-side data interface and the first and second memory-side data interfaces.

22. The IC component of claim **21** wherein the interconnect circuitry comprises steering circuitry to switchably conduct first data values received via a first portion of the controller-side data interface exclusively to either the first memory-side data interface or the second memory-side data interface.

23. The IC component of claim **22** wherein the steering circuitry to switchably conduct the first data values exclusively to either the first memory-side data interface or the second memory-side data interface comprises circuitry to conduct the first data values exclusively to either the first memory-side data interface or the second memory-side data interface in accordance with a control signal that indicates whether the second memory module socket is populated by a memory module.

24. The IC component of claim **23** wherein the interconnect circuitry is further to conduct second data values received via a second portion of the controller-side data interface exclusively to the first memory-side data interface irrespective of whether the control signal indicates that the second memory module socket is populated by a memory module.

25. The IC component of claim **24** wherein the first and second portions of the controller-side data interface comprise simultaneously receive the first data values and the second data values, respectively.

26. The IC component of claim **23** further comprising a programmable register to output, according to a configuration value stored therein, the control signal that indicates whether the second memory module socket is populated by a memory module.

27. The IC component of claim **21** further comprising a third memory-side data interface, K-bits wide, to be coupled to a third memory module socket, K being not more than N divided by three, and wherein the interconnect circuitry is further coupled between the controller-side data interface and the third memory-side data interface.

28. The IC component of claim **27** further comprising a fourth memory-side data interface, J-bits wide, to be coupled to a fourth memory module socket, J being not more than N divided by four, and wherein the interconnect circuitry is further coupled between the controller-side data interface and the fourth memory-side data interface.

29. The IC component of claim **28** wherein M is equal to N/2, K is equal to N/4 and J is equal to N/4.

30. The IC component of claim **21** wherein the first memory-side interface comprises a first group of M signal transceiver circuits and a second group of M signal transceiver circuits, and the second memory-side interface comprises a third group of M signal transceiver circuits, the IC component further comprising power-control circuitry to disable power to either the second group of M signal transceiver circuits or the third group of M signal transceiver circuits in accordance with a control signal that indicates whether the second memory module socket is populated by a memory module.

31. A method of operation within an integrated circuit (IC) component, the method comprising:

receiving first and second data values from a memory control component concurrently via respective portions of an N-bit wide controller-side data interface;

outputting the first data values from the IC component via a first portion of a first memory-side data interface, N-bits wide, to a memory module resident within a first memory module socket; and

outputting the second data values from the IC component, in accordance with a control value, either via a second portion of the first memory-side data interface or via a second memory-side data interface, the second memory-side data interface being M-bits wide, where M is not more than N divided by two.

32. The method of claim **31** wherein outputting the first data values from the IC component via the first portion of a first memory-side data interface comprises outputting the first data values via the first portion of the first memory-side data interface to a first memory module resident within a first memory module socket.

33. The method of claim **32** wherein outputting the second data values from the IC component either via the second portion of the first memory-side data interface or via the second memory-side data interface comprises outputting the second data values via the second memory-side data interface to a second memory module within a second memory module socket if the control value has a first state and outputting the second data values via the second portion of the first memory-side data interface to the first memory module resident within the first memory module socket if the control value has a second state, the second state indicating that the second memory module socket is unpopulated.

34. The method of claim **32** further comprising outputting the second data values from the IC component either via the second portion of the first memory-side data interface or via the second memory-side data interface concurrently with outputting the first data values via the first portion of the first memory-side data interface.

35. The method of claim **31** further comprising storing the control value within a programmable register of the IC component.

36. The method of claim **31** further comprising:

receiving third data values from the memory control component via the N-bit wide controller-side data interface concurrently with reception of the first data values and second data values; and

outputting the third data values from the IC component, in accordance with the control value, via either (i) the second portion of the first memory-side data interface, (ii) the second memory-side data interface, or (iii) a

third K-bit wide memory-side data interface, K being not more than N divided by three.

37. The method of claim **36** further comprising:

receiving fourth data values from the memory control component via the N-bit wide controller-side data interface concurrently with reception of the first data values, second data values and third data values; and

outputting the fourth data values from the IC component, in accordance with the control value, via either (i) the second portion of the first memory-side data interface, (ii) the second memory-side data interface, or (iii) a fourth J-bit wide memory-side data interface, J being not more than N divided by four.

38. The method of claim **37** wherein M is equal to N/2, K is equal to N/4 and J is equal to N/4.

39. The method of claim **37** wherein outputting the first data values, second data values, third data values and fourth data values comprises outputting the first data values, second data values, third data values and fourth data values concurrently from the IC component.

40. A integrated circuit component comprising:

means for receiving first and second data values from a memory control component concurrently via respective portions of an N-bit wide controller-side data interface;

means for outputting the first data values from the IC component via a first portion of a first memory-side data interface, N-bits wide, to a memory module resident within a first memory module socket; and

means for outputting the second data values from the IC component, in accordance with a control value, either via a second portion of the first memory-side data interface or via a second memory-side data interface, the second memory-side data interface being M-bits wide, where M is not more than N divided by two.

* * * * *