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(54) **DC-DC POWER CONVERSION APPARATUS**

DC-DC-WANDLER

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Description

Technical Field

[0001] The present invention relates to a DC-DC power conversion apparatus that converts a DC voltage to a stepped-up or stepped-down DC voltage.

Background Art

[0002] There is a DC-DC power conversion apparatus in the related art having two or more switching units each of which includes two or more semiconductor switching elements that perform switching operations complementarily. All the semiconductor switching elements of the respective switching units are connected in series. The DC-DC power conversion apparatus also has an energy transition capacitor and an inductor. DC-DC conversion is performed using charging/discharging of the energy transition capacitor by switching operations of the semiconductor switching elements of the respective switching units. Low-voltage withstanding semiconductor switching elements and a small inductor can be used and a ratio of an input voltage and an output voltage can be adjusted by changing ON-duties of the semiconductor switching elements (for example, see Patent Document 1).

Related Art Documents

Patent Document

[0003] Patent Document 1: Japanese Patent No. 3414749

Non-Patent Document

[0004] Non-Patent Document 1: Thierry A. Meynard et al: "Multicell Converters: Basic Concepts and Industry Applications", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 5, OCTOBER 2002

[0005] EP 2 485 376 A1 discloses a DC/DC power converter comprising high voltage terminals, low voltage terminals, rectification devices connected in series between the high voltage terminals and switching devices connected in parallel to the rectification devices. A capacitor is provided for retaining a divided voltage of the voltage between the high voltage terminals and in parallel to the rectification devices. A reactor is connected between one of the low voltage terminals and a series connection point among the rectification devices. A control circuit controls the ON/OFF operation of the switching devices, thereby controlling the DC voltage conversion. The control is performed such that a voltage ratio of the DC voltage conversion, the inductance of the reactor and the switching frequency are taken into consideration such that the magnitude of a current ripple flowing in the reactor is equal to or smaller than a predetermined limit irrespective of the voltage ratio.

[0006] WO 2008/032362 A1 describes a DC/DC converter device composed of a capacitor, switching transistors which has a small-scale simple circuit structure and is capable of increase the electric power to be converted. A DC/DC converter device comprises a series circuit of a capacitor and an inductor inserted between a low-voltage DC power supply and a high-voltage DC power supply and semiconductor switching elements. A mode in which simultaneous conduction of the switches and simultaneous conduction of the switches are alternately switched by using as the drive frequency the resonance frequency at which the capacitor and the inductor series-resonate and the series circuit is connected parallel to the low-voltage DC power supply and a mode in which the series circuit is connected in series to the low-voltage DC power supply and this second series circuit is connected parallel to the high-voltage DC power supply are alternately switched thereby to increase the converted power for each switching.

[0007] JP S61 92162 A describes a DC voltage converter provided between a reactor connected with a DC power source and an output voltage smoothing capacitor. The converter has the first and second switching elements, a charging/discharging capacitor and first and second diodes. The capacitor is charged by the first diode when the first switching element is ON, the capacitor is discharged through the second diode when the second switching element is ON, and the discharging current is applied to the capacitor. The switching elements are alternately turned ON, to obtain double voltage of the DC power source.

[0008] US 2008/0211316A1 describes an electric power converter for a DC/DC converter which variably steps up a voltage successively with an optional magnification of one to two times or more and/or step down a voltage successively with a step-down ratio of one time or less. The converter includes a first input-output part, an inductor connected with a positive or a negative electrode side of the first input-output part, plural switches, plural capacitors, a second input-output part connected with plural capacitors, and a control circuit, wherein the control circuit controls the plural switches with operation mode and makes the inductor and plural capacitors selectively functional, wherein the electric power converter

is of a switched capacitance type that performs any operation out of step-up, step-down, regeneration, and continuity, and wherein the control circuit controls to have a period for which two switches out of the plural switches are simultaneously turned ON.

Summary of the Invention

Problem to be Solved by the Invention

[0009] The DC-DC power conversion apparatus in the related art uses the energy transition capacitor and the inductor to perform DC-DC power conversion using charging/discharging of the energy transition capacitor, and low-voltage withstanding semiconductor switching elements and a small inductor can be used.

[0010] In the DC-DC power conversion apparatus in the related art, however, two semiconductor switching elements perform switching operations complementarily. Accordingly, a certain ripple current flows through the inductor independently of an amount of load, and a loss occurs because this current flows further through the energy transition capacitor and the semiconductor switching elements. Hence, power conversion efficiency is low under low load.

[0011] Meanwhile, when an inductance value of the inductor is increased, a ripple current decreases and therefore a loss can be lessened. Hence, it becomes possible to increase power conversion efficiency under low load. However, when an inductance value is increased, there arises a problem that a volume and a weight of the inductor are increased and so are a volume and a weight of the DC-DC power conversion apparatus.

[0012] The invention is devised to solve the problem as above and has an object to provide an improved DC-DC power conversion apparatus capable of reducing a loss under low load even when a small and light inductor having a small inductance value is used.

Means for Solving the Problems

[0013] The above problem is solved and the above object is achieved by a DC-DC power conversion apparatus as described in claim 1. Advantageous embodiments are described in the subclaim.

Advantage of the Invention

[0014] According to the DC-DC power conversion apparatus of the invention, because the DC-DC power conversion apparatus has means for performing operations in four types of switching modes according to a ratio of input/output voltages of the DC-DC power conversion apparatus and a direction of power transmission in the DC-DC power conversion apparatus, the semiconductor switching elements perform a current-discontinuing operation with which an inductor current becomes 0 under low load. Hence, even when a small inductor having a small inductance value is used, a ripple current through the inductor under low load decreases and losses in the energy transition capacitor, the inductor, and the semiconductor switching elements can be lessened. It thus becomes possible to increase power conversion efficiency under low load.

[0015] The foregoing and other objects features, aspects, and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken conjunction with the accompanying drawings.

Brief Description of the Drawings

[0016]

Fig. 1 is an electrical circuit diagram showing a configuration of a main circuit of a DC-DC power conversion apparatus according to a first embodiment of the invention.

Fig. 2 is a view of an overall configuration showing a connection relation among a power supply, a motor generator, and the DC-DC power conversion apparatus according to the first embodiment of the invention.

Fig. 3 is a block diagram showing a configuration of a control unit of the DC-DC power conversion apparatus according to the first embodiment of the invention.

Fig. 4A is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-up operation under high load when a voltage ratio is 2 or greater.

Fig. 4B is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-up operation under low load when a voltage ratio is 2 or greater.

Fig. 5A is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-up operation under high load when a voltage ratio is 2 or smaller.

Fig. 5B is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-up operation under low load when a voltage ratio is 2 or smaller.

Fig. 6A is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-down operation under high load when a voltage ratio is 2 or greater.

Fig. 6B is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-down operation under low load when a voltage ratio is 2 or greater.

Fig. 7A is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-down operation under high load when a voltage ratio is 2 or smaller.

Fig. 7B is a waveform chart showing an operation of the DC-DC power conversion apparatus according to the first embodiment of the invention, that is, a waveform chart of a step-down operation under low load when a voltage ratio is 2 or smaller.

Fig. 8A is a waveform chart showing a step-up operation under high load of a DC-DC power conversion apparatus in the related art.

Fig. 8B is a waveform chart showing a step-up operation under low load of a DC-DC power conversion apparatus in the related art.

Fig. 9 is a view showing power conversion efficiency of the DC-DC power conversion apparatus according to the first embodiment of the invention.

Fig. 10 is an electrical circuit diagram showing a configuration of a main circuit of a DC-DC power conversion apparatus according to a second embodiment of the invention.

Mode for Carrying Out the Invention

[0017] Hereinafter, embodiments of the invention will be described with reference to the drawings. In the respective drawings, same reference numerals denote same or equivalent portions.

First Embodiment

[0018] Fig. 1 is an electrical circuit diagram showing a configuration of a main circuit of a DC-DC power conversion apparatus 10 according to a first embodiment of the invention.

[0019] The DC-DC power conversion apparatus 10 of the first embodiment is a two-way DC-DC power conversion apparatus furnished with a step-up function of converting a DC voltage V0 inputted between a voltage terminal VL and a voltage terminal VN to a stepped-up DC voltage V2 and outputting the DC voltage V2 between a voltage terminal VH and the voltage terminal VN, and a step-down function of converting the DC voltage V2 inputted between the voltage terminal VH and the voltage terminal VN to the stepped-down DC voltage V0 and outputting the DC voltage V0 between the voltage terminal VL and the voltage terminal VN.

[0020] Referring to Fig. 1, the main circuit of the DC-DC power conversion apparatus 10 includes smoothing capacitors C0 and C2 that smooth input/output DC voltages V0 and V2, respectively, a smoothing capacitor C1 functioning as an energy transition capacitor, a plurality of semiconductor switching elements S1a, S1b, S2a, and S2b, and an inductor L. The semiconductor switching elements S1a and S1b form a switching unit SU1 and the semiconductor switching elements S2a and S2b form a switching unit SU2.

[0021] Each of the semiconductor switching elements S1a, S1b, S2a, and S2b is formed of an IGBT (Insulated Gate Bipolar Transistor) and a diode connected to the IGBT in antiparallel.

[0022] The IGBT of each of the semiconductor switching elements S1a, S1b, S2a, and S2b has a collector terminal, an emitter terminal, and a gate terminal. The diode of each of the semiconductor switching elements S1a, S1b, S2a, and S2b is connected between the collector terminal and the emitter terminal of the IGBT of the corresponding semiconductor switching element S1a, S1b, S2a, or S2b in antiparallel so that an anode terminal is connected to the emitter terminal.

[0023] Connections of the DC-DC power conversion apparatus 10 will be described in detail.

[0024] The emitter terminal of the IGBT of the semiconductor switching element S1b is connected to a voltage terminal VM and the collector terminal thereof is connected to a high-voltage end terminal of the smoothing capacitor (energy transition capacitor) C1. The emitter terminal of the IGBT of the semiconductors switching element S1a is connected to

a low-voltage end terminal of the smoothing capacitor (energy transition capacitor) C1 and the collector terminal thereof is connected to the voltage terminal VM. The emitter terminal of the IGBT of the semiconductor switching element S2b is connected to a high-voltage end terminal of the smoothing capacitor (energy transition capacitor) C1 and the collector terminal thereof is connected to a high-voltage end terminal of the smoothing capacitor C2. The emitter terminal of the IGBT of the semiconductor switching element S2a is connected to a low-voltage end terminal of the smoothing capacitor C2 and the collector terminal thereof is connected to the low-voltage end terminal of the smoothing capacitor (energy transition capacitor) C1.

[0025] A low-voltage end terminal of the smoothing capacitor C0 is connected to the voltage terminal VN and a high-voltage end terminal of the smoothing capacitor C0 is connected to the voltage terminal VL. The low-voltage end terminal of the smoothing capacitor C2 is connected to the voltage terminal VN and the high-voltage end terminal of the smoothing capacitor C2 is connected to the voltage terminal VH. One end of the inductor L is connected to the voltage terminal VL and the other end is connected to the voltage terminal VM.

[0026] The gate terminal of the IGBT of the semiconductor switching element S1b is connected to an output terminal of a gate drive circuit 101b and a gate signal G1b is inputted into an input terminal of the gate drive circuit 101b. The gate terminal of the IGBT of the semiconductor switching element S1a is connected to an output terminal of a gate drive circuit 101a and a gate signal G1a is inputted into an input terminal of the gate drive circuit 101a. The gate terminal of the IGBT of the semiconductor switching element S2b is connected to an output terminal of a gate drive circuit 102b and a gate signal G2b is inputted into an input terminal of the gate drive circuit 102b. The gate terminal of the IGBT of the semiconductor switching element S2a is connected to an output terminal of a gate drive circuit 102a and a gate signal G2a is inputted into an input terminal of the gate drive circuit 102a.

[0027] Fig. 2 is a view of an overall configuration showing connections among the DC-DC power conversion apparatus 10, a power supply, and a motor generator. A battery Vs functioning as a voltage source is connected between the voltage terminals VL and VN of the DC-DC power conversion apparatus 10 and a DC terminal of a three-phase inverter INV is connected between the voltage terminals VH and VN. A motor generator MG is connected to AC terminals of the three-phase inverter INV.

[0028] When the motor generator MG performs a power running operation, the DC-DC power conversion apparatus 10 performs a step-up operation to output a DC voltage V0 inputted between the voltage terminals VL and VN as a stepped-up DC voltage V2. When the motor generator MG performs a regenerative operation, the DC-DC power conversion apparatus 10 performs a step-down operation to output a DC voltage V2 inputted between the voltage terminals VH and VN as a stepped-down DC voltage V0.

[0029] Fig. 3 is a block diagram showing a configuration of a control unit of the DC-DC power conversion apparatus 10.

[0030] The control unit includes a switching mode output portion 310, a PWM waveform output portion 320, a step-up/down discrimination portion 330, and a computation portion 340.

[0031] The computation portion 340 receives inputs of a voltage command value V2* of the DC voltage V2 and the DC voltage V2 and outputs an inductor average current command value ILdc*. The step-up/down discrimination portion 330 receives an input of the inductor average current command value ILdc* and outputs a step-up/down signal UD. The switching mode output portion 310 receives inputs of the step-up/down signal UD and the DC voltages V0 and V2 and outputs a switching mode signal SM. The PWM waveform output portion 320 receives inputs of the switching mode signal SM and the inductor average current command value ILdc* and outputs gate signals G1a, G1b, G2a, and G2b.

[0032] The gate signals G1a, G1b, G2a, and G2b are connected to the respective semiconductor switching elements via the corresponding gate drive circuits. The semiconductor switching elements S1a, S1b, S2a, and S2b switch ON when the gate signals G1a, G1b, G2a, and G2b, respectively, are high signals and switch OFF when the gate signals G1a, G1b, G2a, and G2b, respectively, are low signals.

[0033] The computation portion 340 calculates a difference between the voltage command value V2* and the voltage V2 to perform a proportional-integral operation and outputs the result as the inductor average current command value ILdc*. Feedback control on the DC voltage V2 is performed by outputting the inductor average current command value ILdc* so that the DC voltage V2 follows the current command value V2*.

[0034] The step-up/down discrimination portion 330 determines that the ongoing operation is a step-up operation when the inductor average current command value ILdc* is positive and outputs: step-up/down signal UD = step-up signal. When the inductor average current command value ILdc* is negative, the step-up/down discrimination portion 330 determines that the ongoing operation is a step-down operation and outputs: step-up/down signal UD = step-down signal.

[0035] The switching mode selection portion 310 selects a switching mode and outputs the switching mode signal SM.

[0036] In a case where the ongoing operation is a step-up operation and a voltage ratio V2/V0 is greater than 2, the switching mode output portion 310 selects a switching mode [1] and outputs: switching mode signal SM = switching mode [1]. In a case where the ongoing operation is a step-up operation and a voltage ratio V2/V0 is smaller than 2, the switching mode output portion 310 selects a switching mode [2] and outputs: switching mode signal SM = switching mode [2].

[0037] In a case where the ongoing operation is a step-down operation and a voltage ratio V2/VO is greater than 2,

the switching mode output portion 310 selects a switching mode [3] and outputs: switching mode signal SM = switching mode [3]. In a case where the ongoing operation is a step-down operation and a voltage ratio V2/V0 is smaller than 2, the switching mode output portion 310 selects a switching mode [4] and outputs: switching mode signal SM = switching mode [4]. It should be noted that a voltage ratio V2/V0 is 1 or greater independently of operation modes.

[0038] The PWM waveform output portion 320 outputs the gate signals G1a, G1b, G2a, and G2b on the basis of the switching mode and a value of the inductor average current command value ILdc*.

[0039] In the case of the switching mode [1], the PWM waveform output portion 320 outputs the gate signals G1a, G1b, G2a, and G2b with which an ON-duty of the semiconductor switching elements S1a and S2a is 50% or higher and an ON-duty of the semiconductor switching elements S1b and S2b is 0%.

[0040] In the case of the switching mode [2], the PWM waveform output portion 320 outputs the gate signals G1a, G1b, G2a, and G2b with which an ON-duty of the semiconductor switching elements Sa1 and Sa2 is 50% or below and an ON-duty of the semiconductor switching elements S1b and S2b is 0%.

[0041] In the case of the switching mode [3], the PWM waveform output portion 320 outputs the gate signals G1a, G1b, G2a, and G2b with which an ON-duty of the semiconductor switching elements S1a and S2a is 0% and an ON-duty of the semiconductor switching elements S1b and S2b is 50% or below.

[0042] In the case of the switching mode [4], the PWM waveform output portion 320 outputs the gate signals G1a, G1b, G2a, and G2b with which an ON-duty of the semiconductor switching elements S1a and S2a is 0% and an ON-duty of the semiconductor switching elements S1b and S2b is 50% or higher.

[0043] An operation to convert a DC voltage to a stepped-up or stepped-down DC voltage will now be described.

[0044] In a steady state, an average voltage of a voltage Vc1 across the smoothing capacitor (energy transition capacitor) C1 is 1/2 the DC voltage V2, that is V2/2. Because the DC voltage V2 is charged to the smoothing capacitor C2, applied voltages to the respective semiconductor switching elements S1a, S1b, S2a, and S2b are substantially V2/2. Also, as is described in Non-Patent Document 1, a ripple voltage applied to the inductor L decreases and a frequency of the ripple voltage applied to the inductor L is double the switching frequency. Hence, a small inductor L can be used.

[0045] In addition, the gate signals G2a and G2b are signals phase-delayed by 180° with respect to the gate signals G1a and G1b.

[0046] Fig. 4A and Fig. 4B are waveform charts in the switching mode [1] showing an operation of the DC-DC power conversion apparatus 10 of the first embodiment to step-up the DC voltage V0 to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V0 → V2).

[0047] Fig. 4A shows a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is large (high load) and this is a current-continuing operation with which an inductor current is always flowing.

[0048] Fig. 4B shows a step-up operation in a case where power to be stepped-up from the DC current V0 to the DC voltage V2 is small (low load) and this is a current-discontinuing operation with which there is a period during which no inductor current is flowing.

[0049] Fig. 5A and Fig. 5B are waveform charts in the switching mode [2] showing an operation of the DC-DC power conversion apparatus 10 of the first embodiment to step-up the DC voltage V0 to the DC voltage V2 that is less than double the DC voltage V0 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V0 → V2).

[0050] Fig. 5A shows a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is large (high load) and this is a current-continuing operation with which an inductor current is always flowing.

[0051] Fig. 5B shows a step-up operation in a case where power to be stepped-up from the DC current V0 to the DC voltage V2 is small (low load) and this is a current-discontinuing operation with which there is a period during which no inductor current is flowing.

[0052] Fig. 6A and Fig. 6B are waveform charts in the switching mode [3] showing an operation of the DC-DC power conversion apparatus 10 of the first embodiment to step-down the DC voltage V2 to the DC voltage V0 that is less than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V2 → V0).

[0053] Fig. 6A shows a step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is large (high load) and this is a current-continuing operation with which an inductor current is always flowing.

[0054] Fig. 6B shows a step-down operation in a case where power to be stepped-down from the DC current V2 to the DC voltage V0 is small (low load) and this is a current-discontinuing operation with which there is a period during which no inductor current is flowing.

[0055] Fig. 7A and Fig. 7B are waveform charts in the switching mode [4] showing an operation of the DC-DC power conversion apparatus 10 of the first embodiment to step-down the DC voltage V2 to the DC voltage V0 that is more than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V2 → V0).

[0056] Fig. 7A shows a step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is large (high load) and this is a current-continuing operation with which an inductor current is always flowing.

[0057] Fig. 7B shows a step-down operation in a case where power to be stepped-down from the DC current V2 to

the DC voltage V0 is small (low load) and this is a current-discontinuing operation with which there is a period during which no inductor current is flowing.

[0058] In Fig. 4A, Fig. 4B, Fig. 5A, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B, (a) shows chop signals Sc1 and Sc2 and a duty signal Sda(or 1-Sdb), (b) shows the gate signals G1a, G1b, G2a, and G2b, (c) shows a voltage across the inductor L, and (d) shows a current through the inductor L. It should be noted that the abscissa axes of Fig. 4A, Fig. 4B, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B are common time axes.

[0059] In (a) of Fig. 4A, Fig. 4B, Fig. 5A, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B, not only the chop signals Sc1 and Sc2 but also one switching cycle Ts is shown along the time axis. This is shown, by way of example, between two adjacent points at which the chop signal Sc1 drops to 0.0.

[0060] In (b) of Fig. 4A, Fig. 4B, Fig. 5A, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B, not only the gate signals G1a, G1b, G2a, and G2b but also zones 1 through 9 are shown along the time axis.

[0061] In (c) of Fig. 4A, Fig. 4B, Fig. 5A, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B, a voltage across the inductor L is shown by a solid line.

[0062] In (d) of Fig. 4A, Fig. 4B, Fig. 5A, Fig. 5B, Fig. 6A, Fig. 6B, Fig. 7A, and Fig. 7B, a current through the inductor L is shown by a solid line and also an average current Ildc is shown by a broken line.

[0063] Within the PWM waveform output portion 320, the chop signals Sc1 and Sc2 are compared with the duty signal Sda and the gate signals G1a and G2a are outputted. Also, the chop signals Sc1 and Sc2 are compared with the duty signal Sdb and the gate signals G1b and G2b are outputted.

[0064] Cycles of the chop signals Sc1 and Sc2 are denoted by Ts and a phase of the chop signal Sc2 is delayed by 180° with respect to the chop signal Sc1. Also, the chop signals Sc1 and Sc2 are chop signals having amplitude of 1.0. Regarding the chop signals Sc1 and Sc2, magnitude of a signal level corresponding to a valley of chop signals is 0.0 and magnitude of a signal level corresponding to a peak of chop signals is 1.0.

[0065] When the duty signal Sda is greater than the chop signal Sc1, the gate signal G1a is a high signal and when the duty signal Sda is smaller than the chop signal Sc1, the gate signal G1a is a low signal. When the duty signal Sda is greater than the chop signal Sc2, the gate signal G2a is a high signal and when the duty signal Sda is smaller than the chop signal Sc2, the gate signal G2a is a low signal.

[0066] Also, when (1 - Sdb) as the duty signal Sdb is smaller than the chop signal Sc1, the gate signal G1b is a high signal, and when (1 - Sdb) is greater than the chop signal Sc1, the gate signal G1b is a low signal. When (1 - Sdb) is smaller than the chop signal Sc2, the gate signal G2b is a high signal, and when (1 - Sdb) is greater than the chop signal Sc2, the gate signal G2b is a low signal.

[0067] Also, ON times Tla, T1b, T2a, and T2b in one switching cycle of the semiconductor switching elements S1a, S1b, S2a, and S2b, respectively, are expressed by equations as follows.

$$T1a = Sda \times Ts \quad \text{...(Equation 1)}$$

$$T1b = Sdb \times Ts \quad \text{...(Equation 2)}$$

$$T2a = Sda \times Ts \quad \text{...(Equation 3)}$$

$$T2b = Sdb \times Ts \quad \text{...(Equation 4)}$$

[0068] A description will be given on the assumption that the zone 1 is a zone in which the gate signal G1a is a high signal, the gate signal G1b is a low signal, the gate signal G2a is a high signal, and the gate signal G2b is a low signal.

[0069] Also, the zone 2 is given as a zone in which G1a is a high signal, G1b is a low signal, G2a is a low signal, and G2b is a high signal.

[0070] The zone 3 is given as a zone in which G1a is a low signal, G1b is a high signal, G2a is a high signal, and G2b is a low signal.

[0071] The zone 4 is given as a zone in which G1a is a low signal, G1b is a high signal, G2a is a low signal, and G2b is a high signal.

[0072] The zone 5 is given as a zone in which G1a is a high signal, G1b is a low signal, G2a is a low signal, and G2b is a low signal.

[0073] The zone 6 is given as a zone in which G1a is a low signal, G1b is a low signal, G2a is a high signal, and G2b is a low signal.

[0074] The zone 7 is given as a zone in which G1a is a low signal, G1b is a high signal, G2a is a low signal, and G2b is a low signal.

[0075] The zone 8 is given as a zone in which G1a is a low signal, G1b is a low signal, G2a is a low signal, and G2b is a high signal. The zone 9 is given as a zone in which G1a is a low signal, G1b is a low signal, G2a is a low signal, and G2b is a low signal.

[0076] The above is set forth in Table 1 below.

[Table 1]

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone 8	Zone 9
G2b	Lo	Hi	Lo	Hi	Lo	Lo	Lo	Hi	Lo
G2a	Hi	Lo	Hi	Lo	Lo	Hi	Lo	Lo	Lo
G1b	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Lo	Lo
G1a	Hi	Hi	Lo	Lo	Hi	Lo	Lo	Lo	Lo
Lo: low signal Hi: high signal									

[0077] Operations in the respective switching modes will now be described.

[0078] An operation to step-up the DC voltage V0 to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V0 → V2) in the switching mode [1] will be described using Fig. 4A and Fig. 4B. As are shown in Fig. 4A and Fig. 4B, in the switching mode [1], an ON-duty of the semiconductor switching elements S1a and S2a is higher than 50% (Sda > 50%) and an ON-duty of the semiconductor switching elements S1b and S2b is 0% (Sdb = 0%). Hence, one cycle is made up of the zone 1, the zone 5, and the zone 6 and no other zones are present.

[0079] Also, times Ts1, Ts5, and Ts6 of the zone 1, the zone 5, and the zone 6, respectively, in one switching cycle are expressed by equations below. For the zone 1 occurring twice in one cycle, Ts1 is a time per occurrence.

$$Ts5 = (1 - Sda) \times Ts \quad \ldots(\text{Equation } 5)$$

$$Ts6 = (1 - Sda) \times Ts \quad \ldots(\text{Equation } 6)$$

$$Ts1 = (Ts - Ts5 - Ts6)/2 = (Sda - 0.5)Ts \quad \ldots(\text{Equation } 7)$$

[0080] Firstly, a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is large (high load) will be described below with reference to Fig. 4A.

[0081] In the case of a high load, a current in a normal direction is always flowing through the inductor.

[0082] In the zone 1, because the gate signals G1a and G2a are high signals and therefore the semiconductor switching elements S1a and S2a are ON, a current flows in a path specified below and the voltage V0 is applied to the inductor L. For ease of description, a voltage drop across the semiconductor switching elements and the capacitors is 0.

[0083] Capacitor C0 → inductor L → IGBT of semiconductor switching element S1a → IGBT of semiconductor switching element S2a

[0084] In the zone 6, because the semiconductor switching element S2a is ON, a current flows in a path specified below and a voltage (VO - V2/2) is applied to the inductor L.

[0085] Capacitor C0 → Inductor L → diode of semiconductor switching element S1b → capacitor C1 → IGBT of semiconductor switching element S2a

[0086] In the zone 5, because the semiconductor switching element S1a is ON, a current flows in a path specified below and a voltage (V0 - V2/2) is applied to the inductor L.

[0087] Capacitor C0 → inductor L → IGBT of semiconductor switching element Sla → capacitor C1 → diode of semiconductor switching element S2b → capacitor C2

[0088] A relation between the duty signal Sda and the input/output DC voltages V0 and V2 will also be described.

[0089] In a steady state, an average voltage across the inductor L in one switching cycle is 0 by neglecting a voltage drop caused by a resistance component and expressed as below, which is rewritten as Equation 8 below.

$$0 = ((V0 - V2/2) \times (Ts5 + Ts6) + V0 \times (2 \times Ts1))/Ts$$

$$V0 = (1 - Sda) \times V2 \quad \ldots(\text{Equation } 8)$$

[0090] As is obvious from Equation 8 above, by controlling the duty signal Sda under high load, it becomes possible to control a voltage ratio of the input/output DC voltages V0 and V2.

[0091] A step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is small (low load) will now be described below with reference to Fig. 4B.

[0092] An operation in one cycle will be described in order of the zone 1, the zone 6, the zone 1, and the zone 5 in time sequence. In the case of a low load, there is a period during which a current through the inductor L remains 0.

[0093] In the zone 1, because the gate signals G1a and G2a are high signals and therefore the semiconductor switching elements S1a and S2a are ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

[0094] Capacitor C0 → inductor L → IGBT of semiconductor switching element S1a → IGBT of semiconductor switching element S2a

[0095] The DC voltage V0 is applied to the inductor L and the current increases from 0.

[0096] In the zone 6, because the semiconductor switching element S2a is ON, a current flows in a path specified below at the beginning.

[0097] Capacitor C0 → inductor L → diode of semiconductor switching element S1b → capacitor C1 → IGBT of semiconductor switching element S2a

[0098] In this instance, an applied voltage to the inductor L is a negative voltage, (V0 - V2/2), and therefore an inductor current decreases. As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 6 and the current remains 0 for the rest of the period in the zone 6.

[0099] In the zone 1, the current flows in the same manner as described above.

[0100] In the zone 5, because the semiconductor switching element S1a is ON, a current flows in a path specified below at the beginning.

[0101] Capacitor C0 → inductor L → IGBT of semiconductor switching element S1a → capacitor C1 → diode of semiconductor switching element S2b → capacitor C2

[0102] In this instance, an applied voltage to the inductor L is a negative voltage, (V0 - V2/2), and therefore an inductor current decreases. As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 5 and the current remains 0 for the rest of the period in the zone 5.

[0103] In this manner, a current-discontinuing operation with which a current through the inductor L becomes 0 at midpoints in the zone 6 and the zone 5 is performed and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0104] A relation between the duty signal Sda and the input/output DC voltages V0 and V2 will now be described. Firstly, an average current Ildc of the inductor L will be described.

[0105] In the zone 1, the voltage V0 is applied to the inductor. With the use of an inductance value L of the inductor, an inductor maximum current Ilmax is expressed by Equation 9 as follows.

$$Ilmax = V0 \times Ts1/L = V0(Sda - 0.5)Ts/L \quad \ldots(\text{Equation } 9)$$

[0106] Also, given that a zone 61 is a zone in which a current is flowing through the inductor in the zone 6.

[0107] Let Ts61 be a time of the zone 61. Then, because a voltage (V0 - V2/2) is applied to the inductor in the zone 61 and a current through the inductor eventually becomes 0, Ts61 is expressed by Equation 10 as follows.

$$Ts61 = L \times Ilmax/(V2/2 - V0) = (V0/(V2/2 - V0)) \times (Sda - 0.5)Ts \quad \ldots(\text{Equation } 10)$$

[0108] Also, given that a zone 51 is a zone in which a current is flowing through the inductor in the zone 5. Let Ts51 be a time of the zone 51, then Equation 11 below is obtained in the same manner.

$$Ts51 = (V0/(V2/2 - V0)) \times (Sda - 0.5)Ts \quad \ldots(\text{Equation } 11)$$

[0109] Subsequently, the inductor average current Ildc that is an average current in one cycle of the inductor is expressed by Equation 12 as follows.

$$Ildc = 0.5 \times Ilmax \times ((Ts1 + Ts51) + (Ts1 + Ts61))/Ts$$

$$= 0.5 \times (V0 \times V2/(V2/2 - V0)) \times (Sda - 0.5)^2 Ts/L \quad \ldots(\text{Equation } 12)$$

[0110] Also, power P to be stepped-up from the DC voltage V0 to the stepped-up DC voltage V2 can be expressed by Equation 13 below. Hence, by adjusting an ON-duty (duty signal Sda) of the semiconductor switching elements S1a and S2a, it becomes possible to adjust the power P.

$$P = V0 \times Ildc = 0.5 \times (V0^2 \times V2/(V2/2 - V0)) \times (Sda - 0.5)^2 Ts/L \quad \ldots (\text{Equation } 13)$$

[0111] In a case where the power P to be stepped-up is larger than power consumed in the inverter INV, a difference in power is charged to the capacitor C2. Consequently, the DC voltage V2 rises. Conversely, in a case where the power P to be stepped-up is smaller than power consumed in the inverter INV, the capacitor C2 is discharged. Consequently, the DC voltage V2 drops. In the case of a low load, too, by adjusting an ON-duty (duty signal Sda) of the semiconductor switching elements S1a and S2a, it becomes possible to control the power P and hence to control a voltage ratio of the DC voltages V0 and V2.

[0112] In this manner, in an operation to step-up the DC voltage V0 to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V0 $\rightarrow$ V2), by selecting the switching mode [1] in which an ON-duty of the semiconductor switching elements S1a and S2a is higher than 50% (Sda > 50%) and an ON-duty of the semiconductor switching elements S1b and S2b is 0% (Sdb = 0%), it becomes possible to control a voltage ratio of the DC voltages V0 and V2.

[0113] Also, even when an inductor having a small inductance value is used, a current-discontinuing operation with which an inductor current becomes 0 is performed under low load and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0114] An operation to step-up the DC voltage V0 to the DC voltage V2 that is less than double the DC voltage V0 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V0 $\rightarrow$ V2) in the switching mode [2] will be described using Fig. 5A and Fig. 5B.

[0115] As are shown in Fig. 5A and Fig. 5B, in the switching mode [2], an ON-duty of the semiconductor switching elements S1a and S2a is lower than 50% (Sda < 50%) and an ON-duty of the semiconductor switching elements S1b and S2b is 0% (Sdb = 0%). Hence, one cycle is made up of the zone 9, the zone 5, and the zone 6 and no other zones are present.

[0116] Also, times Ts9, Ts5, and Ts6 of the zone 9, the zone 5, and the zone 6, respectively, in one switching cycle are expressed as below. For the zone 9 occurring twice in one cycle, Ts9 is a time per occurrence.

$$Ts5 = Sda \times Ts \quad \ldots(\text{Equation } 14)$$

$$Ts6 = Sda \times Ts \quad \ldots(\text{Equation } 15)$$

$$Ts9 = (Ts - Ts5 - Ts6)/2 = (0.5 - Sda)Ts \quad \ldots(\text{Equation } 16)$$

[0117] Firstly, a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is large (high load) will be described below with reference to Fig. 5A. In the case of a high load, a current in a normal

direction is always flowing through the inductor.

[0118] In the zone 5, because the gate signal G1a is a high signal and therefore the semiconductor switching element S1a is ON, a current flows in a path specified below and a voltage (V0 - V2/2) is applied to the inductor L.

Capacitor C0 → inductor L → IGBT of semiconductor switching element S1a → capacitor C1 → diode of semiconductor switching element S2b → capacitor C2

[0119] In the zone 9, because all the semiconductor switching elements are OFF, a current flows in a path specified below and a voltage (V0 - V2) is applied to the inductor L.

Capacitor C0 → Inductor L → diode of semiconductor switching element S1b → diode of semiconductor switching element S2b → capacitor C2

[0120] In the zone 6, because the gate signal G2a is a high signal and therefore the semiconductor switching element S2a is ON, a voltage is applied to the inductor L. Hence, a current flows in a path specified below and a voltage (VO - V2/2) is applied to the inductor L.

Capacitor C0 → inductor L → diode of semiconductor switching element S1b → capacitor C1 → IGBT of semiconductor switching element S2a

[0121] Also, a relation between the duty signal Sda and the input/output DC voltages V0 and V2 will also be described.

[0122] In a steady state, an average voltage across the inductor L in one switching cycle is 0 and expressed by Equation 17 as follows.

$$0 = ((V0 - V2/2) \times (Ts5 + Ts6) + (V0 - V2) \times (2 \times Ts9))/Ts$$

$$V0 = (1 - Sda) \times V2 \quad \ldots(\text{Equation } 17)$$

[0123] In this manner, by controlling the duty signal Sda under high load, it becomes possible to control a voltage ratio of the input/output DC voltages V0 and V2.

[0124] A step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is small (low load) will now be described below with reference to Fig. 5B.

[0125] An operation in one cycle will be described in order of the zone 5, the zone 9, the zone 6, and the zone 9 in time sequence. In the case of a low load, there is a period during which a current through the inductor L remains 0.

[0126] In the zone 5, because the gate signal G1a is a high signal and therefore the semiconductor switching element S1a is ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

Capacitor C0 → inductor L → IGBT of semiconductor switching element S1a → capacitor C1 → diode of semiconductor switching element S2b → capacitor C2

[0127] A DC voltage (V0 - V2/2) is applied to the inductor L and the current increases from 0.

[0128] In the zone 9, because all the semiconductor switching elements are OFF, a current flows in a path specified below at the beginning.

Capacitor C0 → inductor L → diode of semiconductor switching element S1b → diode of semiconductor switching element S2b → capacitor C2

[0129] In this instance, an applied voltage to the inductor L is a negative voltage, (V0 - V2), and an inductor current decreases. As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 9 and the current remains 0 for the rest of the period in the zone 9.

[0130] Likewise, in the zone 6, because the gate signal G2a is a high signal and therefore the semiconductor switching element S2a is ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

Capacitor C0 → inductor L → diode of semiconductor switching element S1b → capacitor C1 → IGBT of semiconductor switching element S2a

[0131] A voltage (V0 - V2/2) is applied to the inductor L and the current increases from 0.

[0132] In the zone 9, a current flows in the same manner as described for the zone 9 above.

[0133] In this manner, a current-discontinuing operation with which a current through the inductor L becomes 0 at a midpoint in the zone 9 is performed, and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened due to the presence of a period during which the current becomes 0.

[0134] A relation between the duty signal Sda and the input/output DC voltages V0 and V2 will now be described. Firstly, an average current Ildc of the inductor L will be described.

[0135] In the zones 5 and 6, a voltage (VO - V2/2) is applied to the inductor. With the use of an inductance value L of the inductor, an inductor maximum current Ilmax is expressed by Equation 18 as follows.

$$Ilmax = (V0 - V2/2) \times Ts5/L = (V0 - V2/2) \times Sda \times Ts/L \quad \ldots(\text{Equation } 18)$$

[0136] Also, given that a zone 91 is a zone in which a current is flowing through the inductor in the zone 9. Let Ts91 be a time of the zone 91. Then, because a voltage (VO - V2) is applied to the inductor in the zone 91 and a current through the inductor eventually becomes 0, Ts91 is expressed by Equation 19 as follows.

$$Ts91 = L \times Ilmax/(V2 - V0) = ((V0 - V2/2)/(V2 - V0)) \times Sda \times Ts \quad \ldots(\text{Equation } 19)$$

[0137] Subsequently, the inductor average current Ildc that is an average current in one cycle of the inductor is expressed by Equation 20 as follows.

$$Ildc = 0.5 \times Ilmax \times ((Ts5 + Ts91) + (Ts6 + Ts91))/Ts = 0.5 \times (V2(V0 - V2/2)/V2 - V0)) \times Sda^2 \times Ts/L \quad \ldots(\text{Equation } 20)$$

[0138] Also, power P to be stepped-up from the DC voltage V0 to the stepped-up DC voltage V2 can be expressed by Equation 21 below. Hence, by adjusting an ON-duty (duty signal Sda) of the semiconductor switching elements S1a and S2a, it becomes possible to adjust the power P.

$$P = V0 \times Ildc = 0.5 \times (V0 \times V2(V0 - V2/2)/(V2 - V0)) \times Sda^2 \times Ts/L \quad \ldots(\text{Equation } 21)$$

[0139] In the case of a low load, too, by adjusting an ON-duty (duty signal Sda) of the semiconductor switching elements S1a and S2a, it becomes possible to control the power P and hence to control a voltage ratio of the DC voltages V0 and V2.

[0140] In this manner, in an operation to step-up the DC voltage V0 to the DC voltage V2 that is less than double the DC voltage V0 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V0 $\rightarrow$ V2), by selecting the switching mode [2] in which an ON-duty of the semiconductor switching elements S1a and S2a is lower than 50% (Sda < 50%) and an ON-duty of the semiconductor switching elements S1b and S2b is 0% (Sdb = 0%), it becomes possible to control a voltage ratio of the DC voltages V0 and V2.

[0141] Also, even when an inductor having a small inductance value is used, a current-discontinuing operation with which an inductor current becomes 0 is performed under low load and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0142] An operation to step-down the DC voltage V2 to the DC voltage V0 that is less than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V2 $\rightarrow$ V0) in the switching mode [3] will be described using Fig. 6A and Fig. 6B. As are shown in Fig. 6A and Fig. 6B, in the switching mode [3], an ON-duty of the semiconductor switching elements S1b and S2b is lower than 50% (Sdb < 50%) and an ON-duty of the semiconductor switching elements S1a and S2a is 0% (Sda = 0%). Hence, one cycle is made up of the zone 8, the zone 9, and the zone 7 and no other zones are present.

[0143] Also, times Ts8, Ts9, and Ts7 of the zone 8, the zone 9, and the zone 7, respectively, in one switching cycle are expressed as below. For the zone 9 occurring twice in one cycle, Ts9 is a time per occurrence.

$$Ts8 = Sdb \times Ts \quad \ldots(\text{Equation } 22)$$

$$Ts7 = Sdb \times Ts \quad \ldots(\text{Equation } 23)$$

$$Ts9 = (Ts - Ts7 - Ts8)/2 = (0.5 - Sdb)Ts \quad \ldots(\text{Equation } 24)$$

[0144] Firstly, a step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is large (high load) will be described below with reference to Fig. 6A. In the case of a high load, a current in a negative direction is always flowing through the inductor.

[0145] In the zone 8, because the gate signal G2b is a high signal and therefore the semiconductor switching element S2b is ON, a current flows in a path specified below and a voltage (V0 - V2/2) is applied to the inductor L.

Capacitor C2 → IGBT of semiconductor switching element Sb2 → capacitor C1 → diode of semiconductor switching element S1a → inductor L → capacitor C0

[0146] In the zone 9, because all the semiconductor switching elements are OFF, a current flows in a path specified below and a voltage (VO - V2) is applied to the inductor L.

Diode of semiconductor switching element S2a → diode of semiconductor switching element S1a → inductor L → capacitor C0

[0147] In the zone 7, because the gate signal G1b is a high signal and therefore the semiconductor switching element S1b is ON, a current flows in a path specified below and a voltage (VO - V2/2) is applied to the inductor L.

Diode of semiconductor switching element S2a → capacitor C1 → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0148] Also, a relation between the duty signal Sdb and the input/output DC voltages V0 and V2 will also be described.

[0149] In a steady state, an average voltage across the inductor L in one switching cycle is 0 and a relation expressed below is established.

$$0 = ((V0 - V2/2) \times (Ts8 + Ts7) + V0 \times (2 \times Ts9))/Ts$$

$$V0 = Sdb \times V2 \quad \ldots(\text{Equation } 25)$$

[0150] In this manner, by controlling the duty signal Sdb under high load, it becomes possible to control a voltage ratio of the input/output DC voltages V0 and V2.

[0151] A step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is small (low load) will now be described below with reference to Fig. 6B.

[0152] An operation in one cycle will be described in order of the zone 8, the zone 9, the zone 7, and the zone 9 in time sequence. In the case of a low load, there is a period during which a current through the inductor L remains 0.

[0153] In the zone 8, because the gate signal G2b is a high signal and therefore the semiconductor switching element S2b is ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

[0154] Capacitor C2 → IGBT of semiconductor switching element S2b → capacitor C1 → diode of semiconductor switching element S1a → inductor L → capacitor C0

[0155] A negative voltage (V0 - V2/2) is applied to the inductor L and the current increases in a negative direction.

[0156] In the zone 9, because all the semiconductor switching elements are OFF, a current flows in a path specified below at the beginning.

Diode of semiconductor switching element S2a → diode of semiconductor switching element S1a → inductor L → capacitor C0

[0157] In this instance, an applied voltage to the inductor L is V0 that is a positive voltage. Hence, an inductor current flowing in a negative direction decreases.

[0158] As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 9 and the current remains 0 for the rest of the period in the zone 9.

[0159] Likewise, in the zone 7, because the gate signal G1b is a high signal and therefore the semiconductor switching element S1b is ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

Diode of semiconductor switching element S2a → capacitor C1 → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0160] A voltage (V0 - V2/2) is applied to the inductor L and a current increases in a negative direction.

[0161] In the zone 9, a current flows in the same manner as described above.

[0162] In this manner, a current-discontinuing operation with which a current through the inductor L becomes 0 at a midpoint in the zone 9 is performed and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0163] Also, a relation between the duty signal Sdb and the input/output DC voltages V0 and V2 will now be described. Firstly, an average current Ildc of the inductor L will be described.

[0164] In the zones 8 and 7, a voltage (V0 - V2/2) is applied to the inductor. With the use of an inductance value L of the inductor, an inductor minimum current Ilmin is expressed by Equation 26 as follows.

$$Ilmin = (V0 - V2/2) \times Ts8/L = -(V2/2 - V0) \times Sdb \times Ts/L \quad \ldots(\text{Equation } 26)$$

[0165] Also, given that a zone 91 is a zone in which a current is flowing through the inductor in the zone 9. Let Ts91 be a time of the zone 91. Then, because the voltage V0 is applied to the inductor in the zone 91 and a current through the inductor eventually becomes 0, Ts91 is expressed by Equation 27 as follows.

$$Ts91 = -L \times Ilmin/V0 = ((V2/2 - V0)/V0) \times Sdb \times Ts \quad \ldots(\text{Equation } 27)$$

[0166] Subsequently, the inductor average current Ildc that is an average current in one cycle of the inductor is expressed by Equation 28 as follows.

$$Ildc = 0.5 \times Ilmin \times ((Ts8 + Ts91) + (Ts7 + Ts91))/Ts = -0.5 \times (V2(V2/2 - V0)/V0) \times Sdb^2 \times Ts/L \quad \ldots(\text{Equation } 28)$$

[0167] Also, power P to be stepped-down from the DC voltage V2 to the stepped-down DC voltage V0 can be expressed by Equation 29 below. Hence, by adjusting an ON-duty (duty signal Sdb) of the semiconductor switching elements S1b and S2b, it becomes possible to adjust the power P.

[0168] Herein, assume that the power P is stepped-down in a normal direction.

$$P = -V0 \times Ildc = 0.5 \times V2(V2/2 - V0) \times Sdb^2 \times Ts/L \quad \ldots(\text{Equation } 29)$$

[0169] In the case of a low load, too, by adjusting an ON-duty (duty signal Sdb) of the semiconductor switching elements S1b and S2b, it becomes possible to control the power P and hence to control a voltage ratio of the DC voltages V0 and V2.

[0170] In this manner, in an operation to step-down the DC voltage V2 to the DC voltage V0 that is less than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V2 → V0), by selecting the switching mode [3] in which an ON-duty of the semiconductor switching elements S1b and S2b is lower than 50% (Sdb < 50%) and an ON-duty of the semiconductor switching elements S1a and S2a is 0% (Sda = 0%), it becomes possible to control a voltage ratio of the DC voltages V0 and V2.

[0171] Also, even when an inductor having a small inductance value is used, a current-discontinuing operation with which an inductor current becomes 0 is performed under low load and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0172] An operation to step-down the DC voltage V2 to the DC voltage V0 that is more than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V2 → V0) in the switching mode [4] will be described using Fig. 7A and Fig. 7B. As are shown in Fig. 7A and Fig. 7B, in the switching mode [4], an ON-duty of the semiconductor switching elements S1b and S2b is higher than 50% (Sdb > 50%) and an ON-duty of the semiconductor switching elements S1a and S2a is 0% (Sda = 0%). Hence, one cycle is made up of the zone 8, the zone 7, and the zone 4 and no other zones are present.

[0173] Also, times Ts8, Ts7, and Ts4 of the zone 8, the zone 7, and the zone 4, respectively, in one switching cycle are expressed as below. For the zone 4 occurring twice in one cycle, Ts4 is a time per occurrence.

$$Ts8 = (1 - Sdb) \times Ts \quad \ldots(\text{Equation } 30)$$

$$Ts7 = (1 - Sdb) \times Ts \quad \ldots(\text{Equation } 31)$$

$$Ts4 = (Ts - Ts8 - Ts7)/2 = (Sdb - 0.5)Ts \quad \ldots(\text{Equation } 32)$$

[0174] Firstly, a step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is large (high load) will be described below with reference to Fig. 7A.

[0175] In the case of a high load, a current in a negative direction is always flowing through the inductor.

[0176] In the zone 4, because the gate signals G1b and G2b are high signals and therefore the semiconductor switching elements S1b and S2b are ON, a current flows in a path specified below and a voltage (VO - V2) is applied to the inductor L.

[0177] Capacitor C2 → IGBT of semiconductor switching element S2b → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0178] In the zone 7, because the gate signal G1b is a high signal and therefore the semiconductor switching element S1b is ON, a current flows in a path specified below and a voltage (VO - V2/2) is applied to the inductor L.

Diode of semiconductor switching element S2a → capacitor C1 → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0179] In the zone 8, because the gate signal G2b is a high signal and therefore the semiconductor switching element S2b is ON, a current flows in a path specified below and a voltage (V0 - V2/2) is applied to the inductor L.

Capacitor C2 → IGBT of semiconductor switching element S2b → capacitor C1 → diode of semiconductor switching element S1a → inductor L → capacitor C0

[0180] A relation between the duty signal Sdb and the input/output DC voltages V0 and V2 will also be described. In a steady state, an average voltage across the inductor L in one switching cycle is 0 and a relation expressed below is established.

$$0 = ((V0 - V2/2) \times (Ts8 + Ts7) + (V0 - V2) \times (2 \times Ts4))/Ts$$

$$V0 = Sdb \times V2 \quad \ldots(\text{Equation } 33)$$

[0181] In this manner, by controlling the duty signal Sdb under high load, it becomes possible to control a voltage ratio of the input/output DC voltages V0 and V2.

[0182] A step-down operation in a case where power to be stepped-down from the DC voltage V2 to the DC voltage V0 is small (low load) will now be described below with reference to Fig. 7B.

[0183] An operation in one cycle will be described in order of the zone 4, the zone 7, the zone 4, and the zone 8 in time sequence. In the case of a low load, there is a period during which a current through the inductor L remains 0.

[0184] In the zone 4, because the gate signals G1b and G2b are high signals and therefore the semiconductor switching elements S1b and S2b are ON, a voltage is applied to the inductor L and a current starts to flow in a path specified in the following.

Capacitor C2 → IGBT of semiconductor switching element S2b → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0185] A negative voltage (V0 - V2) is applied to the inductor L and the current increases in a negative direction.

[0186] In the zone 7, because the gate signal G1b is a high signal and therefore the semiconductor switching element S1b is ON, a current flows in a path specified below at the beginning.

Diode of semiconductor switching element S2a → capacitor C1 → IGBT of semiconductor switching element S1b → inductor L → capacitor C0

[0187] In this instance, an applied voltage to the inductor L is a positive voltage, (V0 - V2/2). Hence, an inductor current flowing in a negative direction decreases. As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 7 and the current remains 0 for the rest of the period in the zone 7.

[0188] In the zone 4, the current flows in the same manner as described above.

[0189] In the zone 8, because the gate signal G2b is a high signal and therefore the semiconductor switching element S2b is ON, a current flows in a path specified below at the beginning.

Capacitor C2 → IGBT of semiconductor switching element S2b → capacitor C1 → diode of semiconductor switching

element S1a → inductor L → capacitor C0

[0190] In this instance, an applied voltage to the inductor L is a positive voltage, (V0 - V2/2), and an inductor current flowing in a negative direction decreases. As the inductor current decreases, the current eventually becomes 0 at a midpoint in the zone 8 and the current remains 0 for the rest of the period in the zone 8.

[0191] In this manner, a current-discontinuing operation with which a current through the inductor L becomes 0 at midpoints in the zone 7 and the zone 8 is performed and losses in the inductor L, the semiconductor switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0192] A relation between the duty signal Sdb and the input/output DC voltages V0 and V2 will now be described. Firstly, an average current Ildc of the inductor L will be described.

[0193] In the zone 4, a voltage (VO - V2) is applied to the inductor L and an inductor minimum current Ilmin is expressed by Equation 34 as follows.

$$Ilmin = (V0 - V2) \times Ts4/L = -(V2 - V0) \times (Sdb - 0.5)Ts/L \quad \ldots(\text{Equation } 34)$$

[0194] Also, given that a zone 71 and a zone 81 are zones in which a current is flowing through the inductor in the zones 7 and 8, respectively. Let Ts71 and Ts81 be times of the zone 71 and the zone 81, respectively. Then, because a voltage (VO - V2/2) is applied to the inductor in the zone 71 and the zone 81 and a current through the inductor eventually becomes 0, Ts71 and Ts81 are expressed by Equation 35 as follows.

$$Ts71 = Ts81 = -L \times Ilmin/(V0 - V2/2) = ((V2/2 - V0)/(V0 - V2/2))(Sdb - 0.5)Ts \quad \ldots(\text{Equation } 35)$$

[0195] Subsequently, an inductor average current Ildc that is an average current in one cycle of the inductor is expressed by Equation 36 as follows.

$$Ildc = 0.5 \times Ilmin \times ((Ts4 + Ts71) + (Ts4 + Ts81))/Ts = -0.5 \times (V2(V2 - V0)/(V0 - V2/2)) \times (Sdb - 0.5)^2 \times Ts/L \quad \ldots(\text{Equation } 36)$$

[0196] Also, power P to be stepped-down from the DC voltage V2 to the stepped-down DC voltage V0 can be expressed by Equation 37 below. Hence, by adjusting an ON-duty (duty signal Sdb) of the semiconductor switching elements S1b and S2b, it becomes possible to adjust the power P.

[0197] Herein, assume that the power P is stepped-down in a normal direction.

$$P = -V0 \times Ildc = 0.5 \times (V0 \times V2(V2 - V0)/(V0 - V2/2)) \times (Sdb - 0.5)^2 \times Ts/L \quad \ldots (\text{Equation } 37)$$

[0198] Even in the case of a low load, too, by adjusting an ON-duty (duty signal Sdb) of the semiconductor switching elements S1b and S2b, it becomes possible to control the power P and hence to control a voltage ratio of the DC voltages V0 and V2.

[0199] In this manner, in an operation to step-down the DC voltage V2 to the DC voltage V0 that is more than 1/2-time the DC voltage V2 (a voltage ratio V2/VO is smaller than 2 and a direction of power transmission is V2 → V0), by selecting the switching mode [4] in which an ON-duty of the semiconductor switching elements S1b and S2b is higher than 50% (Sdb > 50%) and an ON-duty of the semiconductor switching elements S1a and S2a is 0% (Sda = 0%), it becomes possible to control a voltage ratio of the DC voltages V0 and V2.

[0200] Also, even when an inductor having a small inductance value is used, a current-discontinuing operation with which an inductor current becomes 0 is performed under low load and losses in the inductor L, the semiconductor

switching elements S1a, S1b, S2a, and S2b, and the capacitor C1 are lessened.

[0201] For clarity of a function and an advantage of the DC-DC power conversion apparatus according to the first embodiment of the invention, a comparison with an apparatus in the related art will now be described.

[0202] For purpose of comparison, a description will be given to a case where switching operations are performed complementarily as in the related art for an operation to step-up the DC voltage V0 to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/VO is greater than 2 and a direction of power transmission is V0 → V2) with reference to Fig. 8A and Fig. 8B.

[0203] Fig. 8A shows a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is large (high load) and Fig. 8B shows a step-up operation in a case where power to be stepped-up from the DC voltage V0 to the DC voltage V2 is small (low load).

[0204] In a case where complimentary switching operations in the related art are performed, the semiconductor switching elements S1a and S1b perform switching operations complementarily and the semiconductor switching elements S2a and S2b perform switching operations complementarily. As are shown in Fig. 8A and Fig. 8B, one cycle is made up of the zone 1, the zone 2, and the zone 3 and no other zones are present.

[0205] In the zone 1, the voltage V0 is applied to the inductor and a voltage (V0 - V2/2) is applied to the inductor in the zone 2 and the zone 3. Hence, an inductor current is always flowing.

[0206] As is shown in Fig. 8A, as to an operation under high load, a current flowing through the inductor L is the same in the DC-DC power conversion apparatus of the first embodiment and the example of the related art. It should be appreciated, however, that, as is shown in Fig. 8B, a certain ripple current flows through the inductor L even in an operation under low load in the apparatus in the related art.

[0207] Fig. 9 shows power conversion efficiency (broken line A) of the DC-DC power conversion apparatus of the first embodiment and power conversion efficiency (solid line B) of the example in the related art in an operation to step-up the DC voltage V0 to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V0 → V2). As is shown in Fig. 9, when the switching mode [1] is selected, power conversion efficiency of the DC-DC power conversion apparatus of the first embodiment is enhanced when power to be stepped-up is small owing to a current-discontinuing operation with which a current through the inductor becomes 0 in a part of periods. The same applies to the other switching modes.

[0208] As has been described, the DC-DC power conversion apparatus according to the first embodiment of the invention has two or more switching units each of which includes two semiconductor switching elements Sa and Sb performing switching operations, which semiconductor switching elements of the respective switching units are all connected in series, an energy transition capacitor for conducting charging/discharging according to the switching operations of the respective semiconductor switching elements of the respective switching units, and an inductor. The DC-DC power conversion apparatus is provided with a control unit that makes the semiconductor switching elements of the switching units execute switching operations in four types of switching modes, according to a ratio of input/output voltages of the DC-DC power conversion apparatus and a direction of power transmission in the DC-DC power conversion apparatus, and also makes the semiconductor switching elements carry out a current-discontinuing operation wherein a current flowing through the inductor becomes 0 during the switching operations under low load. By performing four types of switching modes (switching modes [1] through [4]), it becomes possible to readily control a voltage ratio of the DC voltages V0 and V2. Also, even when a small inductor having a small inductance value is used, a ripple current through the inductor under low load decreases and therefore losses in the energy transition capacitor C1, the inductor L, and the semiconductor switching elements S1a, S1b, S2a, and S2b can be lessened. It thus becomes possible to increase power conversion efficiency under low load.

[0209] The four types of switching modes (switching modes [1] through [4]) are as follows. Herein, let V0 be one DC voltage of the DC-DC power conversion apparatus and V2 be the other DC voltage.

Switching Mode [1]

[0210] A switching mode in which an ON-duty of one semiconductor switching element Sa of each switching unit is set to 50% or higher when the DC current V0 is stepped-up to the DC voltage V2 that is more than double the DC voltage V0 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V0 → V2).

Switching Mode [2]

[0211] A switching mode in which an ON-duty of one semiconductor switching element Sa of each switching unit is set to 50% or below when the DC current V0 is stepped-up to the DC voltage V2 that is less than double the DC voltage V0 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V0 → V2).

Switching Mode [3]

[0212] A switching mode in which an ON-duty of the other semiconductor switching element Sb of each switching unit is set to 50% or below when the DC current V2 is stepped-down to the DC voltage V0 that is less than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is greater than 2 and a direction of power transmission is V2 → V0).

Switching Mode [4]

[0213] A switching mode in which an ON-duty of the other semiconductor switching element Sb of each switching unit is set to 50% or higher when the DC current V2 is stepped-down to the DC voltage V0 that is more than 1/2-time the DC voltage V2 (a voltage ratio V2/V0 is smaller than 2 and a direction of power transmission is V2 → V0).

[0214] It should be noted that in a case where a voltage ratio V2/V0 is 2, in the DC-DC power conversion apparatus in the related art adopting complementary switching, too, a voltage applied to the inductor L decreases and so does a ripple current through the inductor L. Accordingly, one more switching mode in which complementary switching takes place is added, so that this switching mode in which complementary switching takes place is selected in a case where a voltage ratio V2/V0 is equal to 2.

[0215] In the first embodiment, IGBTs and diodes are used as the semiconductor switching elements. It should be appreciated, however, that other semiconductor switching elements formed of MOSFETs and diodes may be used instead.

[0216] In the case of MOSFETs, synchronous rectification can be achieved by switching ON the MOSFET while a current is flowing through the diode. Hence, it becomes possible to increase power conversion efficiency further.

[0217] Also, Si semiconductors are often used for the semiconductor switching elements. It should be appreciated, however, that wide-gap semiconductors, such as SiC and GaN, can be used as well.

[0218] By using wide-gap semiconductors, such as SiC and GaN, it becomes possible to lessen a conduction loss and a switching loss in the semiconductor switching elements. Hence, it becomes possible to achieve a DC-DC power conversion apparatus with further higher power conversion efficiency.

Second Embodiment

[0219] Fig. 10 is a circuit diagram showing a configuration of a main circuit of a DC-DC power conversion apparatus according to a second embodiment of the invention.

[0220] A DC-DC power conversion apparatus 40 of the second embodiment is a two-way DC-DC power conversion apparatus furnished with a step-up function of converting a DC voltage V0 inputted between a voltage terminal VL and a voltage terminal VN to a stepped-up DC voltage V2 and outputting the DC voltage V2 between a voltage terminal VH and a voltage terminal VN2, and a step-down function of converting the DC voltage V2 inputted between the voltage terminal VH and the voltage terminal VN2 to the stepped-down DC voltage V0 and outputting the DC voltage V0 between the voltage terminal VL and the voltage terminal VN.

[0221] As is shown in Fig. 10, the DC-DC power conversion apparatus 40 of the second embodiment is different from the DC-DC power conversion apparatus 10 of the first embodiment above shown in Fig. 1 in a connection configuration of the main circuit. Hereinafter, connections of the main circuit of the DC-DC power conversion apparatus 40 of the second embodiment will be described in detail.

[0222] Referring to Fig. 10, an emitter terminal of an IGBT forming a semiconductor switching element S1a is connected to a voltage terminal VN and a collector terminal thereof is connected to a high-voltage end terminal of a smoothing capacitor (energy transition capacitor) C10. An emitter terminal of an IGBT forming a semiconductor switching element S1b is connected to a low-voltage end terminal VN2 of the smoothing capacitor (energy transition capacitor) C10 and a collector terminal thereof is connected to the voltage terminal VN.

[0223] An emitter terminal of an IGBT forming a semiconductor switching element S2b is connected to a voltage terminal VM and a collector terminal thereof is connected to a high-voltage end terminal VH of a smoothing capacitor (energy transition capacitor) C11. An emitter terminal of an IGBT forming a semiconductor switching element S2a is connected to a high-voltage terminal of the smoothing capacitor (energy transition capacitor) C10 and a low-voltage end terminal of the smoothing capacitor (energy transition capacitor) C11, and a collector terminal thereof is connected to the voltage terminal VM.

[0224] In the DC-DC power conversion apparatus 40 of the second embodiment, too, the semiconductor switching elements S1a and S1b perform switching operations and form a switching unit SU1.

[0225] Also, the semiconductor switching elements S2a and S2b perform switching operations as well and form a switching unit SU2.

[0226] The low-voltage end terminal of the smoothing capacitor C0 is connected to the voltage terminal VN and the high-voltage end terminal of the smoothing capacitor C0 is connected to the voltage terminal VL.

[0227] The low-voltage end terminal of the smoothing capacitor C2 is connected to the low-voltage end terminal of the smoothing capacitor (energy transition capacitor) C10 and the high-voltage end terminal of the smoothing capacitor C2 is connected to the high-voltage end terminal of the smoothing capacitor (energy transition capacitor) C11.

[0228] The high-voltage end terminal of the smoothing capacitor (energy transition capacitor) C10 and the low-voltage end terminal of the smoothing capacitor (energy transition capacitor) C11 are connected to each other.

[0229] One terminal of the inductor L is connected to the voltage terminal VL and the other terminal thereof is connected to the voltage terminal VM. Herein, the smoothing capacitor C2 is used. However, because a series body of the smoothing capacitors (energy transition capacitors) C10 and C11 is connected to the smoothing capacitor C2 in parallel, the smoothing capacitor C2 may be eliminated. The smoothing capacitor C10 and the smoothing capacitor C11 divide a voltage V2 between the voltage terminals VH and VN2 into two halves. Hence, V2/2 is given as a voltage across each of the capacitors C10 and C11.

[0230] A gate terminal of the semiconductor switching element S1b is connected to an output terminal of a gate drive circuit 101b and a gate signal G1b is inputted into an input terminal of the gate drive circuit 101b. A gate terminal of the semiconductor switching element S1a is connected to an output terminal of a gate drive circuit 101a and a gate signal G1a is inputted into an input terminal of the gate drive circuit 101a. A gate terminal of the semiconductor switching element S2b is connected to an output terminal of a gate drive circuit 102b and a gate signal G2b is inputted into an input terminal of the gate drive circuit 102b. A gate terminal of the semiconductor switching element S2a is connected to an output terminal of a gate drive circuit 102a and a gate signal G2a is inputted into an input terminal of the gate drive circuit 102a.

[0231] A control unit of the DC-DC power conversion apparatus 40 of the second embodiment is the same as the control unit of the DC-DC power conversion apparatus 10 of the first embodiment above in configuration and operation.

[0232] In the respective switching modes [1] through [4], a voltage across the inductor L is the same as that in the DC-DC power conversion apparatus of the first embodiment above and a current flowing through the inductor L is also the same.

[0233] Accordingly, the DC-DC power conversion apparatus of the second embodiment can also obtain the advantage same as that obtained by the DC-DC power conversion apparatus of the first embodiment above.

Industrial Applicability

[0234] The invention is effectively used for a DC-DC power conversion apparatus that converts a DC voltage to a stepped-up or stepped-down DC voltage.

Description of Reference Numerals and Signs

[0235]

C0 through C2, C10, and C11: capacitor
S1a, S1b, S2a, and S2b: semiconductor switching element
SU1 and SU2: switching unit
L: inductor
G1a, G1b, G2a, and G2b: gate signal
VH, VL VN, VN2, and VM: voltage terminal
101a, 101b, 102a, and 102b: gate drive circuit
310: switching mode output portion
320: PWM waveform output portion
330: step-up/down discrimination portion
340: computation portion
Sda, Sdb, and Sd: duty signal

Claims

1. A DC-DC power conversion apparatus which is a two-way DC-DC power conversion apparatus furnished with a step-up function of converting a DC voltage V0 inputted between low-voltage end terminals (VL, VN) to a stepped-up DC voltage V2 and outputting the DC voltage V2 between high-voltage end terminals (VH, VN), and a step-down function of converting the DC voltage V2 inputted between the high-voltage end terminals (VH, VN) to the stepped-down DC voltage V0 and outputting the DC voltage V0 between the low-voltage end terminals (VL, VN),
the DC-DC power conversion apparatus including two or more switching units (SU1, SU2) each of which includes

two semiconductor switching elements (Sa and Sb) for performing switching operations, which semiconductor switching elements (Sla, S2a, S1b, S2b) of the respective switching units are all connected in series, an energy transition capacitor (C1) for conducting charging/discharging according to the switching operations of the respective semiconductor switching elements (Sa and Sb) of the respective switching units, and an inductor (L) which is connected between a junction point of the semiconductor switching elements (Sa, Sb) constituting the switching units and one end of the low-voltage end terminals (VL), so as to be serially connected to the energy transition capacitor through the semiconductor switching elements of the switching unit,
the DC-DC power conversion apparatus further comprising:

a control unit configured to make the semiconductor switching elements (Sla, S2a, S1b, S2b) of the switching units (SU1, SU2) execute switching operations in four types of switching modes, according to a ratio of input/output voltages of the DC-DC power conversion apparatus and a direction of power transmission in the DC-DC power conversion apparatus, and also arranged to make the semiconductor switching elements (Sa and Sb) carry out a current-discontinuing operation wherein a current flowing through the inductor becomes 0 during the switching operations under low load,
said four types of switching modes including a first switching mode of a step-up operation with the input/output voltage ratio being greater than a predetermined value, a second switching mode of a step-up operation with the input/output ratio being smaller than the predetermined value, a third switching mode of a step-down operation with the input/output voltage ratio being greater than a predetermined value, and a fourth switching mode of a step down operation with the input/output switching ratio being smaller than the predetermined value for the above step down operation;
wherein said predetermined value is 2;
wherein said control unit is configured to make the semiconductor switching elements carry out said current-discontinuing operation by adjusting, in each of the switching modes, the ON-duties of one semiconductor switching element Sa and the other semiconductor switching element Sb in each of the respective switching units, with reference to 50% and 0%;
characterized in that the control unit is configured to make the semiconductor switching elements (S1a, S2a, S1b, S2b) of the switching units execute complementary switching, wherein the semiconductor switching elements (S1a, S1b) of a first switching unit (SU1) of the two or more switching units perform switching complementarily and the semiconductor switching elements (S2a, S2b) of a second switching unit (SU2) of the two or more switching units perform switching complementarily, when an input/output voltage ratio V2/V0 of the DC-DC power conversion apparatus is 2;
and wherein at least one of:

the control unit is configured to set an ON-duty of one semiconductor switching element (S1a, S2a) of each switching unit to 50% or higher, while it sets an ON-duty of the other semiconductor switching element (S1b, S2b) to 0%, for a step-up operation when an input/output voltage ratio V2/V0 of a low-voltage end DC voltage V0 and a high-voltage end DC voltage V2 of the DC-DC power conversion apparatus is greater than 2 and the direction of power transmission is from the low-voltage end DC voltage V0 to the high-voltage end DC voltage V2;
the control unit is configured to set an ON-duty of one semiconductor switching element (S1a, S2a) of each switching unit to 50% or below, while it sets an ON-duty of the other semiconductor switching element (S1b, S2b) to 0%, for a step-up operation when an input/output voltage ratio V2/V0 of the DC-DC power conversion apparatus is smaller than 2 and the direction of power transmission is from a low-voltage end DC voltage V0 to a high-voltage end DC voltage V2;
the control unit is configured to set an ON-duty of one semiconductor switching element (S1b, S2b) of each switching unit to 50% or below, while it sets an ON-duty of the other semiconductor switching element (S1a, S2a) to 0%, for a step-down operation when an input/output voltage ratio V2/V0 of the DC-DC power conversion apparatus is greater than 2 and the direction of power transmission is from a high-voltage end DC voltage V2 to a low-voltage end DC voltage V0; and
the control unit is configured to set an ON-duty of one semiconductor switching element (S1b, S2b) of each switching unit to 50% or higher, while it sets an ON-duty of the other semiconductor switching element (S1a, S2a) to 0%, for a step-down operation when an input/output voltage ratio V2/V0 of the DC-DC power conversion apparatus is smaller than 2 and the direction of power transmission is from a high-voltage end DC voltage V2 to a low-voltage end DC voltage V0.

2. The DC-DC power conversion apparatus according to claim 1, wherein:
the semiconductor switching elements are wide-gap semiconductors including SiC and GaN.

Patentansprüche

1. Eine DC-DC-Leistungsumwandlungsvorrichtung, die eine bidirektionale DC-DC-Leistungsumwandlungsvorrichtung ist, die mit einer Hinauftransformationsfunktion ausgestattet ist, um eine zwischen Niederspannungs-Endklemmen (VL, VN) eingegebene Gleichspannung V0 in eine hinauftransformierte Gleichspannung V2 umzuwandeln und die Gleichspannung V2 zwischen Hochspannungs-Endklemmen (VH, VN) auszugeben, und einer Herabtransformationsfunktion, um die zwischen den Hochspannungs-Endklemmen (VH, VN) eingegebene Gleichspannung V2 in die herabtransformierte Gleichspannung V0 umzuwandeln und die Gleichspannung V0 zwischen den Niederspannungs-Endklemmen (VL, VN) auszugeben,
wobei die DC-DC-Leistungsumwandlungsvorrichtung zwei oder mehrere Schalteinheiten (SU1, SU2), von denen jede zwei Halbleiter-Schaltelemente (Sa und Sb) zum Durchführen von Schaltvorgängen beinhaltet, wobei die Halbleiter-Schaltelemente (Sla, S2a, S1b, S2b) der jeweiligen Schalteinheiten alle in Reihe geschaltet sind, einen Energieumwandlungskondensator (C1) zum Durchführen des Ladens/Entladens gemäß den Schaltvorgängen der jeweiligen Halbleiter-Schaltelemente (Sa und SB) der jeweiligen Schalteinheiten, und einen Induktor (L) beinhaltet, der zwischen einem den Schalteinheiten bildenden Knotenpunkt der Halbleiter-Schaltelemente (Sa, Sb) und einem Ende der Niederspannungs-Endklemmen (VL) verbunden ist, um in Reihe mit dem Energieumwandlungskondensator durch die Halbleiter-Schaltelemente der Schalteinheit verbunden zu sein,
wobei die DC-DC-Leistungsumwandlungsvorrichtung zusätzlich umfasst:

eine Steuereinheit, die konfiguriert ist, die Halbleiter-Schaltelemente (Sla, S2a, S1b, S2b) der Schalteinheiten (SU1, SU2) dazu zu veranlassen, Schaltvorgänge in vier Arten von Schaltmodi auszuführen, gemäß einem Verhältnis von Eingangs-/Ausgangsspannungen der DC-DC-Leistungsumwandlungsvorrichtung und einer Richtung von Leistungsübertragung in der DC-DC-Leistungsumwandlungsvorrichtung, und auch so ausgebildet ist, die Halbleiter-Schaltelemente (Sa und Sb) dazu zu veranlassen, einen Stromunterbrechungsvorgang durchzuführen, wobei ein durch den Induktor fließender Strom während den Schaltvorgängen unter niedriger Last 0 wird,
die vier Arten von Schaltmodi einschließlich einem ersten Schaltmodus eines Hinaufvorgangs mit dem Eingangs-/Ausgangsspannungsverhältnis größer als einem vorbestimmten Wert, einem zweiten Schaltmodus eines Hinaufvorgangs mit dem Eingangs-/Ausgangsverhältnis kleiner als dem vorbestimmten Wert, einem dritten Schaltmodus eines Herabvorgangs mit dem Eingangs-/Ausgangsspannungsverhältnis größer als einem vorbestimmten Wert, und einem vierten Schaltmodus eines Herabvorgangs mit dem Eingangs-/Ausgangsschaltverhältnis kleiner als dem vorbestimmten Wert für den obigen Herabvorgang;
wobei der vorbestimmte Wert 2 ist;
wobei die Steuereinheit konfiguriert ist, die Halbleiter-Schaltelemente dazu zu veranlassen, den Stromunterbrechungsvorgang auszuführen, durch Einstellen, in jedem der Schaltmodi, der Einschaltzeitverhältnisse von einem Halbleiter-Schaltelement Sa und dem anderen Halbleiter-Schaltelement Sb in jeder der jeweiligen Schalteinheiten, mit Bezug auf 50% und 0%;
dadurch gekennzeichnet, dass
die Steuereinheit konfiguriert ist, die Halbleiter-Schaltelemente (Sla, S2a, S1b, S2b) der Schalteinheiten dazu zu veranlassen, ein komplementäres Schalten auszuführen, wobei die Halbleiter-Schaltelemente (Sla, S1b) einer ersten Schalteinheit (SU1) der zwei oder mehreren Schalteinheiten Schalten komplementär durchführen und die Halbleiter-Schaltelemente (S2a, S2b) einer zweiten Schalteinheit (SU2) der zwei oder mehreren Schalteinheiten Schalten komplementär durchführen, wenn ein Eingangs-/Ausgangsspannungsverhältnis V2/V0 der DC-DC-Leistungsumwandlungsvorrichtung 2 ist;
und wobei mindestens eine der:

Steuereinheit konfiguriert ist zum Setzen eines Einschaltverhältnisses eines Halbleiter-Schaltelements (Sla, S2a) von jeder Schalteinheit auf 50% oder höher, während sie ein Einschaltzeitverhältnis des anderen Halbleiterschaltelements (S1b, S2b) auf 0% setzt, für einen Hinaufvorgang, wenn ein Eingangs-/Ausgangsspannungsverhältnis V2/V0 einer am Niederspannungsende liegenden Gleichspannung V0 und einer am Hochspannungsende liegenden Gleichspannung V2 der DC-DC-Leistungsumwandlungsvorrichtung größer als 2 ist und die Richtung einer Leistungsübertragung von der am Niederspannungsende liegenden Gleichspannung V0 zu der am Hochspannungsende liegenden Gleichspannung V2 ist;
Steuereinheit konfiguriert ist zum Setzen eines Einschaltzeitverhältnisses eines Halbleiter-Schaltelements (Sla, S2a) von jeder Schalteinheit auf 50% oder niedriger, während sie ein Einschaltzeitverhältnis des anderen Halbleiterschaltelements (S1b, S2b) auf 0% setzt, für einen Hinaufvorgang, wenn ein Eingangs-/Ausgangsspannungsverhältnis V2/V0 der DC-DC-Leistungsumwandlungsvorrichtung kleiner als 2 ist und die Richtung einer Leistungsübertragung von einer am Niederspannungsende liegenden Gleich-

spannung V0 zu einer am Hochspannungsende liegenden Gleichspannung V2 ist;
Steuereinheit konfiguriert ist zum Setzen eines Einschaltzeitverhältnisses eines Halbleiter-Schaltelements (Sla, S2a) von jeder Schalteinheit auf 50% oder niedriger, während sie ein Einschaltzeitverhältnis des anderen Halbleiterschaltelements (S1b, S2b) auf 0% setzt, für einen Herabvorgang, wenn ein Eingangs-/Ausgangsspannungsverhältnis V2/V0 der DC-DC-Leistungsumwandlungsvorrichtung größer als 2 ist und die Richtung einer Leistungsübertragung von einer am Hochspannungsende liegenden Gleichspannung V0 zu einer am Niederspannungsende liegenden Gleichspannung V2 ist; und
der Steuereinheit konfiguriert ist zum Setzen eines Einschaltzeitverhältnisses eines Halbleiter-Schaltelements (S1b, S2b) von jeder Schalteinheit auf 50% oder höher, während sie ein Einschaltzeitverhältnis des anderen Halbleiterschaltelements (Sla, S2a) auf 0% setzt, für einen Herabvorgang, wenn ein Eingangs-/Ausgangsspannungsverhältnis V2/V0 der DC-DC-Leistungsumwandlungsvorrichtung kleiner als 2 ist und die Richtung einer Leistungsübertragung von einer am Hochspannungsende liegenden Gleichspannung V2 zu einer am Niederspannungsende liegenden Gleichspannung V0 ist.

2. Die DC-DC-Leistungsumwandlungsvorrichtung gemäß Anspruch 1, wobei:
die Halbleiter-Schaltelemente Halbleiter mit breitem Abstand einschließlich SiC und GaN sind.

Revendications

1. Appareil de conversion de courant CC-CC qui est un appareil de conversion de courant CC-CC bidirectionnel doté d'une fonction de survoltage pour convertir une tension CC V0 saisie entre des bornes terminales de basse tension (VL, VN) en une tension CC survoltée V2 et pour délivrer la tension CC V2 entre des bornes terminales de haute tension (VH, VN), et d'une fonction de dévoltage pour convertir la tension CC V2 saisie entre les bornes terminales de haute tension (VH, VN) en la tension CC dévoltée V0 et de délivrance de la tension CC V0 entre les bornes terminales de basse tension (VL, VN),
l'appareil de conversion de courant CC-CC incluant deux ou plus d'unités de commutation (SU1, SU2) dont chacune inclut deux éléments de commutation à semi-conducteurs (Sa et Sb) pour effectuer des opérations de commutation, lesquels éléments de commutation à semi-conducteurs (Sla, S2a, S1b, S2b) des unités de commutation respectives sont tous connectés en série, un condensateur de transition de courant (C1) pour conduire le chargement/déchargement conformément aux opérations de commutation des éléments de commutation à semi-conducteurs respectifs (Sa et Sb) des unités de commutation respectives, et un inducteur (L) qui est connecté entre un point de jonction des éléments de commutation à semi-conducteurs (Sa, Sb) constituant les unités de commutation et une extrémité des bornes terminales de basse tension (VL) de manière à être connectés en série au condensateur de transition de courant à travers les éléments de commutation à semi-conducteurs de l'unité de commutation,
l'appareil de conversion de courant CC-CC comprenant en outre :

une unité de commande configurée pour faire en sorte que les éléments de commutation à semi-conducteurs (Sla, S2a, S1b, S2b) des unités de commutation (SU1, SU2) exécutent des opérations de commutation dans quatre types de modes de commutation, conformément à un rapport de tensions d'entrée/sortie de l'appareil de conversion de courant CC-CC et à une direction de transmission de courant dans l'appareil de conversion de courant CC-CC, et également agencée pour faire en sorte que les éléments de commutation à semi-conducteurs (Sa et Sb) effectuent une opération d'interruption de courant dans laquelle un courant s'écoulant à travers l'inducteur devient 0 au cours des opérations de commutation à basse charge,
lesdits quatre types de modes de commutation incluant un premier mode de commutation d'une opération de survoltage avec le rapport des tensions d'entrée/sortie étant supérieur à une valeur prédéterminée, un deuxième mode de commutation d'une opération de survoltage avec le rapport d'entrée/sortie étant inférieur à la valeur prédéterminée, un troisième mode de commutation d'une opération de dévoltage avec le rapport des tensions d'entrée/sortie étant supérieur à une valeur prédéterminée et un quatrième mode de commutation d'une opération de dévoltage avec le rapport de commutation d'entrée/sortie étant inférieur à la valeur prédéterminée pour l'opération de dévoltage précitée ;
dans lequel ladite valeur prédéterminée est de 2 ;
dans lequel ladite unité de commande est configurée pour faire en sorte que les éléments de commutation à semi-conducteurs effectuent ladite opération d'interruption de courant en ajustant, dans chacun des modes de commutation, les conduites d'un élément de commutation à semi-conducteurs Sa et de l'autre élément de commutation à semi-conducteurs Sb dans chacune des unités de commutation respectives, en se référant à 50 % et à 0 % ;
caractérisé en ce que

l'unité de commande est configurée pour faire en sorte que les éléments de commutation à semi-conducteurs (Sla, S2a, S1b, S2b) des unités de commutation exécutent une commutation complémentaire, dans lequel les éléments de commutation à semi-conducteurs (S1a, S1b) d'une première unité de commutation (SU1) des deux ou plus d'unités de commutation effectuent une commutation de manière complémentaire et les éléments de commutation à semi-conducteurs (S2a, S2b) d'une seconde unité de commutation (SU2) des deux ou plus d'unités de commutation effectuent une commutation de manière complémentaire lorsqu'un rapport de tensions d'entrée/sortie V2/V0 de l'appareil de conversion de courant CC-CC est de 2 ;
et dans lequel au moins l'une des situations suivantes :

l'unité de commande est configurée pour régler une conduite d'un élément de commutation à semi-conducteurs (Sla, S2a) de chaque unité de commutation à 50 % ou plus, tandis qu'elle règle une conduite de l'autre élément de commutation à semi-conducteurs (S1b, S2b) à 0 % pour une opération de survoltage lorsqu'un rapport de tensions d'entrée/sortie V2/V0 d'une tension CC d'extrémité de basse tension V0 et d'une tension CC d'extrémité de haute tension V2 de l'appareil de conversion de courant CC-CC est supérieur à 2 et que la direction de transmission de courant va de la tension CC d'extrémité de basse tension V0 à la tension CC d'extrémité de haute tension V2 ;
l'unité de commande est configurée pour régler une conduite d'un élément de commutation à semi-conducteurs (Sla, S2a) de chaque unité de commutation à 50 % ou moins, tandis qu'elle règle une conduite de l'autre élément de commutation à semi-conducteurs (S1b, S2b) à 0 % pour une opération de survoltage lorsqu'un rapport de tensions d'entrée/sortie V2/V0 de l'appareil de conversion de courant CC-CC est inférieur à 2 et que la direction de transmission de courant va d'une tension CC d'extrémité de basse tension V0 à une tension CC d'extrémité de haute tension V2;
l'unité de commande est configurée pour régler une conduite d'un élément de commutation à semi-conducteurs (S1b, S2b) de chaque unité de commutation à 50 % ou moins, tandis qu'elle règle une conduite de l'autre élément de commutation à semi-conducteurs (Sla, S2a) à 0 % pour une opération de dévoltage lorsqu'un rapport de tensions d'entrée/sortie V2/V0 de l'appareil de conversion de courant CC-CC est supérieur à 2 et que la direction de transmission de courant va d'une tension CC d'extrémité de haute tension V2 à une tension CC d'extrémité de basse tension V0 ; et
l'unité de commande est configurée pour régler une conduite d'un élément de commutation à semi-conducteurs (S1b, S2b) de chaque unité de commutation à 50 % ou plus, tandis qu'elle règle une conduite de l'autre élément de commutation à semi-conducteurs (Sla, S2a) à 0 % pour une opération de dévoltage lorsqu'un rapport de tensions d'entrée/sortie V2/V0 de l'appareil de conversion de courant CC-CC est inférieur à 2 et que la direction de transmission de courant va d'une tension CC d'extrémité de haute tension V2 à une tension CC d'extrémité de basse tension V0.

2. Appareil de conversion de courant CC-CC selon la revendication 1, dans lequel :
les éléments de commutation à semi-conducteurs sont des semi-conducteurs à bande large incluant SiC et GaN.

FIG.1

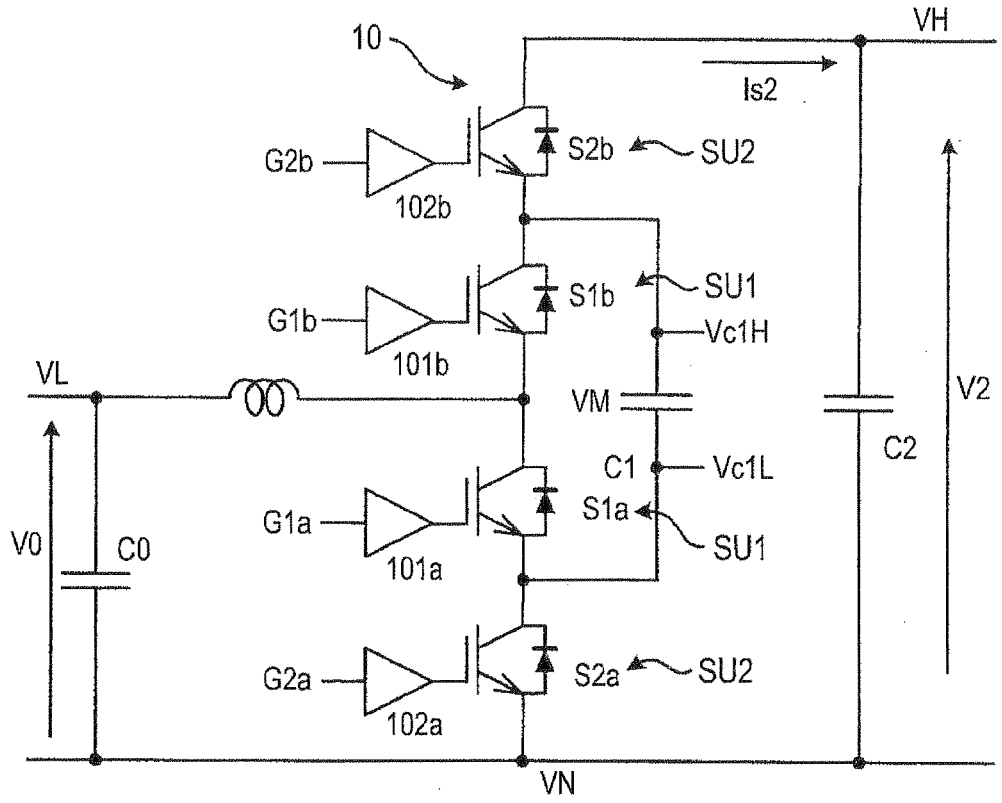


FIG.2

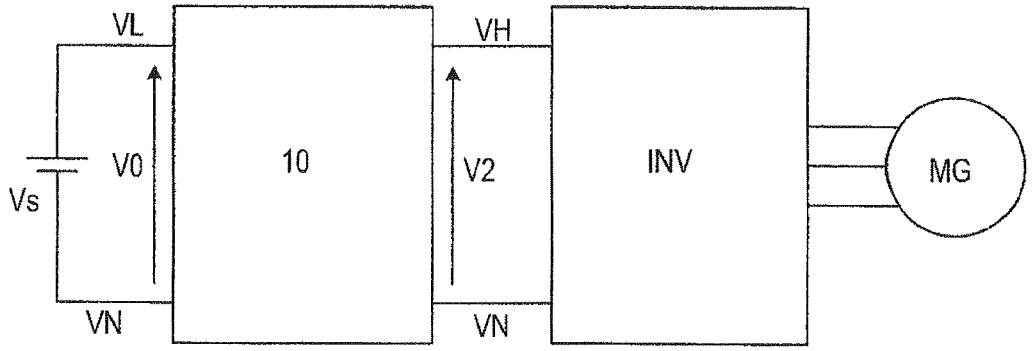


FIG.3

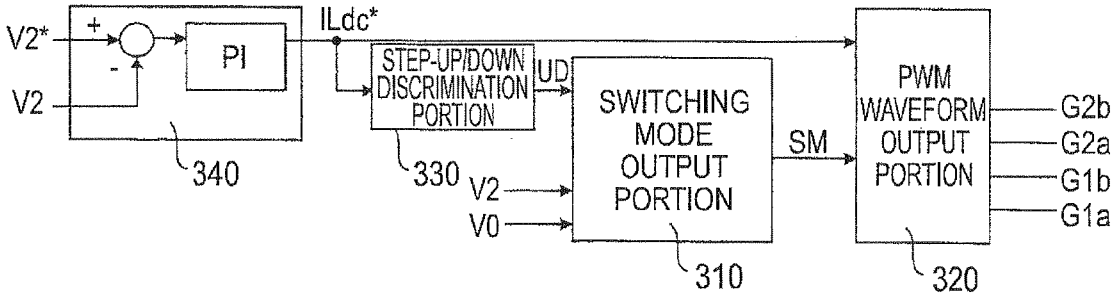


FIG.4A

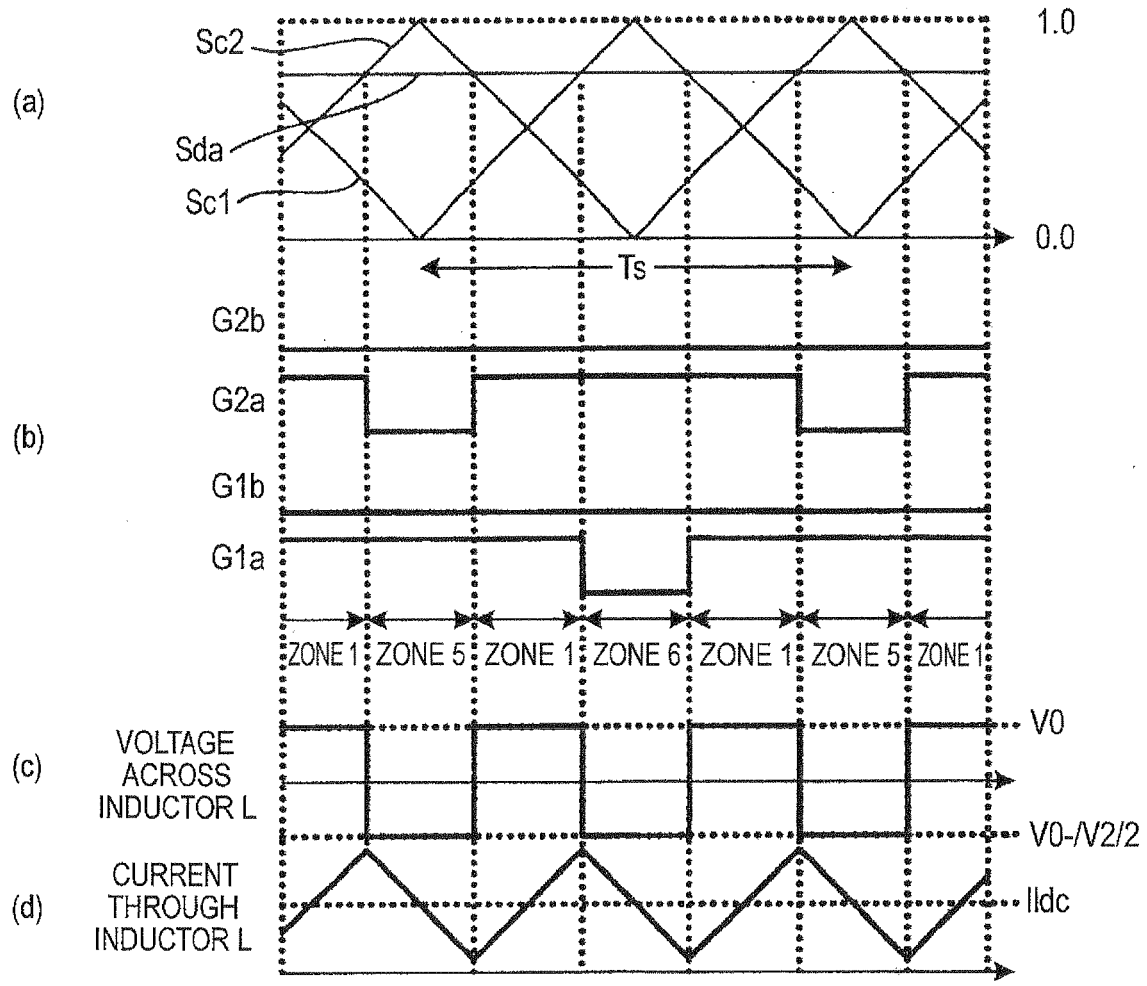

(a)
Sc2
Sda
Sc1
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 1
ZONE 5
ZONE 1
ZONE 6
ZONE 1
ZONE 5
ZONE 1
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.4B

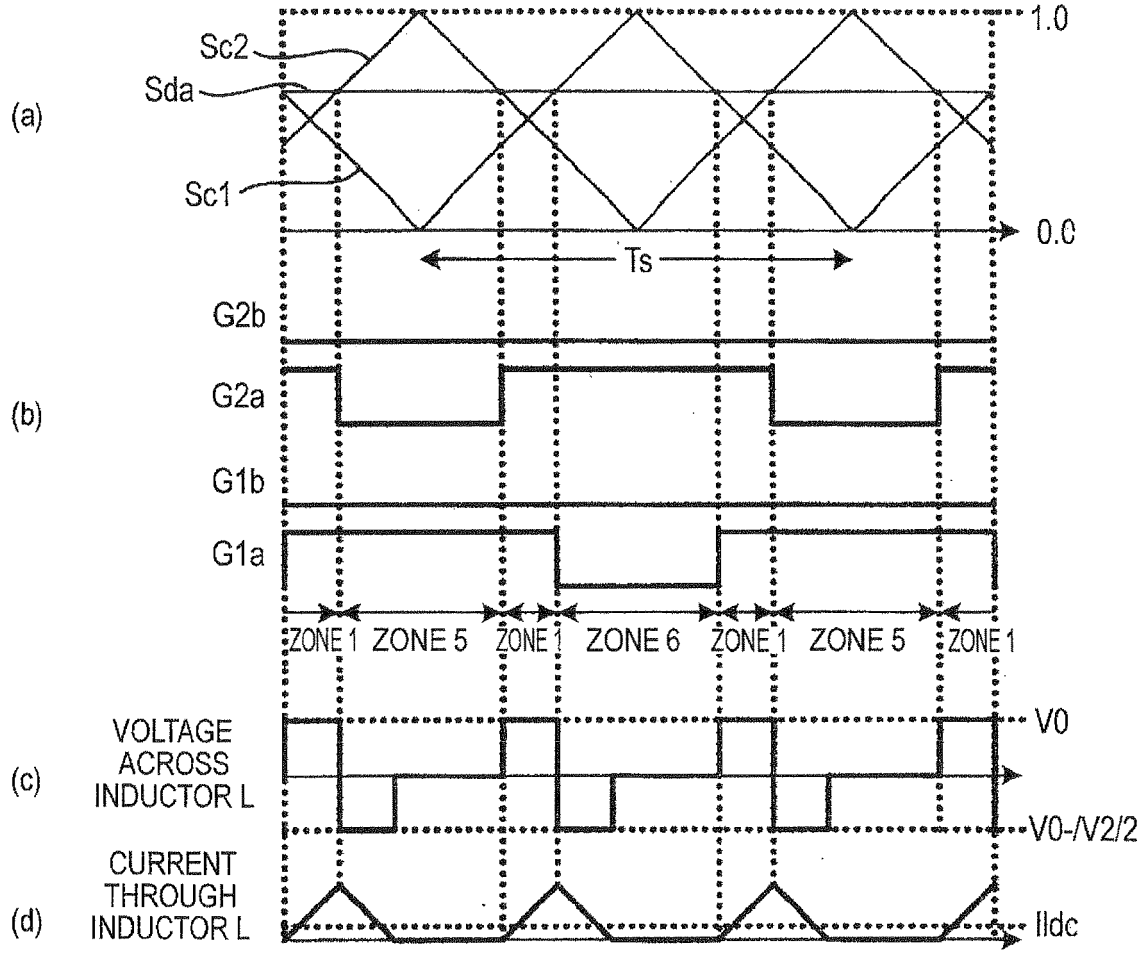

(a)
Sc2
Sda
Sc1
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 1
ZONE 5
ZONE 1
ZONE 6
ZONE 1
ZONE 5
ZONE 1
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.5A

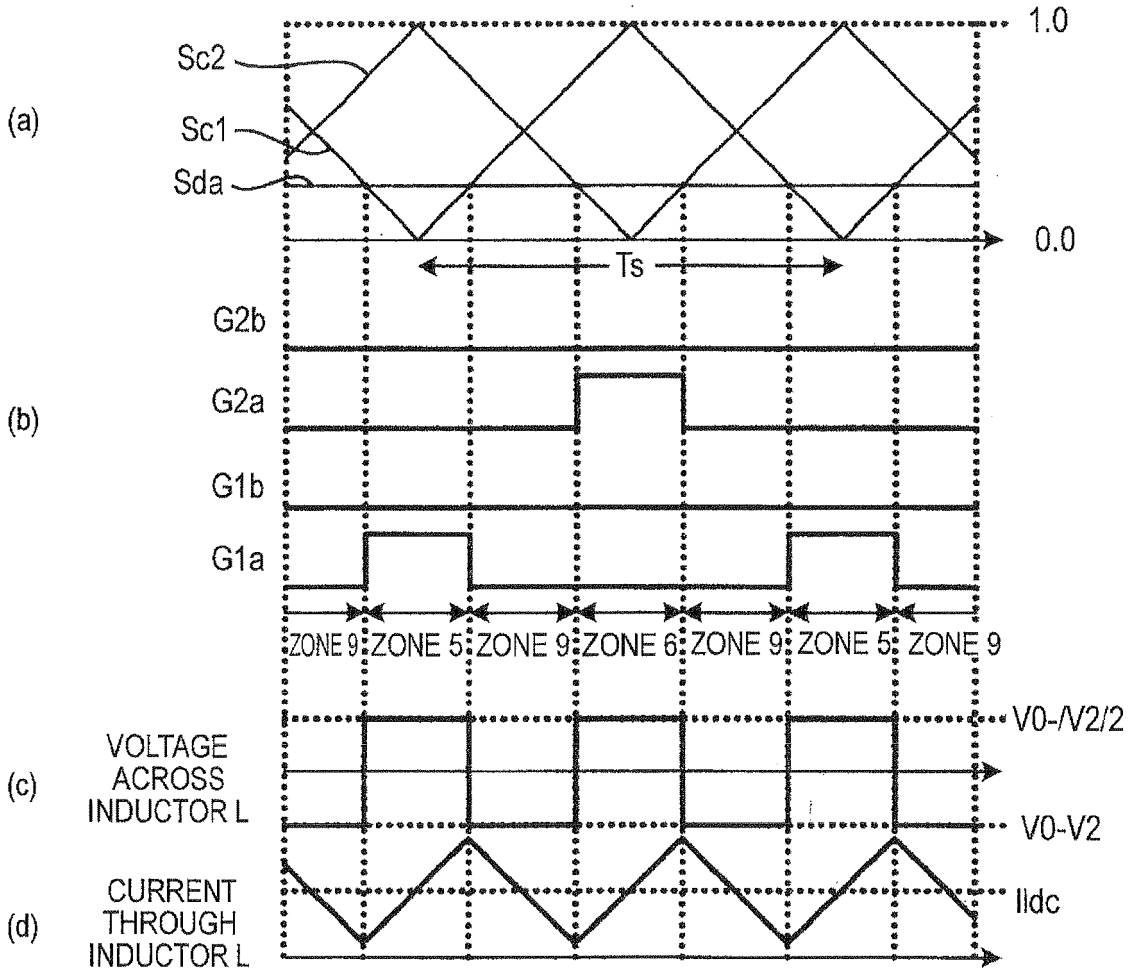

(a)
Sc2
Sc1
Sda
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 9
ZONE 5
ZONE 9
ZONE 6
ZONE 9
ZONE 5
ZONE 9
(c)
VOLTAGE ACROSS INDUCTOR L
V0-/V2/2
V0-V2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.5B

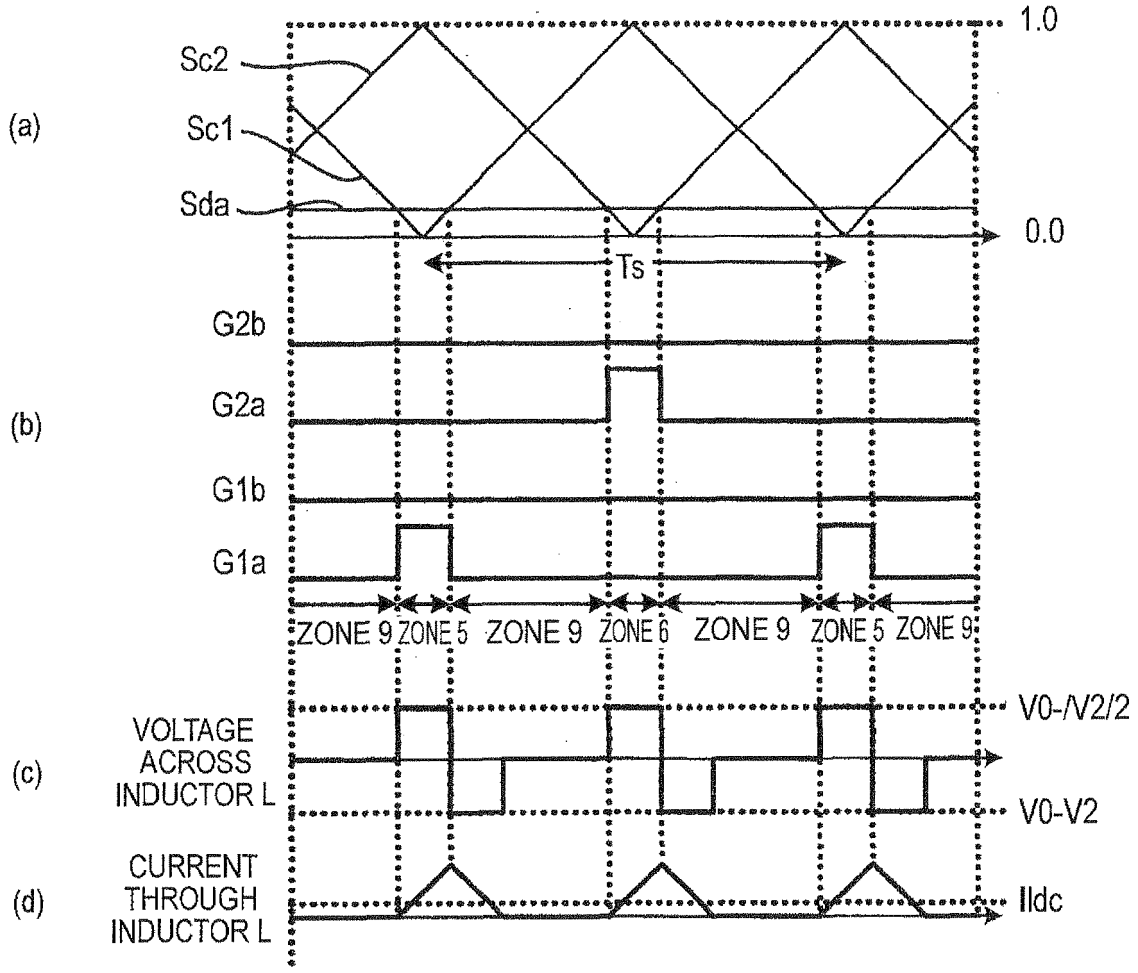

(a)
Sc2
Sc1
Sda
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 9
ZONE 5
ZONE 9
ZONE 6
ZONE 9
ZONE 5
ZONE 9
(c)
VOLTAGE ACROSS INDUCTOR L
V0-/V2/2
V0-V2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.6A

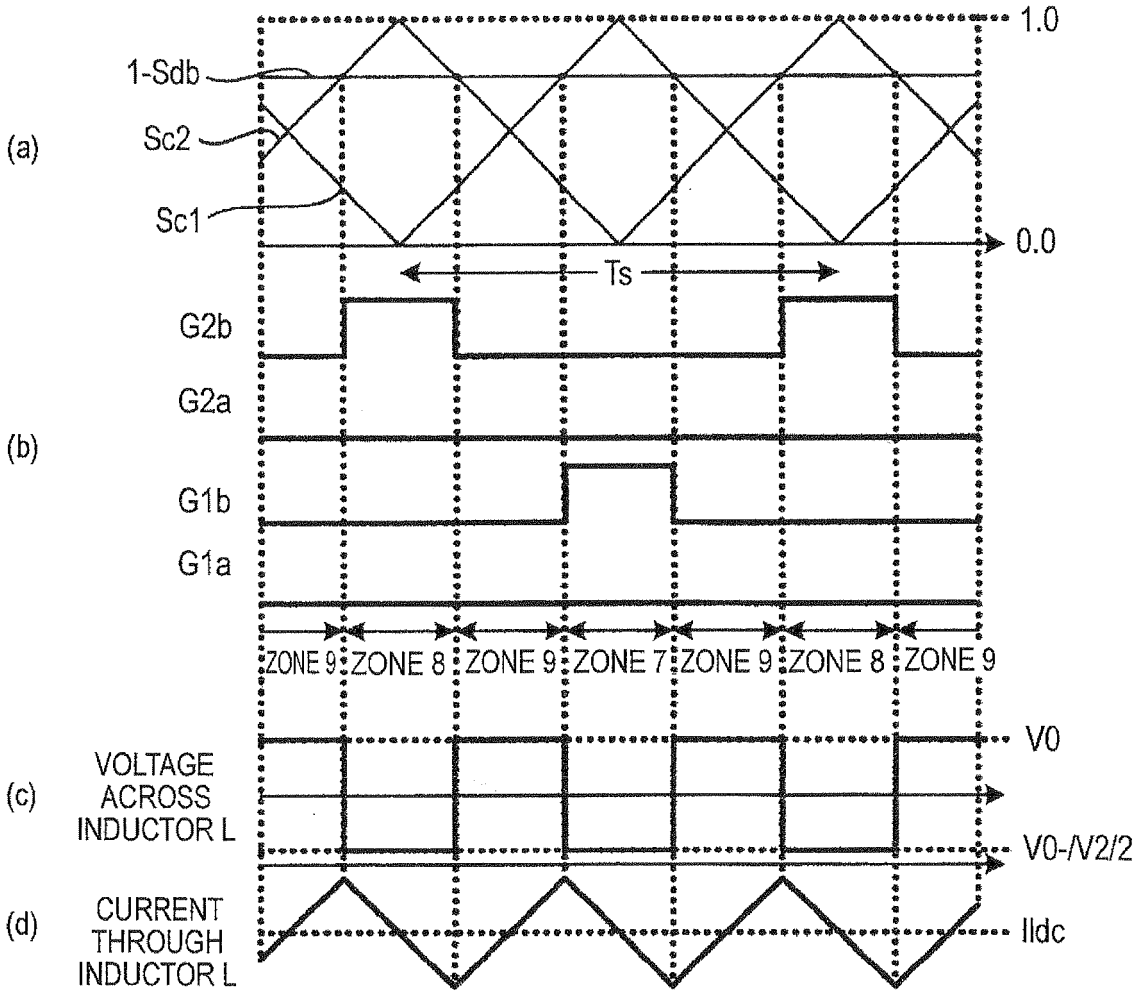

(a)
1-Sdb
Sc2
Sc1
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 9
ZONE 8
ZONE 9
ZONE 7
ZONE 9
ZONE 8
ZONE 9
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.6B

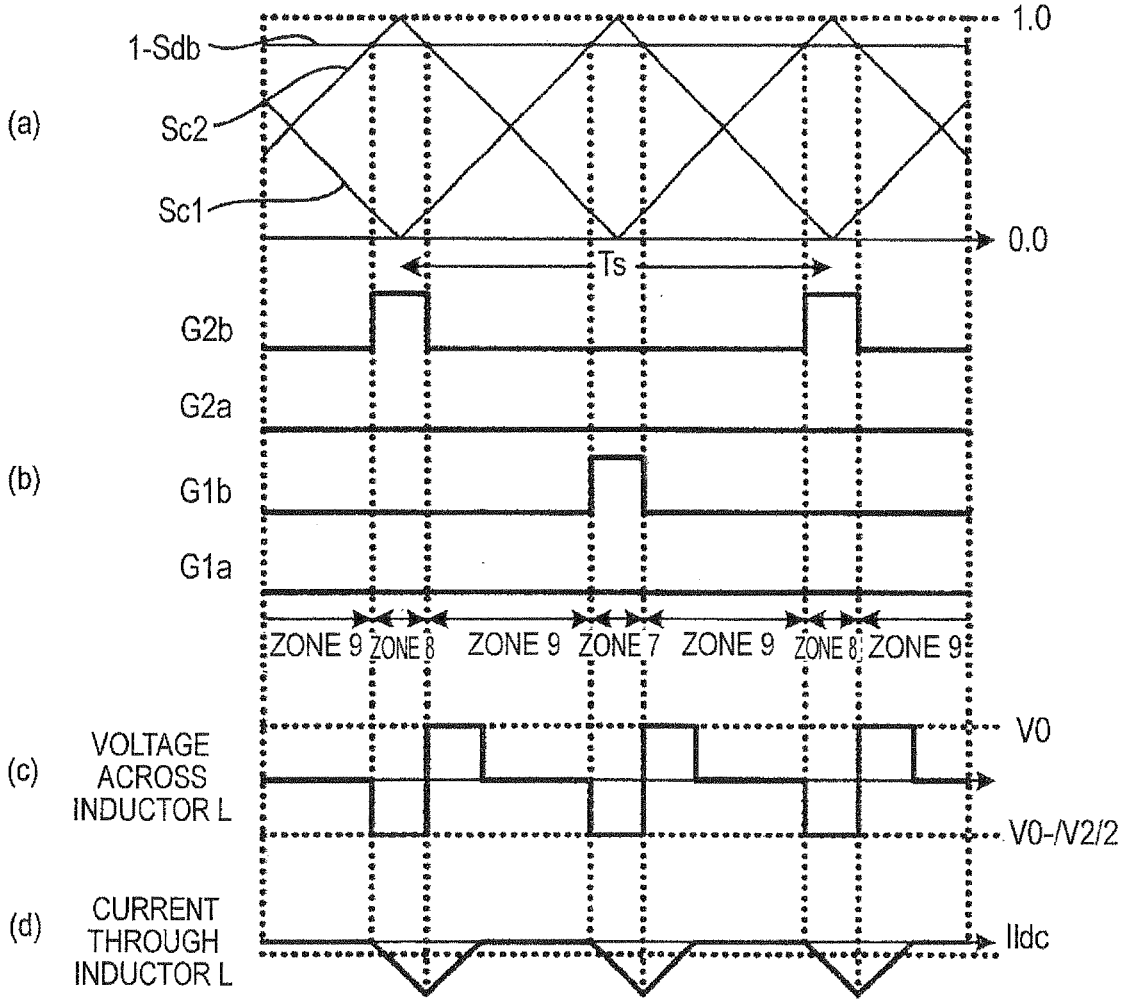

(a)
1-Sdb
Sc2
Sc1
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 9
ZONE 8
ZONE 9
ZONE 7
ZONE 9
ZONE 8
ZONE 9
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.7A

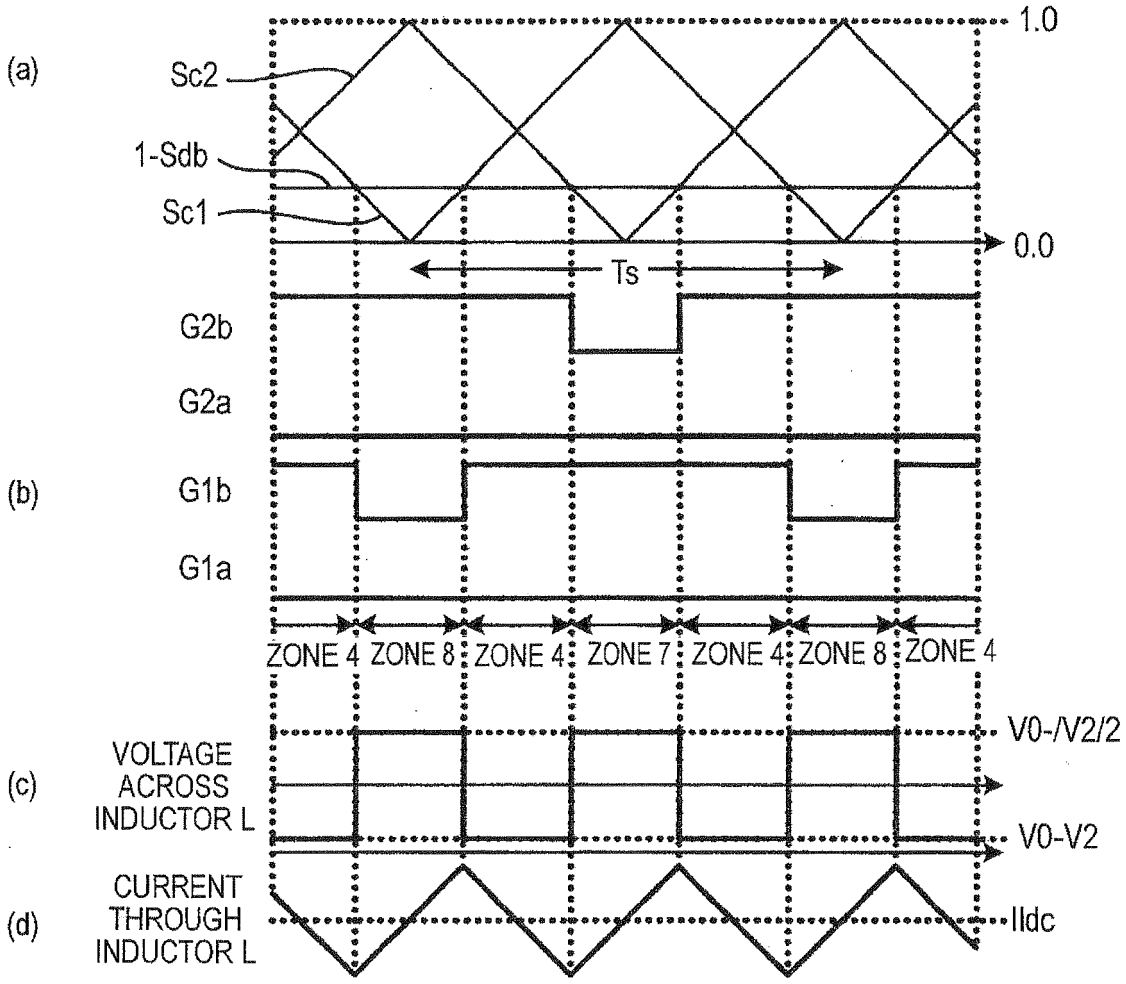

(a)
Sc2
1-Sdb
Sc1
1.0
0.0
Ts
G2b
G2a
(b)
G1b
G1a
ZONE 4
ZONE 8
ZONE 4
ZONE 7
ZONE 4
ZONE 8
ZONE 4
V0-/V2/2
(c)
VOLTAGE ACROSS INDUCTOR L
V0-V2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.7B

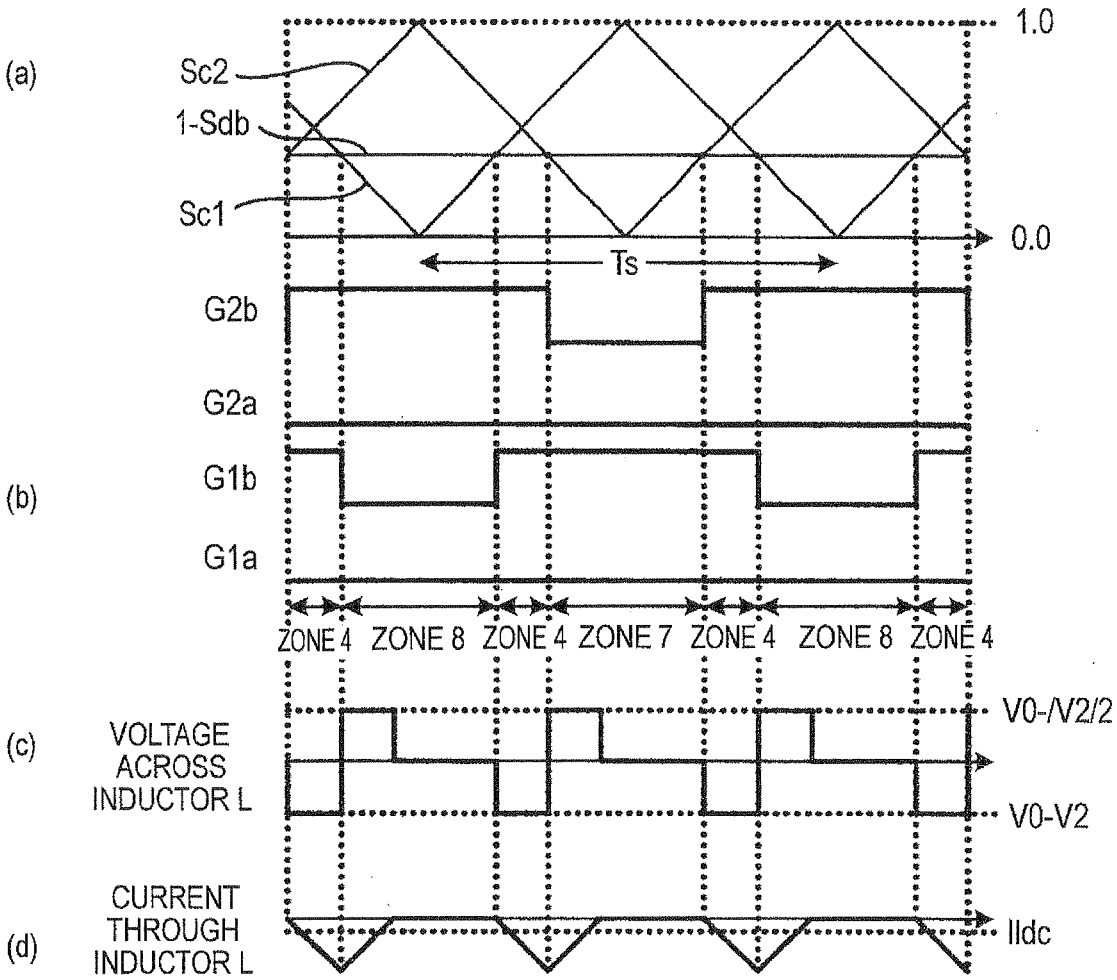

(a)
Sc2
1-Sdb
Sc1
1.0
0.0
Ts
G2b
G2a
(b)
G1b
G1a
ZONE 4
ZONE 8
ZONE 4
ZONE 7
ZONE 4
ZONE 8
ZONE 4
(c)
VOLTAGE ACROSS INDUCTOR L
V0-/V2/2
V0-V2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.8A

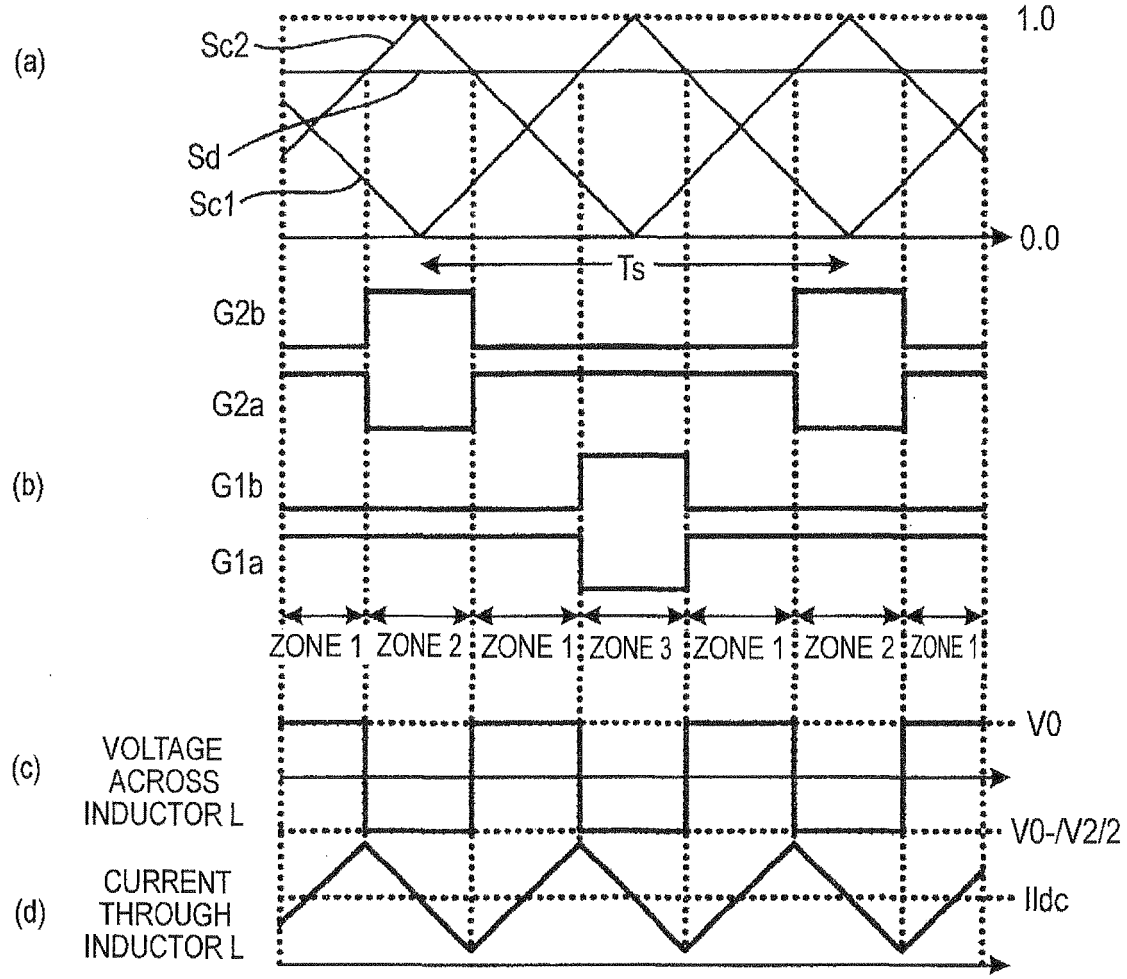

(a)
Sc2
Sd
Sc1
1.0
0.0
Ts
G2b
G2a
(b)
G1b
G1a
ZONE 1
ZONE 2
ZONE 1
ZONE 3
ZONE 1
ZONE 2
ZONE 1
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.8B

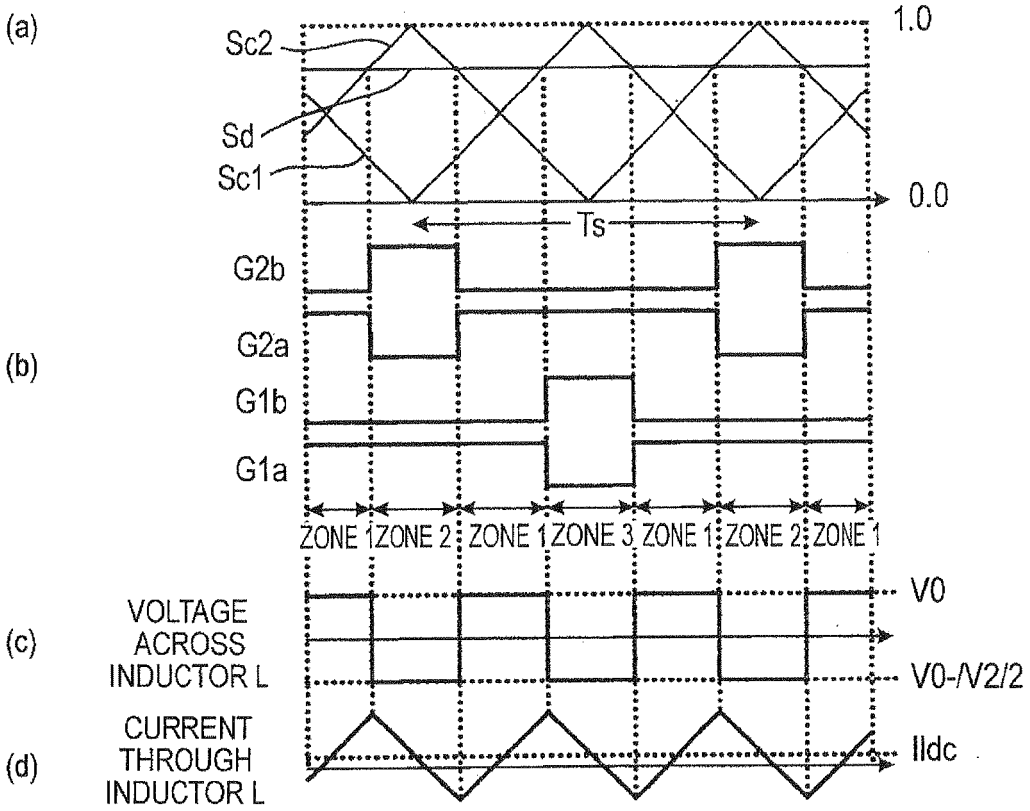

(a)
Sc2
Sd
Sc1
1.0
0.0
Ts
(b)
G2b
G2a
G1b
G1a
ZONE 1 ZONE 2 ZONE 1 ZONE 3 ZONE 1 ZONE 2 ZONE 1
(c)
VOLTAGE ACROSS INDUCTOR L
V0
V0-/V2/2
(d)
CURRENT THROUGH INDUCTOR L
Ildc

FIG.9

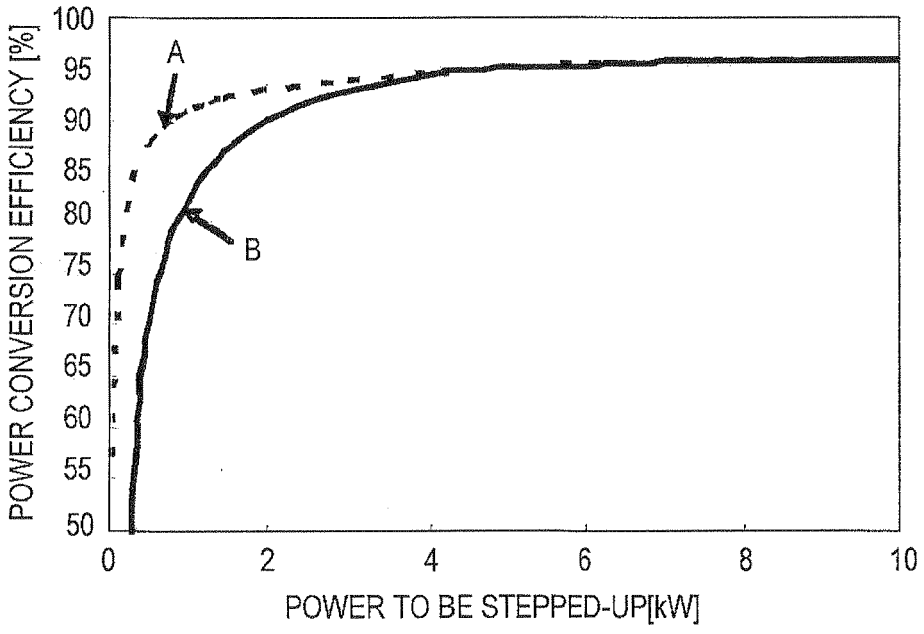
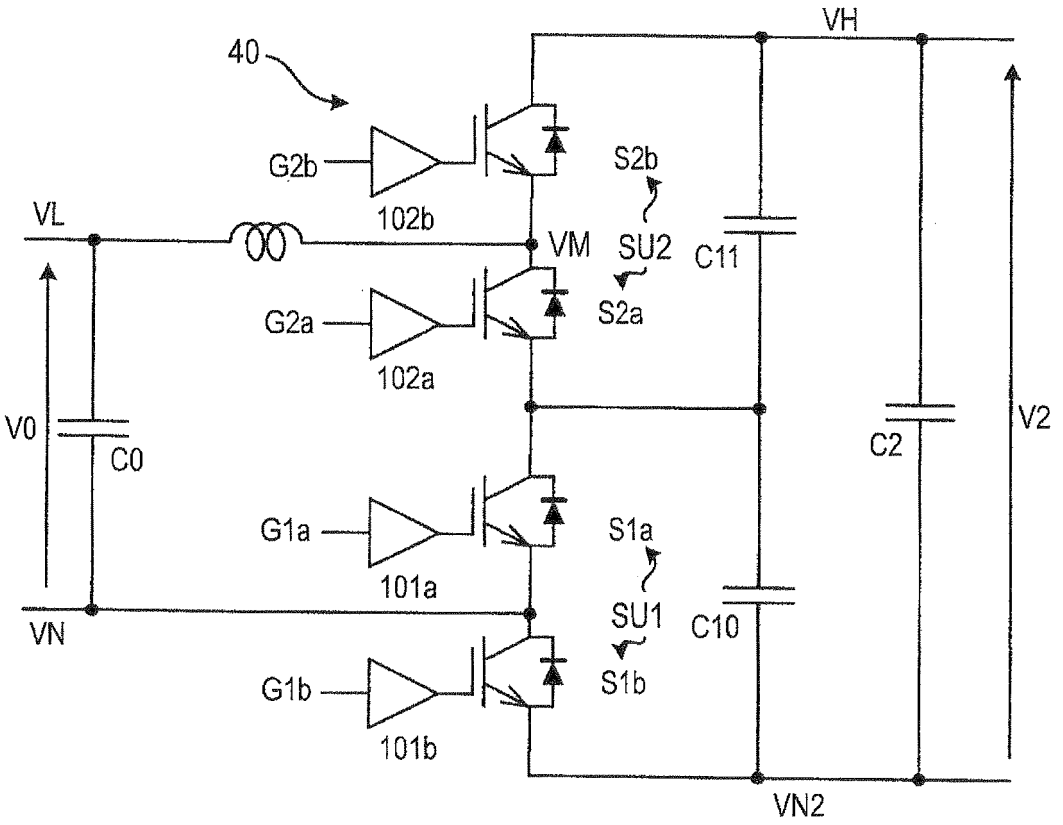

POWER CONVERSION EFFICIENCY [%]
100
95
90
85
80
75
70
65
60
55
50
A
B
0
2
4
6
8
10
POWER TO BE STEPPED-UP[kW]

FIG.10


VH
40
G2b
S2b
VL
102b
VM
SU2
C11
G2a
S2a
102a
V0
C0
C2
V2
G1a
S1a
101a
SU1
C10
VN
G1b
S1b
101b
VN2

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 3414749 B **[0003]**
- EP 2485376 A1 **[0005]**
- WO 2008032362 A1 **[0006]**
- JP 61092162 A **[0007]**
- US 20080211316 A1 **[0008]**

Non-patent literature cited in the description

- **THIERRY A. MEYNARD et al.** Multicell Converters: Basic Concepts and Industry Applications. *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS,* October 2002, vol. 49 (5 **[0004]**