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	European Patent Office Office européen des brevets EUROPEAN PATE Date of publication A3: 17.10.2001 Bulletin 2001/42 Date of publication A2: 24.01.2001 Bulletin 2001/04 Application number: 00306001.9 Date of filing: 14.07.2000 Designated Contracting States: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE Designated Extension States: AL LT LV MK RO SI Priority: 22.07.1999 JP 20742999 Applicant: SHINKO ELECTRIC INDUSTRIES CO. LTD. Nagano-shi, Nagano 380-0921 (JP)				

## (54) Multilayer circuit board

(57) The present invention provides a multilayer circuit board for mounting thereon a semiconductor chip or other electronic elements having electrode terminals or other connection terminals which are arranged in a grid, staggered, or close-packed manner in an improved form to enable reduction in the number of the wiring layers for lead wiring lines, thereby facilitating the production of multilayer circuit boards and providing an improved product reliability. The multilayer circuit board comprises: a base board having a mounting surface for mounting thereon a semiconductor chip and/or other electronic elements having lattice-arranged connection terminals; connection terminal pads (8) arranged on the mounting surface to form a plane lattice corresponding to the lattice arrangement of the connection terminals and having lattice sites each occupied by one of the connection terminal pads (8); lead wiring lines (7) lying on the mounting surface and having one end connected to the connection terminal pads (8) and the other end extending outwardly from the plane lattice; and the said plane lattice having a peripheral zone including periodic vacant lattice areas (A) formed by vacant lattice sites (10) occupied by no connection terminal pads (8).

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Fig.2





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## EUROPEAN SEARCH REPORT

Application Number EP 00 30 6001

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				TECHNICAL FIELDS SEARCHED (Int.CI.7) H01L H05K
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