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(54) Shift register and architecture of same on a display panel

(57) The present invention relates to a shift register and GOA architecture of the same in a display panel comprising a substrate and a plurality of pixels spatially formed on the substrate defining a number of pixel rows, each pixel row having a height of H. The shift register has the plurality of shift register stages disposed spatially and sequentially on the substrate in such a way that the layout of each shift register stage has a height of (j*H), j being an integer greater than one. Each shift register stages is configured to generate j scanning signals for driving j neighboring pixel rows, respectively.

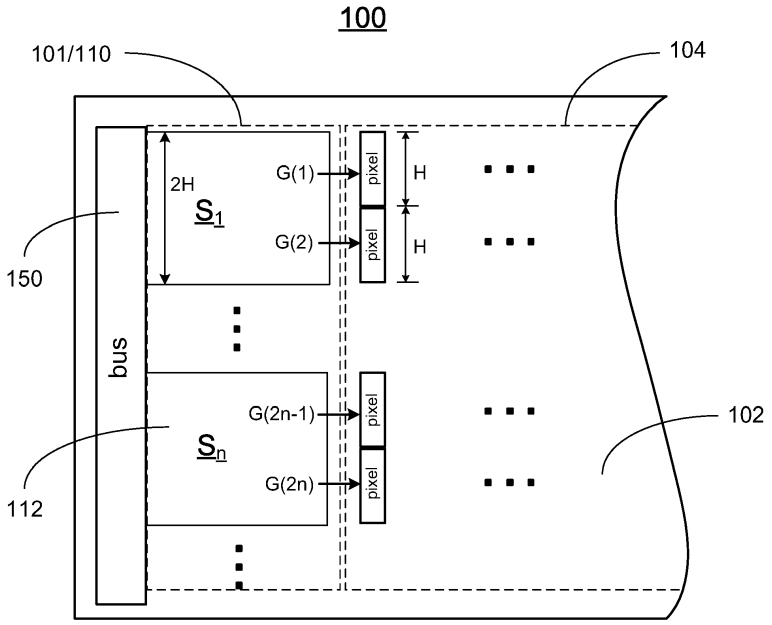

Fig. 1

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Description

FIELD OF THE INVENTION

[0001] The present disclosure relates generally to a shift register, and more particularly, to a shift register and architecture of the same on a display panel having a substrate and a plurality of pixels spatially formed on the substrate defining a number of pixel rows with a pixel height of H. The shift register has the plurality of shift register stages disposed spatially and sequentially on the substrate in such a way that the layout of each shift register stage has a height of (j*H), j being an integer greater than one. Each shift register stages is configured to generate j scanning signals for driving j neighboring pixel rows, respectively.

BACKGROUND OF THE INVENTION

[0002] A display panel has a substrate and pixel elements formed thereon. These pixel elements are substantially arranged in the form of a matrix having gate lines in rows and data lines in columns. The display panel is driven by a driving circuit including a gate driver and a data driver. The gate driver generates a plurality of gate signals (scanning signals) sequentially applied to the gate lines for sequentially turning on the pixel elements row-by-row. The data driver generates a plurality of source signals (data signals), i.e., sequentially sampling image signals, simultaneously applied to the data lines in conjunction with the gate signals applied to the gate lines for displaying an image on the panel.

[0003] In such a driving circuit, a shift register having multiple stages is utilized in the gate driver to generate the plurality of gate signals for sequentially driving the gate lines. To lower down costs, there have been efforts to integrate the shift register and the gate driver into a display panel. One of the efforts, for example, is to fabricate the shift register and the gate driver on a glass substrate of the panel, namely, the gate driver on array (GOA) arrangement, using amorphous silicon (a-Si) thin film transistors (TFTs), and/or low temperature polycrystalline silicon (LTPS) TFTs.

[0004] Fig. 12 shows a display panel 10 with a conventional GOA architecture 11 of a shift register formed thereon. The shift register has a plurality of stages 16. Each stage 16 generates a scanning signal for driving a corresponding pixel row of the display panel. For the GOA architecture 11, each stage 16 is formed on a substrate having a layout 13 with a height of H, which is the same as the height of a pixel row 12 of the display panel 10. As the high resolution is very demanded for high quality of image display, the shift register is usually designed to a great number of stages. Additionally, the circuit of each stage becomes more complicated as the display technology advances. This makes the GOA design of a display panel very complicated.

[0005] Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

SUMMARY OF THE INVENTION

[0006] In one aspect, the present invention relates to a shift register. In one embodiment, the shift register includes a plurality of shift register stages, $\{S_n\}$, n =1, 2, ..., N, N being a positive integer, electrically coupled to each other in series.

[0007] Each stage S_n includes a stage shift circuit having a first input for receiving a first control signal, HCn, and an output for outputting an output signal responsively, and a de-multiplexing circuit comprising a first switch circuit and a second switch circuit, wherein the first switch circuit has a first input for receiving a first clock signal CK1, a second input electrically coupled to the output of the stage shift circuit, and an output for outputting a first scanning signal, G(2n-1), responsively, and wherein the second switch circuit has a first input for receiving a second clock signal CK2, a second input electrically coupled to the output of the stage shift circuit, and an output for outputting a second scanning signal, G(2n), responsively.

[0008] Each of the first control signal HCn, the first clock signal CK1 and the second clock signal CK2 is characterized with a waveform alternating between a high voltage level and a low voltage level, wherein the high voltage levels of the first control signal HCn, the first clock signal CK1 and the second clock signal CK2 have widths, W_H, W_1 and W_2, respectively, satisfying the following relationship of:

$$W_H \geq W_1 + W_2 .$$

[0009] Each of the first and second switch circuits has a first transistor having a gate, a source and a drain electrically coupled to the second input, the first input and the output of the switch circuit, respectively. In one embodiment, each of the first and second switch circuits further has a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the source of the first transistor. In another embodiment, each of the first and second switch circuits also has a pull down circuit electrically coupled to the drain of the first transistor.

[0010] In one embodiment, each of the first and second switch circuits comprises a first transistor having a gate, a source and a drain electrically coupled to the first input, the second input and the output of the switch circuit, respectively, and a diode having an anode and a cathode electrically coupled to the drain and the gate of the first transistor, respectively.

[0011] In another embodiment, each of the first and second switch circuits comprises a diode having an an-

ode electrically coupled to the first input of the switch circuit and a cathode, a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch circuit, respectively, and a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the anode of the diode.

[0012] In yet another embodiment, each of the first and second switch circuits comprises a diode having an anode electrically coupled to the first input of the switch circuit and a cathode, a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch circuit, respectively, and a pull down circuit electrically coupled to the drain of the first transistor.

[0013] The stage shift circuit in one embodiment, further has a second input for receiving a second control signal, LC1, a third input for receiving a third control signal, LC2, a fourth input for receiving a reference voltage VSS, a fifth input for receiving the second scanning signal G(2n-2) output from the immediate prior stage, S_{n-1}, and a sixth input for receiving the second scanning signal G (2n+2) output from the immediate next stage, S_{n+1}.

[0014] In one embodiment, the stage shift circuit includes a pull-up control circuit electrically coupled to the fifth input, a pull-up circuit electrically coupled to the pull-up control circuit, the first input and the output, a pull-down control circuit electrically coupled to the pull-up control circuit, the pull-up circuit, and the second, third and fourth inputs, and a pull-down circuit electrically coupled to the pull-down control circuit, the pull-up circuit, the sixth input and the output.

[0015] In another aspect, the present invention relates to a gate driver-on-array (GOA) architecture of the shift register disclosed above in a display panel comprising a substrate and a plurality of pixels spatially formed on the substrate defining a number of pixel rows, each pixel row having a height of H. In one embodiment the plurality of shift register stages $\{S_n\}$ is disposed spatially and sequentially on the substrate such that each shift register stage S_n has a layout with a height of 2H, and the first and second scanning signals G(2n-1) and G(2n) output from the shift register stage S_n are used to drive the (2n-1)-th pixel row and the (2n)-th pixel row, respectively.

[0016] The GOA architecture further includes a formation of a data bus on the substrate for providing at least the first control signal HCn, and the first and second clock signal CK1 and CK2.

[0017] In yet another aspect, the present invention relates to a shift register comprising a plurality of shift register stages, $\{S_n\}$, n =1, 2, ..., N, N being a positive integer, electrically coupled to each other in series.

[0018] Each stage S_n includes a stage shift circuit having a first input for receiving a first control signal, HCn, and an output for outputting an output signal responsively, and a de-multiplexing circuit for receiving the output signal from the stage shift circuit and j clock signals, CK1, CK2, ... and CKj from a data bus and responsively outputting j scanning signals, G(j*n-j+1), G(j*n-j+2), ... and G(j*n), comprising j switch circuits, j being an integer greater than one, wherein each switch circuit has a first input for receiving a corresponding one of the j clock signals, CK1, CK2, ... and CKj, a second input electrically coupled to the output of the stage shift circuit for receiving the output signal therefrom, and an output for outputting a corresponding one of the j scanning signals, G(j*n-j+1), G(j*n-j+2), ... and G(j*n).

[0019] Each of the first control signal HCn, and the j clock signals, CK1, CK2, ... and CKj is characterized with a waveform alternating between a high voltage level and a low voltage level, wherein the high voltage levels of the first control signal HCn, and the j clock signals, CK1, CK2, ... and CKj have widths, W_H, W_1, W_2, ... and W_j, respectively, satisfying the following relationship of:

$$W_H \geq W_1 + W_2 + \ldots + W_j .$$

[0020] Each of the j switch circuits has a first transistor having a gate, a source and a drain electrically coupled to the second input, the first input and the output of the switch circuit, respectively. In one embodiment, each of the j switch circuits further has a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the source of the first transistor. In another embodiment, each of the j switch circuits also has a pull down circuit electrically coupled to the drain of the first transistor.

[0021] In one embodiment, each of the j switch circuits comprises a first transistor having a gate, a source and a drain electrically coupled to the first input, the second input and the output of the switch circuit, respectively, and a diode having an anode and a cathode electrically coupled to the drain and the gate of the first transistor, respectively.

[0022] In another embodiment, each of the j switch circuits comprises a diode having an anode electrically coupled to the first input of the switch circuit and a cathode, a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch circuit, respectively, and a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the anode of the diode.

[0023] In yet another embodiment, each of the j switch circuits comprises a diode having an anode electrically coupled to the first input of the switch circuit and a cathode, a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch

circuit, respectively, and a pull down circuit electrically coupled to the drain of the first transistor.

[0024] In a further aspect, the present invention relates a GOA architecture of the shift register disclosed above in a display panel comprising a substrate and a plurality of pixels spatially formed on the substrate defining a number of pixel rows, each pixel row having a height of H. In one embodiment, the plurality of shift register stages $\{S_n\}$ is disposed spatially and sequentially on the substrate such that each shift register stage S_n has a layout with a height of (j*H), and the j scanning signals G(j*n-j+1), G(j*n-j+2), ... and G(j*n) output from the shift register stage S_n are used to drive the (j*n-j+1)-th pixel row, (j*n-j+2)-th pixel row, ... and the (j*n)-th pixel row, respectively.

[0025] The GOA architecture also includes a formation of the data bus on the substrate for providing at least the first control signal HCn, and the j clock signals CK1, CK2, ... and CKj.

[0026] These and other aspects of the present invention will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be affected without departing from the spirit and scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings illustrate one or more embodiments of the invention and, together with the written description, serve to explain the principles of the invention. Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment, and wherein:

Fig. 1 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to one embodiment of the present invention;

Fig. 2 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to another embodiment of the present invention;

Fig. 3 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to yet another embodiment of the present invention;

Fig. 4 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to a further embodiment of the present invention;

Fig. 5 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to yet a further embodiment of the present invention;

Fig. 6 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to an alternative embodiment of the present invention;

Fig. 7 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to yet an alternative embodiment of the present invention;

Fig. 8 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to one embodiment of the present invention;

Fig. 9 shows schematically signal time charts of the display panel shown in Fig. 7;

Fig. 10 shows simulated signal time charts of the display panel shown in Fig. 7;

Fig. 11 shows schematically a display panel with a GOA architecture of a shift register formed thereon according to another embodiment of the present invention; and

Fig. 12 shows schematically a display panel with a conventional GOA architecture of a shift register formed thereon.

DETAILED DESCRIPTION OF THE INVENTION

[0028] The present invention is more particularly described in the following examples that are intended as illustrative only since numerous modifications and variations therein will be apparent to those skilled in the art. Various embodiments of the invention are now described in detail. Referring to the drawings, like numbers indicate like components throughout the views. As used in the description herein and throughout the claims that follow, the meaning of "a", "an", and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0029] The terms used in this specification generally have their ordinary meanings in the art, within the context of the invention, and in the specific context where each term is used. Certain terms that are used to describe the invention are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the invention. The use of examples anywhere in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the invention or of any exemplified term. Likewise, the invention is not limited to various embodiments given in this specification.

[0030] As used herein, "around", "about" or "approximately" shall generally mean within 20 percent, preferably within 10 percent, and more preferably within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term "around", "about" or "approximately" can be inferred if not expressly stated.

[0031] As used herein, the term "gate driver on array" or its acronym "GOA" refers to a fabricating layout or architecture of a shift register and/or a gate driver on a glass substrate of a display panel, with amorphous silicon (a-Si) thin film transistors (TFTs), and/or low temperature polycrystalline silicon (LTPS) TFTs.

[0032] As used herein, the terms "comprising," "including," "having," "containing," "involving," and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

[0033] The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings in Figs. 1-11. In accordance with the purposes of this disclosure, as embodied and broadly described herein, this disclosure, in one aspect, relates to a shift register and GOA architecture of the same in a display panel.

[0034] Referring to Fig. 1, a display panel 100 with a GOA architecture 101 of a shift register 110 formed thereon is schematically shown according to one embodiment of the present invention. The display panel 100 includes a substrate 102 and a plurality of pixels 104 spatially formed on the substrate 102 defining a number of pixel rows. Each pixel row has a height of H.

[0035] The shift register 110 includes a plurality of shift register stages, $\{S_n\}$, n =1, 2, ..., N, N being a positive integer, electrically coupled to each other in series. Each shift register stage S_n is configured to receive one or more control and clock signals and to output responsively a first scanning signal G(2n-1) and a second scanning signal G(2n) for driving the (2n-1)-th pixel row and the (2n)-th pixel row, respectively. In this exemplary embodiment, the plurality of shift register stages $\{S_n\}$ is disposed spatially and sequentially on the substrate 102 in such a way that each shift register stage S_n has a layout 112 with a height of 2H. The first and second scanning signals G(2n-1) and G(2n) output from the shift register stage S_n are used to drive the (2n-1)-th pixel row and the (2n)-th pixel row, respectively.

[0036] The GOA architecture 101 also includes a formation of a data bus 150 on the substrate 102 for providing, for example, the control and clock signals for each the shift register stage S_n.

[0037] Referring now to Fig. 2, a display panel 200 with a GOA architecture 201 of a shift register 210 formed thereon is schematically shown according to another embodiment of the present invention. The shift register 210 includes a plurality of shift register stages, $\{S_n\}$, n =1, 2, ..., N, disposed spatially and sequentially on the substrate 202 in such a way that each shift register stage S_n has a layout 212 with a height of 2H.

[0038] Each stage S_n includes a stage shift circuit 220 and a de-multiplexing circuit 230 electrically coupled to the stage shift circuit 220 for outputting a first scanning signal G(2n-1) and a second scanning signal G(2n), which are used to drive the (2n-1)-th pixel row and the (2n)-th pixel row, respectively.

[0039] In this exemplary embodiment shown in Fig. 2, the stage shift circuit 220 has a first input for receiving a first control signal, HC_n, a second input for receiving a second control signal, LC1, a third input for receiving a third control signal, LC2, a fourth input for receiving a reference voltage VSS, a fifth input, a sixth input, and an output for responsively outputting an output signal. Further, the fifth input is adapted for receiving the second scanning signal G(2n-2) output from the immediate prior stage, S_{n-1}, while the sixth input is adapted for receiving the second scanning signal G(2n+2) output from the immediate next stage, S_{n+1}. For such an arrangement, the plurality of shift register stages $\{S_n\}$ is electrically coupled to each other in series.

[0040] According to the present invention, any types of stage shift circuits can be utilized to practice the invention. Generally, the stage shift circuit 220 includes a pull-up control circuit electrically coupled to the fifth input, a pull-up circuit electrically coupled to the pull-up control circuit, the first input and the output, a pull-down control circuit electrically coupled to the pull-up control circuit, the pull-up circuit, and the second, third and fourth inputs, and a pull-down circuit electrically coupled to the pull-down control circuit, the pull-up circuit, the sixth input and the output.

[0041] The de-multiplexing circuit 230 includes a first switch circuit and a second switch circuit. The first switch circuit has a first input for receiving a first clock signal CK1, a second input electrically coupled to the output of the stage shift circuit 220, and an output for outputting the first scanning signal G(2n-1), responsively. The second switch circuit has a first input for receiving a second clock signal CK2, a second input electrically coupled to the output of the stage shift circuit 220, and an output for outputting the second scanning signal G(2n), responsively.

[0042] In practice, the first control signal HC_n is a low frequency AC signal, while both the first and second clock signals CK1 and CK2 are two high frequency AC signals.

[0043] Further, the first and second clock signals CK1 and CK2 are out-of phase from one another. Each of the first control signal HCn, the first clock signal CK1 and the second clock signal CK2 is characterized with a waveform alternating between a high voltage level and a low voltage level. The high voltage levels of the first control signal HC_n, the first clock signal CK1 and the second clock signal CK2 have widths, W_H, W_1 and W_2, respectively, which satisfy the following relationship of:

$$W_H \geq W_1 + W_2 .$$

[0044] Figs. 3-8 show schematically various embodiments of a display panel with a GOA architecture of a shift register formed thereon. All the embodiments of the display panel have the same GOA architecture of the shift register as that of the display panel 200 shown in Fig. 2, where the layout of each shift register stage S_n

on the substrate has a height of 2H, and each shift register stage S_n operably generates a first scanning signal G (2n-1) and a second scanning signal G(2n) for driving the (2n-1)-th pixel row and the (2n)-th pixel row of the display panel, respectively. For such a GOA architecture, the circuit layout of the shift register on the substrate is substantially simplified.

[0045] As shown in Figs. 3-8, however, in these exemplary embodiments, the de-multiplexing circuit having the first and second switch circuits has different configurations.

[0046] For example, as shown in Fig. 3, each of the first and second switch circuits of the de-multiplexing circuit 330 has a transistor T1 or T2 having a gate electrically coupled to the second input of the switch circuit for receiving the output signal of the stage shift circuit, a source coupled to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, and a drain electrically coupled to the output of the switch circuit for outputting a corresponding scanning signal G (2n-1) or G(2n), respectively.

[0047] As shown in Fig. 4, each of the first and second switch circuits of the de-multiplexing circuit 430 has a transistor T1 or T2 and a diode D1 or D2. The transistor T1 or T2 has a gate electrically coupled to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, a source coupled to the second input of the switch circuit for receiving the output signal of the stage shift circuit and a drain electrically coupled to the output of the switch circuit for outputting a corresponding scanning signal G(2n-1) or G(2n), respectively. The diode D1 or D2 has an anode and a cathode electrically coupled to the drain and the gate of the transistor T1 or T2, respectively.

[0048] Referring to Fig. 5, each of the first and second switch circuits of the de-multiplexing circuit 530 has a transistor T1 or T2 and a pull-down unit 1 or a pull-down unit 2. The transistor T1 or T2 has a gate electrically coupled to the second input of the switch circuit for receiving the output signal of the stage shift circuit, a source coupled to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, and a drain electrically coupled to the output of the switch circuit for outputting a corresponding scanning signal G (2n-1) or G(2n), respectively. The pull-down unit 1 or the pull-down unit 2 is electrically coupled to the drain of the transistor T1 or T2, respectively..

[0049] Referring to Fig. 6, each of the first and second switch circuits of the de-multiplexing circuit 630 is similar to that shown in Fig. 5, except that each of the first and second switch circuits includes an additional diode D1 or D2. The diode D1 or D2 has an anode connected to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, and a cathode connected to the source of the transistor T1 or T2.

[0050] Referring to Fig. 7, each of the first and second switch circuits of the de-multiplexing circuit 730 has a first transistor T1 or T2 and a second transistor M1 or M2. The transistor T1 or T2 has a gate electrically coupled to the second input of the switch circuit for receiving the output signal of the stage shift circuit, a source coupled to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, and a drain electrically coupled to the output of the switch circuit for outputting a corresponding scanning signal G(2n-1) or G(2n), respectively. The second transistor M1 or M2 has a gate electrically coupled to the drain of the first transistor T1 or T2, a source electrically couple to the gate, and a drain electrically coupled to the source of the first transistor T1 or T2.

[0051] As shown in Fig. 8, each of the first and second switch circuits of the de-multiplexing circuit 830 is similar to that shown in Fig. 7, except that each of the first and second switch circuits includes an additional diode D1 or D2. The diode D1 or D2 has an anode connected to the first input of the switch circuit for receiving the first clock signal CK1 or the second clock signal CK2, and a cathode connected to the source of the transistor T1 or T2.

[0052] In addition, Fig. 8 also shows an exemplary embodiment of the stage shift circuit 820 of the shift register 810. The stage shift circuit 820 includes a pull-up control circuit 821 electrically coupled to the fifth input for receiving the scanning signal G(2n-2) outputting from the immediately prior shift register stage S_{n-1}, a pull-up circuit 822 electrically coupled to the pull-up control circuit 821, the first input for receiving the first control signal HCn, and the output for outputting a signal g(n), a pull-down control circuit 823 electrically coupled to the pull-up control circuit 821, the pull-up circuit 822, and the second, third and fourth inputs for receiving the second control signal LC1, the third control signal LC2 and the reference voltage VSS, respectively, and a pull-down circuit 824 electrically coupled to the pull-down control circuit 823, the pull-up circuit 822, the sixth input for receiving the scanning signal G(2n+2) outputting from the immediately next shift register stage S_{n+1} and the output for outputting the signal g(n).

[0053] Specifically, the pull-up control circuit 821 includes a transistor T11 having a gate electrically coupled to the fifth input of the stage shift circuit 820 for receiving the scanning signal G(2n-2) outputting from the immediately prior shift register stage S_{n-1}, a source electrically coupled to the gate and a drain electrically coupled to a node Q(n).

[0054] The pull-up circuit 822 includes a transistor T21 having a gate electrically coupled to the node Q(n), a source electrically coupled to the first input of the stage shift circuit 820 for receiving the first control signal HCn, and a drain electrically coupled to the output g(n) of the stage shift circuit 820.

[0055] The pull-down control circuit 823 includes a first pull-down control circuit and a second pull-down control circuit. Each pull-down control circuit has four transistors, for example, T31, T32, T33 and T34 for the first pull-down control circuit, and T35, T36 T37 and T38 for the second pull-down control circuit. For the first pull-down control

circuit, the transistor T31 has a gate electrically coupled to the second input of the stage shift circuit 820 for receiving the second control signal LC1, a source electrically coupled to the gate, and a drain electrically coupled to a node P(n); the transistor T32 has a gate electrically coupled to the node Q(n), a source electrically coupled to the node P(n), and a drain electrically coupled to the fourth input of the stage shift circuit 820 for receiving the reference voltage VSS; the transistor T33 has a gate electrically coupled to the node P(n), a source electrically coupled to the node Q(n), and a drain electrically coupled to the drain of the transistor T32; and the transistor T34 has a gate electrically coupled to the node P(n), a source electrically coupled to the output g(n) of the stage shift circuit 820, and a drain electrically coupled to the drain of the transistor T32. For the second pull-down control circuit, the transistor T35 has a gate electrically coupled to the third input of the stage shift circuit 820 for receiving the third control signal LC2, a source electrically coupled to the gate, and a drain electrically coupled to a node K (n); the transistor T36 has a gate electrically coupled to the node Q(n), a source electrically coupled to the node K(n), and a drain electrically coupled to the fourth input of the stage shift circuit 820 for receiving the reference voltage VSS; the transistor T37 has a gate electrically coupled to the node K(n), a source electrically coupled to the node Q(n), and a drain electrically coupled to the drain of the transistor T36; and the transistor T38 has a gate electrically coupled to the node K(n), a source electrically coupled to the output g(n) of the stage shift circuit 820, and a drain electrically coupled to the drain of the transistor T36.

[0056] The pull-down circuit 824 has a first transistor T41 and a second transistor T42. The first transistor T41 has a gate electrically coupled to the sixth input for receiving the scanning signal G(2n+2) outputting from the immediately next shift register stage S_{n+1}, a source electrically coupled to the node Q(n), and a drain electrically coupled to the drain of the transistor T38. The second transistor T42 has a gate electrically coupled to the gate of the first transistor T41, a source electrically coupled to the output g(n) of the stage shift circuit 820, and a drain electrically coupled to the drain of the transistor T41.

[0057] Fig. 9 is time charts of the control signals HC1, HC2, LC1 and LC2, and the clock signals CK1 and CK2 for the shift register shown in Fig. 8, the voltage potential of the node Q(n), the voltage potential of the output g(n), and the corresponding scanning signals G(2n-2), G(2n-1), G(2n), G(2n+1) and G(2n+2) generated by the shift register in response to the control signals and the clock signals. As shown in the time charts, the high voltage pulse widths W_H, W_1 and W_2 of the first control signal HC1, the first and second clock signals CK1 and CK2 obeys the relationship of $W_H \geq (W_1 + W_2)$.

[0058] Fig. 10 is a simulated time charts of the control signals HC1, HC2, LC1 and LC2, and the clock signals CK1 and CK2 for the shift register shown in Fig. 8, the voltage potential of the node Q(n), the voltage potential of the output g(n), and the corresponding scanning signals G(2n-2), G(2n-1), G(2n), G(2n+1) and G(2n+2) generated by the shift register in response to the control signals and the clock signals.

[0059] Referring to Fig. 11, a display panel 1100 with a GOA architecture 1101 of a shift register 1110 formed thereon is schematically shown according to another embodiment of the present invention. The display panel 1100 includes a substrate 1102 and a plurality of pixels 1104 spatially formed on the substrate 1102 defining a number of pixel rows. Each pixel row has a height of H.

[0060] The shift register 1110 includes a plurality of shift register stages, $\{S_n\}$, n =1, 2, ..., N, electrically coupled to each other in series. Each shift register stage S_n is configured to receive one or more control and clock signals, for example, a control signal HCn and the j clock signals, CK1, CK2, ... and CKj, and to output responsively j scanning signals G(j*n-j+1), G(j*n-j+2), ... and G(j*n) for driving the (j*n-j+1)-th pixel row, (j*n-j+2)-th pixel row, ... and the (j*n)-th pixel row of the display panel 1100, respectively.

[0061] Each stage S_n includes a stage shift circuit and de-multiplexing circuit (not shown). The stage shift circuit is same as that disclosed above. However, the de-multiplexing circuit has j switch circuits, j being an integer greater than one. The de-multiplexing circuit is adapted for receiving the output signal from the stage shift circuit and j clock signals, CK1, CK2, ... and CKj from a data bus 1150 and responsively outputting j scanning signals, G(j*n-j+1), G(j*n-j+2), ... and G(j*n).

[0062] Each switch circuit has the same circuit as shown in Figs. 3-8 and disclosed above. Specifically, each switch circuit has a first input for receiving a corresponding one of the j clock signals, CK1, CK2, ... and CKj, a second input electrically coupled to the output of the stage shift circuit for receiving the output signal therefrom, and an output for responsively outputting a corresponding one of the j scanning signals, G(j*n-j+1), G(j*n-j+2), ... and G(j*n).

[0063] Practically, the first control signal HC_n is a low frequency AC signal, while all the j clock signals, CK1, CK2, ... and CKj are high frequency AC signals. Further, each of the first control signal HCn, and the j clock signals, CK1, CK2, ... and CKj is characterized with a waveform alternating between a high voltage level and a low voltage level, wherein the high voltage levels of the first control signal HC_n, and the j clock signals, CK1, CK2, ... and CKj have widths, W_H, W_1, W_2, ... and W_j, respectively, satisfying the following relationship of:

$$W_H \geq W_1 + W_2 + \ldots + W_j .$$

[0064] In this exemplary embodiment, the plurality of shift register stages $\{S_n\}$ is disposed spatially and sequentially on the substrate 1102 in such a way that the layout of each shift register stage S_n has a height of (j*H),

and the j scanning signals G(j*n-j+1), G(j*n-j+2), ... and G(j*n) output from the shift register stage S_n are used to drive the (j*n-j+1)-th pixel row, (j*n-j+2)-th pixel row, ... and the (j*n)-th pixel row, respectively.

[0065] The GOA architecture 1101 also includes a formation of a data bus 1150 on the substrate 1102 for providing, for example, the first control signal HC_n, and the j clock signals CK1, CK2, ... and CKj for each the shift register stage S_n.

[0066] For such a GOA architecture, the circuit layout of the shift register on the substrate is substantially simplified.

[0067] The foregoing description of the exemplary embodiments of the invention has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

[0068] The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to activate others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly, the scope of the present invention is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

Claims

1. A shift register, comprising a plurality of shift register stages, $\{S_n\}$, n = 1, 2, ..., N, N being a positive integer, electrically coupled to each other in series, each stage S_n comprising:

   a stage shift circuit having a first input for receiving a first control signal, HC_n, and an output for outputting an output signal responsively; and
   a de-multiplexing circuit for receiving the output signal from the stage shift circuit and j clock signals, CK1, CK2, ... and CKj from a data bus and responsively outputting j scanning signals, G (j*n-j+1), G(j*n-j+2), ... and G(j*n), comprising j switch circuits, j being an integer greater than one, wherein each switch circuit has a first input for receiving a corresponding one of the j clock signals, CK1, CK2, ... and CKj, a second input electrically coupled to the output of the stage shift circuit for receiving the output signal therefrom, and an output for outputting a corresponding one of the j scanning signals, G(j*n-j+1), G (j*n-j+2), ... and G(j*n),

   wherein each of the first control signal HC_n, and the j clock signals, CK1, CK2, ... and CKj is characterized with a waveform alternating between a high voltage level and a low voltage level, wherein the high voltage levels of the first control signal HC_n, and the j clock signals, CK1, CK2, ... and CKj have widths, W_H, W_1, W_2, ... and W_j, respectively, satisfying the following relationship of:

$$W_H \geq W_1 + W_2 + \ldots + W_j .$$

2. The shift register of claim 1, wherein each of the j switch circuits comprises a first transistor having a gate, a source and a drain electrically coupled to the second input, the first input and the output of the switch circuit, respectively.

3. The shift register of claim 2 wherein each of the j switch circuits further comprises a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the source of the first transistor.

4. The shift register of claim 2, wherein each of the j switch circuits further comprises a pull down circuit electrically coupled to the drain of the first transistor.

5. The shift register of claim 1, wherein each of the j switch circuits comprises:

   a first transistor having a gate, a source and a drain electrically coupled to the first input, the second input and the output of the switch circuit, respectively; and
   a diode having an anode and a cathode electrically coupled to the drain and the gate of the first transistor, respectively.

6. The shift register of claim 1, wherein each of the j switch circuits comprises:

   a diode having an anode electrically coupled to the first input of the switch circuit and a cathode;
   a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch circuit, respectively; and
   a second transistor having a gate electrically coupled to the drain of the first transistor, a source electrically couple to the gate, and a drain electrically coupled to the anode of the diode.

7. The shift register of claim 1, wherein each of the j switch circuits comprises:

   a diode having an anode electrically coupled to

the first input of the switch circuit and a cathode;
a first transistor having a gate, a source and a drain electrically coupled to the second input of the switch circuit, the cathode of the diode and the output of the switch circuit, respectively; and
a pull down circuit electrically coupled to the drain of the first transistor.

8. The shift register of claim 1, wherein the stage shift circuit further has a second input for receiving a second control signal, LC1, a third input for receiving a third control signal, LC2, a fourth input for receiving a reference voltage VSS, a fifth input for receiving one of the j scanning signal output from the immediate prior stage, S_{n-1}, and a sixth input for receiving one of the j scanning signal output from the immediate next stage, S_{n+1}.

9. The shift register of claim 8, wherein the stage shift circuit comprises;
a pull-up control circuit electrically coupled to the fifth input;
a pull-up circuit electrically coupled to the pull-up control circuit, the first input and the output;
a pull-down control circuit electrically coupled to the pull-up control circuit, the pull-up circuit, and the second, third and fourth inputs; and
a pull-down circuit electrically coupled to the pull-down control circuit, the pull-up circuit, the sixth input and the output.

10. A gate driver-on-array (GOA) architecture of the shift register of claim 1 in a display panel comprising a substrate and a plurality of pixels spatially formed on the substrate defining a number of pixel rows, each pixel row having a height of H, **characterized in that** the plurality of shift register stages $\{S_n\}$ is disposed spatially and sequentially on the substrate such that each shift register stage S_n has a layout with a height of j*H, and the j scanning signals G(j*n-j+1), G(j*n-j+2), ...,and G(j*n) output from the shift register stage S_n are used to drive the (j*n-j+1)-th pixel row, (j*n-j+2)-th pixel row, ... and the (j*n)-th pixel row respectively.

11. The GOA architecture of claim 10, **characterized in that** a data bus is disposed on the substrate for providing at least the first control signal HC_n, and the j clock signals CK1, CK2, ... and CKj.

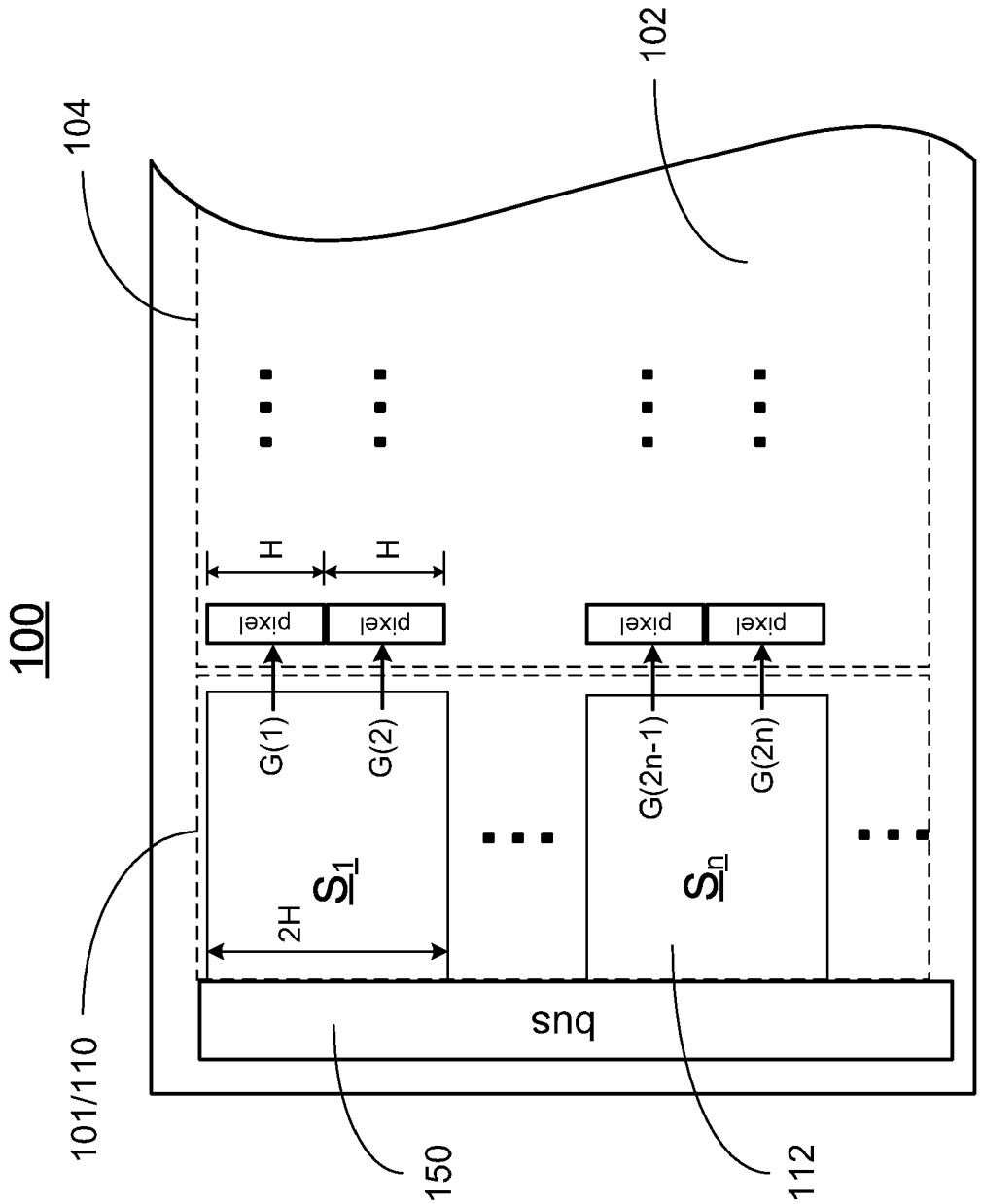
100
104
102
H
H
pixel
pixel
pixel
pixel
G(1)
G(2)
G(2n-1)
G(2n)
2H
S_1
S_n
bus
101/110
150
112

Fig. 1

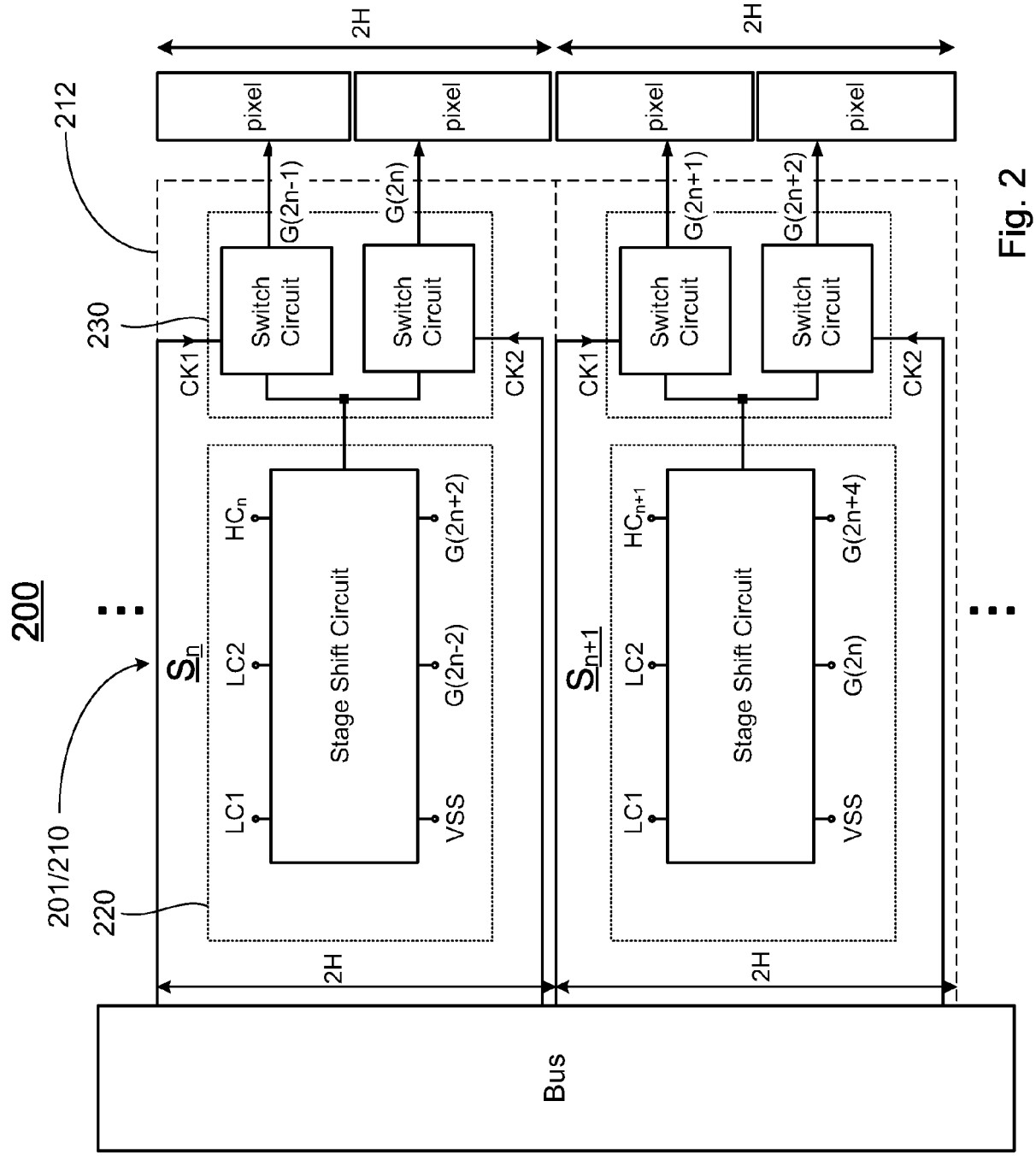
200
212
230
220
201/210
2H
2H
2H
2H
pixel
pixel
pixel
pixel
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
Switch Circuit
Switch Circuit
Switch Circuit
Switch Circuit
CK1
CK2
CK1
CK2
S_n
S_{n+1}
HC_n
HC_{n+1}
LC2
LC1
VSS
Stage Shift Circuit
G(2n+2)
G(2n-2)
G(2n+4)
G(2n)
Bus

Fig. 2

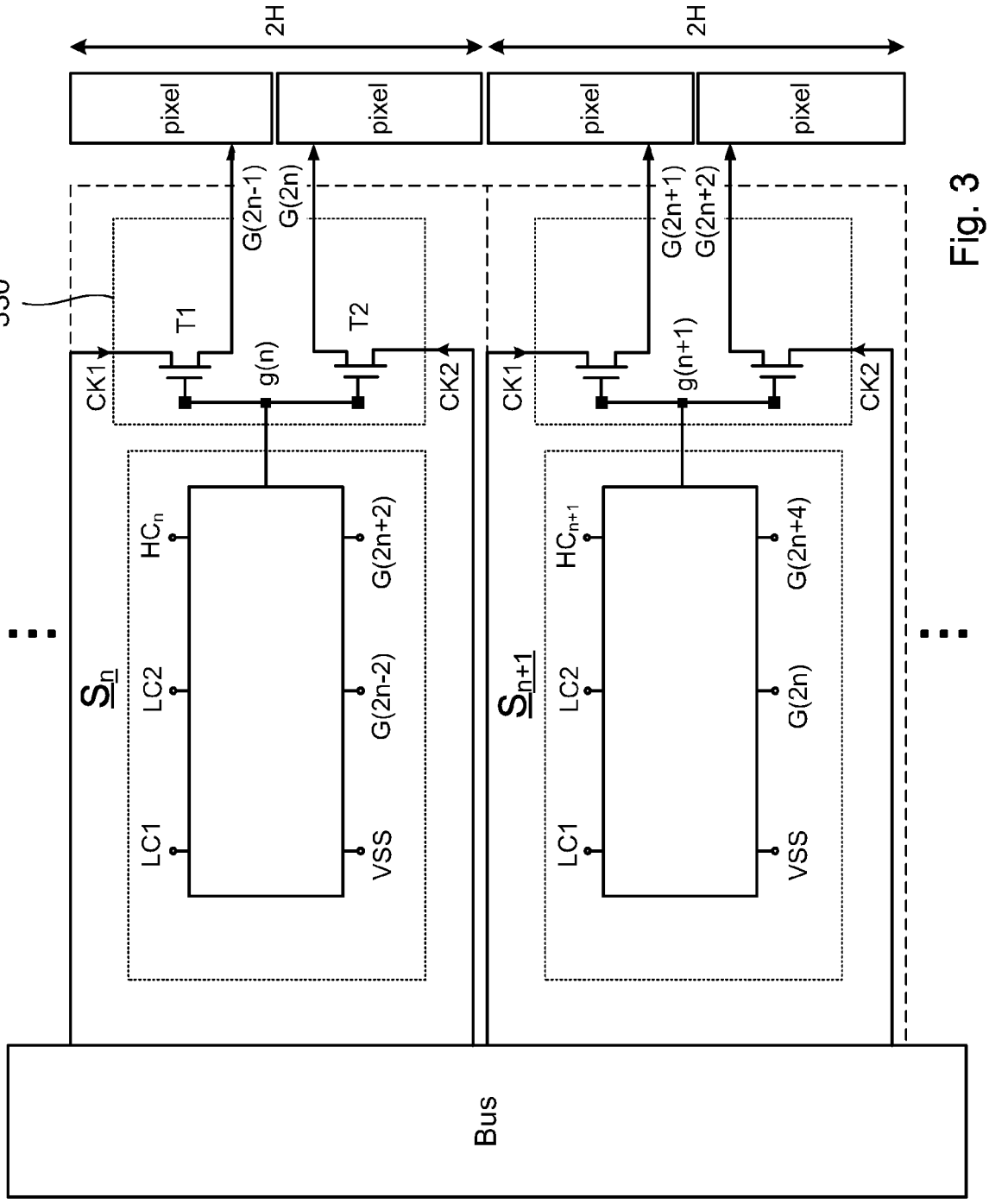
2H
2H
pixel
pixel
pixel
pixel
330
T1
T2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
CK1
CK2
g(n)
g(n+1)
HCn
LC2
LC1
G(2n+2)
G(2n-2)
VSS
Sn
HCn+1
G(2n+4)
G(2n)
Sn+1
Bus

Fig. 3

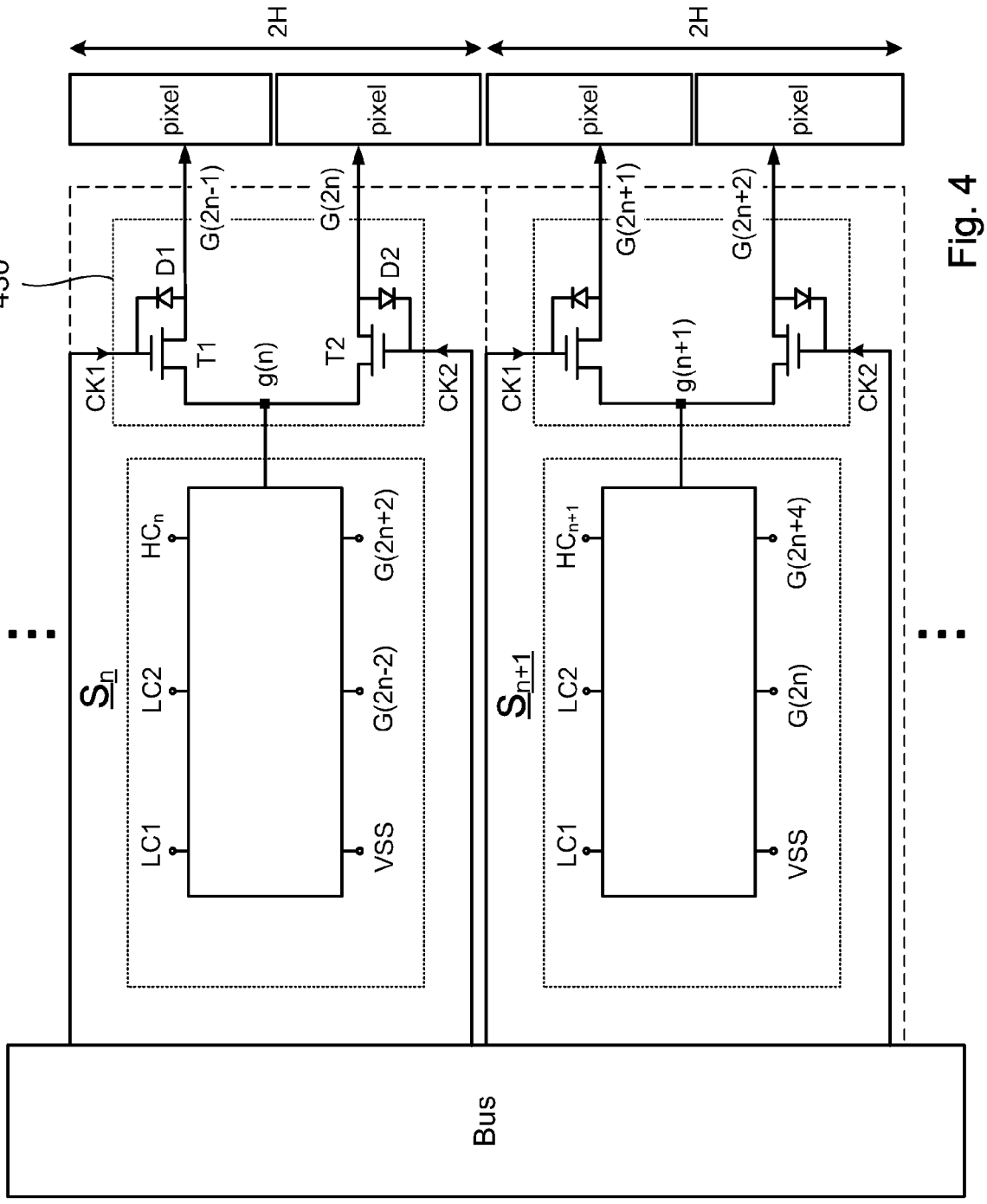
2H
2H
pixel
pixel
pixel
pixel
430
D1
D2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
T1
T2
g(n)
g(n+1)
CK1
CK2
CK1
CK2
S_n
S_{n+1}
HC_n
HC_{n+1}
LC2
LC1
VSS
G(2n+2)
G(2n-2)
G(2n+4)
G(2n)
Bus

Fig. 4

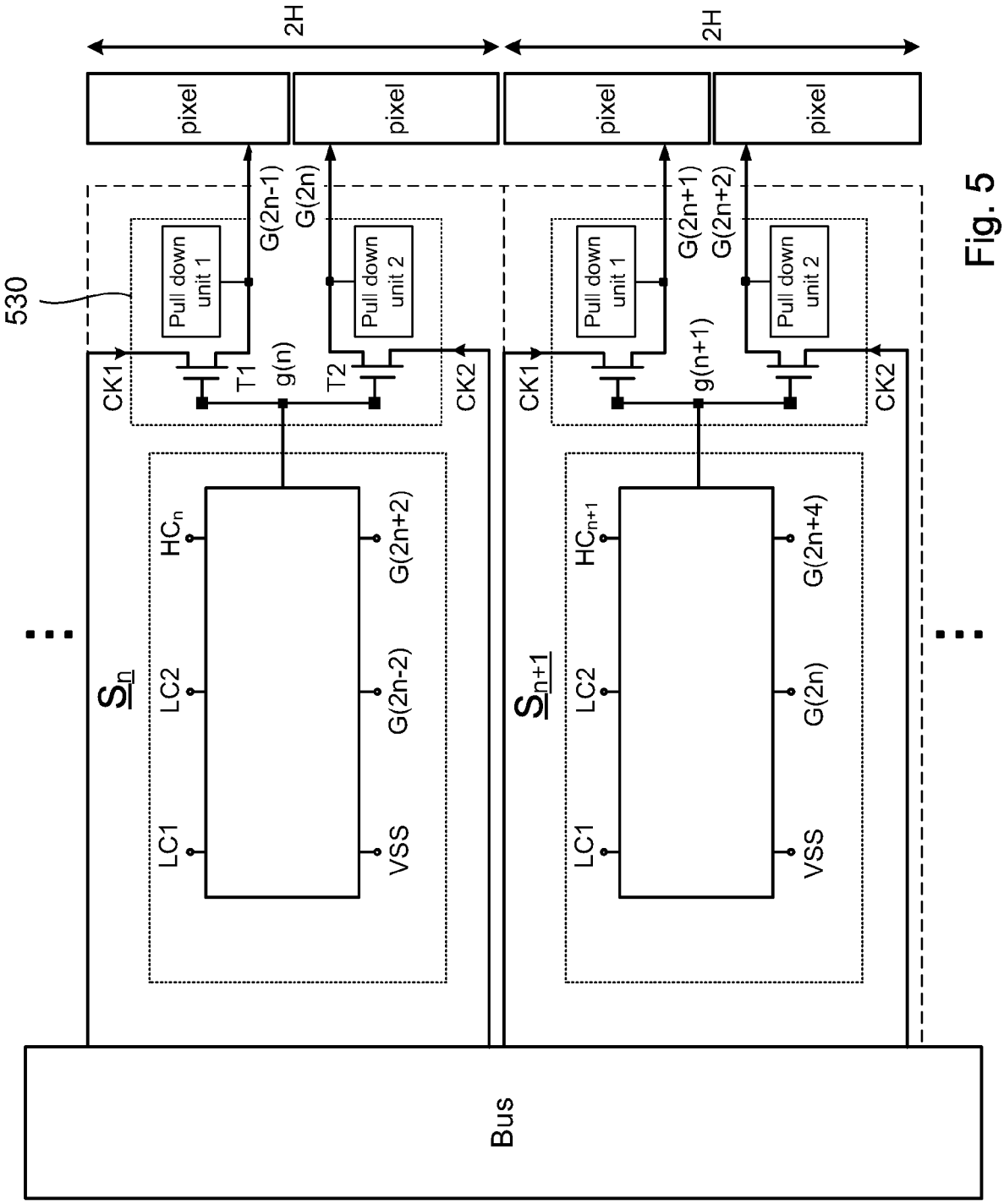
2H
2H
pixel
pixel
pixel
pixel
530
Pull down unit 1
Pull down unit 2
Pull down unit 1
Pull down unit 2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
CK1
T1
g(n)
T2
CK2
CK1
g(n+1)
CK2
HCn
LC2
LC1
G(2n+2)
G(2n-2)
VSS
HCn+1
LC2
LC1
G(2n+4)
G(2n)
VSS
Sn
Sn+1
Bus

Fig. 5

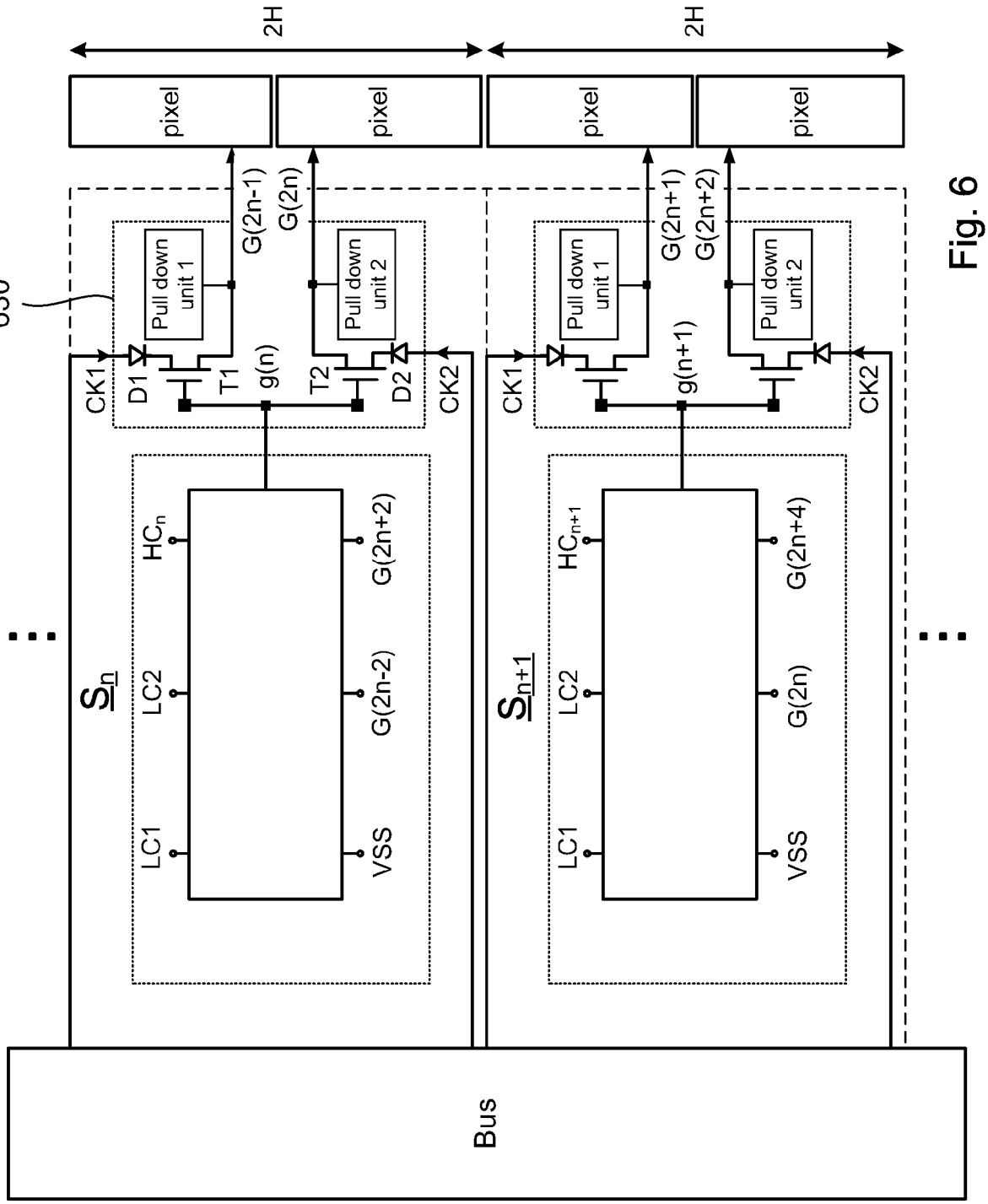
2H
2H
pixel
pixel
pixel
pixel
630
Pull down unit 1
Pull down unit 2
Pull down unit 1
Pull down unit 2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
CK1
D1
T1
g(n)
T2
D2
CK2
CK1
g(n+1)
CK2
HCn
LC2
LC1
G(2n+2)
G(2n-2)
VSS
HCn+1
LC2
LC1
G(2n+4)
G(2n)
VSS
Sn
Sn+1
Bus

Fig. 6

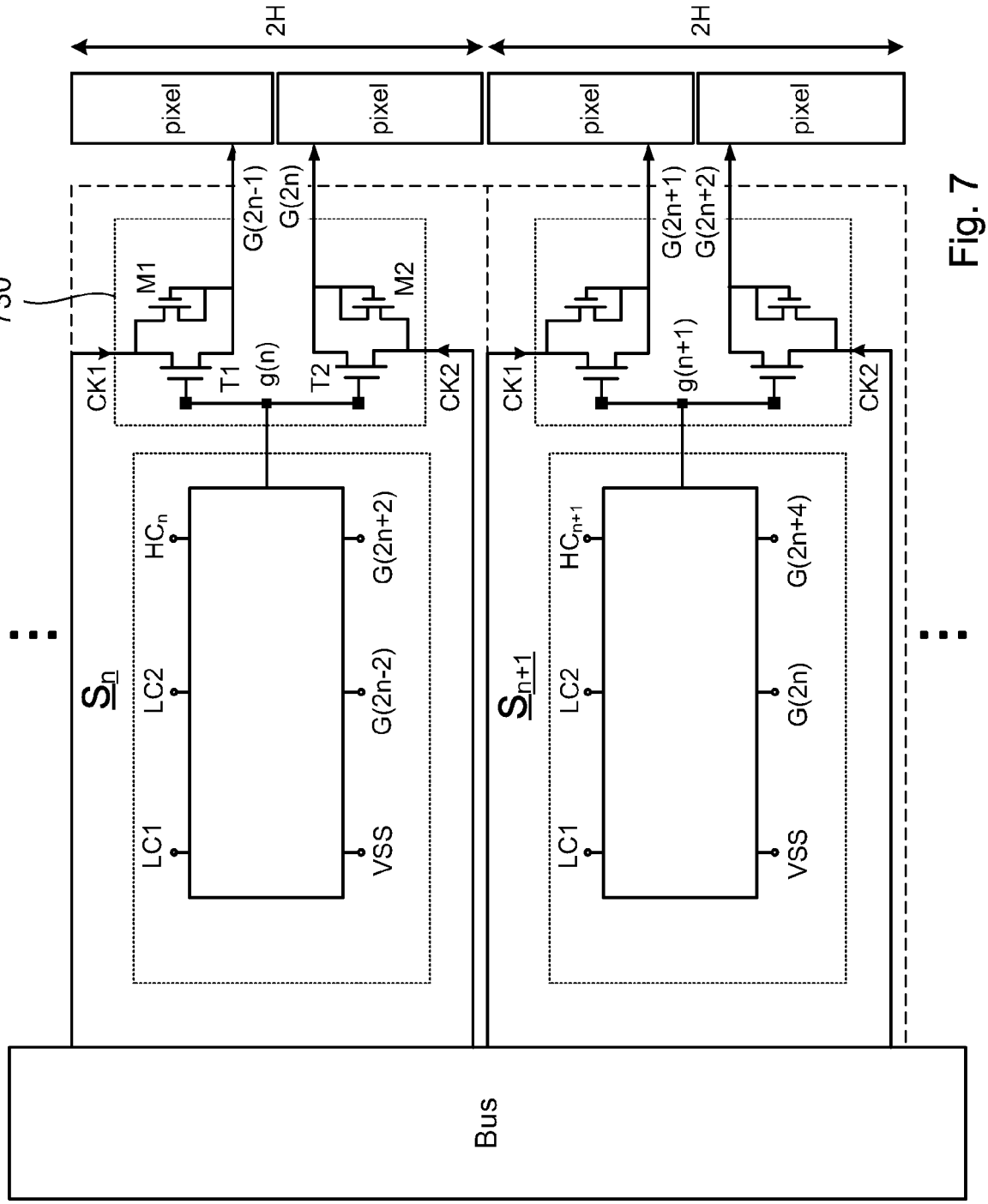
2H
2H
pixel
pixel
pixel
pixel
730
M1
M2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
CK1
T1
g(n)
T2
CK2
CK1
g(n+1)
CK2
HCn
LC2
LC1
G(2n+2)
G(2n-2)
VSS
Sn
HCn+1
LC2
LC1
G(2n+4)
G(2n)
VSS
Sn+1
Bus

Fig. 7

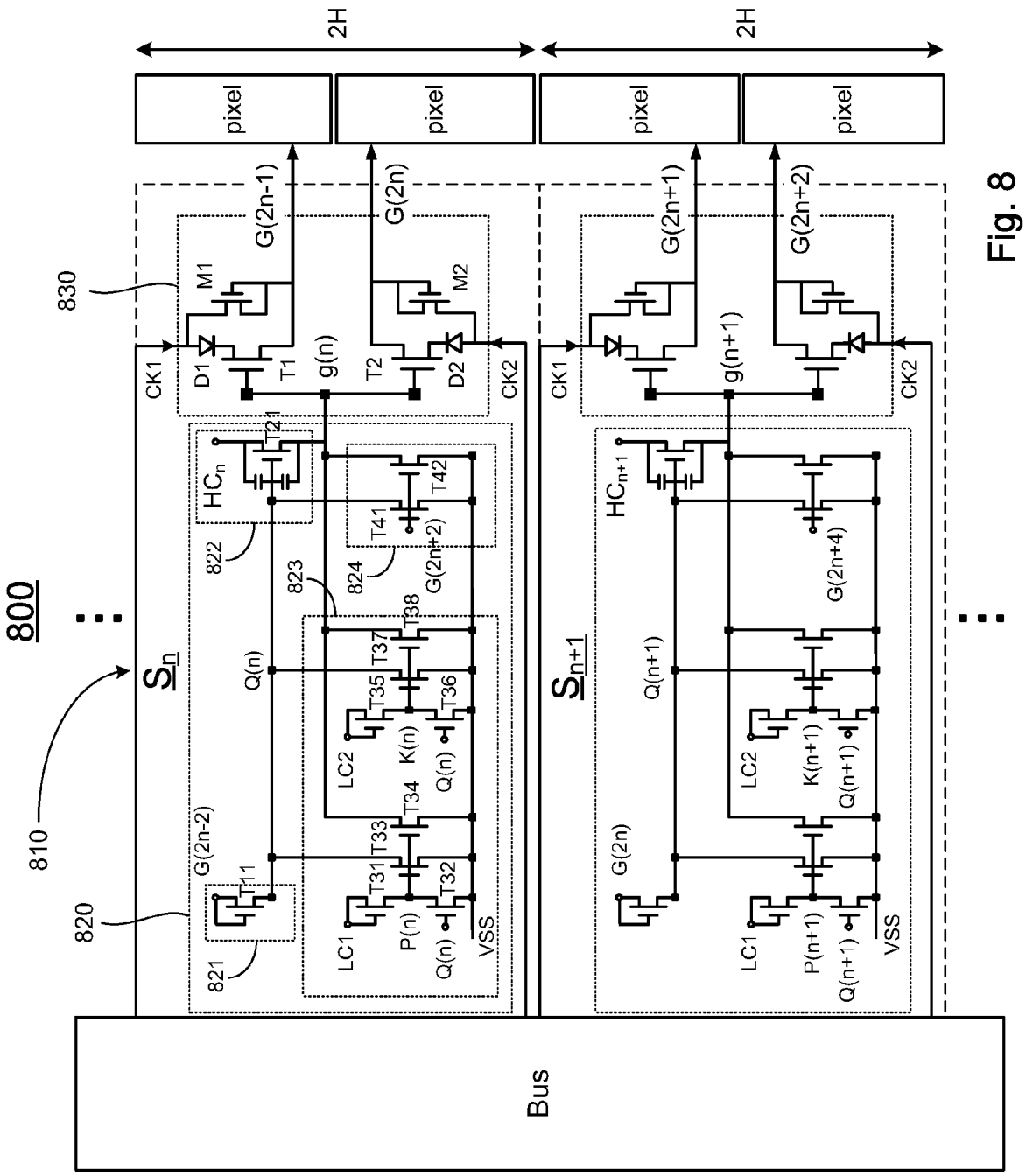
800
810
820
821
822
823
824
830
2H
2H
pixel
pixel
pixel
pixel
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)
M1
M2
D1
D2
T1
T2
CK1
CK2
g(n)
g(n+1)
S_n
S_{n+1}
HC_n
HC_{n+1}
G(2n-2)
G(2n+2)
G(2n+4)
T11
T21
T31
T32
T33
T34
T35
T36
T37
T38
T41
T42
LC1
LC2
P(n)
P(n+1)
K(n)
K(n+1)
Q(n)
Q(n+1)
VSS
Bus

Fig. 8

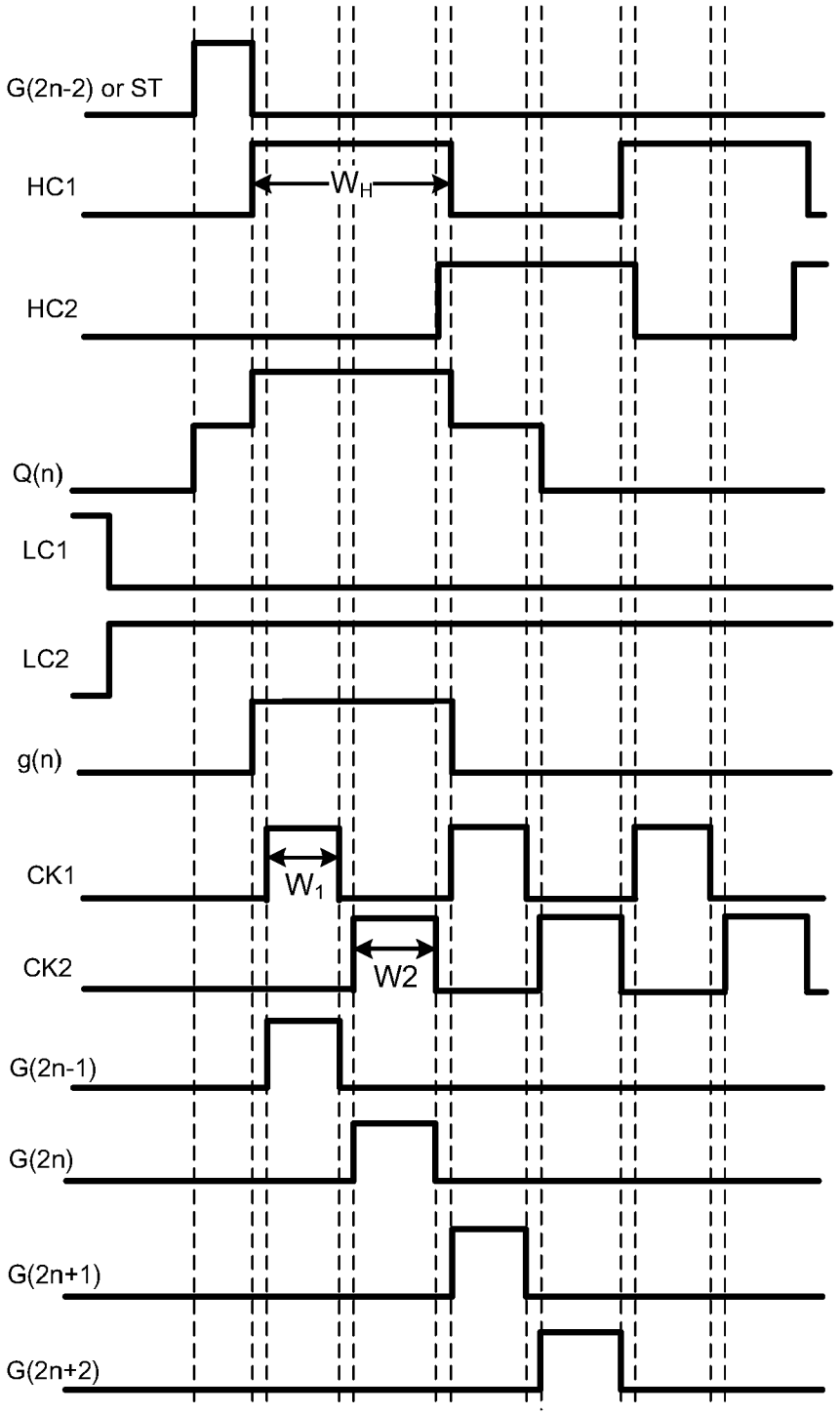
G(2n-2) or ST
HC1
W_H
HC2
Q(n)
LC1
LC2
g(n)
CK1
W_1
CK2
W2
G(2n-1)
G(2n)
G(2n+1)
G(2n+2)

Fig. 9

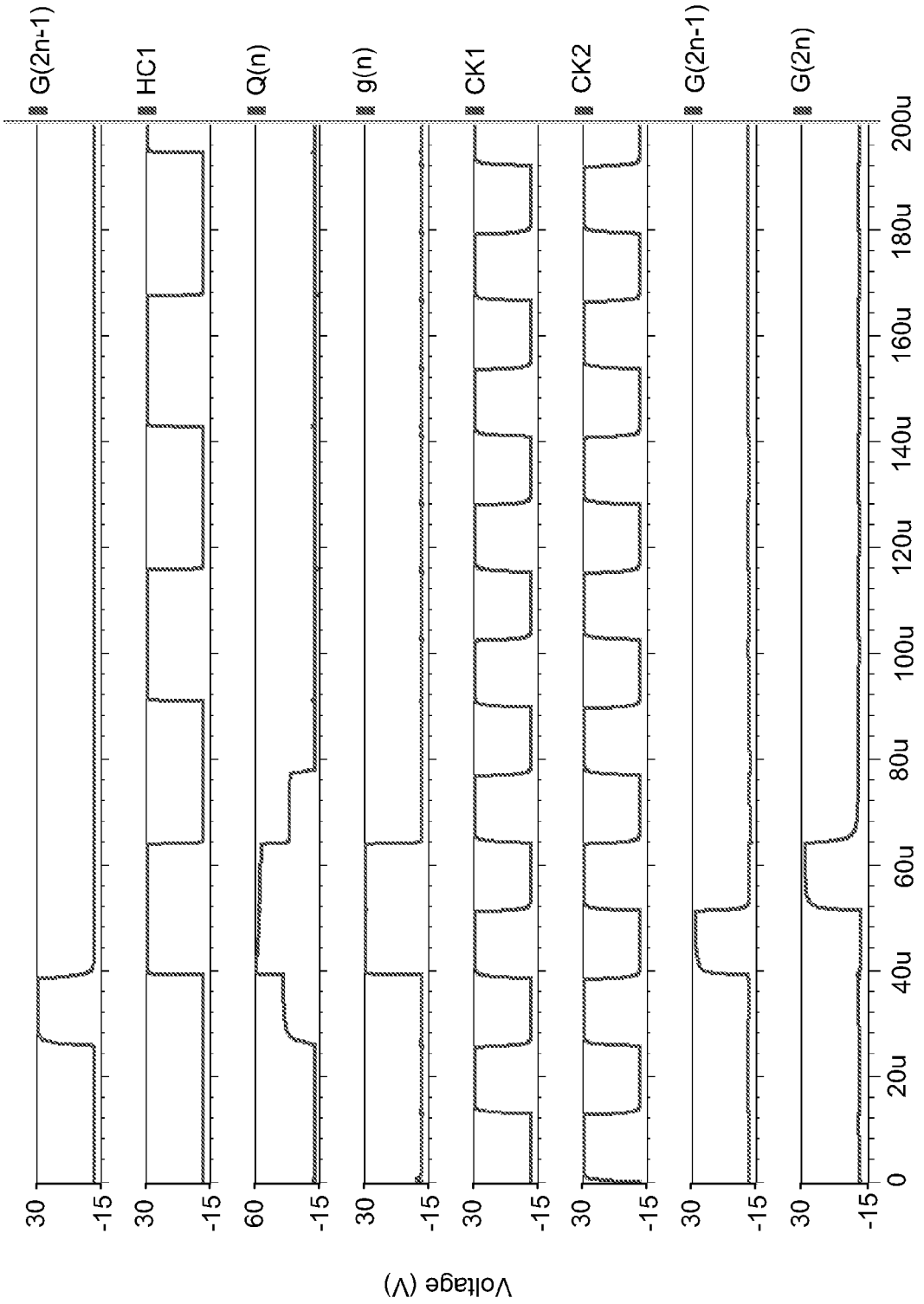
G(2n-1)
HC1
Q(n)
g(n)
CK1
CK2
G(2n-1)
G(2n)
30
-15
30
-15
60
-15
30
-15
30
-15
30
-15
30
-15
30
-15
0
20u
40u
60u
80u
100u
120u
140u
160u
180u
200u
Time (S)
Voltage (V)

Fig. 10

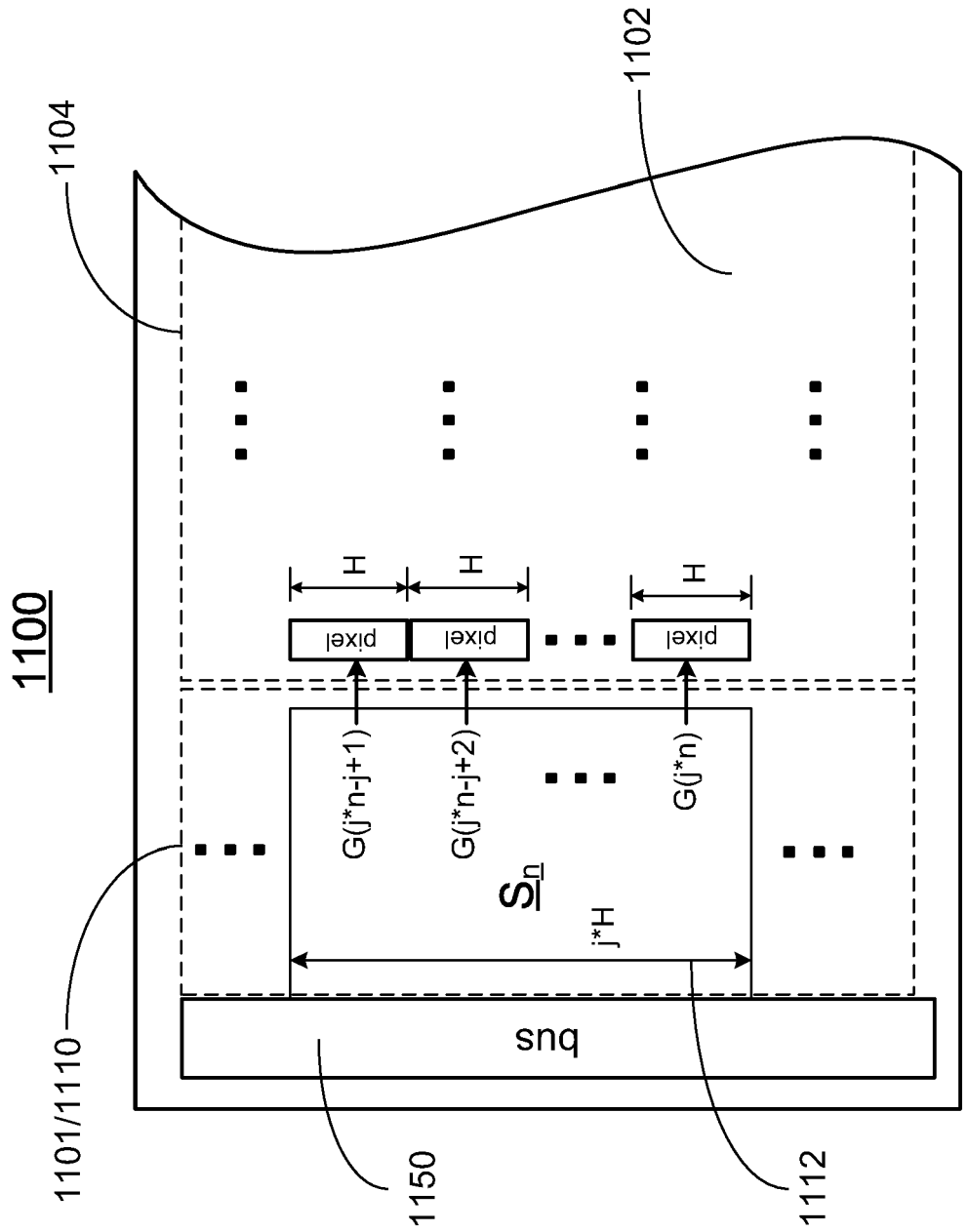
1100
1104
1102
H
H
H
pixel
pixel
pixel
G(j*n-j+1)
G(j*n-j+2)
G(j*n)
Sn
j*H
snq
1101/1110
1150
1112

Fig. 11

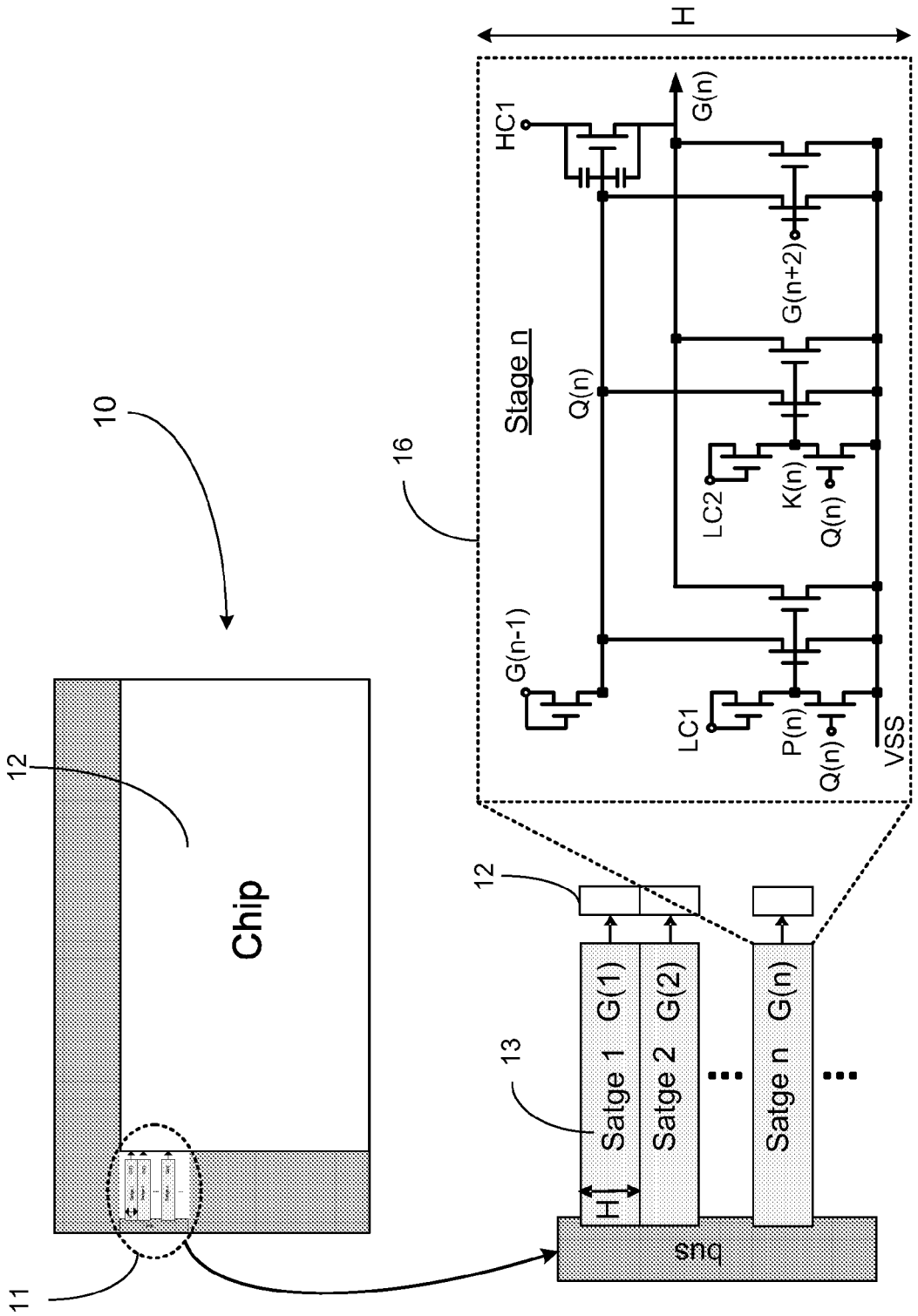

Fig. 12 (Related Art)

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EUROPEAN SEARCH REPORT

Application Number
EP 10 19 3556

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2002/163493 A1 (MATSUSHIMA YASUHIRO [JP] ET AL) 7 November 2002 (2002-11-07) * paragraphs [0098], [0159] - [0162]; figures 6-7 *	1,2,4	INV. G09G3/36 G11C19/00 G11C19/28
X	EP 1 983 500 A2 (TPO DISPLAYS CORP [TW]) 22 October 2008 (2008-10-22) * paragraphs [0019] - [0022]; figures 2-3 *	1,2,4	
X	US 2008/266275 A1 (TSAI YI-CHENG [TW] ET AL) 30 October 2008 (2008-10-30) * paragraphs [0024] - [0036]; figures 2-4 *	1	
A	US 2008/122774 A1 (JO SUNG HAK [KR] ET AL) 29 May 2008 (2008-05-29) * figures 3a,3b *	2	

TECHNICAL FIELDS SEARCHED (IPC)

G09G
G11C

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
The Hague	17 June 2011	Pichon, Jean-Michel

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

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D : document cited in the application
L : document cited for other reasons

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3

EPO FORM 1503 03.82 (P04C01)

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Application Number
EP 10 19 3556

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-7

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).

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LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 10 19 3556

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-7

   a logic function between 2 signals
   ---

2. claims: 1, 8, 9

   a stage of a shift register
   ---

3. claims: 1, 10, 11

   a scan driver on the substrate of the display panel

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 10 19 3556

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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17-06-2011

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002163493 A1	07-11-2002	NONE	
EP 1983500 A2	22-10-2008	CN 101290750 A	22-10-2008
		JP 2008268926 A	06-11-2008
		US 2008252622 A1	16-10-2008
US 2008266275 A1	30-10-2008	NONE	
US 2008122774 A1	29-05-2008	KR 20080000041 A	02-01-2008

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82