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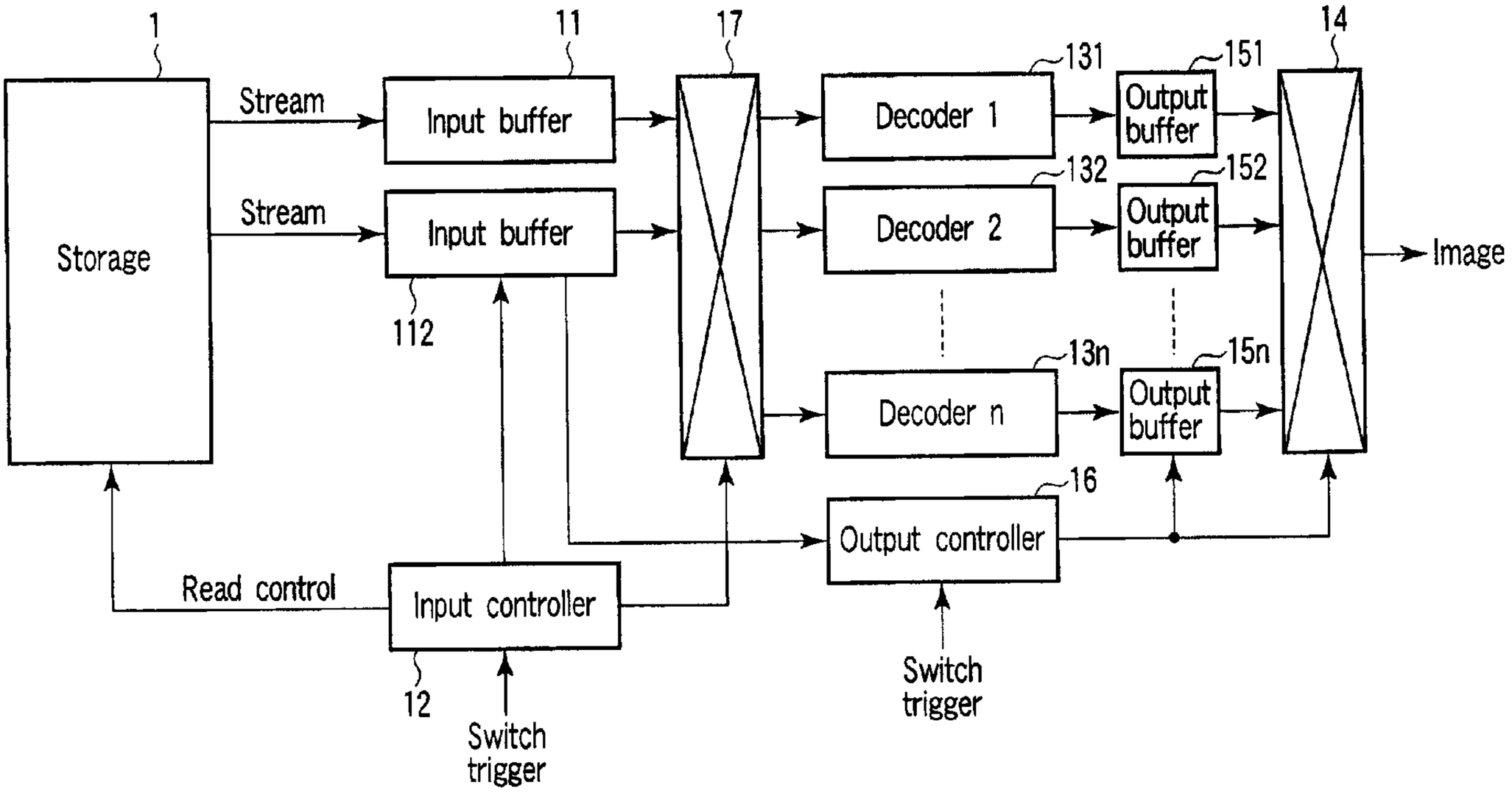
(54) Title: MULTI-DECODER AND METHOD



(57) Abrégé/Abstract:
A multi-decoder includes a plurality of decoders for different types of coding, an output buffer which stores and outputs the decoded output signal output from the decoders, an output switcher which selectively outputs the decoded output signal of the output buffer, and a controller which determines a coding scheme of the stream based on data of the header area of a stream inputted to each of the decoders, and outputs the stream to the corresponding decoder based on the determination result, and controls the output switcher to switch a decoded output signal of a sender to another decoded output signal, when inputting a stream switching signal.

ABSTRACT OF THE DISCLOSURE

A multi-decoder includes a plurality of decoders for different types of coding, an output buffer which stores and outputs the decoded output signal output from the decoders, an output switcher which selectively outputs the decoded output signal of the output buffer, and a controller which determines a coding scheme of the stream based on data of the header area of a stream inputted to each of the decoders, and outputs the stream to the corresponding decoder based on the determination result, and controls the output switcher to switch a decoded output signal of a sender to another decoded output signal, when inputting a stream switching signal.

TITLE OF THE INVENTION

MULTI-DECODER AND METHOD

BACKGROUND OF THE INVENTION

The present invention relates to a multi-decoder, which selectively switches a plurality of streams having mutually different coding to effect decoding, and to a coding method.

In recent years, ground digital broadcasting has started, and thereby, broadcasting stations handle various compression coding video signals, such as MPEG2 (Moving Picture Experts Group 2), MPEG4 and M-JPEG.

Such broadcasting stations require confirmation of a broadcasting material stream by an operator. For this reason, a decoder for decoding the broadcasting material stream to the original video signal is needed. At the broadcasting station, various types of decoder, as well as a multi-decoder, which is capable of switching between various compression coding streams, are used to reproduce the broadcasting material stream.

In such an environment, the decoding delay between decoders differs. For this reason, when an input stream is switched, a video image is instantaneously stopped, and blackout occurs, which also leads to synchronization confusion.

Conventionally, there has been proposed a digital information recorder that smoothly realizes switching of stream between different coding techniques (e.g.,

Jpn. Pat. Appln. KOKAI Publication No. 2005-11453).

However, the foregoing recorder only manages the timing between coding techniques when the stream is coded, and does not switch between various compression coding streams when decoding them.

BRIEF SUMMARY OF THE INVENTION

An object of the invention is to provide a multi-decoder, which can smoothly switch between a plurality of different coding streams without disturbing a video image, and to provide a decoding method.

According to an aspect of the present invention there is provided a multi-decoder selectively switching a plurality of streams to effect decoding, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

a plurality of decoders for different types of coding;

an input buffer connected to an input side of each of the plurality of decoders via a line for transmitting a signal, and configured to temporarily hold a stream input to each of the plurality of decoders;

an output buffer configured to store and output decoded output signals output from the plurality of decoders;

an output switcher configured to selectively output the decoded output signals of the output buffer; and

a controller configured to determine a coding scheme of the stream held in the input buffer based on data of the header area of the stream, to read out the stream from the input buffer, to output the stream to a corresponding decoder based on a determination result, and to control the output switcher so as to switch a decoded output signal of a sender to another decoded output signal, when a stream switching signal is input.

According to another aspect of the present invention there is provided a multi-decoder selectively switching a plurality of streams to effect decoding, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

a plurality of decoders for different types of coding;

an input buffer connected to an input side of each of the plurality of decoders via a line for transmitting a signal, and configured to temporarily hold a stream input to each of the plurality of decoders;

an input controller configured to determine a coding scheme of a stream held in the input buffer based on data of the header area of the stream to read the stream from the input buffer based on a determination result, and to output the stream to a corresponding decoder;

an output buffer configured to store and output decoded output signals output from the plurality of decoders;

an output switcher configured to selectively output each decoded output signal of the output buffer; and

an output controller configured to control the output switcher so as to switch a decoded output signal of a sender to another decoded output signal, when a stream switching instruction signal is input.

According to a further aspect of the present invention there is provided a method of effecting decoding using a plurality of decoders for different types of coding, which selectively switch a plurality of streams, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

temporarily holding a stream input to each of the plurality of decoders in an input buffer which is connected to an input side of said each of the

plurality of decoders via a line for transmitting a signal;

determining a coding scheme of a stream held in the input buffer based on data of the header area of the stream;

reading out the stream from the input buffer based on a determination result, and outputting the stream to a corresponding decoder;

determining whether or not a decoding delay difference is more than one frame, when a stream switching instruction signal is input;

outputting a switching destination stream from the input buffer or a stream sender to the corresponding decoder, before a stream switching time by a time equivalent to the decoding delay difference, in a state of outputting a switching original stream to the corresponding decoder, when the decoding delay difference is more than one frame; and

switching a signal from a switching original decoded output signal to a switching destination decoded output signal, and outputting the switching destination decoded output signal.

According to a further aspect of the present invention there is provided a method of effecting decoding using a plurality of decoders for different types of coding, which selectively switch a plurality of streams, the plurality of streams including

mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

temporarily holding a stream input to each of the plurality of decoders in an input buffer which is connected to an input side of said each of the plurality of decoders via a line for transmitting a signal;

determining a coding scheme of a stream held in the input buffer based on data of the header area of the stream;

reading out the stream from the input buffer based on a determination result, and outputting the stream to a corresponding decoder;

determining whether or not a decoding delay difference is more than one frame, when a stream switching instruction signal is input; and

switching to a switching destination decoded output signal from a switching original decoded output signal delayed by a time equivalent to the decoding delay difference, and outputting the switching destination decoded output signal, when the decoding delay difference is more than one frame.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and

advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention, and together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a block diagram showing the configuration of a multi-decoder according to a first embodiment of the invention;

FIG. 2A is a view to explain an operation of a switching original stream in the first embodiment;

FIG. 2B is a view to explain an operation of a switching destination stream in the first embodiment;

FIG. 2C is a view to explain a decoding output operation of the switching original stream in the first embodiment;

FIG. 2D is a view to explain a decoding output operation of the switching destination stream in the first embodiment;

FIG. 2E is a view to explain an output signal of a output buffer in the first embodiment;

FIG. 3 is a flowchart to explain an operation by an input controller in the first embodiment;

FIG. 4A is a view to explain an operation of a switching original stream according to a second embodiment;

FIG. 4B is a view to explain an operation of a switching destination stream in the second embodiment;

FIG. 4C is a view to explain a decoding output operation of the switching original stream in the second embodiment;

FIG. 4D is a view to explain a decoding output operation of the switching destination stream in the second embodiment;

FIG. 4E is a view to explain an output signal of a output buffer in the second embodiment; and

FIG. 5 is a flowchart to explain an operation by an output controller in the second embodiment.

DETAILED DESCRIPTION OF THE INVENTION

Various embodiments of the invention will be

hereinafter described with reference to the accompanying drawings.

(First embodiment)

FIG. 1 is a block diagram showing the configuration of a multi-decoder according to a first embodiment of the invention. The multi-decoder inputs a stream having a frame structure including a header and data output from a storage 1. The stream is temporarily held in input buffers 111 and 112. The stream held in these input buffers 111 and 112 is decoded in the following manner. Specifically, an input controller 12 analyzes header data to determine coding scheme, and thereafter, reads the header data to decode them using corresponding code scheme decoders 131 to 13n. Output signal from these input buffers 111 and 112 are decoded by corresponding code scheme decoders 131 to 13n.

Decoded output signals from these decoders 131 to 13n are stored in output buffers 151 to 15n. Decoded output signals from these output buffers 151 to 15n are selectively output by an output switcher 14.

An output controller 16 controls the switching of the foregoing output switcher 14 in units of frames.

The input controller 12 analyzes the header data of the stream held in the input buffers 111 and 112 to determine the kind of the stream. Thereafter, the input controller 12 sends a stream shown in FIG. 2A to

the corresponding decoder 131. In this case, if the operator manually switches the stream without automatically switching it, the operator makes a switch into the decoder corresponding to the stream using the input switcher 17.

The input controller 12 determines that the decoding delay difference is several frames from the header data of a switching original stream of the input buffers 111 and that of a switching destination stream stored in the input buffer 112 or the storage 1. In this case, when receiving a switching trigger from an upper system, the input controller 12 reads a stream shown in FIG. 2B from the input buffer 112 or storage 1 in a period of time that is shorter than that of the decoding delay from the time when the output switcher 14 switches the stream. Thereafter, the input controller outputs the stream to the corresponding decoder 132. In this case, the input buffer 111 is in a state of outputting the switching original stream to the corresponding decoder 131.

Each output of the decoders 131 and 132 is as shown in FIG. 2C and FIG. 2D, which is then input to the output buffers 151 and 152. When receiving a signal (switching trigger) such that an input stream is switched, the output controller 16 switches the output switcher 14 to selectively output each decoded output signal of output buffer 151 and 152.

The output buffer 15 taking output timing to read the stream, and as shown in FIG. 2E, the delay difference within one frame is absorbed and synchronized.

FIG. 3 is a flowchart to explain the procedures performed by the input controller 12.

The input controller 12 determines whether or not auto mode is set (step ST3a). If the auto mode is set (Yes), the input controller 12 determines the kind of stream from the header of the streams held in the input buffers 111 and 112 (step ST3b).

The input controller 12 determines whether or not a switching trigger is input from a system upstream (step ST3c). If the switching trigger is input (Yes), the controller 12 determines the decoding delay difference based on the header of the switching original stream held in the input buffer 111 and that of the switching destination stream held in the input buffer 112 (step ST3d). For example, the controller 12 determines whether or not the difference is more than one frame (step ST3e). If the difference is less than one frame (No), the input controller 12 intactly outputs the switching destination stream to the corresponding decoder 132.

Conversely, if the difference is more than one frame (Yes), the input controller 12 previously reads the switching destination stream in a period of time

that is shorter than that of the decoding delay from the time when the output switcher 14 switches the stream. Then, the controller 12 outputs the stream to the corresponding decoder 132 (step ST3f).

When receiving the switching trigger, the output controller 16 switches the output switcher 14 to selectively output each decoded output signal of the output buffers 151 and 152.

As described above, according to the first embodiment, the decoding delay difference within one frame between decoders 131 to 13n is absorbed using the input and output buffers 111 to 11n and 15 as input and output stages of decoders 131 to 13n. The input controller 12 determines the decoding delay difference using the header data of the switching original stream held in the input buffers 111 to 11n and that of the switching destination stream held in the input buffer 111 to 11n or supplied separately by a system upstream. If the delay difference is more than one frame, the output controller 16 controls the switching of the output switcher 14 in the following manner. Specifically, in a state that the switching original stream from the input buffer 111 to 11n is read, the input buffers 111 to 11n or stream sender reads the switching destination stream in a period of time that is shorter than that of the decoding delay difference when the stream is switched. The switching destination

stream is output to the corresponding decoder 132 so that the timing of input to the output switcher 14 is synchronized between the switching original stream and the switching destination stream.

Therefore, the output controller 16 readily controls the switching timing of the output switcher 14. In this way, it is possible to smoothly switch a plurality of streams having different coding to reproduce an uninterrupted video image.

(Second embodiment)

FIG. 4 shows stream switching timing according to a second embodiment of the invention.

The input controller 12 analyzes header data of a stream held in the input buffer 11 to determine the kind of the stream. The controller sends a stream shown in FIG. 4A to the corresponding decoder 131.

A stream shown in FIG. 4B is input to the decoder 132.

The decoded output signals of the decoders are as shown in FIG. 4C and FIG. 4D. These signals are then input to the output switcher 14. When receiving a switching trigger, the output controller 16 determines whether or not the decoding delay difference of the decoder is several frames from header data of the switching original stream of the input buffer 111 and that of the switching destination stream in the input buffer 112 or output from the storage 1. If the

decoding delay difference is several frames, the output switcher 14 is switched, delayed by the decoding delay of the decoder, to selectively output each decoded output signal of the output buffers 151 and 152.

As shown in FIG. 4E, the output buffer 15 reads frames in synchrony with the output timing, and controls the difference between write address and read address so that the amount of the decoder delay and the delay of the output buffer 15 become constant.

FIG. 5 is a flowchart to explain the procedure performed by the output controller 16.

The output controller 16 determines whether or not auto mode is set (step ST5a). If the auto mode is set (Yes), the output controller 1 determines whether or not a switching trigger is input from the upper system (step ST5b).

If the switching trigger is input (Yes), the output controller 16 determines the decoding delay difference based on the header of the switching original stream held in the input buffer 111 and that of the switching destination stream held in the input buffer 112 (step ST5c). For example, the controller 16 determines whether or not the difference is more than one frame (step ST5d).

If the difference is less than one frame (No), the output controller 16 intactly switches the output switcher 14 from a switching original decoded output

signal to a switching destination decoded output signal (step ST5e).

Conversely, if the difference is more than one frame (Yes), the output controller 16 switches the output switcher 14 delayed by the decoding delay of the decoder to selectively output each decoded output signal of the output buffers 151 and 152.

As described above, according to the second embodiment, even if the stream is input to the decoders 131 to 13n in a state that the timing is not synchronized between decoders 131 to 13n, the output controller 16 controls the timing. Thus, the same effect as in the first embodiment is obtained.

The present invention is not limited to the foregoing embodiments. In this case, the configuration of the multi-decoder and stream switching procedures may be variously modified departing from the subject matter of the invention.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A multi-decoder selectively switching a plurality of streams to effect decoding, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

a plurality of decoders for different types of coding;

an input buffer connected to an input side of each of the plurality of decoders via a line for transmitting a signal, and configured to temporarily hold a stream input to each of the plurality of decoders;

an output buffer configured to store and output decoded output signals output from the plurality of decoders;

an output switcher configured to selectively output the decoded output signals of the output buffer; and

a controller configured to determine a coding scheme of the stream held in the input buffer based on data of the header area of the stream, to read out the stream from the input buffer, to output the stream to a corresponding decoder based on a determination result, and to control the output switcher so as to switch a decoded output signal of a sender to another decoded output signal, when a stream switching signal is input.

2. The multi-decoder according to claim 1, wherein the controller includes:

an input controller configured to determine, based on data of the header area of a stream input to each of the decoders, a coding scheme of the stream and output the

stream to the corresponding decoder based on the determination result; and

an output controller configured to control the output switcher to switch a decoded output signal of a sender to another decoded output signal, when inputting a stream switching signal.

3. The multi-decoder according to claim 1, wherein the controller includes

a unit configured to determine whether or not a decoding delay difference is more than one frame based on data of the header area of a switching original stream and data of the header area of a header area of a switching destination stream, and to generate a result, when a decoding delay difference is more than one frame, and

a unit configured to output the switching destination stream to the corresponding decoder before a time equivalent to the decoding delay difference from a stream switching time in a state of outputting the switching original stream to a decoder, in response to the result.

4. The multi-decoder according to claim 1, wherein the controller includes

a unit configured to determine whether or not a decoding delay difference is more than one frame based on data of the header area of a switching original stream and data of the header area of a switching destination stream, and to generate a result, when the decoding delay difference is more than one frame, and

a unit configured to delay switching of a decoded output signal by the output switcher by a time equivalent to the decoding delay difference, in response to the result.

5. A multi-decoder selectively switching a plurality of streams to effect decoding, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

a plurality of decoders for different types of coding;

an input buffer connected to an input side of each of the plurality of decoders via a line for transmitting a signal, and configured to temporarily hold a stream input to each of the plurality of decoders;

an input controller configured to determine a coding scheme of a stream held in the input buffer based on data of the header area of the stream to read the stream from the input buffer based on a determination result, and to output the stream to a corresponding decoder;

an output buffer configured to store and output decoded output signals output from the plurality of decoders;

an output switcher configured to selectively output each decoded output signal of the output buffer; and

an output controller configured to control the output switcher so as to switch a decoded output signal of a sender to another decoded output signal, when a stream switching instruction signal is input.

6. The multi-decoder according to claim 5, wherein the input controller includes

a unit configured to determine whether or not a decoding delay difference is more than one frame based on data of the header area of a switching original stream of the input buffer and data of the header area of a switching destination stream of the input buffer or separately

supplied, and to generate a result, when the decoding delay difference is more than one frame, and

a unit configured to read the switching destination stream from the input buffer or a stream sender to output the stream switching destination to the corresponding decoder, before a time equivalent to the decoding delay difference from the stream switching time in a state of reading the switching destination stream, in response to the result.

7. The multi-decoder according to claim 5, wherein the input controller includes

a unit configured to determine whether or not a decoding delay difference is more than one frame based on data of the header area of a switching original stream of the input buffer and data of the header area of a switching destination stream of the input buffer or separately supplied, and to generate a result, when the decoding delay difference is more than one frame, and

a unit configured to delay switching of a decoded output signal by the output switcher by a time equivalent to the decoding delay difference, in response to the result.

8. A method of effecting decoding using a plurality of decoders for different types of coding, which selectively switch a plurality of streams, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

temporarily holding a stream input to each of the plurality of decoders in an input buffer which is connected

to an input side of said each of the plurality of decoders via a line for transmitting a signal;

determining a coding scheme of a stream held in the input buffer based on data of the header area of the stream;

reading out the stream from the input buffer based on a determination result, and outputting the stream to a corresponding decoder;

determining whether or not a decoding delay difference is more than one frame, when a stream switching instruction signal is input;

outputting a switching destination stream from the input buffer or a stream sender to the corresponding decoder, before a stream switching time by a time equivalent to the decoding delay difference, in a state of outputting a switching original stream to the corresponding decoder, when the decoding delay difference is more than one frame; and

switching a signal from a switching original decoded output signal to a switching destination decoded output signal, and outputting the switching destination decoded output signal.

9. A method of effecting decoding using a plurality of decoders for different types of coding, which selectively switch a plurality of streams, the plurality of streams including mutually different coding, and each of the plurality of streams having a frame structure including a header area and an information area, comprising:

temporarily holding a stream input to each of the plurality of decoders in an input buffer which is connected to an input side of said each of the plurality of decoders via a line for transmitting a signal;

determining a coding scheme of a stream held in the input buffer based on data of the header area of the stream;

reading out the stream from the input buffer based on a determination result, and outputting the stream to a corresponding decoder;

determining whether or not a decoding delay difference is more than one frame, when a stream switching instruction signal is input; and

switching to a switching destination decoded output signal from a switching original decoded output signal delayed by a time equivalent to the decoding delay difference, and outputting the switching destination decoded output signal, when the decoding delay difference is more than one frame.

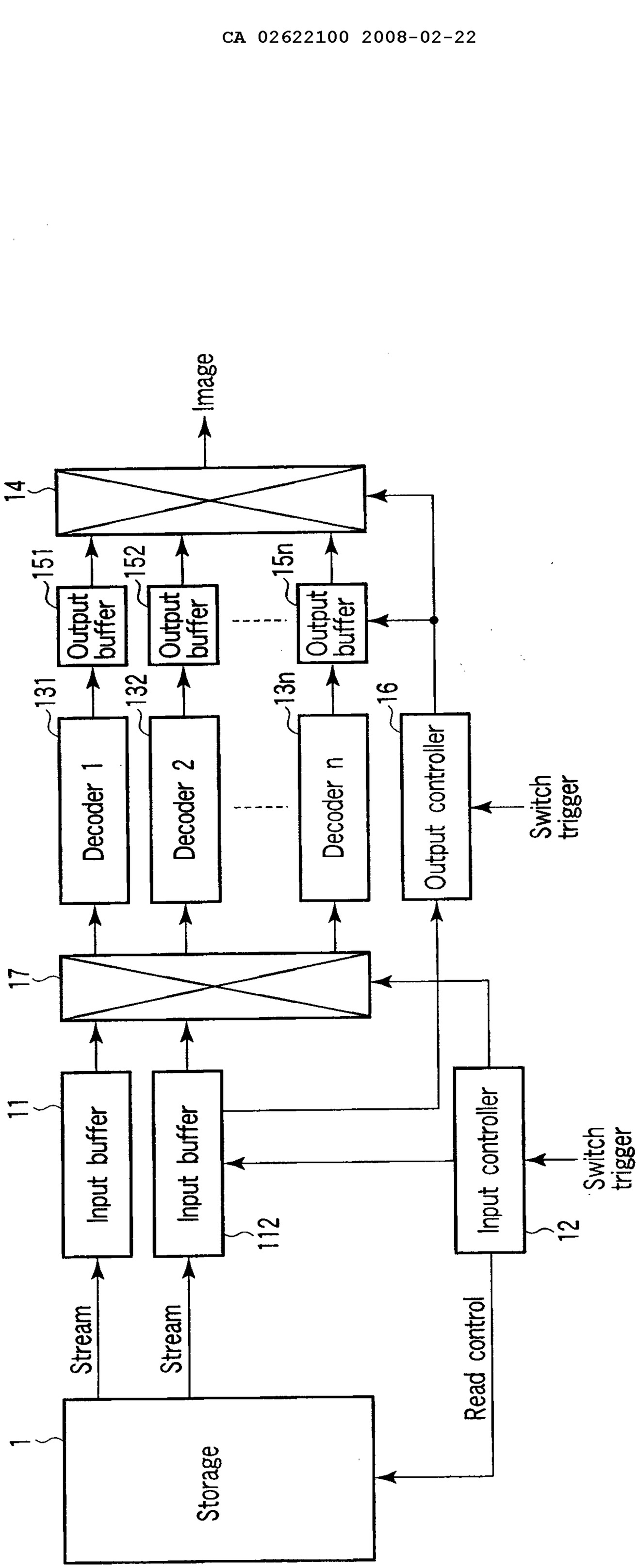


Image
14
151
152
15n
Output buffer
Output buffer
Output buffer
131
132
13n
16
Decoder 1
Decoder 2
Decoder n
Output controller
Switch trigger
17
11
112
12
Input buffer
Input buffer
Input controller
Switch trigger
Stream
Stream
Read control
1
Storage

FIG. 1

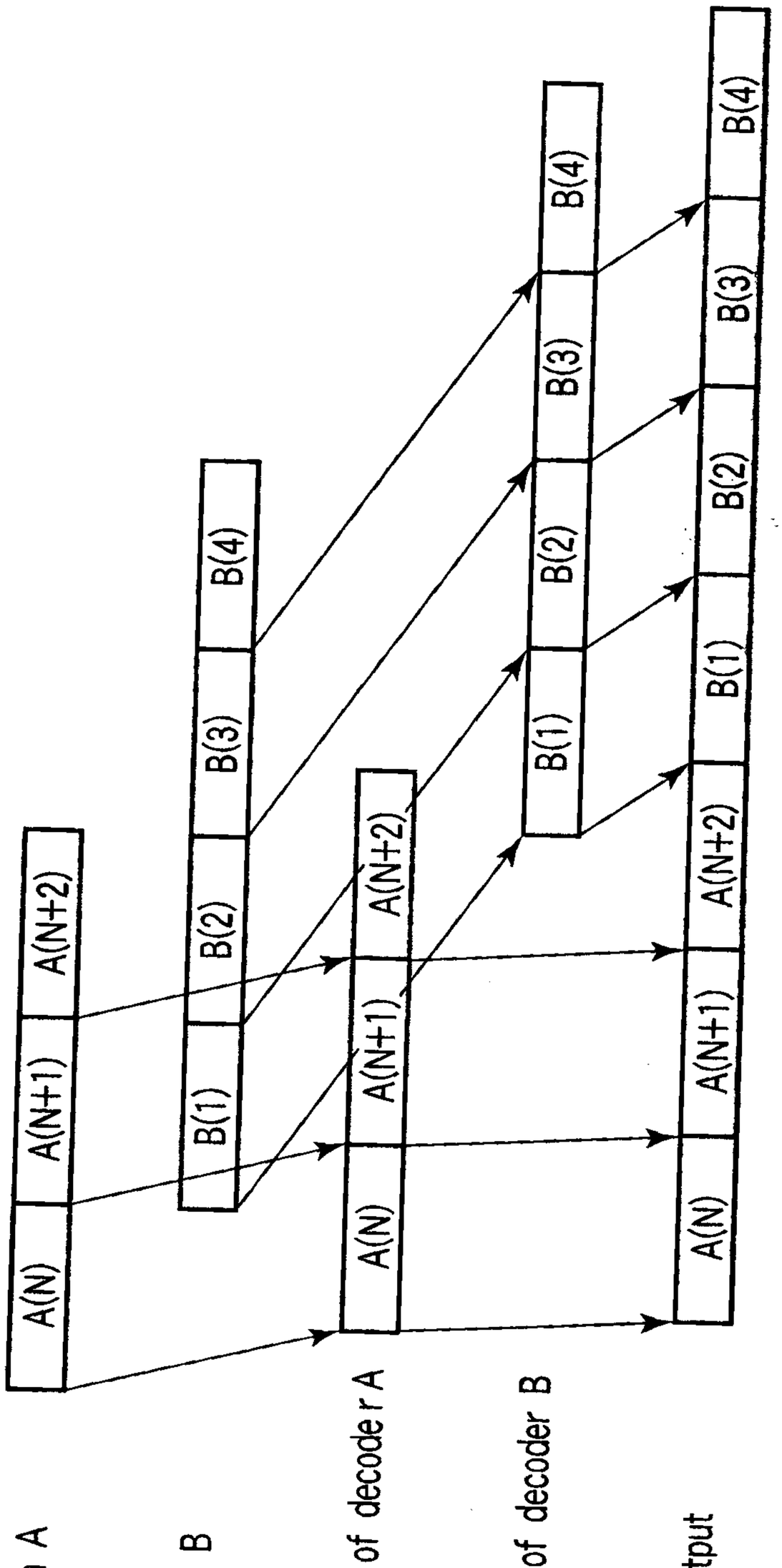


FIG. 2A Stream A

FIG. 2B Stream B

FIG. 2C Output of decoder A

FIG. 2D Output of decoder B

FIG. 2E Final output

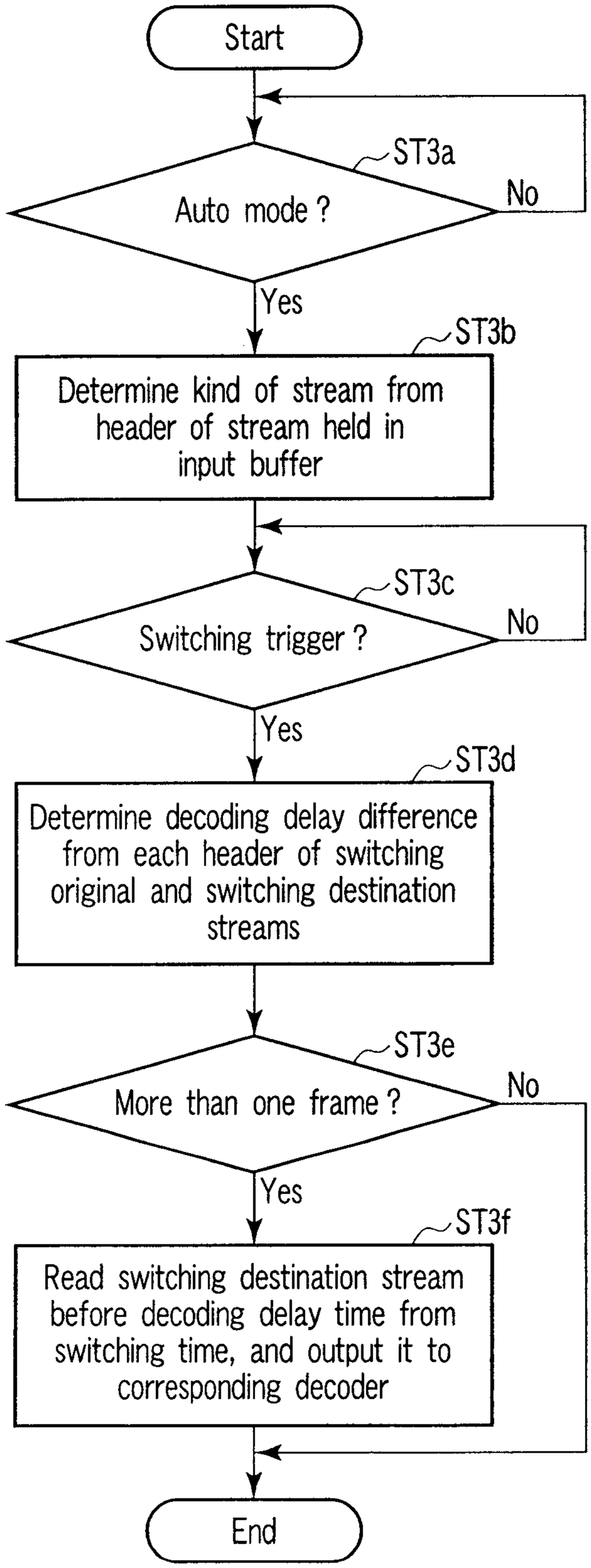

Start
ST3a
Auto mode ?
No
Yes
ST3b
Determine kind of stream from header of stream held in input buffer
ST3c
Switching trigger ?
No
Yes
ST3d
Determine decoding delay difference from each header of switching original and switching destination streams
ST3e
More than one frame ?
No
Yes
ST3f
Read switching destination stream before decoding delay time from switching time, and output it to corresponding decoder
End

FIG. 3

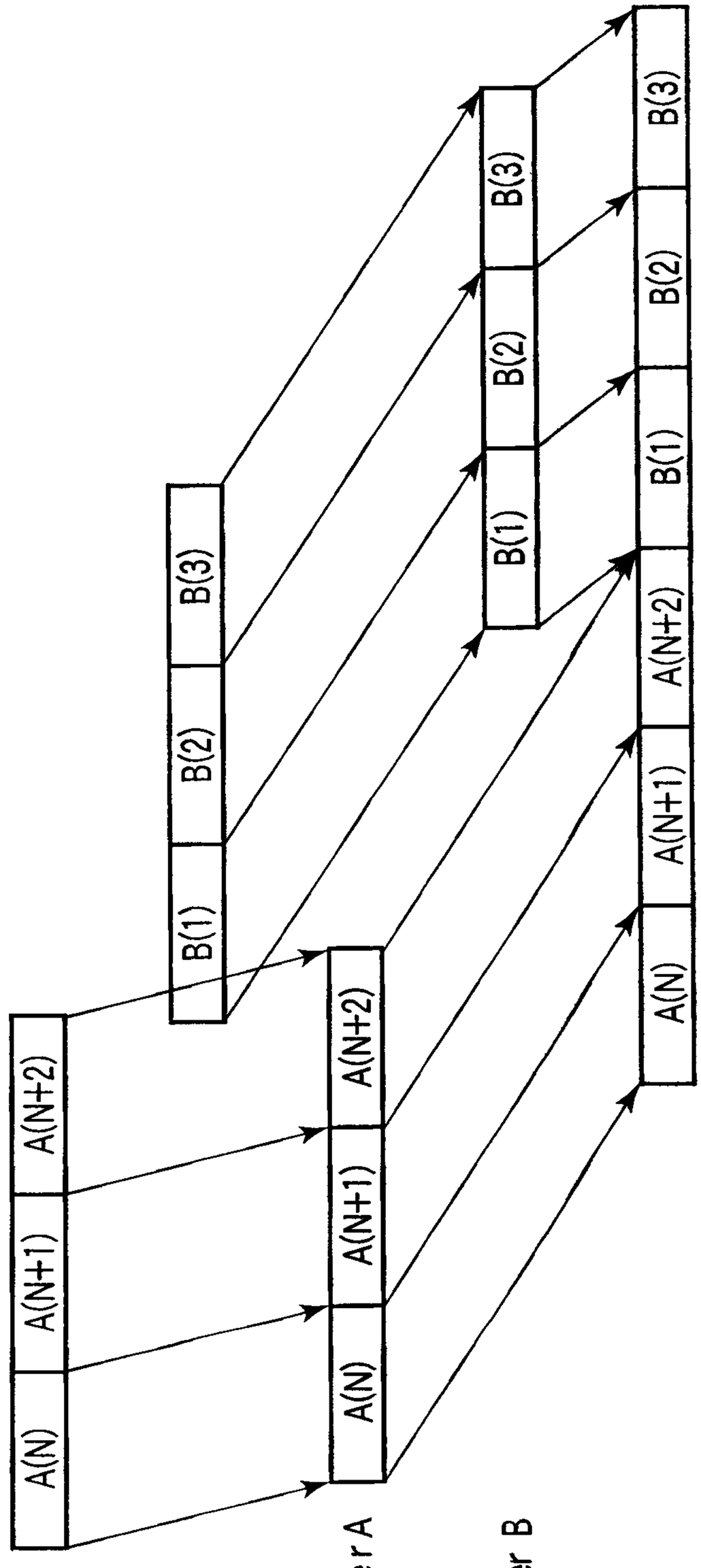


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

FIG. 4E

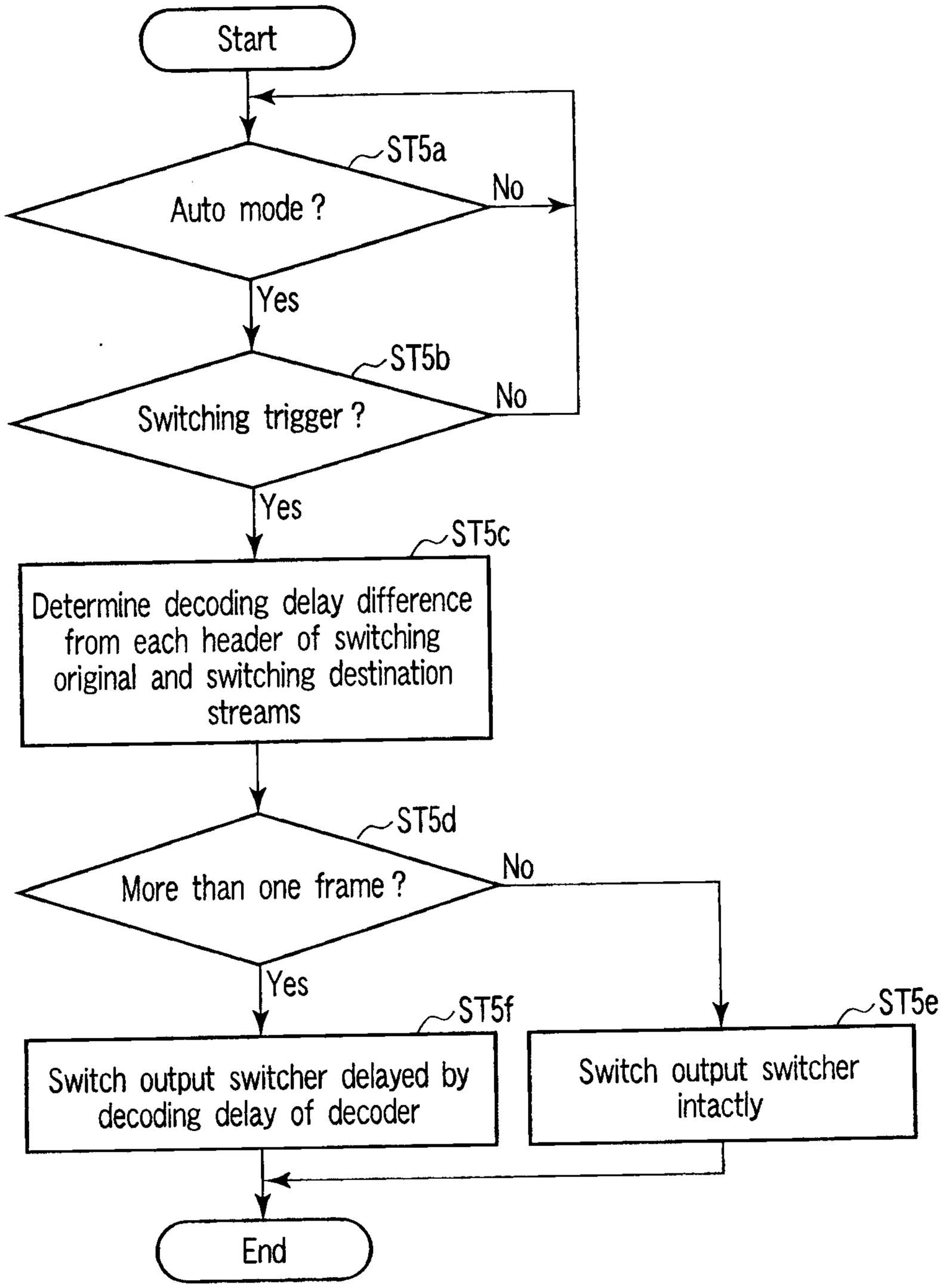
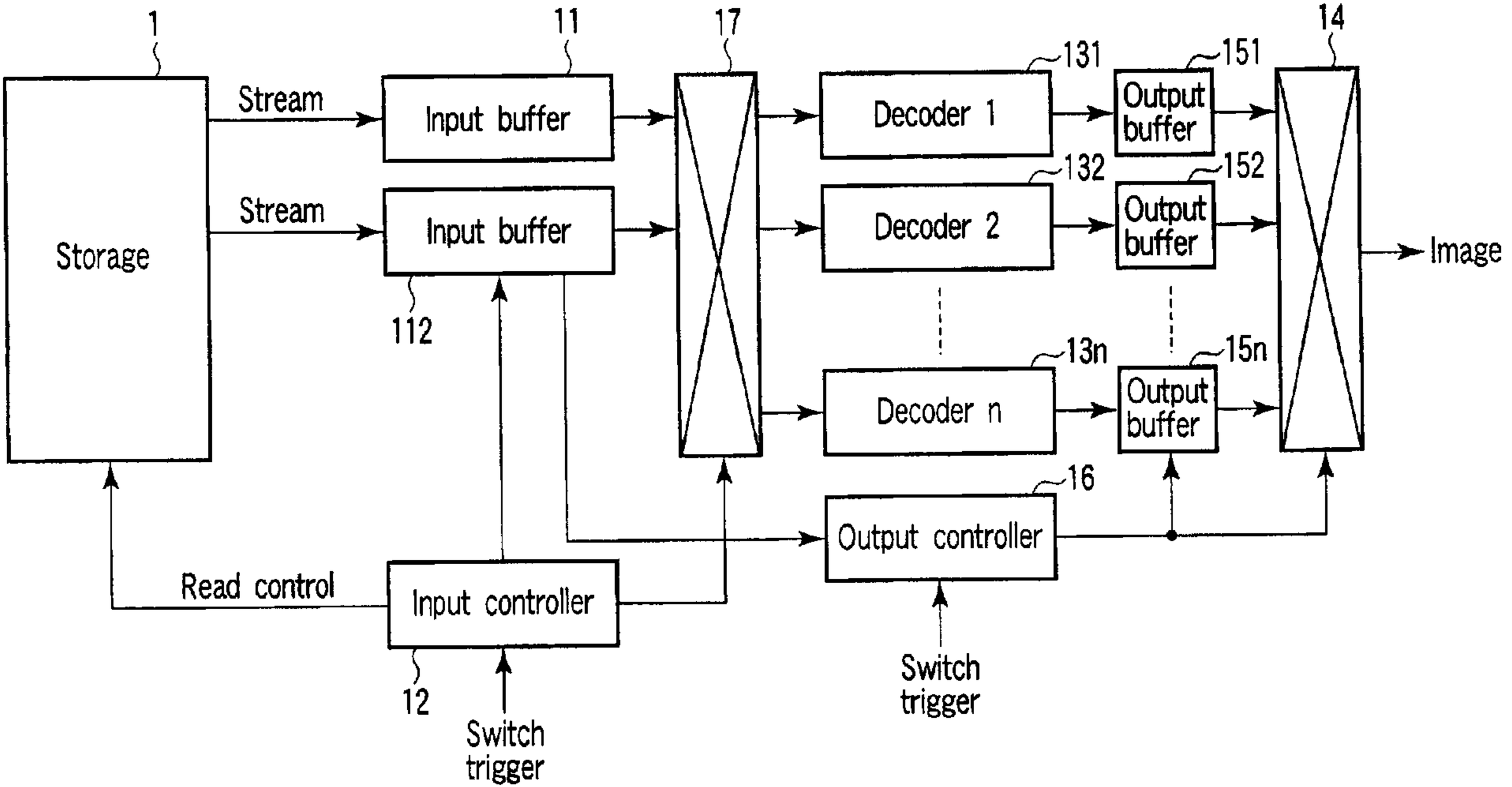

Start
ST5a
Auto mode ?
No
Yes
ST5b
Switching trigger ?
No
Yes
ST5c
Determine decoding delay difference from each header of switching original and switching destination streams
ST5d
More than one frame ?
No
Yes
ST5f
Switch output switcher delayed by decoding delay of decoder
ST5e
Switch output switcher intactly
End

FIG. 5


1
11
17
14
131
151
Storage
Stream
Input buffer
Decoder 1
Output buffer
Stream
Input buffer
132
152
Decoder 2
Output buffer
Image
112
13n
15n
Decoder n
Output buffer
16
Output controller
Read control
Input controller
12
Switch trigger
Switch trigger