US 20190109141A1

(19) **United States**

(12) **Patent Application Publication**

Lee et al.

(10) **Pub. No.: US 2019/0109141 A1**

(43) **Pub. Date: Apr. 11, 2019**

(54) **FLEXIBLE MERGE SCHEME FOR SOURCE/DRAIN EPITAXY REGIONS**

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(21) Appl. No.: **16/206,183**

(22) Filed: **Nov. 30, 2018**

Related U.S. Application Data

(62) Division of application No. 15/492,142, filed on Apr. 20, 2017.

Publication Classification

(51) **Int. Cl.**

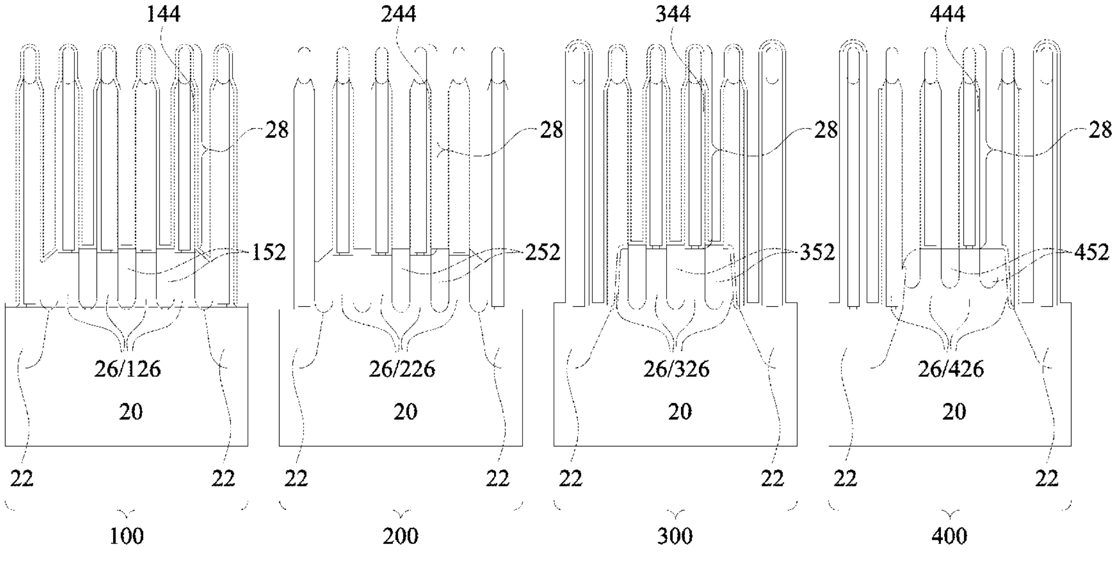
H01L 27/11	(2006.01)
H01L 21/8234	(2006.01)
H01L 29/66	(2006.01)
H01L 21/027	(2006.01)
H01L 21/306	(2006.01)
H01L 21/311	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 27/1104*** (2013.01); ***H01L 21/823431*** (2013.01); ***H01L 21/823418*** (2013.01); ***H01L 29/66636*** (2013.01); ***H01L 21/823437*** (2013.01); ***H01L 27/1116*** (2013.01); ***H01L 29/6656*** (2013.01); ***H01L 21/30604*** (2013.01); ***H01L 21/31111*** (2013.01); ***H01L 21/31144*** (2013.01); ***H01L 21/0273*** (2013.01)

(57) **ABSTRACT**

A method includes etching a first semiconductor fin and a second semiconductor fin to form first recesses. The first and the second semiconductor fins have a first distance. A third semiconductor fin and a fourth semiconductor fin are etched to form second recesses. The third and the fourth semiconductor fins have a second distance equal to or smaller than the first distance. An epitaxy is performed to simultaneously grow first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses. The first epitaxy semiconductor regions are merged with each other, and the second epitaxy semiconductor regions are separated from each other.



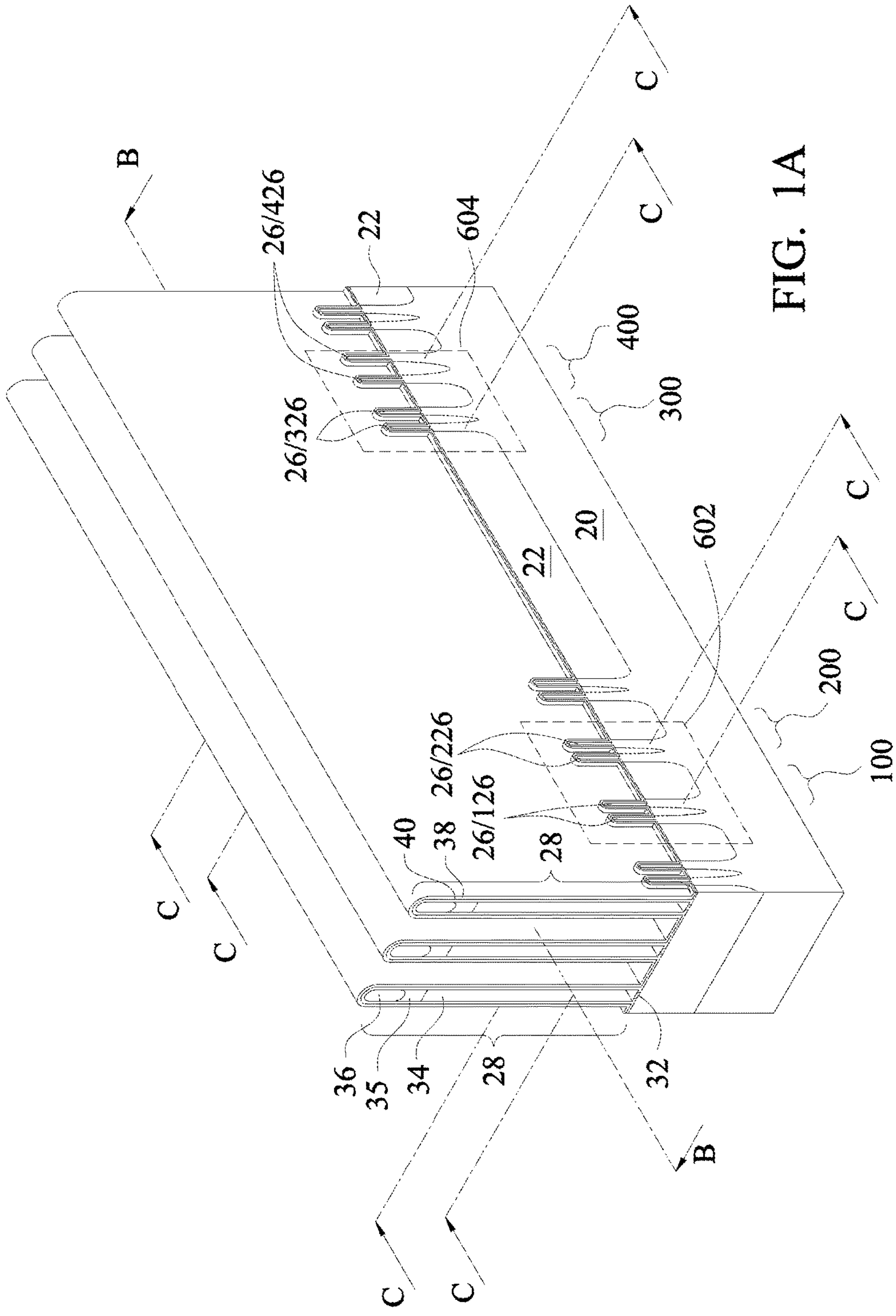

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FIG. 1A

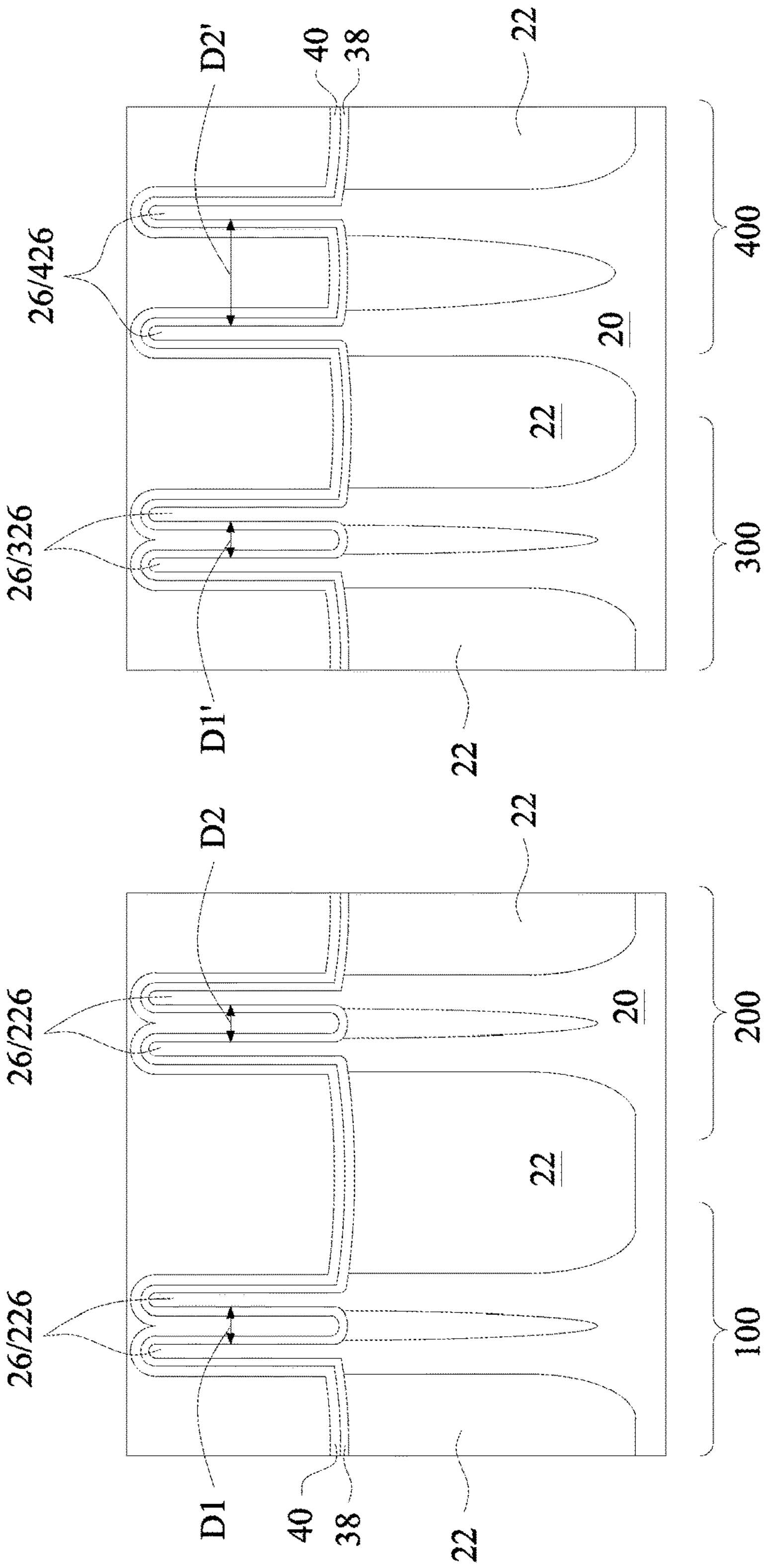
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FIG. 1B

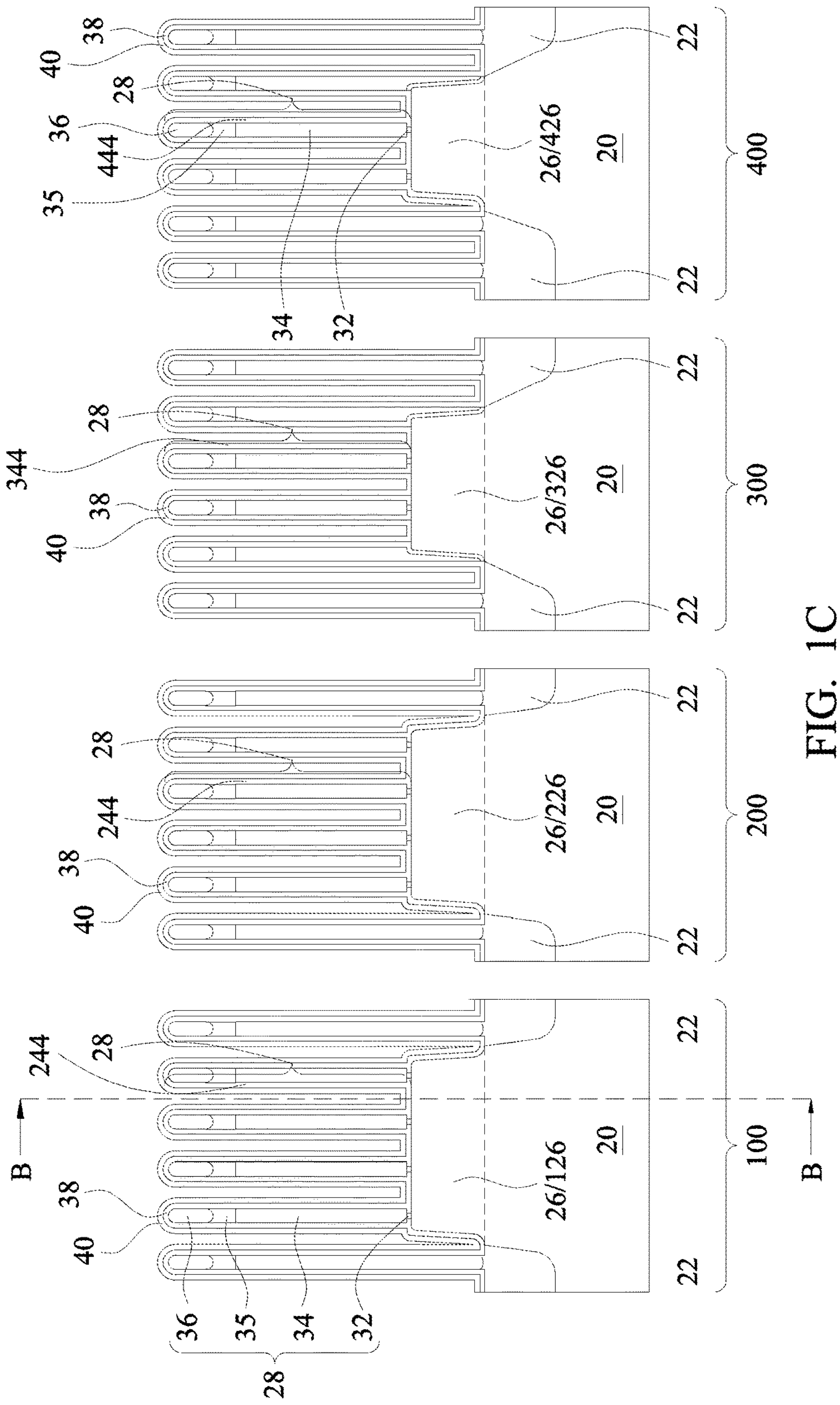
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FIG. 1C

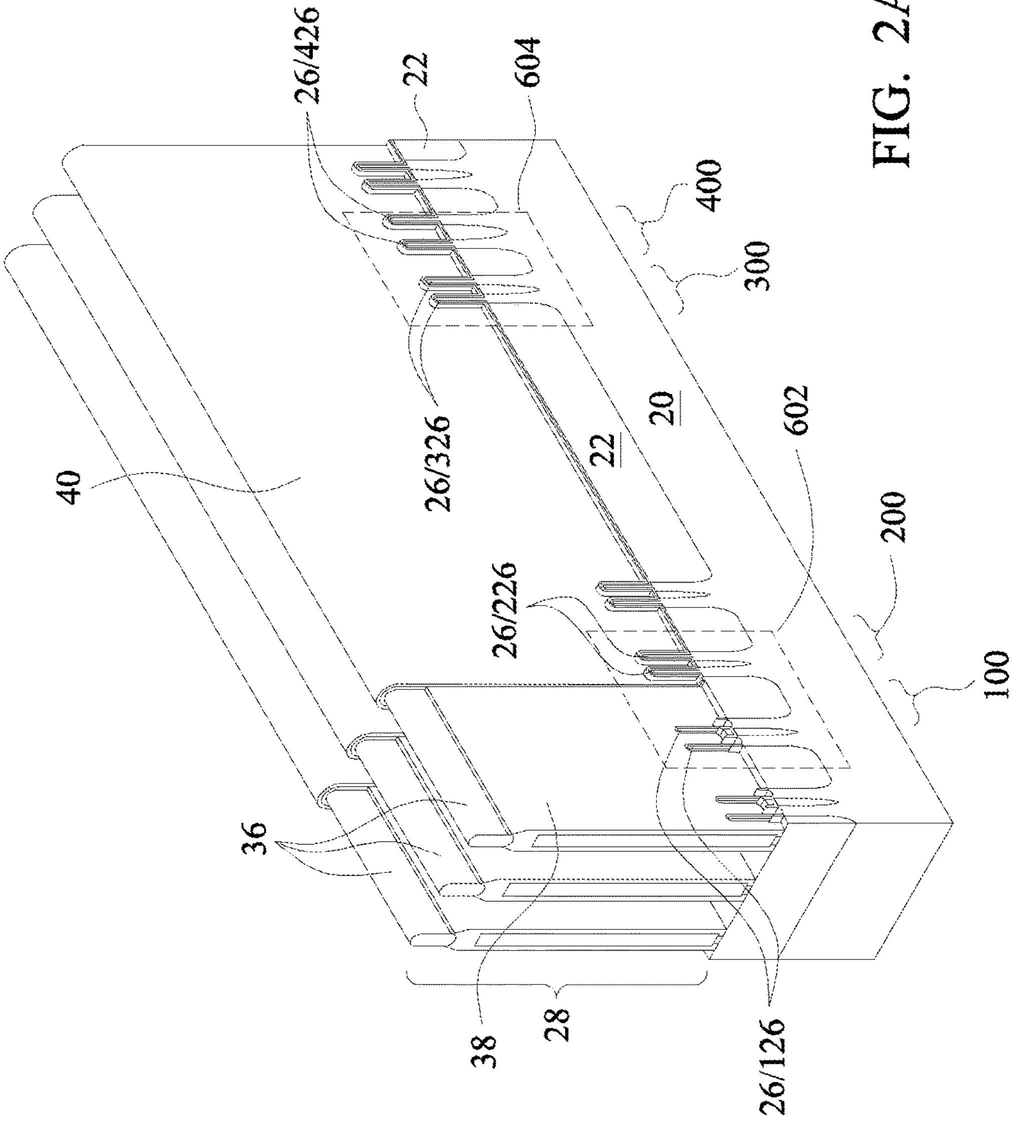
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FIG. 2A

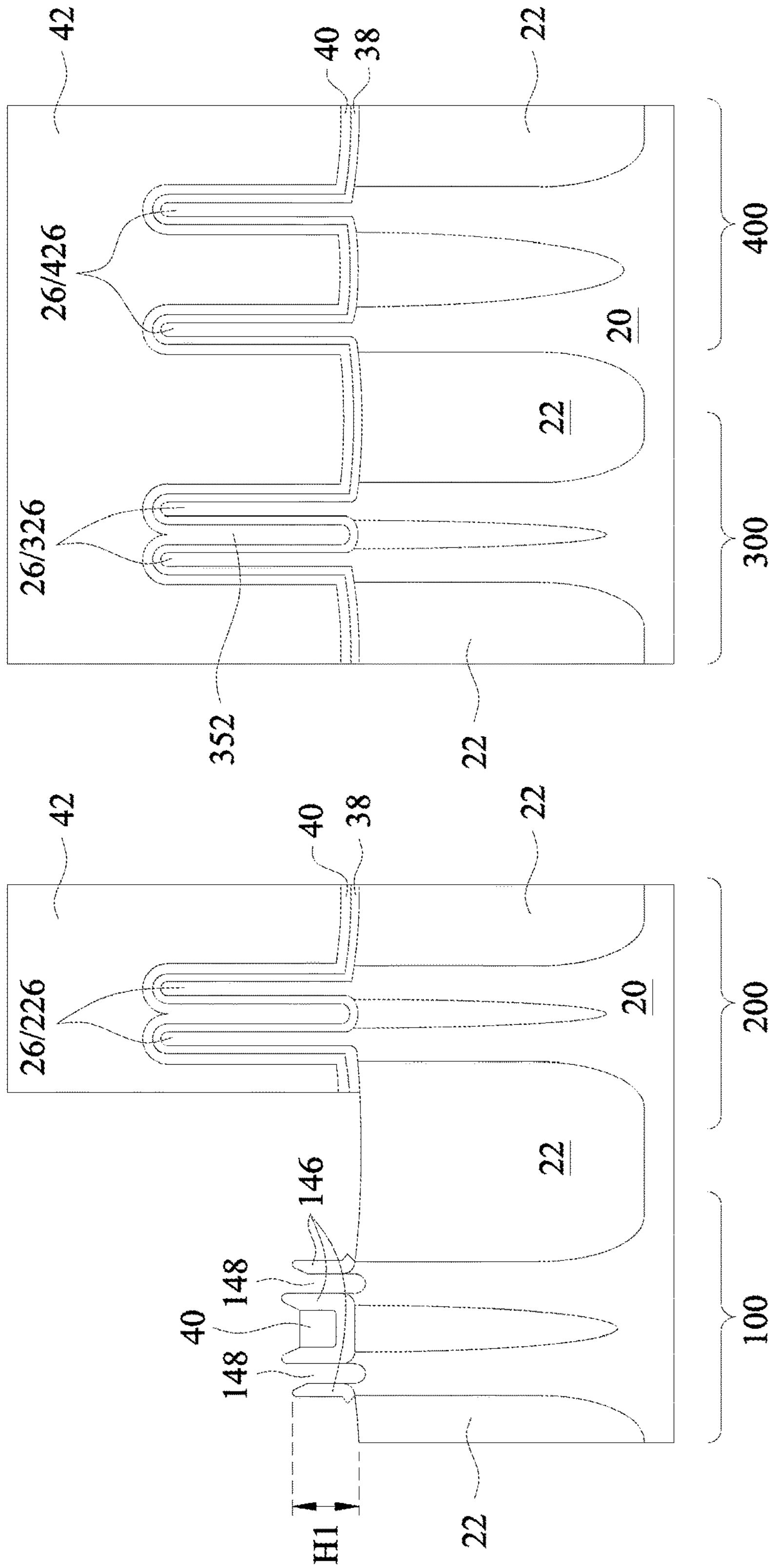
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FIG. 2B

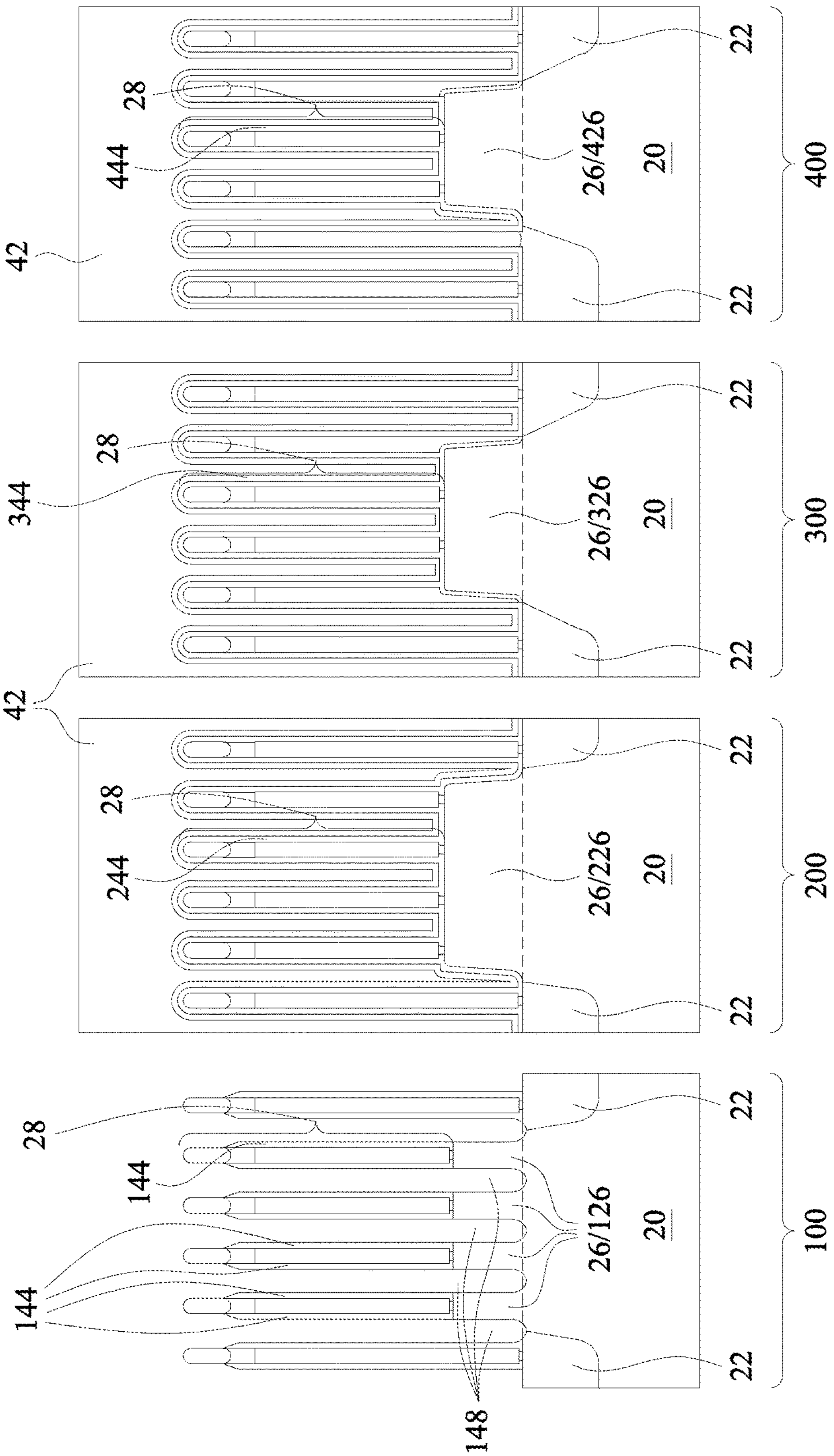
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FIG. 2C

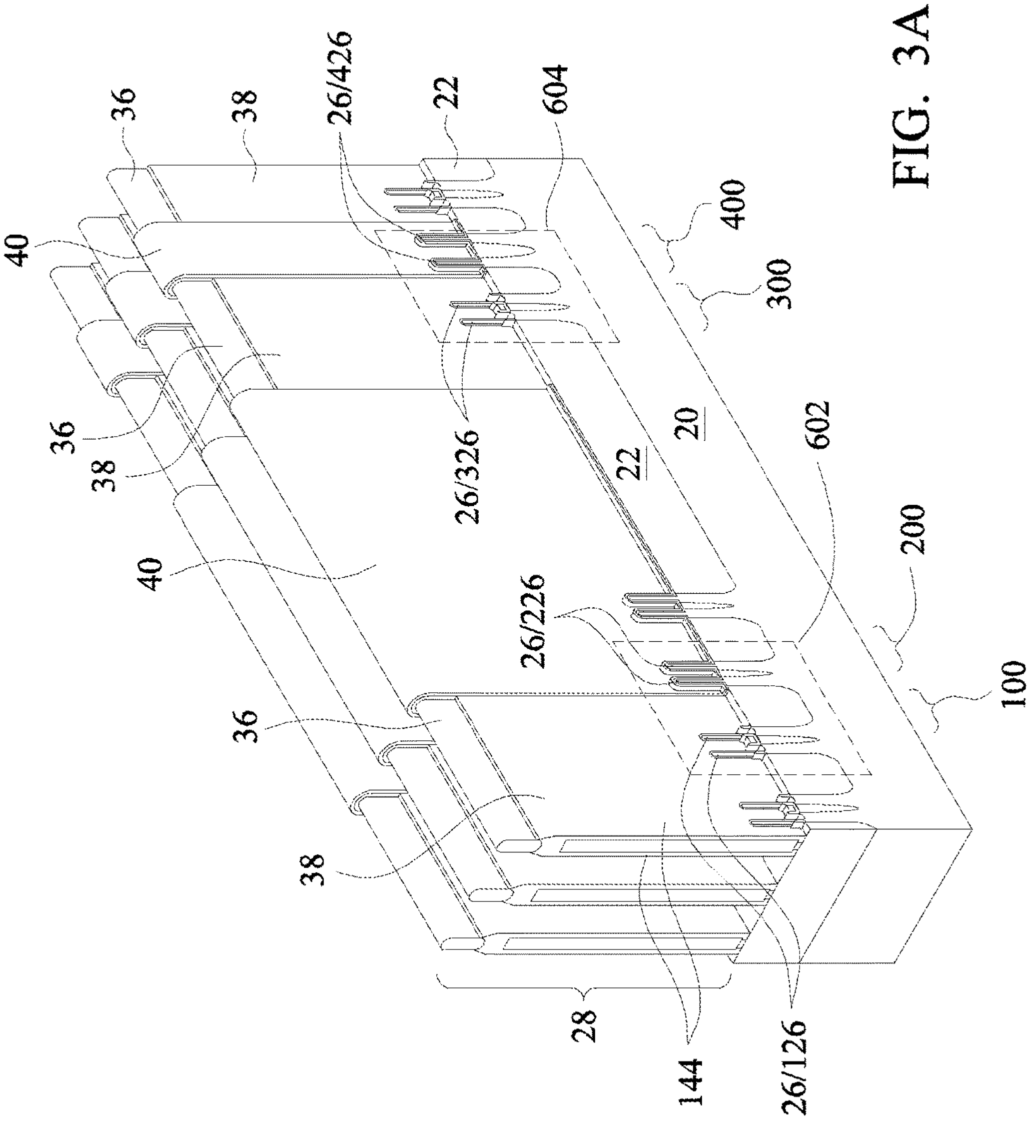
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FIG. 3A

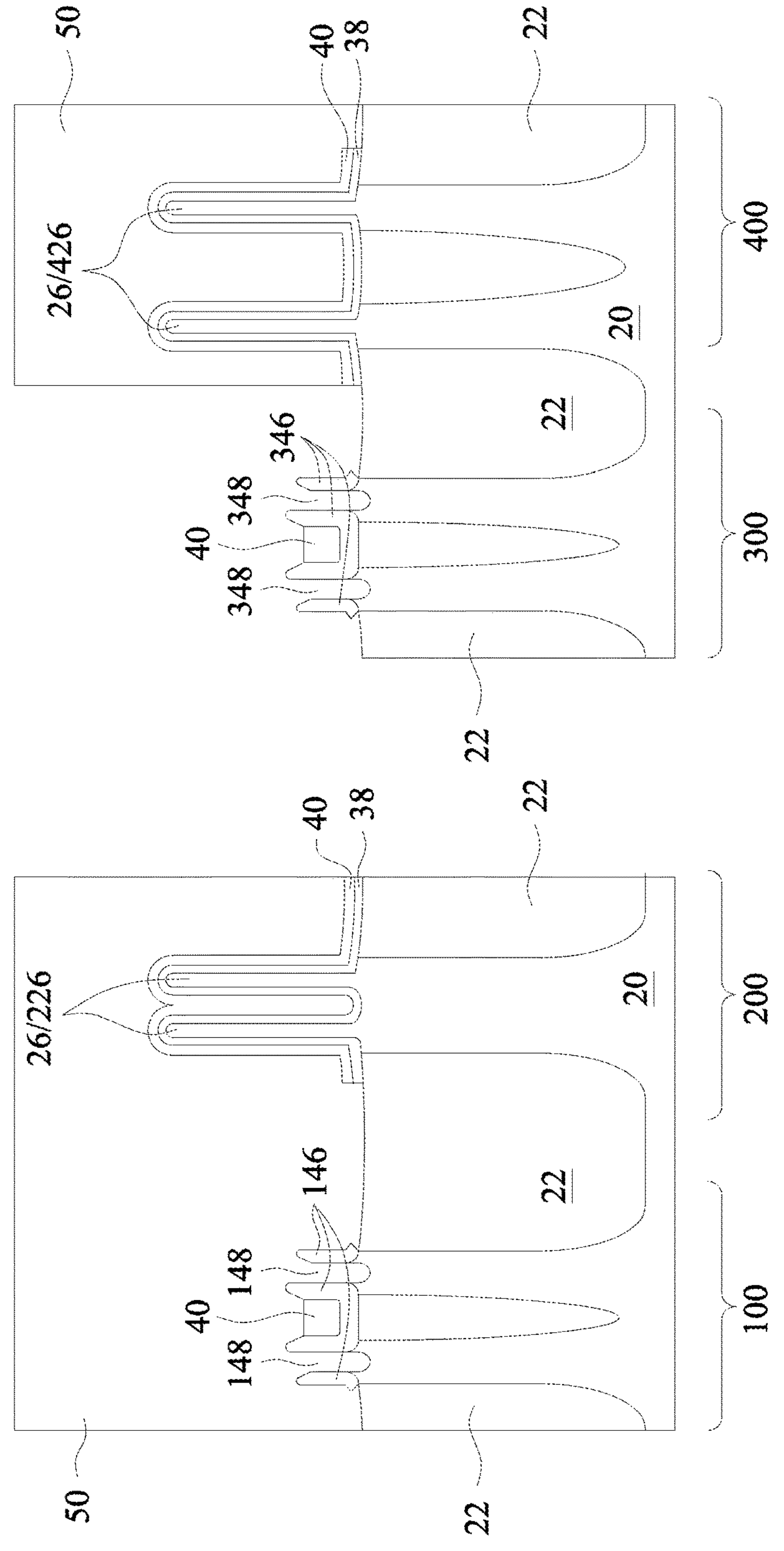
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FIG. 3B

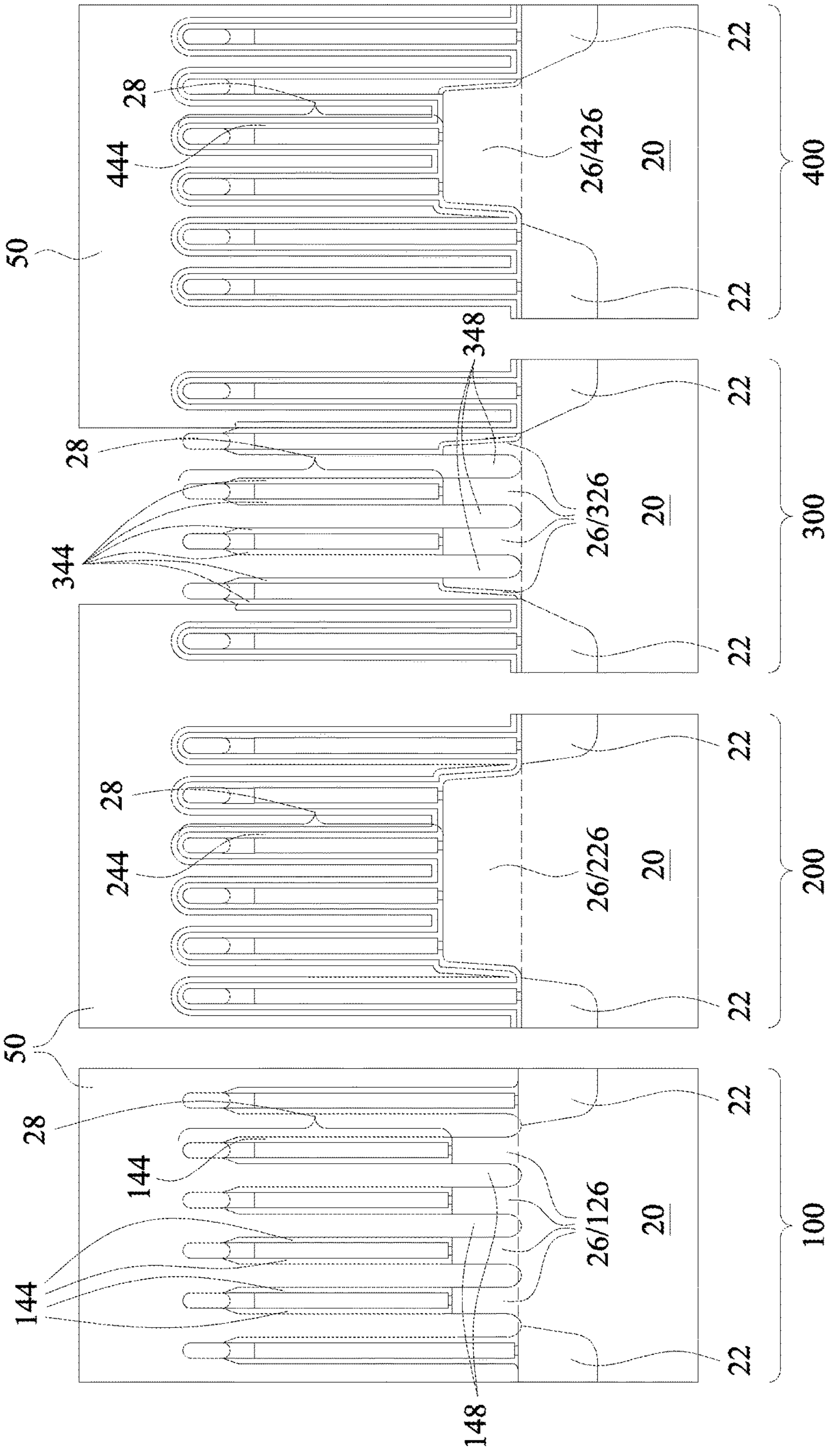
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FIG. 3C

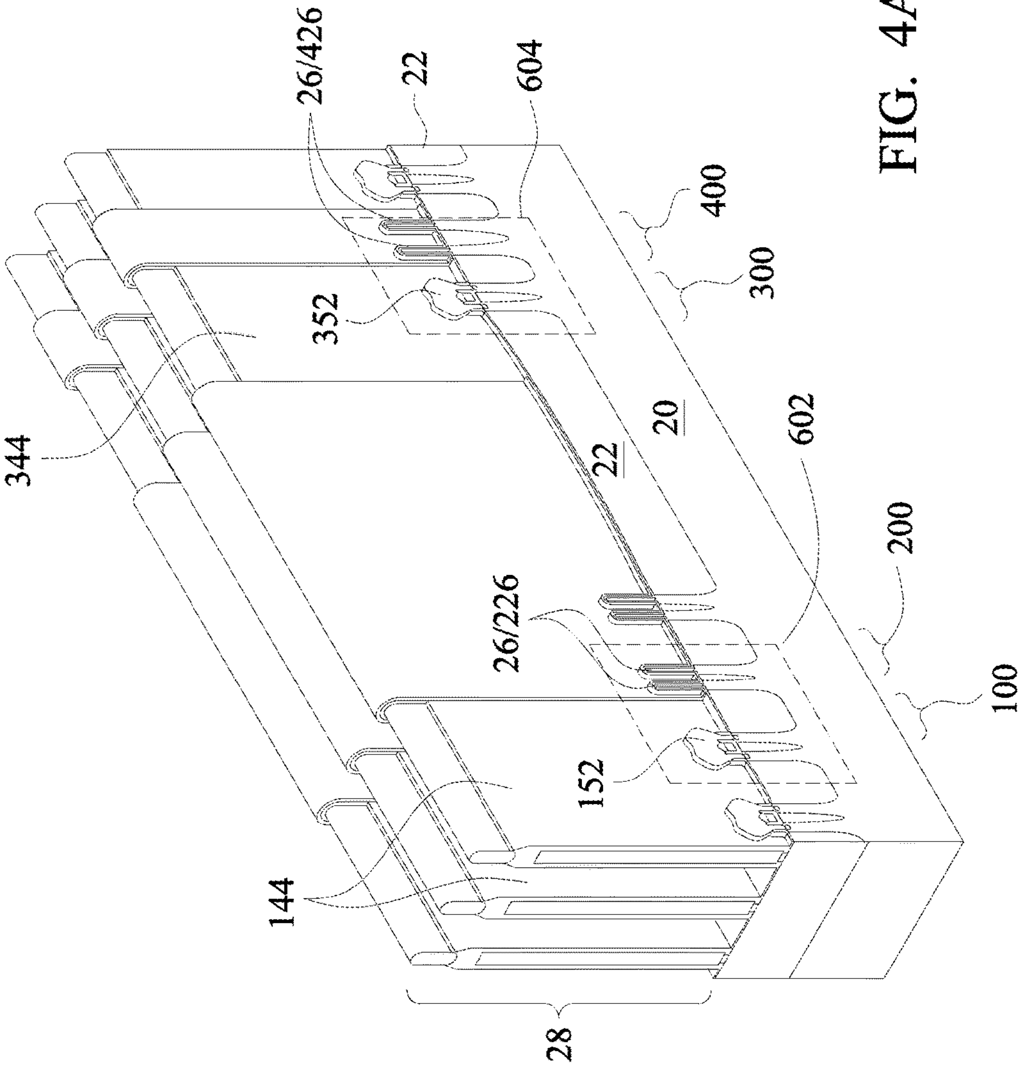

FIG. 4A

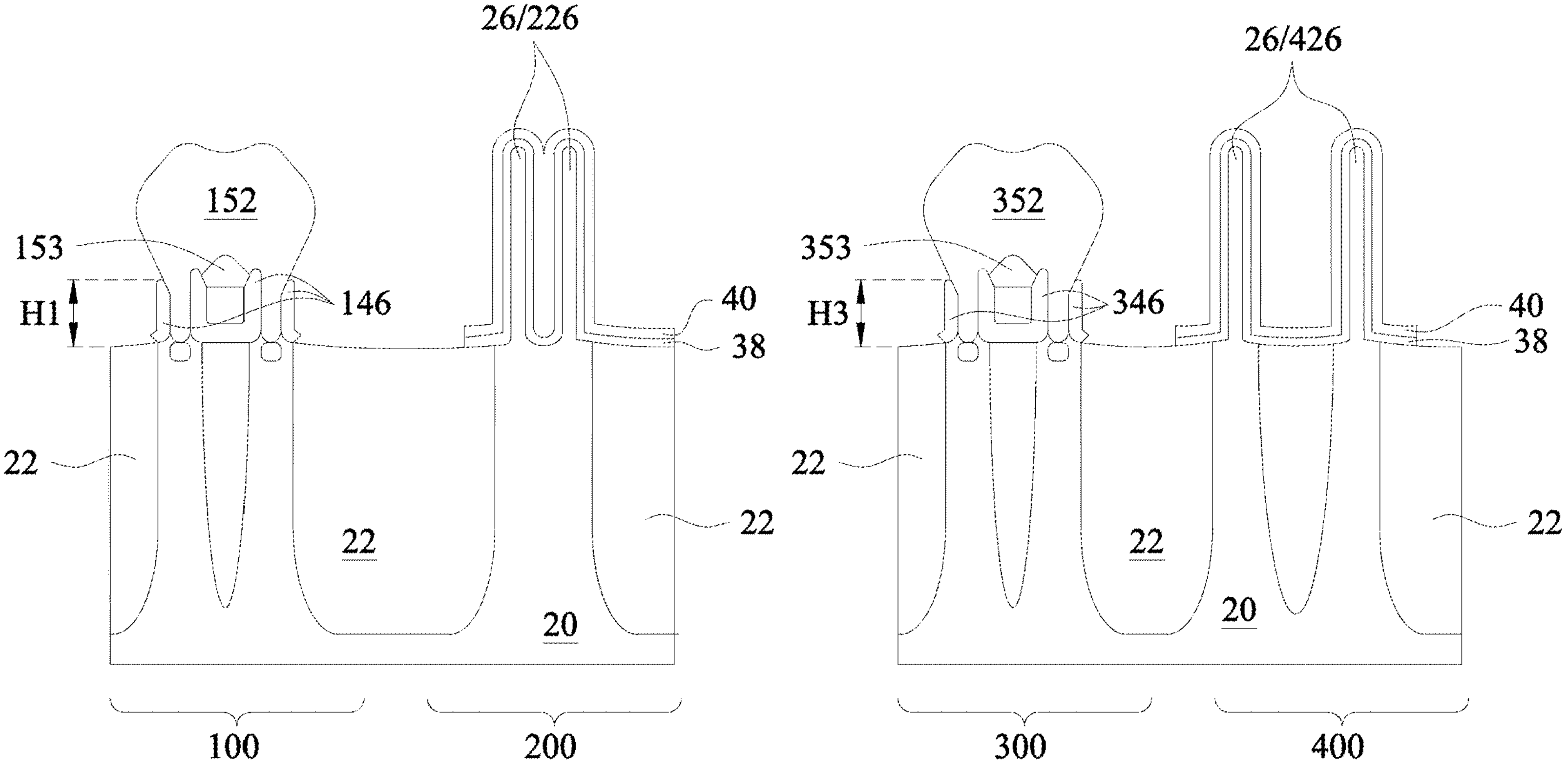
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FIG. 4B

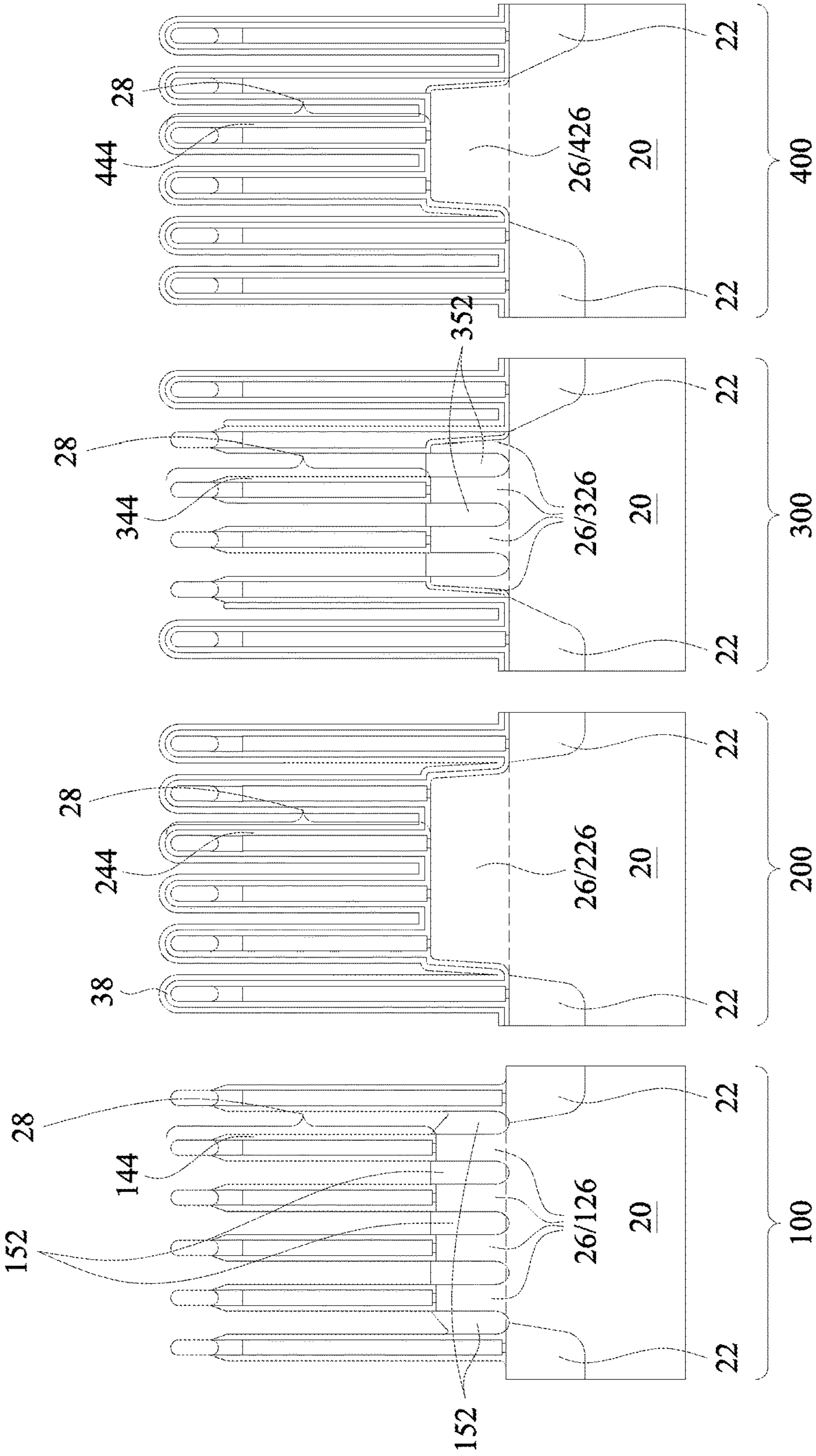
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FIG. 4C

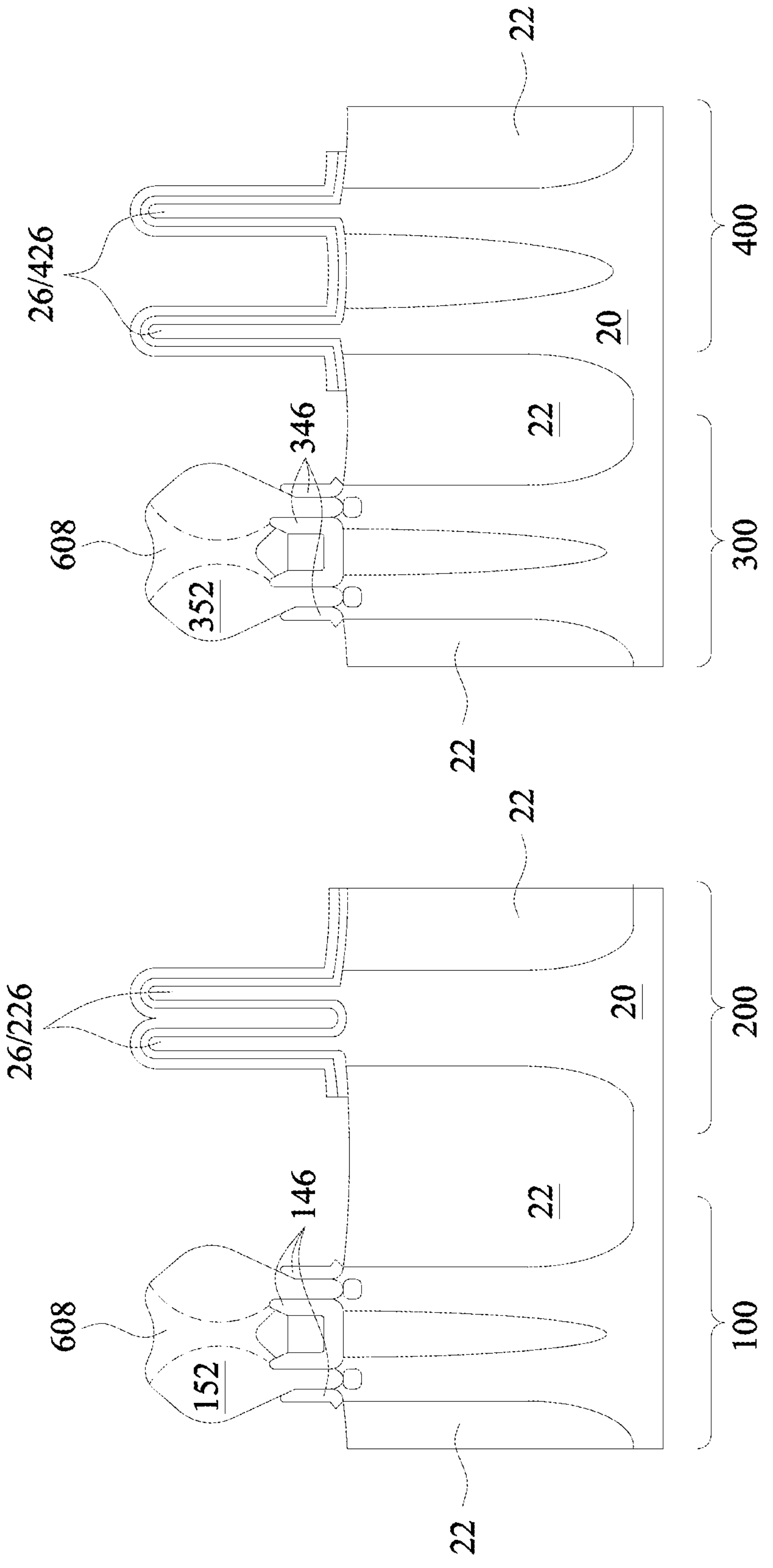
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FIG. 4D

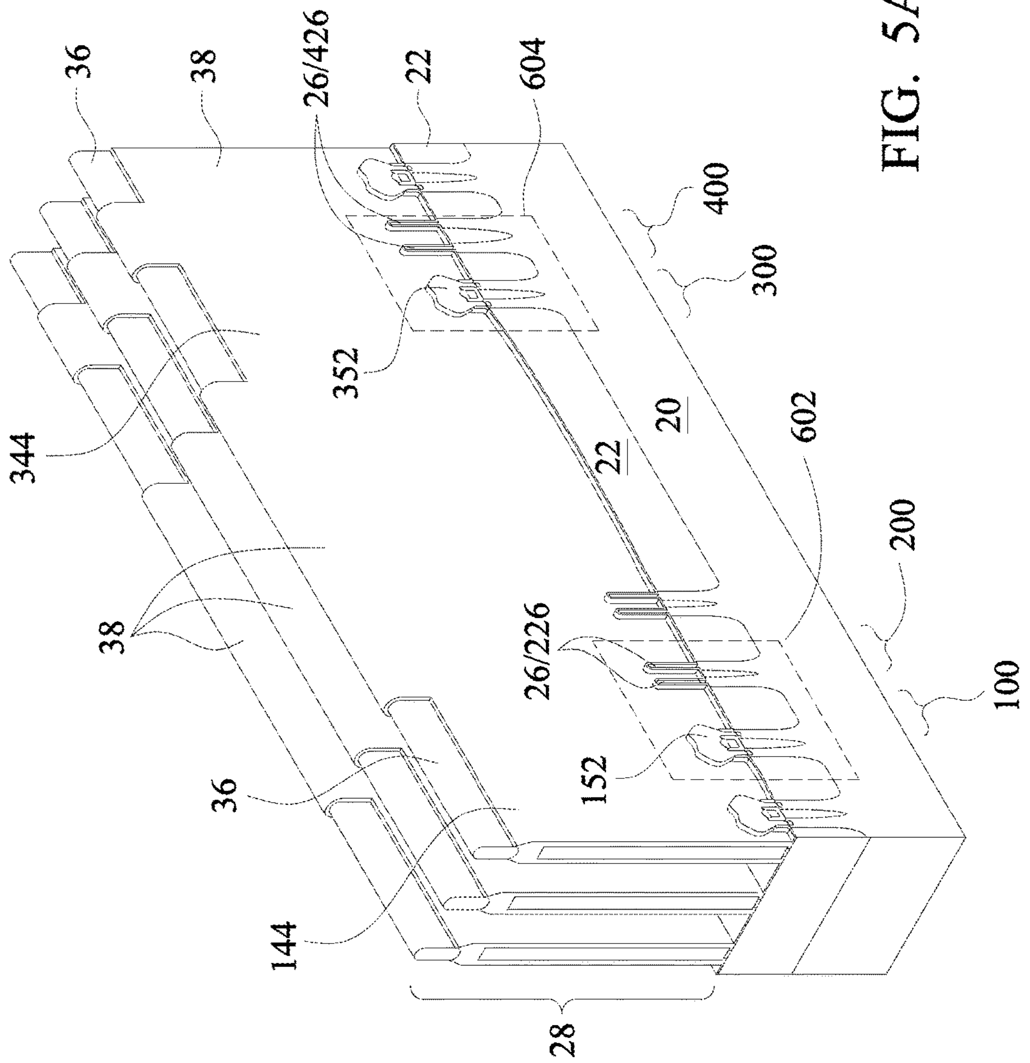
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FIG. 5A

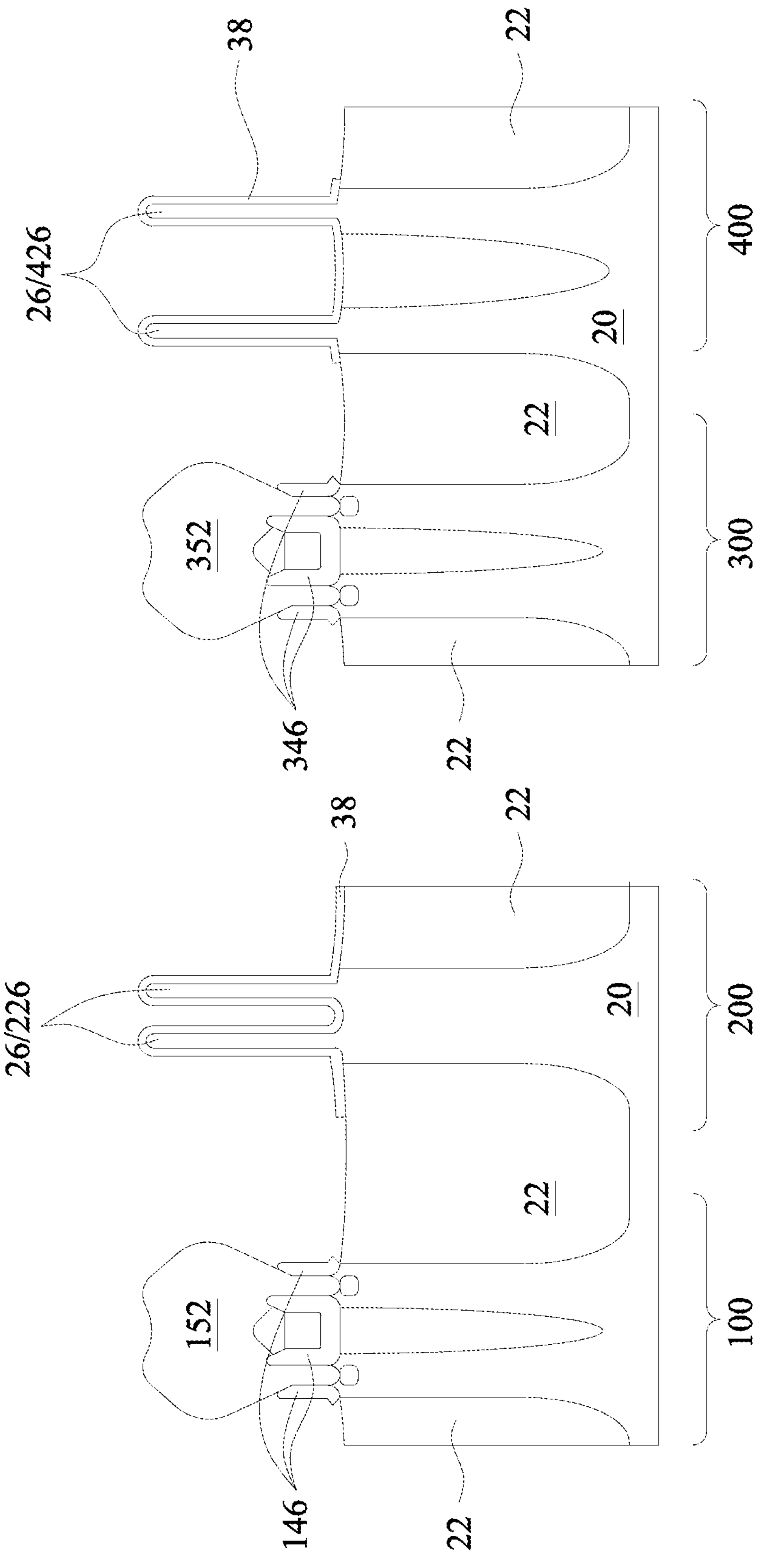
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FIG. 5B

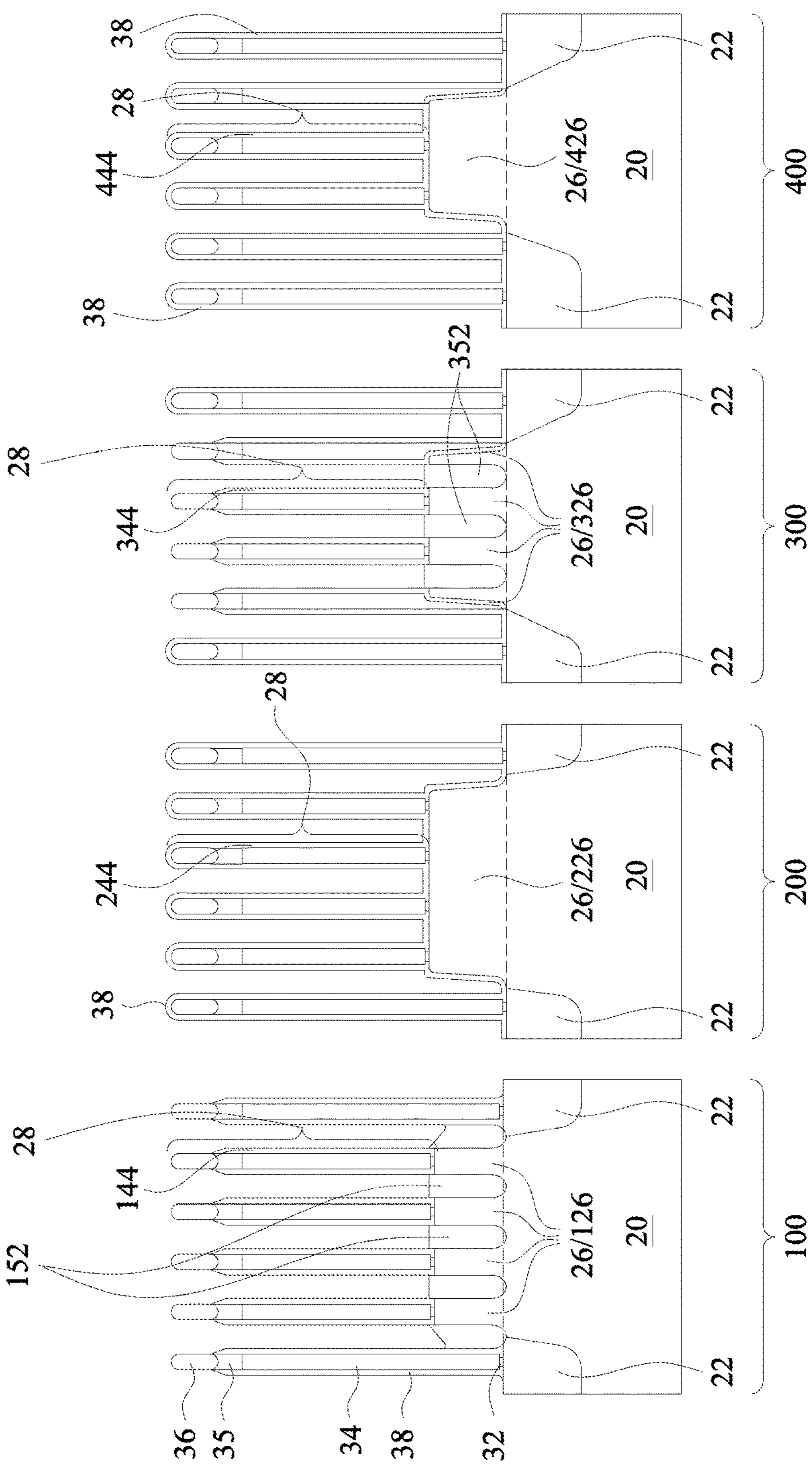
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FIG. 5C

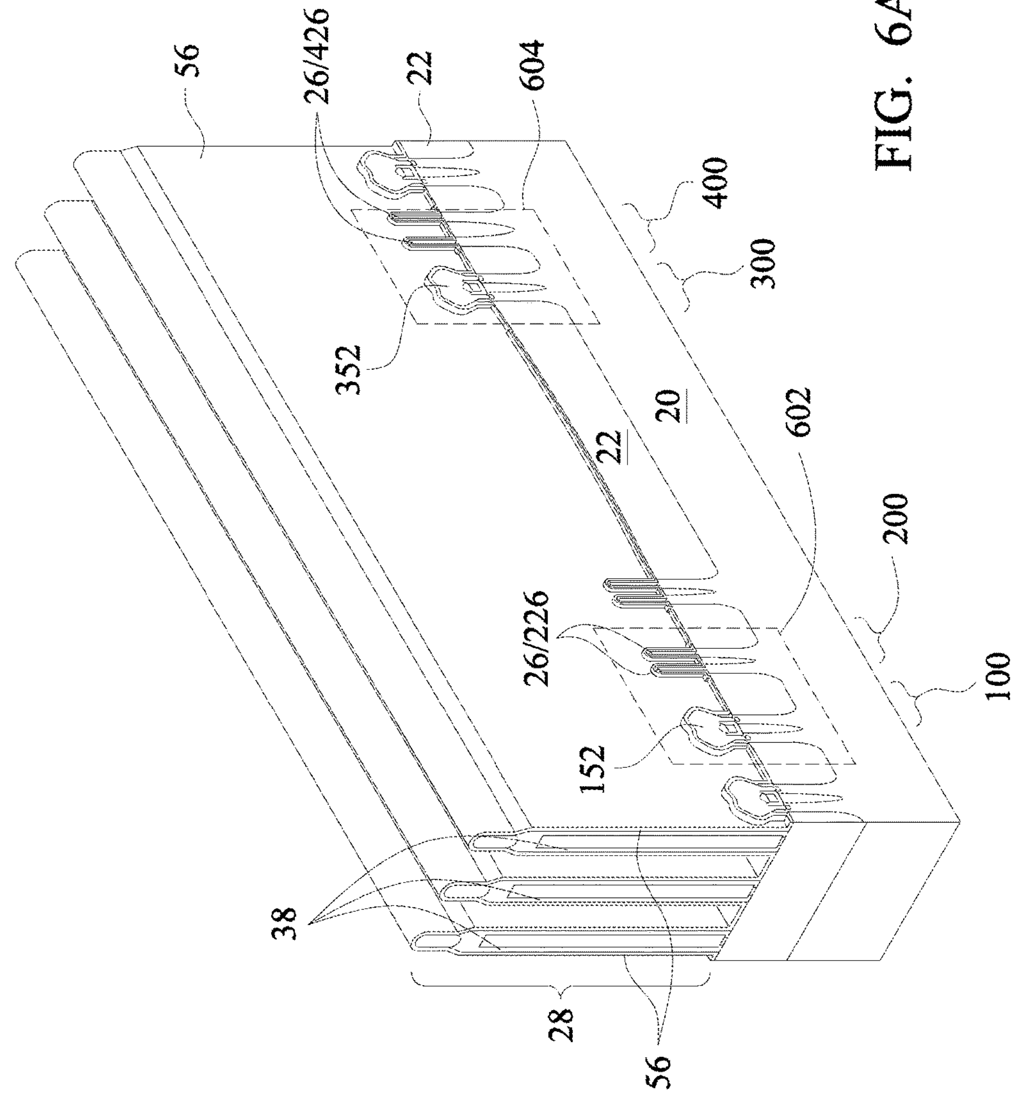

FIG. 6A

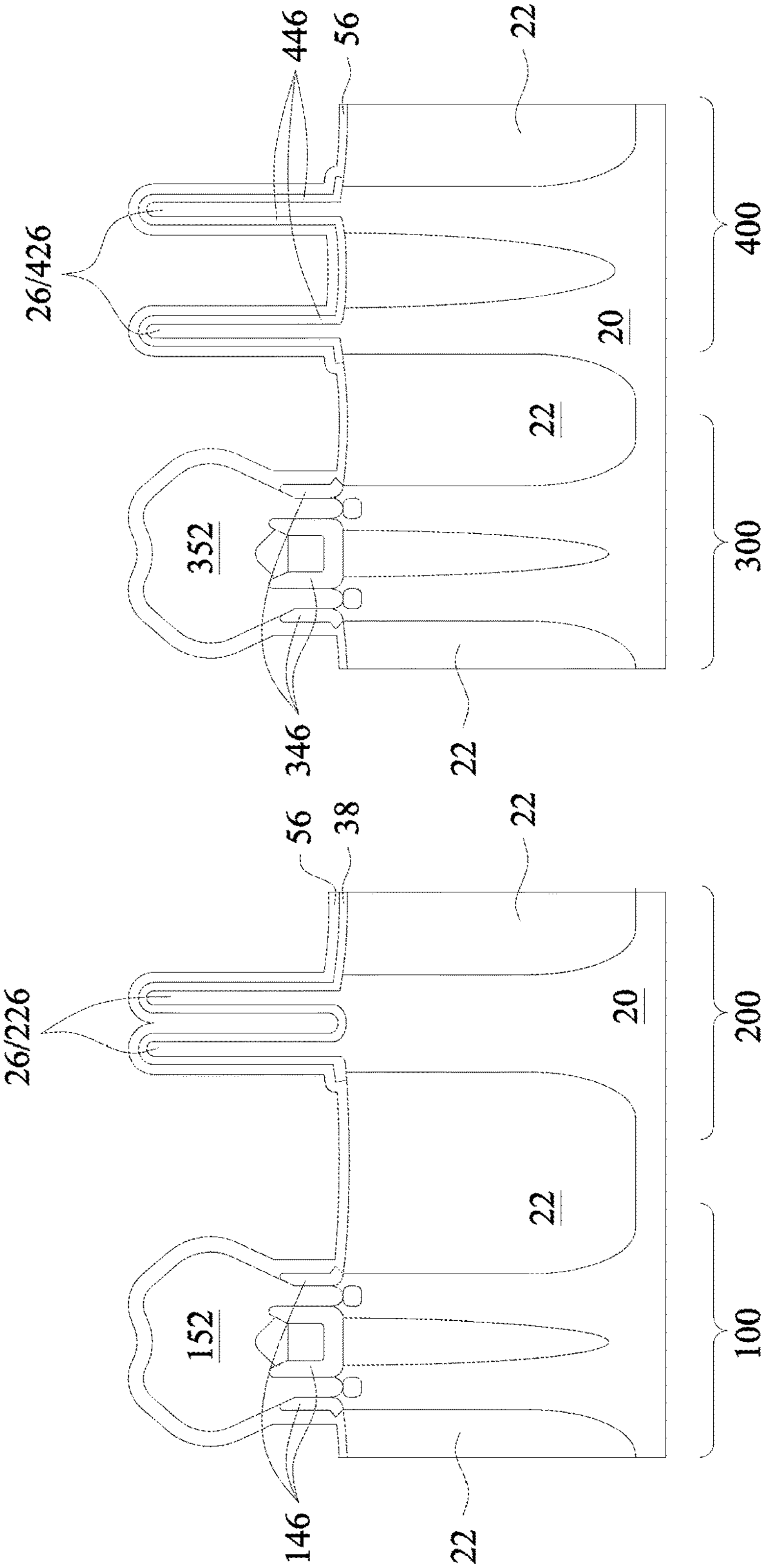
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FIG. 6B

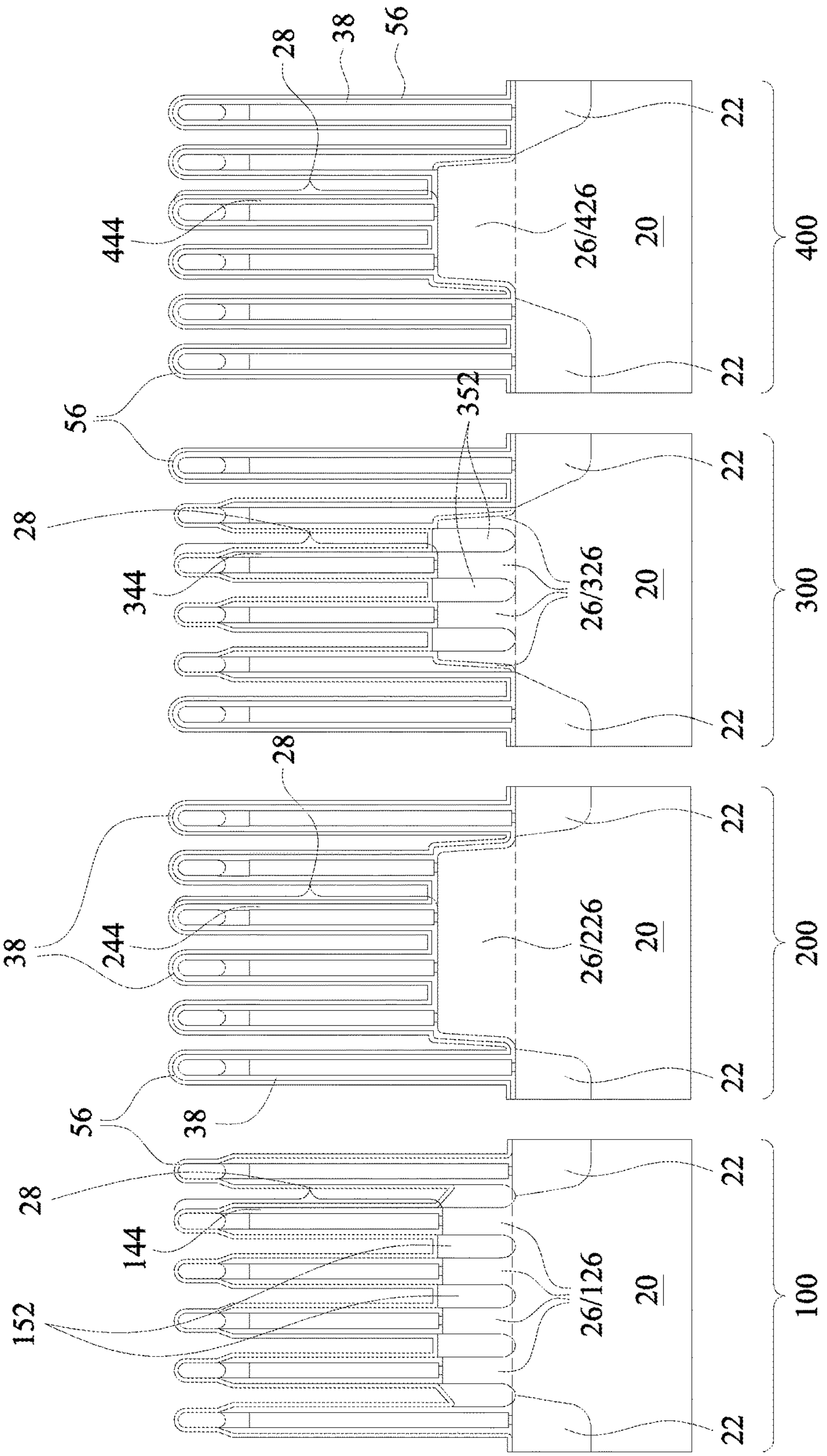
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FIG. 6C

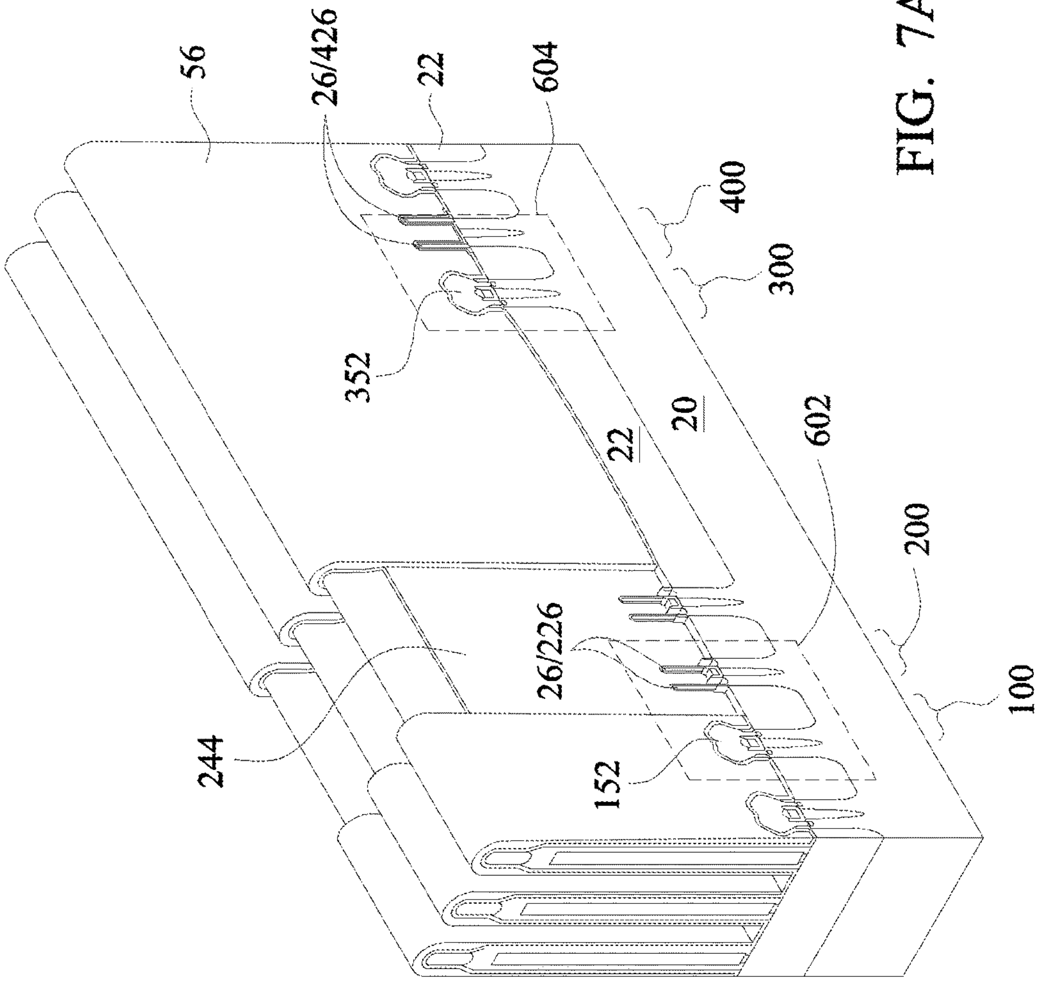

FIG. 7A

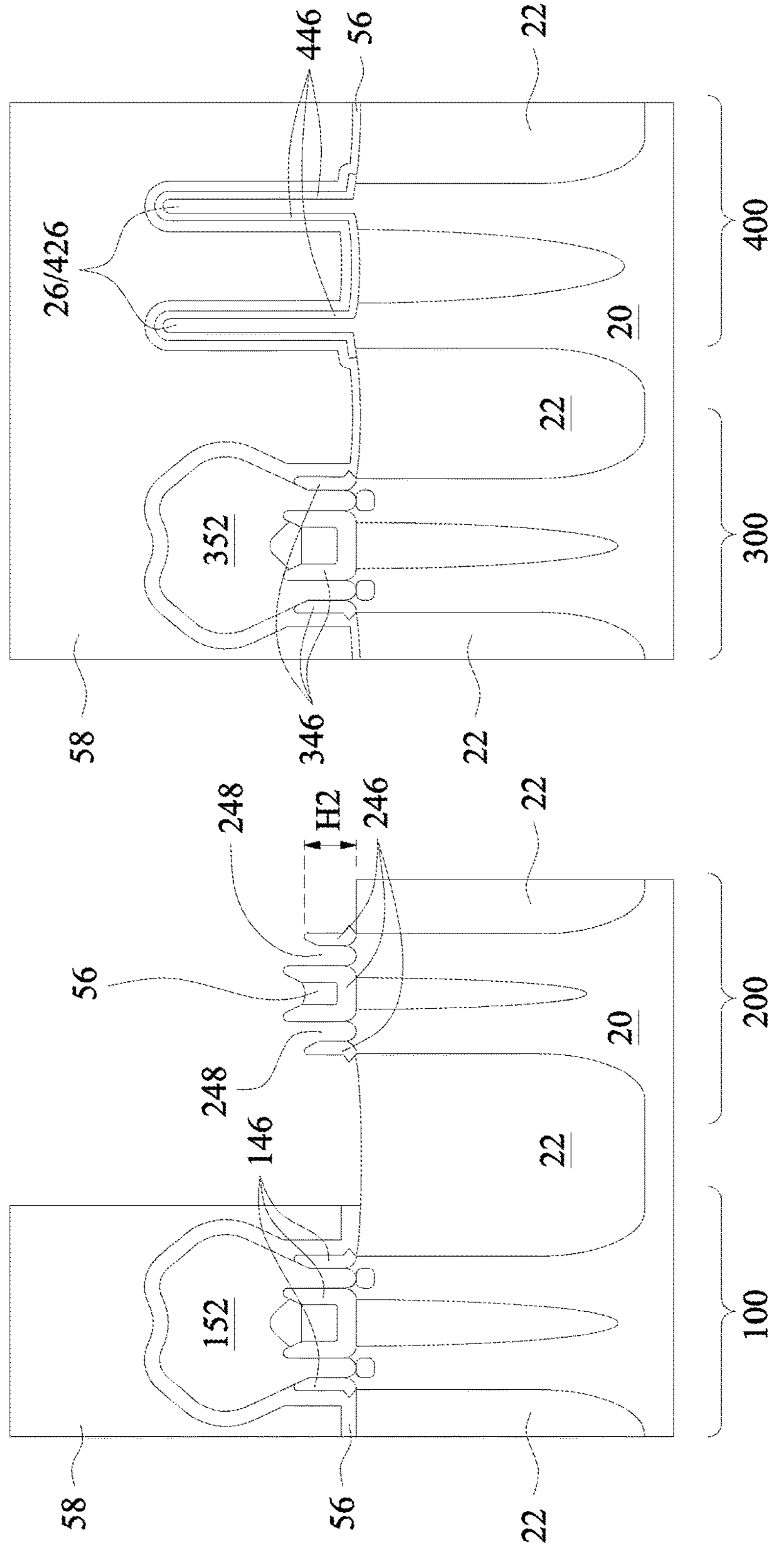
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FIG. 7B

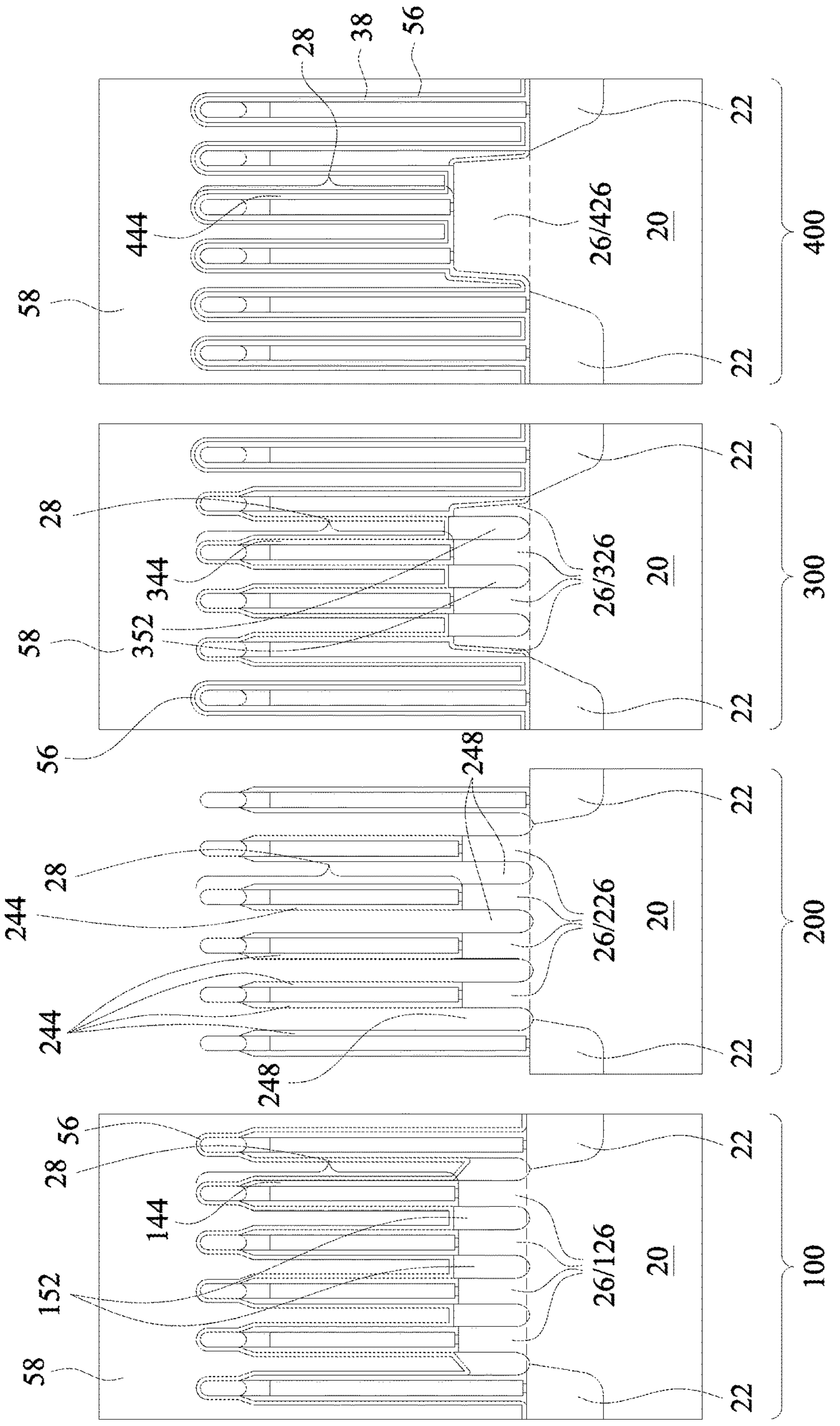
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FIG. 7C

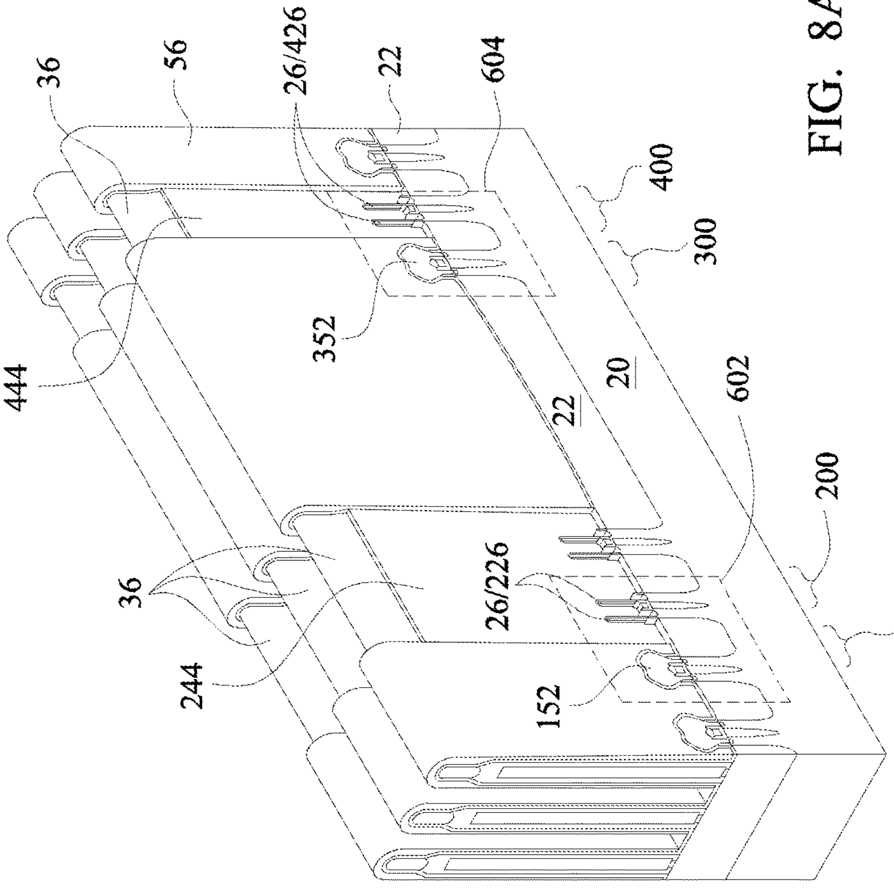
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FIG. 8A

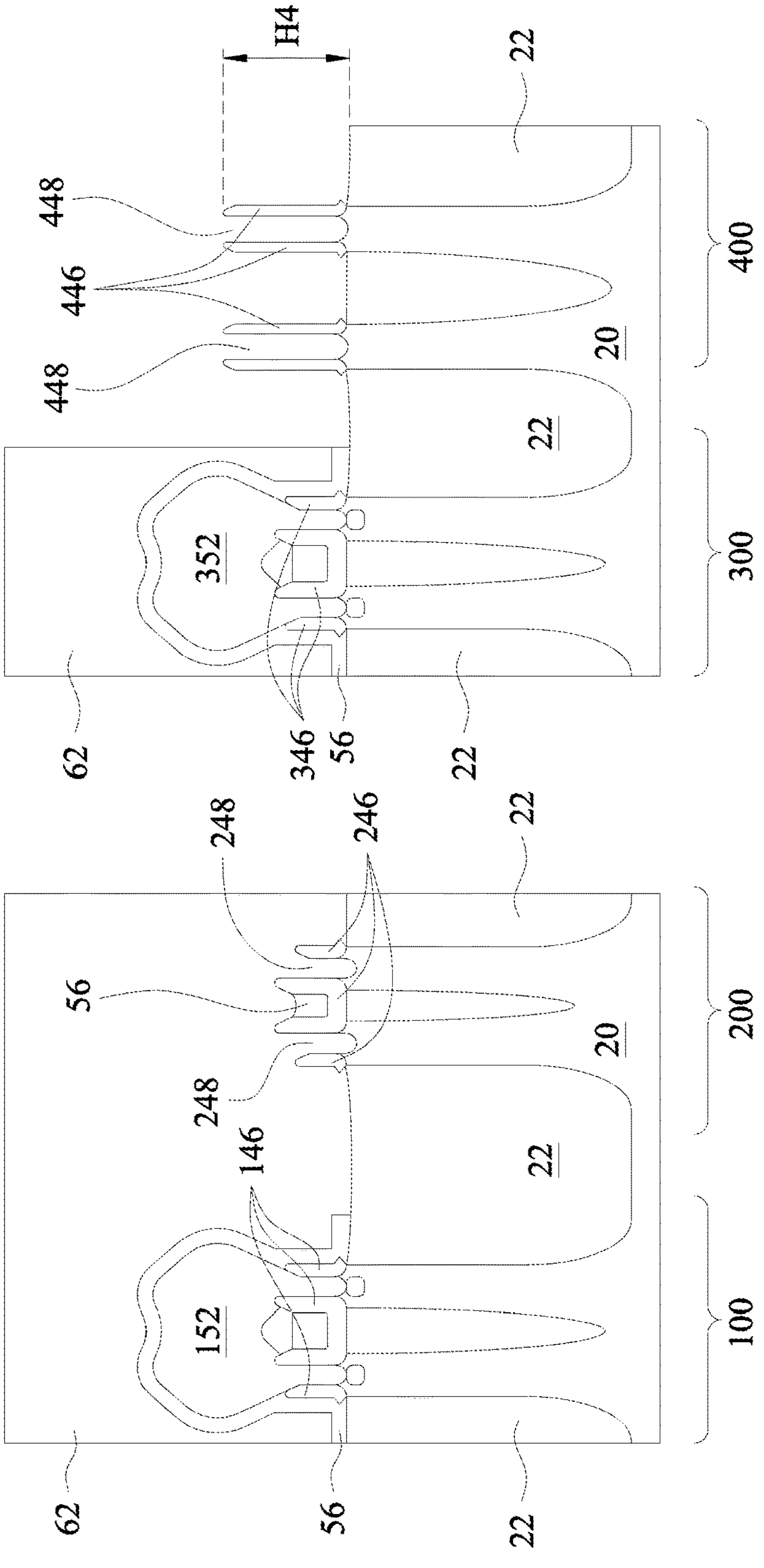
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FIG. 8B

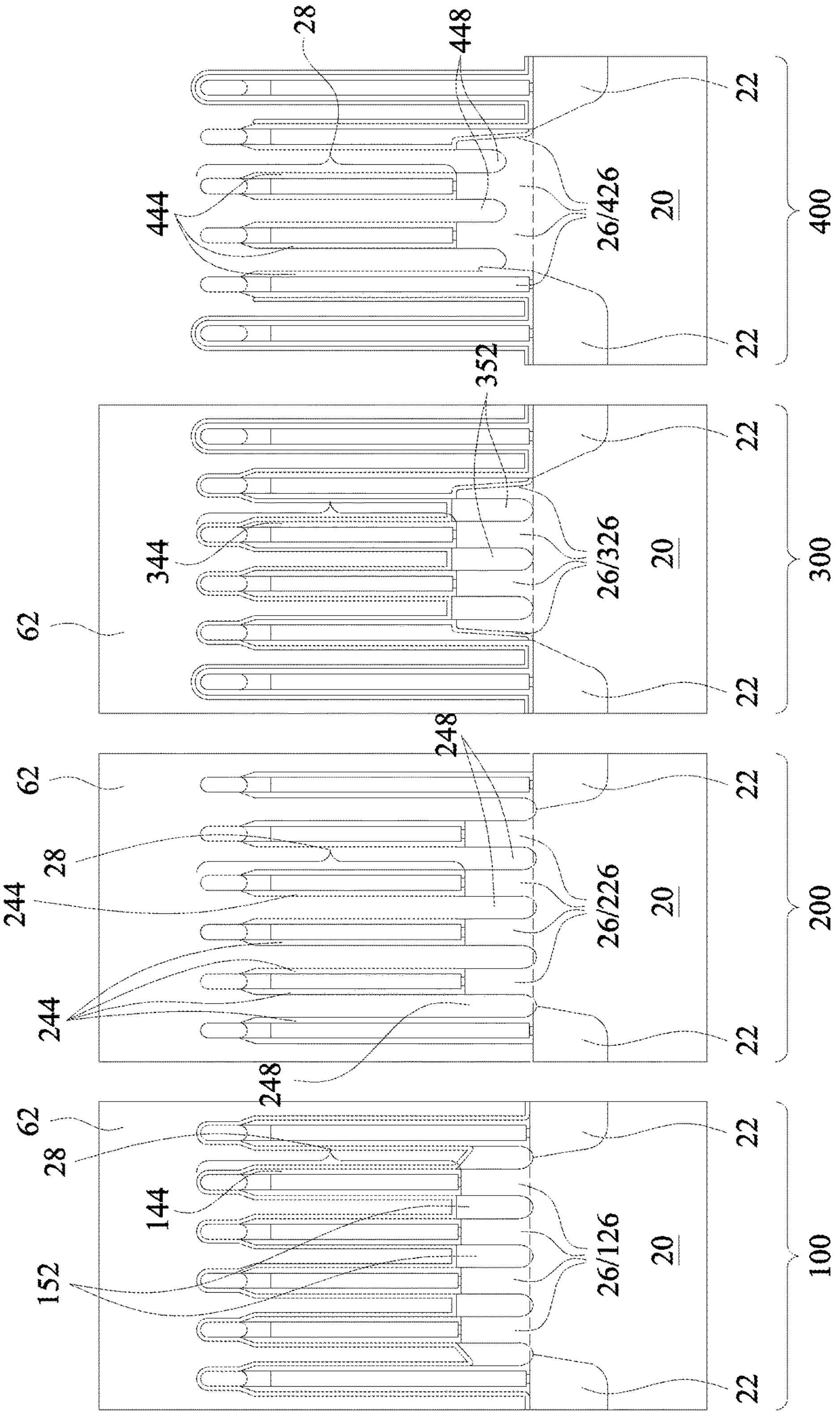
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FIG. 8C

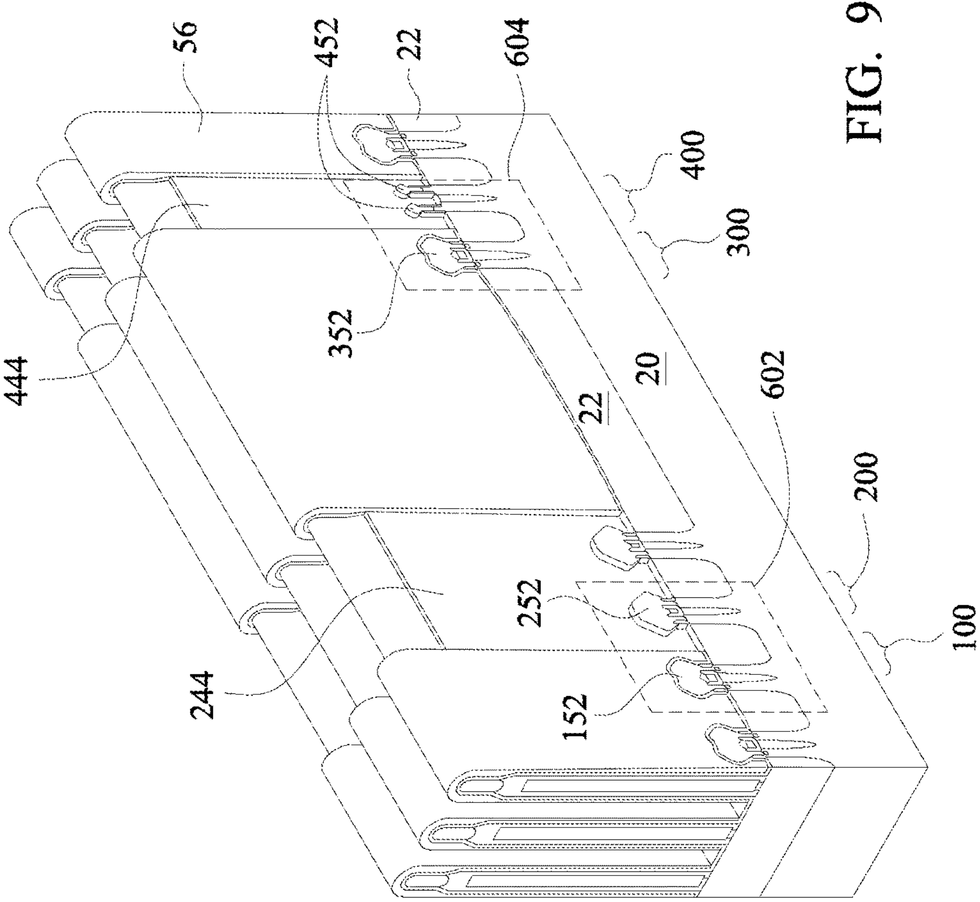

FIG. 9A

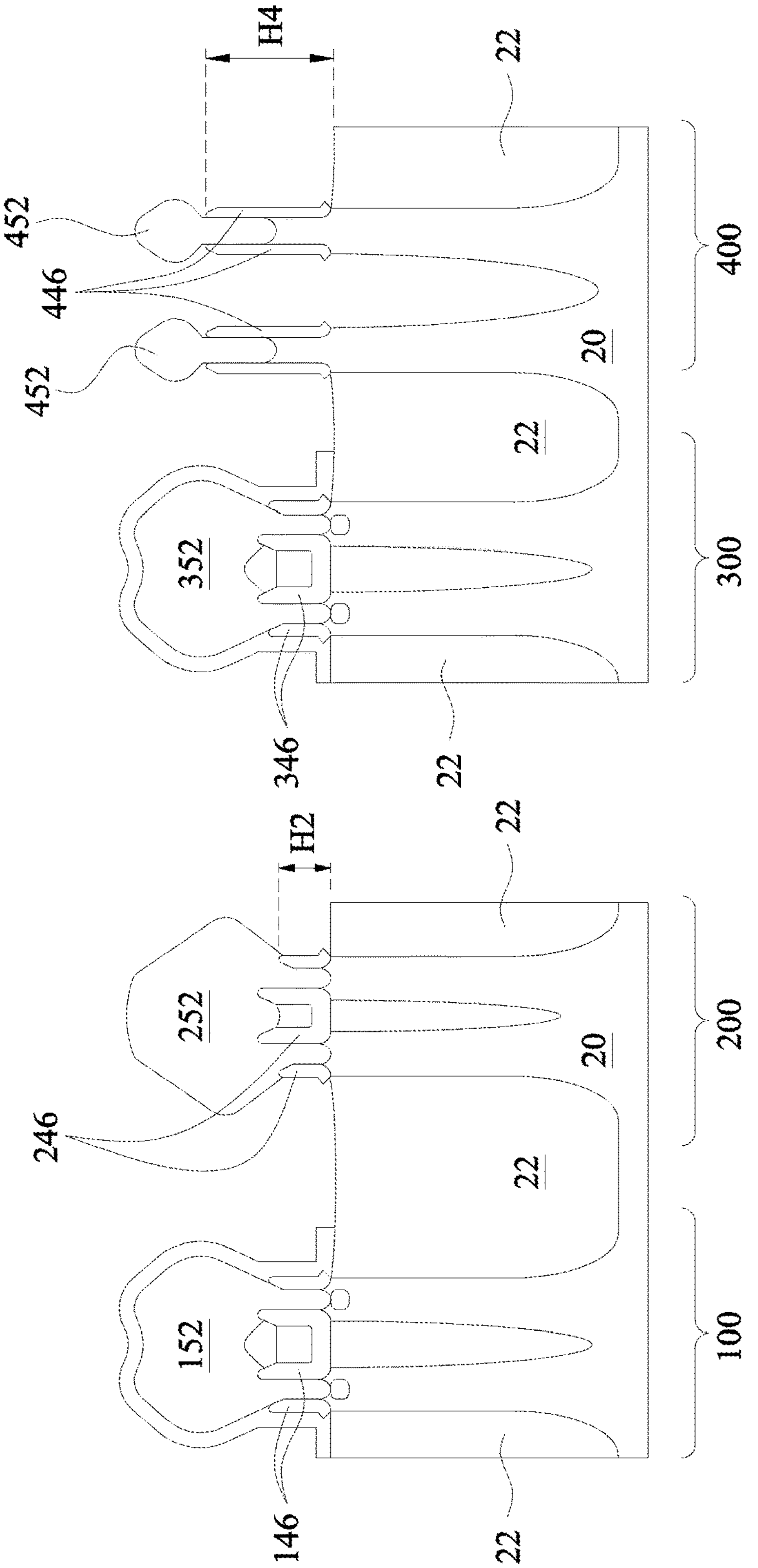
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FIG. 9B

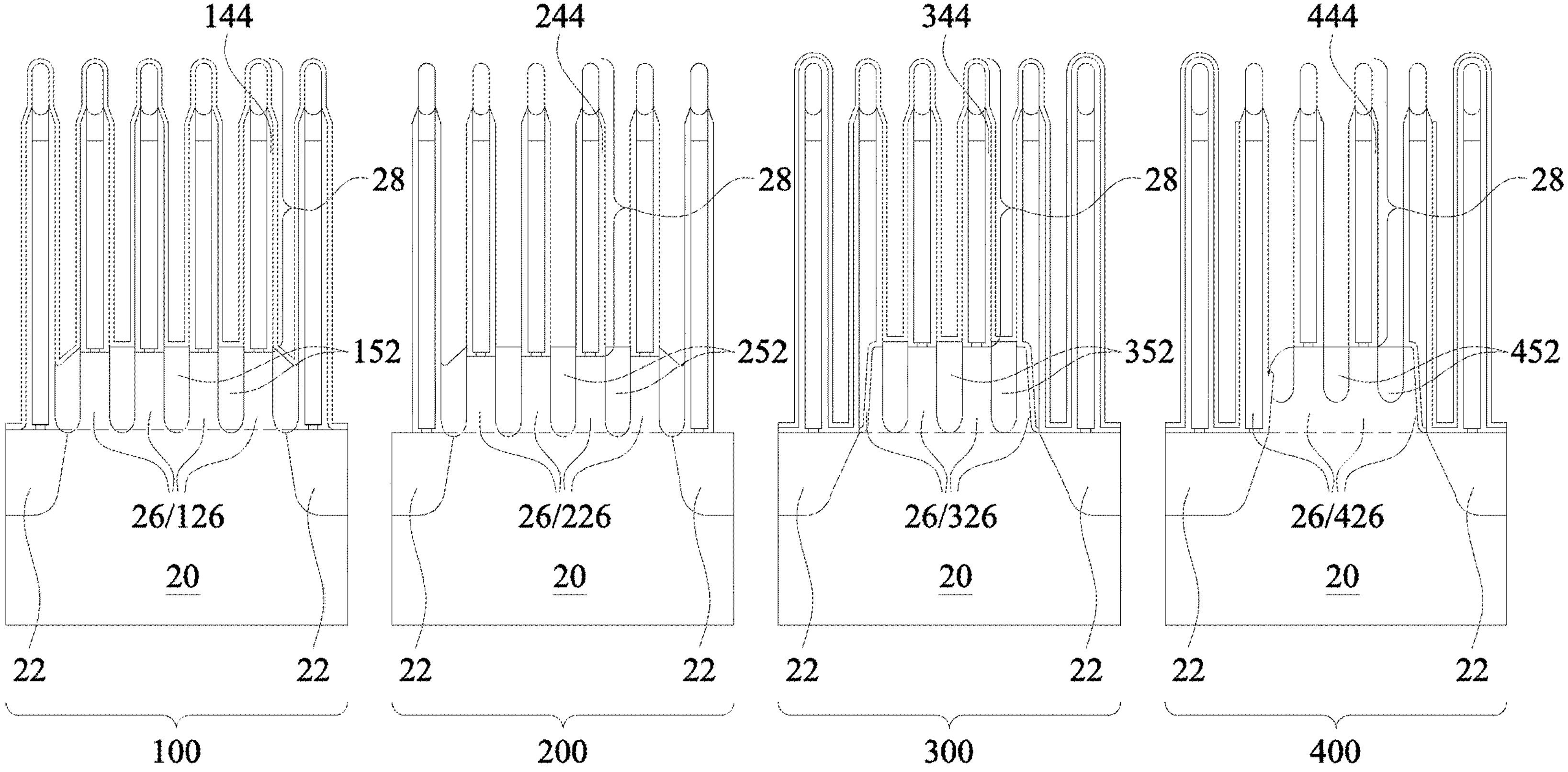
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FIG. 9C

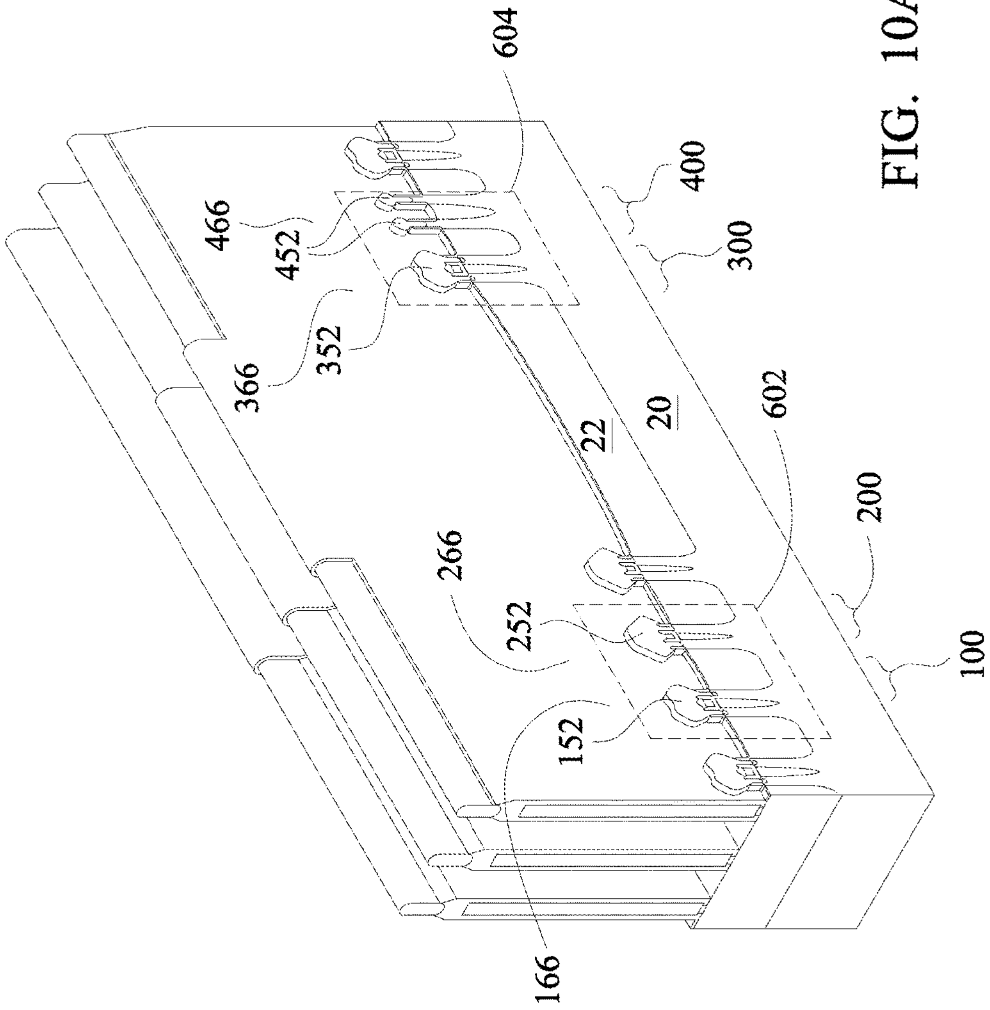

FIG. 10A

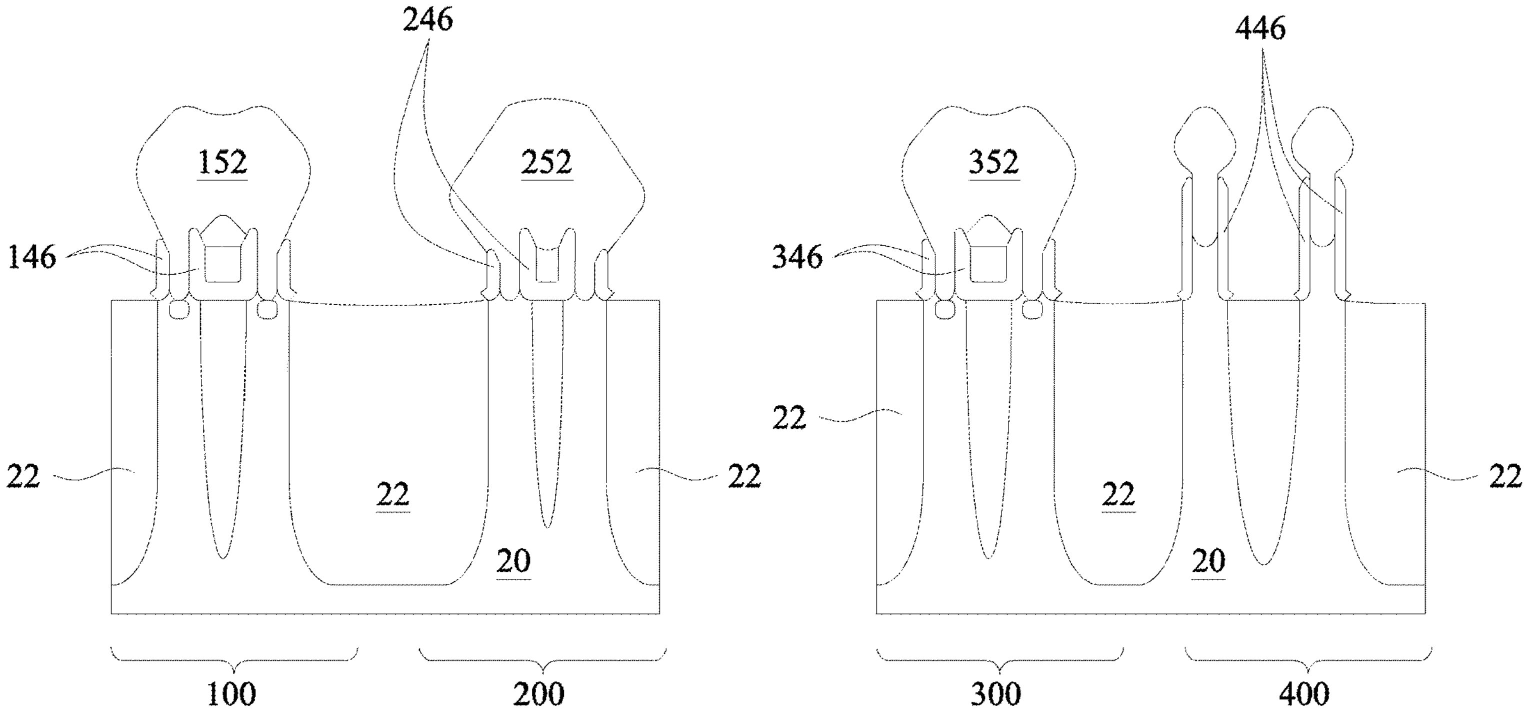
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FIG. 10B

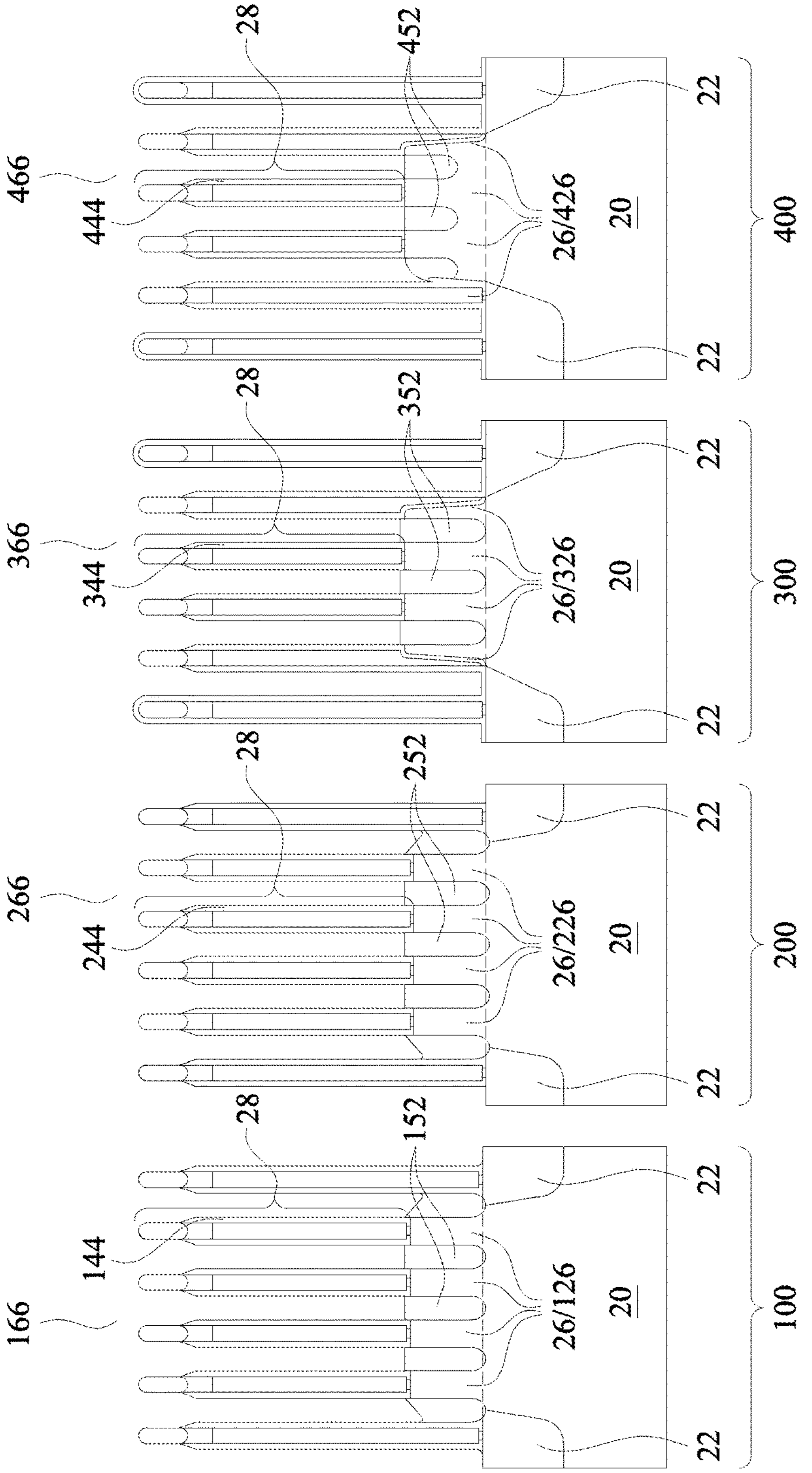
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FIG. 10C

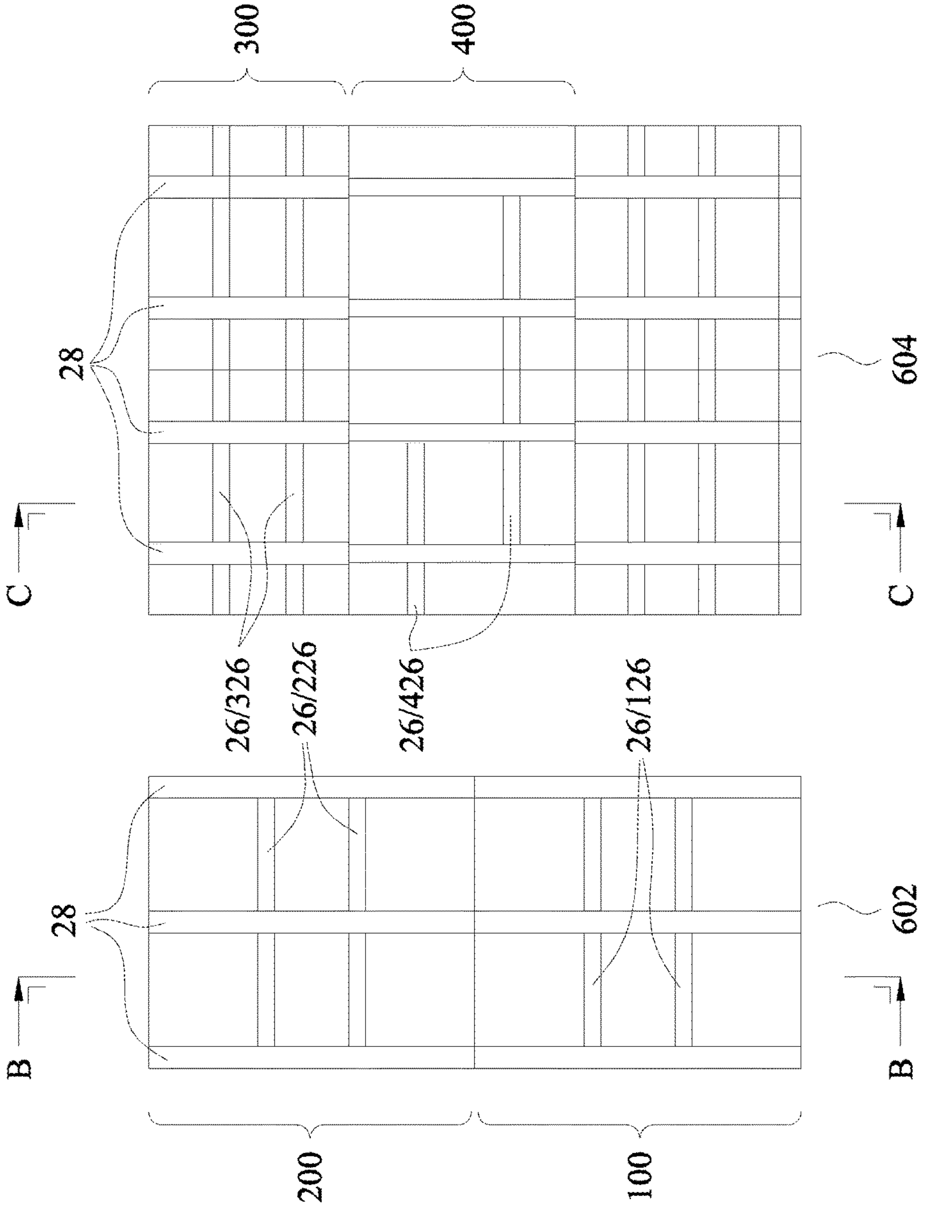

FIG. 11

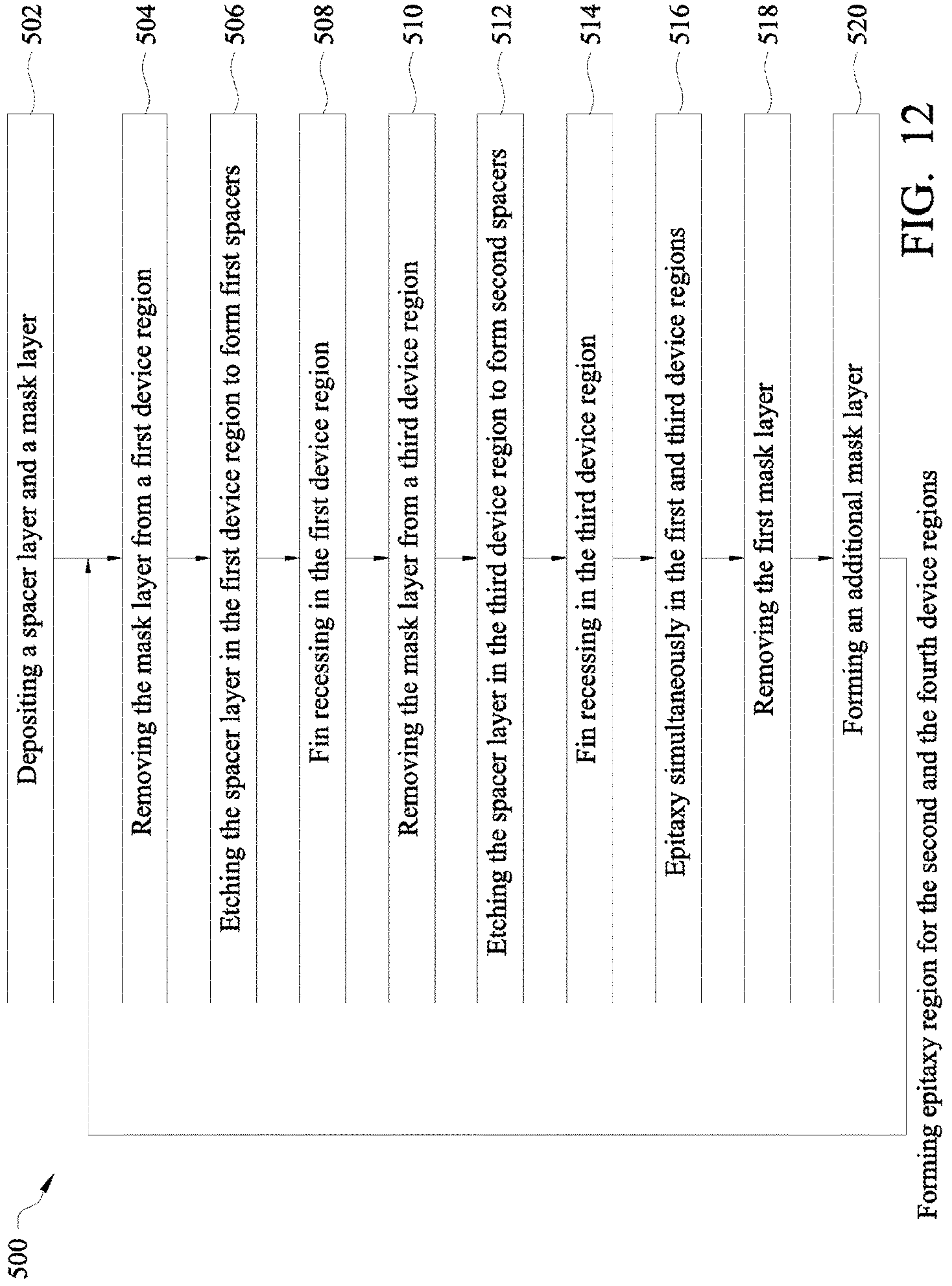
500
502
Depositing a spacer layer and a mask layer
504
Removing the mask layer from a first device region
506
Etching the spacer layer in the first device region to form first spacers
508
Fin recessing in the first device region
510
Removing the mask layer from a third device region
512
Etching the spacer layer in the third device region to form second spacers
514
Fin recessing in the third device region
516
Epitaxy simultaneously in the first and third device regions
518
Removing the first mask layer
520
Forming an additional mask layer
Forming epitaxy region for the second and the fourth device regions

FIG. 12

FLEXIBLE MERGE SCHEME FOR SOURCE/DRAIN EPITAXY REGIONS

PRIORITY CLAIM AND CROSS-REFERENCE

[0001] This application is a divisional of U.S. patent application Ser. No. 15/492,142, entitled "Flexible Merge Scheme for Source/Drain Epitaxy Regions," filed on Apr. 20, 2017, which application is incorporated herein by reference

BACKGROUND

[0002] Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs.

[0003] Such scaling down has also increased the complexity of processing and manufacturing ICs and, for these advances to be realized, similar developments in IC processing and manufacturing are needed. For example, three-dimensional transistors such as a Fin Field-Effect Transistors (FinFETs) have been introduced to replace planar transistors. Although existing FinFET devices and methods of fabricating FinFET devices have been generally adequate for their intended purposes, they have not been entirely satisfactory in all respects. For example, the FinFETs for different circuits such as core (logic) circuits and Static Random Access Memory (SRAM) circuits may have different designs, and the source/drain epitaxy regions grown from neighboring fins may need to be merged for some circuits (such as logic circuits), and need to be separated from each other for other circuits (such as SRAM circuits). However, to save manufacturing cost, the epitaxy for different regions is performed simultaneously. This causes difficulty for selectively making epitaxy regions merged for some circuits, and not merged for other circuits. Accordingly, the merged epitaxy regions need to be trimmed to separate the merged epitaxy regions from each other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIGS. **1**A through **10**C are cross-sectional views and perspective views of intermediate stages in the formation of Fin Field-Effect Transistors (FinFETs) in accordance with some embodiments.

[0006] FIG. **11** illustrates the exemplary layouts of a logic circuit and a Static Random Access Memory (SRAM) circuit in accordance with some embodiments.

[0007] FIG. **12** illustrates a process flow for forming FinFETs in accordance with some embodiments.

DETAILED DESCRIPTION

[0008] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0009] Further, spatially relative terms, such as "underlying," "below," "lower," "overlying," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0010] Fin Field-Effect Transistor (FinFETs) and the method of forming the same are provided in accordance with various exemplary embodiments. The intermediate stages in the formation of the FinFETs are illustrated. The variations of some embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0011] FIGS. **1**A through **10**C illustrate the intermediate stages in the formation of FinFETs. The steps shown in FIG. **1**A through **10**C are also illustrated schematically in the process flow **500** shown in FIG. **12**. Each of the figure numbers in FIGS. **1**A through **10**C may include letter "A," "B," or "C," wherein letter "A" indicates that the respective figure illustrates a perspective view, and letter "B" indicates that the respective figure is obtained from the plane same as the vertical plane containing line B-B in FIG. **1**A, and letter "C" indicates that the respective figure is obtained from (and combined) the planes same as the vertical planes containing lines C-C in FIG. **1**A. Accordingly, the figures whose numbers include letter "B" show the cross-sectional views obtained from the vertical planes parallel to the lengthwise directions of gate stacks, and the figures whose numbers include letter "C" show the cross-sectional views obtained from the vertical planes parallel to the lengthwise directions of semiconductor fins, which will be discussed in detail in subsequent paragraphs.

[0012] FIG. **1**A illustrates a perspective view in the formation of a structure including substrate **20**, isolation regions **22**, semiconductor strips **24** between isolation regions **22**, and semiconductor fins **26** over the top surfaces of isolation regions **22**. Substrate **20** is a semiconductor substrate, which may be a silicon substrate, a silicon carbon substrate, or a substrate formed of other semiconductor materials such as III-V compound semiconductor materials. Substrate **20** may be lightly doped with a p-type or an n-type impurity.

[0013] Isolation regions **22** may be, for example, Shallow Trench Isolation (STI) regions. The formation of STI regions **22** may include etching semiconductor substrate **20** to form trenches, and filling the trenches with a dielectric material(s) to form STI regions **22**. STI regions **22** may include silicon oxide, and other dielectric materials such as nitrides may also be used. Semiconductor fins **26** overlap the underlying semiconductor strips **24**. The formation of semiconductor fins **26** may include recessing STI regions **22**, so that the portions of semiconductor material between the removed portions of STI regions **22** become semiconductor fins **26**. Semiconductor fins **26** and some or substantially entireties of semiconductor strips **24** may be formed of silicon (with no germanium therein) or other silicon-containing compound including, and not limited to, silicon carbon, silicon germanium, or the like.

[0014] A plurality of parallel gate stacks **28** is formed on semiconductor fins **26**. Gate stacks **28** are parallel to each other, and cover portions of semiconductor fins **26**, while leaving some other portions of semiconductor fins **26** uncovered. Gate stacks **28** include gate dielectrics **32** on the sidewalls and the top surfaces of semiconductor fins **26**, and gate electrodes **34** over gate dielectrics **32**. Gate dielectrics **32** may be selected from silicon oxide, silicon nitride, gallium oxide, aluminum oxide, scandium oxide, zirconium oxide, lanthanum oxide, hafnium oxide, combinations thereof, and multi-layers thereof. Gate electrodes **34** may be formed of a conductive material that includes polysilicon, a refractory metal, or the respective compound including, e.g., polysilicon, Ti, W, TiAl, TaC, TaCN, TaAlC, TaAlCN, TiN, and TiW. In other examples, gate electrodes **34** include nickel (Ni), gold (Au), copper (Cu), or the alloys thereof.

[0015] In accordance with some embodiments of the present disclosure, gate stacks **28** remain in the final FinFETs, and form the gate stacks of the final FinFETs. In accordance with alternative embodiments of the present disclosure, gate stacks **28** are dummy gate stacks that will be replaced by replacement gates in subsequent steps. Accordingly, gate stacks **28** may include dummy gate electrodes (which is also denoted as **34**), which may comprise polysilicon, for example. Dummy gate dielectrics **32** may, or may not, be formed between dummy gate electrodes **34** and semiconductor fins **26**.

[0016] Gate stacks **28** may also include hard masks **35** and **36** formed over gate electrodes **34**. In accordance with some embodiments, hard masks **35** are formed of silicon oxide, silicon oxycarbo-nitride (SiOCN), or the like. Hard masks **36** may be formed of silicon nitride (SiN), SiOCN, SiOC, or other dielectric materials in accordance with some embodiments.

[0017] The perspective view show in FIG. **1**A illustrates the exemplary layouts of circuits **602** and **604** as schematically represented by dashed boxes. In accordance with some embodiments, each of circuits **602** and **604** is selected from logic circuits or SRAM circuits, and circuits **602** and **604** may be same types of circuits or different types of circuits. In the following discussion, circuits **602** and **604** are referred to as a logic circuit and an SRAM circuit, respectively as an example, while other combinations are also contemplated.

[0018] In accordance with some embodiments, circuit **602** is formed in a device region including n-type FinFET region **100** and p-type FinFET region **200**, and circuit **604** is formed in a device region including n-type FinFET region **300** and p-type FinFET region **400**. Device regions **100**, **200**, **300**, and **400** are also illustrated in FIGS. **1**B and **1**C through **10**C. Semiconductor fins **126**, **226**, **326**, and **426** are formed in regions **100**, **200**, **300**, and **400**, respectively, and are referred to collectively as semiconductor fins **26**. Gate stacks **28** are formed in the directions perpendicular to the lengthwise directions of semiconductor fins **26**. It is noted that although the gate stacks **28** are illustrated as continuously extending into different device regions **100**, **200**, **300**, and **400** for a compact illustration purpose, the gate stacks **28** in different device regions may be physically separated from each other, or some gate stacks **28** in some of device regions may be connected in any combination, while the gate stacks **28** in other device regions are separated.

[0019] FIG. **1**B illustrates the cross-sectional views of semiconductor fins **26** in device regions **100**, **200**, **300**, and **400**, wherein the cross-sectional view is obtained from the plane crossing line B-B in FIG. **1**A. Also, the plane of cross-sectional view is obtained from the middle of two neighboring gate stacks **28** (as schematically illustrated in FIG. **1**C). As shown in FIG. **1**B, distance D**1** between neighboring fins **126** may be greater than, equal to, or smaller than, distance D**1**' between neighboring fins **326**. Distance D**2** between neighboring fins **226** may be greater than, equal to, or smaller than, distance D**2**' between neighboring fins **426**. The illustrated view in FIG. **1**B reflects the structures shown in the regions marked by dashed lines **602** and **604** in FIG. **1**A (also refer to FIG. **11**).

[0020] FIG. **1**C illustrates the cross-sectional views of device regions **100**, **200**, **300**, and **400**, wherein the cross-sectional views are obtained from the planes crossing lines C-C in FIG. **1**A.

[0021] As shown in FIGS. **1**A, **1**B, and **1**C, dielectric layer **38** is formed. The respective step is illustrated as step **502** in the process flow shown in FIG. **12**. Dielectric layer **38** is alternatively referred to as a spacer layer. In accordance with some embodiments of the present disclosure, spacer layer **38** is formed of silicon nitride, silicon oxide, silicon carbo-nitride (SiCN), silicon oxy-carbo-nitride (SiOCN), silicon oxynitride (SiON), while other dielectric materials may be used. Spacer layer **38** may have a thickness in the range between about 2 nm and about 5 nm.

[0022] Spacer layer **38** is formed as a conformal layer, and hence covers the top surfaces and the sidewalls of semiconductor fins **26** (FIG. **1**B) and gate stacks **28** (FIG. **1**C). The portions of spacer layer **38** on the sidewalls of semiconductor fins **26** are used to form fin spacers, as shown in FIG. **2**B, and the portions of spacer layer **38** on the sidewalls of semiconductor fins **26** are used to form gate spacers.

[0023] Mask layer **40** is formed over spacer layer **38**. The respective step is also illustrated as step **502** in the process flow shown in FIG. **12**. The material of mask layer **40** is selected to have a high etching selectivity with relative to the material of spacer layer **38**. In accordance with some embodiments of the present disclosure, the material of mask layer **40** is also selected from silicon nitride, silicon oxide, silicon carbo-nitride (SiCN), silicon oxy-carbo-nitride (SiOCN), and silicon oxynitride (SiON). Mask layer **40** may have a thickness in the range between about 2 nm and about 10 nm. Mask layer **40** is also formed as a conformal layer. The formation of spacer layer **38** and mask layer **40** may be selected from conformal deposition methods such as Atomic

Layer Deposition (ALD) and Chemical Vapor Deposition (CVD). Both spacer layer **38** and mask layer **40** extend into device regions **100**, **200**, **300**, and **400**.

[0024] FIGS. **2**A, **2**B, and **2**C illustrate the patterning of spacer layer **38** in region **100**. First, photo resist **42** is applied and patterned, wherein the photo resist **42** is illustrated in FIGS. **2**B and **2**C, and not in FIGS. **2**A, although it still exists in FIG. **2**A. Photo resist **42** may be a single-layer photo resist, or a tri-layer photo resist including an inorganic layer (known as middle layer) sandwiched between two photo resists (known as under layer and upper layer). The patterned photo resist **42** covers regions **200**, **300**, and **400**, and leaves region **100** uncovered. Next, an etching step is performed to remove the portions of mask layer **40** from region **100**. The respective step is illustrated as step **504** in the process flow shown in FIG. **12**. Depending on the process and the distance between neighboring fins **126** (FIG. **1**C), mask layer **40** may or may not have a residue portion left between neighboring fins **126**, as shown in FIG. **2**B. After mask layer **40** is removed, the portion of spacer layer **38** in region **100** is exposed, and an anisotropic etching is performed to etch spacer layer **38** in region **100**, so that the top portions of spacer layer **38** on top of fins **126** are removed, exposing fins **126**. The respective step is illustrated as step **506** in the process flow shown in FIG. **12**. The remaining portions of spacer layer **38** on the sidewalls of gate stacks **28** become gate spacers **144** (FIG. **2**C), and the remaining portions of spacer layer **38** on the sidewalls of fins **126** (FIG. **1**B) become fin spacers **146** (FIG. **2**B). The etching time of spacer layer **38** is selected so that fin spacers **146** have appropriate height H**1** (FIG. **2**B).

[0025] In a subsequent step, the exposed semiconductor fins **126** are recessed, for example, in an anisotropic or isotropic etching step, so that recesses **148** (FIGS. **2**B and **2**C) are formed to extend into semiconductor fins **126**. The respective step is illustrated as step **508** in the process flow shown in FIG. **12**. The bottoms of recesses **148** may be higher than, level with, or lower than the top surfaces of STI regions **22**. The etching is performed using an etchant that attacks fins **126**, and hardly attacks fin spacers **146**. Accordingly, in the etching step, the height of fin spacers **146** is substantially not reduced. After the formation of recesses **148**, photo resist **42** is removed, for example, in an ashing step.

[0026] FIGS. **3**A, **3**B, and **3**C illustrate the patterning of spacer layer **38** in region **300**. First, photo resist **50** is applied and patterned, wherein the photo resist **50** is illustrated in FIGS. **3**B and **3**C, and not in FIGS. **3**A, although it still exists in FIG. **3**A. Photo resist **50** may also be a single-layer photo resist or a tri-layer photo resist. The patterned photo resist **50** covers regions **100**, **200**, and **400**, and leaves region **300** uncovered. Next, an etching step is performed to remove the portions of mask layer **40** in region **300**. The respective step is illustrated as step **510** in the process flow shown in FIG. **12**. Depending on the process and the distance between neighboring fins **326** (FIG. **2**C), mask layer **40** may, or may not have a residue portion left between neighboring fins **326** (FIG. **3**C). After mask layer **40** is removed, the portion of spacer layer **38** in region **300** is exposed, and an anisotropic etching is performed to etch spacer layer **38**, so that the top portions of spacer layer **38** on top of fins **326** are removed, exposing fins **326**. The respective step is illustrated as step **512** in the process flow shown in FIG. **12**. The remaining portions of spacer layer **38** on the sidewalls of gate stacks **28** become gate spacers **344** (FIG. **3**C), and the remaining portions of spacer layer **38** on the sidewalls of fins **326** (FIG. **3**B) become fin spacers **346** (FIG. **3**B). The etching time of spacer layer **38** is selected so that fin spacers **346** will have appropriate height H**3** (FIG. **3**B).

[0027] In a subsequent step, the exposed semiconductor fins **326** are recessed, for example, in an anisotropic or isotropic etching step, so that recesses **348** (FIGS. **3**B and **3**C) are formed to extend into semiconductor fins **326**. The respective step is illustrated as step **514** in the process flow shown in FIG. **12**. The bottoms of recesses **348** may be higher than, level with or lower than the top surfaces of STI regions **22**. The etching is performed using an etchant that attacks fins **326**, and hardly attacks fin spacers **346**. Accordingly, in the etching step, the height of fin spacers **346** is substantially not reduced. After the formation of recesses **348**, photo resist **50** is removed.

[0028] FIGS. **4**A, **4**B, and **4**C illustrate the simultaneously epitaxy for forming epitaxy semiconductor regions **152** and **352** (which are source/drain regions of FinFETs) in regions **100** and **300**, respectively. The respective step is illustrated as step **516** in the process flow shown in FIG. **12**. In accordance with some embodiments of the present disclosure, the formation of epitaxy regions **152** and **352** includes epitaxially growing silicon phosphorous (SiP) or phosphorous-doped silicon carbon (SiCP), and the resulting FinFETs formed in regions **100** and **300** are n-type FinFETs. As shown in FIG. **4**B, in the initial stage of the epitaxy, the grown epitaxy regions **152** and **352** are confined by fin spacers **146** and **346**. After the epitaxy regions **152** and **352** are grown to higher than the top ends of epitaxy regions **152** and **352**, respectively, lateral growth also occurs along with the vertical growth, and epitaxy regions **152** and **352** expand laterally.

[0029] The portions of epitaxy regions **152** grown from neighboring recesses **148** may be merged as a large epitaxy region, or remain separated from each other when the epitaxy if finished. The portions of epitaxy regions **352** grown from neighboring recesses **348** may also be merged into a large epitaxy region, or remain separated from each other when the epitaxy if finished. In addition, voids **153** and **353** may be formed when mergence occurs. Whether the mergence occurs or not depends on the heights of the respective fin spacers **146** and **346**, and how long the epitaxy lasts. Accordingly, by adjusting heights H**1** and H**3** (FIG. **4**B), one of the following four scenarios may occur: the mergence occurs for both epitaxy regions **152** and **352**, the mergence occurs for epitaxy regions **152** but not for epitaxy regions **352**, the mergence occurs for epitaxy regions **352** but not for epitaxy regions **152**, and the mergence doesn't occur for either of epitaxy regions **152** and **352**. FIG. **4**D illustrates some exemplary embodiments, wherein the unmerged epitaxy regions **152** and **352** are illustrated if the corresponding epitaxy portions **608** in dashed lines don't exist.

[0030] Referring back to FIG. **4**B, if, for example, it is desirable that the mergence occur for epitaxy regions **152** but not for epitaxy regions **352**, fin spacers **146** may be formed to have height H**1** smaller than height H**3** of fin spacers **346**. As a result, the lateral expansion occurs earlier for epitaxy regions **152** than epitaxy regions **352**, and epitaxy regions **152** merge while epitaxy regions **352** don't merge. In accordance with some embodiments of the present disclosure, to make height **H1** smaller than height **H3**, the period of time TP1 for etching spacer layer **38** (the step shown in FIG. **2**B) may be selected to be longer than the period of time TP3 for etching spacer layer **38** (the step shown in FIG. **3**B). In accordance with some embodiments of the present disclosure, ratio TP1/TP3 may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0. As a result, height **H3**/**H1** may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0. With the merging of neighboring epitaxy regions, the resulting FinFET may have a higher drive (saturation current). With the neighboring epitaxy regions not merged, the resulting FinFETs may be more compact. Accordingly, different requirements of different circuits may be met at the same time without requiring the epitaxy regions to be formed by different epitaxy processes.

[0031] Converse to the above discussion, if it is desirable that the mergence occur for epitaxy regions **352** but not form epitaxy regions **152**, fin spacers **146** may be formed to have height **H1** greater than height **H3** of fin spacers **346**. In accordance with some embodiments of the present disclosure, ratio TP3/TP1 may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0. Also, height **H1**/**H3** may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0.

[0032] In accordance with some embodiments, after the epitaxy, an implantation is performed to implant an n-type impurity such as phosphorous or arsenic into epitaxy regions **152** and **352** to form source/drain regions, which are also referred to using reference numerals **152** and **352**. In accordance with alternative embodiments, no implantation of any n-type impurity is performed, and the n-type impurity was provided through the in-situ doping occurred during the epitaxy.

[0033] FIGS. **5**A through **10**C illustrate the formation of epitaxy regions for the FinFETs in regions **200** and **400**, wherein the respective steps are similar to the repetition of the steps for forming epitaxy regions in device regions **100** and **300**, except the conductivity types of some regions are inversed. First, an etching step is performed to remove remaining portions of mask layer **40** from regions **100**, **200**, **300**, and **400**. The respective step is illustrated as step **518** in the process flow shown in FIG. **12**. Some residue portions of mask layer **40** may (or may not) be left after the etch. The resulting structure is shown in FIGS. **5**A, **5**B, and **5**C.

[0034] Next, as shown in FIG. **6**A, **6**B, and **6**C, mask layer **56** is formed. The respective step is illustrated as step **520** in the process flow shown in FIG. **12**. The material and the formation methods of mask layer **56** may be selected from the same candidate materials and candidate methods for forming mask layer **40**. For example, the material of mask layer **56** may be selected from silicon nitride, silicon oxide, SiCN, SiOCN, and SiON. Mask layer **56** may also be formed using ALD or CVD. The thickness of mask layer **56** may be in the range between about 2 nm and about 10 nm.

[0035] FIGS. **7**A, **7**B, and **7**C illustrate the patterning of spacer layer **38** in region **200**. First, photo resist **58** is applied and patterned, wherein the photo resist **58** is illustrated in FIGS. **7**B and **7**C, and not in FIGS. **7**A, although it still exists in FIG. **7**A. The patterned photo resist **58** covers regions **100**, **300**, and **400**, and leaves region **200** uncovered. Next, an etching step is performed to remove the portions of mask layer **56** in region **200**. Depending on the process and the distance between neighboring fins **226** (FIG. **2**C), mask layer **56** may, or may not have a residue portion left between neighboring fins **226** (FIG. **7**B). After mask layer **56** is removed, the portion of spacer layer **38** in region **200** is exposed, and an anisotropic etching is performed to etch spacer layer **38**, so that the top portions of spacer layer **38** on top of fins **226** (FIG. **6**B) are removed, hence exposing fins **226**. The remaining portions of spacer layer **38** on the sidewalls of gate stacks **28** become gate spacers **244** (FIG. **7**C), and the remaining portions of spacer layer **38** on the sidewalls of fins **226** (FIG. **7**B) become fin spacers **246**. The etching time of spacer layer **38** is selected so that fin spacers **246** have appropriate height **H2** (FIG. **7**B).

[0036] In a subsequent step, the exposed semiconductor fins **226** (FIG. **6**B) are etched, for example, in an anisotropic or isotropic etching step, so that recesses **248** (FIGS. **7**B and **7**C) are formed to extend into semiconductor fins **226**. The bottoms of recesses **248** may be higher than, level with, or lower than the top surfaces of STI regions **22**. The etching is performed using an etchant that attacks fins **226**, and hardly attacks fin spacers **246**. Accordingly, in the etching step, the height **H2** of fin spacers **246** is substantially not reduced. After the formation of recesses **248**, photo resist **58** is removed.

[0037] FIGS. **8**A, **8**B, and **8**C illustrate the patterning of spacer layer **38** in region **400**. First, photo resist **62** is applied and patterned, wherein the photo resist **62** is illustrated in FIGS. **8**B and **8**C, and not in FIGS. **8**A, although it still exists in FIG. **8**A. The patterned photo resist **62** covers regions **100**, **200**, and **300**, and leaves region **400** uncovered. Next, an etching step is performed to remove the portions of mask layer **56** in region **400**. Depending on the process and the distance D2' between neighboring fins **426** (FIG. **2**C), mask layer **56** may, or may not have a residue portion left between neighboring fins **426** (FIG. **8**B). After mask layer **56** is removed, the portion of spacer layer **38** in region **400** is exposed, and an anisotropic etching is performed to etch spacer layer **38**, so that the top portions of spacer layer **38** on top of fins **426** (FIG. **7**B) are removed, exposing fins **426**. The remaining portions of spacer layer **38** on the sidewalls of gate stacks **28** become gate spacers **444** (FIG. **8**C), and the remaining portions of spacer layer **38** on the sidewalls of fins **426** (FIG. **8**B) become fin spacers **446**. The etching time of spacer layer **38** is selected so that fin spacers **446** have appropriate height **H4** (FIG. **8**B).

[0038] In a subsequent step, the exposed semiconductor fins **426** (FIG. **7**B) are etched, for example, in an anisotropic or isotropic etching step, so that recesses **448** (FIGS. **8**B and **8**C) are formed to extend into semiconductor fins **426**. The bottoms of recesses **448** may be higher than, level with or lower than the top surfaces of STI regions **22**. The etching is performed using an etchant that attacks fins **426**, and hardly attack fin spacers **446**. Accordingly, in the etching step, the height of fin spacers **446** is substantially not reduced. After the formation of recesses **448**, photo resist **62** is removed.

[0039] FIGS. **9**A, **9**B, and **9**C illustrate the simultaneously epitaxy for forming epitaxy regions **252** and **452** (which are source/drain regions of FinFETs) in regions **200** and **400**, respectively. In accordance with some embodiments of the present disclosure, the formation of epitaxy regions **252** and **452** includes epitaxially growing silicon germanium, wherein boron may be in-situ doped, so that the resulting FinFETs formed in regions **200** and **400** are p-type FinFETs. As also shown in FIG. **9**B, in the initial stage of the epitaxy, the grown epitaxy regions **252** and **452** are confined by fin spacers **246** and **446**, respectively. After epitaxy regions **252** and **452** are grown to higher than the top ends of epitaxy regions **252** and **452**, respectively, lateral growth also occurs along with the vertical growth, and epitaxy regions **252** and **452** expand laterally.

[0040] The portions of epitaxy regions **252** grown from neighboring recesses **248** may be merged into a large epitaxy region. In accordance with some embodiments of the present disclosure, the portions of epitaxy regions **452** grown from neighboring recesses **148** are not merged. This is achieved by making height H**4** (FIG. **9**B) of fin spacers **446** to be greater than height H2 of fin spacers **246**. To make height H**4** to be greater than height H2, the period of time TP4 for etching spacer layer **38** (the step shown in FIG. **8**B) may be selected to be shorter than the period of time TP2 for etching spacer layer **38** (the step shown in FIG. **7**B). In accordance with some embodiments of the present disclosure, ratio TP2/TP4 may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0. As a result, height H**4**/H2 may be greater than about 1.5, and may be in the range between about 1.5 and about 5.0.

[0041] In accordance with alternative embodiments, the processes for forming fin spacers **236** and **446** may be adjusted to adjust heights H2 and H**4**, and to result in one of the following results: the mergence occurs for both epitaxy regions **252** and **452** (height H2 and H**4** are substantially equal, for example, with difference smaller than about 10 percent), the mergence occurs for epitaxy regions **452** but not for epitaxy regions **252** (with height H2>H**4**), and the mergence doesn't occur for either of epitaxy regions **252** and **452**.

[0042] In accordance with some embodiments, after the epitaxy, an implantation is performed to implant a p-type impurity such as boron or indium into epitaxy regions **252** and **452** to form source/drain regions, which are also referred to using reference numerals **252** and **452**. In accordance with alternative embodiments, no implantation of p-type impurity is performed.

[0043] An etching step is then performed to remove remaining portions of mask layer **56** from regions **100**, **200**, **300**, and **400**, and FIGS. **10**A, **10**B, and **10**C illustrate the structure after mask layer **56** is removed. N-type FinFET **166**, p-type FinFET **266**, n-type FinFET **366**, and p-type FinFETs **466** are thus formed in regions **100**, **200**, **300**, and **400**, respectively. In subsequent steps, source/drain silicide regions (not shown) are formed on the top surfaces of source/drain regions **152**, **252**, **352**, and **452**. An Inter-Layer Dielectric (ILD, not shown) is formed to cover the illustrated FinFETs, and source/drain contact plugs (not shown) may be formed in the ILD to contact the source/drain silicide regions. Gate contact plugs (not shown) may also be formed to contact the illustrated gate electrodes in gate stacks **28**. Also, the illustrate gate stacks **28** may be replaced with replacement gate stacks if gate stacks **28** are dummy gate stacks.

[0044] The embodiments of the present disclosure have some advantageous features. By separating the formation of fin spacers in different device regions, the heights of the fin spacers in different device regions may be adjusted separately. This advantageously results in the flexibility in forming merged or un-merged epitaxy source/drain regions. The formation of the fin spacers shares a common deposition process, and the epitaxy for forming source/drain regions for different device regions is also a common process. The manufacture cost is thus reduced.

[0045] In accordance with some embodiments of the present disclosure, a method includes forming a first gate stack extending on top surfaces and sidewalls of first semiconductor fins with the first semiconductor fins being parallel to and neighboring each other, forming a second gate stack extending on top surfaces and sidewalls of second semiconductor fins with the second semiconductor fins being parallel to and neighboring, each other, and forming a dielectric layer. The dielectric layer includes a first portion extending on the first gate stack and the first semiconductor fins, and a second portion extending on the second gate stack and the second semiconductor fins. In a first etching process, the first portion of the dielectric layer is etched to form first fin spacers on sidewalls of the first semiconductor fins. The first fin spacers have a first height. In a second etching process, the second portion of the dielectric layer is etched to form second fin spacers on sidewalls of the second semiconductor fins. The second fin spacers have a second height greater than the first height. The first semiconductor fins are recessed to form first recesses between the first fin spacers. The second semiconductor fins are recessed to form second recesses between the second fin spacers. The method further includes simultaneously growing first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses. The first epitaxy semiconductor regions grown from neighboring ones of the first recesses merge with each other. The second epitaxy semiconductor regions grown from neighboring ones of the second recesses are separate from each other.

[0046] In accordance with some embodiments of the present disclosure, a method includes etching a first semiconductor fin and a second semiconductor fin to form first recesses. The first and the second semiconductor fins have a first distance. A third semiconductor fin and a fourth semiconductor fin are etched to form second recesses. The third and the fourth semiconductor fins have a second distance equal to or smaller than the first distance. An epitaxy is performed to simultaneously grow first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses. The first epitaxy semiconductor regions are merged with each other, and the second epitaxy semiconductor regions are separated from each other.

[0047] In accordance with some embodiments of the present disclosure, a method includes, in a common deposition process, forming a dielectric layer including a first portion on top surfaces and sidewalls of first semiconductor fins and a second portion on top surfaces and sidewalls of second semiconductor fins. In separate etching processes, the first portion of the dielectric layer and the second portion of the dielectric layer are etched to form first fin spacers and second fin spacers, respectively. The first fin spacers have a first height, and the second fin spacers have a second height greater than the first height. The first semiconductor fins are etched to form first recesses between the first fin spacers. The second semiconductor fins are etched to form second recesses between the second fin spacers. In a common epitaxy process, first epitaxy semiconductor regions are growth from the first recesses, and second epitaxy semiconductor regions are grown from the second recesses. The first epitaxy semiconductor regions merge with each other, and the second epitaxy semiconductor regions are discrete from each other.

[0048] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method comprising:

forming a first semiconductor fin, a second semiconductor fin, a third semiconductor fin, and a fourth semiconductor fin protruding higher than top surfaces of isolation regions, wherein the first semiconductor fin is close to, and have a first distance from, the second semiconductor fin, and the third semiconductor fin is close to, and have a second distance from, the fourth semiconductor fin, wherein the second distance is equal to or smaller than the first distance;

etching the first semiconductor fin and the second semiconductor fin to form first recesses;

etching the third semiconductor fin and the fourth semiconductor fin to form second recesses; and

performing an epitaxy to simultaneously grow first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses, wherein the first epitaxy semiconductor regions are merged with each other, and the second epitaxy semiconductor regions are separated from each other.

2. The method of claim **1**, wherein the second distance is smaller than the first distance.

3. The method of claim **1**, wherein the first recesses are between first fin spacers, and the second recesses are between second fin spacers higher than the first fin spacers.

4. The method of claim **3** further comprising:

forming a dielectric layer covering the first, the second, the third, and the fourth semiconductor fins; and

etching the dielectric layer to form the first fin spacers and the second fin spacers.

5. The method of claim **4**, wherein the first fin spacers and the second fin spacers are formed in separate etching steps.

6. The method of claim **4**, wherein the first fin spacers and the second fin spacers are formed to have different heights.

7. The method of claim **1**, wherein the first epitaxy semiconductor regions and the second epitaxy semiconductor regions are source/drain regions of Fin Field-Effect Transistors (FinFETs).

8. The method of claim **1**, wherein the first epitaxy semiconductor regions and the second epitaxy semiconductor regions are p-type source/drain regions.

9. The method of claim **1**, wherein the first epitaxy semiconductor regions and the second epitaxy semiconductor regions are n-type source/drain regions.

10. A method comprising:

forming first gate spacers on sidewalls of a first semiconductor fin and a second semiconductor fin;

forming first gate stacks on the first semiconductor fin and the second semiconductor fin;

etching the first semiconductor fin and the second semiconductor fin to form first recesses;

forming second gate spacers on sidewalls of a third semiconductor fin and a fourth semiconductor fin;

forming second gate stacks on the third semiconductor fin and the fourth semiconductor fin;

etching the third semiconductor fin and the fourth semiconductor fin to form second recesses; and

performing an epitaxy to simultaneously grow first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses, wherein when the epitaxy is finished, the first epitaxy semiconductor regions are merged with each other, and the second epitaxy semiconductor regions are separated from each other.

11. The method of claim **10**, wherein the first and the second semiconductor fins have a first distance, and wherein the third and the fourth semiconductor fins have a second distance different from the first distance.

12. The method of claim **11**, wherein the second distance is smaller than the first distance.

13. The method of claim **11**, wherein the second distance is equal to the first distance.

14. The method of claim **10** further comprising:

forming first fin spacers on sidewalls of the first semiconductor fin and the second semiconductor fin; and

forming second fin spacers on sidewalls of the third semiconductor fin and the fourth semiconductor fin, wherein the first fin spacers have a first height, and the second fin spacers have a second height different from the first height.

15. The method of claim **14**, wherein the first height is smaller than the second height.

16. The method of claim **14**, wherein the first fin spacers and the second fin spacers are formed in separate etching steps.

17. A method comprising:

forming a first semiconductor fin, a second semiconductor fin, a third semiconductor fin, and a fourth semiconductor fin protruding higher than top surfaces of isolation regions, wherein the first semiconductor fin is close to the second semiconductor fin, and the third semiconductor fin is close to the fourth semiconductor fin;

forming gate stacks to cover portions of each of the first semiconductor fin, the second semiconductor fin, the third semiconductor fin, and the fourth semiconductor fin;

in a first etching process, etching portions of the first semiconductor fin and the second semiconductor fin to form first recesses;

in a second etching process, etching the third semiconductor fin and the fourth semiconductor fin to form second recesses;

performing an epitaxy to grow first epitaxy semiconductor regions from the first recesses and second epitaxy semiconductor regions from the second recesses; and

continuing the epitaxy until the first epitaxy semiconductor regions are merged with each other; and stopping the epitaxy before the second epitaxy semiconductor regions are merged with each other.

18. The method of claim **17**, wherein the first epitaxy semiconductor regions and the second epitaxy semiconductor regions are both n-type source/drain regions.

19. The method of claim **17**, wherein the first epitaxy semiconductor regions and the second epitaxy semiconductor regions are both p-type source/drain regions.

20. The method of claim **17**, wherein the first semiconductor fin and the second semiconductor fin have a first distance, and the third semiconductor fin and the fourth semiconductor fin are immediate neighboring fins having a second distance greater than the first distance.

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