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(54) **PIXEL UNIT CIRCUIT, METHOD OF DRIVING THE SAME, PIXEL CIRCUIT AND DISPLAY DEVICE**

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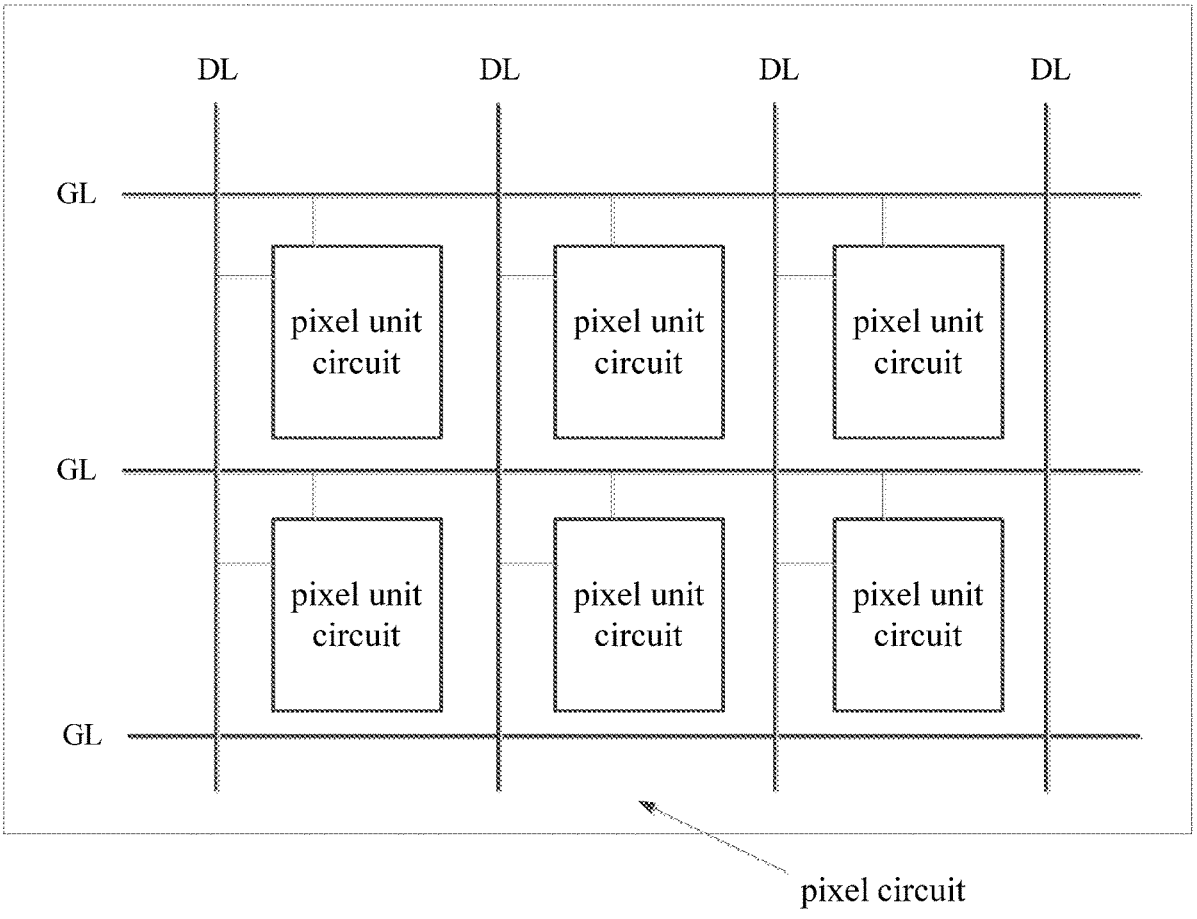
(57) **ABSTRACT**

A pixel unit circuit, a method of driving the same, a pixel circuit and a display device are provided. A pixel unit circuit includes a light-emitting component, a driving transistor, a data writing circuit and a storage capacitor circuit. The data writing circuit is coupled to a data line, a gate line and a gate electrode of the driving transistor, and configured to, under a control of the gate line, enable a connection between the data line and the gate electrode of the driving transistor to be turned on or off. A first end of the storage capacitor circuit is coupled to the gate electrode of the driving transistor, and a second end of the storage capacitor circuit is coupled to a reference voltage input terminal. A second end of the light-emitting component is coupled to a low-level input terminal.



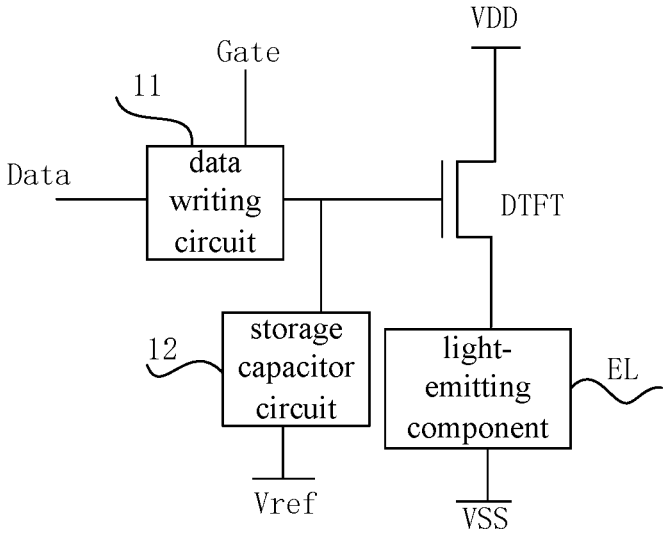


Fig. 1

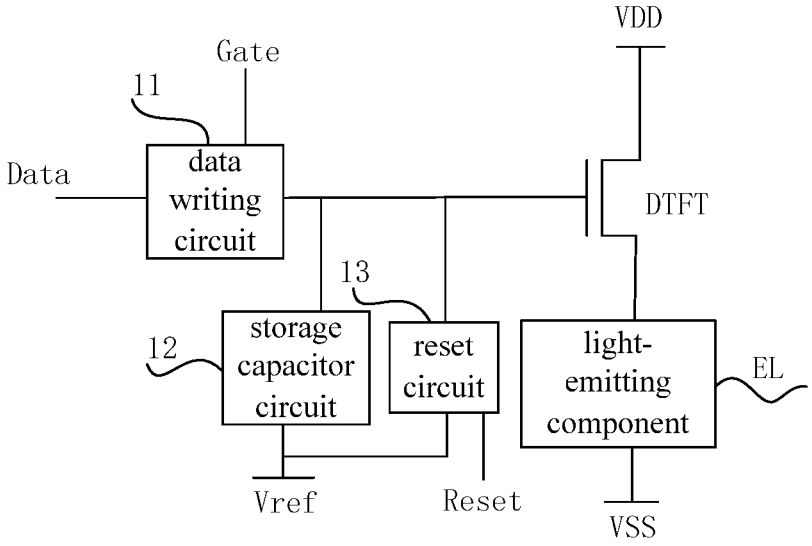


Fig. 2

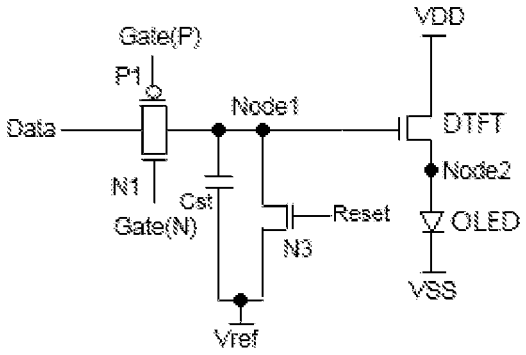


Fig. 3

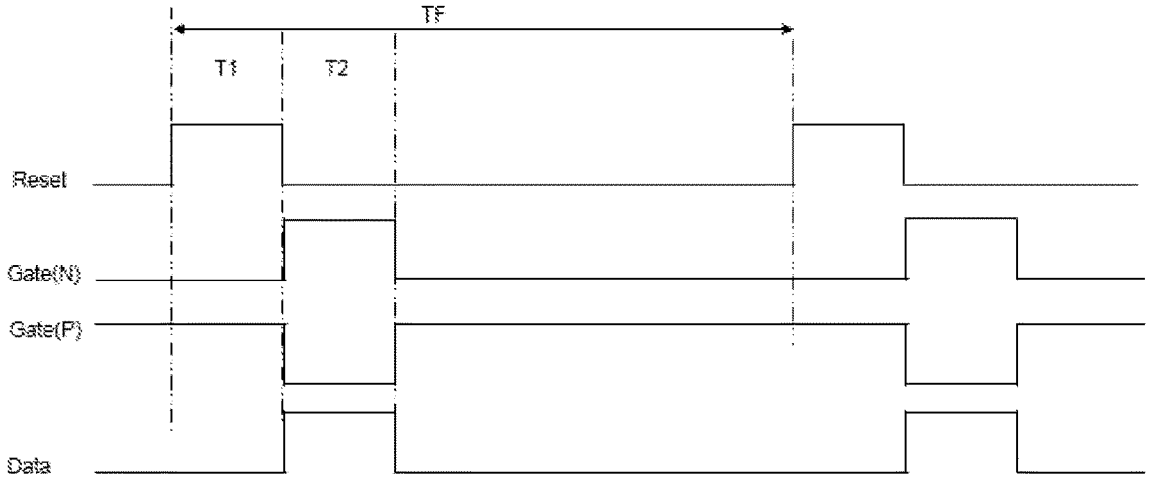


Fig. 4

in each display period, in a light-emitting phase, under a control of the gate line, enabling by the data writing circuit a connection between the data line and the gate electrode of the driving transistor to be turned on, to enable the driving transistor to work in a constant-current region to drive the light-emitting component to emit light, where a source electrode voltage of the driving transistor varies with a gate electrode potential of the driving transistor

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Fig. 5

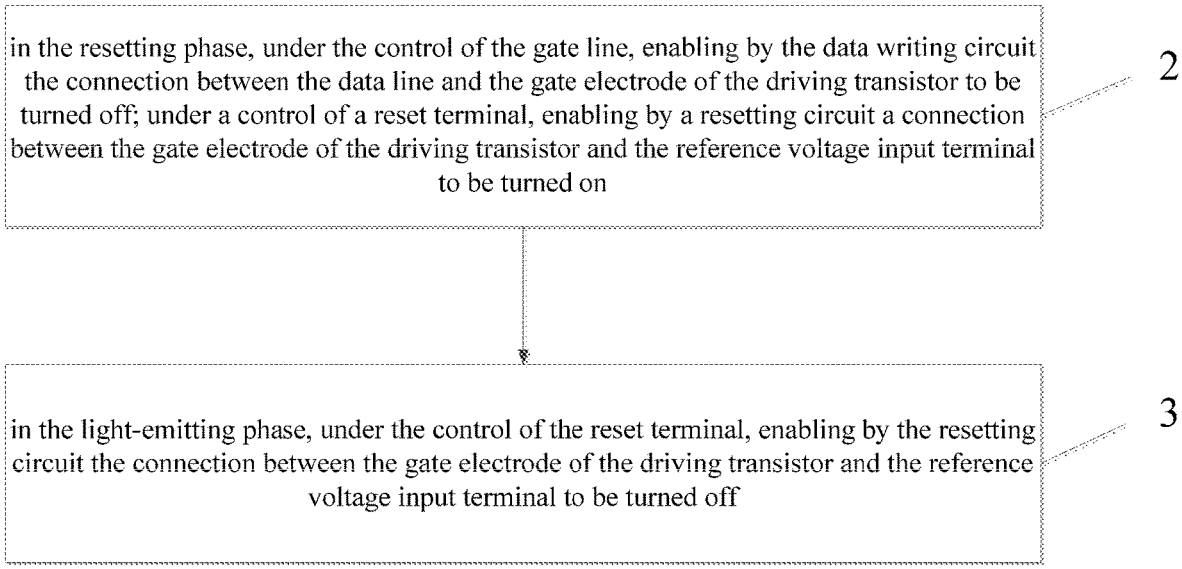
in the resetting phase, under the control of the gate line, enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off; under a control of a reset terminal, enabling by a resetting circuit a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on
2
in the light-emitting phase, under the control of the reset terminal, enabling by the resetting circuit the connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned off
3

Fig. 6

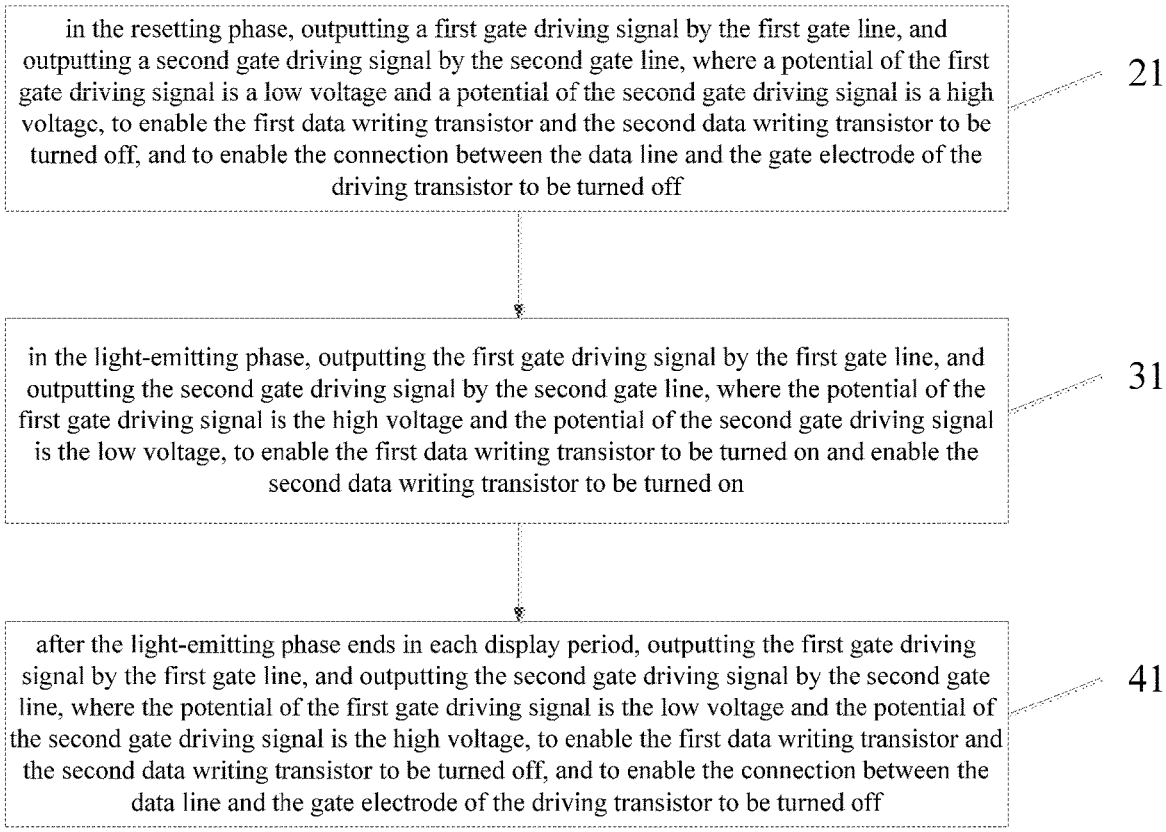
in the resetting phase, outputting a first gate driving signal by the first gate line, and outputting a second gate driving signal by the second gate line, where a potential of the first gate driving signal is a low voltage and a potential of the second gate driving signal is a high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off
21
in the light-emitting phase, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the high voltage and the potential of the second gate driving signal is the low voltage, to enable the first data writing transistor to be turned on and enable the second data writing transistor to be turned on
31
after the light-emitting phase ends in each display period, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the low voltage and the potential of the second gate driving signal is the high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off
41

Fig. 7

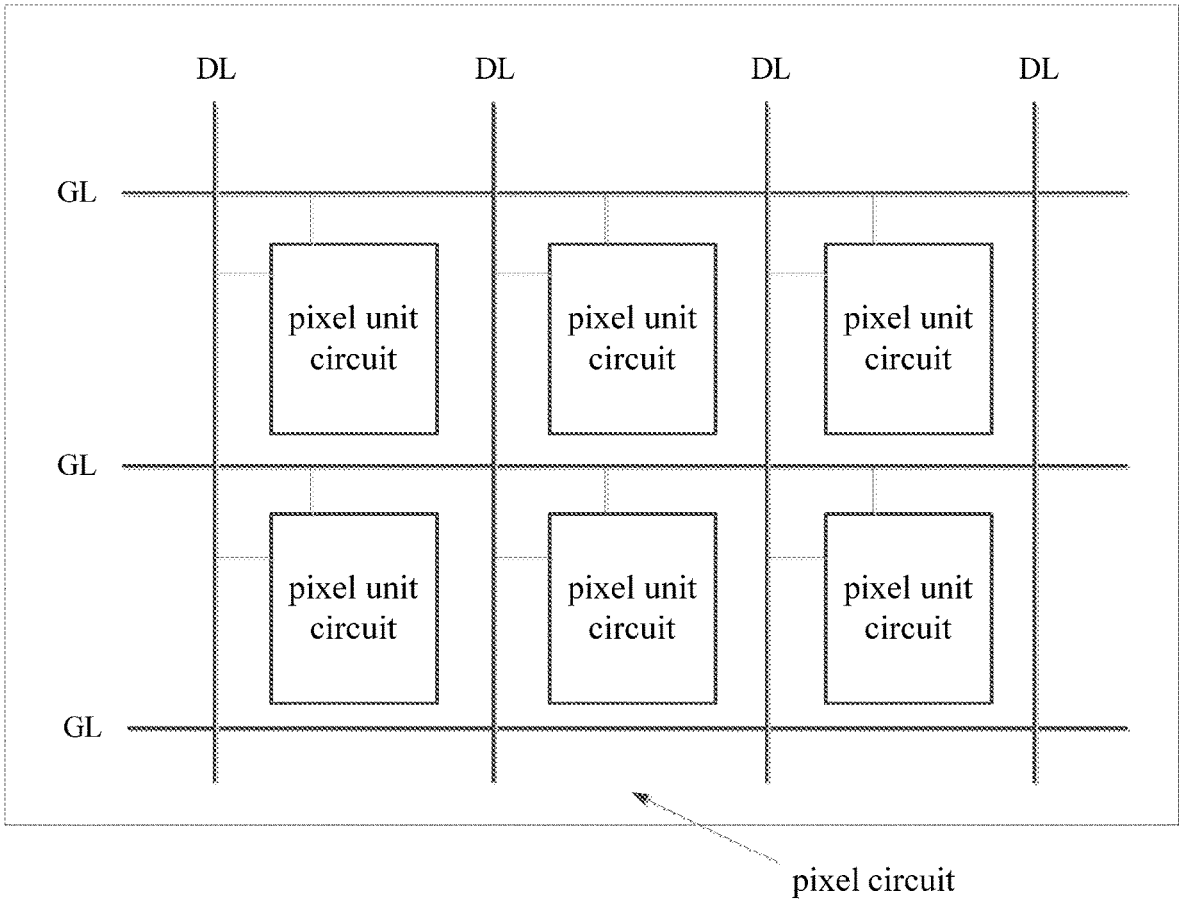
DL
DL
DL
DL
GL
GL
GL
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel circuit

Fig. 8

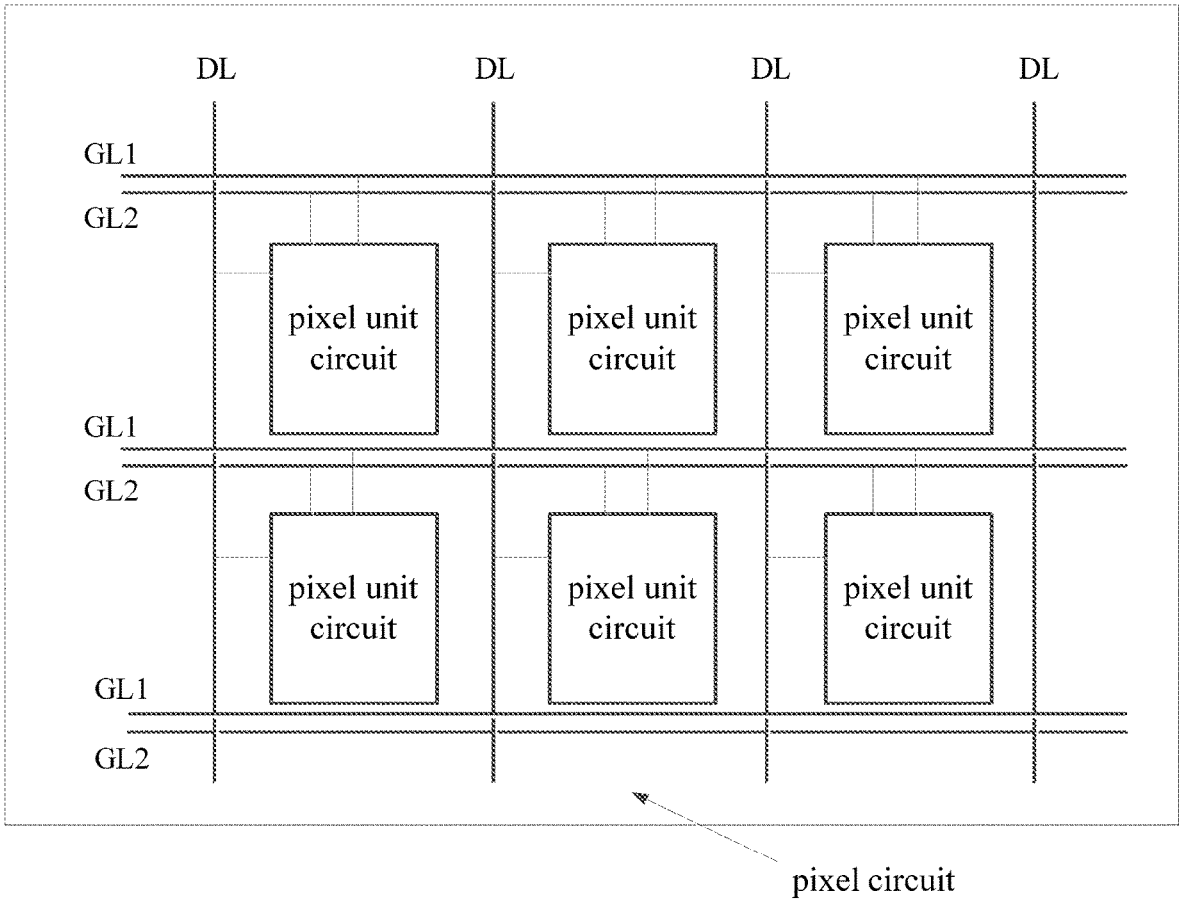
DL
DL
DL
DL
GL1
GL2
pixel unit circuit
pixel unit circuit
pixel unit circuit
GL1
GL2
pixel unit circuit
pixel unit circuit
pixel unit circuit
GL1
GL2
pixel circuit

Fig. 9

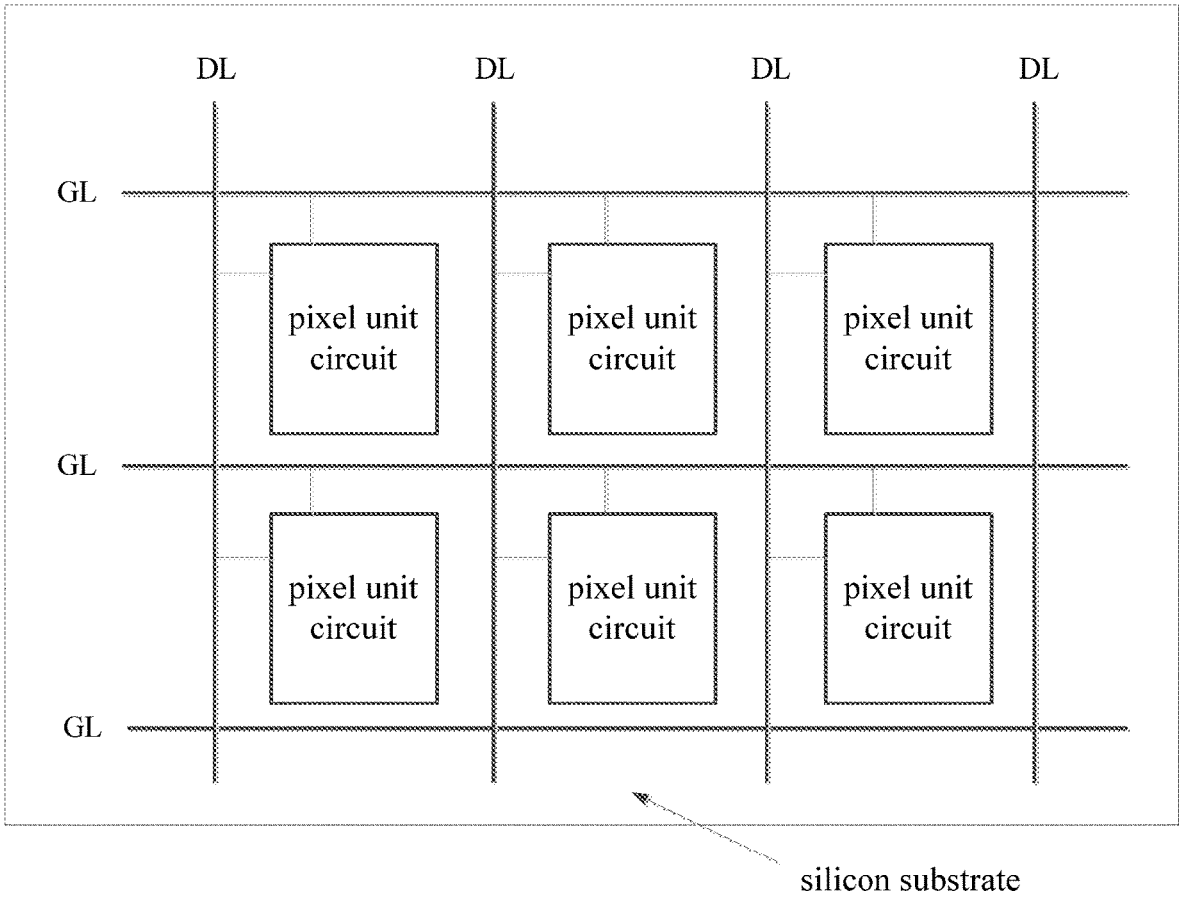
DL
DL
DL
DL
GL
GL
GL
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
pixel unit circuit
silicon substrate

Fig. 10

PIXEL UNIT CIRCUIT, METHOD OF DRIVING THE SAME, PIXEL CIRCUIT AND DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is the U.S. national phase of PCT Application No. PCT/CN2018/098256 filed on Aug. 2, 2018, which claims priority to Chinese Patent Application No. 201710655886.7 filed on Aug. 3, 2017, which are incorporated herein by reference in their entireties.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of display technologies, and in particular, to a pixel unit circuit, a method of driving the same, a pixel circuit and a display device.

BACKGROUND

[0003] The luminance of a silicon-based OLED (Organic Light-Emitting Diode) is usually controlled by driving a current in a subthreshold region of a MOS transistor (metal-oxide-semiconductor field effect transistor). Since the current of the MOS transistor is proportional to its width-to-length ratio, in order to realize the small current of the micro display pixel, the ratio of the W/L (width to length ratio) must be designed to be very small, that is, the length L of the driving MOS transistor must be designed to be very large. As a result, it is very difficult to apply to high-resolution products. The storage capacitor cannot be made large, and the data voltage cannot be stably maintained, resulting in unstable OLED brightness. The subthreshold current of the MOS transistor is sensitive to the gate-source voltage and the threshold voltage, and the peripheral circuit is very complicated, In general, the silicon-based pixel circuit (using a control MOS transistor operating at a subthreshold) is difficult to reduce the area of the driving MOS transistor, so it is difficult to be applied to ultra-high resolution products. The current is sensitive to the gate-source voltage and threshold voltage of the control MOS transistor, and the peripheral circuit is relatively complicated.

SUMMARY

[0004] A pixel unit circuit is provided in the present disclosure, including a light-emitting component, a driving transistor, a data writing circuit and a storage capacitor circuit, where

[0005] a drain electrode of the driving transistor is coupled to a high-level input terminal, a source electrode of the driving transistor is coupled to a first end of the light-emitting component, the driving transistor is an n-type transistor;

[0006] the data writing circuit is coupled to a data line, a gate line and a gate electrode of the driving transistor, and configured to, under a control of the gate line, enable a connection between the data line and the gate electrode of the driving transistor to be turned on or off;

[0007] a first end of the storage capacitor circuit is coupled to the gate electrode of the driving transistor, and a second end of the storage capacitor circuit is coupled to a reference voltage input terminal;

[0008] a second end of the light-emitting component is coupled to a low-level input terminal.

[0009] Optionally, the pixel unit circuit further includes a reset circuit, where

[0010] the reset circuit is coupled to a reset terminal, the reference voltage input terminal and the gate electrode of the driving transistor, and configured to, under a control of the reset terminal, enable a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on or off.

[0011] Optionally, the reset circuit includes a reset transistor, a gate electrode of the reset transistor is coupled to the reset terminal, a first electrode of the reset transistor is coupled to the gate electrode of the driving transistor, a second electrode of the reset transistor is coupled to the reference voltage input terminal, the reset transistor is an n-type transistor or a p-type transistor.

[0012] Optionally, the gate line includes a first gate line and a second gate line;

[0013] the data writing circuit includes:

[0014] a first data writing transistor, where a gate electrode of the first data writing transistor is coupled to the first gate line, a first electrode of the first data writing transistor is coupled to the data line, a second electrode of the first data writing transistor is coupled to the gate electrode of the driving transistor; and

[0015] a second data writing transistor, where a gate electrode of the second data writing transistor is coupled to the second gate line, a first electrode of the second data writing transistor is coupled to the gate electrode of the driving transistor, a second electrode of the second data writing transistor is coupled to the data line;

[0016] the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor.

[0017] Optionally, an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor.

[0018] Optionally, the storage capacitor circuit includes a storage capacitor, where a first end of the storage capacitor is coupled to the gate electrode of the driving transistor and a second end of the storage capacitor is coupled to the reference voltage input terminal.

[0019] Optionally, the light-emitting component includes an organic light-emitting diode, a first end of the light-emitting component is an anode of the organic light-emitting diode, and a second end of the light-emitting component is a cathode of the organic light-emitting diode.

[0020] A method of driving the pixel unit circuit hereinabove is further provided in the present disclosure, including: in each display period,

[0021] in a light-emitting phase, under a control of the gate line, enabling by the data writing circuit a connection between the data line and the gate electrode of the driving transistor to be turned on, to enable the driving transistor to work in a constant-current region to drive the light-emitting component to emit light, where a source electrode voltage of the driving transistor varies with a gate electrode potential of the driving transistor.

[0022] Optionally, each display period further includes a resetting phase, the method further includes:

[0023] in the resetting phase, under the control of the gate line, enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off; under a control of a reset terminal,

enabling by a resetting circuit a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on;

[0024] in the light-emitting phase, under the control of the reset terminal, enabling by the resetting circuit the connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned off.

[0025] Optionally, the reference voltage input terminal is configured to input a reference voltage;

[0026] a difference between the reference voltage and a threshold voltage of the driving transistor is smaller than a sum value of a low level input by the low-level input terminal and a light-up voltage of the light-emitting component.

[0027] Optionally, the gate line includes a first gate line and a second gate line, and the data writing circuit includes: a first data writing transistor, where a gate electrode of the first data writing transistor is coupled to the first gate line; a second data writing transistor, where a gate electrode of the second data writing transistor is coupled to the second gate line; the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor; and when an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor,

[0028] the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off in the resetting phase under the control of the gate line, further includes:

[0029] outputting a first gate driving signal by the first gate line, and outputting a second gate driving signal by the second gate line, where a potential of the first gate driving signal is a low voltage and a potential of the second gate driving signal is a high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off;

[0030] the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned on in the light-emitting phase under the control of the gate line, includes:

[0031] outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the high voltage and the potential of the second gate driving signal is the low voltage, to enable the first data writing transistor to be turned on and enable the second data writing transistor to be turned on;

[0032] the method further includes: after the light-emitting phase ends in each display period, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the low voltage and the potential of the second gate driving signal is the high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off.

[0033] A pixel circuit is further provided in the present disclosure, including a plurality of rows of gate lines, a plurality of columns of data lines and a plurality of pixel unit circuits arranged in an array form hereinabove, where

[0034] the pixel unit circuits in the same row are coupled to the gate lines in the same row, and

[0035] the pixel unit circuits in the same column are coupled to the data lines in the same column.

[0036] Optionally, the gate lines include first gate lines and second gate lines, and the pixel unit circuits in the same row are each coupled to the first gate lines in the same row and the second gate lines in the same row.

[0037] A display device is further provided in the present disclosure, including a plurality of rows of gate lines, a plurality of columns of data lines and a plurality of pixel unit circuits arranged in an array form hereinabove, where

[0038] the pixel unit circuits in the same row are coupled to the gate lines in the same row, and

[0039] the pixel unit circuits in the same column are coupled to the data lines in the same column.

[0040] Optionally, the display device further includes a silicon substrate, where the plurality of rows of gate lines, the plurality of columns of data lines and the plurality of pixel unit circuits are arranged on the silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] FIG. **1** is a schematic view of a pixel unit circuit in some embodiments of the present disclosure;

[0042] FIG. **2** is a schematic view of a pixel unit circuit in some embodiments of the present disclosure;

[0043] FIG. **3** is a circuit diagram of a pixel unit circuit in some embodiments of the present disclosure;

[0044] FIG. **4** is a working sequence diagram of the pixel unit circuit shown in FIG. **2** of the present disclosure;

[0045] FIG. **5** is a flow chart of a method of driving a pixel unit circuit in some embodiments of the present disclosure;

[0046] FIG. **6** is a flow chart of a method of driving a pixel unit circuit in some embodiments of the present disclosure;

[0047] FIG. **7** is a flow chart of a method of driving a pixel unit circuit in some embodiments of the present disclosure;

[0048] FIG. **8** is a schematic view of a pixel circuit in some embodiments of the present disclosure;

[0049] FIG. **9** is a schematic view of a pixel circuit in some embodiments of the present disclosure; and

[0050] FIG. **10** is a schematic view of a display device in some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0051] The present disclosure will be described hereinafter in a clear and complete manner in conjunction with the drawings and embodiments. Obviously, the following embodiments merely relate to a part of, rather than all of, the embodiments of the present disclosure, and based on these embodiments, a person skilled in the art may, without any creative effort, obtain the other embodiments, which also fall within the scope of the present disclosure.

[0052] The transistors in all embodiments of the present disclosure may each be a thin film transistor or a field-effect transistor or other devices having the same characteristics. In the embodiments of the present disclosure, in order to distinguish the two electrodes of the transistor except the gate electrode, one of the electrodes is referred to as a first electrode, and the other electrode is referred to as a second electrode. In the actual operation, the first electrode may be a drain electrode, and the second electrode may be a source electrode; or the first electrode may be a source electrode, and the second electrode may be a drain electrode.

[0053] As shown in FIG. **1**, a pixel unit circuit in some embodiments of the present disclosure includes a light-emitting component, a driving transistor, a data writing circuit and a storage capacitor circuit, where

[0054] a drain electrode of the driving transistor DTFT is coupled to a high-level input terminal configured to input a high level VDD, a source electrode of the driving transistor DTFT is coupled to a first end of the light-emitting component EL, the driving transistor DTFT is an n-type transistor;

[0055] the data writing circuit **11** is coupled to a data line Data, a gate line Gate and a gate electrode of the driving transistor DTFT, and configured to, under a control of the gate line Gate, enable a connection between the data line Data and the gate electrode of the driving transistor DTFT to be turned on or off;

[0056] a first end of the storage capacitor circuit **12** is coupled to the gate electrode of the driving transistor DTFT, and a second end of the storage capacitor circuit **12** is coupled to a reference voltage input terminal configured to input a reference voltage Vref;

[0057] a second end of the light-emitting component EL is coupled to a low-level input terminal configured to input a low level VSS.

[0058] Specifically, the driving transistor may be an NMOS (N-Metal-Oxide-Semiconductor) tube.

[0059] According to the embodiments of the present disclosure, the pixel unit circuit, by utilizing a source electrode follow characteristic of an NMOS transistor (i.e., a driving transistor, a n-type driving transistor) at a constant current (that is, when the driving transistor operates in a constant-current region), changes the potential of the gate electrode of the driving transistor (that is, the potential of the data voltage outputted by the data line) to change the voltage of the source electrode of the driving transistor, and adjusts the illuminance of the light-emitting component by adjusting the voltage difference between the first end of the light-emitting component and the second end of the light-emitting component, thereby solving the following technical issues in the related art: the driving transistor driving the silicon-based OLED to emit light works in the subthreshold region, so the size of the driving transistor needs to be very large, so it cannot be applied to a high-resolution display product, and the size of the storage capacitor cannot be made large, resulting in a that the luminance of the light-emitting component is unstable due to the inability to stably maintain the data voltage.

[0060] Optionally, as shown in FIG. **2**, the pixel unit circuit in some embodiments of the present disclosure further includes a reset circuit **13**;

[0061] The reset circuit **13** is coupled to a reset terminal Reset, the reference voltage input terminal configured to input the reference voltage Vref and the gate electrode of the driving transistor DTFT, and configured to, under a control of the reset terminal Reset, enable a connection between the gate electrode of the driving transistor DTFT and the reference voltage input terminal configured to input the reference voltage Vref to be turned on or off.

[0062] In some embodiments of the present disclosure, the pixel unit circuit may further include the reset circuit **13** to control the potentials of two ends of the storage capacitor circuit **12** to be equal in the resetting phase, thereby quickly discharging the storage capacitor circuit **12**, ensuring that the image of the previous frame does not affect the image of the next frame. By adjusting the voltage value of Vref, the difference between the potential Vref−Vth of the first end of the light-emitting component and the potential VSS of the second end of the light-emitting component in the resetting phase may be smaller than the light-up voltage of the light-emitting component, so that the light-emitting components do not emit light during the resetting phase, and the dynamic image sticking may not occur in the dynamic picture.

[0063] Specifically, the reset circuit may include a reset transistor, a gate electrode of the reset transistor is coupled to the reset terminal, a first electrode of the reset transistor is coupled to the gate electrode of the driving transistor, a second electrode of the reset transistor is coupled to the reference voltage input terminal, the reset transistor is an n-type transistor or a p-type transistor.

[0064] Optionally, the gate line includes a first gate line and a second gate line;

[0065] The data writing circuit includes:

[0066] a first data writing transistor, where a gate electrode of the first data writing transistor is coupled to the first gate line, a first electrode of the first data writing transistor is coupled to the data line, a second electrode of the first data writing transistor is coupled to the gate electrode of the driving transistor; and

[0067] a second data writing transistor, where a gate electrode of the second data writing transistor is coupled to the second gate line, a first electrode of the second data writing transistor is coupled to the gate electrode of the driving transistor, a second electrode of the second data writing transistor is coupled to the data line;

[0068] the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor.

[0069] Optionally, the data writing circuit includes two data writing transistors of opposite types, thereby improving the loss of the transmitted data voltage due to using a single transistor while ensuring that the amplitude range in which the data voltage can be written becomes larger.

[0070] Optionally, an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor.

[0071] Optionally, the first data writing transistor and the second data writing transistor adopt a TFT characteristic curve symmetrical transistor, that is, the absolute value of the threshold voltage of the first data writing transistor is equal to the absolute value of the threshold voltage of the second data writing transistor, thereby solving the glitch caused by the sudden jump of the gate driving signals of the two gate lines.

[0072] Specifically, the storage capacitor circuit may include a storage capacitor, where a first end of the storage capacitor is coupled to the gate electrode of the driving transistor and a second end of the storage capacitor is coupled to the reference voltage input terminal

[0073] Specifically, the light-emitting component may include an organic light-emitting diode; an anode of the organic light-emitting diode is a first end of the light-emitting component, and a cathode of the organic light-emitting diode is a second end of the light-emitting component.

[0074] As shown in FIG. **3**, the pixel unit circuit in some embodiments of the present disclosure includes: an organic

light-emitting diode OLED, a driving transistor DTFT, a data writing circuit, a storage capacitor Cst and a resetting circuit **12**, wherein

[0075] a drain electrode of the driving transistor DTFT is coupled to a high-level input terminal configured to input a high level VDD, a source electrode of the driving transistor DTFT is coupled to an anode of the organic light-emitting diode OLED, the driving transistor DTFT is an n-type transistor;

[0076] a first end of the storage capacitor Cst is coupled to the gate electrode of the driving transistor DTFT, and a second end of the storage capacitor Cst is coupled to a reference voltage input terminal configured to input a reference voltage Vref;

[0077] a cathode of the organic light-emitting diode OLED is coupled to a low-level input terminal configured to input a low level VSS;

[0078] The reset circuit includes: a reset transistor N**3**, a gate electrode of the reset transistor N**3** is coupled to the reset terminal Reset, a source electrode of the reset transistor N**3** is coupled to the gate electrode of the driving transistor DTFT, and a drain electrode thereof is coupled to a reference voltage input terminal configured to input the reference voltage Vref;

[0079] The data writing circuit includes:

[0080] a first data writing transistor N**1**, where a gate electrode of the first data writing transistor N**1** is coupled to the first gate line Gate (N), a drain electrode of the first data writing transistor N**1** is coupled to the data line Data, a source electrode of the first data writing transistor N**1** is coupled to the gate electrode of the driving transistor DTFT; and

[0081] a second data writing transistor P**1**, where a gate electrode of the second data writing transistor P**1** is coupled to the second gate line Gate (P), a drain electrode of the second data writing transistor P**1** is coupled to the gate electrode of the driving transistor DTFT, a drain electrode of the second data writing transistor P**1** is coupled to the data line Data;

[0082] The first data writing transistor N**1** is an NMOS transistor, and the second data writing transistor P**1** is a PMOS transistor.

[0083] In some embodiments of the present disclosure, N**3** is an n-type transistor. In the actual operation, N**3** may also be a p-type transistor, and the type of the reset transistor is not limited herein.

[0084] As shown in FIG. **3**, in some embodiments of the present disclosure, Node **1** is a first node coupled to a gate electrode of the driving transistor DTFT, and Node **2** is a second node coupled to an anode of the organic light-emitting diode OLED.

[0085] As shown in FIG. **4**, when the pixel unit circuit shown in FIG. **3** works, in one frame display time period TF,

[0086] in the resetting phase T**1**, Reset outputs a high level, N**3** is turned on, Node**1** writes in Vref, and Cst is discharged (the potentials at both ends of Cst are Vref, which can quickly clear and discharge Cst), while the potential of Node**2** becomes Vref−Vth, where Vth is the threshold voltage of the DTFT. At this time, Vref adopts a lower potential close to VSS in a silicon-based CMOS (Complementary Metal Oxide Semiconductor) process, so that a difference between the potential Vref−Vth of the anode of the OLED and the potential VSS of the cathode of the OLED is smaller than the light-up voltage of the OLED, so that the display screen is black and does not emit light during the resetting phase. At present, the light-up voltage of both a white light OLED or an OLED device in which each sub-pixel is separately illuminated are larger than 2V, so the voltage value of Vref may be determined according to the process of silicon-based CMOS and the specification of the product. In the resetting phase T**1**, Gate electrode (P) outputs a low voltage (for example, 0V), and Gate electrode (N) outputs a high voltage (for example, 5V), so that both N**1** and P**1** are turned off.

[0087] In the lighting phase T**2**, Gate electrode (P) outputs a high voltage (for example, 5V), Gate electrode (N) outputs a low voltage (for example, 0V), N**1** and P**1** are simultaneously turned on, and the data voltage Vdata on Data is charged to Node**1** and stored into Cst. At this time, DTFT works in the constant-current region, using the source electrode follow characteristic of the NMOS transistor (i.e., DTFT) in the constant current state, the voltage of Node**2** is Vdata−Vth. The voltage value of Vdata is changed to change the voltage of the Node**2**, so as to change the voltage difference between the anode of the OLED and the cathode of the OLED to change the light-emitting luminance of the OLED.

[0088] After the illumination phase T**2** ends, Gate electrode (P) outputs a low voltage (e.g., may be 0V), and Gate electrode (N) outputs a high voltage (e.g., may be 5V), such that both N**1** and P**1** are turned off.

[0089] As shown in FIG. **4**, in the actual operation, the absolute value of the differential pressure of the rising edge of Gate electrode (N) may be set to be equal to the absolute value of the differential pressure of the falling edge of Gate electrode (P) at this time, and the absolute value of the differential pressure of the falling edge Gate electrode (N) is set to be equal to the absolute value of the differential pressure of the rising edge of Gate electrode (P) at this time, so as to counteract the glitch of the voltage of the anode of the OLED when the data writing circuit adopts a single transistor.

[0090] Optionally, in order to counteract the glitch of the pull-up and pull-down of the written data caused by Gate electrode (N) and Gate electrode (P), it is necessary to set the absolute value of the differential pressure of the rising edge of Gate electrode (N) to be equal to the absolute value of the differential pressure at the falling edge of Gate electrode (P) at this time, and the absolute value of the differential pressure at the falling edge of Gate electrode (N) is set to be equal to the absolute value of the differential pressure at the rising edge of Gate electrode (P) at this time.

[0091] Specifically, when the voltage value range of the data voltage changes, the voltage value of the high voltage and the voltage value of the low voltage may also change accordingly.

[0092] The data writing circuit uses dual transistors (P**1** and N**1**) for the purpose of increasing the voltage range of Node**1**, which is equivalent to increasing the voltage range of Node**2**, and finally increasing the adjustable voltage range of the light-emitting of the OLED device. The voltage transmitted through P**1** (P**1** is a PMOS transistor) to Node**1** is at relatively high level. When Vgsp<Vthp, P**1** is in the on-state (Vgsp is the gate electrode-source electrode voltage of P**1**, Vthp is the threshold voltage of P**1**), Vgsp=Vgate (P)−Vdata), Vgate (P) is the voltage output by Gate (P). When Vgsp>Vthp, P**1** is in a non-conducting state, that is, when Vdata<Vgate(P)−Vthp, Vdata cannot be transmitted to

Note**1** through the conductive P**1**. The voltage transmitted through N**1** (N**1** is a NMOS transistor) to Node**1** is at a relatively low level. When Vgsn>Vthn, N**1** is in an on-state (Vgsn is the gate electrode-source electrode voltage of N**1**, Vthn is the threshold voltage of N**1**), Vgsn=Vgate (N)−Vdata, Vgate (N) is the voltage output by Gate electrode (N). When Vgsn<Vthn, N**1** is in a non-conducting state, that is, when Vdata>Vgate(N)−Vthn, Vdata cannot be transmitted to Node**1** through conductive N**1**.

[0093] P**1** and N**1** are transistors with symmetric characteristics of TFT (Thin Film Transistor), that is, Vthp=−Vthn, and the double transistor is adopted as the switch transistor for transmitting the data voltage Vdata to Node**1**, thereby reducing the noise. At the beginning of light-emitting phase T**2**, the rising edge of the voltage outputted by Gate electrode (N) will raise the potential of Node**1**, thereby raising the potential of Node**2**, that is, if the data writing circuit includes only N**1**, at the beginning of the light-emitting phase T**2** (That is, when Vdata is just in the beginning to input, the potential of the anode of the OLED will appear as a rising glitch corresponding to the rising edge of the voltage output by Gate electrode (N). At the end of the light-emitting phase T**2**, the voltage output of Gate electrode (N) is at the falling edge and will pull down the potential of Node**1**, thus lowering the potential of Noed**1**, that is, if the data writing circuit includes only N**1**, when the light-emitting phase T**2** ends, the anode potential of the OLED will appear a falling glitch corresponding to the falling edge of the voltage output by Gate electrode (N). The waveform of the voltage output by Gate electrode (P) is opposite to the waveform of the voltage output by Gate electrode (N). At the beginning of the light-emitting phase T**2**, the voltage output of Gate electrode (P) is declining, and the voltage of the anode of the OLED will appear a falling glitch. At the end of the illuminating phase T**2**, the voltage output of the Gate electrode (P) is at the rising edge, and the voltage of the anode of the OLED will appear a rising glitch. The double transistor (N**1** and P**1**) may counteract the glitch caused when using the single transistor.

[0094] A method of driving the pixel unit circuit hereinabove is further provided in some embodiments of the present disclosure. As shown in FIG. **5**, the method includes:

[0095] Step **1**: in each display period, in a light-emitting phase, under a control of the gate line, enabling by the data writing circuit a connection between the data line and the gate electrode of the driving transistor to be turned on, to enable the driving transistor to work in a constant-current region to drive the light-emitting component to emit light, where a source electrode voltage of the driving transistor varies with a gate electrode potential of the driving transistor.

[0096] According to method of driving the pixel unit circuit in some embodiments of the present disclosure, the potential of the gate electrode of the driving transistor (that is, the potential of the data voltage outputted by the data line) is changed to change the voltage of the source electrode of the driving transistor, and the illuminance of the light-emitting component is adjusted by adjusting the voltage difference between the first end of the light-emitting component and the second end of the light-emitting component, thereby solving the following technical issues in the related art: the driving transistor driving the silicon-based OLED to emit light works in the subthreshold region, so the size of the driving transistor needs to be very large, so it cannot be applied to a high-resolution display product, and the size of the storage capacitor cannot be made large, resulting in a that the luminance of the light-emitting component is unstable due to the inability to stably maintain the data voltage.

[0097] Optionally, each display period further includes a resetting phase. As shown in FIG. **6**, the method further includes: in each display period,

[0098] Step **2**: in the resetting phase, under the control of the gate line, enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off; under a control of a reset terminal, enabling by a resetting circuit a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on;

[0099] Step **3**: in the light-emitting phase, under the control of the reset terminal, enabling by the resetting circuit the connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned off.

[0100] Optionally, each display period further includes a resetting phase prior to the light-emitting phase. The driving method of the pixel unit circuit in some embodiments of the present disclosure may further include a resetting step to control the potentials of two ends of the storage capacitor circuit to be equal in the resetting phase, thereby quickly discharging the storage capacitor circuit, ensuring that the image of the previous frame does not affect the image of the next frame. By adjusting the voltage value of reference voltage input terminal, the difference between the potential of the first end of the light-emitting component and the potential of the second end of the light-emitting component in the resetting phase may be smaller than the light-up voltage of the light-emitting component, so that the light-emitting components do not emit light during the resetting phase, and the dynamic image sticking may not occur in the dynamic picture.

[0101] Specifically, the reference voltage input terminal is configured to input a reference voltage;

[0102] Optionally, a difference between the reference voltage and a threshold voltage of the driving transistor is smaller than a sum value of a low level input by the low-level input terminal and a light-up voltage of the light-emitting component, so as to reduce the voltage difference between the first end and the second end of the light-emitting component in the resetting phase, so that the light-emitting component does not illuminate, ensuring that dynamic image sticking does not occur in the dynamic picture.

[0103] Specifically, the gate line includes a first gate line and a second gate line, and the data writing circuit includes: a first data writing transistor, where a gate electrode of the first data writing transistor is coupled to the first gate line; a second data writing transistor, where a gate electrode of the second data writing transistor is coupled to the second gate line; the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor; and when an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor, as shown in FIG. **7**, the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off in the resetting phase under the control of the gate line, further includes:

[0104] Step **21**: in the resetting phase, outputting a first gate driving signal by the first gate line, and outputting a second gate driving signal by the second gate line, where a potential of the first gate driving signal is a low voltage and a potential of the second gate driving signal is a high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off;

[0105] as shown in FIG. **7**, the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned on in the light-emitting phase under the control of the gate line, includes:

[0106] Step **31**: in the light-emitting phase, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the high voltage and the potential of the second gate driving signal is the low voltage, to enable the first data writing transistor to be turned on and enable the second data writing transistor to be turned on;

[0107] as shown in FIG. **7**, the method further includes:

[0108] Step **41**: after the light-emitting phase ends in each display period, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, where the potential of the first gate driving signal is the low voltage and the potential of the second gate driving signal is the high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off.

[0109] A pixel circuit is further provided in some embodiments of the present disclosure. As shown in FIG. **8**, the pixel circuit includes: a plurality of rows of gate lines GLs, a plurality of columns of data lines DLs and a plurality of pixel unit circuits arranged in an array form hereinabove, where

[0110] the pixel unit circuits in the same row are coupled to the gate line GL in the same row, and

[0111] the pixel unit circuits in the same column are coupled to the data line DL in the same column.

[0112] As shown in FIG. **9**, in some embodiments of the present disclosure, the gate lines include first gate lines GL**1***s* and second gate lines GL**2***s*, and the pixel unit circuits in the same row are each coupled to the first gate line GL**1** in the same row and the second gate line GL**2** in the same row.

[0113] It should be noted that "coupled to" in the embodiments of the present disclosure include direct connections and indirect connections implemented via other elements.

[0114] A display device is further provided in some embodiments of the present disclosure. As shown in FIG. **10**, the display device includes: a plurality of rows of gate lines GLs, a plurality of columns of data lines DLs and a plurality of pixel unit circuits arranged in an array form hereinabove, where

[0115] the pixel unit circuits in the same row are coupled to the gate line GL in the same row, and

[0116] the pixel unit circuits in the same column are coupled to the data line DL in the same column.

[0117] Optionally, the display device further includes a silicon substrate, where the plurality of rows of gate lines, the plurality of columns of data lines and the plurality of pixel unit circuits are arranged on the silicon substrate.

[0118] The above are merely some embodiments of the present disclosure. A person skilled in the art may make further modifications and improvements without departing from the principle of the present disclosure, and these modifications and improvements shall also fall within the scope of the present disclosure.

1. A pixel unit circuit, comprising a light-emitting component, a driving transistor, a data writing circuit and a storage capacitor circuit, wherein

a drain electrode of the driving transistor is coupled to a high-level input terminal, a source electrode of the driving transistor is coupled to a first end of the light-emitting component, the driving transistor is an n-type transistor;

the data writing circuit is coupled to a data line, a gate line and a gate electrode of the driving transistor, and configured to, under a control of the gate line, enable a connection between the data line and the gate electrode of the driving transistor to be turned on or off;

a first end of the storage capacitor circuit is coupled to the gate electrode of the driving transistor, and a second end of the storage capacitor circuit is coupled to a reference voltage input terminal;

a second end of the light-emitting component is coupled to a low-level input terminal;

a source electrode voltage of the driving transistor varies with a gate electrode potential of the driving transistor.

2. The pixel unit circuit according to claim **1**, further comprising a reset circuit, wherein

the reset circuit is coupled to a reset terminal, the reference voltage input terminal and the gate electrode of the driving transistor, and configured to, under a control of the reset terminal, enable a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on or off.

3. The pixel unit circuit according to claim **2**, wherein the reset circuit comprises a reset transistor, a gate electrode of the reset transistor is coupled to the reset terminal, a first electrode of the reset transistor is coupled to the gate electrode of the driving transistor, a second electrode of the reset transistor is coupled to the reference voltage input terminal, the reset transistor is an n-type transistor or a p-type transistor.

4. The pixel unit circuit according to claim **1**, wherein the gate line comprises a first gate line and a second gate line;

the data writing circuit comprises:

a first data writing transistor, wherein a gate electrode of the first data writing transistor is coupled to the first gate line, a first electrode of the first data writing transistor is coupled to the data line, a second electrode of the first data writing transistor is coupled to the gate electrode of the driving transistor; and

a second data writing transistor, wherein a gate electrode of the second data writing transistor is coupled to the second gate line, a first electrode of the second data writing transistor is coupled to the gate electrode of the driving transistor, a second electrode of the second data writing transistor is coupled to the data line;

the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor.

5. The pixel unit circuit according to claim **2**, wherein the gate line comprises a first gate line and a second gate line;

the data writing circuit comprises:

a first data writing transistor, wherein a gate electrode of the first data writing transistor is coupled to the first gate line, a first electrode of the first data writing transistor is coupled to the data line, a second electrode of the first data writing transistor is coupled to the gate electrode of the driving transistor; and

a second data writing transistor, wherein a gate electrode of the second data writing transistor is coupled to the second gate line, a first electrode of the second data writing transistor is coupled to the gate electrode of the driving transistor, a second electrode of the second data writing transistor is coupled to the data line;

the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor.

6. The pixel unit circuit according to claim **3**, wherein the gate line comprises a first gate line and a second gate line;

the data writing circuit comprises:

a first data writing transistor, wherein a gate electrode of the first data writing transistor is coupled to the first gate line, a first electrode of the first data writing transistor is coupled to the data line, a second electrode of the first data writing transistor is coupled to the gate electrode of the driving transistor; and

a second data writing transistor, wherein a gate electrode of the second data writing transistor is coupled to the second gate line, a first electrode of the second data writing transistor is coupled to the gate electrode of the driving transistor, a second electrode of the second data writing transistor is coupled to the data line;

the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor.

7. The pixel unit circuit according to claim **4**, wherein an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor.

8. The pixel unit circuit according to claim **1**, wherein the storage capacitor circuit comprises a storage capacitor, wherein a first end of the storage capacitor is coupled to the gate electrode of the driving transistor and a second end of the storage capacitor is coupled to the reference voltage input terminal.

9. The pixel unit circuit according to claim **1**, wherein the light-emitting component comprises an organic light-emitting diode, the first end of the light-emitting component is an anode of the organic light-emitting diode, and the second end of the light-emitting component is a cathode of the organic light-emitting diode.

10. A method of driving the pixel unit circuit according to claim **1**, comprising: in each display period,

in a light-emitting phase, under a control of the gate line, enabling by the data writing circuit a connection between the data line and the gate electrode of the driving transistor to be turned on, to enable the driving transistor to work in a constant-current region to drive the light-emitting component to emit light, wherein a source electrode voltage of the driving transistor varies with a gate electrode potential of the driving transistor.

11. The method according to claim **10**, wherein each display period further comprises a resetting phase, the method further comprises:

in the resetting phase, under the control of the gate line, enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off; under a control of a reset terminal, enabling by a resetting circuit a connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned on;

in the light-emitting phase, under the control of the reset terminal, enabling by the resetting circuit the connection between the gate electrode of the driving transistor and the reference voltage input terminal to be turned off.

12. The method according to claim **11**, wherein the reference voltage input terminal is configured to input a reference voltage;

a difference between the reference voltage and a threshold voltage of the driving transistor is smaller than a sum value of a low level input by the low-level input terminal and a light-up voltage of the light-emitting component.

13. The method according to claim **11**, wherein the gate line comprises a first gate line and a second gate line, and the data writing circuit comprises:

a first data writing transistor, wherein a gate electrode of the first data writing transistor is coupled to the first gate line;

a second data writing transistor, wherein a gate electrode of the second data writing transistor is coupled to the second gate line;

the first data writing transistor is an n-type transistor, and the second data writing transistor is a p-type transistor; and

when an absolute value of a threshold voltage of the first data writing transistor is equal to an absolute value of a threshold voltage of the second data writing transistor, the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned off in the resetting phase under the control of the gate line, further comprises:

outputting a first gate driving signal by the first gate line, and outputting a second gate driving signal by the second gate line, wherein a potential of the first gate driving signal is a low voltage and a potential of the second gate driving signal is a high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off;

the enabling by the data writing circuit the connection between the data line and the gate electrode of the driving transistor to be turned on in the light-emitting phase under the control of the gate line, comprises:

outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, wherein the potential of the first gate driving signal is the high voltage and the potential of the second gate driving signal is the low voltage, to enable the first data writing transistor to be turned on and enable the second data writing transistor to be turned on;

the method further comprises: after the light-emitting phase ends in each display period, outputting the first gate driving signal by the first gate line, and outputting the second gate driving signal by the second gate line, wherein the potential of the first gate driving signal is

the low voltage and the potential of the second gate driving signal is the high voltage, to enable the first data writing transistor and the second data writing transistor to be turned off, and to enable the connection between the data line and the gate electrode of the driving transistor to be turned off.

14. A pixel circuit, comprising a plurality of rows of gate lines, a plurality of columns of data lines and a plurality of pixel unit circuits arranged in an array form according to claim **1**, wherein

the pixel unit circuits in the same row are coupled to the gate line in the same row, and the pixel unit circuits in the same column are coupled to the data line in the same column.

15. The pixel circuit according to claim **14**, wherein the gate lines comprise first gate lines and second gate lines, and the pixel unit circuits in the same row are each coupled to the first gate line in the same row and the second gate line in the same row.

16. A display device, comprising a plurality of rows of gate lines, a plurality of columns of data lines and a plurality of pixel unit circuits arranged in an array form according to claim **1**, wherein

the pixel unit circuits in the same row are coupled to the gate line in the same row, and the pixel unit circuits in the same column are coupled to the data line in the same column.

17. The display device according to claim **16**, further comprising a silicon substrate, wherein the plurality of rows of gate lines, the plurality of columns of data lines and the plurality of pixel unit circuits are arranged on the silicon substrate.

18. The display device according to claim **16**, wherein the gate lines comprise first gate lines and second gate lines, and the pixel unit circuits in the same row are each coupled to the first gate line in the same row and the second gate line in the same row.

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