(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2006 (29.06.2006)

PCT

(10) International Publication Number
WO 2006/068642 A1

(51) International Patent Classification:
H01L 23/495 (2006.01) *H01L 23/31* (2006.01)

(21) International Application Number:
PCT/US2004/043076

(22) International Filing Date:
20 December 2004 (20.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.** [US/US]; 5005 E. McDowell Road - A700, Phoenix, AZ 85008 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **CARNEY, Francis J.** [US/US]; 549 East Palo Verde, Gilbert, AZ 85296 (US). **SEDDON, Michael J.** [US/US]; 2760 E. Milky Way, Gilbert, AZ 85296 (US).

(74) Agents: **JACKSON, Kevin B.** et al.; Patent Administration - A700, P.O. Box 62890, Phoenix, AZ 85082-2890 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

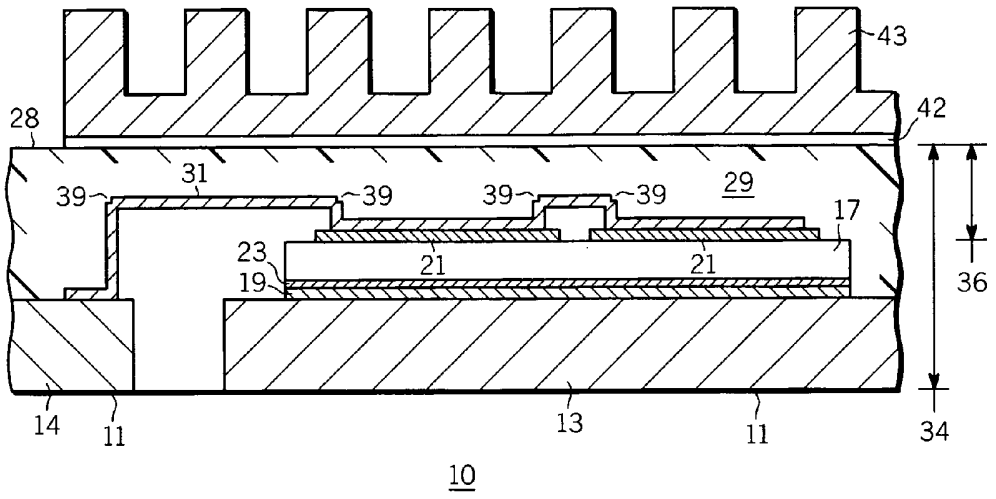
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** SEMICONDUCTOR PACKAGE STRUCTURE HAVING ENHANCED THERMAL DISSIPATION CHARACTERISTICS



(57) **Abstract:** In one embodiment, a packaged semiconductor device having enhanced thermal dissipation characteristics includes a lead frame structure and a semiconductor chip having a major current carrying or heat generating electrode. The semiconductor chip is oriented so that the major current carrying electrode faces the top of the package or away from the next level of assembly. The packaged semiconductor device further includes a non-planar, stepped or undulating attachment structure coupling the current carrying electrode to the lead frame. A high thermal conductivity mold compound and thin package profile further enhance thermal dissipation.

WO 2006/068642 A1

SEMICONDUCTOR PACKAGE STRUCTURE HAVING ENHANCED THERMAL DISSIPATION CHARACTERISTICS

Background of the Invention

[0001] The present invention relates in general to semiconductor device packaging and, more particularly, to semiconductor components housed in packages having improved heat transfer characteristics.

[0002] There is a continuing demand for electronic systems with a higher functionality and smaller physical size. With this demand, there are several challenges that face electronic component designers and manufacturers. Such challenges include the management of heat generated by power semiconductor devices, which are typically arranged closely together or next to sensitive logic circuits on electronic circuit boards.

[0003] In current configurations, plastic encapsulated devices are commonly used. One problem with plastic packages is that the thermal conductivity out of a package is often limited by the plastic molding material. As a result, the majority of the heat generated by the semiconductor device is transferred through the lower part of the package next to the printed circuit board. Because the printed circuit boards are becoming more densely populated, the boards cannot properly dissipate or handle large amounts of heat. When this happens, the boards can warp, which can cause damage to both the board and the components on the board. In addition, the heat itself can damage other components on the printed circuit board or the materials that make up the board.

[0004] In view of this problem, the semiconductor industry is migrating to packages that have the capability of transferring heat out through the top of the package

instead of through the printed circuit boards. Such packages may also include a heat sink attached to the top of the package to further aid in heat transfer.

[0005] One such package is the DirectFET™ package shown in a Board Mounting Application Note AN-1035 entitled "DirectFET™ Technology" dated January 2002 by International Rectifier Corporation. In this design, plastic mold compound is eliminated altogether because of its perceived poor heat transfer characteristics.

[0006] This design has several disadvantages. First, because the package does not use mold compound, the semiconductor is left unprotected making it susceptible to damage or contamination. Also, this design utilizes non-standard manufacturing techniques, which adds to manufacturing cycle time and increases manufacturing costs. In addition, in certain applications this design places the main current carrying electrode (e.g., source electrode) in a down orientation or next to the printed circuit board, which lessens heat transfer capability. In other applications, this design places the main current carrying electrode in an up orientation or away from the printed circuit board, but in direct contact with an unpassivated heat sink, which is a safety concern under operation.

[0007] Accordingly, a need exists for semiconductor packages that have enhanced thermal dissipation characteristics without detrimentally impacting device reliability, safety, manufacturing cycle time, and cost.

Brief Description of the Drawings

[0008] FIG. 1 illustrates an enlarged cross-sectional view of a package structure according to an embodiment of the present invention;

[0009] FIG. 2 illustrates an enlarged cross-sectional view of a package structure according to a second embodiment of the present invention;

[0010] FIG. 3 illustrates an enlarged cross-sectional view of a package structure according to a third embodiment of the present invention;

[0011] FIG. 4 illustrates an enlarged cross-sectional view of a package structure according to a fourth embodiment of the present invention;

[0012] FIG. 5 illustrates an enlarged cross-sectional view of a package structure according to a fifth embodiment of the present invention;

[0013] FIG. 6 illustrates an embodiment of an interconnect scheme for the package structures of FIGS. 1 and 4;

[0014] FIG. 7 illustrates another embodiment of an interconnect scheme for the package structures of FIGS. 1 and 4;

[0015] FIG. 8 illustrates an embodiment of an interconnect scheme for the package structures of FIGS. 2 and 3; and

[0016] FIG. 9 illustrates another embodiment of an interconnect scheme for the package structures of FIGS. 2 and 3.

Detailed Description of the Drawings

[0017] For ease of understanding, elements in the drawing figures are not necessarily drawn to scale, and like element numbers are used where appropriate throughout the various figures. Although the invention is described using a QFN/DFN embodiment, those skilled in the art will recognize that the present invention is applicable to other types of packages as well, particularly those where enhanced heat transfer characteristics are important.

[0018] FIG. 1 shows an enlarged cross-sectional view of a packaged semiconductor structure, QFN/DFN package, leadless packaged device or package 10 having enhanced thermal dissipation or heat transfer characteristics in accordance with the present invention. Packaged device 10 includes a conductive substrate or lead frame 11, which includes a flag, plate, or die attach portion 13 and a lead, terminal, connection, or pad portion 14. Lead frame 11 comprises, for example, copper, a copper alloy (e.g., TOMAC 4, TAMAC 5, 2ZFROFC, or CDA194), a copper plated iron/nickel alloy (e.g., copper plated Alloy 42), plated aluminum, plated plastic, or the like. Plated materials include copper, silver, multi-layer plating such nickel-palladium and gold. Flag portion 13 and pad portion 14 are used to connect or couple to bonding pads on a next level of assembly such as a printed circuit board.

[0019] Package 10 further includes an electronic chip or semiconductor device 17, which is attached to flag 13 using a die attach layer 19. Semiconductor device 17 comprises, for example, a power MOSFET device, a bipolar transistor, an insulated gate bipolar transistor, a thyristor, a diode, an analog or digital integrated circuit, a sensor, a passive component, or other electronic device. In an exemplary embodiment, semiconductor device 17 comprises a power MOSFET

device including a source, an up-source or major current carrying electrode 21, a drain, down-drain or current carrying electrode 23, and a gate or control electrode 26 (shown in FIG. 6). Source electrode 21 comprises, for example, a solderable top metal, aluminum, an aluminum alloy, or the like. Drain electrode 23 typically comprises a solderable metal layer or layers such as TiNiAg, CrNiAu, or the like. In accordance with the present invention, semiconductor chip 17 is in a major current carrying electrode or source electrode "up" configuration. That is, the major heat generating electrode (e.g., electrode 21) of semiconductor chip 17 is oriented away from or opposite from the side of package 10 that will be attached to the next level assembly. This orientation promotes heat transfer out of top surface 28 of package 10, instead of through the next level of assembly or through the chip itself.

[0020] An attachment structure, undulating, stepped, or non-planar attachment structure or conductive clip or strap 31 is coupled to source electrodes 21 and pad portion 14 to provide an electrical path between semiconductor chip 17 and pad portion 14. Clip 31 comprises, for example, rigid copper or a copper alloy and is optionally plated with silver for either solder attachment or conductive epoxy attachment. In the embodiment shown and in accordance with the present invention, clip 31 preferably is undulating, stepped or non-planar so that portions of clip 31 are closer to top surface 28 of package 10 and not in contact with semiconductor chip 17. This provides a reduced thermal resistance path for improved conductive heat transfer away from semiconductor chip 34 compared to a flat or planar clip. Preferably, at least about 50% of the surface area of clip 31 is in contact with electrode 21, and the balance of the surface area is that portion of clip 31 undulating or stepped away from electrode 21. Preferably, clip 31 has at

least 2 steps. Optional attachment or interconnect schemes for control electrode 26 are shown and described in conjunction with FIGS. 6 and 7.

[0021] An encapsulating or passivating layer 29 is formed over lead frame 11, semiconductor chip 17, and at least portions of clip 31 using a single cavity or overmolding process. In accordance with the present invention, encapsulating layer 29 comprises a high thermal conductivity mold compound. Preferably, encapsulating layer 29 comprises a mold compound having a thermal conductivity greater than about 3.0 Watts/MK. Suitable high conductivity mold compounds are available from Sumitomo Plastics America of Santa Clara, California (e.g., EME A700 series) and Hitachi Chemical of Santa Clara, California (e.g., a CEL 9000 series mold compound).

[0022] Preferably, package 10 has an overall height 34 less than about 1.10 millimeters. In a more preferred embodiment, height 34 is less than about 0.80 millimeters. Additionally, the thickness of encapsulating layer 29 above semiconductor chip 17 is less than about 0.53 millimeters. These dimensions together with undulating clip 31, the orientation of major current carrying electrode 21, and the high conductivity mold compound provide for an enhanced heat transfer effect. In particular, thermal studies evaluating a comparable sized package 10 to a DirectFET™ product showed that a package 10 according to the present invention assembled with a mold compound having a thermal conductivity greater that or equal to about 3.0 Watts/mK, and a height 34 of less than about 0.80 millimeters had an equal or better thermal resistance (junction to top of package) characteristic.

[0023] Undulating clip 31 is shown with one or more optional mold lock features or notches 39, which are used to provide better adhesion between encapsulating layer 29 and

clip 31. More or fewer notches 39 may be used. Additionally, package 10 includes an optional heat sink device 43, which is attached to package 10 with, for example, a high conductivity epoxy material 42, such as a CEL9750 HFLO(AL3) or a CEL9210 HFLO(AL2) epoxy available from Hitachi Chemical, or an EMF 760a epoxy available from Sumitomo Plastics America. It is understood that heat sink 43 is an option for all package embodiment described including those shown in FIGS. 2-5 hereinafter. In applications where safety is a concern, heat sink 43 is optionally coated with an insulating material such as a thermal grease.

[0024] FIG. 2 shows an enlarged cross-sectional view of a packaged semiconductor structure, QFN/DFN package, leadless packaged device, or package 100 according to a second embodiment of the present invention. Package 100 is similar to package 10 except that instead of undulating clip 31, an undulating or non-planar attachment structure or ribbon bond(s) 231 is used to couple major current carrying electrode 21 semiconductor chip 17 to pad portion 14.

[0025] Ribbon bond 231 refers to a flexible rectangular shaped conductor, wherein a width 51 of ribbon bond 231 (shown in FIG. 7) is greater than a thickness 52 of ribbon bond 231. Suitable materials for ribbon bond 231 include gold, aluminum, silver, palladium, copper or the like. Attachment of ribbon bond 231 typically includes ultrasonic wedge bonding end 232 to source electrodes 21, and wedge bonding end 233 to pad portion 14. In one embodiment, ribbon bond 231 is formed having a thickness of about twenty five microns and a width of about seventy five microns. Alternatively, ribbon bond 231 is typically formed to a thickness 52 of about six microns to fifty microns and a width 52 of about fifty microns to fifteen hundred microns wide. One advantage of the embodiments of FIGS. 1 and 2 is

that the top side of packages 10 and 100 are electrically insulated so that the safety issues associated with prior art structure are avoided.

[0026] FIG. 3 shows an enlarged cross-sectional view of a packaged semiconductor structure, QFN/DFN package, leadless packaged device, or package 110 according to a third embodiment of the present invention. Package 110 is similar to package 10 except that in package 110, an encapsulating layer 129 covers only a portion of undulating clip 31. That is, in package 110, portions 310 of clip 31 are left exposed, which further enhances the heat transfer characteristics of the package while semiconductor chip 17 is still covered or passivated by encapsulating layer 129. In this embodiment, encapsulating layer 129 preferably comprises materials similar to encapsulating layer 29.

[0027] FIG. 4 shows an enlarged cross-sectional view of a packaged semiconductor structure, QFN/DFN package, leadless packaged device, or package 200 according to another embodiment of the present invention. Package 200 is similar to package 100 except that in package 200, an encapsulating layer 229 covers only a portion of attachment structure or ribbon bond 231. That is, in package 200, portions 331 of ribbon bond 231 are left exposed, which further enhances the heat transfer characteristics of the package while semiconductor chip 17 is still covered or passivated by encapsulating layer 129. In this embodiment, encapsulating layer 229 preferably comprises materials similar to encapsulating layer 29.

[0028] In a preferred method for forming packages 110 and 200, after attachment structures 31 and 231 are formed, the assemblies are placed in a molding apparatus so that portions 310 and 331 contact or adjoin a surface of the mold cavity. The surface of the mold cavity acts as a mask to prevent encapsulating material 129 and 229 from covering

portions 310 and 331.

[0029] FIG. 5 shows an enlarged cross-sectional view of a packaged semiconductor structure, QFN/DFN package, leadless packaged device, or package 210 according to a further embodiment of the present invention. Package 210 is similar to package 100 except that in package 210, an undulating or non-planar attachment structure or ribbon bond 431 is used having an omega or substantially omega-like shape. That is ribbon bond 431 includes base portions 432 and upper portions 433 above semiconductor chip 17, wherein the base portions 432 have a width less than the width of upper portions 433. Omega shaped ribbon bond 431 provides an undulating attachment structure that has more conductive surface area, which provides for a package with enhanced heat transfer characteristics. In an alternative embodiment, portions of omega shaped ribbon bond 431 are exposed similar to the packages shown in FIGS. 3 and 4.

[0030] FIGS. 6-9 show embodiments of different attachment structure schemes for use with the present invention prior to an encapsulation step. FIG. 6 shows lead frame 11 and semiconductor chip 17 of FIG. 1 with the addition of control electrode attachment structure 61 coupling a control electrode 26 (as referenced in paragraph [0019]) on semiconductor chip 17 to pad portion 114. In this embodiment, control electrode attachment structure 61 comprises a ribbon bond. In general, an area of control electrode 26 is selected to be approximately three times the width by three times the thickness of the ribbon bond. One advantage to ribbon bond 61 is that compared to contact areas required for wire bonds, ribbon bond area can be smaller without sacrificing manufacturability, reliability or strength.

[0031] FIG. 7 shows lead frame 11 and semiconductor chip 17 of FIG. 2 with the addition of ribbon bond 61 as

described in conjunction with FIG. 6. FIG. 7 further shows a plurality of or multiple ribbon bonds 231, and includes width 51 as referenced in paragraph [0025].

[0032] FIG. 8 shows lead frame 11 and semiconductor chip 17 of FIG. 1 with the addition of wire bond 71, which is an attachment structure coupling a control electrode 226 on semiconductor chip 17 to a pad portion 114 of lead frame 11. In this embodiment, control electrode 226 comprises a metal suitable for wire bonding such as aluminum or an aluminum alloy. Wire bond 71 is formed using conventional wire bonding techniques, and comprises for example, aluminum or gold. In a preferred embodiment, wire bond 71 has a loop height that is less than the height of undulating clip 31 so that wire bond 71 is not exposed in the embodiment of FIG. 3.

[0033] FIG. 9 shows lead frame 11 and semiconductor chip 17 of FIG. 2 with the addition of wire bond 71 coupling control electrode 226 on semiconductor chip 17 to pad portion 114 of lead frame 11. In this embodiment, control electrode 226 comprises a metal suitable for wire bonding such as aluminum or an aluminum alloy. Wire bond 71 is formed using conventional wire bonding techniques, and comprises for example, aluminum or gold. In a preferred embodiment, wire bond 71 has a loop height that is less than the height of ribbon bond 231 so that wire bond 71 is not exposed in the embodiment of FIG. 4.

[0034] By now it should be appreciated that there has been provided a semiconductor package structure that has enhanced thermal dissipation or heat transfer characteristics. The package includes an electronic chip that is orientated so that the heat generating or major current carrying electrode is away from the side of the package intended to attach to a next level of assembly. This provides an improved thermal path through the top of

the package. The package further includes an undulating attachment structure that places a portion of the attachment structure closer to the top of the package thereby further reducing the thermal resistance path. In addition, the package incorporates a high thermal conductivity mold compound (greater than about 3.0 W/mK) and a thin profile (less than about 1.10 millimeters) to further enhance thermal dissipation. In an alternative embodiment, a portion of the undulating attachment structure is exposed to further enhance thermal dissipation. In an additional embodiment, the undulating attachment structure has an omega-like shape to provide more conductive surface area for heat transfer. In a still further embodiment, a heat sink device is added to the top of the package to further enhance thermal dissipation.

CLAIMS

What is claimed is:

1. A semiconductor package comprising:

a conductive substrate having a flag portion and a pad portion;

an electronic chip coupled to the flag portion, wherein the electronic chip includes a major current carrying electrode on a surface opposite the flag portion;

an attachment structure coupling the major current carrying electrode to the pad portion; and

an encapsulating layer having a thermal conductivity greater than or equal to about 3.0 Watts/mK, wherein the encapsulating layer covers the electronic chip and at least a portion of the undulating attachment structure.

2. The package of claim 1 wherein the attachment structure comprises a stepped clip.

3. The package of claim 2 wherein a portion of the stepped clip is exposed.

4. The package of claim 2 wherein the stepped clip has at least two steps.

5. The package of claim 1 wherein the attachment structure comprises a undulating ribbon bond.

6. The package of claim 5 wherein a portion of the undulating ribbon bond is exposed.

7. The package of claim 5 wherein the undulating ribbon bond has a substantially omega-like shape.

8. The package of claim 1 wherein the encapsulating layer covers the attachment structure.

9. The package of claim 1 wherein the package has height less than about 1.10 millimeters.

10. The package of claim 1 wherein the electronic chip further includes a control electrode, and wherein the conductive substrate further includes a second pad portion, and wherein a second attachment structure couples the control electrode to the second pad portion.

11. The package of claim 9 wherein the second attachment structure includes a ribbon bond.

12. The package of claim 9 wherein the second attachment structure includes a wire bond.

13. The package of claim 1 wherein the attachment structure includes a mold lock.

14. The package of claim 1 further comprising a heat sink attached to an upper surface of the semiconductor package.

15. A leadless semiconductor package having enhanced thermal dissipation comprising:

a lead frame including a terminal portion;

a semiconductor device having a first electrode on a surface;

a stepped attachment structure coupled to the first electrode and the terminal portion; and

a passivating layer covering the semiconductor device and at least a portion of the stepped attachment structure.

16. The leadless semiconductor package of claim 15 wherein the stepped attachment structure comprises an stepped clip having at least two steps.

17. The leadless semiconductor package of claim 15 wherein the stepped attachment structure comprises an undulating ribbon bond.

18. The leadless semiconductor package of claim 15 wherein a portion of the stepped attachment structure is exposed.

19. The leadless semiconductor package of claim 15 wherein the stepped attachment structure has a substantially omega-like shape.

20. The leadless semiconductor package of claim 15 wherein the passivating layer comprises a material having a thermal conductivity greater than or equal to about 3.0 Watts/mK.

21. A electronic package comprising:

a semiconductor die having a major current carrying electrode;

a stepped attachment structure coupled to the major current carrying electrode; and

an encapsulating layer covering at least a portion of the semiconductor die while leaving a portion of the stepped attachment structure exposed.

22. The electronic package of claim 21 wherein the stepped attachment structure comprises a stepped clip.

23. The electronic package of claim 21 wherein the

stepped attachment structure comprises an undulating ribbon bond.

24. The electronic package of claim 21 wherein the semiconductor die further includes a control electrode and a second attachment structure attached thereto.

25. The electronic package of claim 24 wherein the second attachment structure comprises a ribbon bond.

26. The electronic package of claim 24 wherein the second attachment structure comprises a wire bond.

27. The electronic package of claim 21 wherein the encapsulating layer comprises a material having a thermal conductivity greater than or equal to about 3.0 Watts/mK.

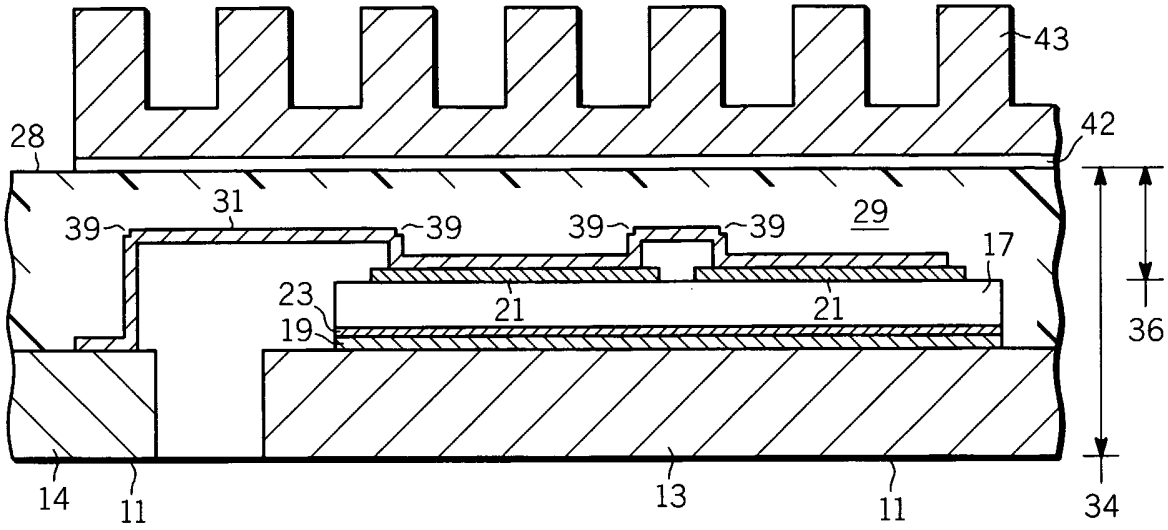

43
42
28
31
39
39
39
39
29
17
23
21
21
19
36
14
11
13
11
34
10

FIG. 1

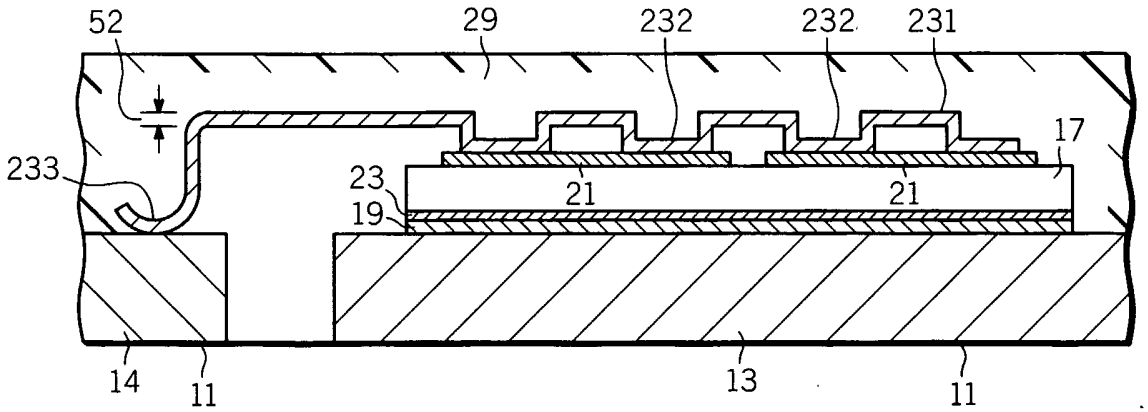

100
52
29
232
232
231
17
233
23
21
21
19
14
11
13
11

FIG. 2

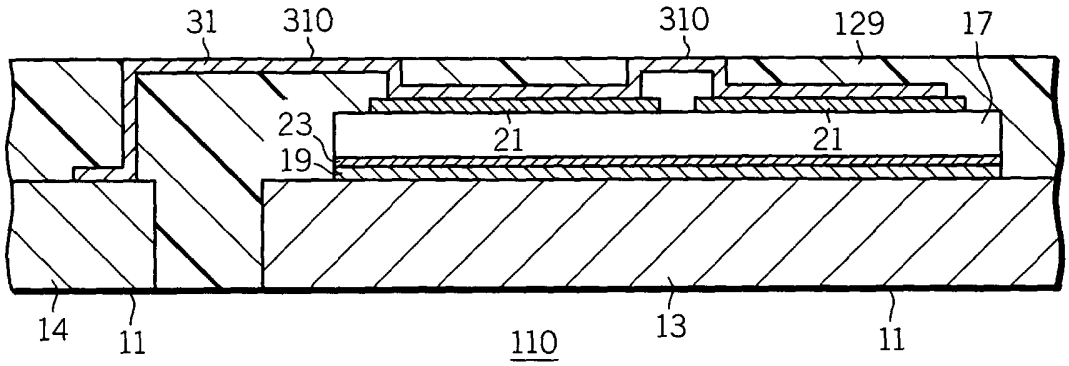


FIG. 3

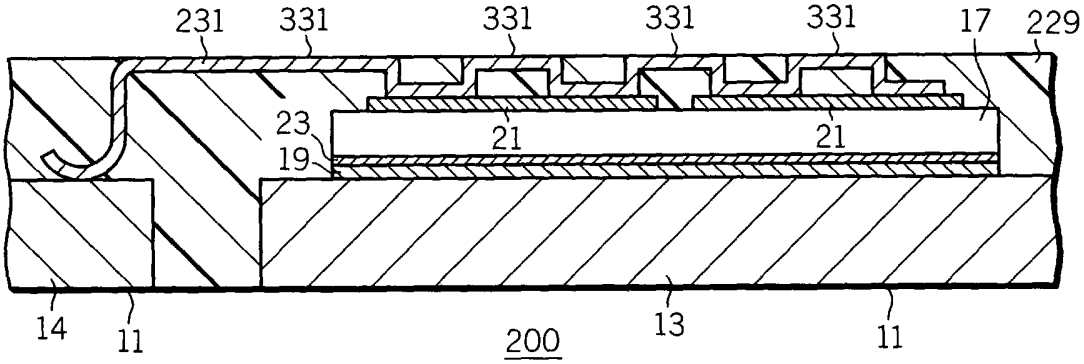


FIG. 4

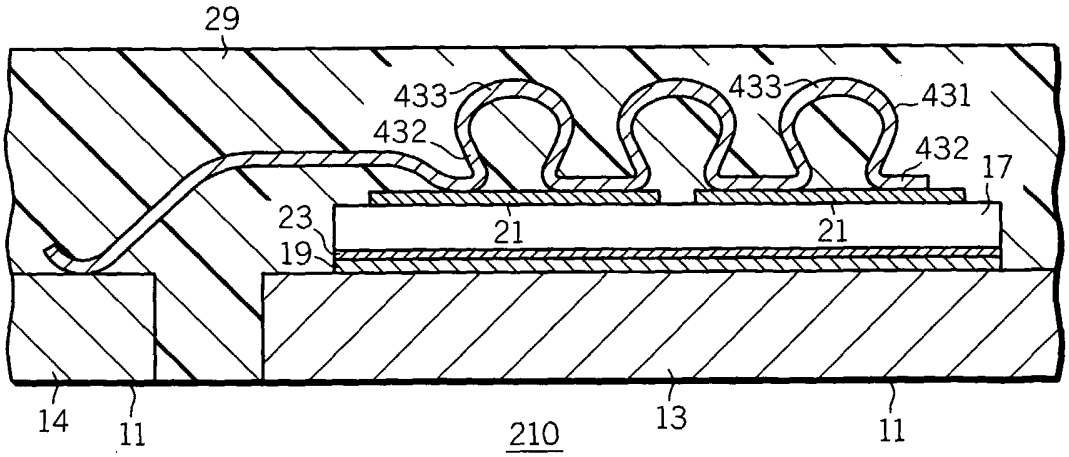


FIG. 5

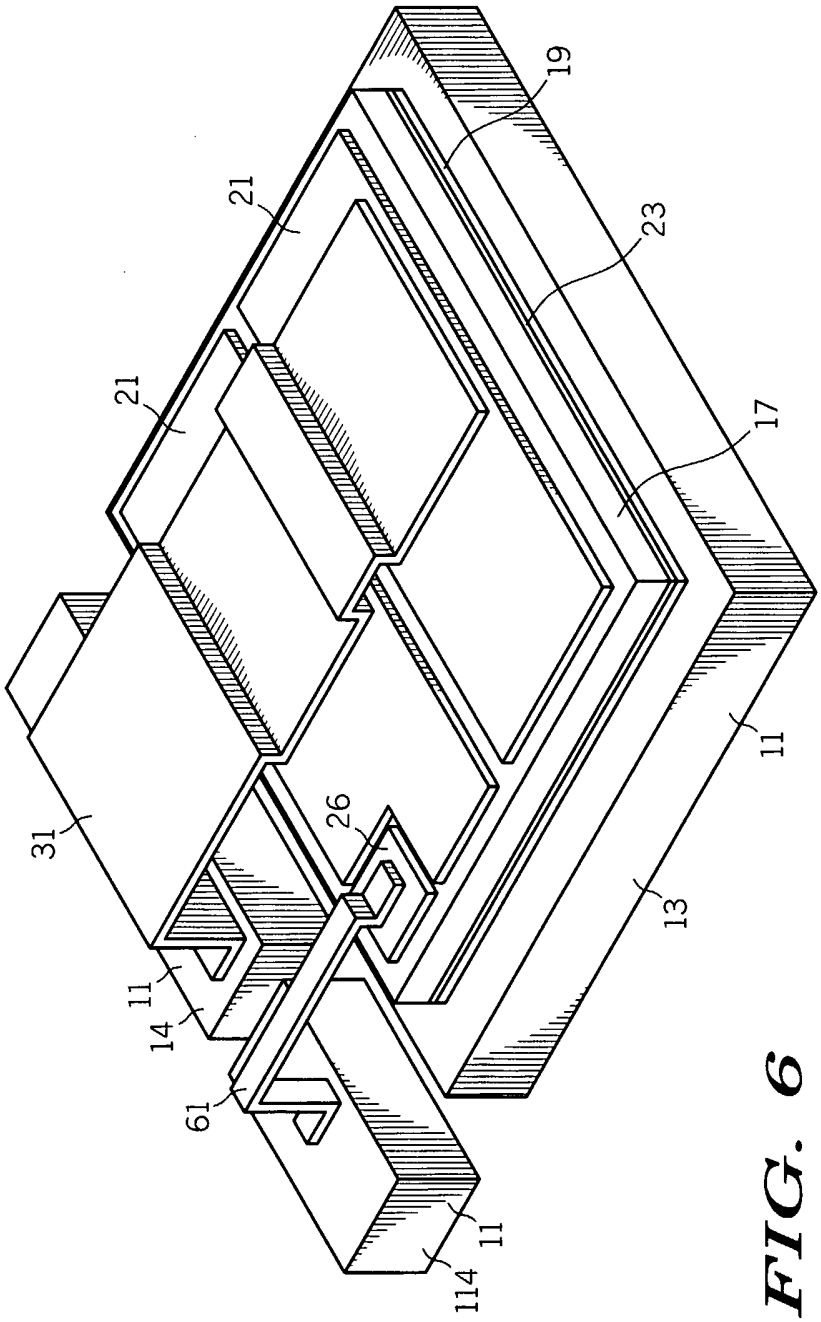


FIG. 6

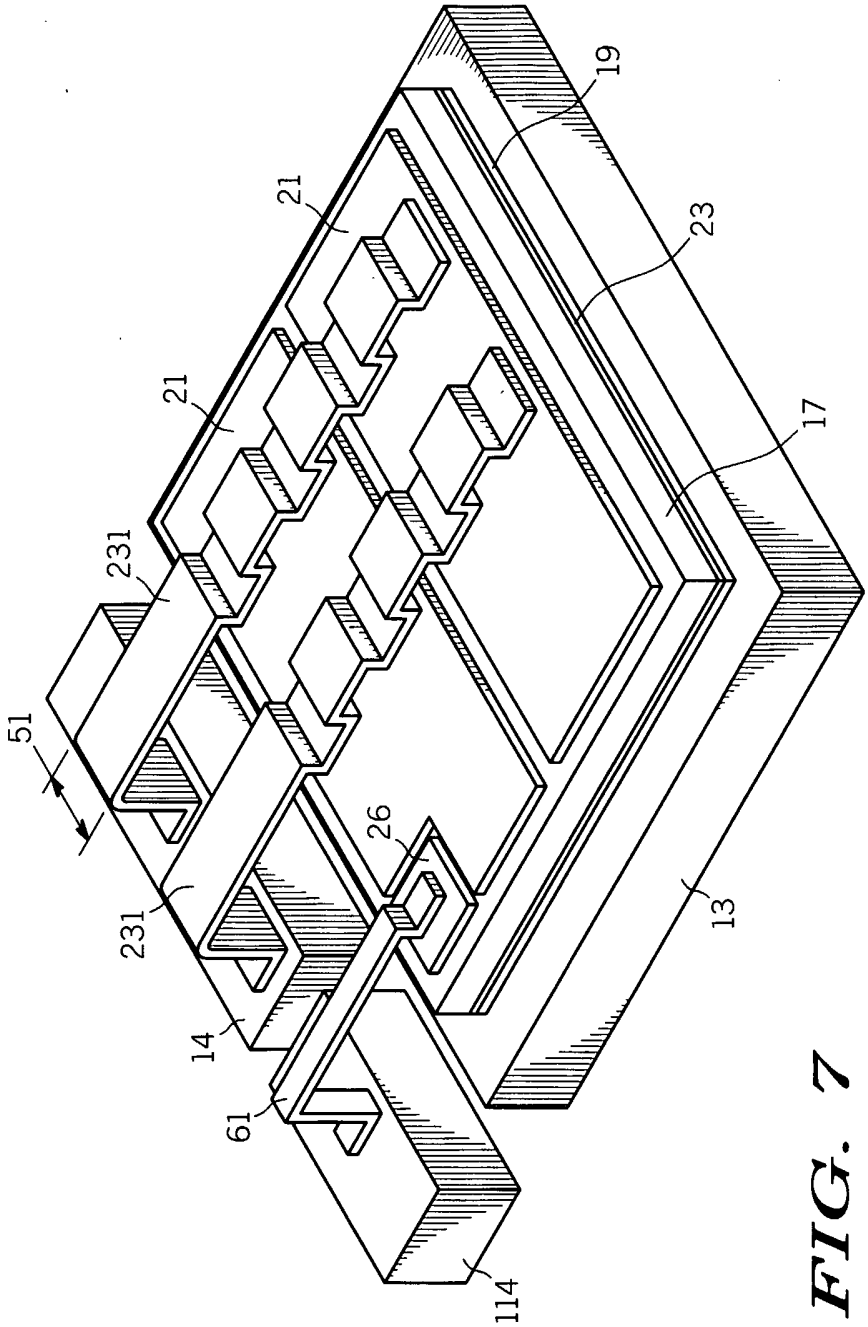


FIG. 7

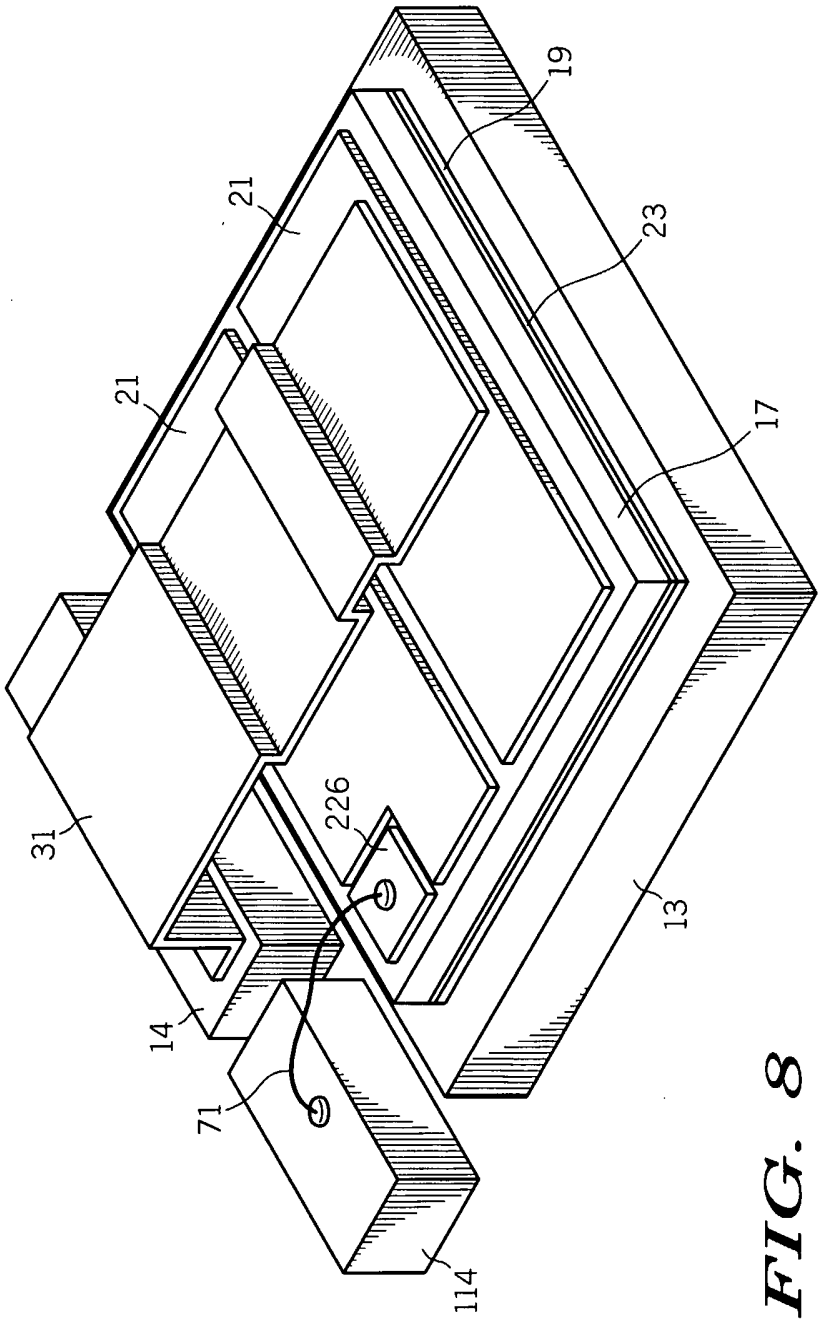


FIG. 8

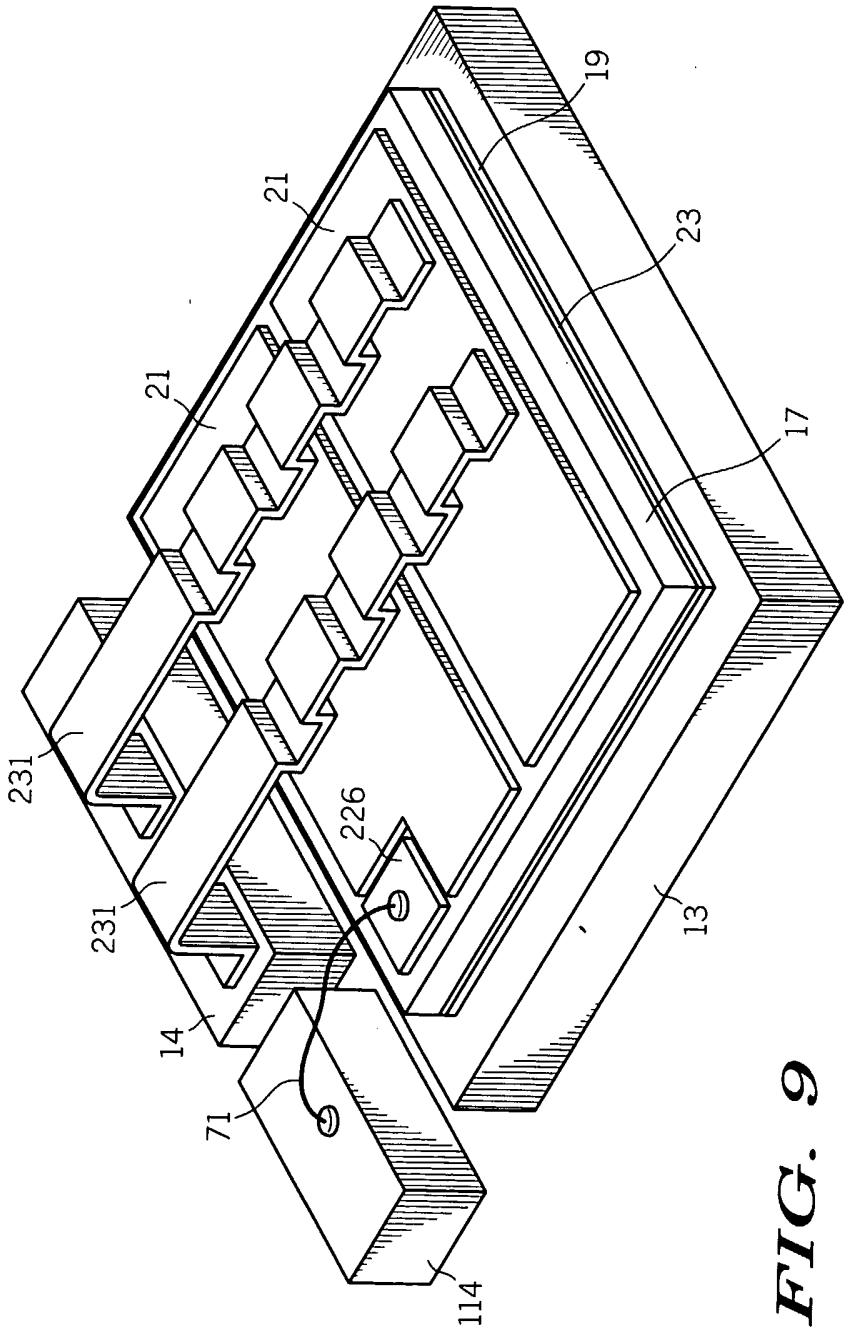


FIG. 9

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/043076

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/495 H01L23/31

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 630 726 B1 (CROWLEY SEAN T ET AL) 7 October 2003 (2003-10-07) figures 1,4	15, 17-19, 21,23-26 1-14,16, 20,22,27
Y	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 12, 5 December 2003 (2003-12-05) & JP 2004 277572 A (RENESAS TECHNOLOGY CORP), 7 October 2004 (2004-10-07) abstract	1,3, 5-14,20, 27
Y	US 2001/033022 A1 (EWER PETER R) 25 October 2001 (2001-10-25) the whole document	2,4,16, 22

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2005	26/09/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Cortes Rosa, Joao

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2004/043076

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 372 539 B1 (BAYAN JAIME ET AL) 16 April 2002 (2002-04-16) the whole document	1
A	US 2003/082854 A1 (KASAHARA TETSUICHIRO ET AL) 1 May 2003 (2003-05-01) the whole document	15,21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2004/043076

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6630726	B1	07-10-2003	US	6873041 B1	29-03-2005
JP 2004277572	A	07-10-2004	NONE		
US 2001033022	A1	25-10-2001	AU	5541801 A	07-11-2001
			TW	517371 B	11-01-2003
			WO	0182373 A1	01-11-2001
US 6372539	B1	16-04-2002	NONE		
US 2003082854	A1	01-05-2003	CN	1414629 A	30-04-2003
			JP	2003133499 A	09-05-2003
			TW	222730 B	21-10-2004